SIDDHI SINGH

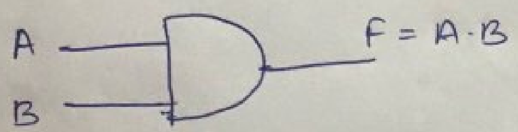
17BIT0028

BASIC LOGIC GATES (Exp-1)

Q. Verify the truth tables for AND, OR, NOT, XOR, XNOR

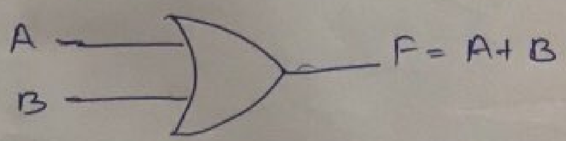
a) AND

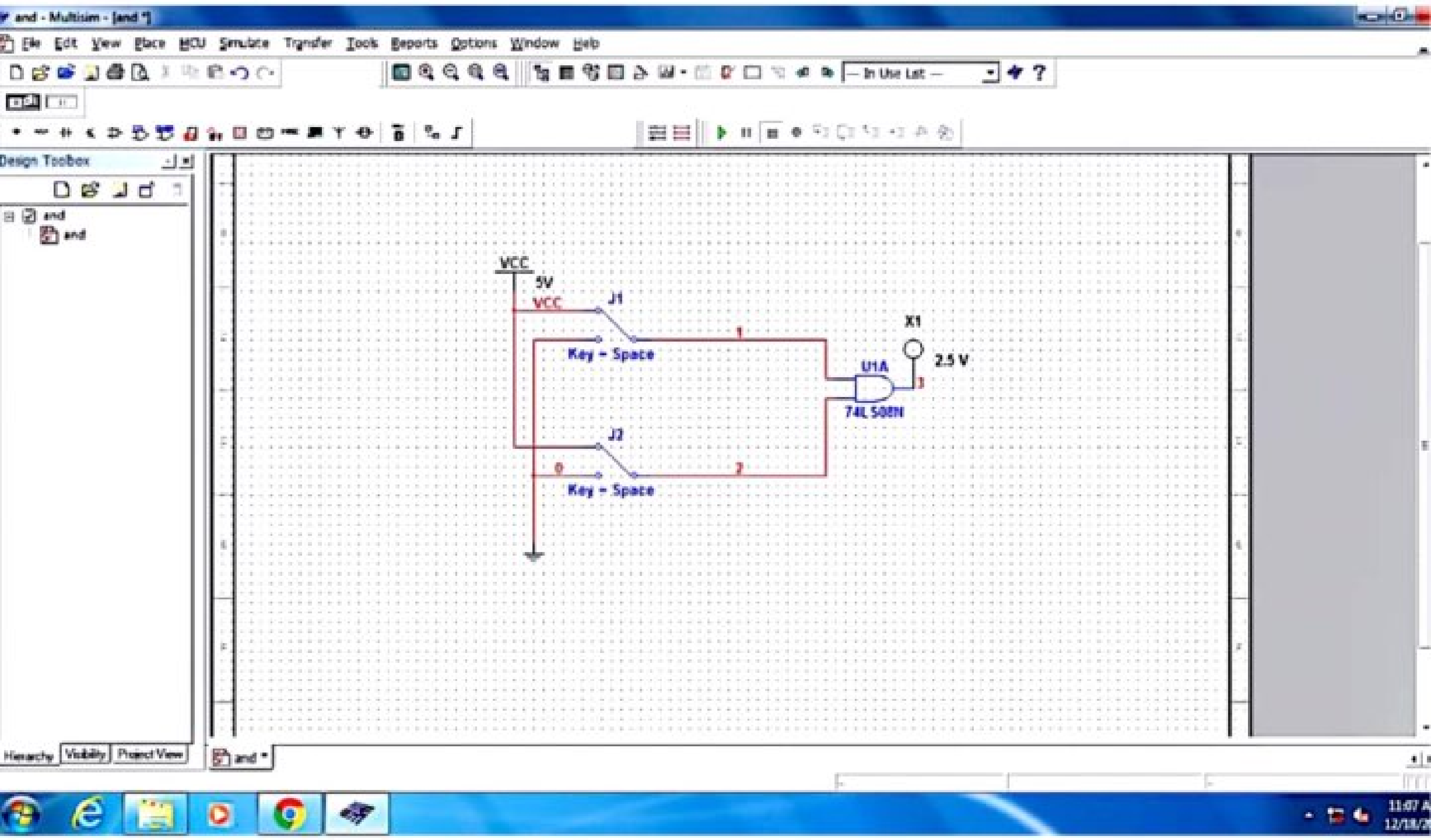
A	B	A·B
0	0	0
0	1	0
1	0	0
1	1	1



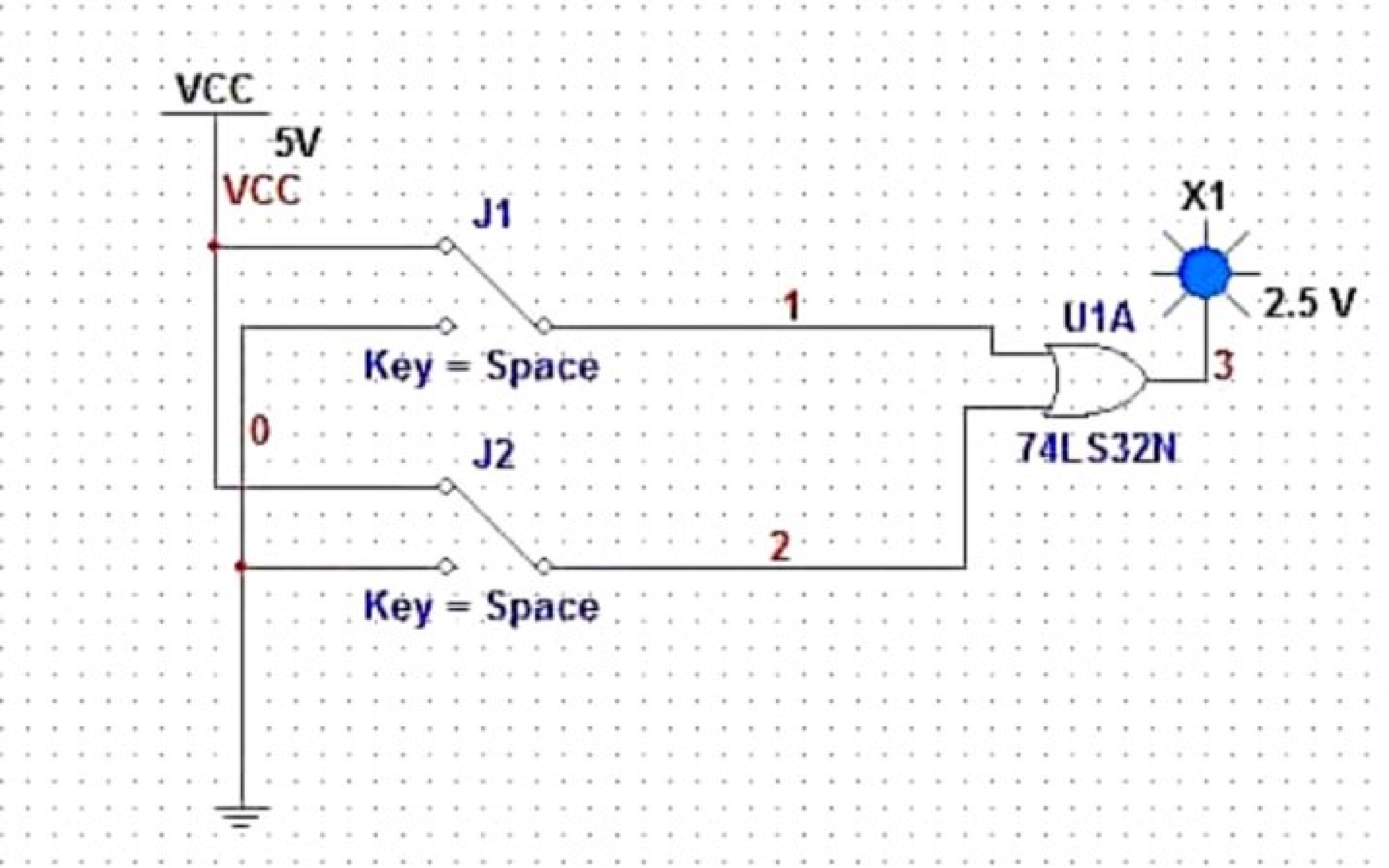
b) OR

A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1



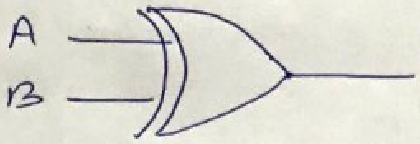


and - Multisim - [and *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
VCC
5V
VCC
J1
Key = Space
1
X1
2.5 V
U1A
74LS08N
J2
0
2
Key = Space


VCC
5V
VCC
J1
X1
1
U1A
2.5 V
Key = Space
3
0
J2
74LS32N
2
Key = Space

c) XOR ($A \oplus B$)

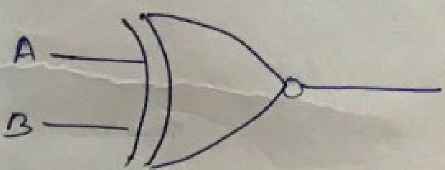
A	$\bar{A}$	B	$\bar{B}$	$A\bar{B}$	$\bar{A}B$	$A\bar{B} + \bar{A}B$
0	1	0	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	0	1	0	0	0	0



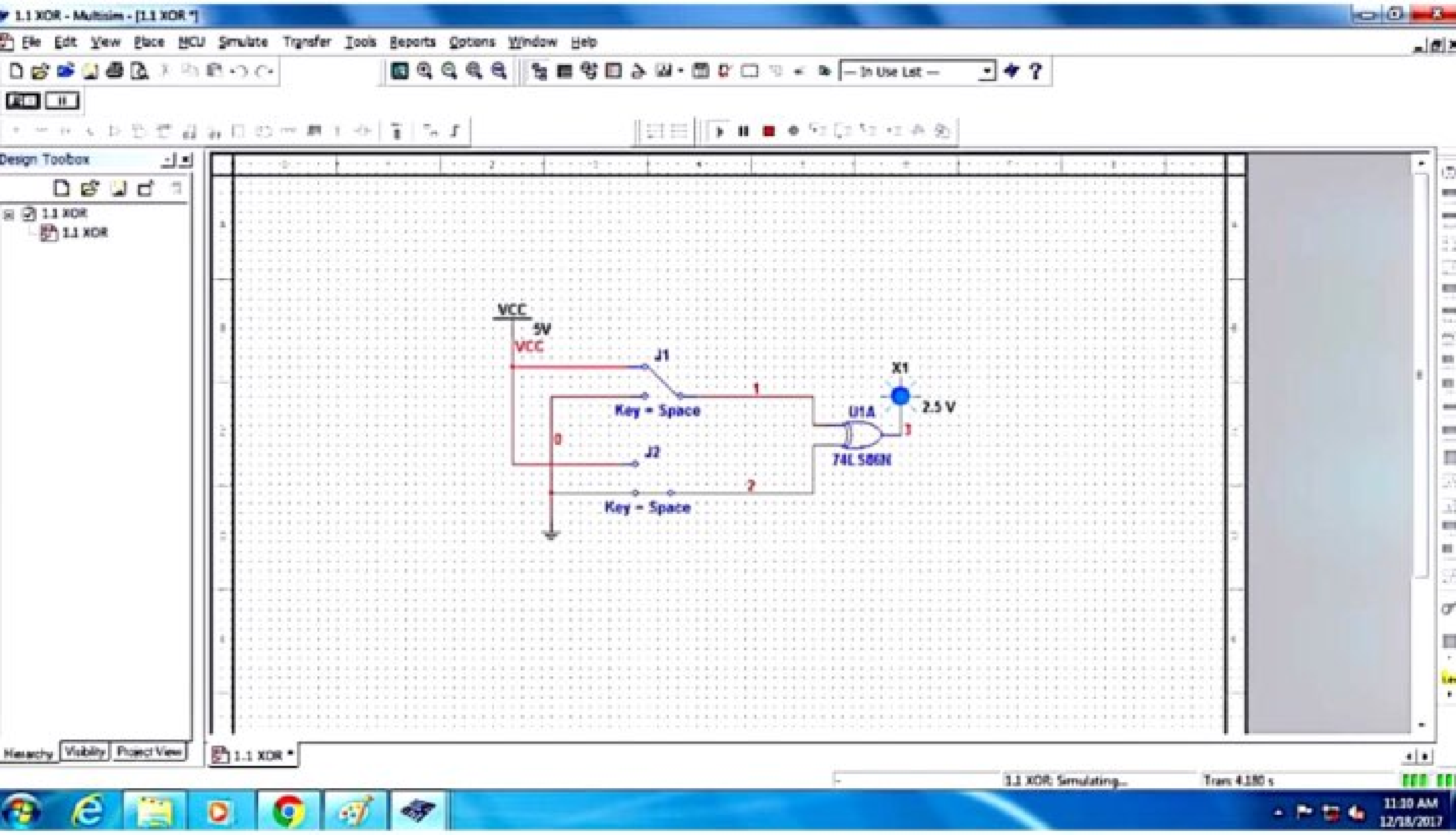
$F = A \oplus B$

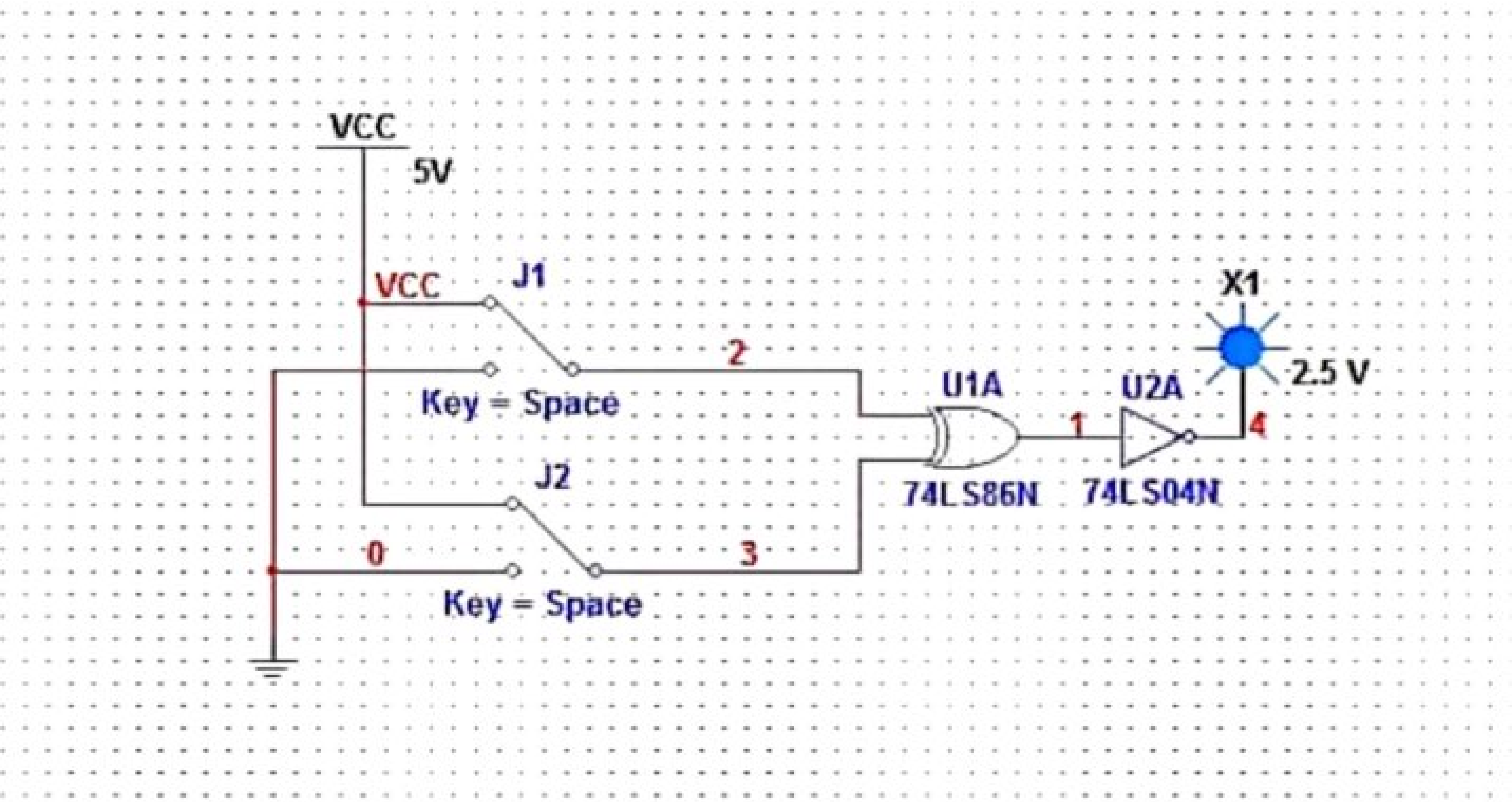
d) XNOR ($\overline{A \oplus B}$)

A	B	$A \oplus B$	$\overline{A \oplus B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1



$F = \overline{A \oplus B}$

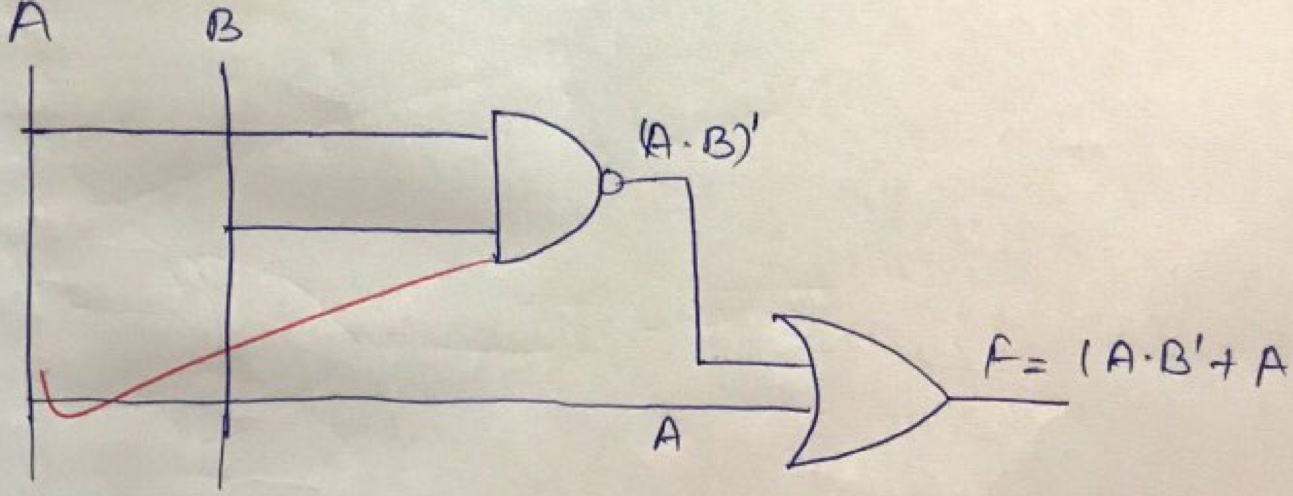

1.1 XOR - Multisim - [1.1 XOR *]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
1.1 XOR
VCC
5V
J1
Key = Space
U1A
74LS86N
X1
2.5 V
J2
Key = Space
1.1 XOR: Simulating...
11:10 AM
12/18/2017

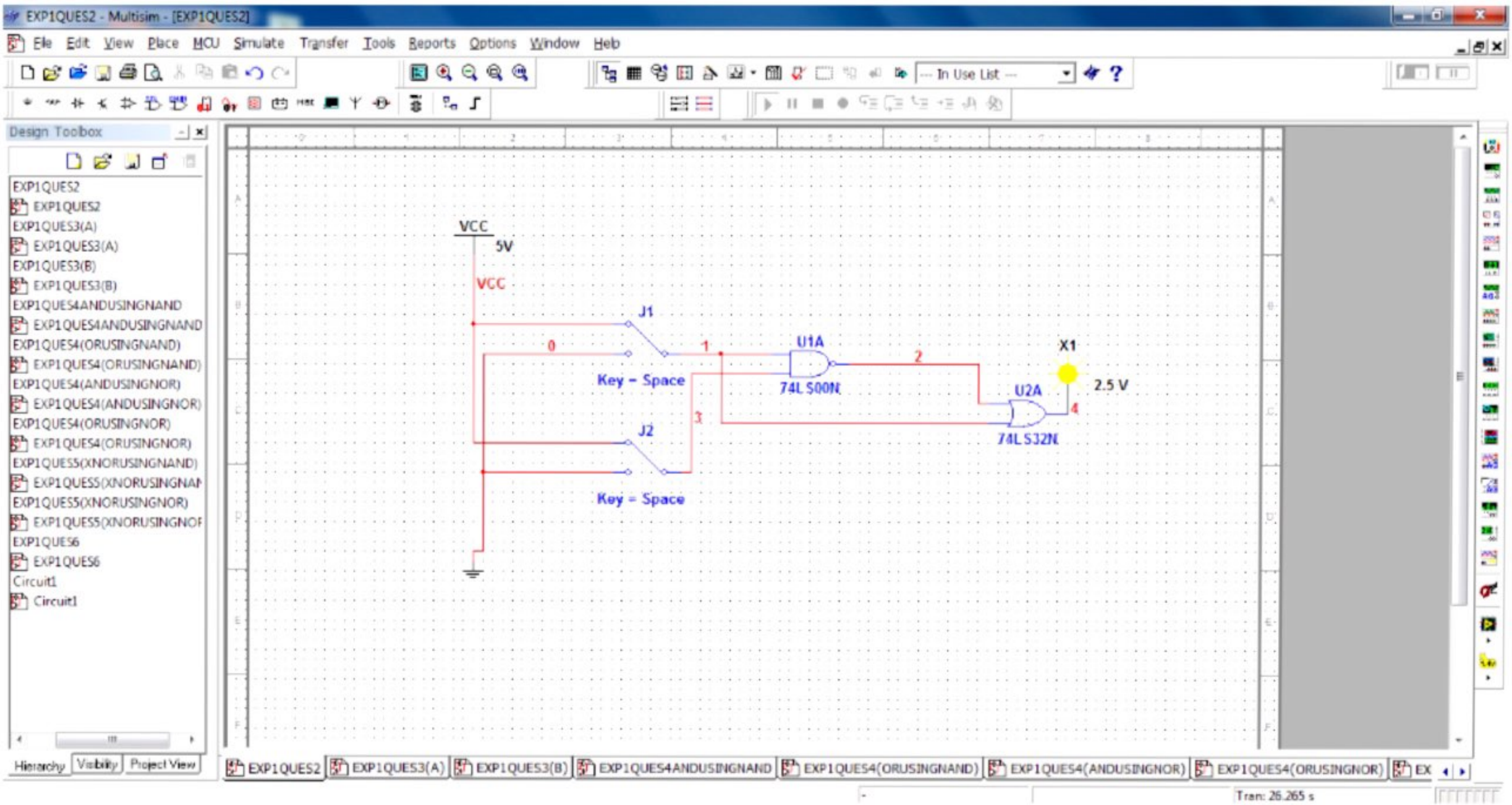

VCC
5V
VCC
J1
2
Key = Space
J2
0
3
Key = Space
U1A
74LS86N
1
U2A
74LS04N
4
X1
2.5 V

Q. Verify the expression experimentally.

$$F = ((A \cdot B)' + A)$$

A	B	A·B	(A·B)'	(A·B)' + A
0	0	0	1	1
0	1	0	1	1
1	0	0	1	1
1	1	1	0	1

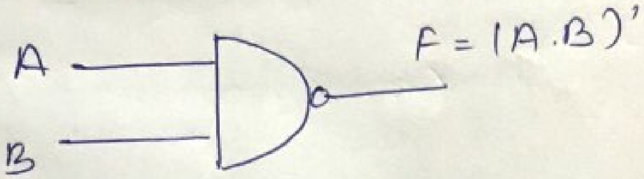



EXP1QUES2 - Multisim - [EXP1QUES2]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
EXP1QUES2
EXP1QUES3(A)
EXP1QUES3(B)
EXP1QUES4ANDUSINGNAND
EXP1QUES4(ORUSINGNAND)
EXP1QUES4(ANDUSINGNOR)
EXP1QUES4(ORUSINGNOR)
EXP1QUES5(XNORUSINGNAND)
EXP1QUES5(XNORUSINGNOR)
EXP1QUES6
Circuit1
VCC
5V
J1
Key = Space
J2
Key = Space
U1A
74LS00N
U2A
74LS32N
X1
2.5 V
Hierarchy
Visibility
Project View
Tran: 26.265 s

Q. Verify the truth tables for universal gates

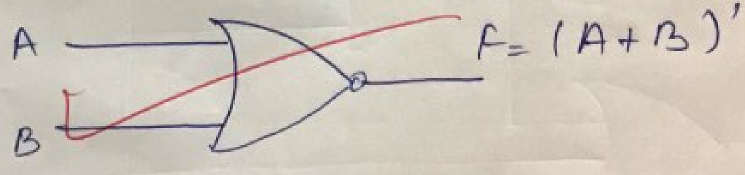
NAND Gate

A	B	A.B	(A.B)'
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

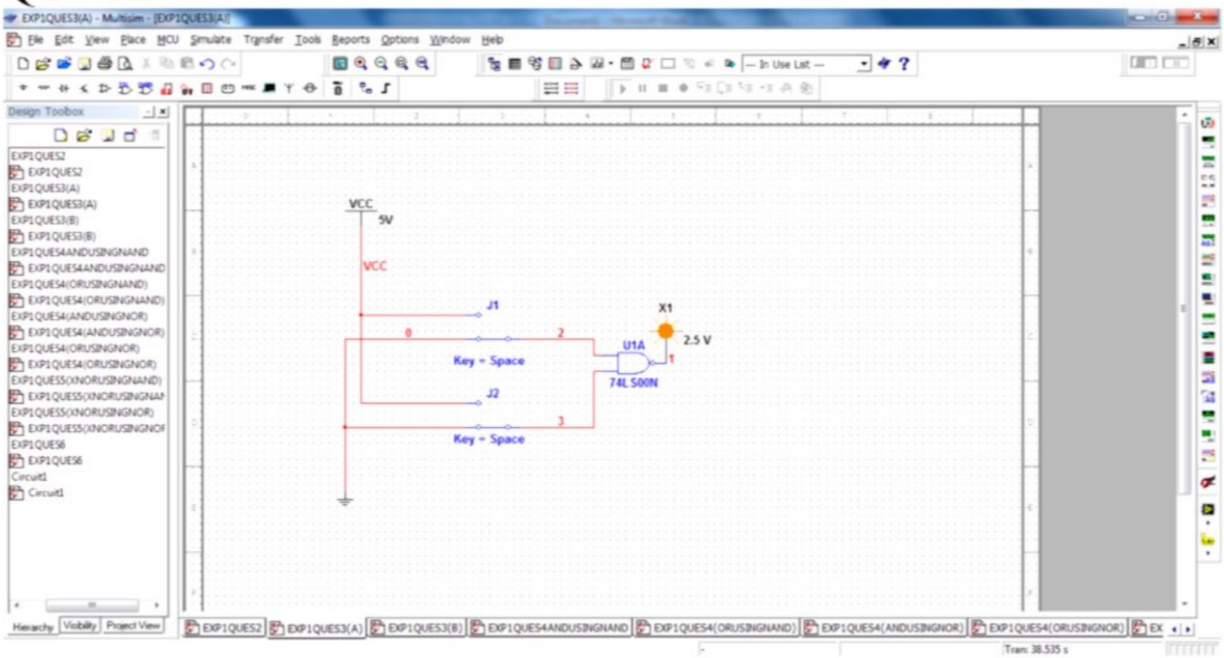


NOR Gate

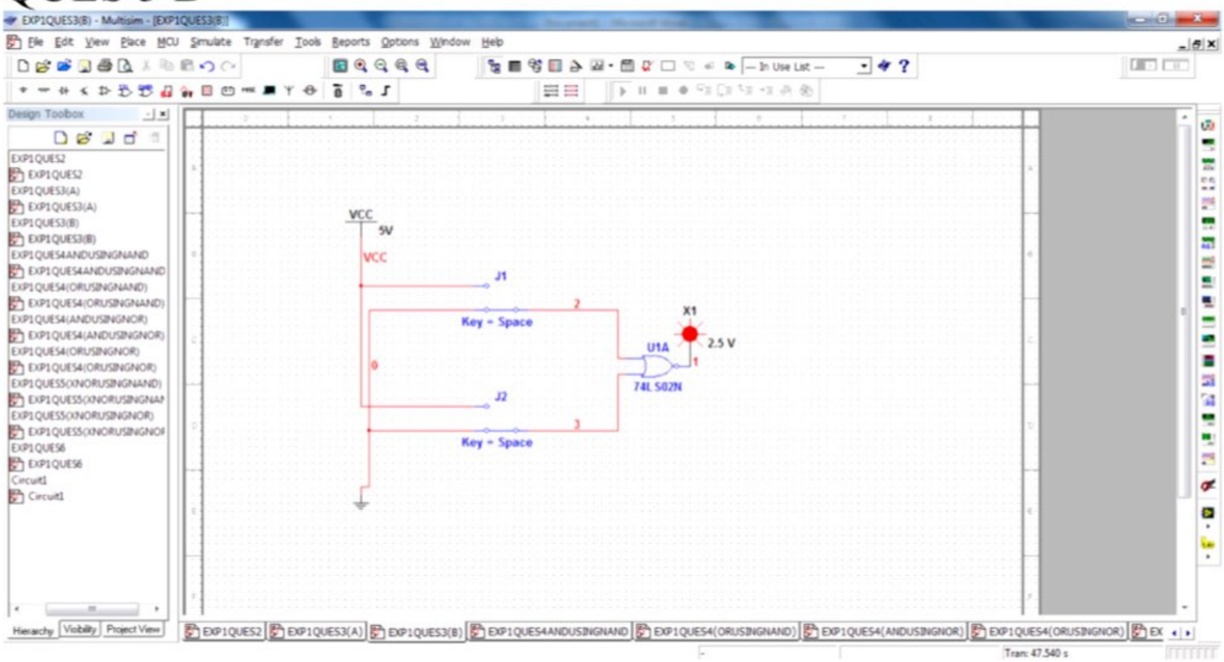
A	B	A+B	(A+B)'
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0



QUES 3 A.



QUES 3 B

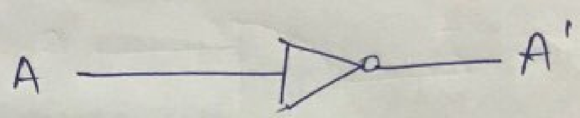


EXP1QUES3(B) - Multisim - [EXP1QUES3(B)]
File Edit View Place MCU Simulate Transfer Tools Reports Options Window Help
Design Toolbox
VCC
5V
J1
Key = Space
J2
Key = Space
X1
2.5 V
U1A
74LS02N

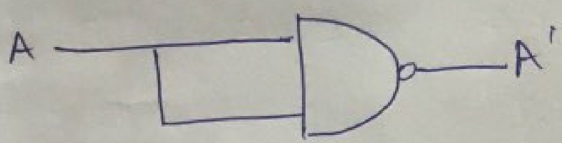
Q. Use universal gates (NAND & NOR) to formulate other basic logic gates & demonstrate the equivalence between them.

NOT GATE

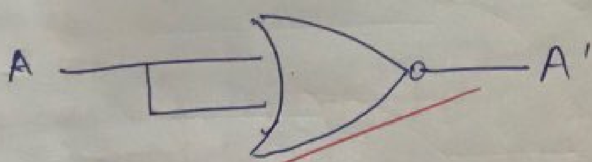
A	$\bar{A}$
0	1
1	0



* Equivalence using NAND Gate

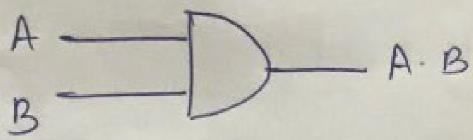


* Equivalence using NOR Gate

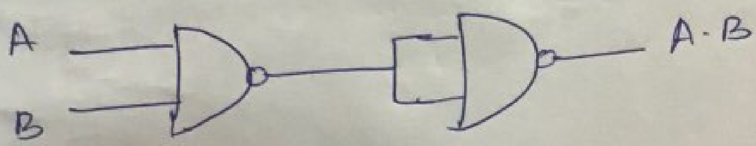


AND GATE

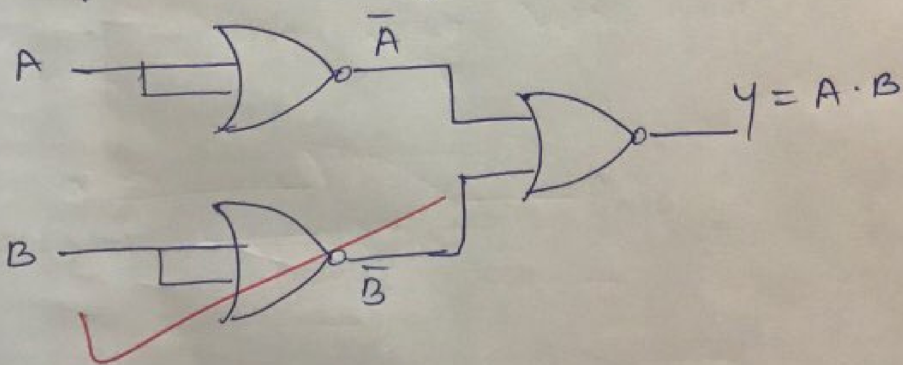
A	B	A·B
0	0	0
0	1	0
1	0	0
1	1	1



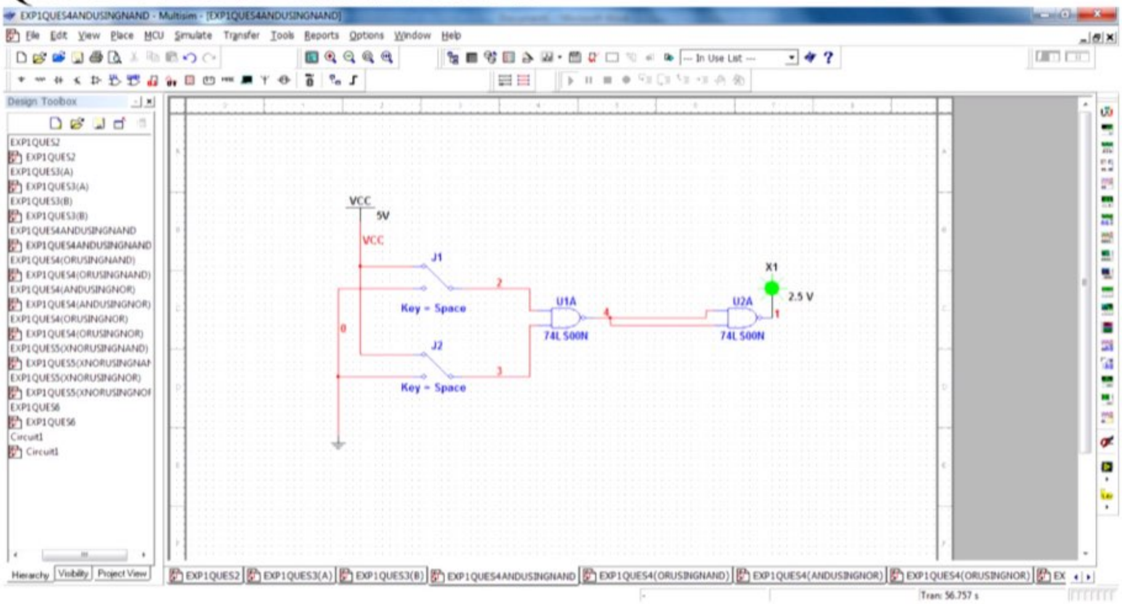
Equivalence using NAND Gate



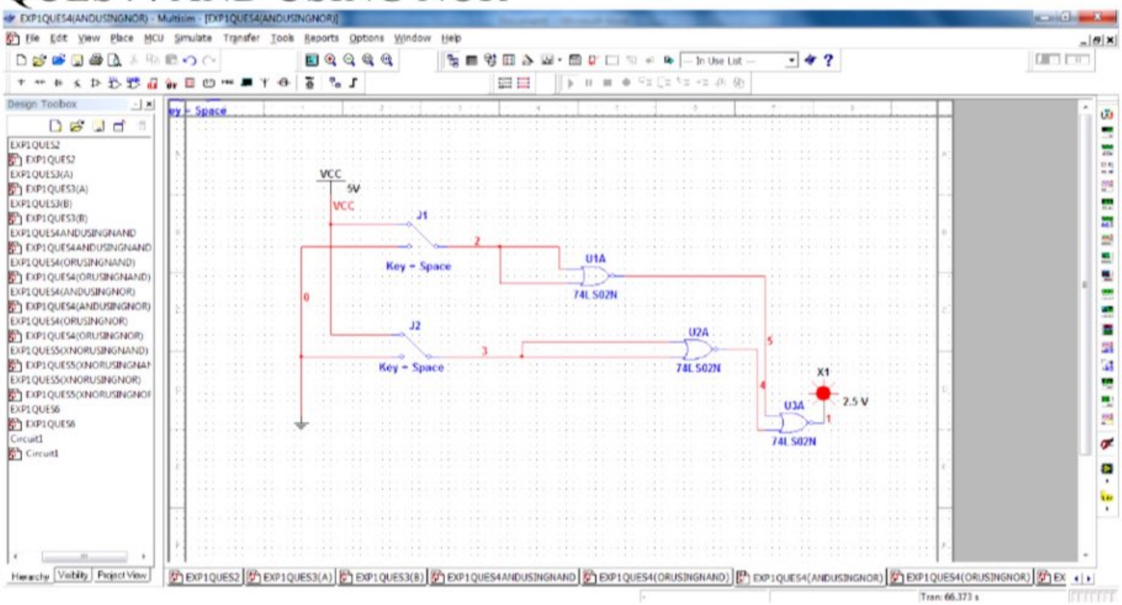
Equivalence using NOR Gate



QUES 4 : AND USING NAND

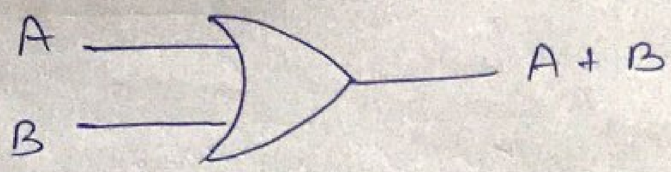


QUES4 : AND USING NOR

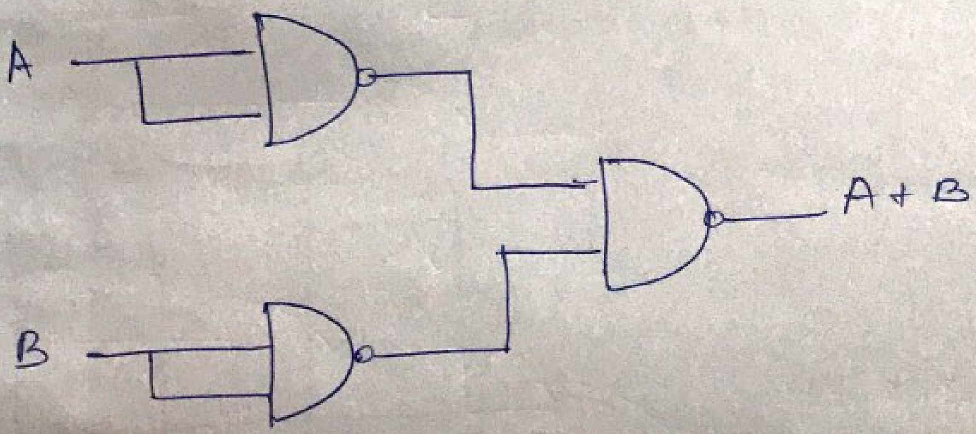


OR GATE

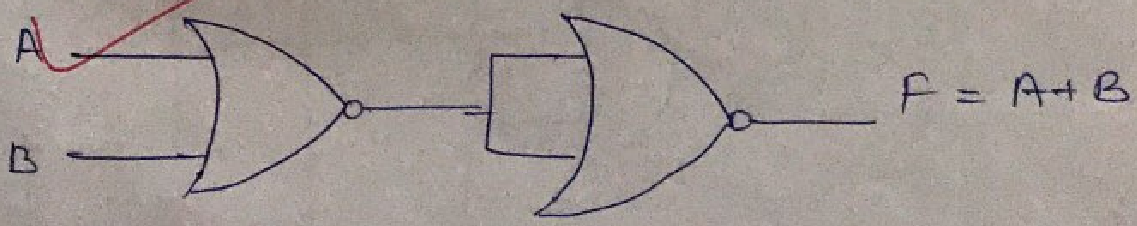
A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1



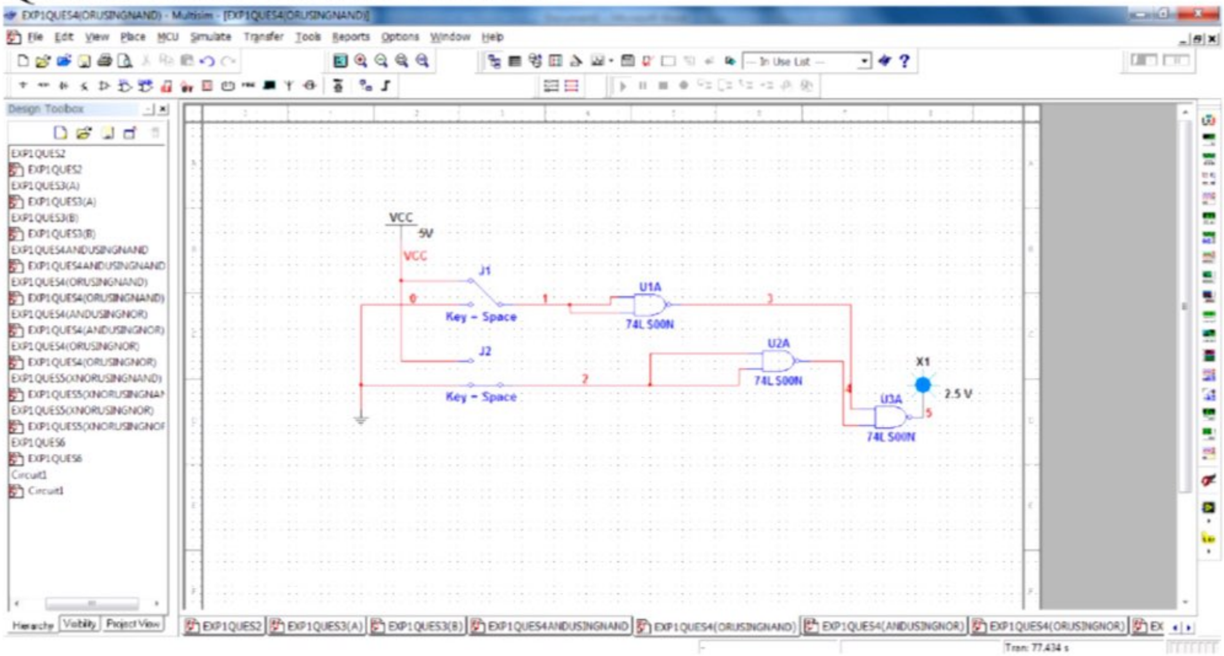
Equivalence using NAND Gate



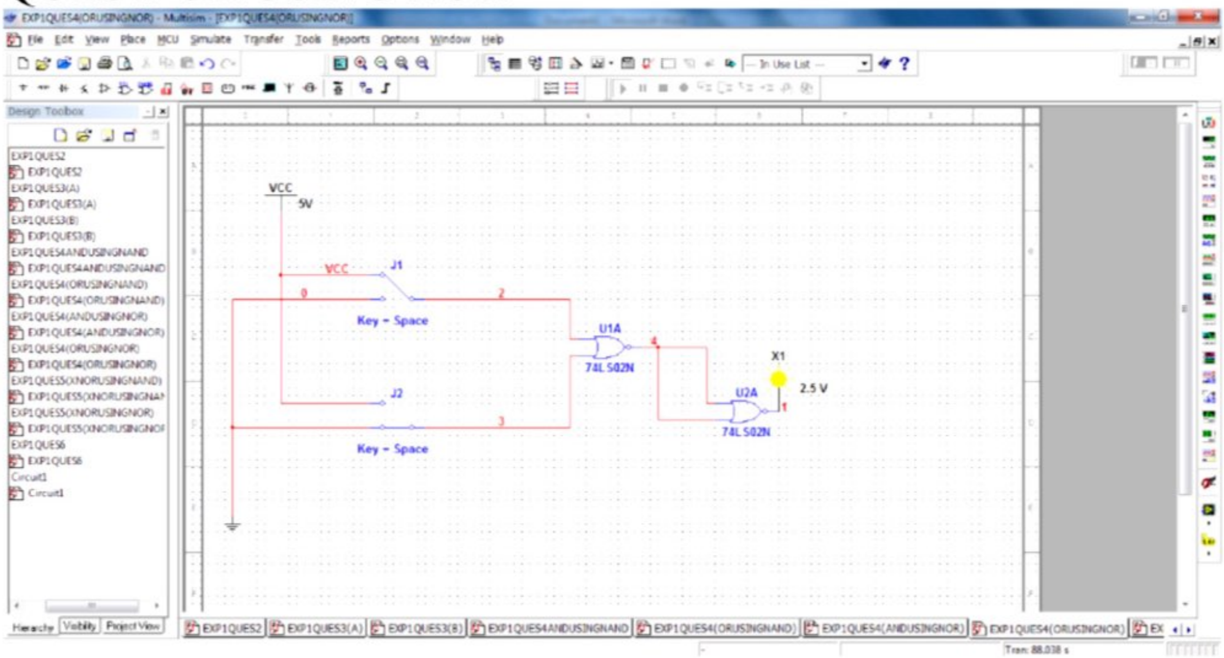
Equivalence using NOR Gate



QUES 4: OR USING NAND



QUES4: OR USING NOR

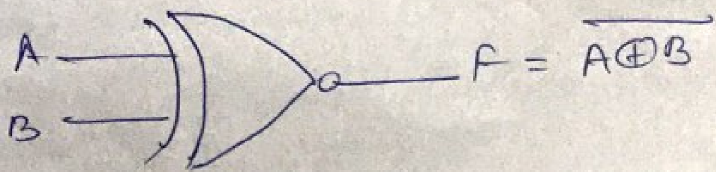


Scanned by CamScanner

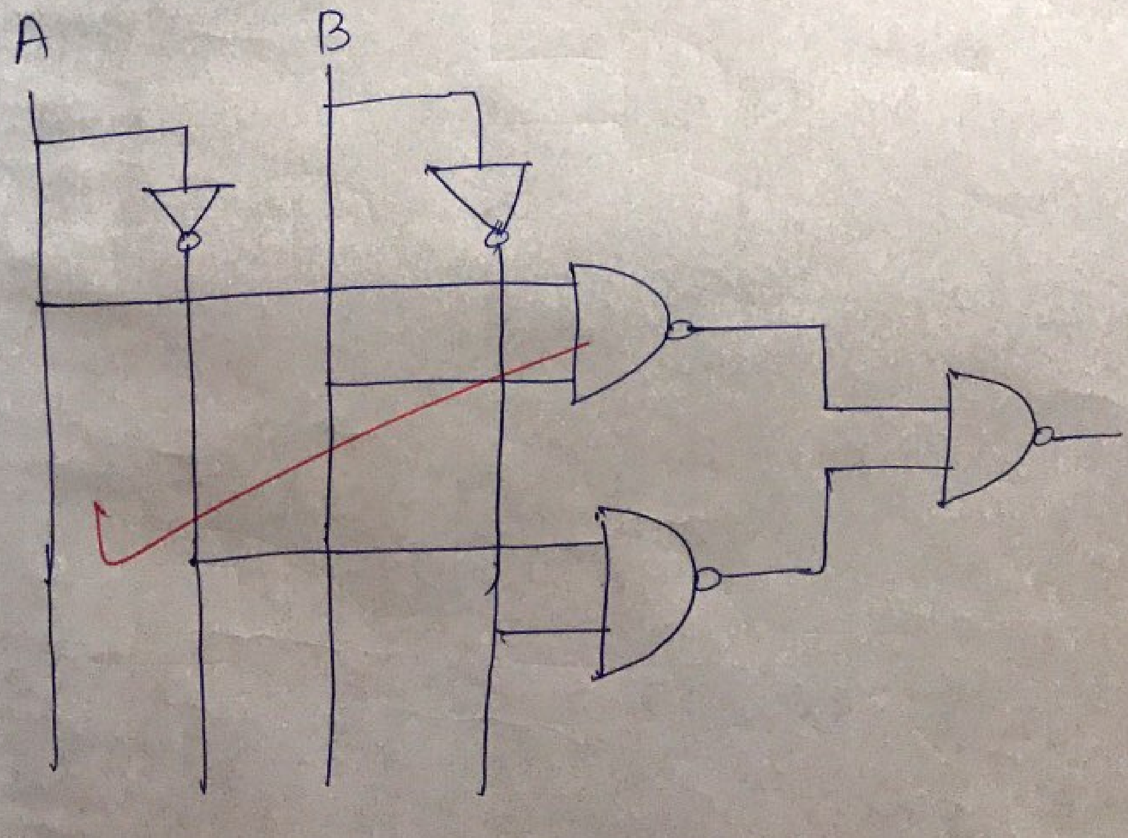
Q. Implement XNOR Gate using NAND gate and represent its implementation using NOR gate

XNOR

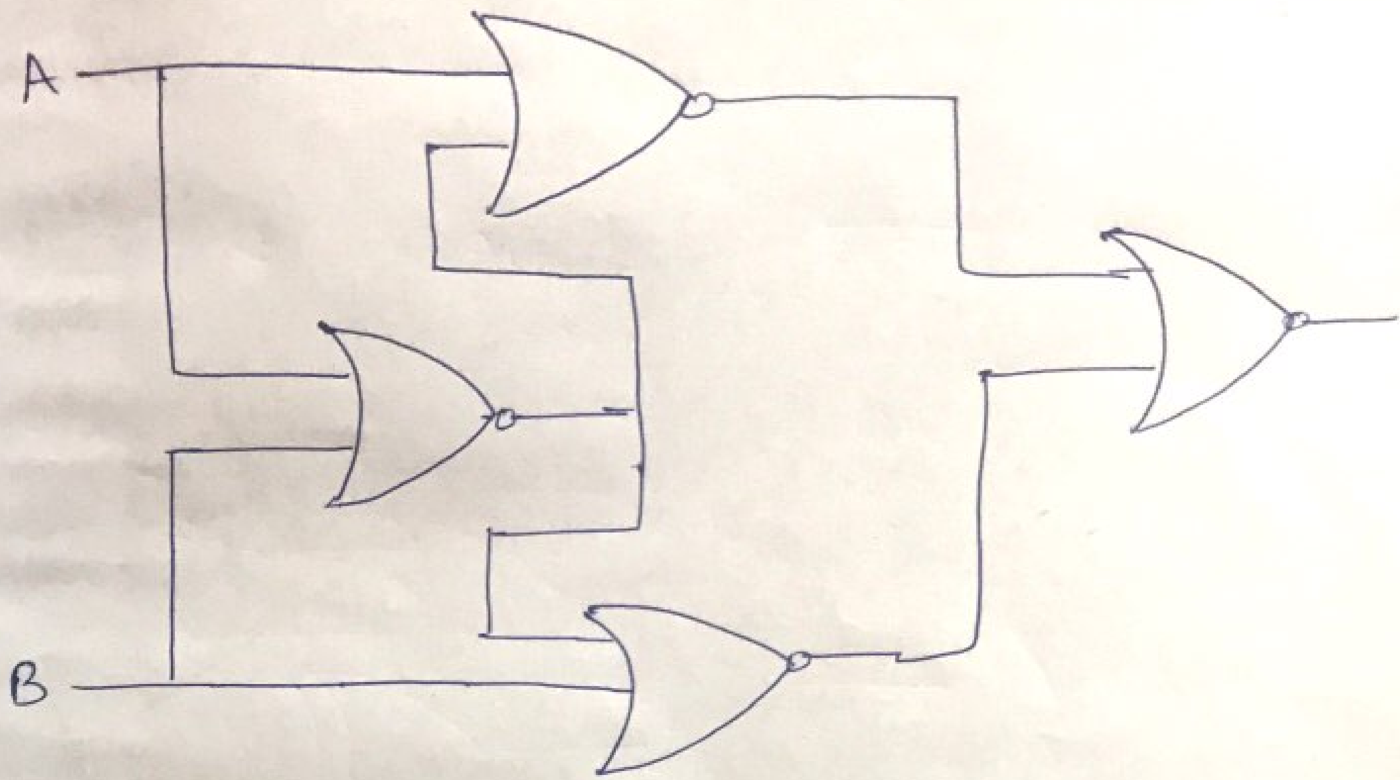
A	B	$A \oplus B$	$\overline{A \oplus B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1



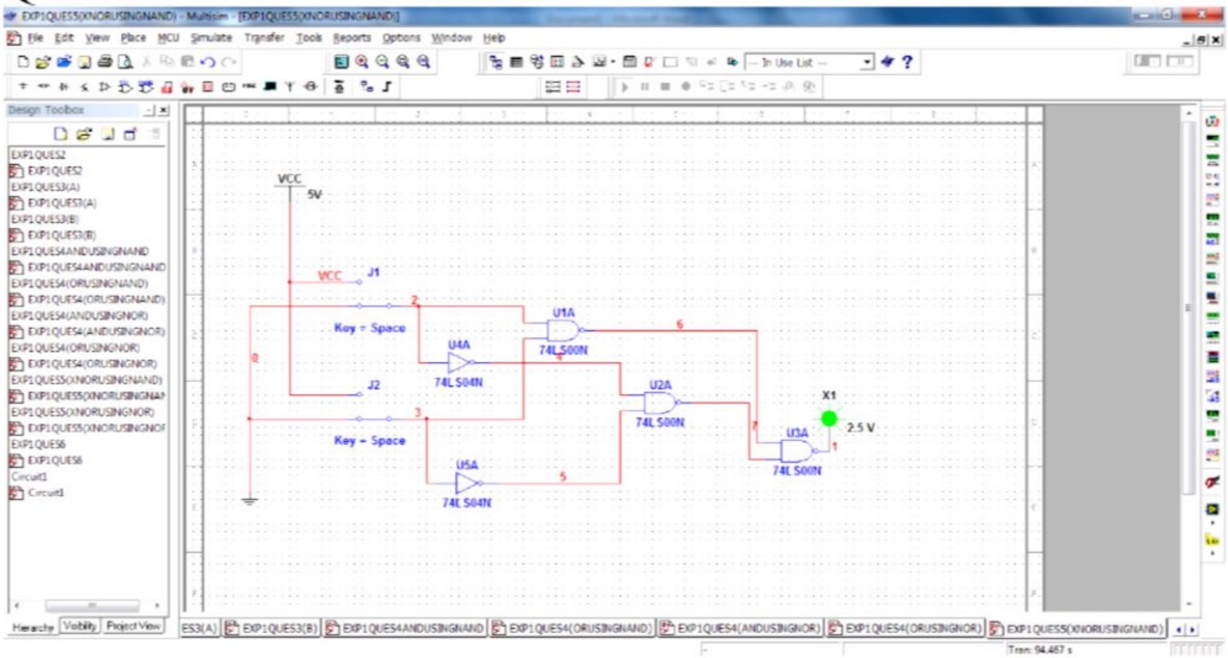
XNOR gate using NAND gate



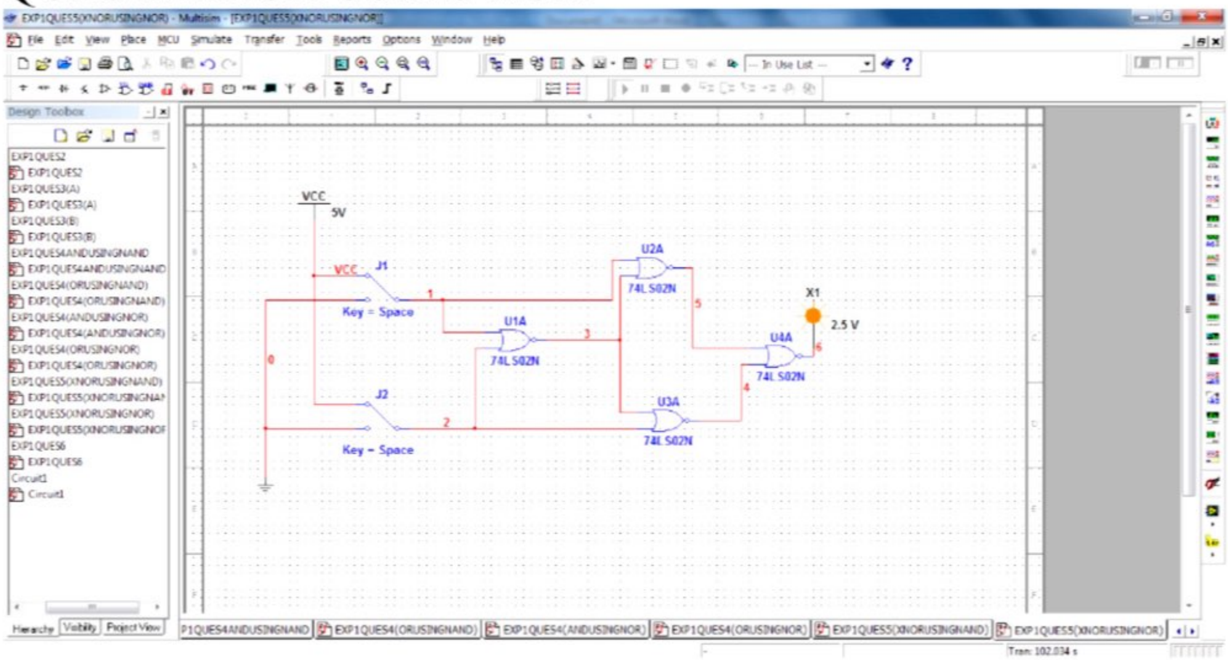
XNOR gate using NOR gate



QUES 5: XNOR USING NAND



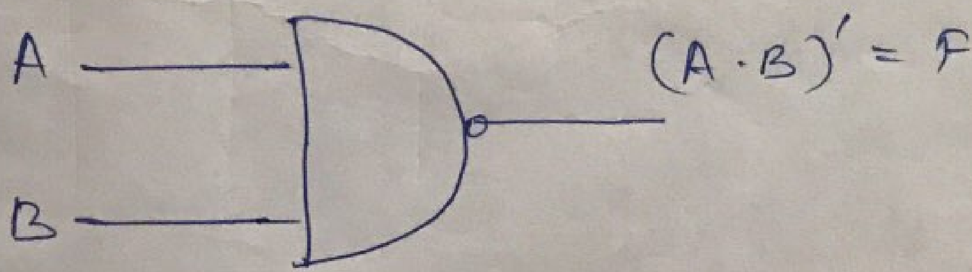
QUES 5: XNOR USING NOR



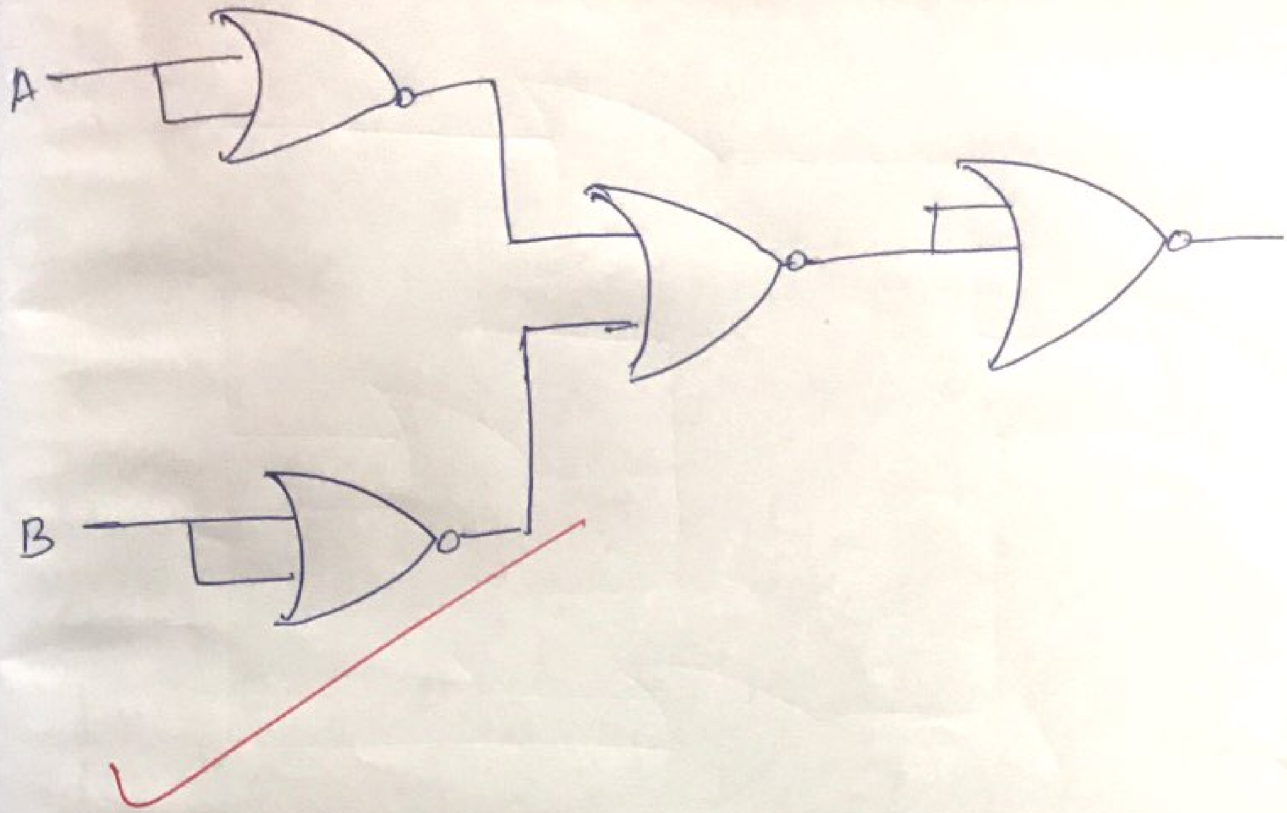
Q. Implement NAND using NOR gate

NAND Gate

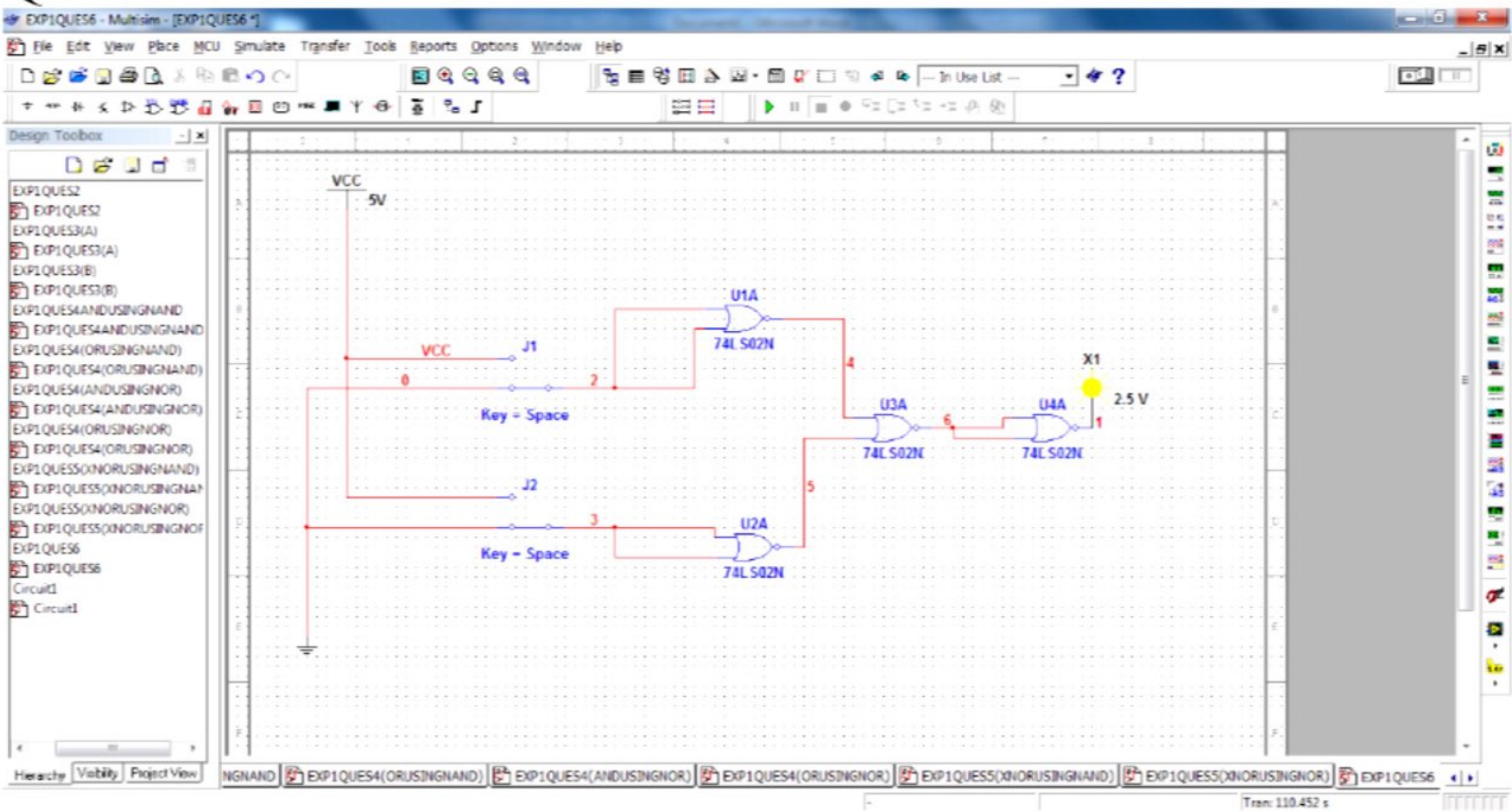
A	B	A·B	(A·B)'
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



NAND using NOR gates

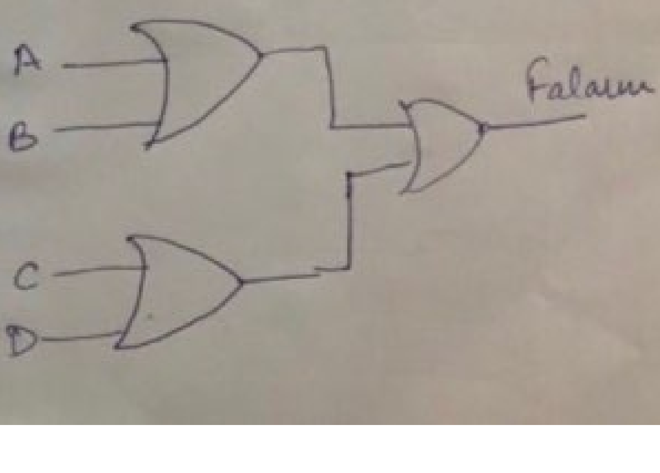


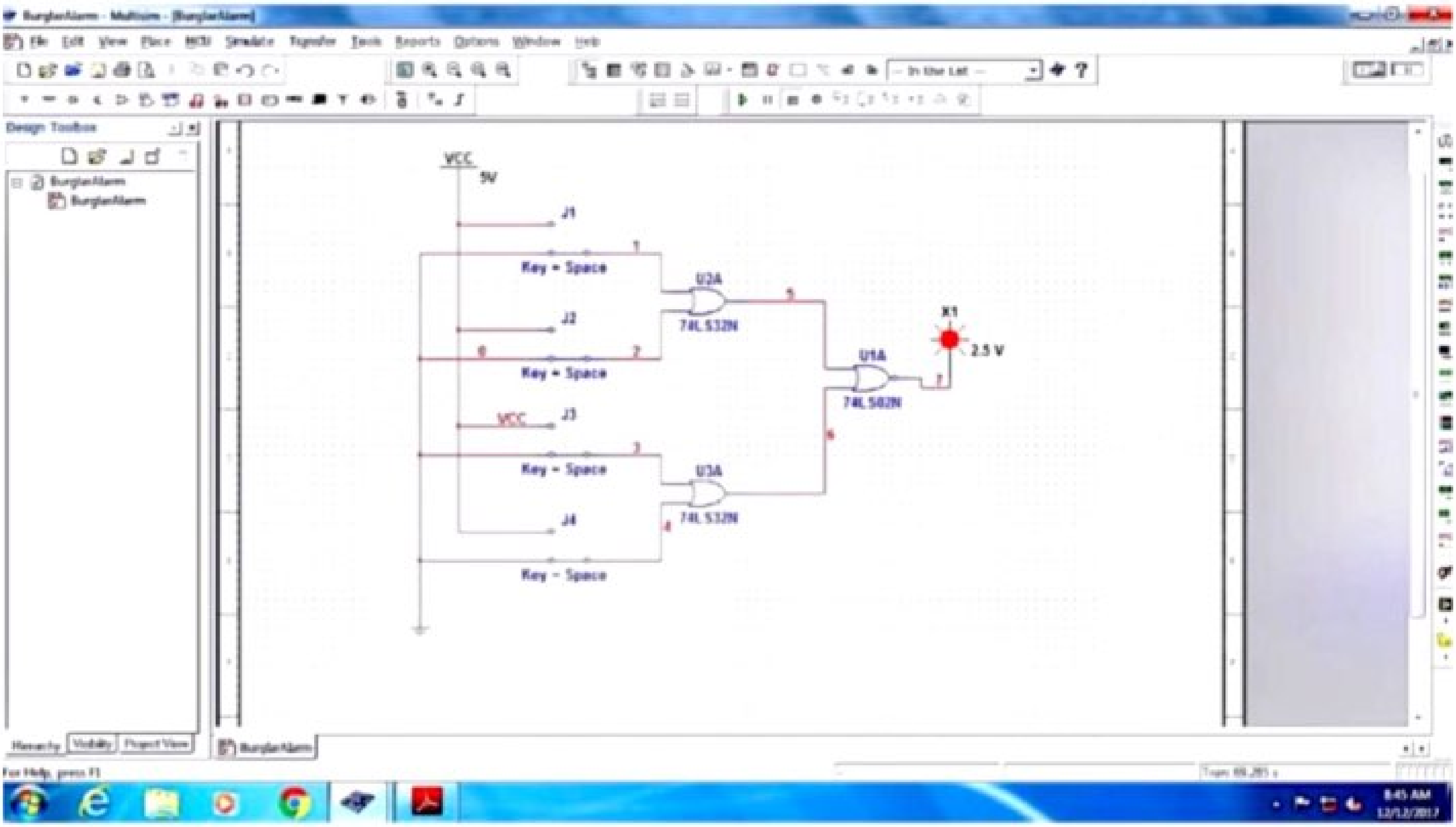
QUES 6


EXP1QUES6 - Multisim - [EXP1QUES6 *]
VCC
5V
VCC
J1
Key = Space
J2
Key = Space
U1A
74LS02N
U2A
74LS02N
U3A
74LS02N
U4A
74LS02N
X1
2.5 V
Tran: 110.452 s

Q A burglar alarm for a car has a normally LOW (grounded) switch on each of four doors. If any door is opened, the output of that switch goes HIGH. The alarm is set off with an active-LOW output. What type of gate will provide this logic?

A	B	C	D	Falarm
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0





BurglarAlarm - Multisim - [BurglarAlarm]
VCC
5V
J1
Key = Space
U2A
74LS32N
J2
Key = Space
X1
2.5 V
U1A
74LS08N
VCC
J3
Key = Space
U3A
74LS32N
J4
Key = Space

Combinational Circuits

Q. Design a combinational circuit which takes a three bit input number and generate a six-bit output which is the square of the given input number.

A	B	C	O_1	O_2	O_3	O_4	O_5	O_6
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0	1

$O_1 = \Sigma(6, 7)$

A \ BC	$\bar{B}\bar{C}$ 00	$\bar{B}C$ 01	BC 11	$B\bar{C}$ 10
$\bar{A}$ 0	0	1	3	2
A 1	4	5	1 (7)	1 (6)

$O_1 = AB$

$O_2 = \Sigma(4,5,7)$

$A \backslash BC$	$\bar B \bar C$	$\bar B C$	BC	$B \bar C$
$\bar A$	0	1	3	
A	1 4	1 5	1 6	7

$$O_2 = A\bar B + AC$$
$$= A(\bar B + C)$$

$O_3 = \Sigma(3,5)$

	$\bar B \bar C$	$\bar B C$	BC	$B \bar C$
$\bar A$	0	1	1 3	2
A	4	1 5	7	6

$$O_3 = \bar A BC + A\bar B C$$
$$= C(A \oplus B)$$

$O_4 = \Sigma(2,6)$

$A \backslash BC$	$\bar B \bar C$	$\bar B C$	BC	$B \bar C$
$\bar A$	0	1	3	1 2
A	4	5	7	1 6

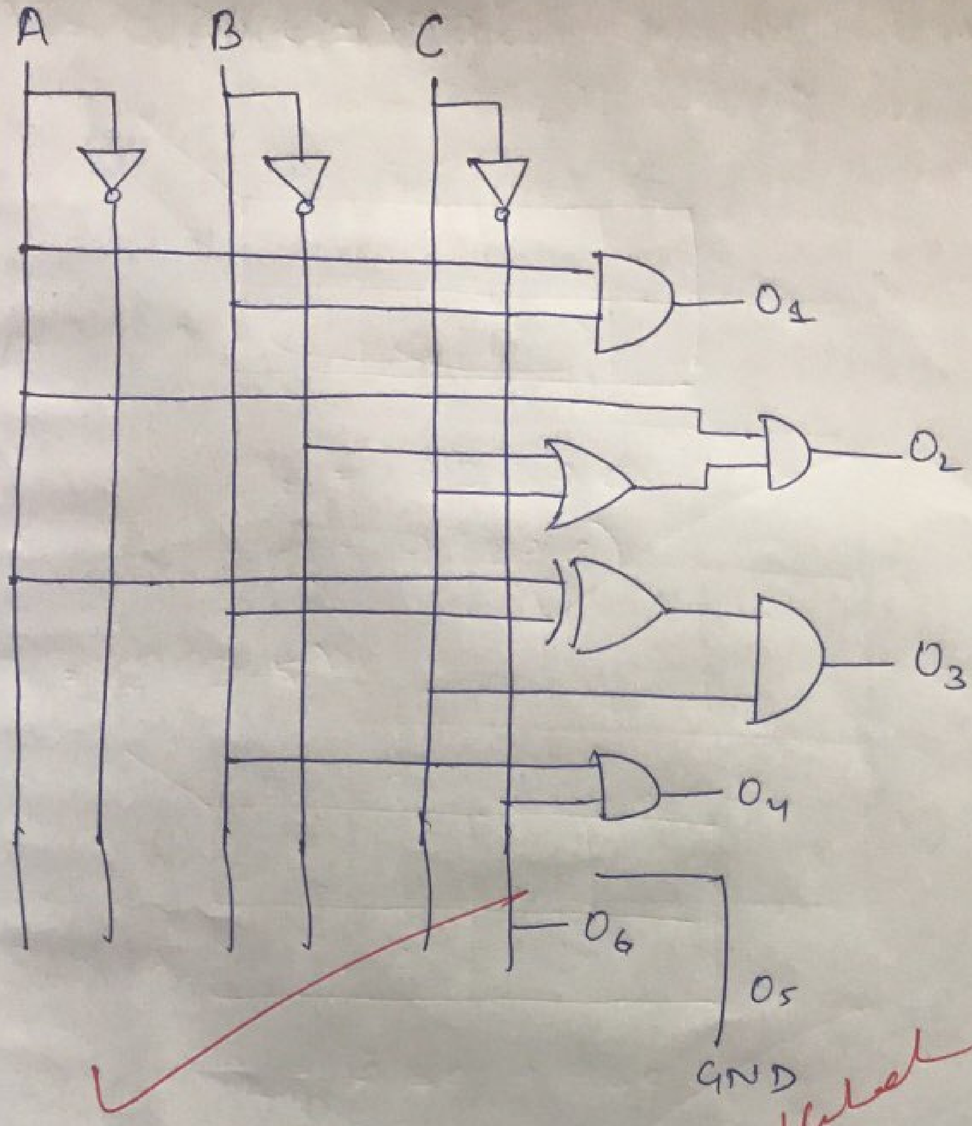
$$O_4 = B\bar C$$

$O_5 = \text{GND}$

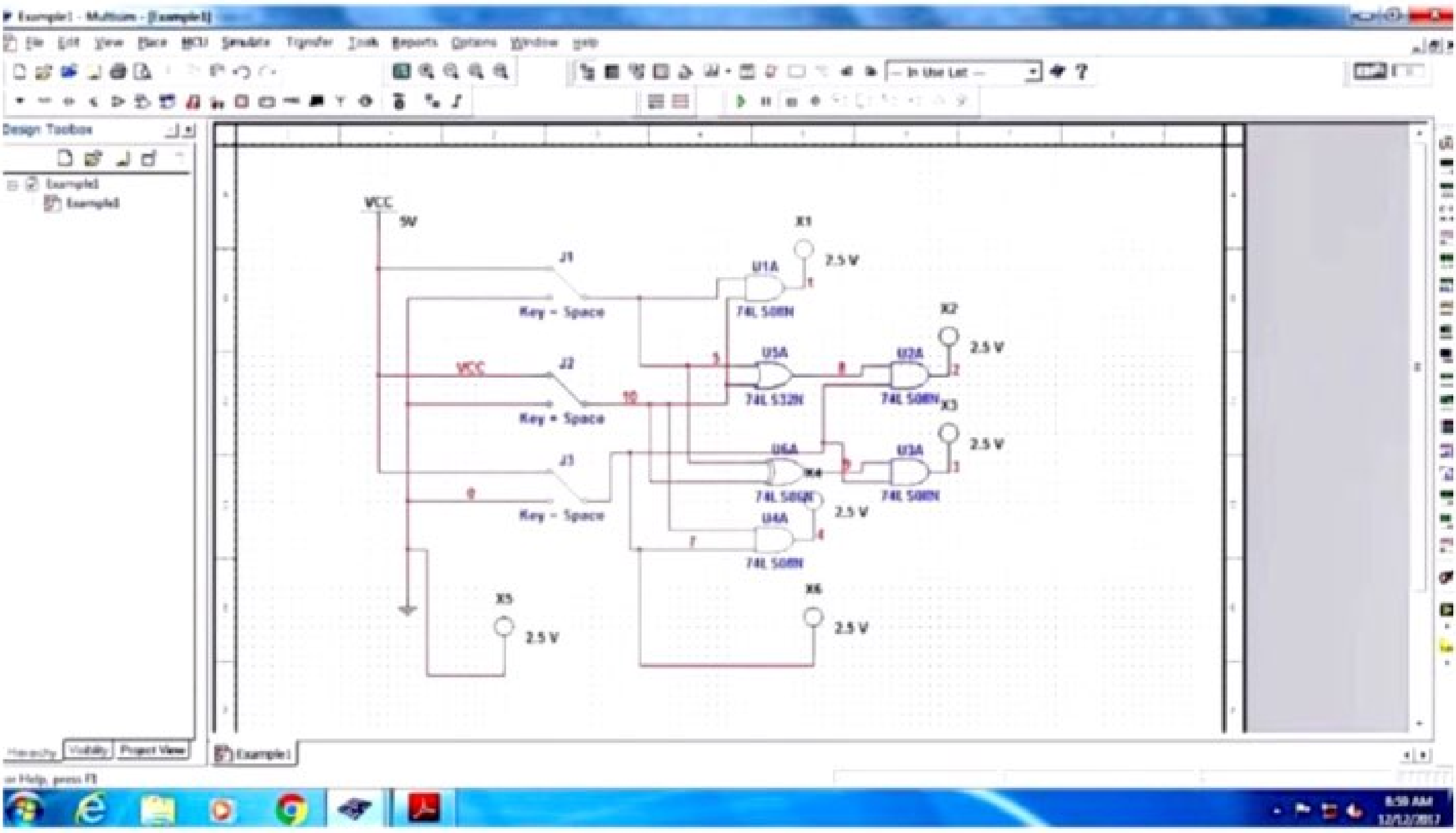
$O_6 = \Sigma(1,3,5,7)$

	$\bar B \bar C$	$\bar B C$	BC	$B \bar C$
$\bar A$	0	1 1	1 3	2
A	4	1 5	1 7	6

$O_6 = C$



21/12/2017


Example1 - Multisim - [Example1]
VCC
5V
J1
Key = Space
J2
Key = Space
J3
Key = Space
VCC
U1A
74LS08N
U5A
74LS32N
U2A
74LS08N
U6A
U3A
74LS08N
U4A
74LS08N
X1
X2
X3
X4
X5
X6
2.5 V