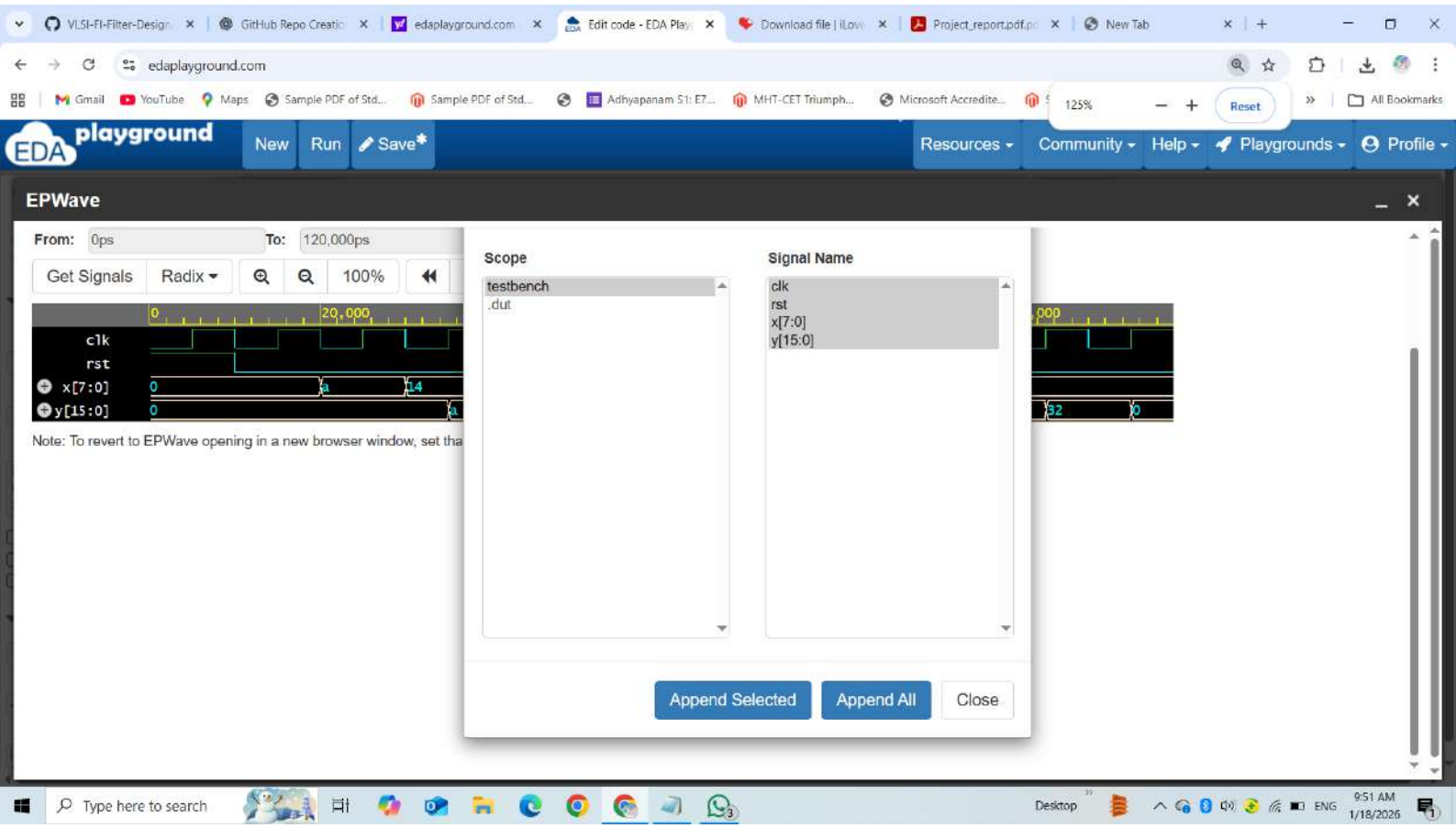
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playground
New
Run
Save*
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Profile
EPWave
From: 0ps
To: 120,000ps
Get Signals
Radix
100%
clk
rst
x[7:0]
y[15:0]
Note: To revert to EPWave opening in a new browser window, set tha
Scope
testbench
.dut
Signal Name
clk
rst
x[7:0]
y[15:0]
Append Selected
Append All
Close
Type here to search
Desktop
ENG
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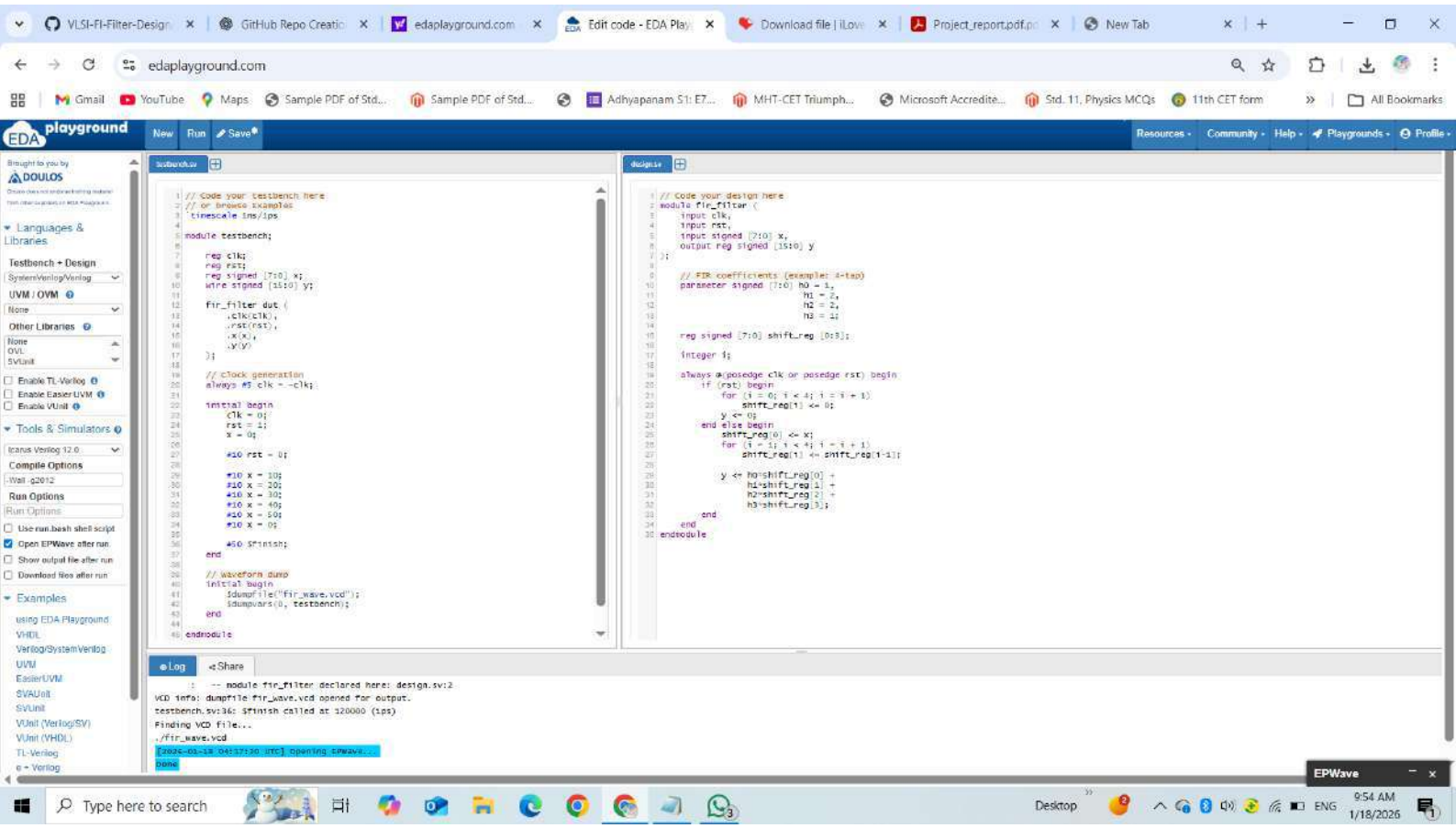
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EDA playground
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Save
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Help
Playgrounds
Profile
testbench.sv
design.sv
// Code your testbench here
// or browse Examples
`timescale 1ns/1ps
module testbench;
reg clk;
reg rst;
reg signed [7:0] x;
wire signed [15:0] y;
fir_filter dut (
.clk(clk),
.rst(rst),
.x(x),
.y(y)
);
// Clock generation
always #5 clk = ~clk;
initial begin
clk = 0;
rst = 1;
x = 0;
#10 rst = 0;
#10 x = 10;
#10 x = 20;
#10 x = 30;
#10 x = 40;
#10 x = 50;
#10 x = 0;
#50 $finish;
end
// Waveform dump
initial begin
$dumpfile("fir_wave.vcd");
$dumpvars(0, testbench);
end
endmodule
// Code your design here
module fir_filter (
input clk,
input rst,
input signed [7:0] x,
output reg signed [15:0] y
);
// FIR coefficients (example: 4-tap)
parameter signed [7:0] h0 = 1,
h1 = 2,
h2 = 2,
h3 = 1;
reg signed [7:0] shift_reg [0:3];
integer i;
always @(posedge clk or posedge rst) begin
if (rst) begin
for (i = 0; i < 4; i = i + 1)
shift_reg[i] <= 0;
y <= 0;
end else begin
shift_reg[0] <= x;
for (i = 1; i < 4; i = i + 1)
shift_reg[i] <= shift_reg[i-1];
y <= h0*shift_reg[0] +
h1*shift_reg[1] +
h2*shift_reg[2] +
h3*shift_reg[3];
end
end
endmodule
Log
Share
-- module fir_filter declared here: design.sv:2
VCD info: dumpfile fir_wave.vcd opened for output.
testbench.sv:36: $finish called at 120000 (1ps)
Finding VCD file...
./fir_wave.vcd
[2026-01-18 04:37:30 UTC] Opening EPWave...
Done
EPWave
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Testbench + Design
UVM / OVM
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Examples
Type here to search
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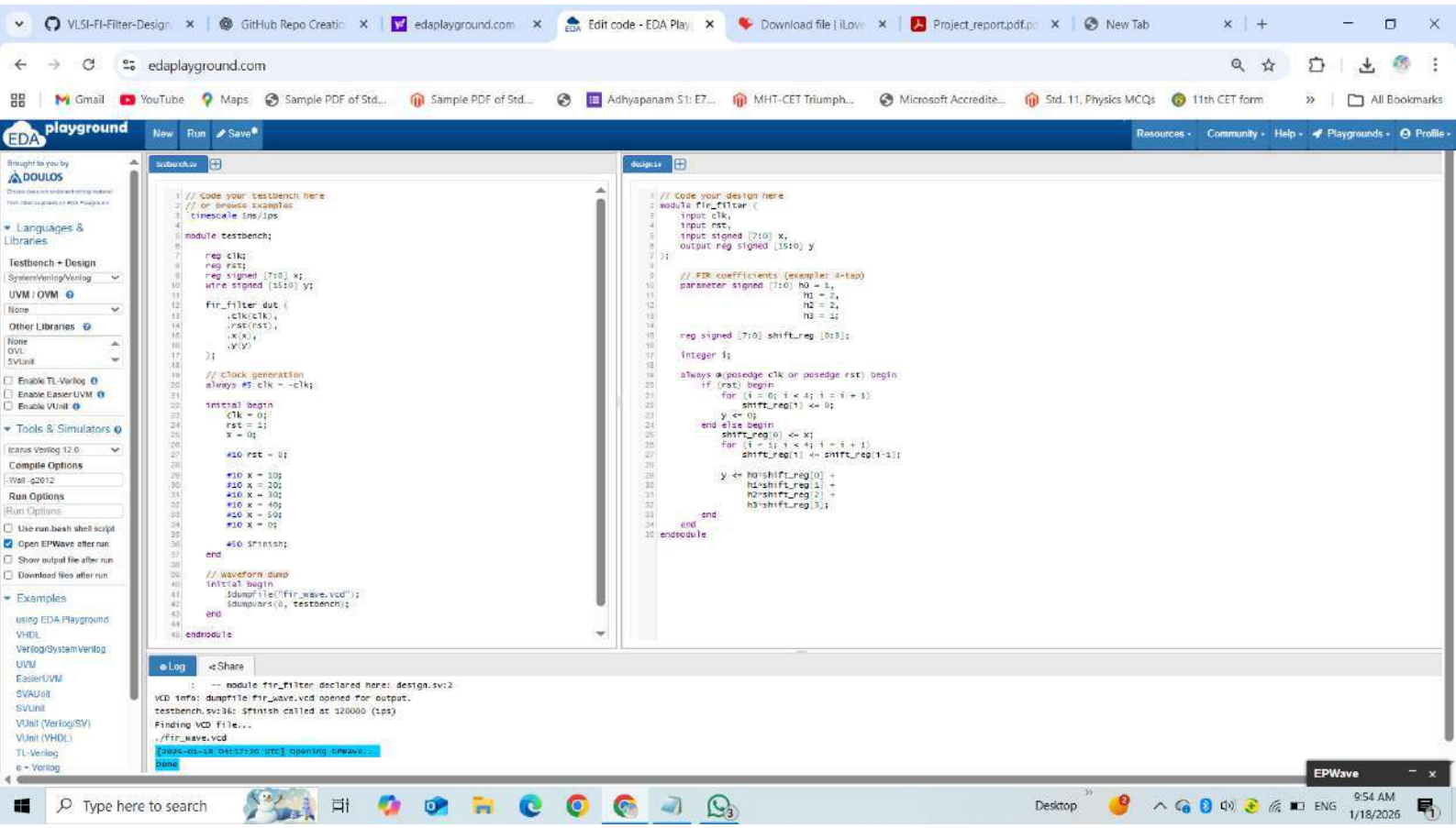
edaplayground.com
EDA playground
New
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Playgrounds
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testbench.sv
design.sv
// Code your testbench here
// or browse Examples
`timescale 1ns/1ps
module testbench;
reg clk;
reg rst;
reg signed [7:0] x;
wire signed [15:0] y;
fir_filter dut (
.clk(clk),
.rst(rst),
.x(x),
.y(y)
);
// Clock generation
always #5 clk = ~clk;
initial begin
clk = 0;
rst = 1;
x = 0;
#10 rst = 0;
#10 x = 10;
#10 x = 20;
#10 x = 30;
#10 x = 40;
#10 x = 50;
#10 x = 0;
#50 $finish;
end
// Waveform dump
initial begin
$dumpfile("fir_wave.vcd");
$dumpvars(0, testbench);
end
endmodule
// Code your design here
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input clk,
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input signed [7:0] x,
output reg signed [15:0] y
);
// FIR coefficients (example: 4-tap)
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h1 = 2,
h2 = 2,
h3 = 1;
reg signed [7:0] shift_reg [0:3];
integer i;
always @(posedge clk or posedge rst) begin
if (rst) begin
for (i = 0; i < 4; i = i + 1)
shift_reg[i] <= 0;
y <= 0;
end else begin
shift_reg[0] <= x;
for (i = 1; i < 4; i = i + 1)
shift_reg[i] <= shift_reg[i-1];
y <= h0*shift_reg[0] +
h1*shift_reg[1] +
h2*shift_reg[2] +
h3*shift_reg[3];
end
end
endmodule
Log
Share
-- module fir_filter declared here: design.sv:2
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[2026-01-18 04:37:30 UTC] Opening EPWave...
Done
EPWave
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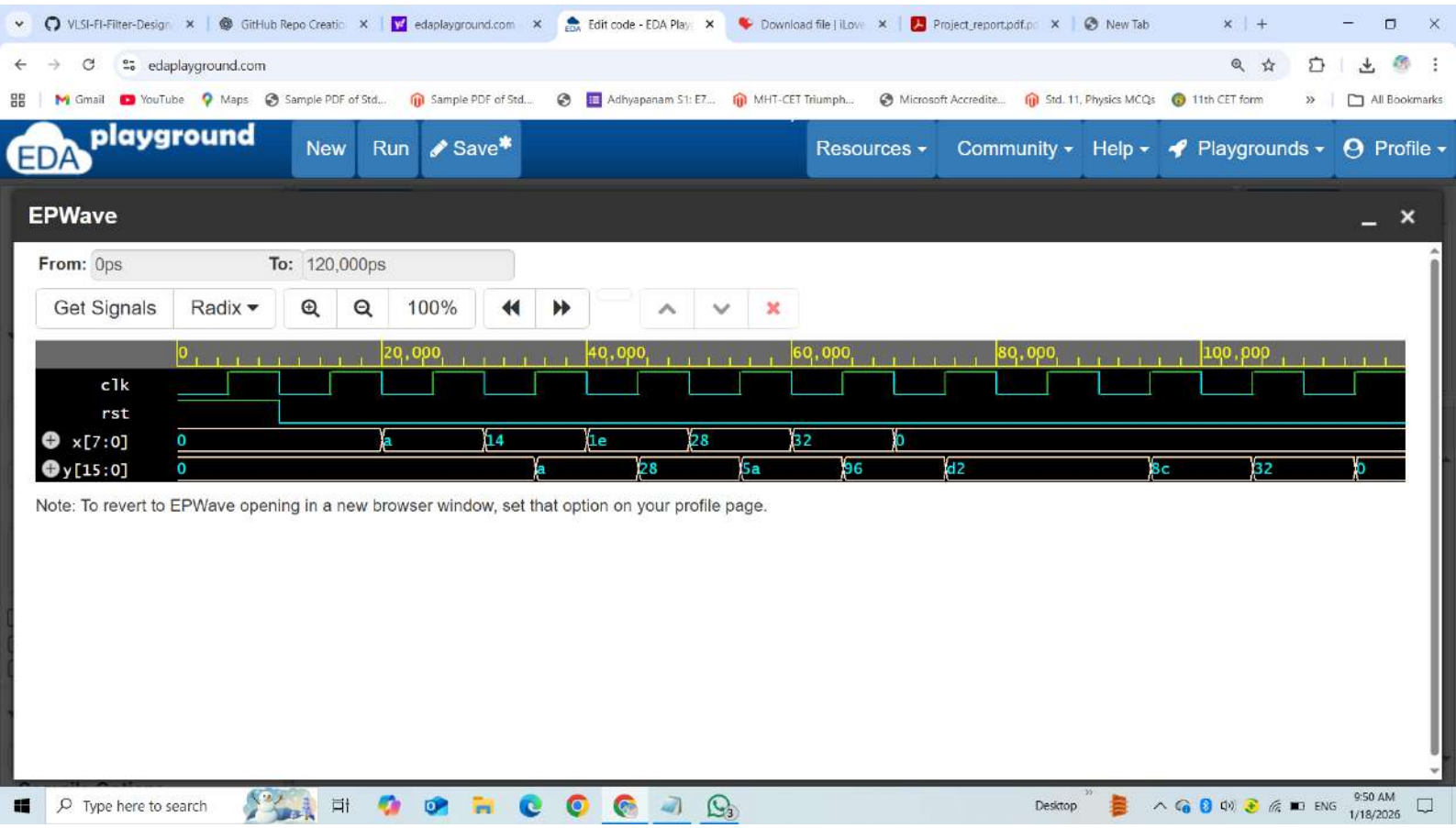
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EPWave
From: 0ps
To: 120,000ps
Get Signals
Radix
100%
0
20,000
40,000
60,000
80,000
100,000
clk
rst
x[7:0]
0
a
14
1e
28
32
0
y[15:0]
0
a
28
5a
96
d2
8c
32
0
Note: To revert to EPWave opening in a new browser window, set that option on your profile page.
Type here to search
Desktop
ENG
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