VLSI Design of FIR Filter for DSP Applications

Abstract

This project focuses on the design and implementation of a Finite Impulse Response (FIR) filter using Verilog HDL. FIR filters are commonly used in DSP applications due to their inherent stability and linear phase response.

Introduction

Digital filters are essential components in modern communication and signal processing systems. FIR filters are preferred in applications requiring precise phase characteristics.

Methodology

1. FIR coefficients generated using MATLAB
2. RTL code written in Verilog HDL
3. Testbench developed for functional verification
4. Theoretical waveform behavior analyzed

Tools Used

- MATLAB
- Verilog HDL
- GitHub

Results

The FIR filter produces finite-duration output corresponding to the applied input. Impulse response validates correct filter behavior.

Conclusion

The project successfully demonstrates FIR filter implementation using VLSI design principles and Verilog HDL.

Future Scope

- FPGA implementation
- Power and area optimization
- ASIC synthesis