

Quartus Compilation Report – FIR Filter

The FIR filter design was compiled using Intel Quartus Prime Lite Edition.

The compilation process completed successfully, as shown in the Quartus message window.

From the compilation summary visible in the screenshot:

- Analysis & Synthesis: Successful
- Total Errors: 0
- Total Warnings: 0
- Flow Status: Successful
- Elapsed Time: 00:01:51 (approx.)

The successful compilation confirms that the FIR filter Verilog code is syntactically correct and can be implemented on the selected FPGA device. No modifications or debugging were required, as the tool reported no errors or warnings throughout the process.

This screenshot serves as the official proof of successful synthesis and compilation of the FIR filter design in Intel Quartus Prime Lite.