## **Instruction Set**

<b>Instruction</b> \Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADD (immediate)	imm									dest src		000		1		
ADD (register)	000000 dest								src2 src			000		0		
SUB (immediate)	imm									dest src			001			1
SUB (register)	000000 dest								src2 src			001		0		
LOAD (immediate)	imm									est				010		1
LOAD (register)	000000 dest								0	0	SI	rc	010			0
LOAD (relative)	imm								dest src			010		1		
BANK SWITCH	imm								1111					010		0
STORE (immediate)	imm								sr	src 00		011		1		
STORE (register)	000000 dest							est	0	0	SI	rc		011		0
STORE (relative)	imm								sr	rc2 src				011		1
JUMP (immediate)	imm								0000					100		1
JUMP (register)	000000000											rc		100		0
JUMP (relative)	imm								00 1				100		1	
HALT	1111111								0000					100		0
JUMPZ (immediate)	imm								0000				101		1	
JUMPZ (register)	000000000											rc		101		0
JUMPZ (relative)	imm									0	0	1		101		1
	I															
JUMPNZ (immediate)	imm									0000				110		1
JUMPNZ (register)	000000000								src				110		0	
JUMPNZ (relative)	imm									0	0	1		110		1
HINADAL (*									0022							
JUMPN (immediate)	imm								0000					111		1
JUMPN (register)	000000000											rc		111		0
JUMPN (relative)	imm									0	0	1		111		1