Design an Inverter using CMOS transistor

DIGITAL IC DESIGN

(ELE4620)

Bachelor of Technology in Electronics Engineering

Submitted By

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Submitted To

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ALIGARH-202002 (INDIA)

NOVEMBER, 2024

Objective: -

To design an inverter on Cadence Virtuoso tool using GPDK90 technology.

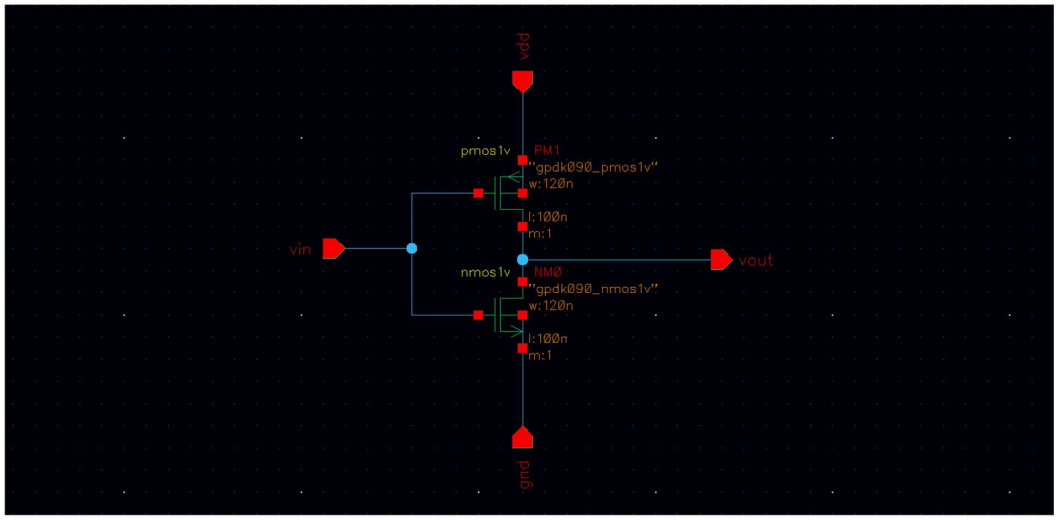
Tools and Technologies: -

• Cadence Virtuoso

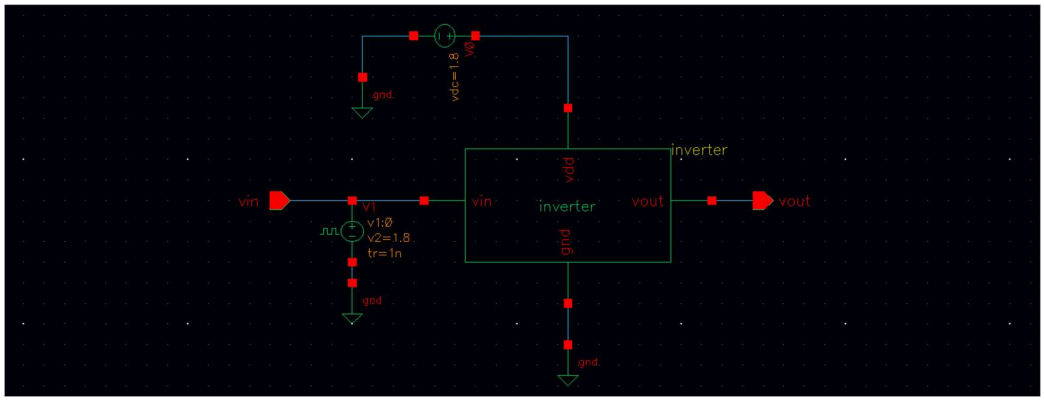
• GPDK90 technology

Design Flow (procedure): -

1. **Schematic Design**
    - The CMOS inverter schematic was created in Cadence Virtuoso, followed by symbol generation for reuse in simulations and testbenches.

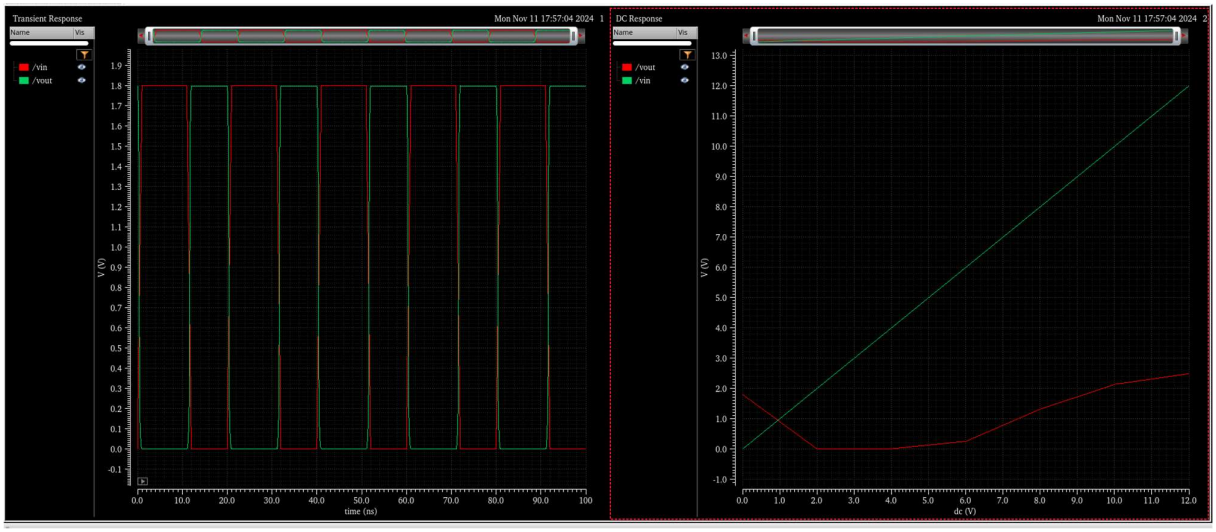


2. **Testbench Setup**
    - A testbench was designed to simulate the behaviour of the CMOS inverter and validate its output characteristics.



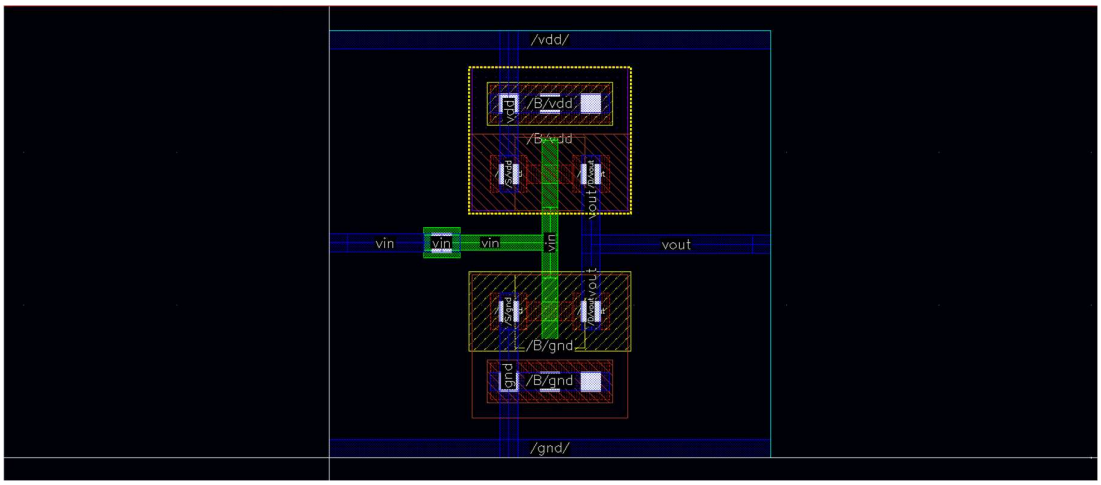
3. Simulation Results

- The inverter's Voltage Transfer Characteristics (VTC) and threshold voltage were measured through transient and DC sweep analyses.



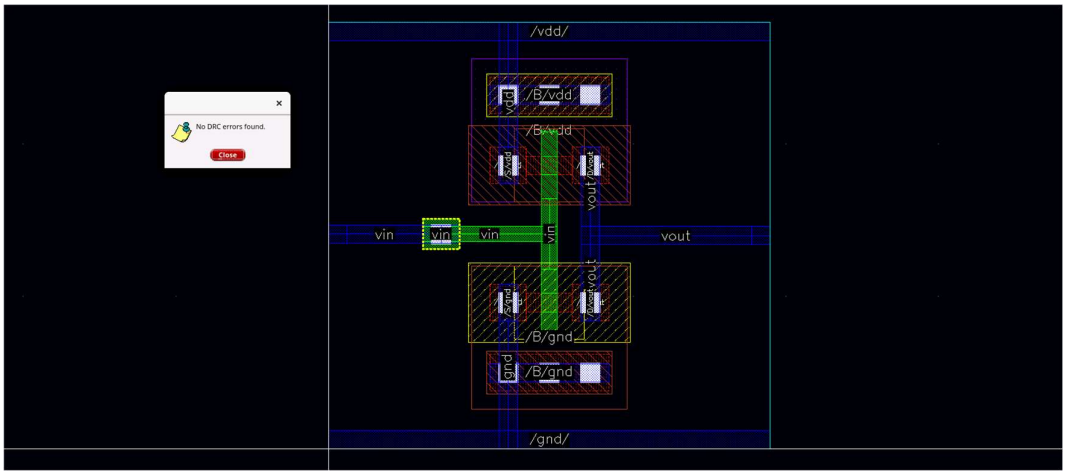
4. Layout Design

- The layout of the CMOS inverter was designed, following the specifications of GPDK90 technology. This layout forms the foundation for DRC and LVS checks.



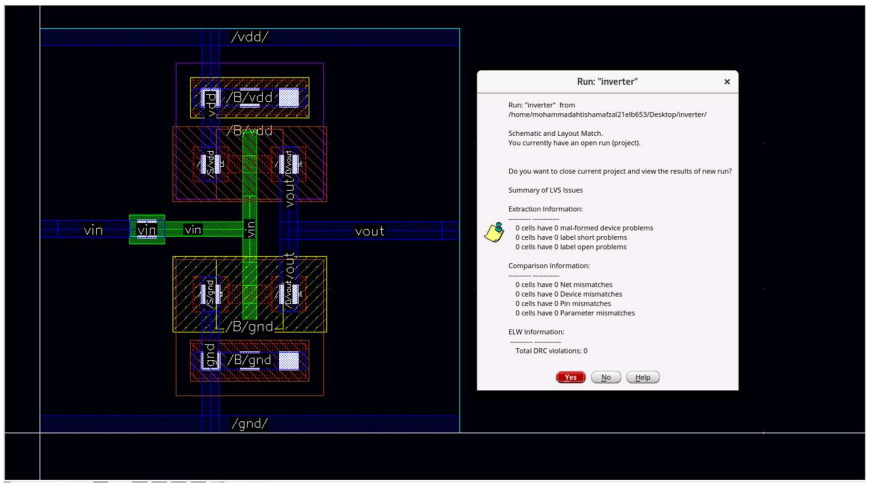
5. DRC Check

- Design Rule Check (DRC) check was performed to verify that the layout complies with fabrication rules.



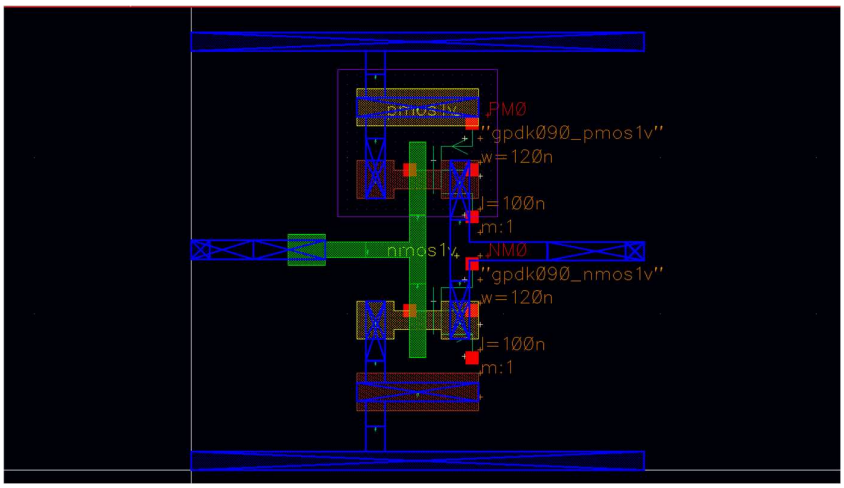
6. LVS Check

- Layout Versus Schematic (LVS) check was performed to verify that the layout complies with matches the schematic.



7. RC Parasitics Extraction

- RC parasitics were extracted from the layout to account for resistive and capacitive elements, which affect the circuit's performance in post-layout simulations.



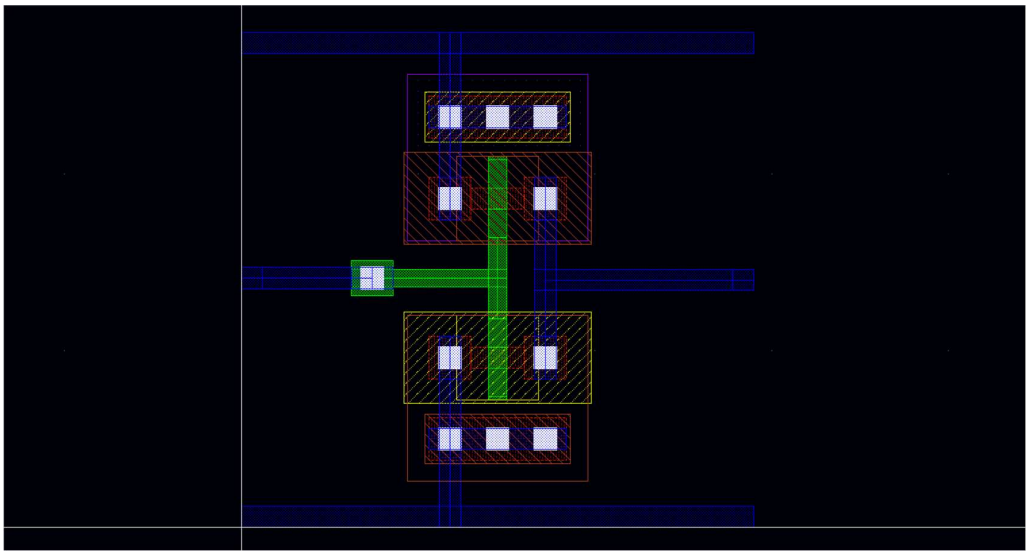
8. Pre-Layout and Post-Layout Simulations

- Simulations were performed on both pre-layout and post-layout designs to compare performance metrics such as delay.
- **Pre-Layout Results**
    - The delay measured in pre-layout simulations was found to be 115.1 ps.

- **Post-Layout Results**
    - Post-layout simulations showed an increase in delay to 122.4 ps due to parasitic effects.

9. GDSII File Generation

- The final layout was exported in GDSII format, ready for tape-out and further fabrication steps.



Conclusion: -

The project successfully covered the design, simulation, and layout of a CMOS inverter using Cadence Virtuoso. Beginning with the schematic design and testbench setup, the inverter's performance was validated through simulations, ensuring accurate Voltage Transfer Characteristics (VTC) and threshold voltage measurements. The subsequent layout design adhered to the GPDK90 technology specifications, forming a reliable base for DRC and LVS checks, which confirmed compliance with design and fabrication rules. The final GDSII file generation prepares the layout for potential tape-out, completing the design process for fabrication readiness. This comprehensive flow establishes a robust approach for CMOS inverter design and verification, ensuring both functionality and manufacturability.