Design a Half Adder using CMOS transistor

DIGITAL IC DESIGN

(ELE4620)

Bachelor of Technology in Electronics Engineering

Submitted By

MOHAMMAD AHTISHAM AFZAL

21ELB653

SIDDIQUE AHMAD

21ELB293

Submitted To

MOHD. WAJID

DEPARTMENT OF ELECTRONICS ENGINEERING

ZAKIR HUSAIN COLLEGE OF ENGINEERING & TECHNOLOGY

ALIGARH MUSLIM UNIVERSITY

ALIGARH-202002 (INDIA)

NOVEMBER, 2024

Objective: -

To design a Half Adder (EXOR based) on Cadence Virtuoso tool using GPDK90 technology.

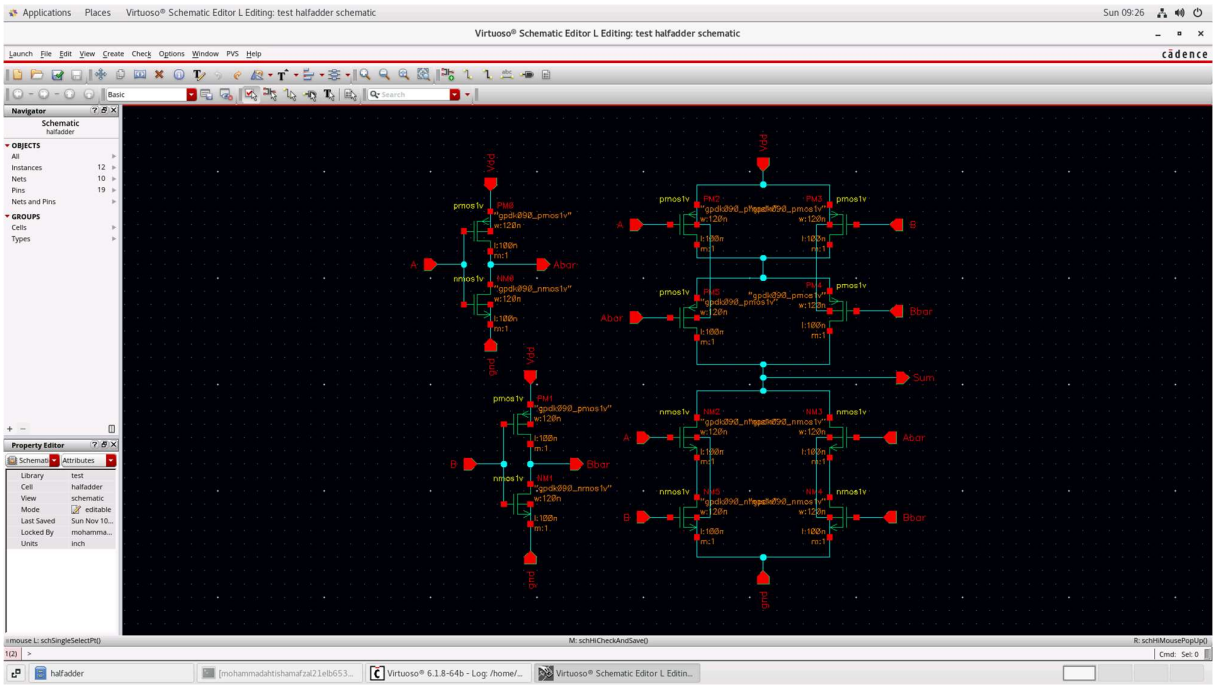
Tools and Technologies: -

• Cadence Virtuoso

• GPDK90 technology

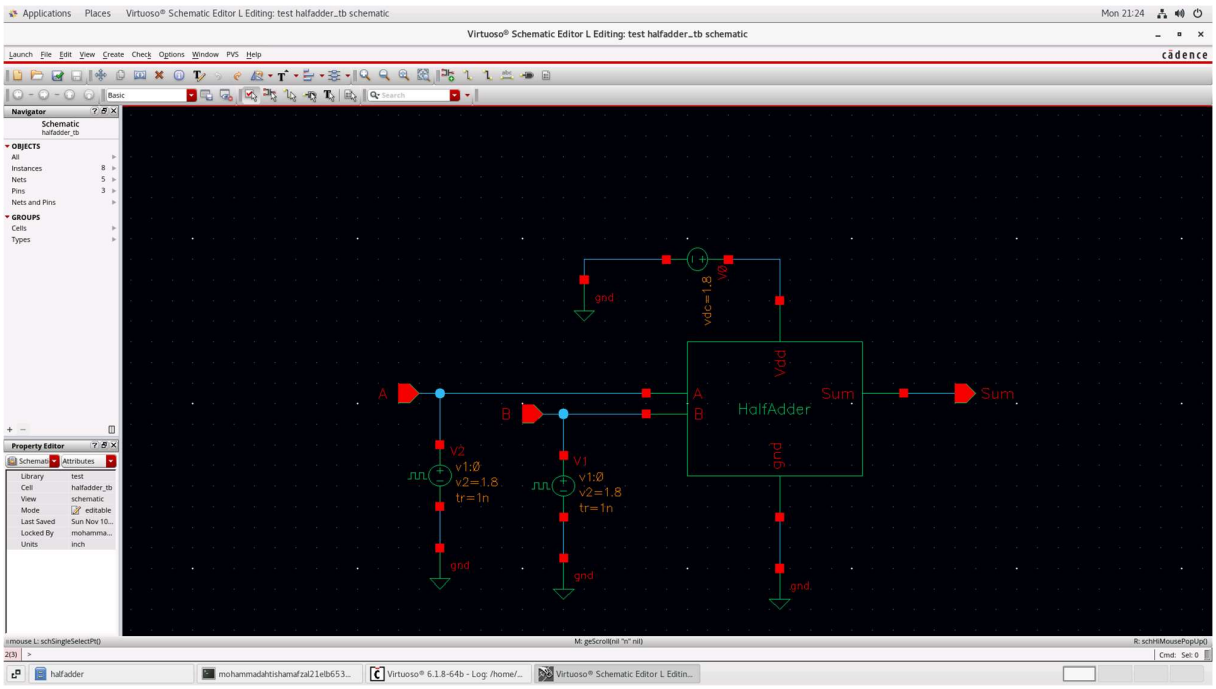
Design Flow (procedure): -

1. **Schematic Design**
    - The CMOS half adder schematic was created in Cadence Virtuoso, followed by symbol generation for reuse in simulations and testbenches.



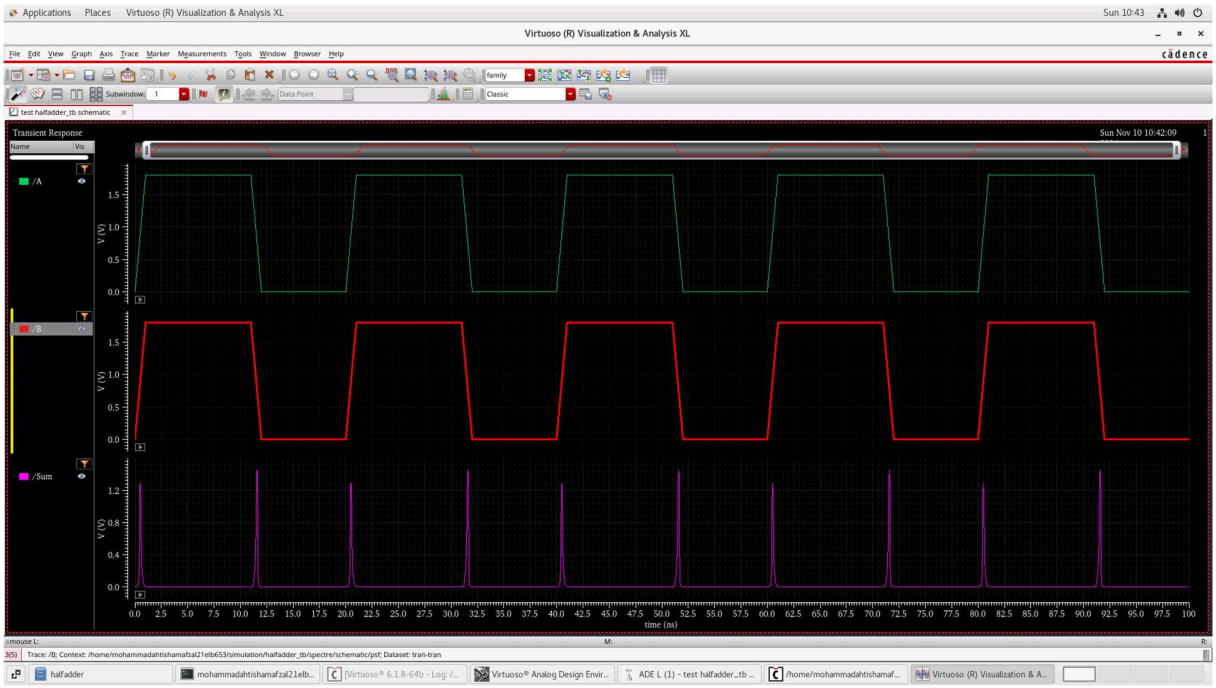
2. Testbench Setup

- A testbench was designed to simulate the behaviour of the CMOS half adder and validate its output characteristics.



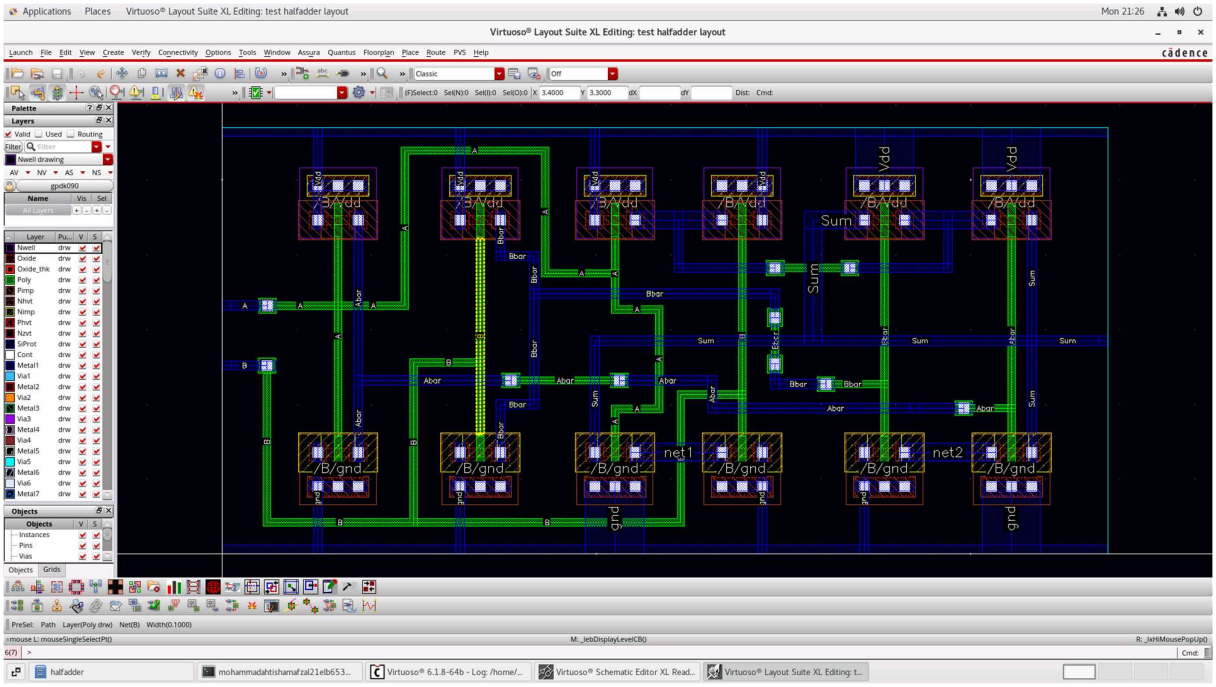
3. Simulation Results

- The half adder's Voltage Transfer Characteristics (VTC) and threshold voltage were measured through transient and DC sweep analyses.



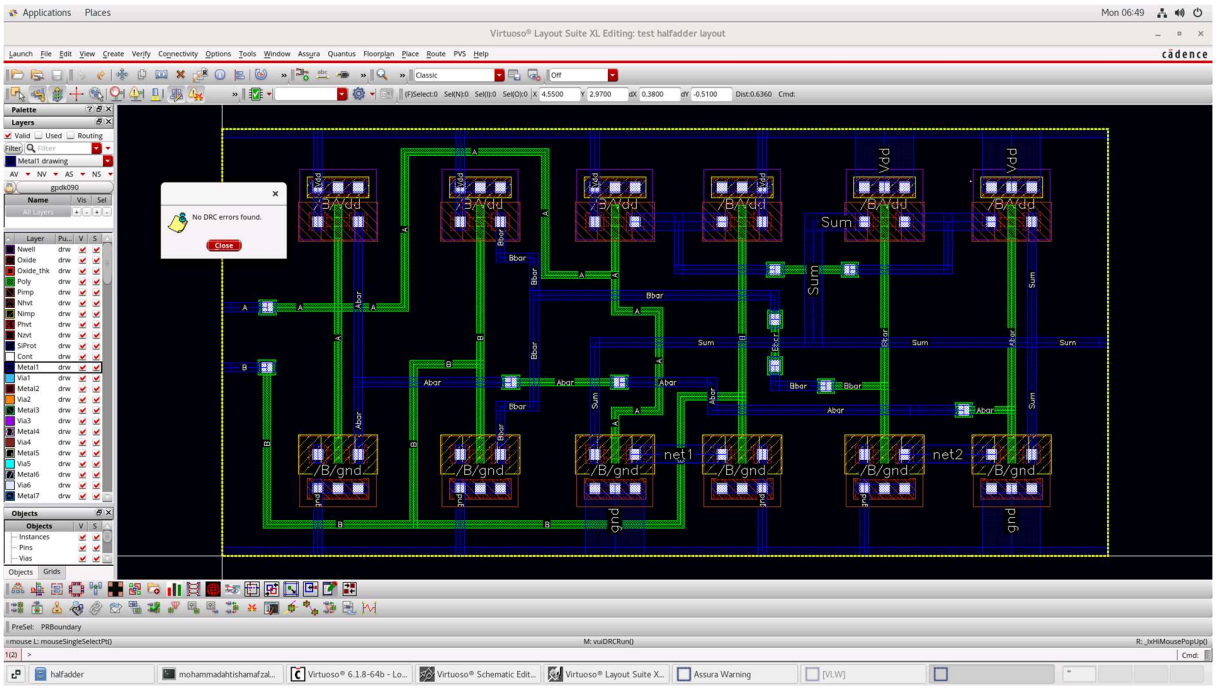
4. Layout Design

- The layout of the CMOS half adder was designed, following the specifications of GPDK90 technology. This layout forms the foundation for DRC and LVS checks.



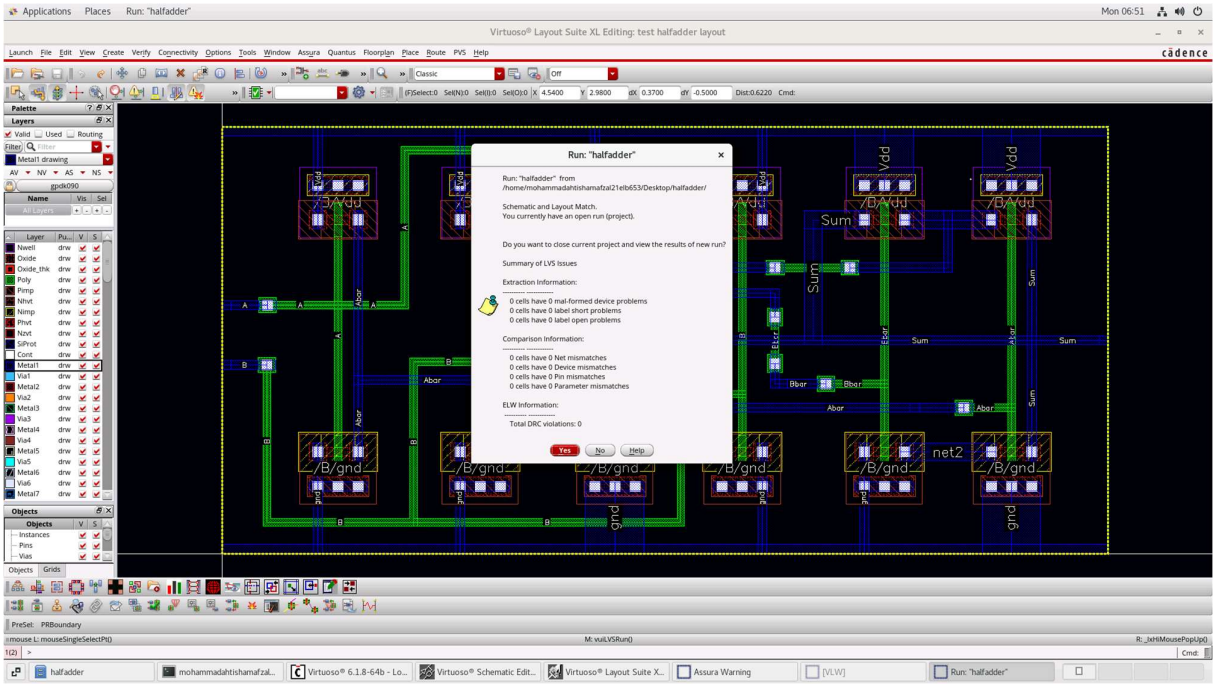
5. DRC Check

- Design Rule Check (DRC) check was performed to verify that the layout complies with fabrication rules.



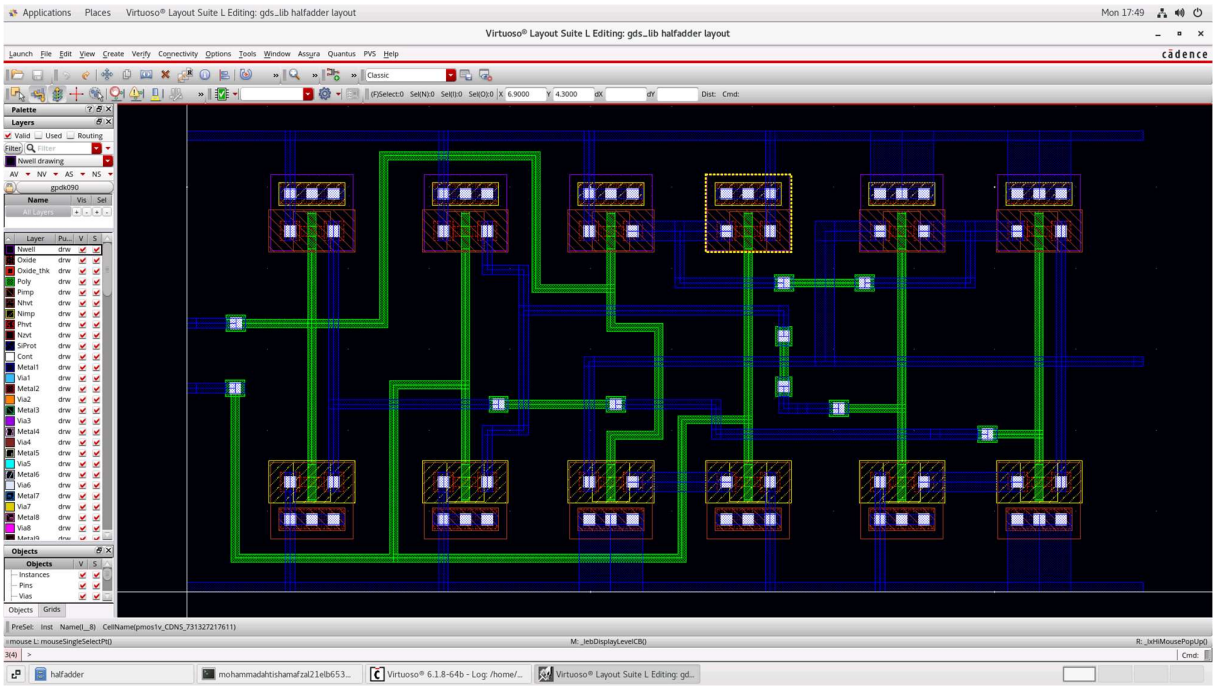
6. LVS Check

- Layout Versus Schematic (LVS) check was performed to verify that the layout complies with matches the schematic.



7. GDSII File Generation

- The final layout was exported in GDSII format, ready for tape-out and further fabrication steps.



Conclusion: -

The project successfully covered the design, simulation, and layout of a CMOS Half Adder using Cadence Virtuoso. Beginning with the schematic design and testbench setup, the half adder's performance was validated through simulations, ensuring accurate Voltage Transfer Characteristics (VTC) and threshold voltage measurements. The subsequent layout design adhered to the GPDK90 technology specifications, forming a reliable base for DRC and LVS checks, which confirmed compliance with design and fabrication rules. The final GDSII file generation prepares the layout for potential tape-out, completing the design process for fabrication readiness. This comprehensive flow establishes a robust approach for CMOS inverter design and verification, ensuring both functionality and manufacturability.