

The Instruction Set Architecture (ISA):

Types of instructions supported = 3

No. of ALU operations supported = 2

No. of registers in register set = 3

Word size of CPU = 5

Word size of RAM & ISA = 16

Register Mode:

Opcode		Register 1	Register 2	Unused
Type (2 bits)	Operations (1 bit)	2 bits	2 bits	9 bits
00	0 (NOT)	00-10 (R0-R2)	XX	
	1 (ROR)	00-10 (R0-R2)	00-10 (R0-R2)	

Register Mode NOT: 00 0 00 00 000000000**Register Mode ROR:** 00 1 00 01 000000000**Immediate Mode:**

Opcode		Register 1	Constant	Unused
Type (2 bits)	Operations (1 bit)	2 bits	5 bits	6 bits
01	0 (NOT)	00-10 (R0-R2)	XXXXX	
	1 (ROR)	00-10 (R0-R2)	00000-00010 (R0-R2)	

Immediate Mode NOT: 01 0 00 00000 000000**Immediate Mode ROR:** 01 1 00 00001 000000**Branching Mode:**

Opcode		Address	Unused
Type (2 bits)	Operations (1 bit)	3 bits	10 bits
10	0 (JZ)	000-111 (0-7)	

Branching JZ: 10 0 000 0000000000