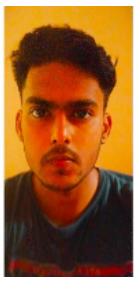
PERSONAL DETAILS



Name	**Sidhant Priyadarshi**
Email Id	sidhant1922@gmail.com
Contact Number	9560121498
Address	Pali road, rohtas Dehri on sone, Bihar, 821307
Date of Birth	22/12/2003
Gender	Male
Marital Status	Single
Languages Known	Hindi, English

SUMMARY

Computer architecture and Frontend digital VLSI enthusiast and ability to perform with the team. I love to design digital systems using verilog HDL.

CAREER OBJECTIVE

I want to be certified digital/chip design engineer. I have the motive to take part in making India to be self-reliant on semiconductor industry.

EDUCATION

Year of Passing	Degree/Course	Percentage/CGPA
Pursuing	Electronics and Communication Engineering Kle Technological University , Kle society	8.5

EXPERIENCE

Jun-2021 - Till Today	**KLE Technological University**
Co-cordinator	-Conducting academics events for the ECE branch. -We have conducted few events and workshops till date. -Improving academic skills in students and ourselves.

PROJECTS

Project Name: RISCV-RV32I

Role: RTL design **Team Size:** 1 **Project Duration:** 1 Month

Project Detail -Worked on designing basic ALU operation of mips32 using verilog with 5-stage pipeline design. -https://github.com/sidhantp1906/RV32I

Project Name: GUESS & LOTTERY GAME

Role: Python script development **Team Size:** 1 **Project Duration:** 5 Day

Project Detail -Designed a simple guess and lottery game using python3. -https://github.com/sidhantp1906/guess-game-using-python -https://github.com/sidhantp1906/lottery-game

Project Name: 32-BIT CSD MULTIPLIER

Role: RTL design **Team Size:** 1 **Project Duration:** 20 Day

Project Detail -Design of 32-bit CSD multiplier using booth techniques using verilog HDL. -https://github.com/sidhantp1906/csd-multiplier-using-booth-technique

ACHIEVEMENTS

eSIM-marathon finalist	Marathon conducted by FOSSEE IIT-Bombay for circuit design and simulation using eSIM and skywater130nm technology

SKILLS

Verilog	
Digital design	
Tools	Xilinx ISE, Iverilog, Ltspice, MATLAB, Simulink, eSIM, ArduinoIDE
C Programming language	Intermediate
Embedded systems	
SystemVerilog	
Python	
Computer architecture	

Arduino uno r3

AREAS OF INTERESTS

Frontend-digital VLSI, RTL design, RISC assembly, SOC design

COURSES

VLSI SOC design using verilog HDL	-Designing digital systems using verilog HDL. -https://elearn.maven-silicon.com
VLSI CAD part 1: Logic	-Boolean algebra and basics of operation to start with backend of ASIC design flow. -https://www.coursera.org/account/accomplishments/certificate/2P6NUBE2X728
VLSI CAD part 2: Layout	-Basics algorithm to perform placement & routing , Static timing analysis and other backend functionality. -https://www.coursera.org/account/accomplishments/certificate/N755B3AQ58ZD
RISCV-SPEC-V2.2	-Understanding the ISA of RISCV. -https://riscv.org/
Computer Organization and Design-RISCV edition	-Starting with design of RISCV with taking performance and all other keys into consideration. -https://riscv.org/
Book_SystemVerilog_for_verification	-Basic knowledge about VMM(verification methodology module). -https://www.springer.com
Introduction to logic circuit and logic design using verilog	-Design of digital systems using verilog. -https://www.springer.com

LINKS

Github	https://github.com/sidhantp1906
LinkedIn	https://www.linkedin.com/in/sidhant-priyadarshi-028612185

DECLARATION

I hereby declare that all the details furnished here are true to the best of my knowledge and belief.

Sidhant Priyadarshi