Sidhant Priyadarshi

Student

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Hubli

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Student with enthusiasm in frontend designing of digital system and ability to perform with team. I love designing digital systems using Verilog HDL. I will love to work as a DIGITAL DESIGN ENGINEER

EDUCATION

BE
KLE Technological University

07/2019 - 07/2023

Courses
- Electronics And Communication Engineering

PUC
Mother Khazani Convent School

05/2017 - 05/2019

Courses
- Physics, Chemistry, Maths

VOLUNTEER EXPERIENCE

OFFICE BEARER
KLE Technological University

06/2021 - Present

Tasks
- Organising academic events for ECE branch
- We have organised workshops on Python, MATLAB and quizes on pre-placement activities
- Improvement of academic skills within us and students

SKILLS AND TOOLS

Verilog | SystemVerilog | Python | Digital Electronics | Computer Architecture | Digital System Design | Arduino IDE | LTSpice | Xilinx ISE | Arduino Uno R3 | IVerilog

PERSONAL PROJECTS

RISCV-RV32I (06/2021 - 07/2021)
- I have designed 5-stage pipelined RV32I core for few of the instructions using Verilog HDL
- First stage is fetching data from code memory, Second is decoding, Third is executing the instructions, Fourth is loading and storing, Fifth stage it is writing back the output in desired register location
- https://github.com/sidhantp1906/RV32I

GUESS GAME (07/2021 - 07/2021)
- Designed a simple guessing game using Python3. 7
- In which it will be generating a random number and user have to guess the number if it is guessed in first attempt it will print lucky else it will count the number of steps taken to guess correct output and luck meter
- https://github.com/sidhantp1906/guess-game-using-python

32-BIT CSD multiplier (05/2021 - 06/2021)
- Designed and implemented a CSD multiplier using Verilog HDL
- First I converted binary multiplier into its CSD representation and using booth algorithm I performed multiplication operation
- https://github.com/sidhantp1906/csd-multiplier-using-booth-technique

COURSE CERTIFICATES

VLSI CAD PART 1 : LOGIC (06/2020 - 07/2020)
Basics about digital logic design offered on coursera

VLSI CAD PART 2: LAYOUT (07/2020 - 07/2020)
Algorithms and Basics about backend functionalities of designing SOC's

VLSI SOC's DESIGN USING VERILOG HDL (06/2021 - 07/2021)
Designing of digital system using Verilog HDL

LANGUAGES

HINDI
Full Professional Proficiency

English
Professional Working Proficiency

INTERESTS

DIGITAL DESIGN ENGINEER(FRONTEND ROLE)