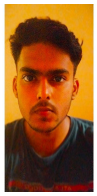

Last Updated on 17th July 2022

Sidhant Priyadarshi

sidhant1922@gmail.com | 9560121498

EDUCATION

KLE TECHNOLOGICAL UNIVERSITY

Bachelor in Engineering
Expected in july 2023 | Karnatak, IN
CGPA: 8.73

MOTHER KHAZANI CONVENT SCHOOL

Senior Secondary
Grad. in July 2019 | Delhi, IN
CGPA 8.25

LINKS

Github: **sidhantp1906**
LinkedIn: **Sidhant Priyadarshi**

EXPERIENCE

KLE TECHNOLOGICAL UNIVERSITY

EA Office Bearer
June 2021 – june 2022 | Hubli, Karnatak

- Organizing academic events for ECE branch.
- We have organized workshops on Python, MATLAB and quizes on pre-placement activities, etc.
- I was the speaker of RTL Workshop at KLE Technological University and VLSI Overview at MJCET, Hyderabad.

SKILLS

PROGRAMMING

Verilog, SystemVerilog, OOPS
Python, C, MATLAB, UNIX.

TOPICS

Computer Architecture, STA,
Digital/Analog Electronics, UVM,
AMBA Protocols, UART/I2C/SPI,
Arduino, Microcontroller.

TOOLS

Digital
Xilinx ISE, Cadence Genus, IcarusVerilog and GTKWAVE.
Analog
Cadence Virtuoso, Synopsys Custom Compiler.
Mixed Signal
LTSpice, eSIM.

PERSONAL PROJECTS

RISC-V RV32I

Designed 5-stage pipelined RV32I core for few of the instructions using Verilog HDL.
Link to Project.

AMBA - APB4 AND AHB-LITE

Designed a AMBA protocols like APB and AHB-LITE using Verilog HDL.
Link to Project.

FCFS ARBITER DESIGN AND VERIFICATION

Designed a FCFS Arbiter using Verilog HDL and verfied using VMM based verification.
Click to visit report.

32-BIT CSD MULTIPLIER

Designed and implemented a CSD multiplier using Verilog HDL.
Link to Project.

RESEARCH

PARALLEL DIGITAL VLSI ARCHITECTURE FOR COMBINED SVM TRAINING AND CLASSIFICATION

Research Experience Undergrad
Feb 2022 – Present | Hubli, Karnatak
Worked with **Prof. Dr Saroja V Siddamal** on research and design of SVM training and classification digital architecture which classifies between diabetic and non diabetic person based on glucose level. This work will be published by the end of this year.

COURSES/CERTIFICATES

VLSI CAD Logic to Layout:	Coursera
Learn to build UVM/OVM testbench from scratch:	Udemy
VLSI SOC Design using Verilog HDL:	MAVEN SILICON
eSIM Marathon finalist:	IIT-Bombay and VSD
Cloud based Analog Design Hackathon finalist:	Synopsys and VSD

LANGUAGE

English
Hindi

AREAS OF INTEREST

RTL Design, Computer Architecture
SOC Design and Verification
Programming