

A Programmable Sustaining Amplifier for Reconfigurable MEMS-Referenced Oscillators

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Abstract—We describe a highly-programmable integrated sustaining amplifier for reconfigurable MEMS-referenced oscillators. The frequency response, voltage gain, and phase shift of the amplifier can be independently controlled using bias currents, thus enabling it to be interfaced with a variety of MEMS devices with resonant frequencies in the 10-120kHz range. The chip, which was designed in 0.5 μ m CMOS, also includes i) an automatic level control (ALC) circuit; and ii) an independently-adjustable background compensation network (BCN) that is used for canceling the parasitic electrical capacitance of the resonator. We present experimental data that confirms the functionality of individual circuit blocks and also the amplifier as a whole.

I. INTRODUCTION

Stable oscillators are vital components in a variety of applications including navigation systems and wireless transceivers. Quartz crystal oscillators have dominated the timing and frequency control market for decades but are not suitable for monolithic integration with CMOS circuitry [1]. Oscillators referenced to MEMS/NEMS resonators [2] are emerging alternatives due to their small form factors, ultra-high Q [3], low power consumption, good long-term stability [4], compatibility with batch processing, high reliability, overall low cost, and wide operating temperature range.

This paper describes a highly-programmable integrated sustaining amplifier that builds on our prior work [5]. The goal is to develop a single chip that supports MEMS-referenced oscillators based on i) various types of resonators (capacitive, piezoelectric, etc.); ii) large batches of nominally-identical resonators; or iii) different modes of the same resonator. Such a chip will enable researchers to easily characterize the performance of a variety of fabricated MEMS resonators, as well as explore new topics such as the effects of mode coupling in oscillators based on multimode resonators.

II. SUSTAINING AMPLIFIER DESIGN

Fig. 1 shows a block diagram of the sustaining amplifier along with an electrical model of a MEMS device near one of its resonant modes. The amplifier contains a low-noise preamplifier (LNA), MOS-based active resistor, two second-order G_m - C based band-pass filters (BPFs), three all-pass filters (APFs) as phase shifters, variable gain amplifiers (VGAs), an automatic level control (ALC), a “background compensation” network (BCN) to cancel the parasitic electrical capacitance of the resonator (C_p in Fig. 1), and an op-amp-based output

buffer. Various parameters of these blocks are adjustable using off-chip bias currents, as described later. In our experiments, these were generated by digitally-programmable current sources implemented on the PCB.

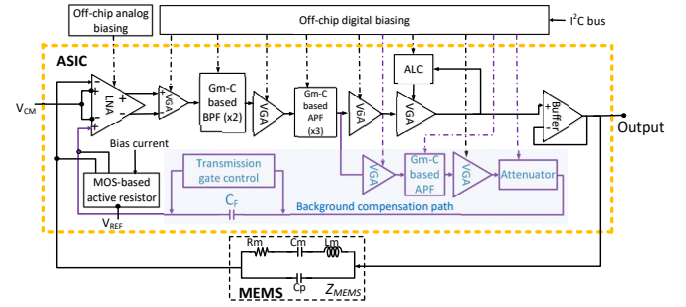


Fig. 1. Block diagram of the sustaining amplifier connected across a MEMS resonator (modeled as an impedance Z_{MEMS}) to generate oscillations. The background compensation network (BCN) is shown within a shaded box.

An earlier version of the design was discussed in [5] but not experimentally verified. Here we focus on a revised chip with many design improvements and new features (ALC, BCN, etc.) and present a variety of experimental results.

Low-Noise Amplifier (LNA): A resistively-loaded differential amplifier was used as the LNA in [5]; its inputs were connected to i) the MEMS resonator, and ii) a DC bias voltage. In this version, we need the two inputs for the MEMS and BCN paths, respectively. Unwanted capacitive coupling between these terminals (due to C_{gs} of the input transistors) is eliminated by using a differential difference structure [6] as shown in Fig. 2. Specifically, the bias voltage $V_{CM,LNA}$ is an AC ground that prevents coupling between v_{IN+} and v_{IN-} .

We have added MOS-based active resistors ($M_{18,19}$) to set the DC common-mode level at the input terminals. When biased in subthreshold, their resistance $R_{in} = \phi_T / (\kappa I_B)$, where ϕ_T is the thermal voltage, $\kappa \approx 0.7$ is the subthreshold slope constant, and I_B is a bias current. The ability to set R_{in} to very large values ($\sim G\Omega$) is an advantage over discrete amplifiers; it maximizes the transmission $Z_{in} / (Z_{in} + Z_{MEMS})$ through the resonator where $Z_{in} = R_{in} || 1 / (sC_{in})$ is the input impedance of the LNA. Also, the input-referred noise PSD is

$$\overline{\nu_{ni}^2} = \frac{16k_bT}{g_{m,9}} \left(\gamma + \frac{1}{A_0} \right) \quad (1)$$

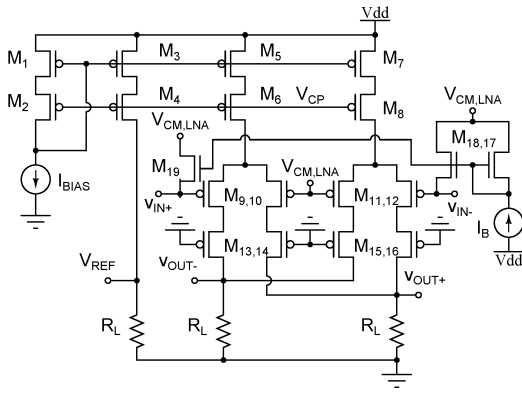


Fig. 2. The differential-difference low-noise amplifier (DD-LNA).

where $g_{m,9}$ is the transconductance of the input transistors, $\gamma \approx 2/3$ and $A_0 = g_{m,9}R_L$ is the DC gain. The two terms are due to noise added by the transistors and resistors, respectively. The value of $g_{m,9}$ can be adjusted via the bias current I_{BIAS} , while $R_L = 248\text{k}\Omega$ is fixed. Finally, a copy of I_{BIAS} is used to generate a DC voltage V_{REF} that is fed as a common-mode reference for other stages in the amplifier.

Wide-Linear-Range (WLR) Amplifier: We use a WLR operational transconductance amplifier (OTA) as the basic signal processing block for the design. Specifically, we use a modified version of the 13-transistor design proposed by Sarpeshkar et al. [7]. Our design uses source degeneration and bump linearization to improve the linear range V_L , but gate (instead of well) inputs. This limits V_L to $\approx 3\phi_T(1+1/\kappa)/\kappa \approx 270\text{mV}$ as compared to 1.7V in [7], but improves input common mode range. Gate inputs also reduce offset and layout area as the transistors can be fabricated in the same well. Systematic offsets were reduced by cascoding all the current mirrors.

Band-Pass Filter (BPF): Two cascaded second-order G_m - C BPFs determine the frequency response of the amplifier, i.e., enable the selection of a particular resonant mode. Each BPF utilizes the same topology as in [5], but uses the new WLR-OTA. Specifically, two OTAs in a negative feedback loop gyrate the impedance of a capacitor to realize an active inductor, since passive on-chip ones are impractical at such low frequencies. A third OTA acts as a variable resistor to form a parallel RLC circuit, and the OTA bias currents are adjusted to set the resulting center frequency and Q . The common-mode voltage V_{CM} is set by V_{REF} generated within the LNA.

All-Pass Filter (APF): Three cascaded G_m -C APFs control the phase shift of the amplifier, i.e., enable the phase criterion for oscillations to be satisfied for the chosen mode. Each APF utilizes the same topology as in [5], but uses the new WLR-OTA. Specifically, a first-order G_m -C low-pass filter (LPF) creates a delay τ . Two other OTAs convert i) the input voltage, and ii) the LPF output voltage to currents that are then added using KCL and converted back to a voltage by a fourth OTA. This results in unity voltage gain and a frequency-dependent phase shift of $-2 \tan^{-1}(\omega\tau)$. Thus, each APF provides a phase shift of 0-180° as τ is adjusted from 0 to ∞ via a

bias current. However, in practice τ can only be varied over a finite range, which reduces the useful control range to $\sim 120^\circ$. Hence three cascaded APFs are used for $\sim 360^\circ$ control.

Variable Gain Amplifier (VGA): Four cascaded VGAs control the voltage gain of the amplifier after the APF, i.e., enable the gain criterion for oscillations to be satisfied for the chosen mode. Each VGA uses three OTAs (see Fig. 3): two set the variable gain G_{m2}/G_{m1} , while the third acts as a variable resistor of value $1/G_{m0}$ to create a high-pass filter at the input. The latter allows the VGAs to be AC-coupled, which prevents accumulation of DC offset and low-frequency interference (such as 60Hz pickup). Additional VGA stages were used before and after the BPF to ensure that signal amplitudes at the BPF and APF input terminals can be maintained within their respective linear ranges.

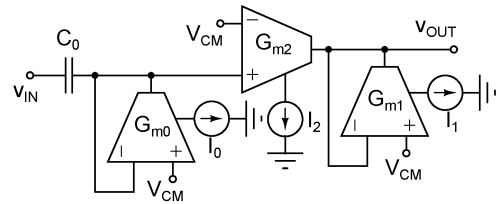


Fig. 3. The AC-coupled variable gain amplifier (VGA).

Automatic Level Control (ALC): We implement an ALC that regulates the output voltage amplitude V_{OUT} of the oscillator by adjusting the amplifier's gain. Using an ALC prevents damage to the MEMS resonator due to overload; it has also been observed to remove an unwanted $1/f^3$ component from the oscillator's phase noise spectrum [8]. The circuit (see Fig. 4) uses an envelope detector (ED) to sense V_{OUT} . An OTA (G_{m3}) then compares the ED output with a reference voltage V_{ED} to generate a feedback current that adjusts the bias i_4 of an OTA in one of the VGA stages, thus implementing gain control. ALC loops should be much slower than the oscillation period to ensure stability; in our case the loop dynamics are dominated by the ED time constant τ_{ED} , which can be adjusted via the bias current I_{ED} .

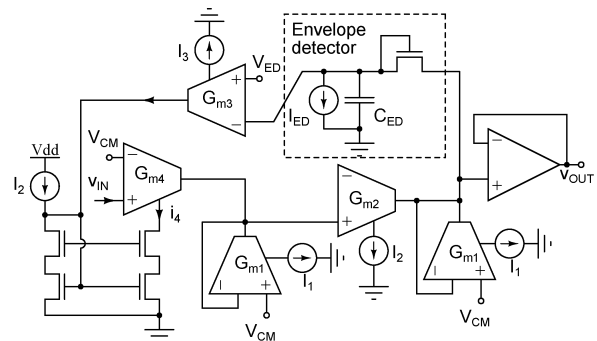


Fig. 4. The automatic level control (ALC) circuit. The value of $C_{ED} = 20\text{pF}$.

Assume that the overall open-loop gain of the forward path (MEMS and amplifier) near the resonant frequency is set to

$\alpha > 1$ with the ALC loop disabled. With the ALC enabled and the loop closed, steady-state oscillations then require the VGA bias current i_4 to decrease by a factor of α from its initial value, i.e., $i_4 = I_2 - G_{m3}(v_{ED,OUT} - V_{ED}) = I_2/\alpha$ where $v_{ED,OUT} = (V_{OUT} - V_D)$ is the output voltage of the ED and $V_D \approx 2\phi_T/\kappa \approx 75\text{mV}$ is its dead zone. As a result,

$$V_{OUT} \approx V_{ED} + V_D + V_L \left(1 - \frac{1}{\alpha}\right) \frac{I_2}{I_3} \quad (2)$$

Here $V_L = I_3/G_{m3} \approx 270\text{mV}$ is the linear range of the feedback OTA. The output amplitude is a linear function of V_{ED} ; it can be written as $V_{ED} + V_D + \beta$ where the offset β depends on V_L , α , and the ratio I_2/I_3 . We generally choose $I_3 \gg I_2$ to get high loop gain and make β negligible.

Background Compensation Network (BCN): An amplitude- and phase-tunable network cancels the parasitic electrical feedthrough of the MEMS resonator. Such feedthrough, which is generally broadband, can make it difficult for the system to oscillate at the true mechanical resonance frequency. This is undesirable since off-resonant operation degrades close-in phase noise. Moreover, the feedthrough need not be purely capacitive as shown in Fig. 1; it is better modeled as a distributed RC impedance Z_{ELEC} for resonators fabricated on highly-resistive substrates such as SiC [9].

The output voltage of the BCN is written as $A_{BCN}v_{OUT}$, where v_{OUT} is the output of the main amplifier and A_{BCN} is a complex number controlled by VGA, APF, and attenuator bias currents. The BCN drives an on-chip capacitor $C_F \approx 28\text{fF}$ that feeds back a compensation signal to the negative terminal of the LNA. In order for this to cancel transmission through Z_{ELEC} at the oscillation frequency ω_0 , we need

$$A_{BCN}(\omega_0) = \frac{Z_{in}(\omega_0) + 1/(j\omega_0 C_F)}{Z_{in}(\omega_0) + Z_{ELEC}(\omega_0)} \quad (3)$$

III. EXPERIMENTAL RESULTS

The design was fabricated in OnSemi $0.5\mu\text{m}$ CMOS technology. It occupies a layout area of $1150\mu\text{m} \times 1150\mu\text{m}$, operates off a 3.3V supply and consumes $270\mu\text{W}$. Fig. 5(a) shows a die photograph. The packaged chip was mounted on a test board (see Fig. 5(b)) designed to fit inside a vacuum chamber along with the resonator. Such chambers have a limited number of electrical feedthroughs (4 in our case), so the board was designed to require only 4 connections: power, output, and a 2-wire I²C bus. An external microcontroller uses the bus to program 16 on-board digital potentiometers. The latter are combined with op-amps to realize programmable bias current generators that in turn set all on-chip parameters with 8-bit precision.

The value of R_{in} , the active resistor at the LNA input terminals, was calibrated using the setup shown in Fig. 6(a). A small off-chip capacitor ($C_c = 1\text{pF}$) was used to inject a signal into the terminal, and the resulting transfer function measured using a low-noise preamplifier (SR560, Stanford Research Systems). Given the known input impedance of the preamplifier, the value of R_{in} can then be estimated from the cut-off frequency f_c of the resulting CR high-pass filter. The

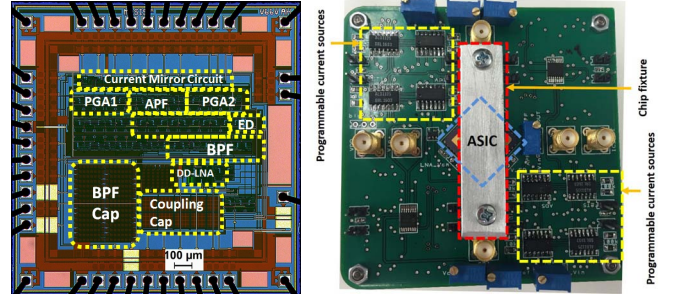


Fig. 5. (a) Die micrograph of the chip (size = $1.5\text{mm} \times 1.5\text{mm}$). (b) Photograph of the test board (size = $7.5\text{cm} \times 7.5\text{cm}$).

example shown in Fig. 6(b) corresponds to $V_B = 0.38\text{V}$, which results in $f_c = 2.63\text{kHz}$ and $R_{in} = 151\text{M}\Omega$. Additionally, the value of this active resistor was found to vary between $8\text{M}\Omega$ and $110\text{k}\Omega$ as its control voltage varied between 0.5V and 0.9V respectively, which is in good agreement with simulations.

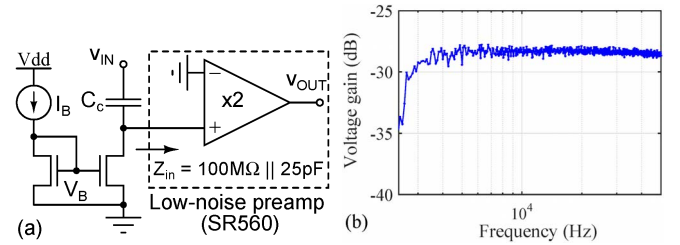


Fig. 6. (a) LNA input resistance calibration. (b) Typical data ($V_B = 0.38\text{V}$).

Fig. 7 shows that the center frequency and Q of the BPF are adjustable from $\sim 2\text{-}90\text{kHz}$ and $1\text{-}8$, respectively, while Fig. 8 shows that the APF phase shift can be adjusted over the full 360° range as expected. Moreover, the peak amplifier gain can be adjusted from $0\text{-}80\text{dB}$ using the VGAs, which is sufficient to overcome the transmission loss of typical comb-drive and piezoelectric MEMS resonators in this frequency range.

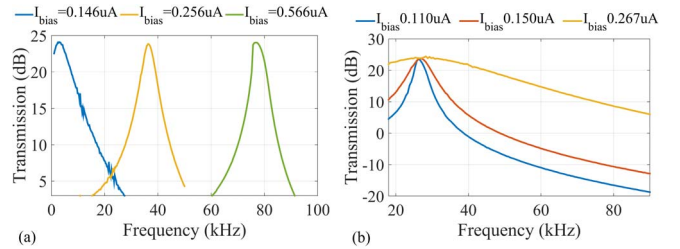


Fig. 7. BPF measurement results: tuning of (a) center frequency, and (b) Q .

The input-referred noise $\overline{v_{ni}^2}$ of the amplifier was measured with the BPF center frequency set to $f_0 = 26\text{kHz}$. Results are shown in Fig. 9 for an LNA bias current of $2.5\mu\text{A}$. The lowest noise occurs around f_0 , where the BPF gain is high enough for the LNA noise to dominate, i.e., to prevent noise from later stages from contributing to $\overline{v_{ni}^2}$. The result is $\sim 7.2\text{nV/Hz}^{1/2}$, which agrees with simulations and corresponds to a resistance

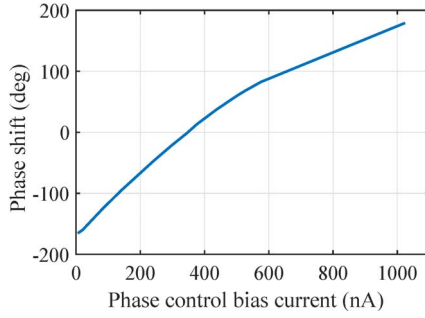


Fig. 8. APF measurement results: tuning of overall amplifier phase shift.

of $R_n = 3.13\text{k}\Omega$ at room temperature. Moreover, $R_n \ll R_m$, the motional impedance of typical MEMS resonators. Thus, the close-in phase noise of the oscillator will be dominated by the high- Q resonator, as desired [5].

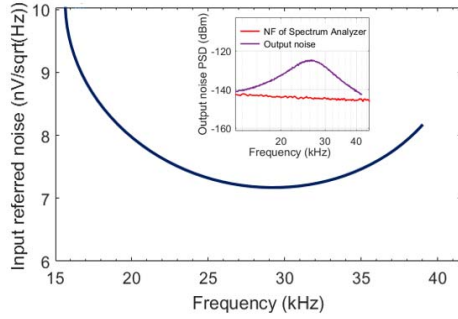


Fig. 9. Measured input-referred noise of the amplifier. BPF center frequency was tuned at 26 kHz. (Inset) Measurements of i) output noise PSD, and ii) the noise floor (NF) of the spectrum analyzer.

The overall functionality of the chip was verified by connecting several off-the-shelf quartz tuning fork resonators (motional resistance $R_m = 30\text{--}50\text{k}\Omega$) in feedback to generate stable self-sustained oscillations. In each case, the BPF, APF, and VGA were programmed to realize a start-up gain of $\alpha \approx 3$ near resonance, while the ALC was programmed to set the output amplitude to $V_{OUT} \approx 100\text{mV}$. The resulting phase noise spectra for 3 different quartz-referenced oscillators at room temperature are shown in Fig. 10. Phase noise at a given offset increases significantly with center frequency.

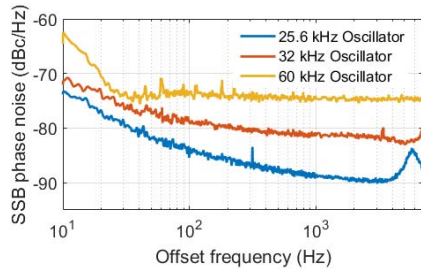


Fig. 10. Measured phase noise of various quartz-referenced oscillators.

The experimental performance of the chip is summarized in Table I; it is generally in good agreement with simulations.

TABLE I
EXPERIMENTAL PERFORMANCE SUMMARY OF THE AMPLIFIER

Low-noise amplifier (LNA) (for $I_B = 2.5\mu\text{A}$)	Gain: 12dB; Bandwidth: $\sim 1\text{MHz}$ Thermal noise PSD: $7.2\text{nV}/\text{Hz}^{1/2}$ $1/f$ corner frequency: $< 10\text{kHz}$
Band-pass filter (BPF)	Center frequency (f_0): 2–90kHz; Q : 1–8 Dynamic range (DR): 60.7dB (24kHz, $Q = 2$) Linear range: 500mV (THD $< 5\%$, 24kHz, $Q = 2$)
All-pass filter (APF)	Phase control: 0–360° Phase control sensitivity: $\approx 0.6^\circ/\text{nA}$
Variable gain amplifier (VGA)	Settable gain: 0–80dB
Automatic level control (ALC)	Amplitude control voltage (V_{ED}): 0–0.5V ED time constant: 8-bit control
Background compensation path	Gain control: -20–40dB Phase control: 0–180°

IV. CONCLUSION

We have developed a highly-programmable sustaining amplifier for MEMS-referenced oscillators in the 2–90kHz range. Preliminary experimental results with quartz resonators confirm the functionality of the chip. In future work, we will use SiC and poly-Si comb-drive MEMS resonators and characterize the resulting phase noise and long-term frequency stability in vacuum. Suitable devices are available and are being characterized. We also plan to design a new integrated sustaining amplifier for higher-frequency resonators (0.1–10MHz), which are of interest for a variety of next-generation wireless communications and sensing applications.

ACKNOWLEDGMENTS

We would like to thank the MOSIS Educational Program (MEP) for chip fabrication. This work was funded by a National Science Foundation Grant (ECCS-1509721).

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