Siddhartha

FPGAs / Machine Learning Engineer

- Singapore
- https://sidmontu.github.io
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- Github
- LinkedIn

Personal Statement

Computer engineer/researcher with a strong academic track record looking for a fresh challenge. I am especially interested in hardware design and/or machine-learning related projects, as I have relevant experience in both areas. Lifelong learner open to picking up new technology stacks when needed, and ready to work hard towards ambitious targets.

Hardware

- Strong foundational experience
- Proficient with Verilog
- Familiar with FPGA tools
- VivadoHLS / PYNQ Framework
- RF communication fundamentals

Software

- Experienced UNIX user, comfortable with command-line tools.
- Experienced C/C++ programmer
- Strong Python developer
- Tensorflow/PyTorch machine learning frameworks
- Data Analysis using R
- Typesetting with LaTeX
- Version control, *e.g.* `git`

Work Experience

Oct 2017 - Dec 2019

Postdoctoral Research Associate　　　　University of Sydney
Main Project: High-speed machine learning for RF applications
This project explored the feasibility of applying and implementing deep learning models on FPGAs for doing *real-time* radio-frequency spectral prediction. I served as the lead technical engineer on this project, and built a software-framework for automating the end-to-end flow of modeling, training, and implementing convolutional neural networks on FPGAs. Topics/technology-stacks learnt during the course of the project: Python, Tensorflow/Tensorpack, VivadoHLS, low-precision neural networks.
Other roles: Project supervision / guidance to undergraduate students doing their final-year projects, involvement in other research projects in the lab.

Jun – Oct 2012

Undergraduate Research Assistant　　　Imperial College London
Under the University Research Opportunities Program (UROP), I embarked on a summer project under the supervision of Nachiket Kapre, which eventually served as a foundation to my PhD research. The work produced during this stint was published as a short paper in the 2014 IEEE Field-Programmable Custom Computing Machines conference proceedings.

Education

2013 – 2019

Doctor of Philosophy　　　Nanyang Technological University, Singapore
Dissertation: Dataflow Optimized Overlays for FPGAs
This thesis introduces Dataflow Coprocessor Overlay (DaCO), a token dataflow overlay architecture tuned for FPGAs. DaCO pushes the performance boundaries of existing designs by exploiting static criticality information to support out-of-order execution inside each processing element. When compared to in-order designs, DaCO delivers up to $2.4\times$ improvement in performance.

2009 – 2012

Undergraduate　　　Imperial College London
BEng in Electrical & Electronics Engineering, graduated with a second-upper class honors degree.

Notable Publications

🎓 **Google Scholar**

2018
DaCO: A High-Performance Token Dataflow Coprocessor Overlay for FPGAs
Siddhartha, Nachiket Kapre
International Conference on Field-Programmable Technology

2018
Hoplite-Q: Priority-Aware Routing in FPGA Overlay NoCs
Siddhartha, Nachiket Kapre
IEEE 26th Annual International Symposium on Field-Programmable Custom Computing Machines

2020
LUXOR: An FPGA Logic Cell Architecture for Eficient Compressor Tree Implementations
Seyedramin Rasoulinezhad, Siddhartha, Hao Zhou, Lingli Wang, David Boland, Philip Leong
ACM/SIGDA International Symposium on FPGAs

2018
Long Short-Term Memory for Radio Frequency Spectral Prediction and its Real-Time FPGA Implementation
Siddhartha, Yee Hui Lee, Duncan Moss, Julian Faraone, Perry Blackmore, Daniel Salmond, David Boland, and Philip Leong
IEEE Military Communications Conference (MILCOM)

2020
Real-Time Automatic Modulation Classification using RFSoC
Stephen Tridgell, David Boland, Philip Leong, Ryan Kastner, Alireza Khodamoradi, Siddhartha
27th Reconfigurable Architectures Workshop