Siddhartha

CONTACT INFORMATION

sidmontu@gmail.com | +61 411-771-811
https://sidmontu.github.io | sidmontu

RESEARCH INTERESTS

FPGAs, Machine Learning, Circuit Design, High-Performance Computing

EDUCATION

Nanyang Technological University, Singapore

PhD, Computer Science & Engineering, February 2019

- Dissertation Title: *Dataflow Optimized Overlays for FPGAs*
- Advisor: Nachiket Kapre

Imperial College London, London, United Kingdom

BEng, Electrical & Electronics Engineering, June 2012

RESEARCH EXPERIENCE

Posdoctoral Research Associate October 2017 to Present

Computering Engineering Lab,
School of Electrical and Electronics Engineering
University of Sydney
Supervisors: Philip Leong, David Boland

Research Assistant July 2012 to September 2012

Circuits and Systems Research Group,
Electrical and Electronics Engineering Department
Imperial College London
Supervisor: Nachiket Kapre

SKILLS

Hardware Design / Hardware Acceleration

- **Verilog** : Competent with the language – completed multiple large research projects using associated compilation/simulation tools.
- **Vivado/Quartus** : Active contributor to the FPGA research field. Familiar with FPGA architectures, and comfortable with using Xilinx/Intel vendor tools.
- **VivadoHLS** : Actively learning and using the environment to prototype and implement hardware designs in research projects.
- **CUDA** : Familiar with CUDA programming framework – used for projects in class assignments and research projects.

Software Engineering

- **C/C++** : Competent and very comfortable with the programming environment. Developed and managed multiple C/C++-based projects, and familiar with development tools and good design practices.
- **Command line tools** : Strong preference for Unix-based environments – comfortable working with popular command line tools (e.g. git, sed, awk, grep, etc).
- **Python** : Primary choice of language for most software development projects lately.
- **Tensorflow/Tensorpack** : Currently use extensively to design and train neural networks for various research projects.
- **R** : Primary choice of programming environment for data analysis. Have completed a 10-module data science specialization course offered by the John Hopkins University on Coursera that was taught in R.
- **LaTeX** : Primary choice for typesetting any technical reports, or conference/journal publications. This CV was built on an existing open-source LaTeX template.

Publications

1. **Siddhartha**, and Nachiket Kapre "DaCO: A High-Performance Token Dataflow Coprocessor Overlay for FPGAs" *International Conference on Field-Programmable Technology*, December 2018 (Poster)

2. **Siddhartha**, David Boland, Steve Wilton, Barry Flower, Philip Leong, and Perry Blackmore "Simultaneous Inference and Training using On-FPGA Weight Perturbation Techniques" *International Conference on Field-Programmable Technology*, December 2018 (Poster)

3. **Siddhartha**, Yee Hui Lee, Duncan Moss, Julian Faraone, Perry Blackmore, Daniel Salmond, David Boland, and Philip Leong "Long Short-Term Memory for Radio Frequency Spectral Prediction and its Real-Time FPGA Implementation" *IEEE Military Communications Conference (MILCOM)*, October 2018
[DOI: 10.1109/MILCOM.2018.8599833]

4. **Siddhartha**, Nachiket Kapre "Hoplite-Q: Priority-Aware Routing in FPGA Overlay NoCs" *IEEE 26th Annual International Symposium on Field-Programmable Custom Computing Machines*, May 2018
[DOI: 10.1109/FCCM.2018.00012]

5. **Siddhartha**, Nachiket Kapre "eBSP: Managing NoC traffic for BSP workloads on the 16-core Adapteva Epiphany-III Processor." *Design, Automation, and Test in Europe*, March 2017
[DOI: 10.23919/DATE.2017.7926961]

6. **Siddhartha**, Nachiket Kapre "Out-of-Order Dataflow Scheduling for FPGA Overlays." *Overlay Architectures for FPGAs Workshop (co-located with FPGA 2017)*, February 2017 (Position Paper)
[DOI: arXiv:1705.02734]

7. Gopalakrishna Hegde, **Siddhartha**, Nachiappan Ramasamy, Nachiket Kapre "CaffePresso: An Optimized Library for Deep Learning on Embedded Accelerator-based platforms." *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems*, October 2016 (Best Paper Award)
[DOI: 10.1145/2968455.2968511]

8. Sidharth Maheshwari, Gourav Modi, **Siddhartha**, Nachiket Kapre "Vector FPGA Acceleration of 1-D DWT Computations using Sparse Matrix Skeletons." *26th IEEE International Conference on Field-Programmable Logic and Applications*, August 2016 (Poster)
[DOI: 10.1109/FPL.2016.7577361]

9. **Siddhartha**, Nachiket Kapre "Communication Optimization for the 16-core Epiphany Floating-Point Processor Array." *24th IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2016 (Short Paper)
[DOI: 10.1109/FCCM.2016.15]

10. Gopalakrishna Hegde, **Siddhartha**, Nachiappan Ramasamy, Vamsi Buddha, Nachiket Kapre "Evaluating Embedded FPGA Accelerators for Deep Learning Applications." *24th IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2016 (Short Paper)
[DOI: 10.1109/FCCM.2016.14]

11. Nachiket Kapre, Han Jianglei, Andrew Bean, Pradeep Moorthy, and **Siddhartha** "GraphMMU: Memory Management Unit for Sparse Graph Accelerators." *22nd Reconfigurable Architectures Workshop (co-located with IPDPS)*, May 2015
[DOI: 10.1109/IPDPSW.2015.101]

12. Pradeep Moorthy, **Siddhartha**, and Nachiket Kapre "A Case for Embedded FPGA-based SoCs for Energy-Efficient Acceleration of Graph Problems." *Supercomputing Frontiers 2015*, March 2015
[DOI: 10.14529/jsfi150307]

13. **Siddhartha**, Nachiket Kapre "FPGA Acceleration of Irregular Iterative Computations using Criticality-Aware Dataflow Optimizations." *International Symposium on Field-Programmable Gate Arrays*, February 2015 (Short Paper)
[DOI: 10.1145/2684746.2689110]

14. **Siddhartha**, Nachiket Kapre "Fanout Decomposition Dataflow Optimizations for FPGA-based Sparse LU Factorization." *International Conference on Field-Programmable Technology*, December 2014 (Short Paper)
[DOI: 10.1109/FPT.2014.7082787]

15. **Siddhartha**, Nachiket Kapre "Heterogeneous Dataflow Architectures for FPGA-based Sparse LU Factorization." *The International Conference on Field Programmable Logic and Applications*, September 2014 (Short Paper)
[DOI: 10.1109/FPL.2014.6927401]

16. Nachiket Kapre, **Siddhartha** "Limits of Statically-Scheduled Token Dataflow Processing." *International workshop on Data-Flow Models (DFM) for Extreme Scale Computing (co-located with PACT 2014)*, August 2014
[DOI: 10.1109/DFM.2014.21]

17. **Siddhartha**, Nachiket Kapre "Breaking Sequential Dependencies in FPGA-based Sparse LU Factorization." *International Symposium on Field Programmable Custom Computing Machines*, May 2014 (Short Paper)
[DOI: 10.1109/FCCM.2014.26]

Awards

Richard Newton Young Fellow Award, Design Automation Conference — June 2013

Teaching Experience

Project Supervisor, University of Sydney — Semesters 2018–Present
Guidance and supervision given to multiple undergraduate students on their final year project.

Teaching Assistant, NTU — Semesters 2014–2016
CE4054 - Programmable System on Chip,
CE4052 - Embedded Software Development

Extra-Curricular

Data Science Specialization — March 2015 – April 2016
John Hopkins University
- Offered via the Coursera platform, the Data Science Specialization teaches how to use the tools of the trade, think analytically about complex problems, manage large data sets, deploy statistical principles, create visualizations, build and evaluate machine learning algorithms, publish reproducible analyses, and develop data products.

Communication Coach — January 2014 – November 2016
School of Humanities and Social Sciences, NTU
- A university-wide coaching role on written & verbal communication skills for undergraduate and graduate students.