




### CONTACT INFORMATION

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### INTERESTS

Machine Learning, MLOps, FPGAs, HFT, HPC, RF Communications

### PROFESSIONAL SUMMARY

Experienced mid-career software engineer with a FPGA-focused research background looking for a fresh challenge. Especially interested in applied AI and ML infrastructure projects (e.g. MLOps), with/without hardware acceleration (e.g. FPGAs/ASICs) as an auxiliary goal. Referees on request.

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## Work Experience

### Machine Learning Engineer (Contract), SAP Singapore

Jun 2021 to Present

- Building enterprise search solutions for internal stakeholders using Elasticsearch/Opensearch stacks.
- Implementing DNN-based semantic-similarity algorithms for information retrieval and ranking of results.
- MLOps tooling: setting up labeling, data cleaning, and evaluation pipelines for efficient ML iterations.
- Tools/frameworks used (non-exhaustive): [Elastic|Open]search, Docker, Poetry, Kubernetes, Kibana, Grafana, etc.

### CTO/Founder, Inpact Technologies Pte Ltd (inPact.ai), Singapore

May 2020 to Sep 2021

- Led product development across all aspects of machine learning, frontend, backend, and deployment.
- Hired and managed contractors and an intern to meet product development targets regularly.
- Hands-on experience with technologies/frameworks such as ReactJS/Redux/SASS, serverless, spaCy, and more.
- Handled business functions such as customer acquisition, investor relations, fundraising, marketing, and more.
- Raised S\$75K from Entrepreneur First, an international VC firm funded by some of the top investors in the world.

### Postdoctoral Research Associate, University of Sydney, Australia

Oct 2017 to Dec 2019

- Research & development on a “High-Speed Machine Learning for RF Communications” project commissioned by the Australian Defense Agency, leading to a peer-reviewed publication at [MILCOM 2018](#).
- Contribution to other FPGA-based research projects in the lab on topics such as [on-chip training](#), [logic cell architecture design](#), and [automatic modulation classification](#). Total 5 research papers/posters published at peer-reviewed conferences.
- Supervision & guidance to undergraduate students on their final-year research projects.
- Sysadmin duties on available compute resources in the lab.

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## Education & Certifications

### Nanyang Technological University (NTU), Singapore

Jan 2013 to Feb 2019

PhD, Computer Science & Engineering, Advisor: [Nachiket Kapre](#)  
Dissertation: [Dataflow Optimized Overlays for FPGAs](#)  
Teaching Assistant: Programmable System on Chip (CE4054), Embedded Software Development (CE4052)

### Imperial College London, United Kingdom

Oct 2009 to Jun 2012

BEng, Electrical & Electronics Engineering, 2nd Upper Class Honors

### Machine Learning Engineering for Production (MLOps) Specialization, DeepLearning.AI

Ongoing

4-module specialization offered through the Coursera MOOC platform. Focuses on best in-industry practices for deploying data-centric machine learning systems. Instructors include Andrew Ng (founder DeepLearning.AI and Coursera), Robert Crowe (Tensorflow Developer Engineer, Google), Laurence Moroney (Lead AI Advocate, Google), and more.

### Data Science Specialization, John Hopkins University

Mar 2015 to Apr 2016

10-module specialization that covers concepts and tools essential for building effective data science pipelines. Capstone project on building a text-prediction R web-app, similar to the predictive text technology found in mobile phones today.

## Full Papers (Conferences/Journals)

1. Seyedramin Rasoulinezhad, **Siddhartha**, Hao Zhou, Lingli Wang, David Boland, and Philip Leong “LUXOR: An FPGA Logic Cell Architecture for Efficient Compressor Tree Implementations” *Proceedings of the 2020 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, February 2020  
[DOI: [10.1145/3373087.3375303](https://doi.org/10.1145/3373087.3375303)]
2. **Siddhartha**, and Nachiket Kapre “DaCO: A High-Performance Token Dataflow Coprocessor Overlay for FPGAs” *International Conference on Field-Programmable Technology*, December 2018  
[DOI: [10.1109/FPT.2018.00032](https://doi.org/10.1109/FPT.2018.00032)]
3. **Siddhartha**, Yee Hui Lee, Duncan Moss, Julian Faraone, Perry Blackmore, Daniel Salmond, David Boland, and Philip Leong “Long Short-Term Memory for Radio Frequency Spectral Prediction and its Real-Time FPGA Implementation” *IEEE Military Communications Conference (MILCOM)*, October 2018  
[DOI: [10.1109/MILCOM.2018.8599833](https://doi.org/10.1109/MILCOM.2018.8599833)]
4. **Siddhartha**, Nachiket Kapre “Hoplite-Q: Priority-Aware Routing in FPGA Overlay NoCs” *IEEE 26th Annual International Symposium on Field-Programmable Custom Computing Machines*, May 2018  
[DOI: [10.1109/FCCM.2018.00012](https://doi.org/10.1109/FCCM.2018.00012)]
5. Gopalakrishna Hegde, **Siddhartha**, Nachiket Kapre “CaffePresso: Accelerating Convolutional Networks on Embedded SoCs” *ACM Transactions on Embedded Computing Systems (TECS)*, January 2018  
[DOI: [10.1145/3105925](https://doi.org/10.1145/3105925)]
6. **Siddhartha**, Nachiket Kapre “eBSP: Managing NoC traffic for BSP workloads on the 16-core Adapteva Epiphany-III Processor.” *Design, Automation, and Test in Europe*, March 2017  
[DOI: [10.23919/DATE.2017.7926961](https://doi.org/10.23919/DATE.2017.7926961)]
7. Gopalakrishna Hegde, **Siddhartha**, Nachiappan Ramasamy, Nachiket Kapre “CaffePresso: An Optimized Library for Deep Learning on Embedded Accelerator-based platforms.” *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems*, October 2016 (Best Paper Award)  
[DOI: [10.1145/2968455.2968511](https://doi.org/10.1145/2968455.2968511)]
8. Pradeep Moorthy, **Siddhartha**, and Nachiket Kapre “A Case for Embedded FPGA-based SoCs for Energy-Efficient Acceleration of Graph Problems.” *Supercomputing Frontiers 2015*, March 2015  
[DOI: [10.14529/jsfi150307](https://doi.org/10.14529/jsfi150307)]

## Short Papers / Posters / Workshops

1. Stephen Tridgell, David Boland, Philip Leong, Ryan Kastner, Alireza Khodamoradi, and **Siddhartha** “Real-time Automatic Modulation Classification using RFSoc” *27th Reconfigurable Architectures Workshop (co-located with IPDPS 2020)*, May 2020  
[DOI: [10.1109/IPDPSW50202.2020.00021](https://doi.org/10.1109/IPDPSW50202.2020.00021)]
2. Stephen Tridgell, David Boland, Philip Leong, and **Siddhartha** “Real-time Automatic Modulation Classification” *International Conference on Field-Programmable Technology*, December 2019 (Poster)  
[DOI: [10.1109/ICFPT47387.2019.00052](https://doi.org/10.1109/ICFPT47387.2019.00052)]
3. **Siddhartha**, David Boland, Steve Wilton, Barry Flower, Perry Blackmore, and Philip Leong “Simultaneous Inference and Training using On-FPGA Weight Perturbation Techniques” *International Conference on Field-Programmable Technology*, December 2018 (Poster)  
[DOI: [10.1109/FPT.2018.00060](https://doi.org/10.1109/FPT.2018.00060)]
4. **Siddhartha**, Nachiket Kapre “Out-of-Order Dataflow Scheduling for FPGA Overlays.” *Overlay Architectures for FPGAs Workshop (co-located with FPGA 2017)*, February 2017 (Position Paper)  
[DOI: [arXiv:1705.02734](https://arxiv.org/abs/1705.02734)]
5. Sidharth Maheshwari, Gourav Modi, **Siddhartha**, Nachiket Kapre “Vector FPGA Acceleration of 1-D DWT Computations using Sparse Matrix Skeletons.” *26th IEEE International Conference on Field-Programmable Logic and Applications*, August 2016 (Poster)  
[DOI: [10.1109/FPL.2016.7577361](https://doi.org/10.1109/FPL.2016.7577361)]
6. **Siddhartha**, Nachiket Kapre “Communication Optimization for the 16-core Epiphany Floating-Point Processor Array.” *24th IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2016 (Short Paper)  
[DOI: [10.1109/FCCM.2016.15](https://doi.org/10.1109/FCCM.2016.15)]

7. Gopalakrishna Hegde, **Siddhartha**, Nachiappan Ramasamy, Vamsi Buddha, Nachiket Kapre “Evaluating Embedded FPGA Accelerators for Deep Learning Applications.” *24th IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2016 (Short Paper)  
[DOI: 10.1109/FCCM.2016.14]
8. Nachiket Kapre, Han Janglei, Andrew Bean, Pradeep Moorthy, and **Siddhartha** “GraphMMU: Memory Management Unit for Sparse Graph Accelerators.” *22nd Reconfigurable Architectures Workshop (co-located with IPDPS)*, May 2015  
[DOI: 10.1109/IPDPSW.2015.101]
9. **Siddhartha**, Nachiket Kapre “FPGA Acceleration of Irregular Iterative Computations using Criticality-Aware Dataflow Optimizations.” *International Symposium on Field-Programmable Gate Arrays*, February 2015 (Short Paper)  
[DOI: 10.1145/2684746.2689110]
10. **Siddhartha**, Nachiket Kapre “Fanout Decomposition Dataflow Optimizations for FPGA-based Sparse LU Factorization.” *International Conference on Field-Programmable Technology*, December 2014 (Short Paper)  
[DOI: 10.1109/FPT.2014.7082787]
11. **Siddhartha**, Nachiket Kapre “Heterogeneous Dataflow Architectures for FPGA-based Sparse LU Factorization.” *The International Conference on Field Programmable Logic and Applications*, September 2014 (Short Paper)  
[DOI: 10.1109/FPL.2014.6927401]
12. Nachiket Kapre, **Siddhartha** “Limits of Statically-Scheduled Token Dataflow Processing.” *International workshop on Data-Flow Models (DFM) for Extreme Scale Computing (co-located with PACT 2014)*, August 2014  
[DOI: 10.1109/DFM.2014.21]
13. **Siddhartha**, Nachiket Kapre “Breaking Sequential Dependencies in FPGA-based Sparse LU Factorization.” *International Symposium on Field Programmable Custom Computing Machines*, May 2014 (Short Paper)  
[DOI: 10.1109/FCCM.2014.26]