

Siddhartha

CONTACT INFORMATION	7, Woodsvale Condominium, #06-13 Woodlands Drive 72, S738092	065-9857 4171 siddhart005@e.ntu.edu.sg sidmontu.com
RESEARCH INTERESTS	Embedded Systems Design, FPGA/GPU Computing, Hardware Design, Graph Problems, Numerical Computing, Machine Learning	
EDUCATION	Nanyang Technological University , Singapore Ph.D., Embedded Systems Design, <i>Expected:</i> Winter 2016 <ul style="list-style-type: none">• Current Project Area: <i>Dataflow Computing Model for Heterogeneous Embedded Coprocessors</i>• Advisors: Nachiket Kapre, Assistant Professor Imperial College London , London, United Kingdom B.Eng., Electrical & Electronics Engineering, Jun 2012	
RESEARCH EXPERIENCE	Research Student Centre of High Performance Embedded Systems (CHiPES), Nanyang Technological University Supervisor: Nachiket Kapre, Assistant Professor Research Assistant Circuits & Systems Research Group, EEE, Imperial College London Supervisors: Nachiket Kapre, Assistant Professor	Jan 2013 to present June 2012 to Oct. 2012
AWARDS	Richard Newton Young Fellow Award, Design Automation Conference	Jun 2013
PROGRAMMING SKILLS	Software: <ul style="list-style-type: none">• C, C++, R, Java, Bash, Python, L^AT_EX, MATLAB, Pascal, PHP, Javascript, MySQL, and others Hardware: <ul style="list-style-type: none">• VHDL, Verilog, SystemVerilog, Vivado HLS, CUDA, MaxIDE	
SERVICE	Communication Coach, School of Humanities & Social Sciences <ul style="list-style-type: none">• Coaching graduate/undergraduate students on both written & verbal communication skills	Jan 2014 – Present
REFERENCES	Nachiket Kapre Assistant Professor, School of Computer Engineering, Nanyang Technological University	Phone: 065-6513 8042 E-mail: nachiket@ntu.edu.sg

Publications

- OCTOBER 2016 CaffePresso: An Optimized Library for Deep Learning on Embedded Accelerator-based platforms
Gopalakrishna Hegde, **Siddhartha**, Nachiappan Ramasamy, Nachiket Kapre
International Conference on Compilers, Architecture, and Synthesis for Embedded Systems
DOI: Upcoming
- AUGUST 2016 Vector FPGA Acceleration of 1-D DWT Computations using Sparse Matrix Skeletons
Sidharth Maheshwari, Gourav Modi, **Siddhartha**, Nachiket Kapre
26th IEEE International Conference on Field-Programmable Logic and Applications
DOI: Upcoming
- MAY 2016 Communication Optimization for the 16-core Epiphany Floating-Point Processor Array
Siddhartha, Nachiket Kapre
24th IEEE International Symposium on Field-Programmable Custom Computing Machines
DOI: 10.1109/FCCM.2016.15
- MAY 2016 Evaluating Embedded FPGA Accelerators for Deep Learning Applications
Gopalakrishna Hegde, **Siddhartha**, Nachiappan Ramasamy, Vamsi Buddha, Nachiket Kapre
24th IEEE International Symposium on Field-Programmable Custom Computing Machines
DOI: 10.1109/FCCM.2016.14
- MAY 2015 GraphMMU: Memory Management Unit for Sparse Graph Accelerators
Nachiket Kapre, Han Janglei, Andrew Bean, Pradeep Moorthy, and **Siddhartha**
22nd Reconfigurable Architectures Workshop 2015 (co-located with IPDPS 2015)
DOI: 10.1109/IPDPSW.2015.101
- MAR 2015 A Case for Embedded FPGA-based SoCs for Energy-Efficient Acceleration of Graph Problems
Pradeep Moorthy, **Siddhartha**, and Nachiket Kapre
Supercomputing Frontiers 2015
DOI: 10.14529/jsfi150307
- FEB 2015 FPGA Acceleration of Irregular Iterative Computations using Criticality-Aware Dataflow Optimizations
Siddhartha, and Nachiket Kapre
International Symposium on Field-Programmable Gate Arrays
DOI: 10.1145/2684746.2689110

- DEC 2014 Fanout Decomposition Dataflow Optimizations for FPGA-based Sparse LU Factorization
Siddhartha, and Nachiket Kapre
International Conference on Field-Programmable Technology
DOI: 10.1109/FPT.2014.7082787
- SEP 2014 Heterogeneous Dataflow Architectures for FPGA-based Sparse LU Factorization
Siddhartha, and Nachiket Kapre
The International Conference on Field Programmable Logic and Applications
DOI: 10.1109/FPL.2014.6927401
- AUG 2014 Limits of Statically-Scheduled Token Dataflow Processing
Nachiket Kapre, and **Siddhartha**
The International workshop on "Data-Flow Models (DFM) for extreme scale computing"
DOI: 10.1109/DFM.2014.21
- MAY 2014 Breaking Sequential Dependencies in FPGA-based Sparse LU Factorization
Siddhartha, and Nachiket Kapre
International Symposium on Field Programmable Custom Computing Machines
DOI: 10.1109/FCCM.2014.26