Siddhartha

Software/Hardware Engineer

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Personal Statement

Experienced mid-career software engineer with a FPGA-focused research background looking for a fresh challenge. Especially interested in applied AI and ML engineering projects (e.g. MLOps), with/without hardware acceleration (e.g. FPGAs/ASICs) as an auxiliary goal.

Software Experience

- UNIX and CLI
- Python3
- PyTorch / Tensorflow / spaCy
- C/C++ programming
- ReactJS / Redux / SASS
- Data analysis/visualizations in R

Hardware Experience

- Foundational knowledge
- Verilog / Verilator
- FPGA toolchains: Vivado & Quartus
- VivadoHLS / PYNQ Frameworks
- RF communication (Ettus RFNoC Framework)

Deployment Experience

- AWS cloud services
- Docker & docker-compose
- Unit-testing & coverage
- TravisCI automated builds

Work Experience

Jun'21 – Present **Machine Learning Engineer (Contract)** SAP Asia Pte Ltd

- Part of the machine learning engineering team that builds scalable and production-ready ML solutions for internal stakeholders.
- Worked with [Elastic|Open]Search, Docker, FastAPI, Agile, ReactJS, etc.

Feb'20 – Present **Founder & CTO** inPact AI

- Led product development across all aspects of machine learning, frontend, backend, and deployment.
- Hired and managed two contractors and an intern to meet regular product development targets.
- Hands-on product development experience with ReactJS, serverless framework, and AWS cloud infrastructure.
- Handled business functions such as customer acquisition, corporate partnerships, investor relations, fundraising, marketing, and more.
- Raised S$75K pre-seed from Entrepreneur First, an international VC firm funded by Reid Hoffman (founder of LinkedIn), founders of DeepMind and PayPal, and some of the top investors in the world.

Oct'17 – Dec'19 **Postdoctoral Research Associate** University of Sydney

- Conducted research on: next-generation FPGA (overlay) architectures, low-precision deep neural networks, on-chip machine learning, and RF communication systems (Ettus RFNoC framework).
- Core team member on a high-speed machine learning project for RF communications using FPGAs.
- (Co-)Authored 5 peer-reviewed research papers/posters.
- Supervised final year undergraduate projects, assisted with teaching/invigilation, and undertook sysadmin duties over lab resources.

Education

2013 – 2019 **Doctor of Philosophy** Nanyang Technological University, Singapore

Dissertation: Dataflow Optimized Overlays for FPGAs

Supervisor: Dr. Nachiket Kapre

- Developed DaCO, a Dataflow Coprocessor Overlay optimized for Arria 10 FPGAs.
- Key research contributions: (1) custom dataflow scheduling circuit that enables large-scale out-of-order instruction execution at runtime, (2) priority-aware NoC packet routing for criticality-aware dataflow communication, and (3) compiler support to optimize dataflow graphs for better runtime performance.
- (Co-)Authored a total of 15 research papers/posters during the candidacy.

2009 – 2012 **Bachelors of Engineering (BEng)** Imperial College London

Faculty of Electrical & Electronics Engineering, graduated with a second-upper class honors degree.

Certifications

Ongoing *Machine Learning Engineering for Production (MLOps) Specialization*

Coursera MOOC offered by DeepLearning.AI

4-module specialization focusing on best in-industry practices for deploying data-centric machine learning systems. Instructors include Andrew Ng (founder DeepLearning.AI and Coursera), Robert Crowe (Tensorflow Developer Engineer, Google), Laurence Moroney (Lead AI Advocate, Google), and more.

Apr 2016 *Data Science Specialization*

Coursera MOOC offered by John Hopkins University

10-module specialization that covers concepts and tools essential for building effective data science pipelines. Instructors include Jeff Leek, Roger D. Peng, and Brian Caffo, all of whom are professors at John Hopkins university.