Siddhartha

Machine Learning/FPGA Engineer

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Personal Statement

Experienced mid-career software engineer with a FPGA-focused research background looking for a fresh challenge. Especially interested in applied AI and machine learning engineering projects, with/without hardware acceleration (e.g. FPGAs/ASICs) as an auxiliary goal.

Hardware

- Strong foundational experience
- Proficient with (System)Verilog
- Familiar with FPGA tools
- VivadoHLS / PYNQ Framework
- RF communication (Ettus RFNoC Framework)

Software

- Experienced with UNIX and CLI
- Strong Python developer
- PyTorch/Tensorflow + Tensorpack machine learning frameworks
- MLOps tools such as MLFlow, Hub, and Label Studio
- Product design with ReactJS / Redux / SASS
- Data analysis/visualizations in R
- C/C++ programming on embedded systems
- Typesetting with LaTeX

Deployment

- Hands-on experience with AWS cloud products
- Serverless Application Framework
- Cortex.dev for ML inference deployment and monitoring

Work Experience

Feb'20 – Present **Founder, CTO & Director** inPact.ai

- Led product development across all aspects of machine learning, frontend, backend, and deployment.
- Hired and managed contractors and an intern to meet product development targets regularly. Enforced good development practices such as version control, linters, code reviews, etc.
- Gained hands-on development experience with MLOps tools: Label studio for data annotation, MLFlow for model registry, Hub for dataset/feature store, and Cortex.dev for model deployment.
- Hands-on experience with ReactJS and serverless frameworks. Setup inPact's cloud infrastructure on AWS – used a myriad of AWS cloud services such as Cognito, DynamoDB, S3, SNS, Lambda, etc.
- Handled business functions such as customer acquisition, corporate partnerships, investor relations, fundraising, marketing, and more.
- Raised S$75K pre-seed from Entrepreneur First, an international VC firm funded by Reid Hoffman (founder of LinkedIn), founders of DeepMind and PayPal, and some of the top investors in the world.

Oct'17 – Dec'19 **Postdoctoral Research Associate** University of Sydney

- Conducted research on: next-generation FPGA (overlay) architectures, low-precision deep neural networks, on-chip machine learning, and RF communication systems (Ettus RFNoC framework).
- Core team member on a project (High-Speed Machine Learning for RF Communication) commissioned by the Australian Defense Force.
- (Co-)Authored 5 peer-reviewed research papers/posters during the stint at the lab.
- Supervised final year undergraduate projects, assisted with teaching/invigilation, and undertook sysadmin duties over lab resources.

Education

2013 – 2019 **Doctor of Philosophy** Nanyang Technological University, Singapore

Dissertation: Dataflow Optimized Overlays for FPGAs

Supervisor: Dr. Nachiket Kapre

- Introduced DaCO, a Dataflow Coprocessor Overlay optimized for Arria 10 FPGAs.
- Key research contributions: (1) custom dataflow scheduling circuit that enables large-scale out-of-order instruction execution at runtime, (2) priority-aware NoC packet routing for criticality-aware dataflow communication, and (3) compiler support to optimize dataflow graphs for better runtime performance.
- (Co-)Authored a total of 15 research papers/posters/journals at top-tier IEEE conferences during the candidacy.

2009 – 2012 **Bachelors of Engineering (BEng)** Imperial College London

Faculty of Electrical & Electronics Engineering, graduated with a second-upper class honors degree.

Notable Publications

Google Scholar

2018 **DaCO: A High-Performance Token Dataflow Coprocessor Overlay for FPGAs**
Siddhartha, Nachiket Kapre
International Conference on Field-Programmable Technology

2020 **LUXOR: An FPGA Logic Cell Architecture for Eficient Compressor Tree Implementations**
Seyedramin Rasoulinezhad, Siddhartha, Hao Zhou, Lingli Wang, David Boland, Philip Leong
ACM/SIGDA International Symposium on FPGAs

2018 **Long Short-Term Memory for Radio Frequency Spectral Prediction and its Real-Time FPGA Implementation**
Siddhartha, Yee Hui Lee, Duncan Moss, Julian Faraone, Perry Blackmore, Daniel Salmond, David Boland, and Philip Leong
IEEE Military Communications Conference (MILCOM)

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