Siddhartha

Machine Learning / FPGA Engineer

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WORK EXPERIENCE

Feb 2020 - Present — Singapore

Founder, CTO, Director
inPact.ai

- Led product development across all aspects of machine learning, frontend, backend, and deployment.
- Hired and managed contractors and an intern to meet product development targets regularly. Enforced good development practices such as version control, linters, code reviews, etc.
- Gained hands-on development experience with MLOps tools: Label studio for data annotation, MLFlow for model registry, Hub for dataset/feature store, and Cortex.dev for model deployment.
- Hands-on experience with ReactJS and serverless frameworks. Setup inPact's cloud infrastructure on AWS – used a myriad of AWS cloud services such as Cognito, DynamoDB, S3, SNS, Lambda, etc.
- Handled business functions such as customer acquisition, corporate partnerships, investor relations, fundraising, marketing, and more.
- Raised S$75K pre-seed from Entrepreneur First, an international VC firm funded by Reid Hoffman (founder of LinkedIn), founders of DeepMind and PayPal, and some of the top investors in the world.

Oct 2017 - Dec 2019 — Sydney, Australia

Postdoctoral Research Associate
University of Sydney

- Conducted research on: next-generation FPGA (overlay) architectures, low-precision deep neural networks, on-chip machine learning, and RF communication systems (Ettus RFNoC framework).
- Core team member on a project (High-Speed Machine Learning for RF Communication) commissioned by the Australian Defense Force.
- (Co-)Authored 5 research papers/posters during the stint at the lab.
- Supervised final year undergraduate projects, assisted with teaching/invigilation, and undertook sysadmin duties over lab resources.

SKILLS & COMPETENCIES

PyTorch / Tensorflow
C / C++
Verilog / VHDL
Typesetting in LaTeX
PyTorch / Tensorflow
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EDUCATION

Jan 2013 - Jan 2019 — Singapore

PhD, Computer Science & Engineering
Nanyang Technological University (NTU)
Dissertation Title: Dataflow Optimized Overlays for FPGAs
Supervisor: Dr. Nachiket Kapre

- Introduces DaCO, a Dataflow Coprocess Overlay optimized for the Arria 10 FPGAs. Research challenges addressed include:
- Custom dataflow scheduling circuit that enables large-scale out-of-order instruction execution at runtime,
- Priority-aware NoC packet routing for improved criticality-aware dataflow communication, and
- Compiler support that optimizes the dataflow graph for improved runtime execution.
- (Co-)Authored a total of 15 research papers/posters/journals at top-tier IEEE conferences during the candidacy.

Oct 2009 - Jun 2012 — London, UK

Bachelors of Engineering (BEng)
Electrical & Electronics Engineering (EEE)
Imperial College London

NOTABLE PUBLICATIONS

- **DaCO: A High-Performance Token Dataflow Coprocessor Overlay for FPGAs**, *Siddhartha, Nachiket Kapre*, International Conference on Field-Programmable Technology 2018
- **Hoplite-Q: Priority-Aware Routing in FPGA Overlay NoCs**, *Siddhartha, Nachiket Kapre*, IEEE International Symposium on Field-Programmable Custom Computing Machines 2018
- **LUXOR: An FPGA Logic Cell Architecture for Efficient Compressor Tree Implementations**, *Seyedramin Rasoulinezhad, Siddhartha, Hao Zhou, Lingli Wang, David Boland, Philip Leong*, ACM International Symposium on FPGAs 2020
- **Long Short-Term Memory for Radio Frequency Spectral Prediction and its Real-Time FPGA Implementation**, *Siddhartha, Yee Hui Lee, Duncan Moss, Julian Faraone, Perry Blackmore, Daniel Salmond, David Boland, and Philip Leong*, IEEE Military Communications Conference 2018
- **Real-Time Automatic Modulation Classification using RFSoC**, *Stephen Tridgell, David Boland, Philip Leong, Ryan Kastner, Alireza Khodamoradi, Siddhartha*, 27th Reconfigurable Architectures Workshop 2020

INTERESTS

Applied AI
Computer Vision
Natural Language Processing
Computer Architecture
FPGA Technologies
RF Communication Systems