

Siddhartha

Machine Learning / FPGA Engineer

CONTACT INFORMATION



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INTERESTS

Machine Learning, FPGAs, HPC, RF Communications

PROFESSIONAL SUMMARY

Seasoned researcher interested in FPGAs and efficient architectures for deep learning applications. My past research projects involve developing high-speed, low-latency machine learning solutions for RF communication systems on the Xilinx RFSoc board, building token dataflow overlay architectures for accelerating highly sparse and irregular workloads, and more.

For the last 12 months, I have been building AI-driven products as a founder of my own company (inPact.ai). I have worn multiple hats in this role; from core technology development of the complete product stack (frontend, backend, and AI) to founder duties that include hiring, customer acquisition, fundraising, project management, etc.

EXPERIENCE

CTO/Founder

May 2020 to Present

Inpact Technologies Pte Ltd (inPact.ai), Singapore

As a CTO:

- Led product development across all aspects of machine learning, frontend, backend, and deployment.
- Hired and managed contractors and an intern to meet product development targets regularly. Enforced good development practices such as version control, linters, code reviews, etc.
- Gained hands-on development experience with MLOps tools: Label studio for data annotation, MLFlow for model registry, Hub for dataset/feature store, and Cortex.dev for model deployment.
- Hands-on experience with ReactJS and serverless frameworks. Setup inPact's cloud infrastructure on AWS – used a myriad of AWS cloud services such as Cognito, DynamoDB, S3, SNS, Lambda, etc.

As a Founder:

- Handled business functions such as customer acquisition, corporate partnerships, investor relations, fundraising, marketing, and more.
- Raised S\$75K pre-seed from Entrepreneur First, an international VC firm funded by Reid Hoffman (founder of LinkedIn), founders of DeepMind and PayPal, and some of the top investors in the world.

Founder in Residence

Jan 2020 to May 2020

Entrepreneur First (EF) Singapore (Batch SG7)

EF is a talent investor that brings together intelligent and ambitious people into a highly-charged environment where they are presented with the opportunity to find a suitable co-founder and launch a brand new company from the ground up. The 3-month program is run and supervised by experienced (ex-)entrepreneurs who test your business ideas and team chemistry regularly during weekly check-ins. At the end of the 3-month program, founders pitch their ideas (with traction/validation) to an internal investment committee, where founders then receive pre-seed capital if successful.

inPact was one of the ten successful companies (SG7 batch) to receive funds from EF in May 2020.

Postdoctoral Research Associate October 2017 to December 2019

Computing Engineering Lab,
School of Electrical and Information Engineering
University of Sydney
Supervisors: Philip Leong, David Boland

Responsibilities included: research & development on the “High-Speed Machine Learning for RF Communications” project commissioned by the Australian Defense Agency, research & development on other ongoing projects in the lab (5 papers published at peer-reviewed conferences), supervising final-year undergraduate students on their research projects, sysadmin duties on local compute resources, etc.

Research Assistant July 2012 to September 2012

Circuits and Systems Research Group,
Electrical and Electronics Engineering Department
Imperial College London
Supervisor: Nachiket Kapre

Undergraduate researcher hired under the Imperial College UROP program, on recommendation from supervisor Dr. Nachiket Kapre. Worked on acyclic dataflow graph reassociation techniques for sparse matrix workloads; work that eventually served as a foundation for subsequent PhD research and was published in peer-reviewed conferences.

EDUCATION

Nanyang Technological University (NTU), Singapore

PhD, Computer Science & Engineering, February 2019

- Dissertation Title: *Dataflow Optimized Overlays for FPGAs*
- Advisor: Nachiket Kapre

Imperial College London, London, United Kingdom

BEng, Electrical & Electronics Engineering, June 2012

TEACHING

Project Supervisor, University of Sydney Semesters 2018–2019

Responsibilities: Guidance and supervision to undergraduate students on their final year projects.

Teaching Assistant, NTU Semesters 2014–2016

CE4054 - Programmable System on Chip,
CE4052 - Embedded Software Development

EXTRA-
CURRICULAR

Data Science Specialization March 2015 – April 2016

John Hopkins University

- Offered via the Coursera platform, the Data Science Specialization teaches how to use the tools of the trade, think analytically about complex problems, manage large data sets, employ statistical methodologies, create visualizations, build and evaluate machine learning algorithms, publish reproducible analyses, and develop data products. Capstone project delivered a text-prediction R web-app, similar to the predictive text technology found in mobile phones today.

1. Seyedramin Rasoulinezhad, **Siddhartha**, Hao Zhou, Lingli Wang, David Boland, and Philip Leong “LUXOR: An FPGA Logic Cell Architecture for Efficient Compressor Tree Implementations” *Proceedings of the 2020 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA)*, February 2020
[DOI: 10.1145/3373087.3375303]
2. **Siddhartha**, and Nachiket Kapre “DaCO: A High-Performance Token Dataflow Coprocessor Overlay for FPGAs” *International Conference on Field-Programmable Technology*, December 2018
[DOI: 10.1109/FPT.2018.00032]
3. **Siddhartha**, Yee Hui Lee, Duncan Moss, Julian Faraone, Perry Blackmore, Daniel Salmond, David Boland, and Philip Leong “Long Short-Term Memory for Radio Frequency Spectral Prediction and its Real-Time FPGA Implementation” *IEEE Military Communications Conference (MILCOM)*, October 2018
[DOI: 10.1109/MILCOM.2018.8599833]
4. **Siddhartha**, Nachiket Kapre “Hoplite-Q: Priority-Aware Routing in FPGA Overlay NoCs” *IEEE 26th Annual International Symposium on Field-Programmable Custom Computing Machines*, May 2018
[DOI: 10.1109/FCCM.2018.00012]
5. Gopalakrishna Hegde, **Siddhartha**, Nachiket Kapre “CaffePresso: Accelerating Convolutional Networks on Embedded SoCs” *ACM Transactions on Embedded Computing Systems (TECS)*, January 2018
[DOI: 10.1145/3105925]
6. **Siddhartha**, Nachiket Kapre “eBSP: Managing NoC traffic for BSP workloads on the 16-core Adapteva Epiphany-III Processor.” *Design, Automation, and Test in Europe*, March 2017
[DOI: 10.23919/DATE.2017.7926961]
7. Gopalakrishna Hegde, **Siddhartha**, Nachiappan Ramasamy, Nachiket Kapre “CaffePresso: An Optimized Library for Deep Learning on Embedded Accelerator-based platforms.” *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems*, October 2016 (Best Paper Award)
[DOI: 10.1145/2968455.2968511]
8. Pradeep Moorthy, **Siddhartha**, and Nachiket Kapre “A Case for Embedded FPGA-based SoCs for Energy-Efficient Acceleration of Graph Problems.” *Supercomputing Frontiers 2015*, March 2015
[DOI: 10.14529/jsfi150307]

Short Papers / Posters / Workshops

1. Stephen Tridgell, David Boland, Philip Leong, Ryan Kastner, Alireza Khodamoradi, and **Siddhartha** “Real-time Automatic Modulation Classification using RFSoc” *27th Reconfigurable Architectures Workshop (co-located with IPDPS 2020)*, May 2020
[DOI: TBA]
2. Stephen Tridgell, David Boland, Philip Leong, and **Siddhartha** “Real-time Automatic Modulation Classification” *International Conference on Field-Programmable Technology*, December 2019 (Poster)
[DOI: 10.1109/ICFPT47387.2019.00052]

3. **Siddhartha**, David Boland, Steve Wilton, Barry Flower, Perry Blackmore, and Philip Leong “Simultaneous Inference and Training using On-FPGA Weight Perturbation Techniques” *International Conference on Field-Programmable Technology*, December 2018 (Poster)
[DOI: [10.1109/FPT.2018.00060](https://doi.org/10.1109/FPT.2018.00060)]
4. **Siddhartha**, Nachiket Kapre “Out-of-Order Dataflow Scheduling for FPGA Overlays.” *Overlay Architectures for FPGAs Workshop (co-located with FPGA 2017)*, February 2017 (Position Paper)
[DOI: [arXiv:1705.02734](https://arxiv.org/abs/1705.02734)]
5. Sidharth Maheshwari, Gourav Modi, **Siddhartha**, Nachiket Kapre “Vector FPGA Acceleration of 1-D DWT Computations using Sparse Matrix Skeletons.” *26th IEEE International Conference on Field-Programmable Logic and Applications*, August 2016 (Poster)
[DOI: [10.1109/FPL.2016.7577361](https://doi.org/10.1109/FPL.2016.7577361)]
6. **Siddhartha**, Nachiket Kapre “Communication Optimization for the 16-core Epiphany Floating-Point Processor Array.” *24th IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2016 (Short Paper)
[DOI: [10.1109/FCCM.2016.15](https://doi.org/10.1109/FCCM.2016.15)]
7. Gopalakrishna Hegde, **Siddhartha**, Nachiappan Ramasamy, Vamsi Buddha, Nachiket Kapre “Evaluating Embedded FPGA Accelerators for Deep Learning Applications.” *24th IEEE International Symposium on Field-Programmable Custom Computing Machines*, May 2016 (Short Paper)
[DOI: [10.1109/FCCM.2016.14](https://doi.org/10.1109/FCCM.2016.14)]
8. Nachiket Kapre, Han Jianglei, Andrew Bean, Pradeep Moorthy, and **Siddhartha** “GraphMMU: Memory Management Unit for Sparse Graph Accelerators.” *22nd Reconfigurable Architectures Workshop (co-located with IPDPS)*, May 2015
[DOI: [10.1109/IPDPSW.2015.101](https://doi.org/10.1109/IPDPSW.2015.101)]
9. **Siddhartha**, Nachiket Kapre “FPGA Acceleration of Irregular Iterative Computations using Criticality-Aware Dataflow Optimizations.” *International Symposium on Field-Programmable Gate Arrays*, February 2015 (Short Paper)
[DOI: [10.1145/2684746.2689110](https://doi.org/10.1145/2684746.2689110)]
10. **Siddhartha**, Nachiket Kapre “Fanout Decomposition Dataflow Optimizations for FPGA-based Sparse LU Factorization.” *International Conference on Field-Programmable Technology*, December 2014 (Short Paper)
[DOI: [10.1109/FPT.2014.7082787](https://doi.org/10.1109/FPT.2014.7082787)]
11. **Siddhartha**, Nachiket Kapre “Heterogeneous Dataflow Architectures for FPGA-based Sparse LU Factorization.” *The International Conference on Field Programmable Logic and Applications*, September 2014 (Short Paper)
[DOI: [10.1109/FPL.2014.6927401](https://doi.org/10.1109/FPL.2014.6927401)]
12. Nachiket Kapre, **Siddhartha** “Limits of Statically-Scheduled Token Dataflow Processing.” *International workshop on Data-Flow Models (DFM) for Extreme Scale Computing (co-located with PACT 2014)*, August 2014
[DOI: [10.1109/DFM.2014.21](https://doi.org/10.1109/DFM.2014.21)]
13. **Siddhartha**, Nachiket Kapre “Breaking Sequential Dependencies in FPGA-based Sparse LU Factorization.” *International Symposium on Field Programmable Custom Computing Machines*, May 2014 (Short Paper)
[DOI: [10.1109/FCCM.2014.26](https://doi.org/10.1109/FCCM.2014.26)]