Assignment – 1

ASSIGNMENT - 1

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1) Draw the internal architectural block diagram of 8085 microprocessor and explain working of each block of 8085 in brief.

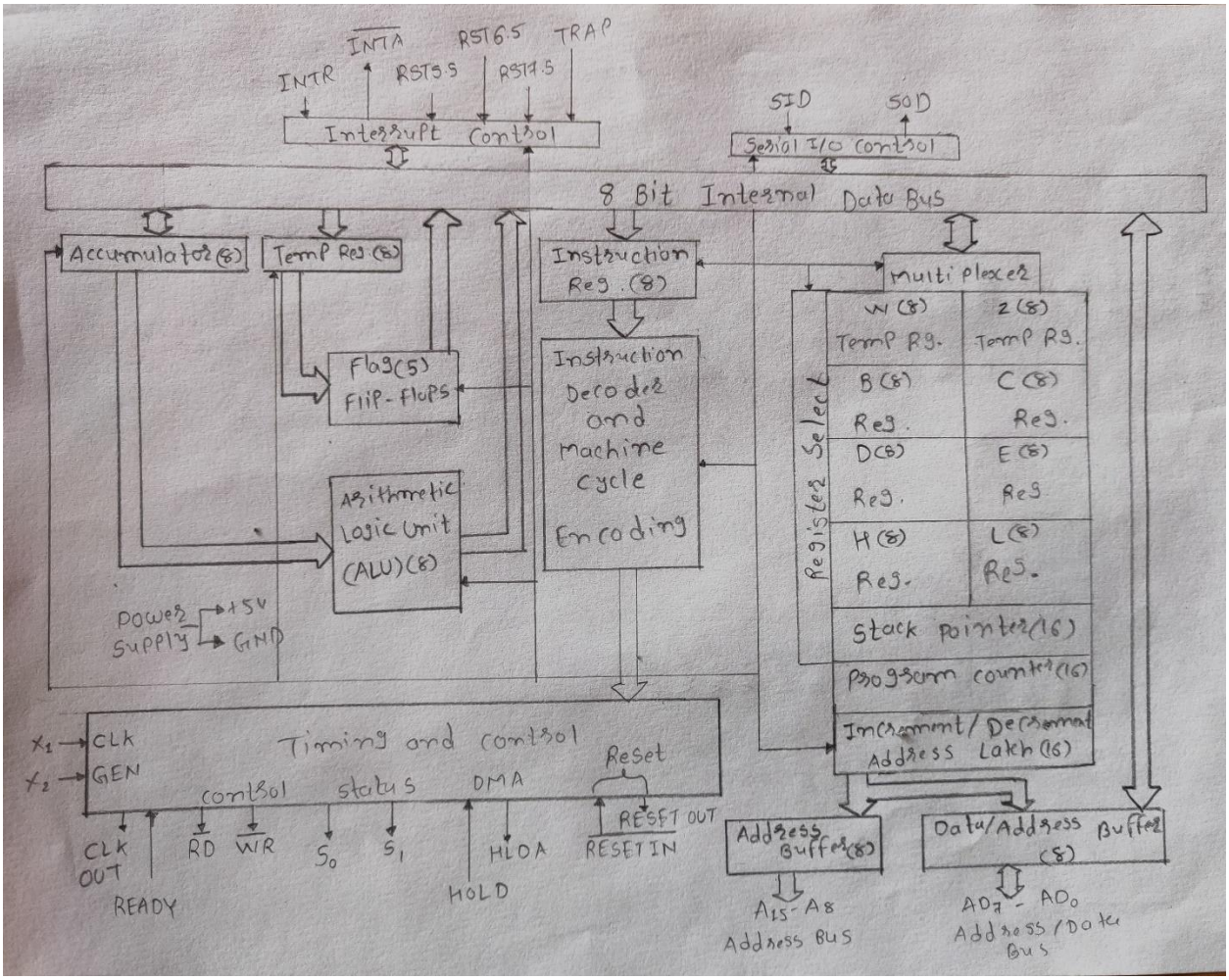
→ 8085 consists of the following functional units.

⇒ Accumulator:
It is an 8-bit register used to perform arithmetic logical, I/O & LOAD / STORE operations. It is connected to internal data bus & ALU. Result of operation is stored in Accumulator.

⇒ Asithmetic and logic unit:
As the name suggests, It performs arithmetic and logical operations like Addition, Subtraction, AND, OR etc. on 8-bit data.

⇒ General Purpose Register:
There are 6 general purpose registers in 8085 processor, i.e. B, C, D, E, H & L. Each register can hold 8-bit data. These registers can work in pair to hold 16-bit data and their pairing combination is like B-C, D-E & H-L.

⇒ Program counter:
It is a 16-bit register used to store the memory address location of the next instruction to be executed. Microprocessor increments the program whenever an instruction is being executed, so that the program counter points to the memory address of the next instruction that is going to be executed.


INTR
INTA
RST5.5
RST6.5
RST7.5
TRAP
Interrupt control
SID
SOD
Serial I/O control
8 Bit Internal Data Bus
Accumulator (8)
Temp Reg. (8)
Instruction Reg. (8)
Multiplexer
Flag (5) Flip-Flops
Instruction Decoder and Machine Cycle Encoding
Arithmetic Logic Unit (ALU) (8)
Register Select
W (8) Temp Rg.
Z (8) Temp Rg.
B (8) Reg.
C (8) Reg.
D (8) Reg.
E (8) Reg
H (8) Reg.
L (8) Reg.
Stack pointer (16)
Program counter (16)
Increment/Decrement Address Latch (16)
Power Supply
+5V
GND
X1
X2
CLK GEN
Timing and control
control
status
DMA
Reset
CLK OUT
READY
RD
WR
S0
S1
HLDA
HOLD
RESET OUT
RESET IN
Address Buffer (8)
Data/Address Buffer (8)
A15 - A8
Address Bus
AD7 - AD0
Address/Data Bus

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⇒ Stack Pointer:
It is also a 16-bit register works like stack, which is always incremented/ decremented by 2 during push & pop operations.

⇒ Temporary register:
It is an 8-bit register, which holds the temporary data of arithmetic and logical operations.

⇒ Flag register:
It is an 8-bit register having 1-bit flip-flops, which holds either 0 or 1 depending upon the result stored in the accumulator.
sign (S): set (1) if 7th bit of result is 1; else (0)
zero (Z): Set (1) if result is zero, else (0).
Auxiliary Carry (AC): Set (1) if carry bit is generated by 3rd bit & passed to bit 4th bit.
Parity (P): Set (1) if result has even no of 1's & Reset (0) if result has odd no of 1's.
Carry (CY): Set (1) if arithmetic operation results in carry; else (0).

⇒ Instruction register and decoder:
It is an 8-bit register. When an instruction is fetched from memory then it is stored in the instruction register. Instruction decoder decodes the information present in the instruction register.

⇒ Timing and control unit:
It provides timing and control signal to the microprocessor to perform operations. Following are the timing and control signals, which control external

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and internal circuits.
control signals: READY, $\overline{RD}$, $\overline{WR}$, ALE
status signals: S0, S1, IO/$\overline{M}$
DMA signals: HOLD, HLDA
RESET signals: RESET IN, RESET OUT

⇒ Interrupt control:
As the name suggests it controls the interrupts during a process. When a microprocessor is executing a main program and whenever an interrupt occurs, the microprocessor shifts the control from the main program to process the incoming request. After the request is completed the control goes back to the main program.
There are 5 interrupt signals in 8085 microprocessor INTR, RST 7.5, RST 6.5, RST 5.5, TRAP.

⇒ Serial Input / output control
It controls the serial data communication by using these two instructions: SID (serial Input data) and SOD (serial output data).

⇒ Address buffer and address-data buffer
The content stored in the stack Pointer and Program counter is loaded into the address buffer and address-data buffer to communicate with the CPU. The memory and I/O chips are connected to these buses; the CPU can exchange the desired data with the memory and I/O ~~chips~~ chips

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=> Address bus:

Whereas address bus carries the location to where it should be stored and it is unidirectional. It is used to transfer the data & Address I/O devices. Group of 16 unidirectional lines generally identified as A0 to A15. The bits flow from microprocessor to Peripheral devices. 16 address lines are capable of addressing 65536 memory locations, so, 8085 has 64K memory locations.

=> data bus:

Data bus carries the data to be stored. It is bidirectional. Group of 8 lines Identified as D0 to D7. 8 data lines enable microprocessor to manipulate data ranging from 00H to FFH (2^8=256 numbers). Largest number appears on data bus is 1111 1111 => $(255)_{10}$. As Data bus is of 8-bit, 8085 is known as 8-bit microprocessor.

=> multiplexes:

A multiplexer pulls out the right group of bits depending on the instruction.

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(2) List and explain 8085 addressing modes with suitable example.

→ Addressing Modes in 8085
1) Immediate
2) Direct
3) Register Addressing
4) Indirect
4) Implicit

1) Immediate Addressing mode:
→ In this mode, the 8/16-bit data is specified in the instruction itself as one of its operand.
→ Ex
MVI B, 20H
LXI D, 1034H

2) Direct Addressing Mode:
→ In this type of addressing mode, the 8 or 16-bit memory address is directly provided with the instruction.
→ Ex
LDA 1035H
IN 8-bit Port
OUT 8-bit Port

3) Register Addressing mode:
→ This type of addressing mode specifies register or register pair that contains data.
→ Ex
MOV A, B
ADD B

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4) Indirect addressing mode:
→ In this type of addressing mode, 16-bit memory address is indirectly provided with the instruction using a register pair.
→ Ex

```
LDAX   D ; A ← M[DE]
STAX   D : A → M[DE]
```

5) Implicit / Implied Addressing mode:
→ This mode doesn't require any operand; the data is specified by the opcode itself.
→ Ex

```
CMP
CMA
```

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3) Draw and explain the pin diagram of 8085 microprocessor.

⇒ The pins of an 8085 microprocessor can be classified into seven groups.

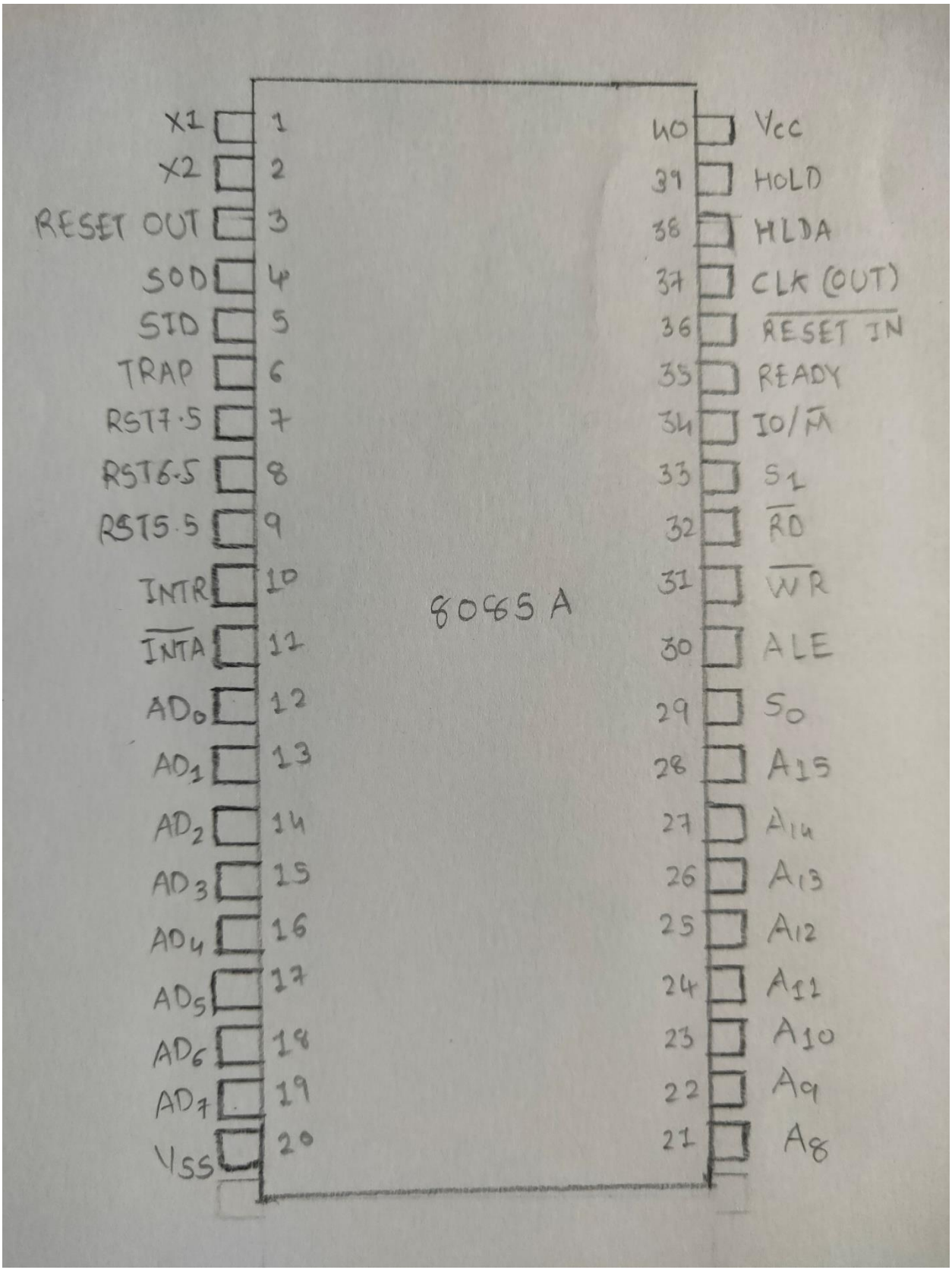
→ Address bus:
A15-A8 are unidirectional and used to carry high-order address of 16 bit address. It carries the most significant 8-bits of memory/IO address (pin 28-21).

→ Data bus: pin (19-12)
AD7-AD0, it can carries the least significant 8-bit (low-order address) address and data bus. The low-order address bus can be separate from these signals by using a latch (ALE)

→ Control and status signals:
These signals are used to identify the nature of operation. There are 3 control signal and 3 status signals

1. $\overline{RD}$ ↔ This signal indicates that the selected IO or memory device is to be read and is ready for accepting data available on the data bus (pin-32)

2. $\overline{WR}$ ↔ This signal indicates that the data on the data bus is to be written into a selected memory or IO location (pin-31).


X1 1
X2 2
RESET OUT 3
SOD 4
SID 5
TRAP 6
RST7.5 7
RST6.5 8
RST5.5 9
INTR 10
INTA 11
AD0 12
AD1 13
AD2 14
AD3 15
AD4 16
AD5 17
AD6 18
AD7 19
VSS 20
8085A
40 VCC
39 HOLD
38 HLDA
37 CLK (OUT)
36 RESET IN
35 READY
34 IO/M
33 S1
32 RD
31 WR
30 ALE
29 S0
28 A15
27 A14
26 A13
25 A12
24 A11
23 A10
22 A9
21 A8

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3. ALE ↔ (Address latch Enable) It is a positive going pulse generated when a new operation is started by the microprocessor. When the pulse goes high, It Indicates address (ALE ← 1, then Address bus). when the pulse goes down, it indicates data (ALE ← 0, then Data bus) (pin-30).

→ Three status signals are IO/M, S0 & S1

1. IO/$\overline{M}$ ↔ This signal is used to differentiate between IO and memory operation
   IO/$\overline{M}$ = high Then IO
   IO/$\overline{M}$ = low Then memory

2. S1 & S0 ↔ Identify the type of current operation (pin 30 & 29)

S_1	S_0	
0	0	HLT
0	1	WRITE
1	0	Read
1	1	OPCODE FETCH

→ clock signals:
X1, X2 – A Crystal (RC, LC network) is connected at these two pins and is used to set frequency of internal clock
CLK (OUT) – used as the system clock for devices connected to 8085 microprocessor

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→ Interrupts & externally initiated signals.

INTERRUPT are the signals generated by external devices to request the microprocessor to perform a task.

INTA (output) - It is an interrupt acknowledgment signal
INTR (Input) - Interrupt Request It is used for general purpose interrupt.
RESET IN - This reset the microprocessor by setting the program counter to zero.
RESET OUT - this signal is used to reset the ~~micro~~ all connected devices when micro processor is reset.
RST 7.5, RST 6.5, RST 5.5 (Input) - Restart interrupts These are vector interrupts that transfer the program control to specific memory locations all have higher priorities than INTR interrupt.
TRAP (Input): This is a non-mask able interrupt & has the highest priority.
READY : Indicates the device is ready to send & recieve.
HOLD: Indicates that another master is requesting the use of the address and data buses.
HLDA: (HOLD Acknowledge): It indicates that the CPU has received the HOLD request and it will relinquish the bus in the next cycle

→ SOD (Serial output data line)- The output SOD is set/reset as specified by the SIM instruction.
→ SID (Serial input data line)- the data on this line is loaded into accumulator whenever RIM instruction is executed.

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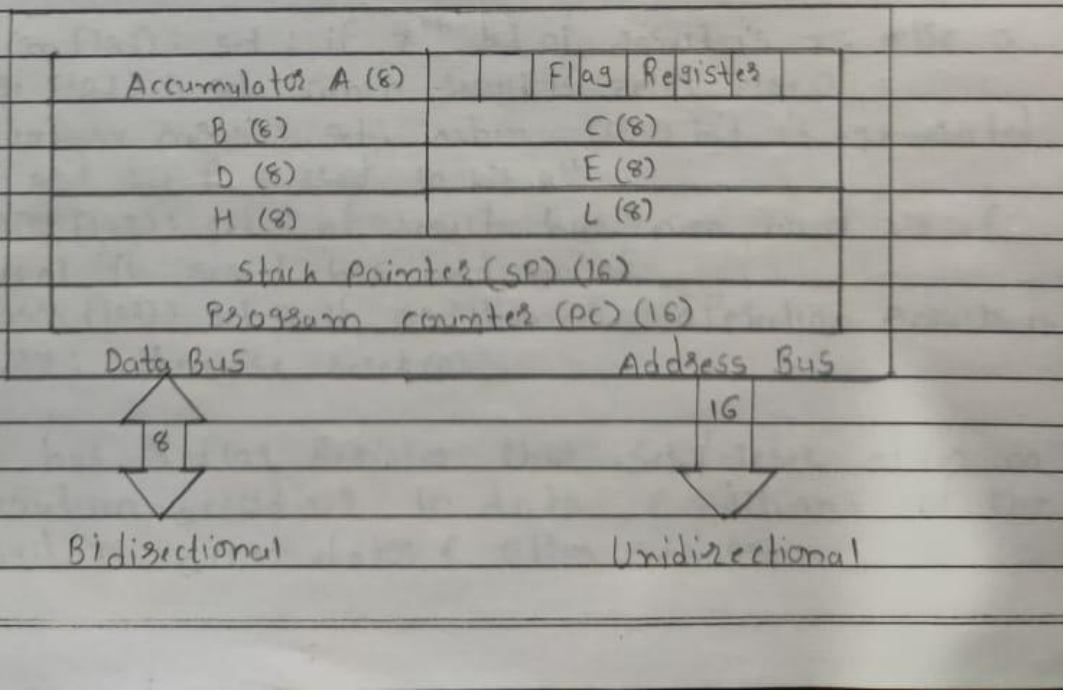
→ Power supply & frequency signal
V_{cc} → Pin 40, +5V supply
V_{ss} → Pin 20, Ground

→ Control & status:

IO/$\overline{M}$	$\overline{RD}$	$\overline{WR}$	operation
0	0	0	HLT
0	0	1	MEMR
0	1	0	MEMW
0	1	1	Opcode fetch
1	0	0	HLT
1	0	1	IOR
1	1	0	IOW
1	1	1	NOP

4) Explain 8085 Programming model and Flag Register.



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→ 6 general purpose registers to store 8-bit data B, C, D, E, H & L.
→ Can be combined as fixed register pairs - BC, DE, HL to perform 16 bit operations.
→ Used to store or copy data using data copy instructions.

⇒ Accumulator
→ 8-bit register, Identified as A
→ Part of ALU
→ Used to store 8-bit data to perform arithmetic & logical operations.
→ Result of operation is stored in Accumulator.

⇒ Flag Register.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	Z	X	AC	X	P	X	CY

S (Sign Flag): Set; if 7th bit of result is 1; else 0
Z (Zero Flag): Set; when result is zero; else 0
AC (Auxiliary carry): Set; when carry bit is generated by 3rd bit & passed to bit 4th
P (Parity Flag): Set; if result has even no of 1's & Reset if result has odd no of
CY (Carry Flag): Set; if arithmetic operation results in carry; otherwise reset (0).

→ ALU has 5 Flag Registers that set/reset after an operation according to data conditions of the result in accumulator & other registers.

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→ Helpful in decision making process of microprocessor.
→ conditions are tested through software instructions.

→ Stack Pointer (SP):
- used as memory pointer.
- Points to the memory location in R/W memory, called stack
- Beginning of stack is defined by loading a 16-bit address in the stack pointer.

→ Program Counter (PC):
- microprocessor uses PC register to sequence the execution of instructions.
- Its function is to point to memory address from which next byte is to be fetched.
- when a byte is being fetched, PC is incremented by 1 to point next memory location.

5) Describe the different types of instruction sets used in 8085.

→ An instruction of a computer is a command given to the computer to perform a specified operation on given data. in microprocessor, the instruction set is the collection of the instructions that the microprocessor is designed to execute.

→ Data Transfer group:
Instructions which are used to transfer the data form a register to another register, from memory to register or register to memory come under this group. MOV, MVI, LXI, LDA, STA etc.

→ Arithmetic group:
The instructions of this group perform arithmetic operations such as addition, subtraction, Increment or decrement of the content of a register or a memory. ADD, ADC, ADI, DAD, SUB etc.

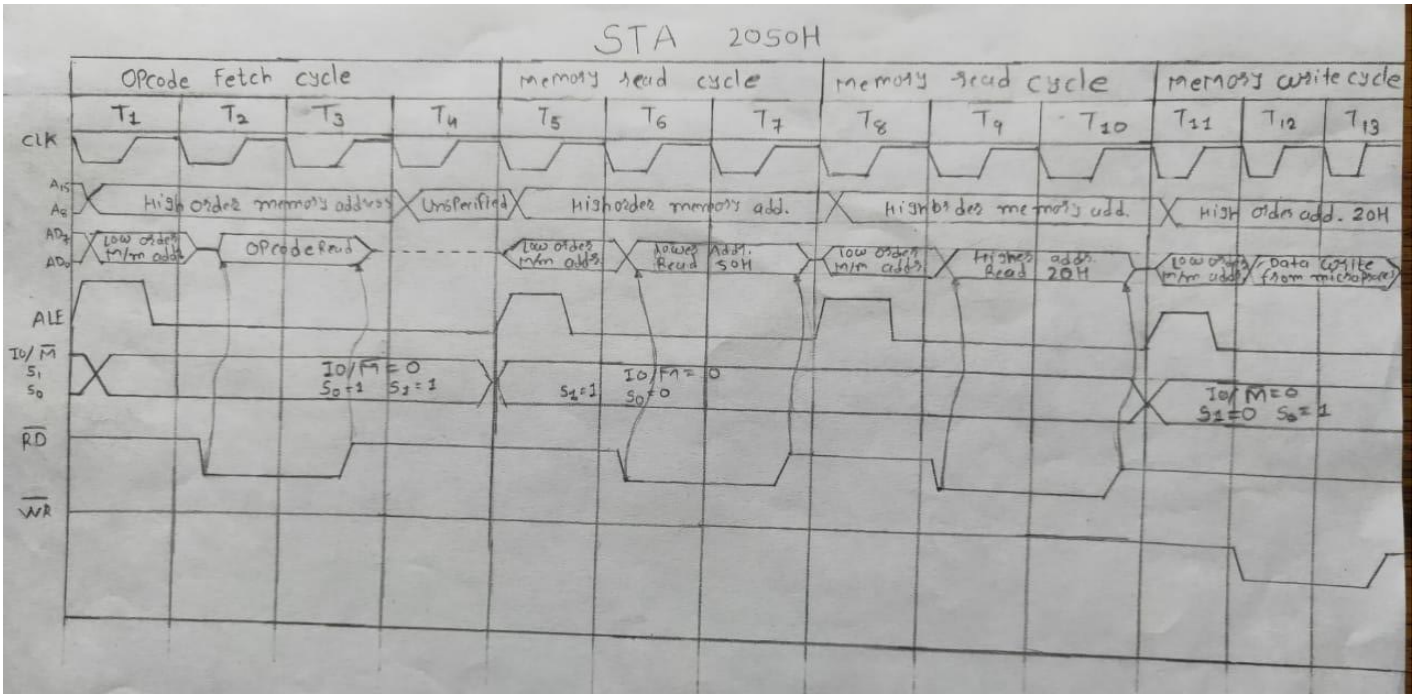
→ Logical group:
The instructions in this group perform logical operation such as AND, OR, compare, rotate. etc

→ Branch control group:
This instructions contains the instructions for conditional and unconditional jump, subroutine call and return and restart. JMP, JC, JNZ, CZ, CP etc

→ control group:
This group contains the instructions for input / output ports, stack and machine control SIM, RIM, NOP etc.

6) Explain the execution of instruction STA 2050H with neat timing diagram.

→ In 8085 instruction set, STA is a mnemonic that stands for store Accumulator contents in memory. In this instruction, Accumulator content will be stored to a memory location whose 16-bit address is indicated in the instruction as 2050H. This instruction uses absolute addressing for specifying the destination. This instruction occupies 3-bytes of memory. First Byte is required for the opcode, and next successive 2-Bytes provide the 16-bit address divided into 8-bits each consecutively



STA 2050H Timing Diagram

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→ In STA 2050H The first byte will contain the opcode hex value 32H. next Byte in memory will hold 50H and after that 20H will be kept in the last third Byte.

→ So this instruction STA 2050H requires 3-Bytes, 4-machine cycles (opcode Fetch, memory Read, memory Read, memory write) and 13 T-states for execution as shown in the timing diagram.

(7) Explain execution of instruction LDA 3000H with timing diagram.

→ LDA is a mnemonic that stands for Load Accumulator with the contents from memory. In this instruction Accumulator will get initialized with 8 bit content from the 16-bit memory

→ In LDA 3000H It occupies 3-Bytes in the memory. First byte specifies the opcode, and next 2-bytes provide the 16-bit address.

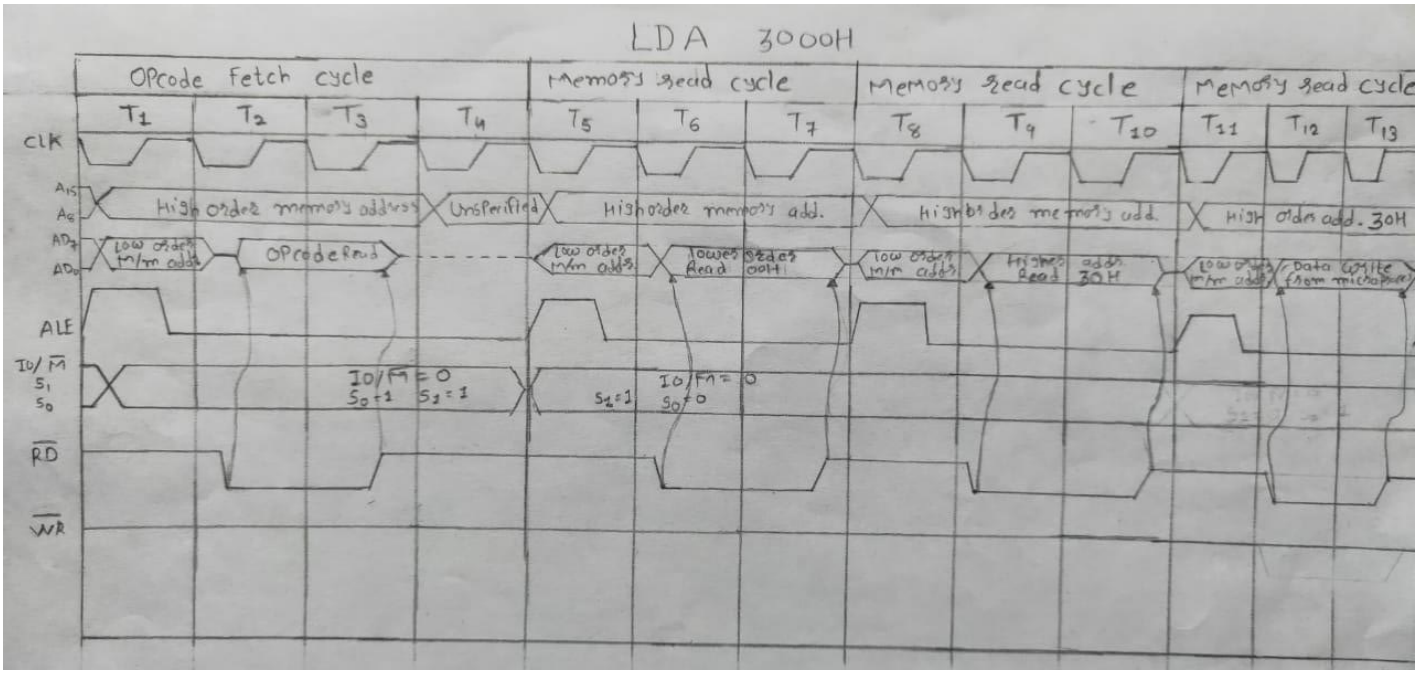
→ so this instruction LDA 3000H requires 3-Bytes, 4-machine cycles (opcode Fetch, memory Read, memory Read, memory Read) and 13 T-states for execution as shown in the timing diagram

(8) Describe basic machine cycle used in 8085. Draw Timing diagram for OUT instruction.

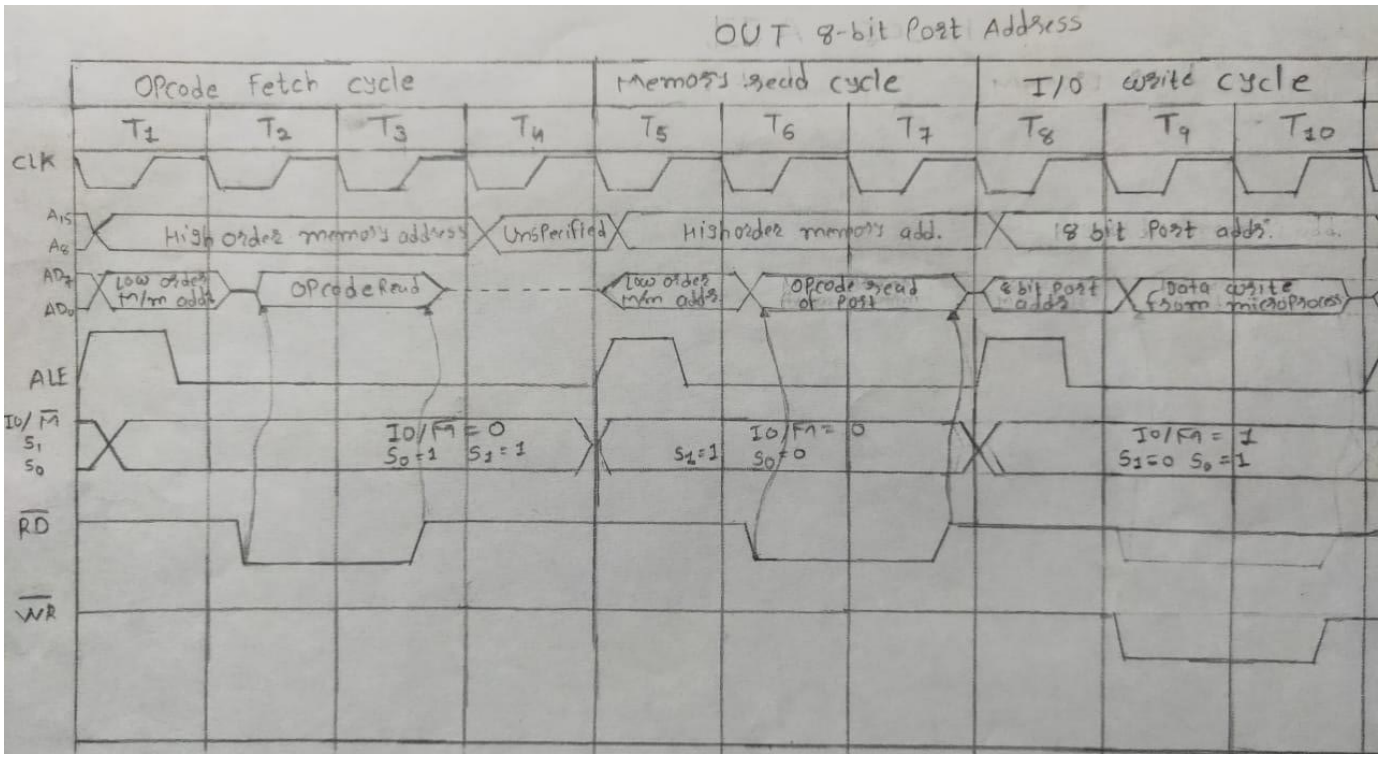
→ Machine cycle is defined as time required by the microprocessor to complete an operation.

→ This cycle may consist 3 to 6 T-states.

→ The basic microprocessor operation such as reading a byte from I/O port for writing byte to memory



LDA 3000H Timing Diagram



OUT Timing Diagram

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⇒ opcode fetch machine cycle:
The opcode fetch machine cycle (OFMC) involves the fetching of the opcode of the instruction to be executed and the decoding process of that opcode. Usually, it consists of four T states.

⇒ Memory read machine cycle:
contents from a memory location are read during the memory read machine cycle (MRMC). This cycle is also known as the operand fetch machine cycle But there are cases when MRMC is not used for operand fetch but for reading data of given memory location This machine cycle spans over three T states.

⇒ Memory write machine cycle:
contents are written to a memory location/ stack during a memory write machine cycle (MWMC). This machine cycle spans over Three T states.

⇒ IO read machine cycle:
contents from an IO device are read during IO read machine cycle (IORMC). This machine cycle spans three T states and is similar to MRMC except for the IO/M̄ signal.

⇒ IO write machine cycle:
contents are written to an IO device during IO write machine cycle (IOWMC). This machine cycle spans three T states and is similar to MWMC except for the IO/M̄ signal.

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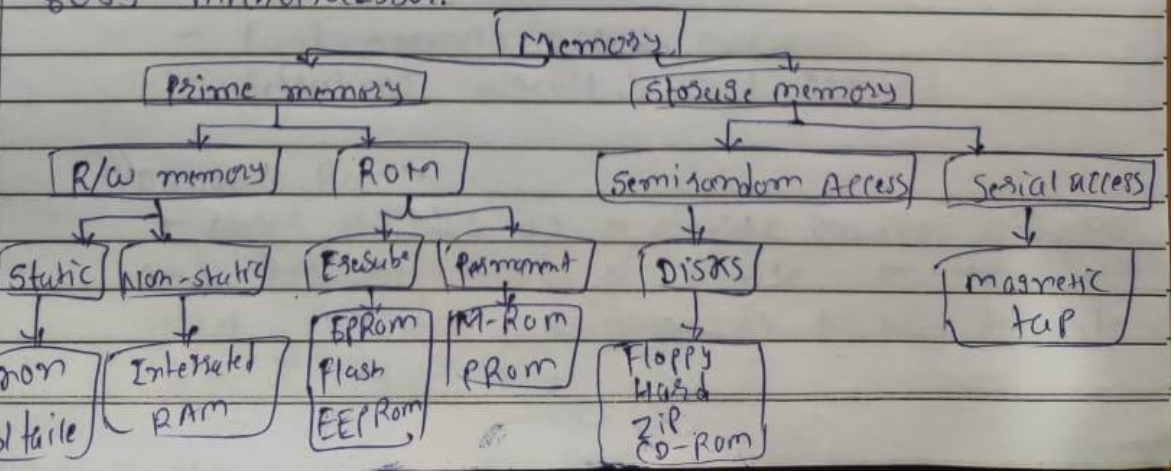
⇒ Interrupt acknowledge machine cycle:

An external IO device issues an interrupt signal (INTR), to tell the microprocessor that it wants a certain task done. When microprocessor receives such a signal, it responds by making the $\overline{INTA}$ signal (interrupt acknowledgement signal) low for some time to tell the device that it has received the request and will take the necessary actions. This whole process is carried out in interrupt acknowledge machine cycle. are usually execute one of two instruction RST(FF) or (CALL. FFFF)

⇒ Bus idle machine cycle:

There are some situations when no data transfer takes place But it does not mean that the microprocessor is idle during that time as there might be some operations going on in the CPU. It is the data/ address bus that is idle such a machine cycle is named a Bus idle machine cycle (BIMC).

(9) write a short note on memory classification of 8085 microprocessor.



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→ There are two basic kinds of memory used in microprocessor systems. memories are classified as two types volatile memories and non-volatile memories.

→ Volatile memories is random access memory (RAM) and non-volatile memories is read only memory (ROM).

→ Volatile memory retain their stat as long as power is applied or data loses when the power is turned off.

→ other hand non-volatile memory can hold data even if power is turned off.

⇒ Random access memory (RAM):

The memory in which the time taken to transfer information to or from any desired random location is always the same is called random access memory.

→ types of Rams
- static RAM
- Dynamic RAM

i) static Ram:-
- consists of circuits capable of retaining their state as long as power is applied. are know as static Ram
- Fast memory access, costly
- Refreshing circuit is not required

ii) Dynamic Ram:-
- stores the data as a charge on the capacitor and they refreshing of charge on the capacitor after every few milliseconds to hold the data even if power is ON.

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⇒ Read only memory (Rom):

It is memory that performs the read only operation. we can't write data in read only memories. It is non-volatile memory. Generally Rom is used to store the binary codes for the sequence of instructions you want the computer to carry out and data such as look up tables. this is because this type of information does not change.

i) masked Rom:
- the program or data are permanently installed at the time of manufacturing as per requirement.
- The data cannot be altered.

ii) PRom (Programmable Read only memory)
- The memory has nichrome or Polysilicon wires arranged in a matrix these wires can be functionally viewed as diode or fuses.
- This memory can be programmed by users with a special PRom Programmer that selectively burns the fuses according to the bit pattern to be stored. is called burning the PRom.

(iii) EPRom (Erasable Programmable Read only memory)
→ The memory stores a bit by charging the floating gate of FET.
→ All the information can be erased by exposing the chip to ultraviolet light through its quartz window and the chip can be reprogrammed because the chip can be reused many times.

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(iv) EEPROM (Electrically Erasable Programmable read only memory).

- This memory is functionally similar to EPROM except them that information can be altered by using electrical signals at the register level rather than erasing all the information.

(10) How address and data lines AD0-AD7 of 8085 are demultiplexed? Discuss the diagram of generation of control signals in 8085.

→ As we know that $A_{15}-A_8$ is highest order 8 bits of memory address and I/O address. AD_7-AD_0 is lower order 8 bits of memory address or I/O address. They also serves as data bus.

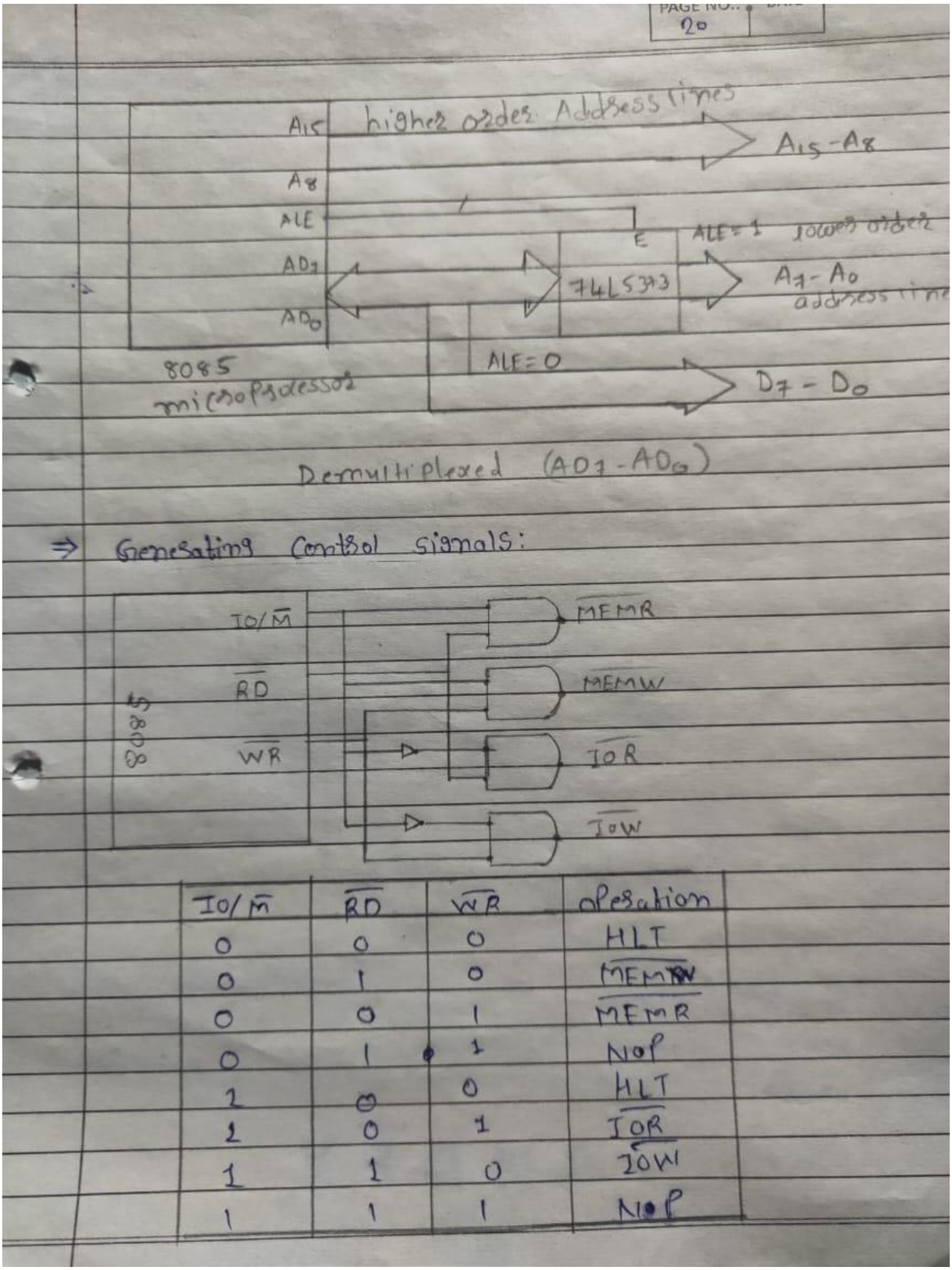
→ External memory or I/O device need the complete 16-bit address for decoding and interfacing. That's why we need demultiplexing and this is done by ALE signal.

ALE: 1

in 1'st clock cycle T_1 It is used used as lower order address bus (unidirectional)

ALE: 0

In T_2 and T_3 it is used as data bus (bidirectional



IO/M̄	RD̄	WR̄	operation
0	0	0	HLT
0	1	0	MEMW̄
0	0	1	MEMR̄
0	1	1	NOP
1	0	0	HLT
1	0	1	IOR̄
1	1	0	IOW̄
1	1	1	NOP