Siddharth Rajguru

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Summary

A motivated electrical engineer generalist with experience in hardware optimization, testing, image processing and virtualization

Education

M.S., Electrical Engineering, Texas Tech University, TX. (GPA: 3.5) Dec. 2015

B.S., Electrical Engineering (Math. Minor), Texas Tech University, TX. Dec. 2013

Experience

(References on request)

Blackberry Corp., Redwood City, CA.: Software Developer Student (Enterprise Cloud IoT applications) May 2015 – Aug. 2015

- Implemented and managed VM configuration scripts using configuration management tools
- Created automation scripts and test scripts for continuous integration servers
- Created Node Package Management (npm) solutions for private publishing and package hosting
- VM performance assessment and verification based on hardware and hypervisor specifications
- Created functional test cases and tested applications based on provisioned virtual hardware

Carl Zeiss Meditec, CA.: System/Software Intern (Cirrus HD-OCT product line research and development) Jun. 2014 – Oct. 2014

- Debugged applications and performed integration and performance testing
- Analyzed memory fragmentation behavior and a temporary workaround for a 32-bit application
- Performance tested Intel based medical instruments for application compatibility and assessing bottlenecks
- Optimized processor clock speeds and memory requirements for better cost to performance ratio
- Performance assessment for legacy instruments based on Intel's Nahelam and Sandy Bridge microarchitectures
- Performed trade off study for performance between SATA based storage solutions and PCIe based storage
- Took the lead to provide a workflow for hardware based on core and chipset architectural roadmaps
- Received training in TFS (code control), Scrum, medical device lifecycle, software workflow and testing/monitoring tools

Tools and Language familiarity

Verilog	C/C++	ShellScript	Linux	JavaScript	FPGA	Testing	µControllers	CUDA
Intel XTU	Vtune	Architectures	TCP/IP	MATLAB	Cadence	KVM/ESXi	Overclocking	RISC
Network	DSP	Virtualization	Eclipse	OpenCV	Labview	NGiNX	MSP430	Jenkins
Spartan3E	ARM M4	MSP430	x86	ARM AM335x	Zync SOC	OpenNebula	Ansible	Docker

Notable Projects 2011-2015

Academic/Self started Projects

- Virtualization server: Created a virtualization server using Esxi and vSphere for orchestration
  - Virtualization using Intel VT-d and VT-x compatible hardware for bare metal hypervisors
  - Performed optimizations to power target, core voltage, clock multipliers and turbo power targets
  - Used Intel XTU and Intel Vtune Amplifier for real time analysis and thermal performance and stability
  - Analyzed performance differences between Haswell and Haswell refresh in both single and hyper threaded cores
- Functionality tester: Designed a logic IC functionality tester for basic logic ICs
  - Linux based single board computer (ARM Sitara) for upper level command line control and GPIO
  - Used Angstrom Linux to design a simple C++ application to select between functional tests and type of gate
  - Spartan3E based FPGA fabric for low level interface with DUTs with switchable logic profiles
  - Used Verilog to create gate specific test cases to provide pass/fail flag to the ARM board
- 32-Bit RISC behavioral model (Xilinx ISE and Verilog)
  - Created non synthesizable 32-bit RISC architecture using Xilinx ISE
  - Architecture based on a 32x32 memory bank, a 32-bit ALU and a barrel shifter
  - Tested core modules for functionality and operation code execution
- Parametric and functional testing: Tested logic ICs and ADC using bench and automated testing tools
  - Tested for VOH/VOL, Iddq, Continuity, power consumption and functionality
  - Used Labview based National Instruments PXi platform automated tester
  - Used Keithley programmable multi-meter for bench testing
  - Tested for repeatability, reproducibility and error calculation between bench and automated equipment
  - Created statistical distribution of results based on ideal specifications for binning

- Autonomous vehicle: Metal path following FPGA based autonomous vehicle
    - Spartan3E based motor control and sensor feedback logic in Verilog
    - Implemented metal detecting sensor for path guidance and an ultrasonic sensor to start/stop triggers
- GPU Benchmarking: Benchmarked Directx 11.2 compatible GPUs from Nvidia and AMD
    - Assessment based on TDP, power consumption, core frequency and usable memory bandwidth
    - Performed optimizations to power target, core voltage, memory frequency and memory voltage
    - Used proprietary AMD and Nvidia monitoring tools for thermal performance and stability
    - Analyzed performance bottlenecks based on Nvidia Maxwell GM204 and AMD Grenada Pro architectures
- CUDA implementation: Trade off study between parallel execution and serial execution using CUDA API
    - Created simple test programs with different computational intensities in C and CUDA C
    - Included Matlab's accelerated libraries for additional testing for computational times
- Automated testing: Test plan creation and execution on a digital ATE
    - DUTs tested: ADC and Logic ICs
    - Performed large sample testing on DUTs for repeatability and reproducibility
    - Results used for statistical binning of the DUTs based on performance
- Low Noise Amplifier: Designed, built and tested 2.4Ghz Wifi amplifier
    - Theoretical design and testing using Smith charts, N.I. AWR Suite and LTSpice using industry standard spec. limits
    - PCB layout etching and milling using EagleCad
    - Final device testing using microwave spectrum analyzer and digital oscilloscopes
- Personal Web Application: Created and deployed a web application for hosting my portfolio
    - Created front-end using HTML, CSS and Bootstrap components
    - v1.0.0 deployment using NGiNX reverse proxy and ExpressJS server with basic security
    - Security: DoS mitigation, connection limits, request rate/burst limit, blacklisting
- Medical Imaging: Implement MRI, CT and Doppler Ultrasound reconstruction techniques
    - MRI: Image significance mapping for multi-coil image reconstruction
    - CT: Usage of radon and inverse radon transform algorithms for projection based reconstruction

University Activities and Awards

Texas Tech University, TX.: Tutor, Electrical Engineering Jan. 2014 – May 2015

- Created instructional videos and assist students on FPGAs and digital logic theory
- Provided one on one guidance for behavioral modeling of logic circuits

Texas Tech University, TX.: IT support, IT Solutions Center Aug. 2013 – Nov. 2013

- Provided support on Microsoft products and network related issues

Dept. of Electrical and Computer Engineering, Texas Tech University

- Ray Butler Scholarship awarded by Texas Tech University 2015
- Russell Seacat Jr. Scholarship awarded by Texas Tech University 2014
- Volunteer judge at Gear 2012 (a robotics competition for kids)