Siddharth Rajguru

Dallas, TX.; Cell: 806-317-3712; Email: siddharth.rajguru2013@gmail.com
Website: http://siddraj.com; Git repository: http://github.com/sidraj2002

Summary

A motivated generalist with experience in cloud infrastructure deployment, embedded hardware and medical devices

Education

M.S., Electrical Engineering, Texas Tech University, TX. (GPA: 3.5)   Dec. 2015

B.S., Electrical Engineering (Math. Minor), Texas Tech University, TX. (GPA: 2.9)   Dec. 2013

Experience   (References on request)

Amazon Web Services, Dallas, TX.: Cloud Support Associate Engineer (AWS infrastructural support)   Apr. 2016 – Present

- Provide customer facing architectural and deployment support for web applications within AWS infrastructure
- Specializing in DevOps technologies for configuration management and continuous integration
- Large application stack deployments using JSON templates on the CloudFormation platform
- Prototyping Node.JS applications, deployment stacks and configuration scripts
- SSL end to end encryption, IPSEC tunneling and packet analysis between AWS virtual networks
- Linux operating system level troubleshooting for block devices, networking and process management
- Bug analysis for: S3FS interaction with AWS API and Elastic Beanstalk queueing daemon
- Troubleshooting Databases (MySql) and cache clusters (Redis and Memched)
- Provide training on Ansible and AWS F1 (FPGA) instances (ongoing)
- Training projects: SNMP monitoring using Cactii, Three-tier Wordpress application and Cross-VPC tunneling

Blackberry Corp., Redwood City, CA.: Software Developer Student (Enterprise Cloud IoT applications)   May 2015 - Aug. 2015

- Implemented and managed VM configuration scripts using Ansible configuration management tool
- Created Node Package Management (npm) solution for private publishing and package hosting
- Created automation scripts for database replication and health checks
- Implemented scripts in Jenkins for continuous integration and automated publishing
- Created functional test cases and tested NodeJS applications and databases
- Used OpenNebula orchestration interface for VM performance analysis and creation
- Stress tested web applications using Jmeter for availability and robustness
- Received experience building cloud infrastructure and designing for scalability in an Agile Scrum environment

Carl Zeiss Meditec, CA.: System/Software Intern (Cirrus HD-OCT product line research and development)   Jun. 2014 - Oct. 2014

- Debugged C# applications, performed integration and performance testing
- Stress tested medical device hardware using over-clocking and benchmarking tools
- Tested application for memory performance and bottlenecks due to fragmentation
- Performed a trade off study for application performance between SATA and PCIe based storage solutions
- Took the lead to provide a workflow for hardware based on core and chipset architectural roadmaps
- Performed tasks using TFS code control based on the Scrum methodology for software lifecycle

Computing Skills

AWS EC2	ElasticBeanstalk	CloudFormation	ElasticContainer	AWS RDS	Amazon Linux	VPC Networking
NodeJS / NPM	AngularJS	KrakenJS	Bootstrap	Jmeter	Grunt	Mocha
MySQL	CouchDB	NGiNX / Apache	Jenkins	Ansible	Chef	Docker
Git / Gerrit	JIRA	Eclipse	Visual Studio	MATLAB	TFS	SCRUM
JavaScript	C/C++	Shell Script	JSON / YAML	HTML5	Verilog	Ubuntu

Notable Projects 2011-2015

Academic/Self Started Projects

- Personal Web Application: Created and deployed a web application for hosting my portfolio
  - Created front-end using HTML, CSS and Bootstrap components
  - Created JavaScript handlers for dynamic page functionality
  - Used ExpressJS server for application deployment
  - Used NGiNX reverse proxy for additional security and scalability
  - Staged and tested the application on AWS EC2 running Ubuntu
  - Stress tested webserver with Jmeter for bottlenecks

- Web application optimization and security: Optimization for scalability and performance
  - Created configuration management script for parallel deployment
  - Used NGiNX for multi-instance management and caching
  - Improved performance and availability through multiple instances
  - Implemented timeouts and request rates to prevent DoS attacks
  - Used blacklisting scripts to filter high querying I.P. addresses
  - In-progress:Enhancements: Docker container deployment, NGiNX caching and load balancing
  - In-progress:Security: WAF, NGiNX access log parsing, basic authentication.
- Virtualization server and networking: Created a virtualization server using Esxi and vSphere for orchestration
  - Virtualization using Intel VT-d and VT-x compatible hardware for bare metal hypervisors
  - Provisioned virtual storage and computational parameters based on available hardware
  - Deployed server in a DMZ configuration for web application testing
  - Traffic monitoring and DHCP setup for a dual network EdgeOS Ubiquiti router
- Medical Imaging: Implemented MRI and Computed Tomography reconstruction techniques in Matlab
  - MRI: Image significance mapping for multi-coil image reconstruction
  - MRI: Created a Matlab algorithm for FOV based image cropping and significance map generation
  - CT: Usage of radon and inverse radon transform algorithms for projection based reconstruction
  - CT: Fourier domain filters for noise reduction and blur reduction
- Image processing service: Created a web service using WCF with a forms app for frontend usage
  - Implemented OpenCV image processing algorithms on the backend service along with a SQL lite database
  - Deployed forms application using IIS Express server
  - Ported OpenCV libraries using EMGU C# wrapper
  - Implemented FFT, Edge detection and noise reduction libraries
- Functionality tester: A cross platform embedded tester using an embedded Linux processor and a FPGA
  - Linux based single board computer (ARM Sitara) for upper level command line control and GPIO
  - Used Angstrom Linux to design a simple C++ application to select between functional tests and type of gate
  - Spartan3E based FPGA fabric for low level interface with DUTs with switchable logic profiles
  - Used Verilog to create gate specific test cases to provide pass/fail flag to the ARM board
- 32-Bit RISC behavioral model (Xilinx ISE and Verilog)
  - Developed chip-level designs for functional and storage modules on a standard RISC architecture
  - Created a non-synthesizable 32-bit RISC model with a 32-bit control word

Academic activities and Awards

Texas Tech University, TX.: Tutor, Electrical Engineering   Jan. 2014 – May 2015

- Created instructional videos and assist students on FPGAs and digital logic theory

Texas Tech University, TX.: IT support, IT Solutions Center   Aug. 2013 – Nov. 2013

- Provided support on Microsoft products and network related issues

Texas Tech University, TX.: Scholarships

- Ray Butler Scholarship awarded by Texas Tech University 2015
- Russell Seacat Jr. Scholarship awarded by Texas Tech University 2014