5LIH0: Digital Integrated Circuit Design Assignment 1

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I. INTRODUCTION

In order to design a custom IC, the first step is to specify the design parameters according to the application requirements. For designing an inverter for minimum load, the length and width of pmos and nmos transistors are the major design parameters. The next step involves creating a schematic of inverter in the cadence tool. Figure 1 shows this implementation. After this, the inverter is connected to the load and power supply as shown in figure 2. The circuit is simulated, and output waveforms are checked. Once the above steps are successful, the layout of inverter can be developed in the tool according to the design specification and design rules of 45nm process[1] and layout verification is performed. The last steps involve PEX analysis and post-layout simulation.

II. LAB DESCRIPTION

A. *Schematic Entry*.

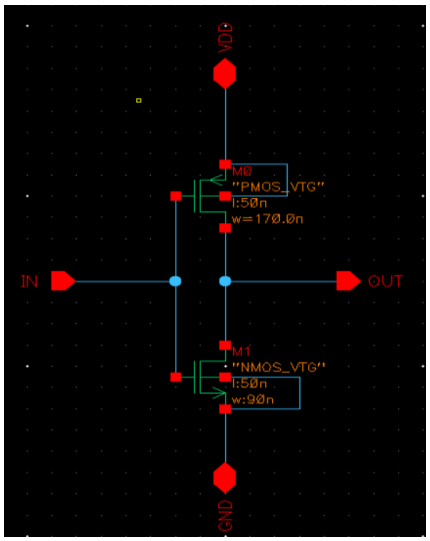

Fig. 1. The circuit schematic of an inverter.

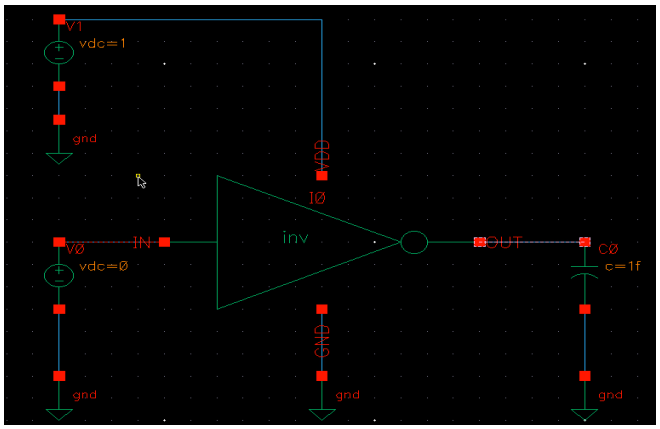

Fig. 2. Schematic simulation of an inverter.

In this step, the pmos and nmos transistors are selected from the NSCU_Devices_FreePDK45 library and the inverter is designed as shown in figure 1 with VDD, GND, IN and OUT connections. This design is abstracted into a inverter layer shown as inv in figure 2. Now, this inverter can be used to design further circuits.

In the schematic simulation, the inverter is simulated by connecting to input source, VDD, GND and a load as shown in figure 2. Below is the output waveform of the simulation.

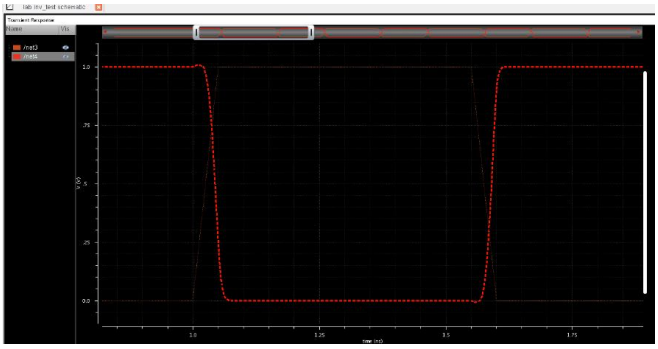

Fig. 3. Schematic simulation output waveform of an inverter.

At this step, by keeping W/L ratio of nmos transistor and length(L) of pmos transistor fixed, the width(W) of pmos transistor is varied until equal rise and fall time output waveforms are obtained. In the assignment, the inverter is designed for 0 F capacitance load and at W=170nm of nmos transistor, equal rise and fall times in the output waveform were observed.

B. *Layout Edit*

In this step, the layout of the inverter is designed according to transistors parameters designed in schematic simulation step and according to the design rules mentioned in [1]. The active layer defines the

openings in the SiO2 covering the substrate. N-implant or P-implant layers indicates where to implant n-type or p-type atoms. The polysilicon layer is the gate layer that connects n and p regions. The n-well and p-well layers form the substrate layers of the inverter. The contacts are used to serve as electrical connection points of individual layers. The metal layer M1 connects the contacts. The VTG layer is used to indicate the general threshold voltage.

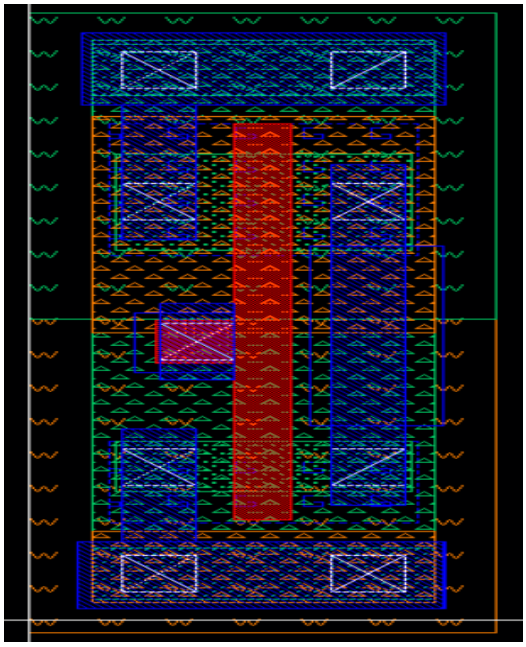

Fig. 4. The layout of an inverter.

Once the layout is edited and saved, design rule check is performed to check whether the layout is designed in accordance to the design rules. Upon successful check, output shown in figure 5 is obtained.

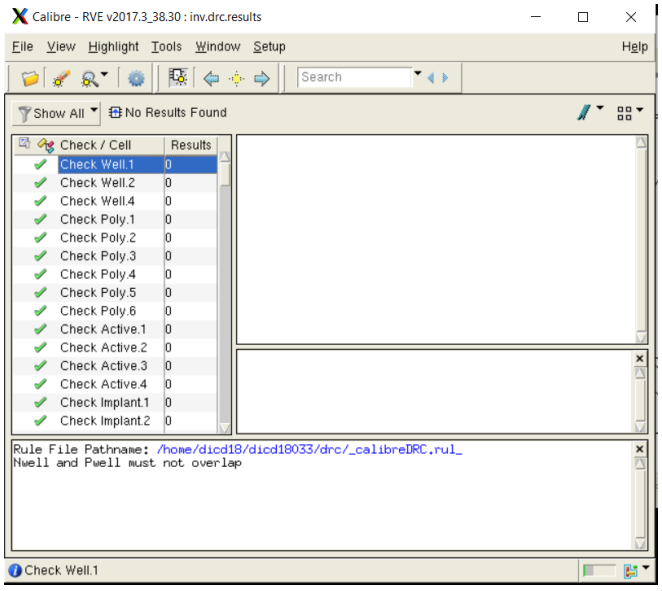

Fig. 5. DRC check output

The next step is to perform layout versus schematic design check to make sure the pin mapping, number of devices and parameters are mapped correctly. Upon successful check, output shown in figure 6 is obtained.

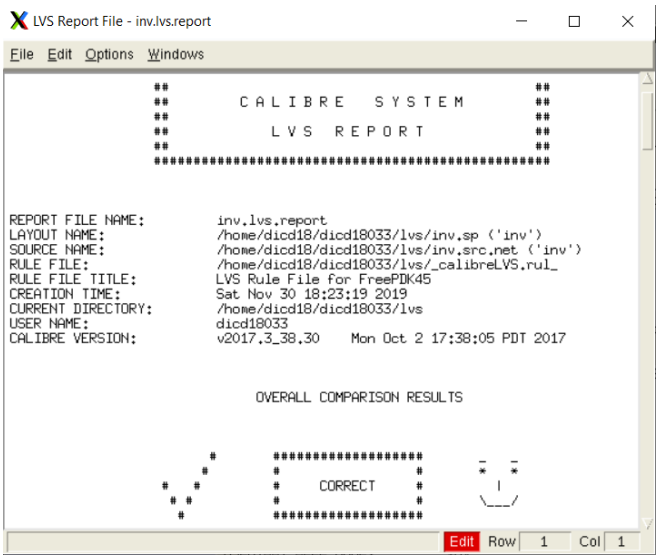

Fig. 6. Output LVS check

III. RESULTS

After performing all the steps mentioned in section II, the inverter was designed and simulated with loads and results were tabulated.

SL.no	Load	Schematic		Layout	
		Transition time	Propagation Delay	Transition time	Propagation Delay
1	0 F	6.6303 ps	Tr= 33.448 ps Tf = 32.3864 ps	10.056ps	Tr= 46.0158ps Tf = 44.963ps
2	50f F	-	-	-	-
3	1 Inverter	9.745 ps	Tr= 35.384 ps Tf = 34.508 ps	14.269 ps	Tr= 48.670 ps Tf = 47.798 ps
4	F04	19.472 ps	Tr= 40.616 ps Tf = 40.343 ps		Tr= 55.412 ps Tf = 56.676 ps
5	500f F	-	-	-	-

Fig. 7. Output results

Since the inverter was designed for minimum load, it cannot drive higher loads (50 fF, 500 fF). At such loads the output waveform observed is shown in figure 8 and 9.

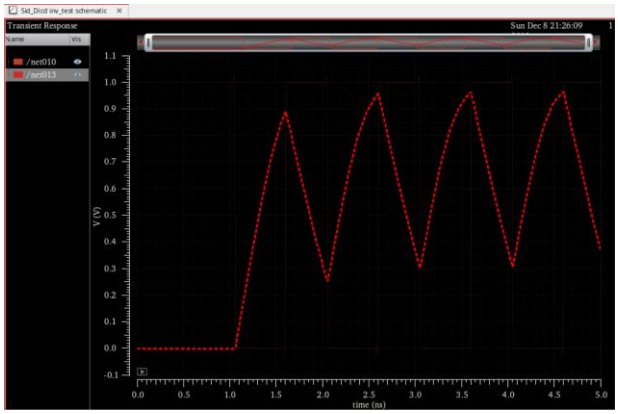

Fig.8. Output waveform for 50f F load capacitance

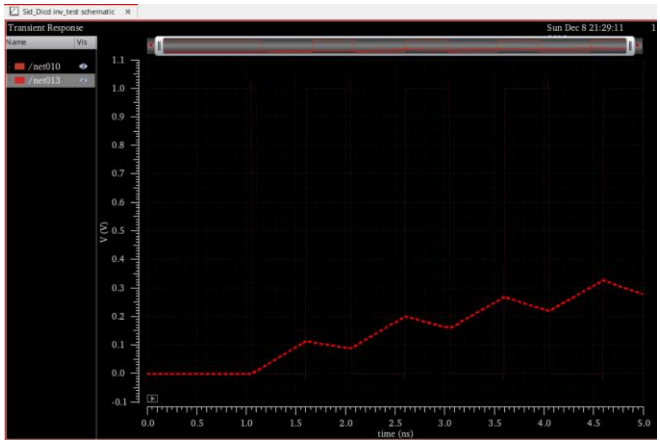

Fig.9. Output waveform for 500f F load capacitance

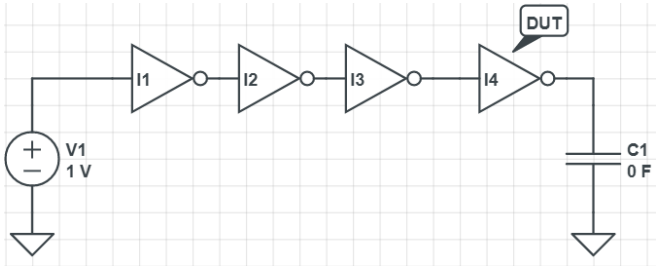

Fig. 10. Connection diagram of inverter with a load

The low and high noise margins is calculated using the equations, $NM_L = V_{IL} - V_{OL}$ and $NM_H = V_{OH} - V_{IH}$ represent the levels of noise that can be sustained when chain of inverters are connected. From figure 11, estimated value of V_{IL} is 0.44V and V_{IH} is 0.57V . This implies, $NM_L = 0.44 - 0 = 0.44V$ and $NM_H = 1 - 0.57 = 0.43V$, respectively.

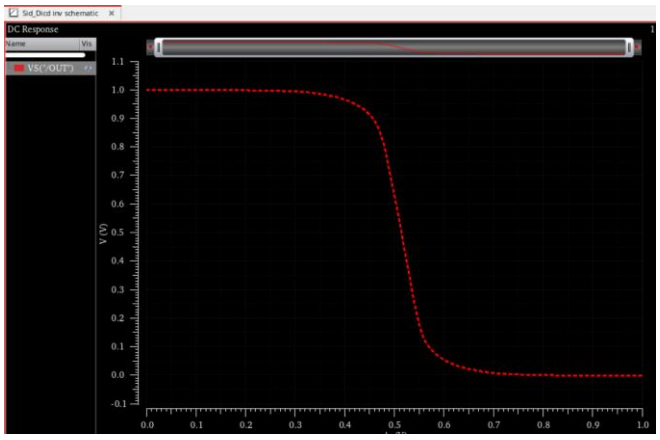

Fig. 11. VTC curve of inverter with V_{dc} =1V and V_{dd} =1V.

PEX analysis output:

DESIGN "INV"

; DATE "Sat Nov 30 18:25:51 2019"

; VENDOR "Mentor Graphics Corp."

; PROGRAM "Calibre xRC v2017.3_38.30"

; CIRCUIT TEMPERATURE 27C

; NOMINAL TEMPERATURE 27C

;

mgc_rve_device_template "PMOS_VTL" "D" "G" "S" "b"

mgc_rve_device_template "NMOS_VTL" "D" "G" "S" "b"

mgc_rve_device_template "PMOS_VTH" "D" "G" "S" "b"

mgc_rve_device_template "NMOS_VTH" "D" "G" "S" "b"

mgc_rve_device_template "PMOS_VTG" "D" "G" "S" "b"

mgc_rve_device_template "NMOS_VTG" "D" "G" "S" "b"

mgc_rve_device_template "PMOS_THKOX" "D" "G" "S" "b"

mgc_rve_device_template "NMOS_THKOX" "D" "G" "S" "b"

mgc_rve_device_template "v" "P" "M"

mgc_rve_device_template "f" "P" "M"

mgc_rve_parasitic_template "c" "r" "l" "k" "h"

mgc_rve_cell_start "inv" "IN" "GND" "VDD" "OUT"

mr_pi "NMOS_VTG" "MM1" '("MM1_d" "MM1_g" "MM1_s" "MM1_b") '(("l" 5e-08) ("w" 9e-08) ("ad" 9.45e-15) ("as" 9.45e-15) ("pd" 3.9e-07) ("ps" 3.9e-07) ("lpe" 3)) '(0.18 0.2275)

mr_pi "PMOS_VTG" "MM0" '("MM0_d" "MM0_g" "MM0_s" "MM0_b") '(("l" 5e-08) ("w" 1.7e-07) ("ad" 1.785e-14) ("as" 1.785e-14) ("pd" 5.5e-07) ("ps" 5.5e-07) ("lpe" 3)) '(0.18 0.6575)

mr_ni "IN" 160.931 6.197e-17 6.07403e-17 '("MM0_g" "MM1_g")

mr_pp 'c "ciIN_14" '("c_13_p" "0") 0.00824647f

mr_pp 'c "ciIN_15" '("IN" "0") 0.00561454f

mr_pp 'c "ciIN_16" '("MM0_g" "0") 0.0265828f

mr_pp 'c "ciIN_17" '("MM1_g" "0") 0.0215262f

mr_pp 'r "rIN_18" '("IN_11" "c_13_p") 5.98

mr_pp 'r "rIN_19" '("IN_11" "IN") 89.3538

mr_pp 'r "rIN_20" '("IN_5" "c_13_p") 1.98872

mr_pp 'r "rIN_21" '("IN_5" "MM0_g") 32.76

mr_pp 'r "rIN_22" '("IN_1" "c_13_p") 1.98872

mr_pp 'r "rIN_23" '("IN_1" "MM1_g") 28.86

```
mr_ni "GND" 1.17063 3.24428e-17 3.83552e-17 '( "MM1_b" "MM1_s" )
mr_pp 'c "ciGND_10" '("c_17_n" "0") 0.0144724f
mr_pp 'c "ciGND_11" '("c_20_p" "0") 0.00797735f
mr_pp 'c "ciGND_12" '("MM1_s" "0") 0.00999306f
mr_pp 'r "rGND_13" '("c_17_n" "GND") 0.158333
mr_pp 'r "rGND_14" '("MM1_b" "c_20_p") 0.143886
mr_pp 'r "rGND_15" '("MM1_b" "c_17_n") 0.093799
mr_pp 'r "rGND_16" '("MM1_s" "c_20_p") 0.774615

mr_ni "VDD" 1.43755 3.53582e-17 3.05084e-17 '( "MM0_b" "MM0_s" )
mr_pp 'c "ciVDD_10" '("c_27_n" "0") 0.0149844f
mr_pp 'c "ciVDD_11" '("c_30_n" "0") 0.00811453f
mr_pp 'c "ciVDD_12" '("MM0_s" "0") 0.0122593f
mr_pp 'r "rVDD_13" '("c_27_n" "VDD") 0.186275
mr_pp 'r "rVDD_14" '("MM0_b" "c_30_n") 0.150135
mr_pp 'r "rVDD_15" '("MM0_b" "c_27_n") 0.0926758
mr_pp 'r "rVDD_16" '("MM0_s" "c_30_n") 1.00846

mr_ni "OUT" 1.99727 3.17332e-17 8.02297e-17 '( "MM0_d" "MM1_d" )
mr_pp 'c "ciOUT_12" '("c_40_n" "0") 0.00434881f
mr_pp 'c "ciOUT_13" '("OUT" "0") 0.00991329f
mr_pp 'c "ciOUT_14" '("c_37_n" "0") 0.00426963f
mr_pp 'c "ciOUT_15" '("MM0_d" "0") 0.00677398f
mr_pp 'c "ciOUT_16" '("MM1_d" "0") 0.00642745f
mr_pp 'r "rOUT_17" '("OUT_4" "c_40_n") 0.23192
mr_pp 'r "rOUT_18" '("OUT_4" "OUT") 0.352511
mr_pp 'r "rOUT_19" '("c_37_n" "OUT_15") 0.23192
mr_pp 'r "rOUT_20" '("c_37_n" "OUT") 0.304
mr_pp 'r "rOUT_21" '("MM0_d" "c_40_n") 0.453077
mr_pp 'r "rOUT_22" '("MM1_d" "OUT_15") 0.423846

mr_pp 'c "cc_1" '("MM1_g" "MM1_s") 0.00321486f
mr_pp 'c "cc_2" '("IN" "MM1_s") 0.0064247f
mr_pp 'c "cc_3" '("MM1_g" "c_17_n") 0.00162199f
mr_pp 'c "cc_4" '("IN" "c_17_n") 8.50013e-19
mr_pp 'c "cc_5" '("MM0_g" "MM0_s") 0.00463848f
mr_pp 'c "cc_6" '("IN" "MM0_s") 0.00459791f
mr_pp 'c "cc_7" '("MM0_g" "c_27_n") 0.00166145f
mr_pp 'c "cc_8" '("IN" "c_27_n") 6.61715e-19
mr_pp 'c "cc_9" '("MM1_g" "MM1_d") 0.0024949f
mr_pp 'c "cc_10" '("MM0_g" "MM0_d") 0.00265309f
mr_pp 'c "cc_11" '("MM1_g" "c_37_n") 0.0031386f
mr_pp 'c "cc_12" '("IN" "OUT") 0.0225054f
mr_pp 'c "cc_13" '("c_13_p" "OUT") 0.0031386f
mr_pp 'c "cc_14" '("MM0_g" "c_40_n") 0.0031386f
mr_pp 'c "cc_15" '("MM1_s" "MM0_s") 3.12887e-19
mr_pp 'c "cc_16" '("c_20_p" "c_30_n") 2.40087e-19
mr_pp 'c "cc_17" '("c_17_n" "c_27_n") 4.63025e-19
mr_pp 'c "cc_18" '("MM1_s" "MM1_d") 0.00899139f
mr_pp 'c "cc_19" '("c_17_n" "MM1_d") 0.0140458f
mr_pp 'c "cc_20" '("c_17_n" "c_37_n") 0.00219039f
mr_pp 'c "cc_21" '("MM0_s" "MM0_d") 0.00899139f
mr_pp 'c "cc_22" '("c_27_n" "MM0_d") 0.00723625f
mr_pp 'c "cc_23" '("c_27_n" "c_40_n") 0.00170525f
mgc_rve_cell_end
```

IV. PITFALLS AND CONCLUSION

The hands-on experience on designing an inverter was a very good learning experience for me. The tutorial videos were very helpful. One of the important tricks I learnt is to never design the layout until the length and width parameters are finalized in the schematic layout.

In conclusion, the goal of transistor sizing is to make the rise and fall time equal because it depends on the effective resistance of nmos and pmos transistor and the load capacitance.

REFERENCES

[1]NSCU_EDA_Wiki, https://www.eda.ncsu.edu/wiki/FreePDK45:Contents