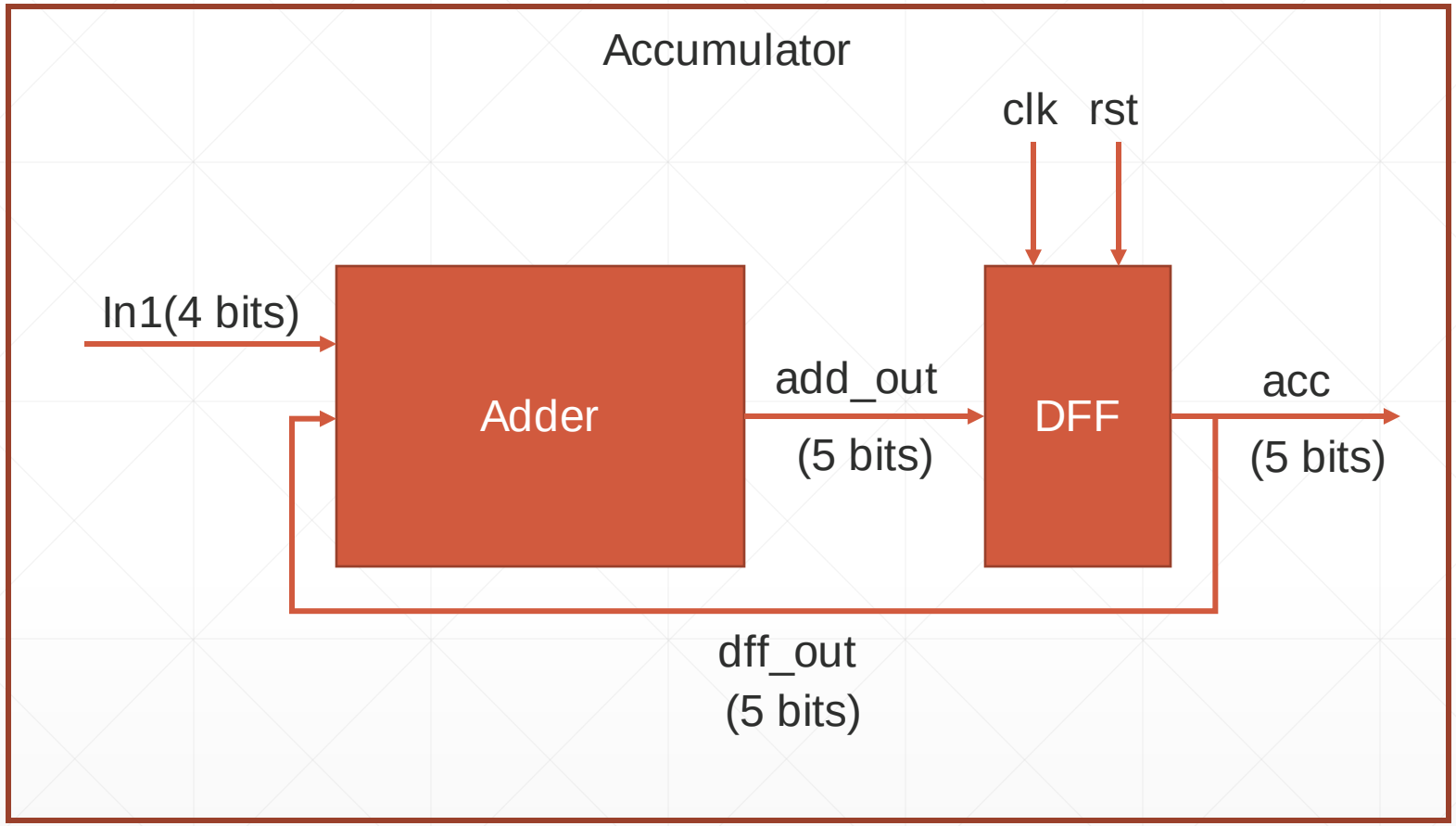
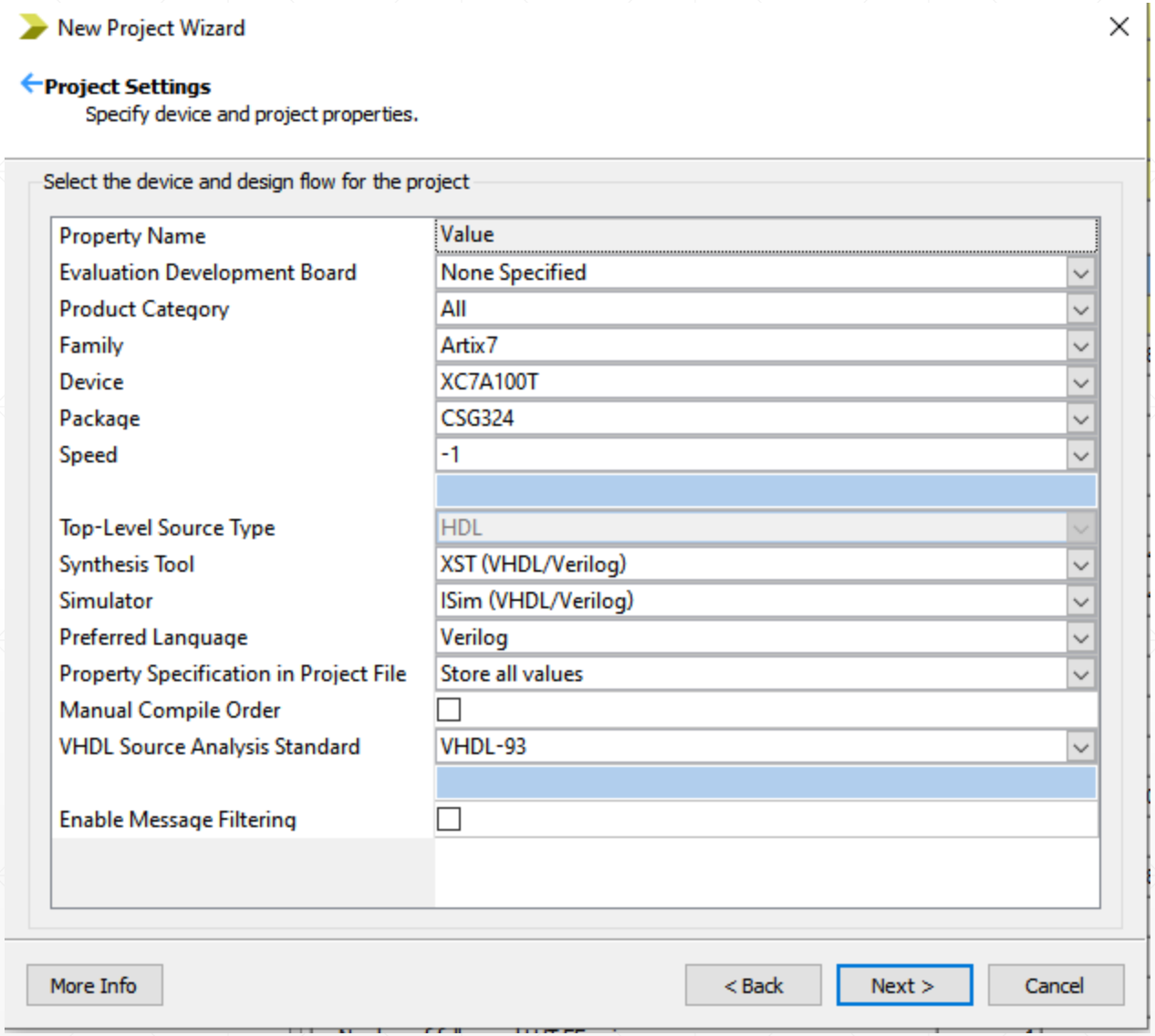
Verilog Live Demo

CS60004 : Hardware Security


Accumulator
clk
rst
In1(4 bits)
Adder
add_out
(5 bits)
DFF
acc
(5 bits)
dff_out
(5 bits)


New Project Wizard
Project Settings
Specify device and project properties.
Select the device and design flow for the project
Property Name
Value
Evaluation Development Board
None Specified
Product Category
All
Family
Artix7
Device
XC7A100T
Package
CSG324
Speed
-1
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISim (VHDL/Verilog)
Preferred Language
Verilog
Property Specification in Project File
Store all values
Manual Compile Order
VHDL Source Analysis Standard
VHDL-93
Enable Message Filtering
More Info
< Back
Next >
Cancel