

INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR
 Department of Computer Sc & Engg
 Computer Organisation and Architecture (CS31007)
 Mid-semester (Autumn)
 END

Place: NC: 142, 241, 242, 243, 244, 341

Date: Mon, Nov 21, 2022

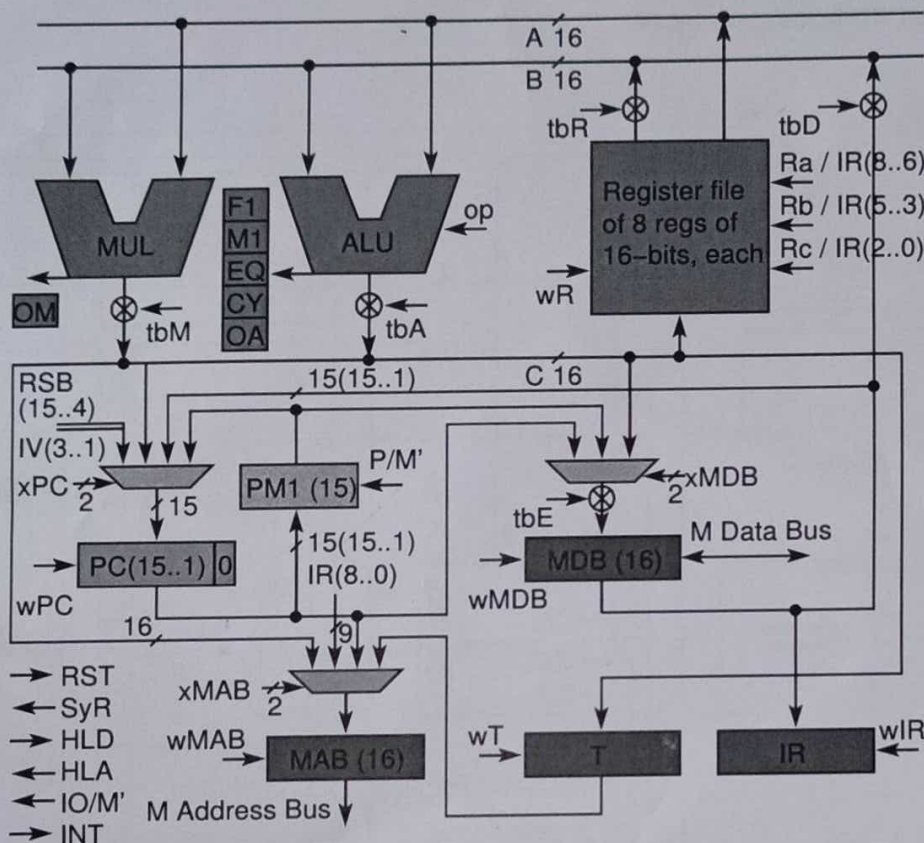
Time: 2-5pm (AN), 3 hours

Students: 155

Marks: 100

Answer ALL the questions

1. Consider the CPU in the given figure.



- (a) The **LDM R M** instruction for loading register **R** (indicated as **rrr**) with the contents of the memory location **M** consists of the main instruction as **1110000rrr-----** followed by a 16-bit address. List the micro-operations, with respect to the given data path, to carry out **LDM R M**, beyond instruction fetch. Show the activation of the control points to carry out the required micro operations.
- (b) The **JSR M** instruction for jump to subroutine consists of the main instruction as **11001-----** followed by a 16-bit address. List the micro-operations, with respect to the given data path, to carry out **JSR M**, beyond instruction fetch. Use **R7** as the stack pointer. You may assume that the ALU has opcodes to add/subtract 2. Show the activation of the control points to carry out the required micro operations.
- (c) How does the CPU handle an interrupt? Explain with respect to the given data path.
- (d) What are vectored interrupts and how are they used?

5

3

5

3

9

5

30

2. (a) Consider a two-level memory hierarchy comprising of a 2^n bytes main memory and 2^m bytes cache. The cache block (line) size is 2^p bytes. Illustrate the mapping of a physical address to a cache block for:
- direct mapping and
 - k -way associative mapping, where $k = 2^s$.
- (b) What is the Belady's anomaly in the context of caches and how can it be avoided?
- (c) What's the difference between *write back* and *write through* policies?
- (d) Explain the address translation scheme for virtual memory (VM) with paging and also explain how caching and VM work together.

5

5

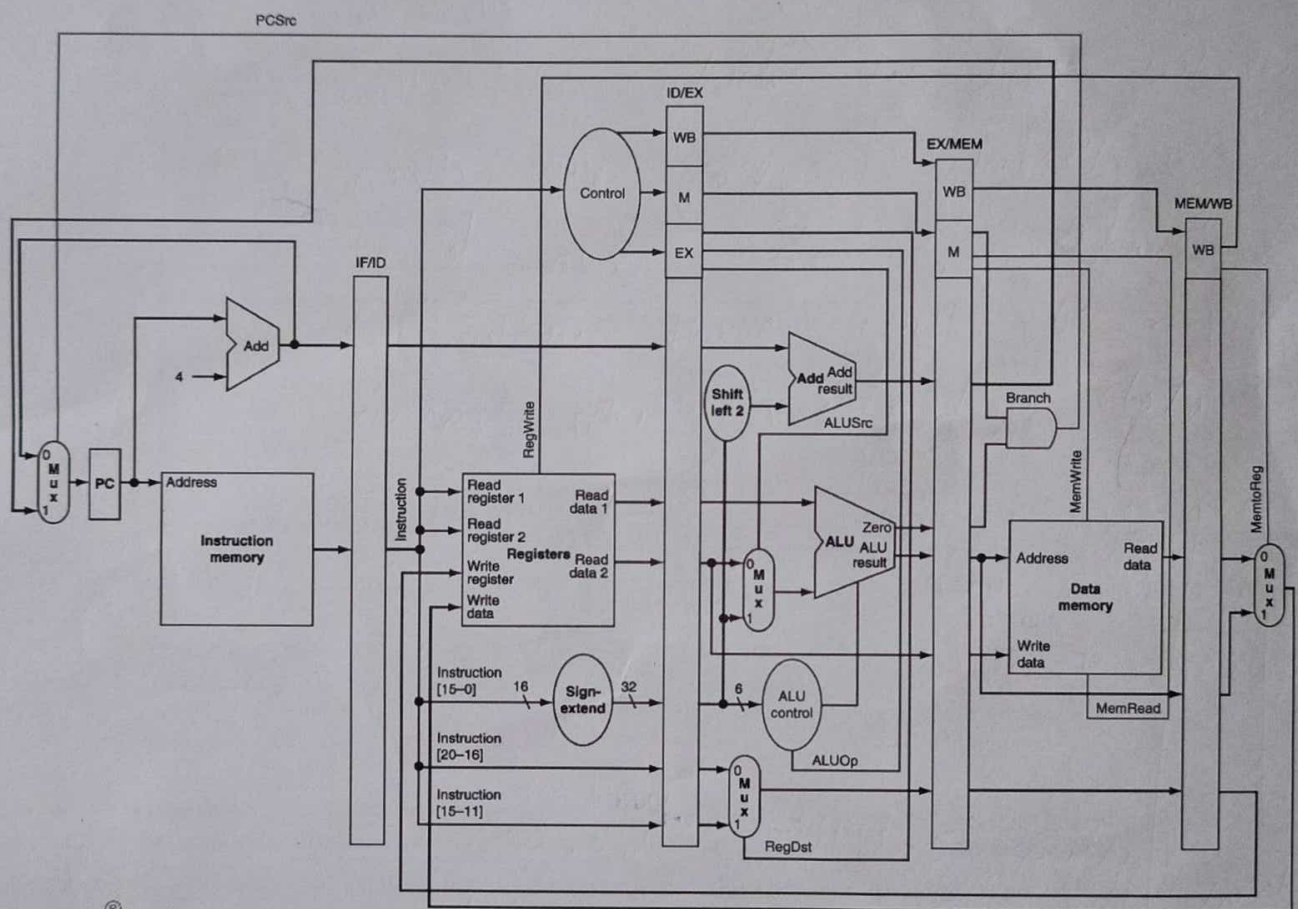
5

5

10

30

3. Consider the CPU in the given figure.



- (a) Explain the execution of a typical arithmetic instruction in such a pipelined CPU.
- (b) Explain the execution of load and store instructions in such a pipelined CPU.
- (c) What data hazards may arise in the operation of this pipelined CPU and how could those be resolved?
- (d) What control hazards may arise in the operation of this pipelined CPU and how could those be resolved?
- (e) How are interrupts handled in such a pipelined CPU?

5

5

10

5

5

30

4. (a) Explain the working of program controlled input/output and interrupt driven input/output, highlighting the benefits of the latter. 5
- (b) Explain the working of Direct Memory Access (DMA) for efficient data transfer, indicate the timing diagrams of the signals that are involved. How is CPU throughput increased with DMA? 5

10