Indian Institute of Technology (IIT-Kharagpur)

AUTUMN Semester, 2022
COMPUTER SCIENCE AND ENGINEERING

CS39001: Computer Organization Lab

Lab Test (Group 2)

INSTRUCTIONS: Please upload the verilog and project files to CSE Moodle.
You can submit the circuit diagrams on a sheet of paper. Make sure to write your name and roll number of the sheet.

Design a rotate circuit with shifters and adders only

Objective of the Project:

In this project, we would design a circuit which takes as input (x, y), both of which can be represented by an 8-bit number, and an angle to rotate by θ. The circuit should produce an output x_1, y_1, where the following holds:

$$\begin{pmatrix} x_1 \\ y_1 \end{pmatrix} = \frac{1}{cos\theta} \begin{pmatrix} cos\theta & -sin\theta \\ sin\theta & cos\theta \end{pmatrix} \cdot \begin{pmatrix} x \\ y \end{pmatrix}$$

For your convenience we provide with a look-up which you can store in your design to look up the value of $k = -log_2(tan\theta)$. Note that this is not defined for $\theta = 0°$. Also assume your possible values of θ given in Table 1, along with an additional possible input of $0°$.

For the design proceed in the following steps:

1. Represent x and y as two 8-bit numbers. Express x_1, y_1 in terms of x and y, and k. Note that the transformations can be done with only an 8-bit adder, and some programmable shifters. You can use other associated peripheral data-path elements, but no multipliers, etc. Draw the circuit diagram. For $\theta = 0°$, x_1, y_1 will be outputted unchanged. (20 marks)

2. Write the verilog code Rotbytheta in the Xilinx tool for realizing the circuit. Also write the test-bench to simulate the verilog code. Note that the top-level of the design module Rotbytheta must be structural, while the internal modules, may be behavioral. (20 marks)

3. Download the bit-stream onto your FPGA device and demonstrate its working. (10 marks)

Table 1: Different shift values (k) for various θ

θ	10°	20°	30°	40°	60°	70°	80°
k	3	2	1	0	-1	-2	-3