Computer Organization and Architecture Laboratory

Assignment 1

Introduction to Verilog Programming

Group 53
Umang Singla - 20CS10068
Siddharth Vishwakarma - 20CS10082

Half Adder

Half Adder is a combinational arithmetic circuit that adds two bits (A and B) and outputs a sum bit (S) and a carry bit (C).

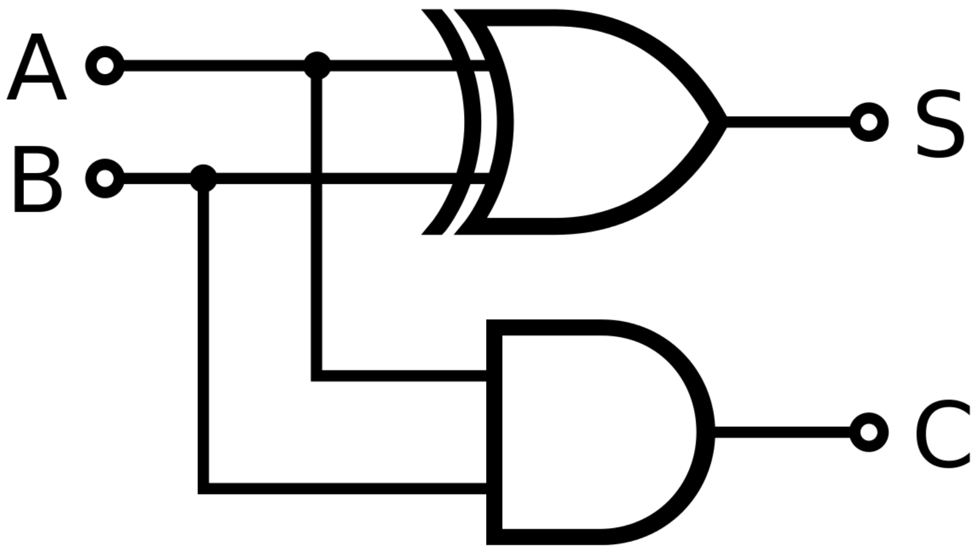
Truth Table for Half Adder

A (input)	B (input)	C (output)	S (output)
0	0	0	0
1	0	0	1
0	1	0	1
1	1	1	0

We can write the boolean expression for outputs as:

S = A $\otimes$ B

C = A.B



Relevant File(s): *half_addr.v, test_half_addr.v*

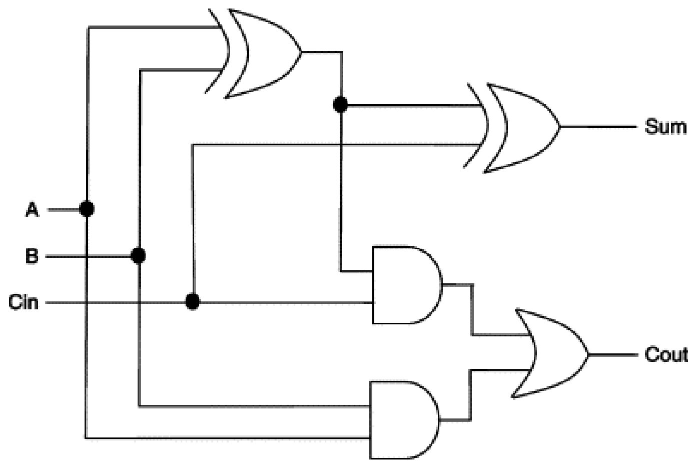
Full Adder

Half Adder is a combinational arithmetic circuit that adds three bits (A, B, and C-IN) and outputs a sum bit (S) and a carry bit (C-Out).

Truth Table for Full Adder

A (input)	B (input)	C-IN (input)	Sum (output)	C-Out (output)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

We can write the boolean expression for outputs as:
Sum = C-IN ⊗ (A ⊗ B)
C = A.B + A.C-IN + B.C-IN



Relevant File(s): *full_addr.v, test_full_addr.v*

Ripple Carry Adder

In the first step of this section, we cascade 8 full adders to create an 8-bit ripple carry adder. Next, a 16-bit ripple carry adder is created by cascading two 8-bit ripple carry adders. To create a 32-bit ripple carry adder, we similarly cascade two 16-bit ripple carry adders. The 64-bit ripple carry adder is created by cascading two 32-bit ripple carry adders.

Relevant File(s): *Ripple_Carry_Adder_8bit.v*
Ripple_Carry_Adder_16bit.v
Ripple_Carry_Adder_32bit.v
Ripple_Carry_Adder_64bit.v

How can you use the above circuit, to compute the difference between 2 n bits numbers?

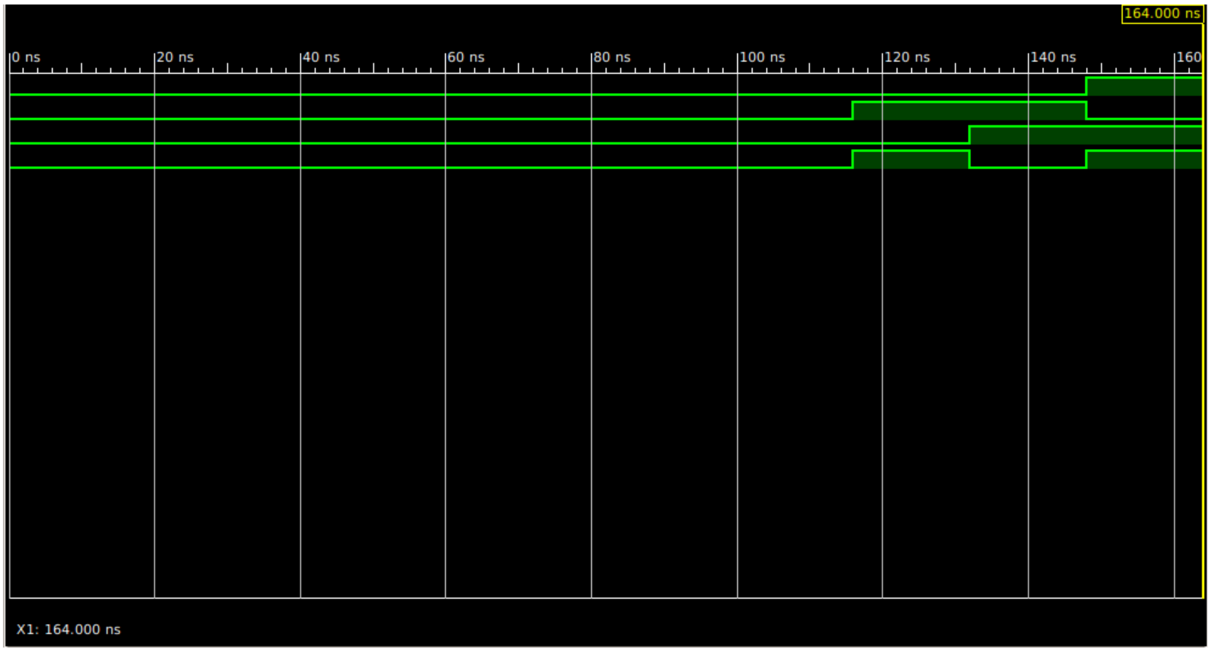
A ripple carry adder is used to calculate the sum of two n bits numbers. But we can modify our inputs to the adder so as to calculate the difference between 2 numbers as follows:

- ➢ a - b = a + (-b)
- ➢ -b is 2's complement of b, which can be computed as -b = ~b + 1, where ~b is 1's complement of b.
- ➢ So, we can calculate the difference between two numbers by passing a and ~b as input and 1 as carry-in.

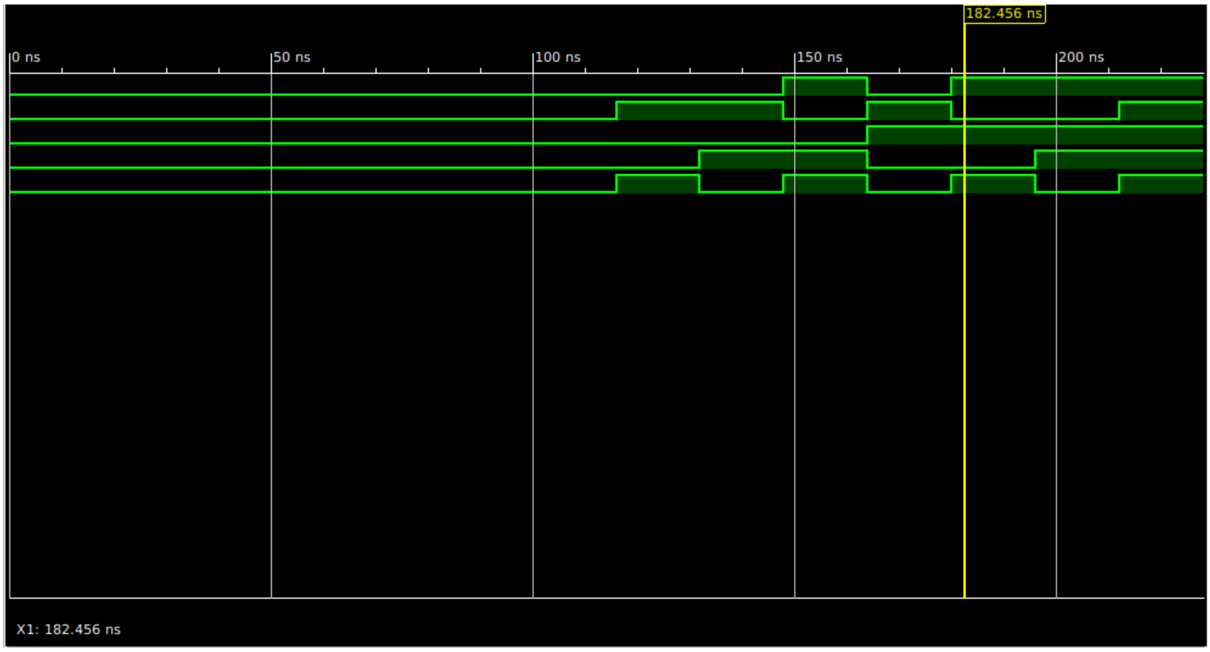
Synthesis Summary

Circuit	Total Delay (in ns)
Half Adder	1.066
Full Adder	1.246
8-bit RCA	3.471
16-bit RCA	6.167
32-bit RCA	11.559
64-bit RCA	22.343

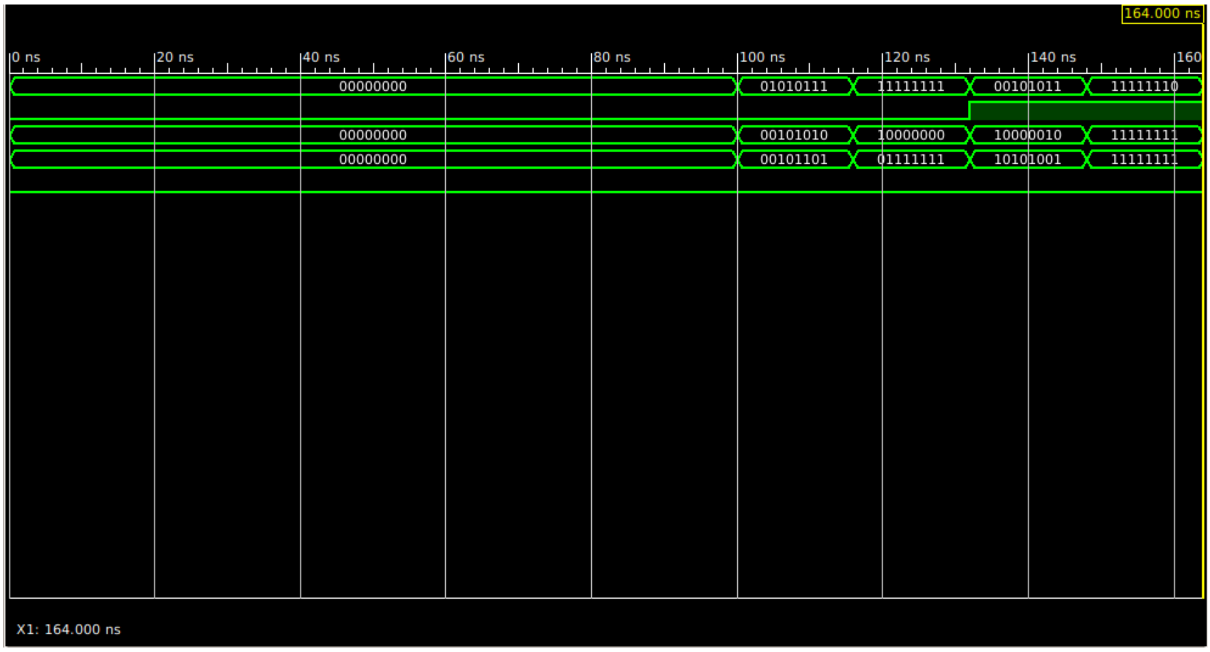
Behavioral Simulation Screesshots:



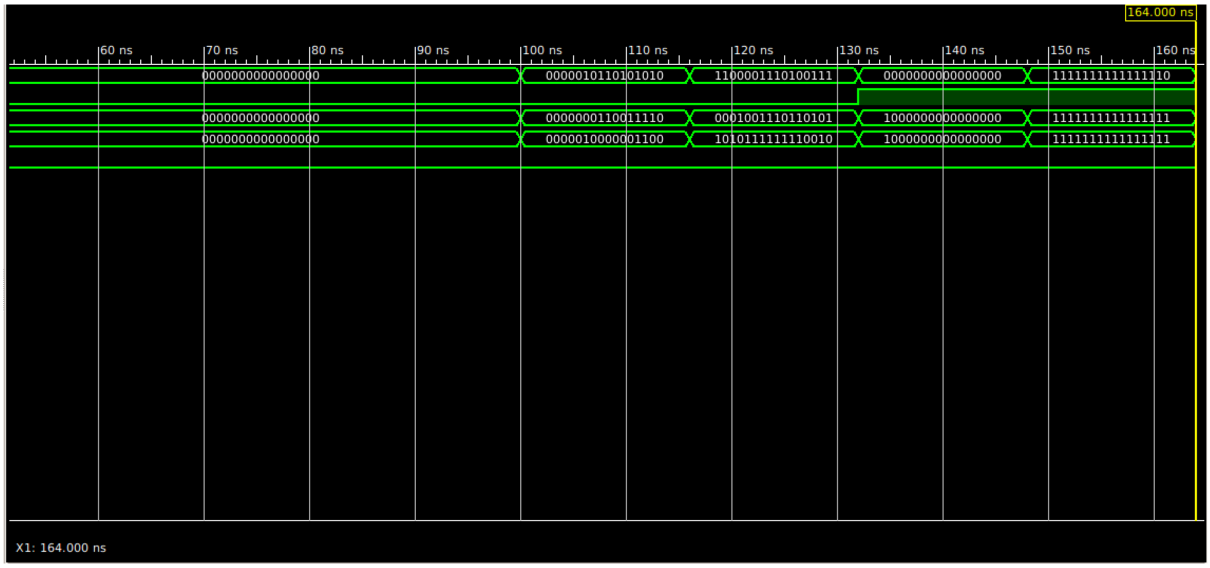
HALF ADDER



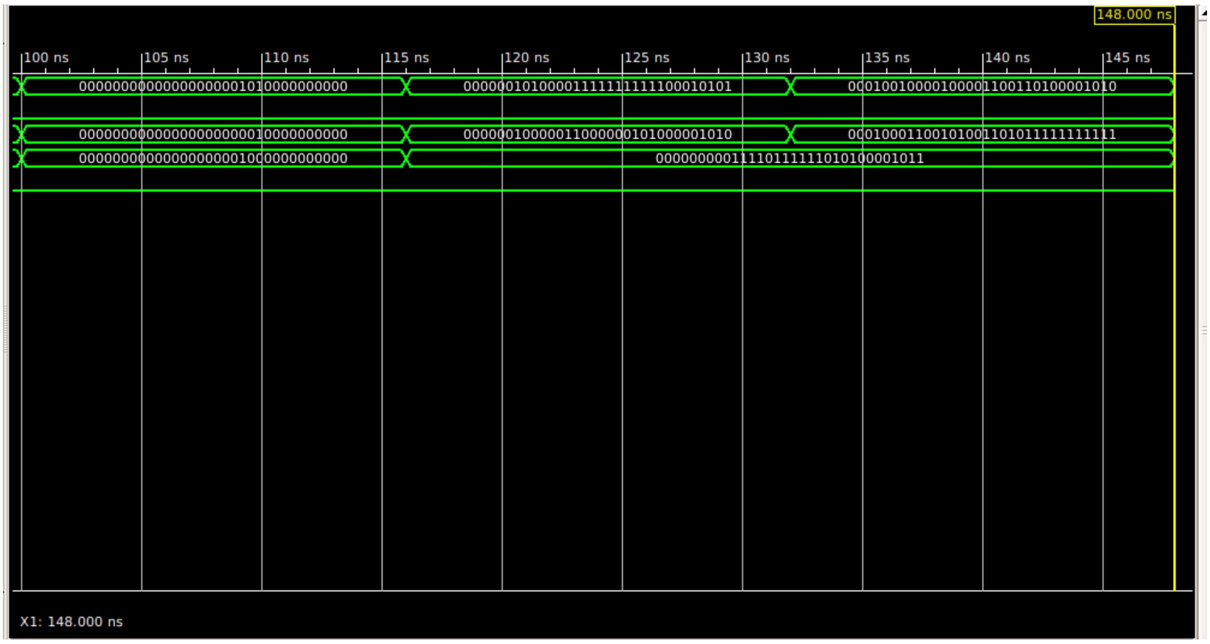
FULL ADDER



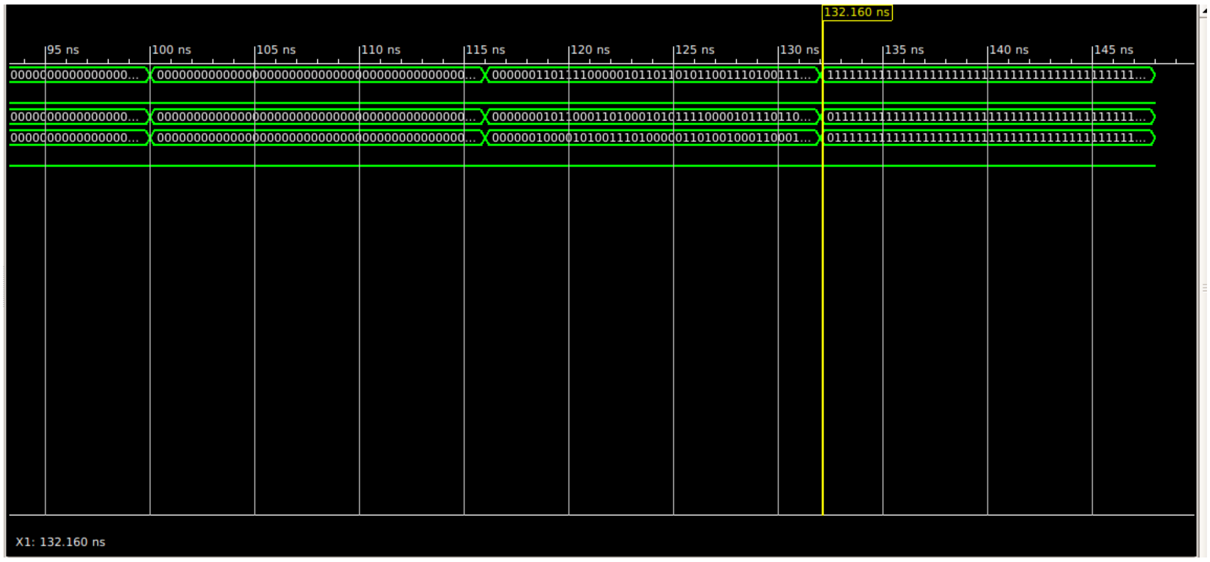
8-BIT RCA



16-BIT RCA



32-BIT RCA



64-BIT RCA

Relevant Files for Test Bench:

- *test_half_adder.v*
- *test_full_adder.v*
- *test_RCA_8bit.v*
- *test_RCA_16bit.v*
- *test_RCA_32bit.v*
- *test_RCA_64bit.v*
- *test_RCA_difference.v*