Release 14.7 - xst P.20131013 (lin64)

-->
Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.02 secs

-->
Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.02 secs

-->
Reading design: half_addr.prj

TABLE OF CONTENTS

===
*   Synthesis Options Summary   *
===
---- Source Parameters
Input File Name   : "half_addr.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name   : "half_addr"
Output Format   : NGC
Target Device   : xc7a100t-1-csg324

---- Source Options
Top Module Name   : half_addr

Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 32
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

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* HDL Parsing *
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```
Analyzing Verilog file "/home/siddharth/Assignment_3/half_addr.v" into library work
Parsing module <half_addr>.

=========================================================================
*                     HDL Elaboration                     *
=========================================================================

Elaborating module <half_addr>.

=========================================================================
*                     HDL Synthesis                       *
=========================================================================

Synthesizing Unit <half_addr>.
    Related source file is "/home/siddharth/Assignment_3/half_addr.v".
    Summary:
Unit <half_addr> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Xors                                  : 1
 1-bit xor2                            : 1

=========================================================================

=========================================================================
*                 Advanced HDL Synthesis                  *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Xors                                  : 1
 1-bit xor2                            : 1

=========================================================================

=========================================================================
*                     Low Level Synthesis                 *
=========================================================================

Optimizing unit <half_addr> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block half_addr, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report
```

Found no macro
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*   Partition Report   *
===

Partition Implementation Status

  No Partitions were found in this design.

===
*   Design Summary   *
===

Top Level Output File Name   : half_addr.ngc

Primitive and Black Box Usage:

BELS   : 2
LUT2   : 2
IO Buffers   : 4
IBUF   : 2
OBUF   : 2

Device utilization summary:

Selected Device : 7a100tcsg324-1

Slice Logic Utilization:
 Number of Slice LUTs: 2 out of 63400   0%
    Number used as Logic: 2 out of 63400   0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used: 2
   Number with an unused Flip Flop: 2 out of   2   100%
   Number with an unused LUT: 0 out of   2   0%
   Number of fully used LUT-FF pairs: 0 out of   2   0%
   Number of unique control sets: 0

IO Utilization:
 Number of IOs: 4
 Number of bonded IOBs: 4 out of   210   1%

Specific Feature Utilization:

Partition Resource Summary:

No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -1

Minimum period: No path found
Minimum input arrival time before clock: No path found
Maximum output required time after clock: No path found
Maximum combinational path delay: 1.066ns

Timing Details:

All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis
Total number of paths / destination ports: 4 / 2

Delay: 1.066ns (Levels of Logic = 3)
Source: a (PAD)
Destination: cout (PAD)

Data Path: a to cout

Cell:in->out	Gate fanout	Net Delay	Delay	Logical Name (Net Name)
IBUF:I->O	2	0.001	0.542	a_IBUF (a_IBUF)
LUT2:I0->O	1	0.124	0.399	cout1 (cout_OBUF)
OBUF:I->O		0.000		cout_OBUF (cout)
Total		1.066ns (0.125ns logic, 0.941ns route) (11.7% logic, 88.3% route)		

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Cross Clock Domains Report:

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Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 4.33 secs

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Total memory usage is 479452 kilobytes

Number of errors   :   0 (0 filtered)
Number of warnings :   0 (0 filtered)
Number of infos   :   0 (0 filtered)