Release 14.7 - xst P.20131013 (lin64)

-->
Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.03 secs

-->
Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.03 secs

-->
Reading design: Ripple_Carry_Addr_8bit.prj

TABLE OF CONTENTS

===
*   Synthesis Options Summary   *
===
---- Source Parameters
Input File Name   : "Ripple_Carry_Addr_8bit.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name   : "Ripple_Carry_Addr_8bit"
Output Format   : NGC
Target Device   : xc7a100t-1-csg324

---- Source Options
Top Module Name   : Ripple_Carry_Addr_8bit

Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 32
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

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* HDL Parsing *
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```
Analyzing Verilog file "/home/siddharth/Assignment_3/half_addr.v" into library work
Parsing module <half_addr>.
Analyzing Verilog file "/home/siddharth/Assignment_3/full_addr.v" into library work
Parsing module <full_addr>.
Analyzing Verilog file "/home/siddharth/Assignment_3/Ripple_Carry_Addr_8bit.v" into library work
Parsing module <Ripple_Carry_Addr_8bit>.

=========================================================================
*                     HDL Elaboration                     *
=========================================================================

Elaborating module <Ripple_Carry_Addr_8bit>.

Elaborating module <full_addr>.

Elaborating module <half_addr>.

=========================================================================
*                     HDL Synthesis                       *
=========================================================================

Synthesizing Unit <Ripple_Carry_Addr_8bit>.
    Related source file is "/home/siddharth/Assignment_3/Ripple_Carry_Addr_8bit.v".
    Summary:
 no macro.
Unit <Ripple_Carry_Addr_8bit> synthesized.

Synthesizing Unit <full_addr>.
    Related source file is "/home/siddharth/Assignment_3/full_addr.v".
    Summary:
 no macro.
Unit <full_addr> synthesized.

Synthesizing Unit <half_addr>.
    Related source file is "/home/siddharth/Assignment_3/half_addr.v".
    Summary:
Unit <half_addr> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Xors                                  : 16
 1-bit xor2                            : 16

=========================================================================

=========================================================================
*                  Advanced HDL Synthesis                 *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report
```

Macro Statistics
Xors : 16
1-bit xor2 : 16

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* Low Level Synthesis *
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Optimizing unit <Ripple_Carry_Addr_8bit> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block Ripple_Carry_Addr_8bit, actual ratio is 0.

Final Macro Processing ...

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Final Register Report

Found no macro
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* Partition Report *
==========

Partition Implementation Status

No Partitions were found in this design.

==========
* Design Summary *
==========

Top Level Output File Name : Ripple_Carry_Addr_8bit.ngc

Primitive and Black Box Usage:

BELS : 12
LUT3 : 4
LUT5 : 8
IO Buffers : 26
IBUF : 17
OBUF : 9

Device utilization summary:

Selected Device : 7a100tcsg324-1

Slice Logic Utilization:
 Number of Slice LUTs: 12 out of 63400   0%
    Number used as Logic: 12 out of 63400   0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used: 12
   Number with an unused Flip Flop: 12 out of   12   100%
   Number with an unused LUT: 0 out of   12   0%
   Number of fully used LUT-FF pairs: 0 out of   12   0%
   Number of unique control sets: 0

IO Utilization:
 Number of IOs: 26
 Number of bonded IOBs: 26 out of   210   12%

Specific Feature Utilization:

Partition Resource Summary:

  No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

No clock signals found in this design

Asynchronous Control Signals Information:

No asynchronous control signals found in this design

Timing Summary:

Speed Grade: -1

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 3.471ns

Timing Details:

All values displayed in nanoseconds (ns)

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=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 97 / 9
-------------------------------------------------------------------------
Delay:               3.471ns (Levels of Logic = 6)
  Source:            A<1> (PAD)
  Destination:       S<7> (PAD)

  Data Path: A<1> to S<7>
                        Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2   0.001   0.925  A_1_IBUF (A_1_IBUF)
     LUT5:I0->O            3   0.124   0.550  fa1/cout1 (c2)
     LUT5:I3->O            3   0.124   0.550  fa3/cout1 (c4)
     LUT5:I3->O            3   0.124   0.550  fa5/cout1 (c6)
     LUT5:I3->O            1   0.124   0.399  fa7/cout1 (cout_OBUF)
     OBUF:I->O                 0.000          cout_OBUF (cout)
    ----------------------------------------
    Total                      3.471ns (0.497ns logic, 2.974ns route)
                               (14.3% logic, 85.7% route)

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Cross Clock Domains Report:
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=========================================================================


Total REAL time to Xst completion: 5.00 secs
Total CPU time to Xst completion: 4.66 secs

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Total memory usage is 479548 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```