Release 14.7 - xst P.20131013 (lin64)

-->
Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.01 secs

-->
Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.01 secs

-->
Reading design: Ripple_Carry_Addr_16bit.prj

TABLE OF CONTENTS

===
*   Synthesis Options Summary   *
===
---- Source Parameters
Input File Name   : "Ripple_Carry_Addr_16bit.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name   : "Ripple_Carry_Addr_16bit"
Output Format   : NGC
Target Device   : xc7a100t-1-csg324

---- Source Options
Top Module Name   : Ripple_Carry_Addr_16bit

Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No

---- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 32
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES

---- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5

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* HDL Parsing *
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```
Analyzing Verilog file "/home/siddharth/Assignment_3/half_addr.v" into library work
Parsing module <half_addr>.
Analyzing Verilog file "/home/siddharth/Assignment_3/full_addr.v" into library work
Parsing module <full_addr>.
Analyzing Verilog file "/home/siddharth/Assignment_3/Ripple_Carry_Addr_8bit.v" into library work
Parsing module <Ripple_Carry_Addr_8bit>.
Analyzing Verilog file "/home/siddharth/Assignment_3/Ripple_Carry_Addr_16bit.v" into library work
Parsing module <Ripple_Carry_Addr_16bit>.

=========================================================================
*                     HDL Elaboration                     *
=========================================================================

Elaborating module <Ripple_Carry_Addr_16bit>.

Elaborating module <Ripple_Carry_Addr_8bit>.

Elaborating module <full_addr>.

Elaborating module <half_addr>.

=========================================================================
*                     HDL Synthesis                       *
=========================================================================

Synthesizing Unit <Ripple_Carry_Addr_16bit>.
    Related source file is "/home/siddharth/Assignment_3/Ripple_Carry_Addr_16bit.v".
    Summary:
 no macro.
Unit <Ripple_Carry_Addr_16bit> synthesized.

Synthesizing Unit <Ripple_Carry_Addr_8bit>.
    Related source file is "/home/siddharth/Assignment_3/Ripple_Carry_Addr_8bit.v".
    Summary:
 no macro.
Unit <Ripple_Carry_Addr_8bit> synthesized.

Synthesizing Unit <full_addr>.
    Related source file is "/home/siddharth/Assignment_3/full_addr.v".
    Summary:
 no macro.
Unit <full_addr> synthesized.

Synthesizing Unit <half_addr>.
    Related source file is "/home/siddharth/Assignment_3/half_addr.v".
    Summary:
Unit <half_addr> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Xors                                  : 32
 1-bit xor2                            : 32
```

```
=========================================================================

=========================================================================
*                  Advanced HDL Synthesis                  *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Xors                                  : 32
 1-bit xor2                            : 32

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=========================================================================
*                  Low Level Synthesis                  *
=========================================================================

Optimizing unit <Ripple_Carry_Addr_16bit> ...

Optimizing unit <Ripple_Carry_Addr_8bit> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block Ripple_Carry_Addr_16bit, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Found no macro
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=========================================================================
*                  Partition Report                  *
=========================================================================

Partition Implementation Status
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  No Partitions were found in this design.

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=========================================================================
*                  Design Summary                  *
=========================================================================

Top Level Output File Name         : Ripple_Carry_Addr_16bit.ngc

Primitive and Black Box Usage:
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```
# BELS                      : 24
#      LUT3                 : 8
#      LUT5                 : 16
# IO Buffers                : 50
#      IBUF                 : 33
#      OBUF                 : 17

Device utilization summary:
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Selected Device : 7a100tcsg324-1


Slice Logic Utilization:
 Number of Slice LUTs:                 24  out of  63400     0%
    Number used as Logic:              24  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     24
   Number with an unused Flip Flop:      24  out of     24   100%
   Number with an unused LUT:             0  out of     24     0%
   Number of fully used LUT-FF pairs:     0  out of     24     0%
   Number of unique control sets:         0

IO Utilization:
 Number of IOs:                    50
 Number of bonded IOBs:                50  out of    210    23%

Specific Feature Utilization:

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Partition Resource Summary:
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  No Partitions were found in this design.

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================================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
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No asynchronous control signals found in this design

Timing Summary:
```

Speed Grade: -1

  Minimum period: No path found
  Minimum input arrival time before clock: No path found
  Maximum output required time after clock: No path found
  Maximum combinational path delay: 6.167ns

Timing Details:

All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis
  Total number of paths / destination ports: 321 / 17

Delay: 6.167ns (Levels of Logic = 10)
  Source: A<1> (PAD)
  Destination: S<15> (PAD)

  Data Path: A<1> to S<15>
                        Gate   Net
    Cell:in->out   fanout   Delay   Delay Logical Name (Net Name)
    -- ------------
    IBUF:I->O   2   0.001   0.925 A_1_IBUF (A_1_IBUF)
    LUT5:I0->O   3   0.124   0.550 rca_8bit_1/fa1/cout1 (rca_8bit_1/c2)
    LUT5:I3->O   3   0.124   0.550 rca_8bit_1/fa3/cout1 (rca_8bit_1/c4)
    LUT5:I3->O   3   0.124   0.550 rca_8bit_1/fa5/cout1 (rca_8bit_1/c6)
    LUT5:I3->O   3   0.124   0.550 rca_8bit_1/fa7/cout1 (temp_cout)
    LUT5:I3->O   3   0.124   0.550 rca_8bit_2/fa1/cout1 (rca_8bit_2/c2)
    LUT5:I3->O   3   0.124   0.550 rca_8bit_2/fa3/cout1 (rca_8bit_2/c4)
    LUT5:I3->O   3   0.124   0.550 rca_8bit_2/fa5/cout1 (rca_8bit_2/c6)
    LUT5:I3->O   1   0.124   0.399 rca_8bit_2/fa7/ha2/Mxor_sum_xo<0>1 (S_15_OBUF)
    OBUF:I->O   0.000   S_15_OBUF (S<15>)

    Total   6.167ns (0.993ns logic, 5.174ns route)
                                 (16.1% logic, 83.9% route)

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Cross Clock Domains Report:

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Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 4.27 secs

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Total memory usage is 479600 kilobytes

Number of errors   :   0 (0 filtered)

Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)