Computer Organization and Architecture Laboratory

Verilog Assignment 2

4-bit counter using verilog

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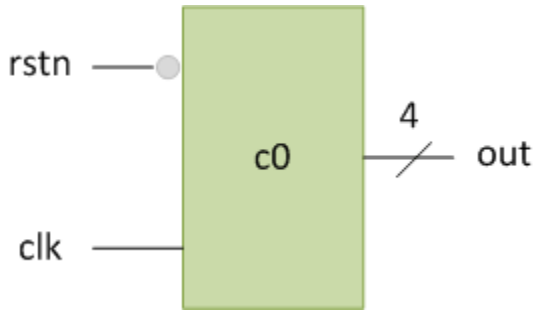
4-bit counter

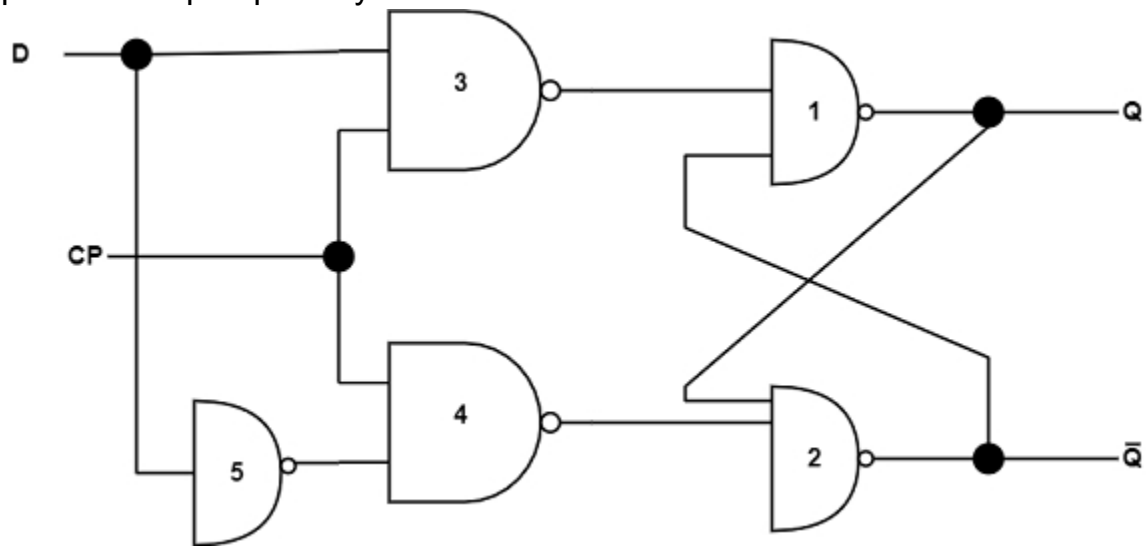
A 4 bit counter starts increasing from 4’b0000 to 4’b1111 and then roll backs to 4’b0000. The 4-bit counter will keep on running until the clock is running and the reset is in high state.

The design contains 2 inputs one for the clock and another for an active-low reset. When the value of the reset pin is 0 the counter starts again from 4’b0000. There is one output which gives the counter value.



D Flip Flop:

The D flip-flop has a single digital input labeled "D" and is a clocked flip-flop. The output of a D flip-flop always reflects the state of the word "D" when it is clocked.



Schematic Circuit for Structural 4-bit Counter