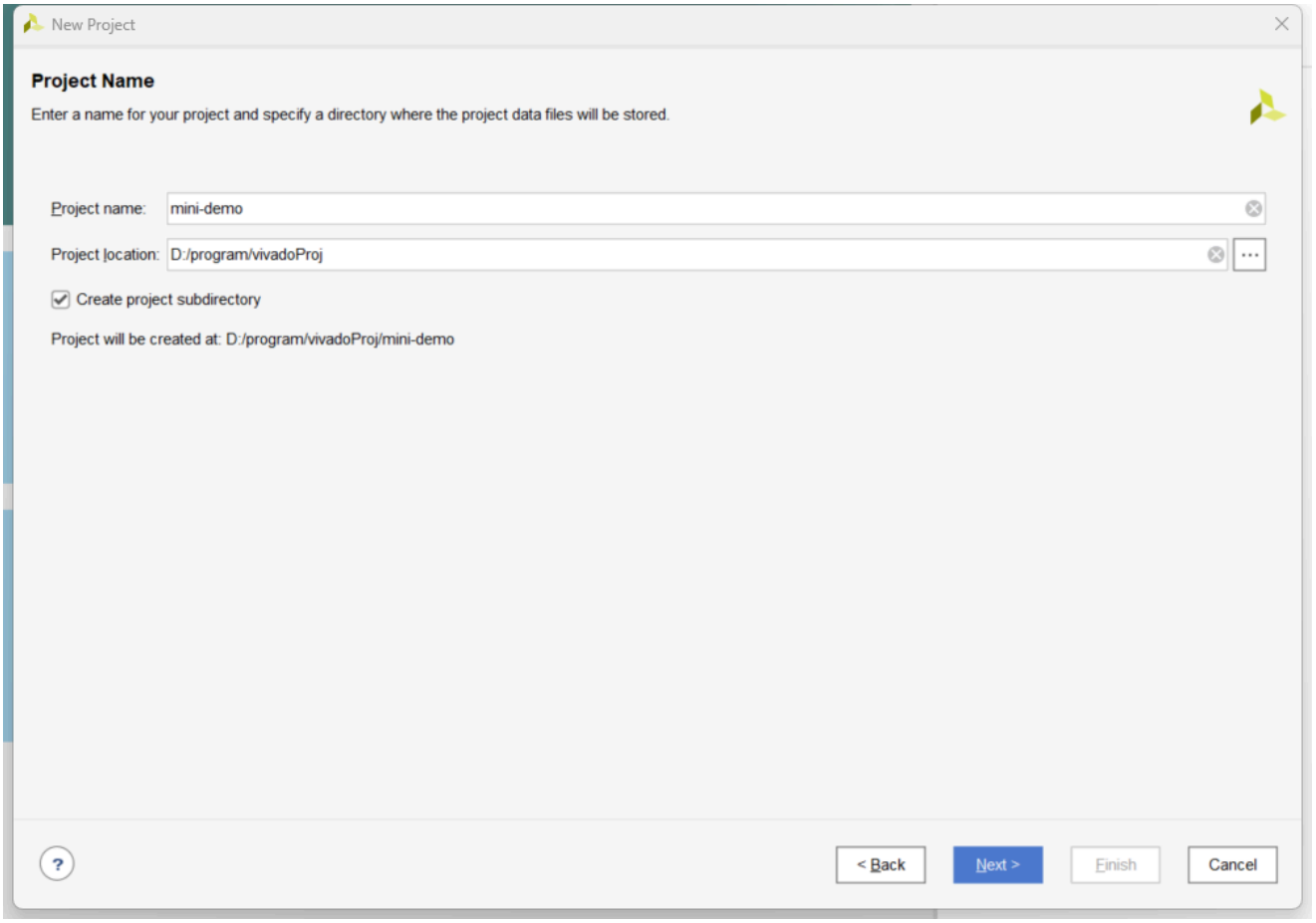
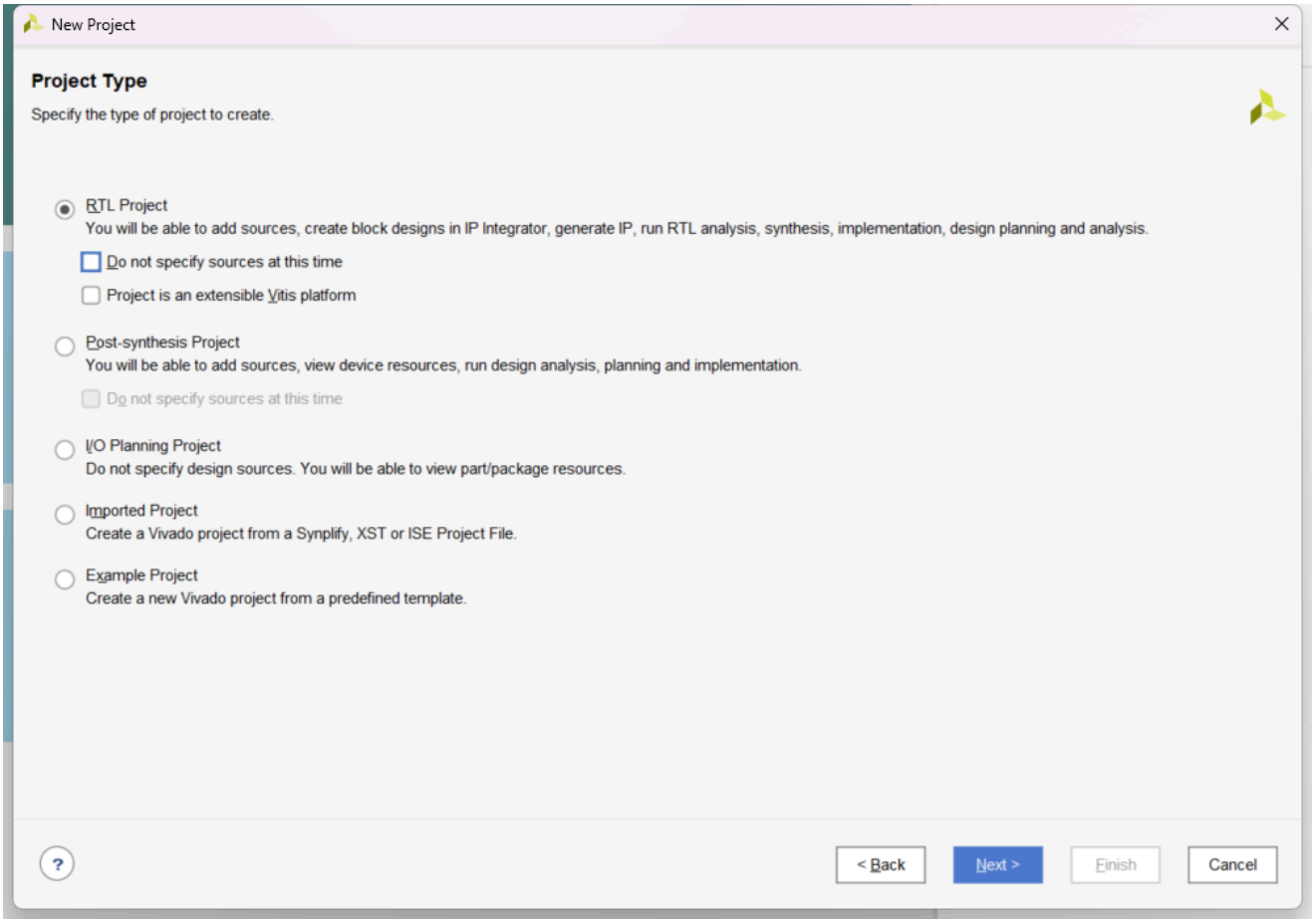
mini的FPGA烧写过程

创建项目导入文件

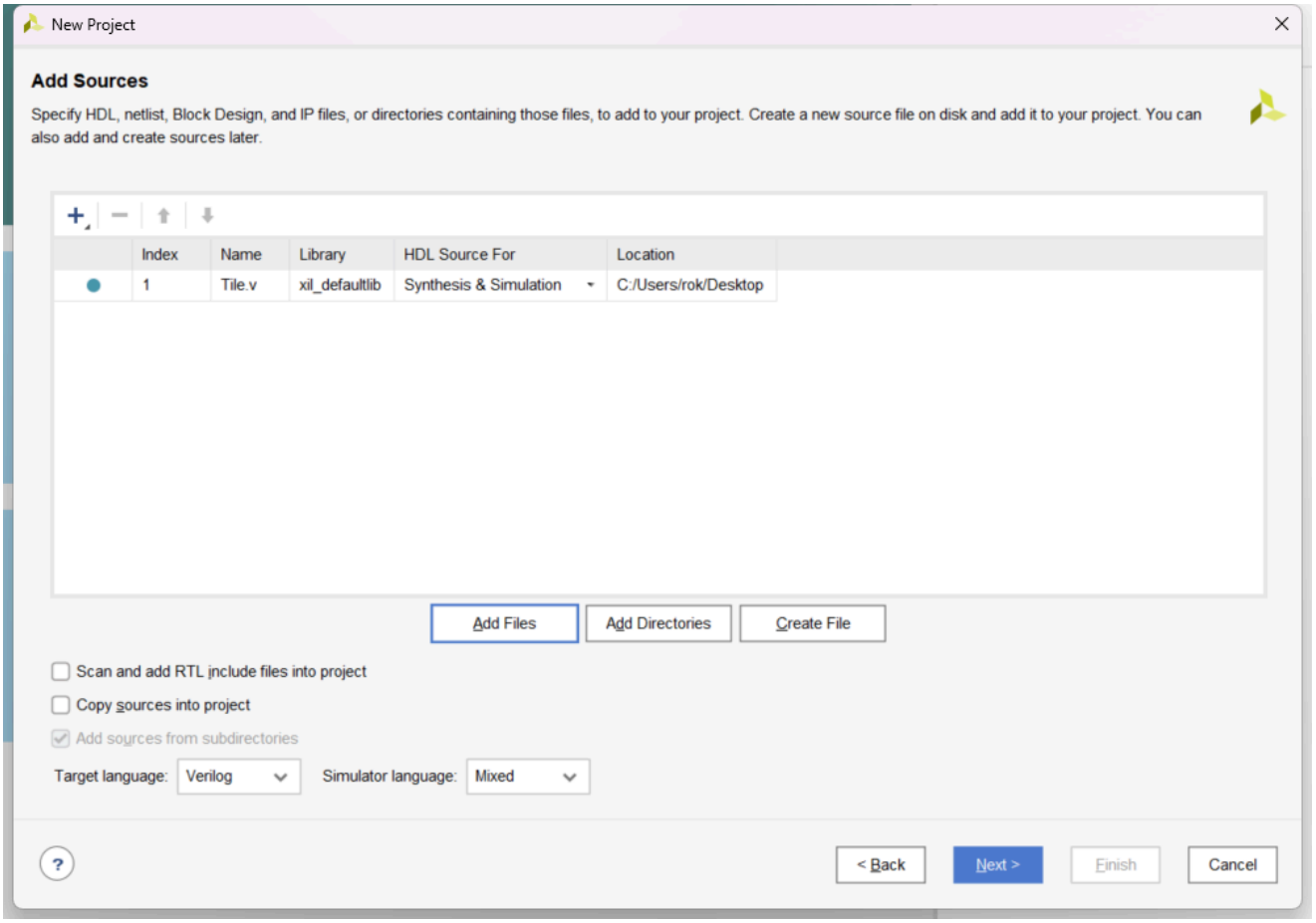
新建一个项目



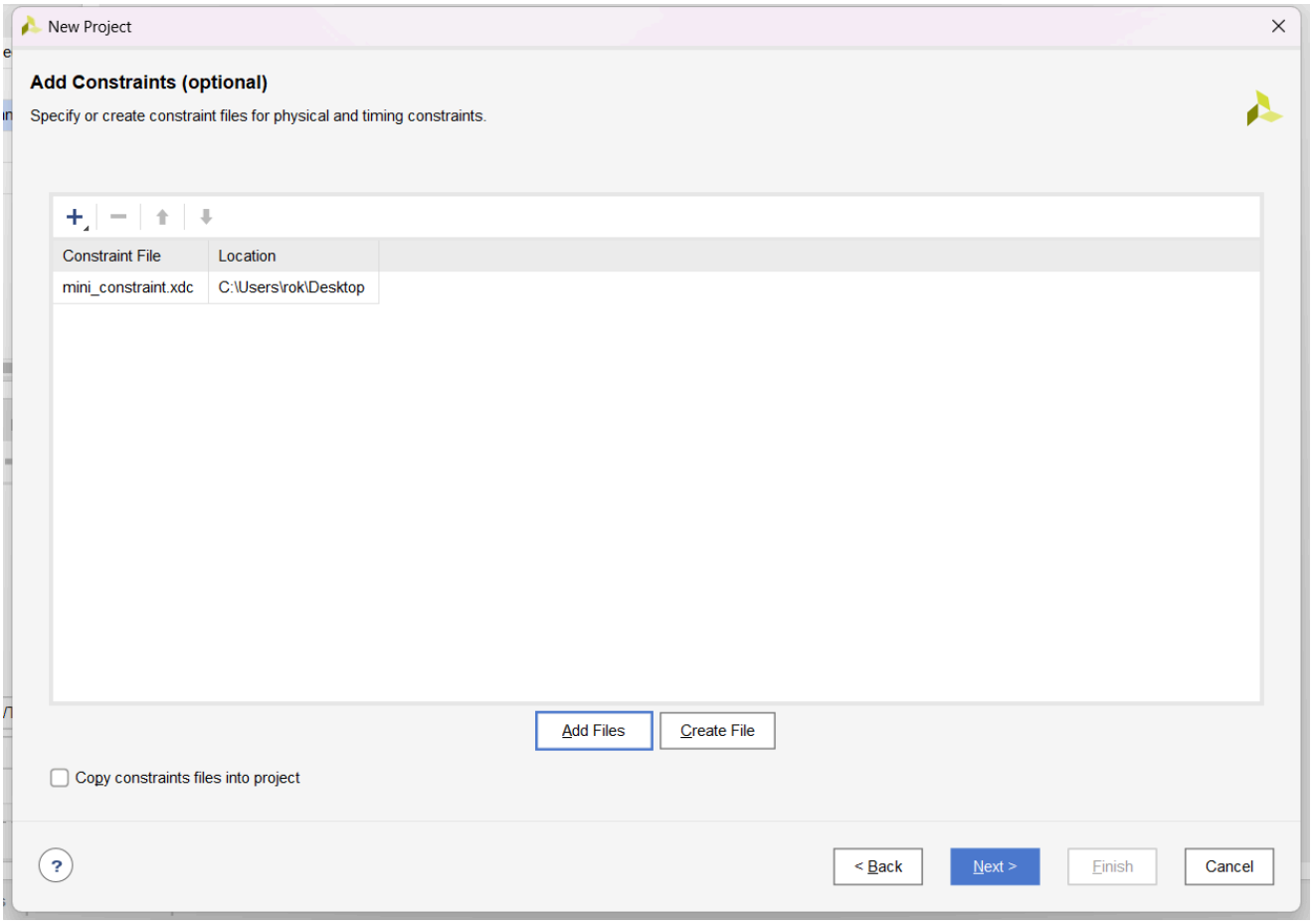
不勾选“Do not specify sources at this time”



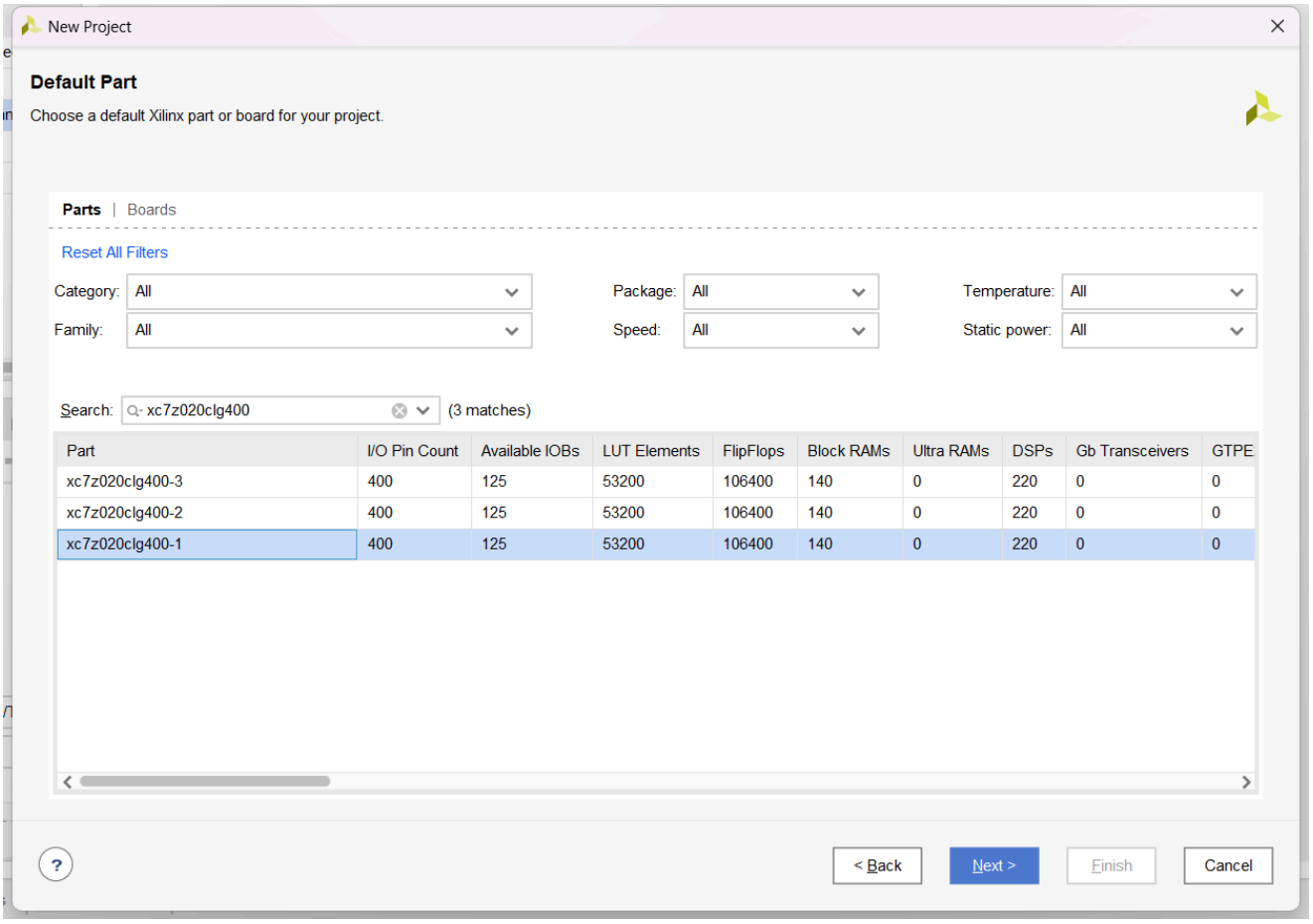
添加对应Verilog文件



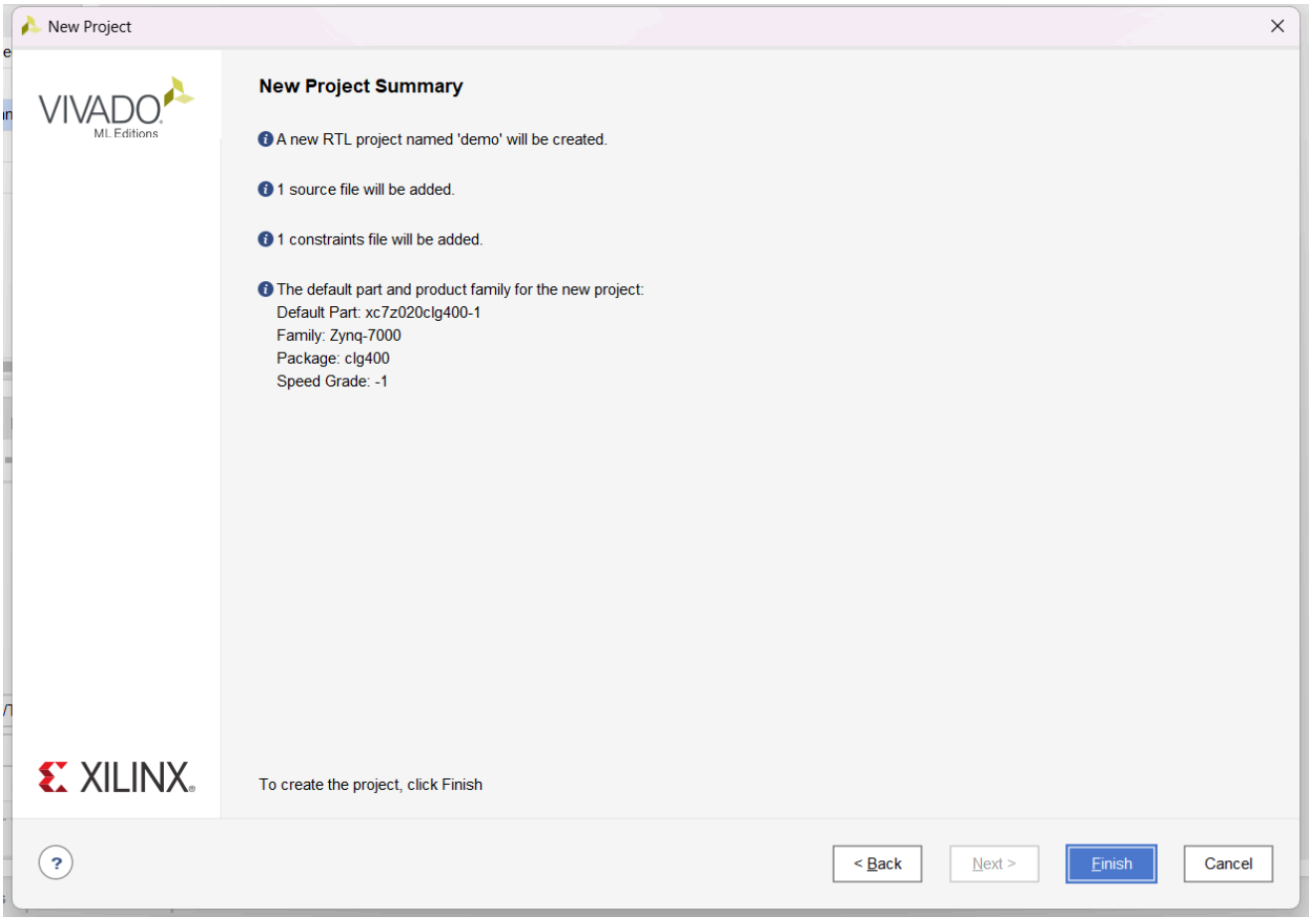
添加对应约束文件



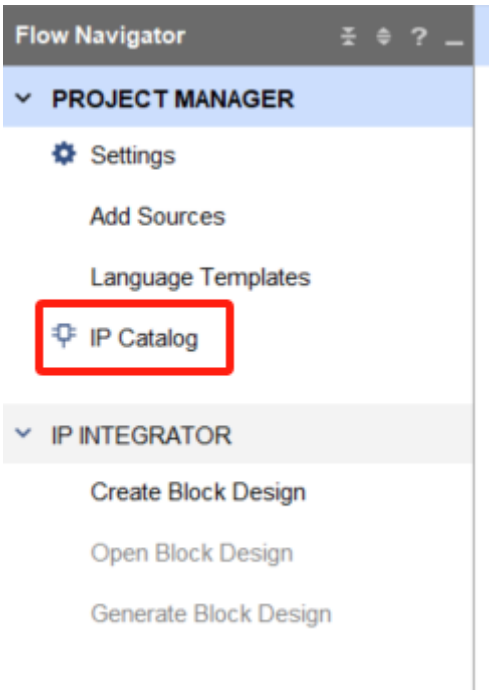
选择FPGA芯片型号



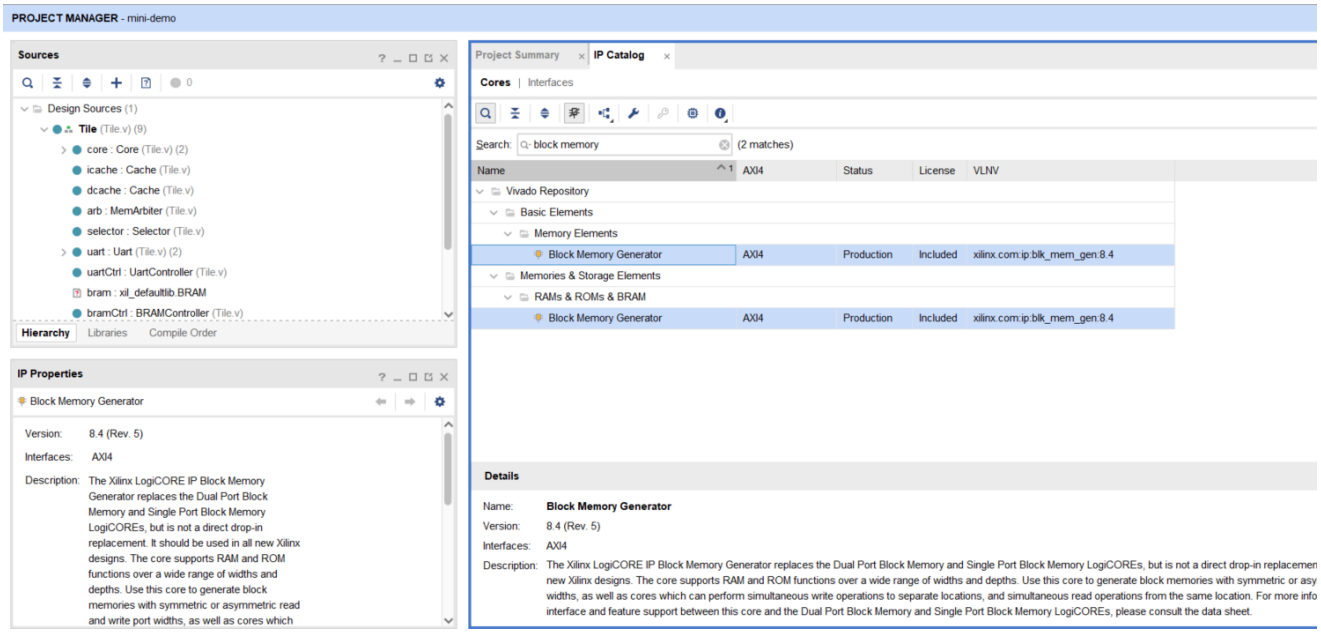
点击Finish创建完成



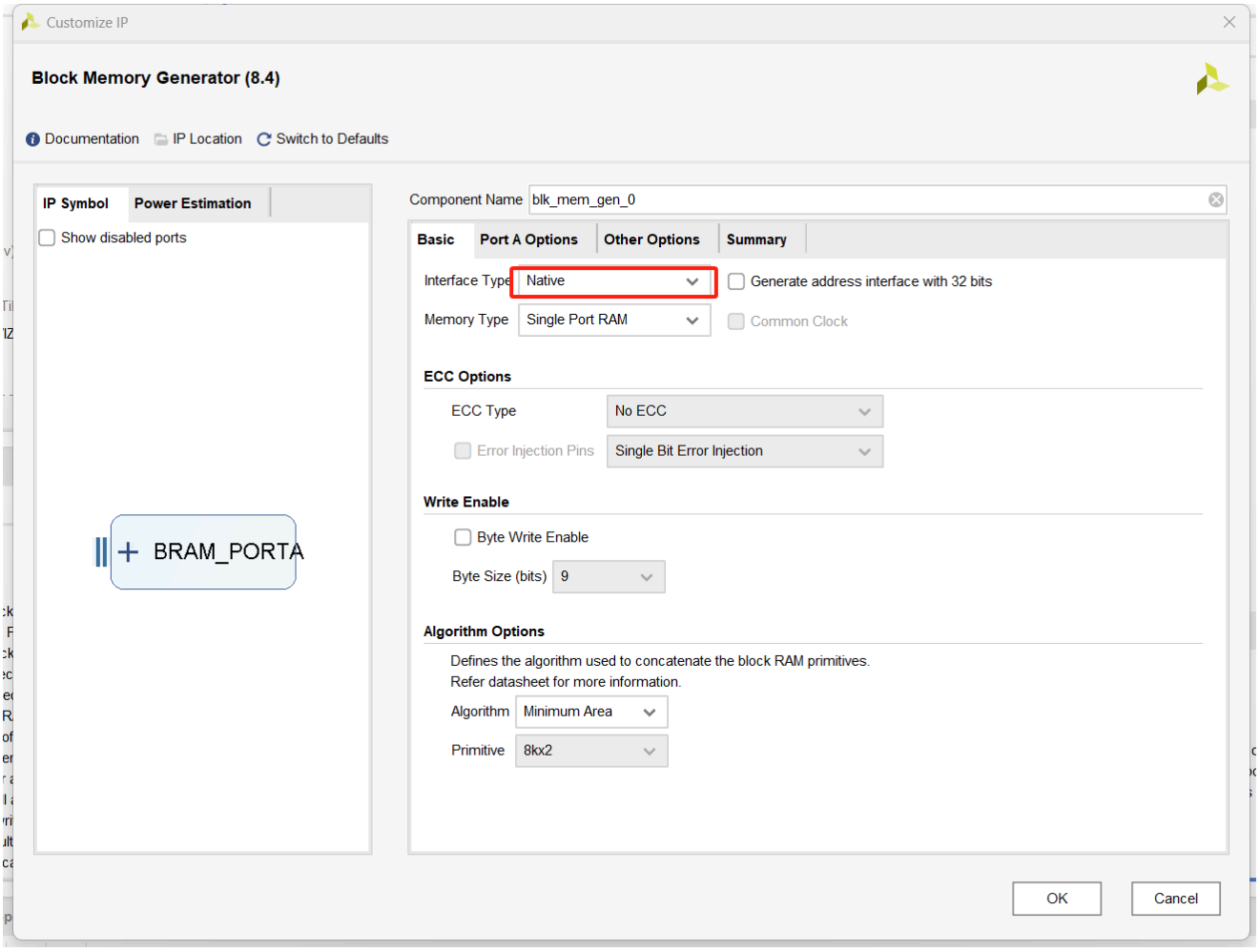
添加BRAM IP Core



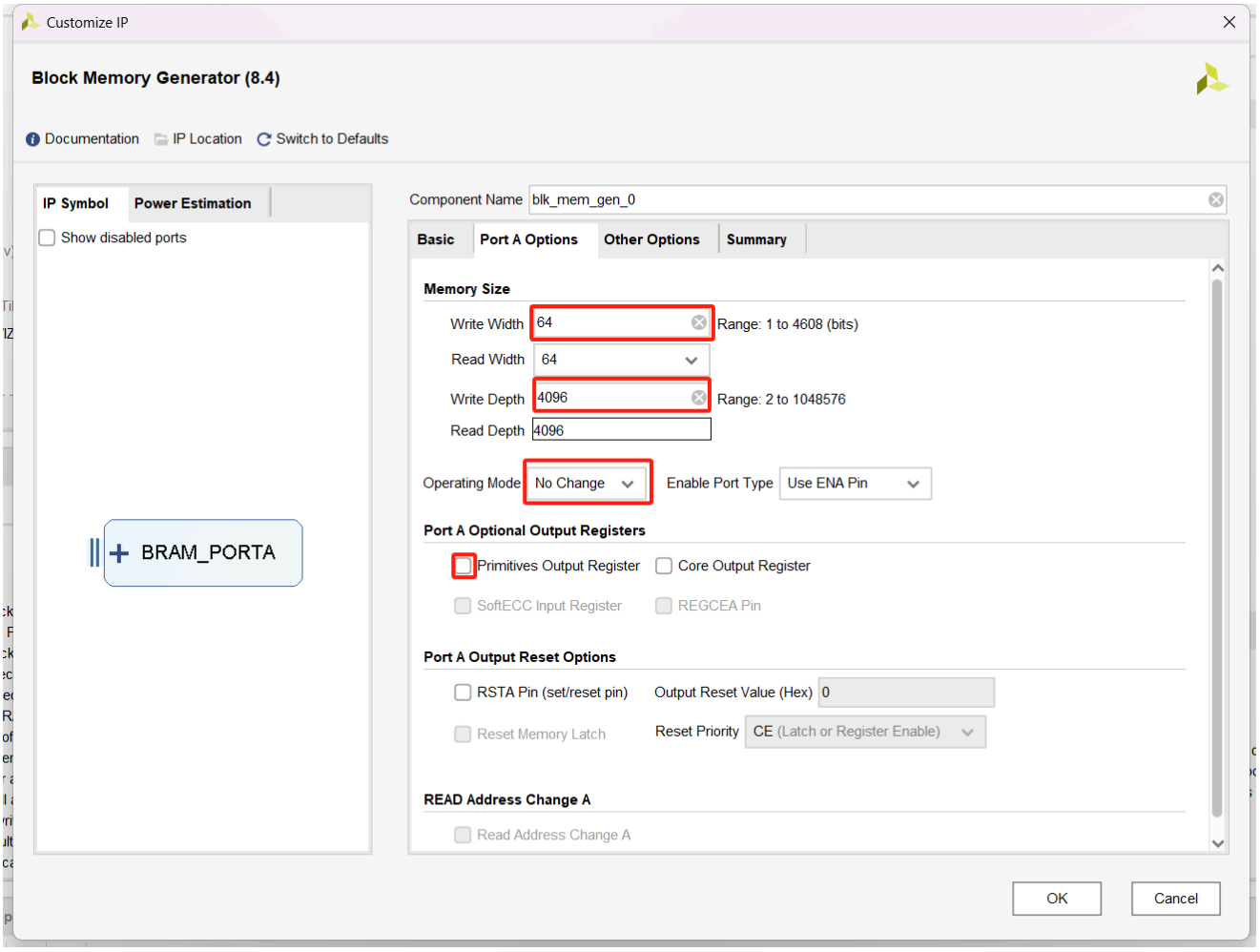
从IP Catalog中搜索选择“Block Memory Generator”



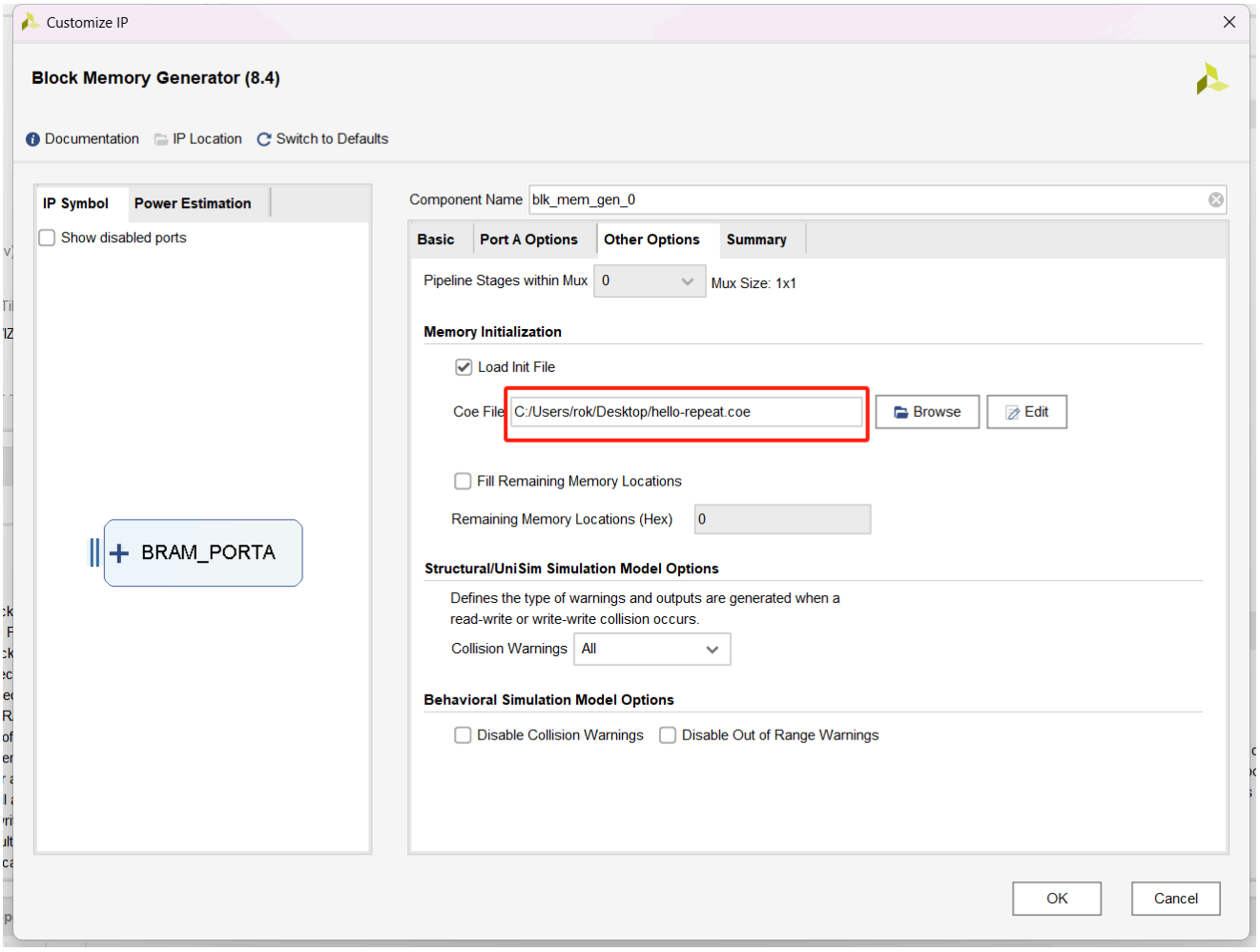
接口类型选择“Native”



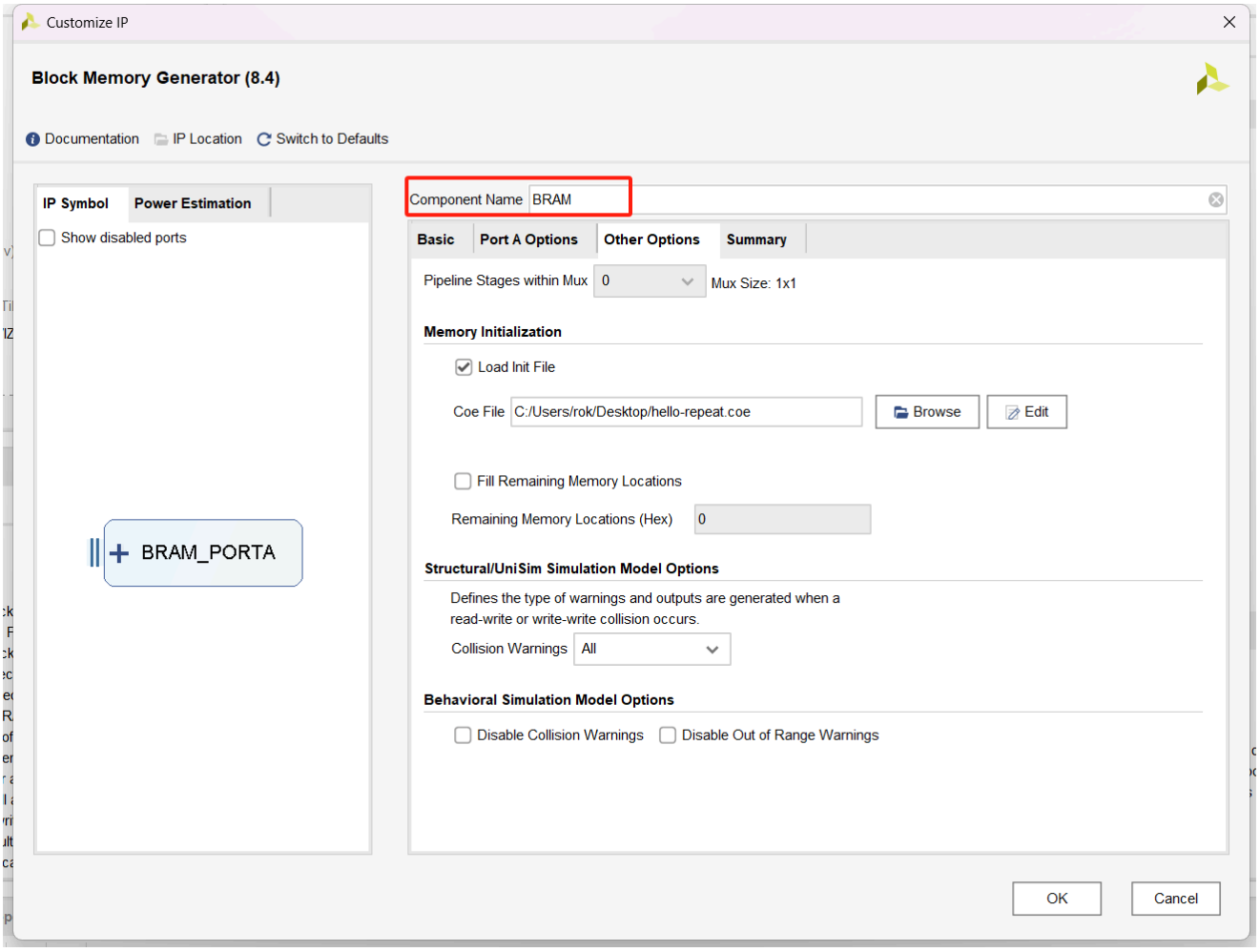
更改Port A位宽和深度，配置操作模式，取消勾选“Primitives Output Register”



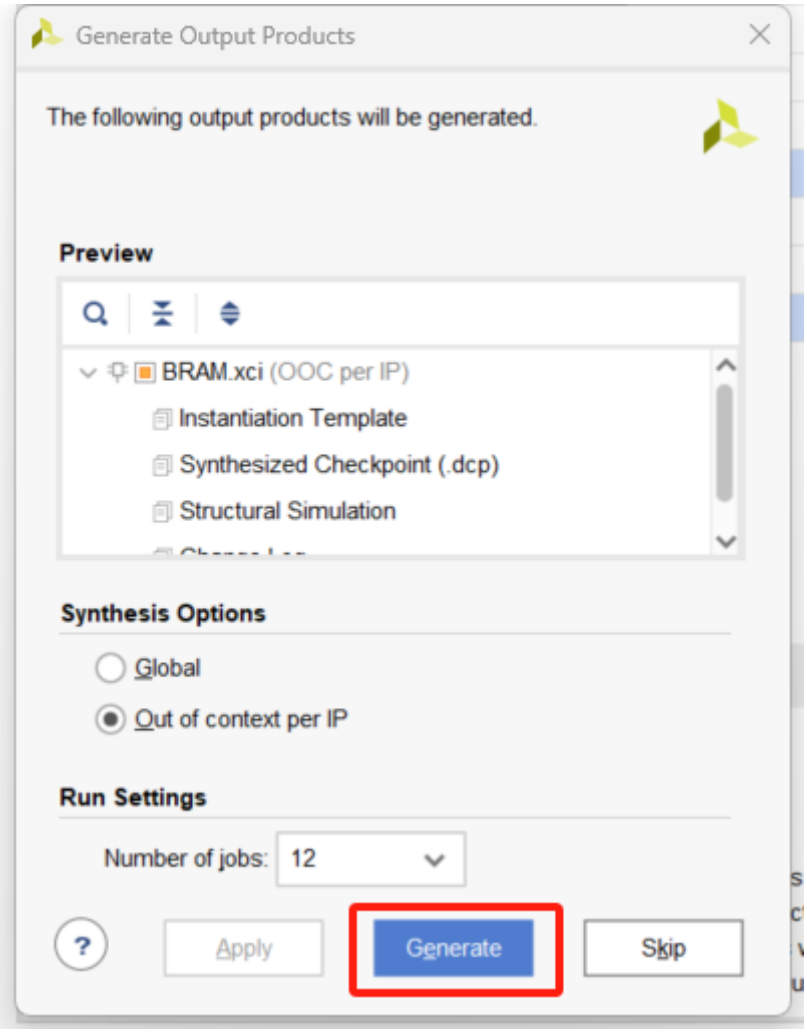
加载coe文件到BRAM中



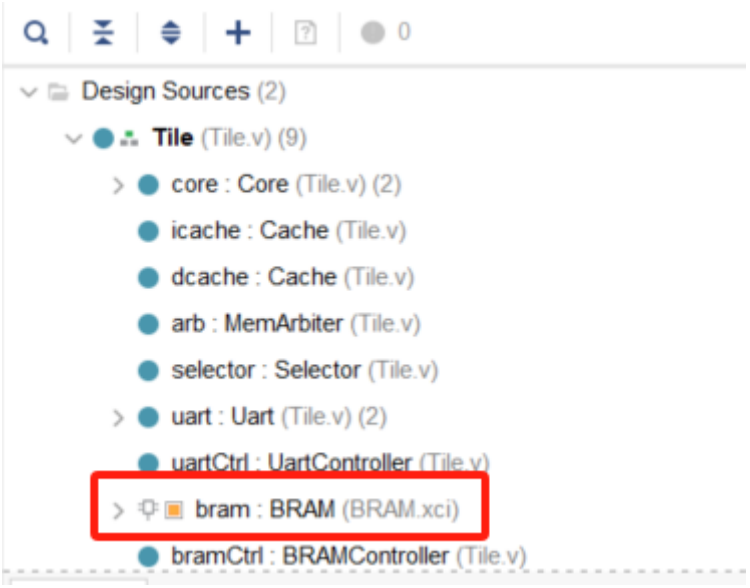
更改设备名称为“BRAM”



点击OK和Generate，生成IP Core的Verilog代码

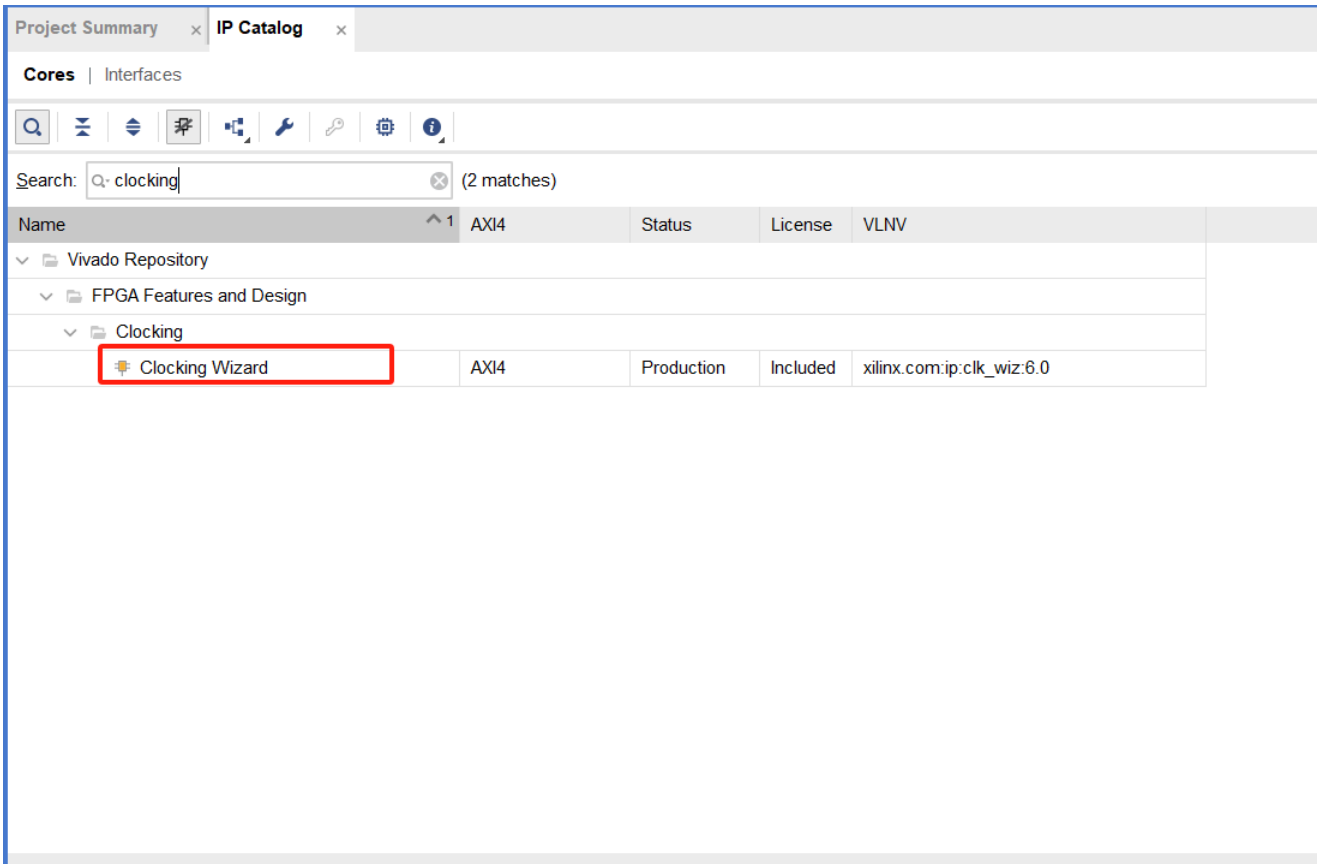

Generate Output Products
The following output products will be generated.
Preview
BRAM.xci (OOC per IP)
Instantiation Template
Synthesized Checkpoint (.dcp)
Structural Simulation
Synthesis Options
Global
Out of context per IP
Run Settings
Number of jobs: 12
Apply
Generate
Skip

完成

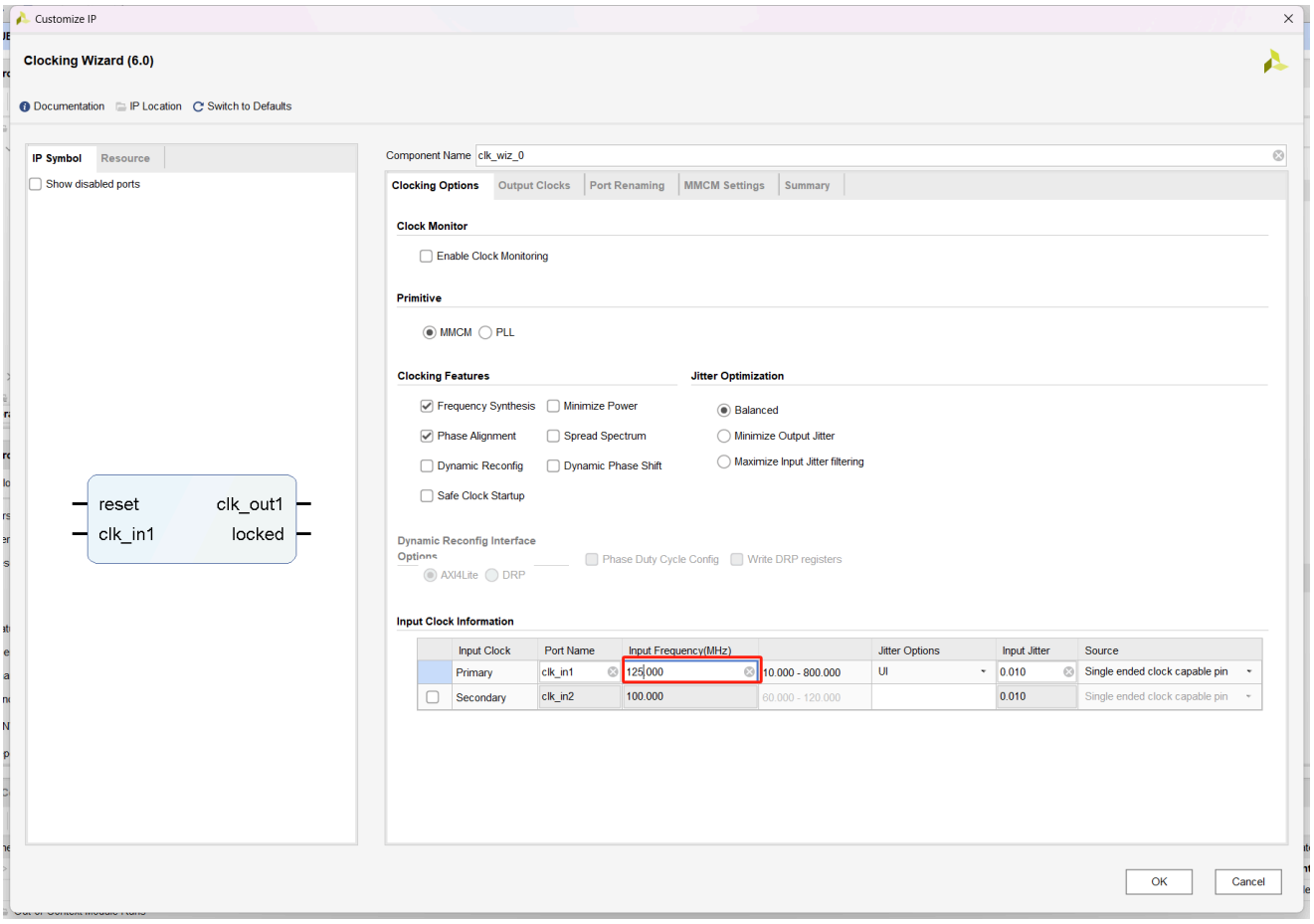

Design Sources (2)
Tile (Tile.v) (9)
core : Core (Tile.v) (2)
icache : Cache (Tile.v)
dcache : Cache (Tile.v)
arb : MemArbiter (Tile.v)
selector : Selector (Tile.v)
uart : Uart (Tile.v) (2)
uartCtrl : UartController (Tile.v)
bram : BRAM (BRAM.xci)
bramCtrl : BRAMController (Tile.v)

添加clocking wizard IP

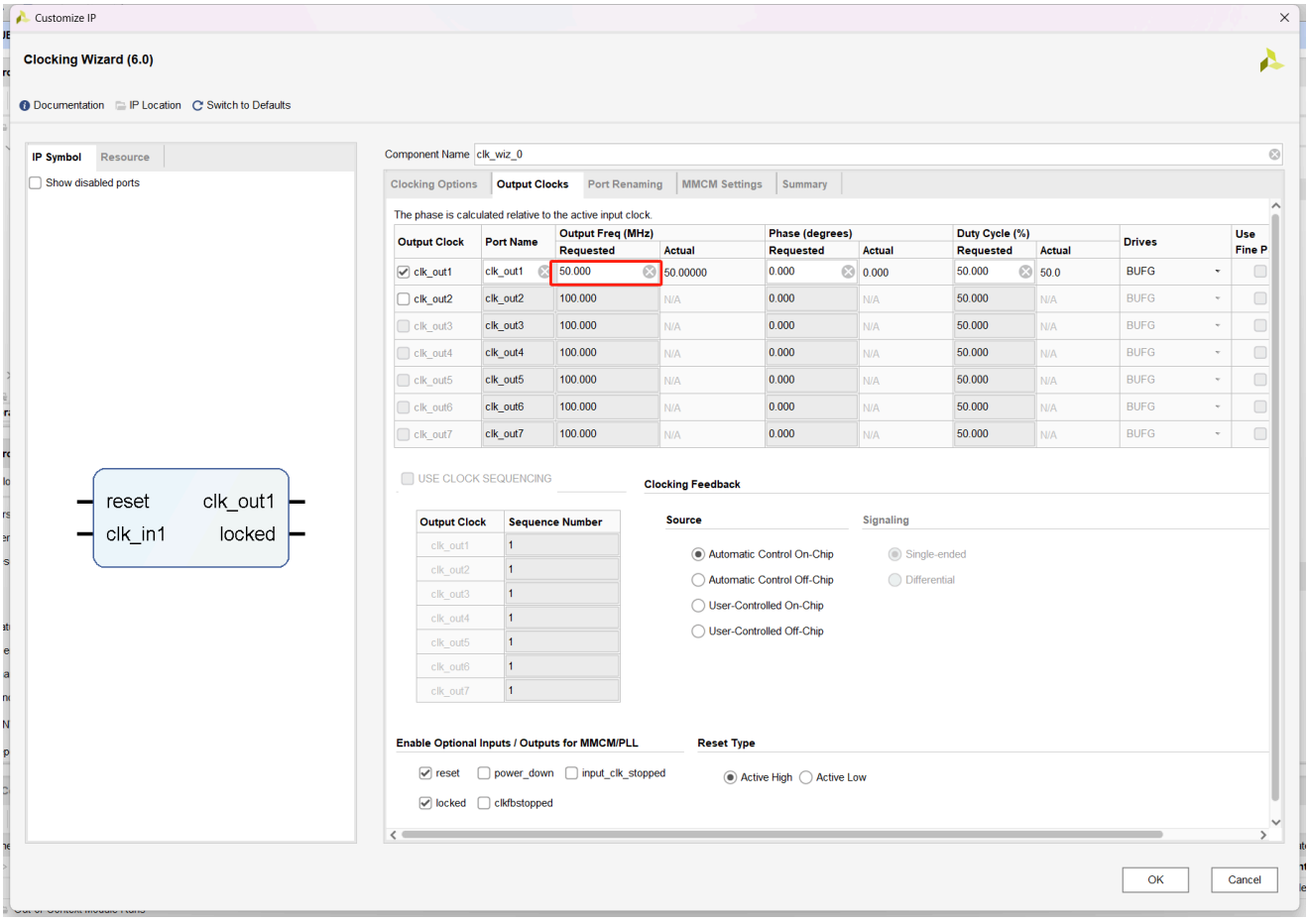
再次搜索ip核，选择clocking wizard



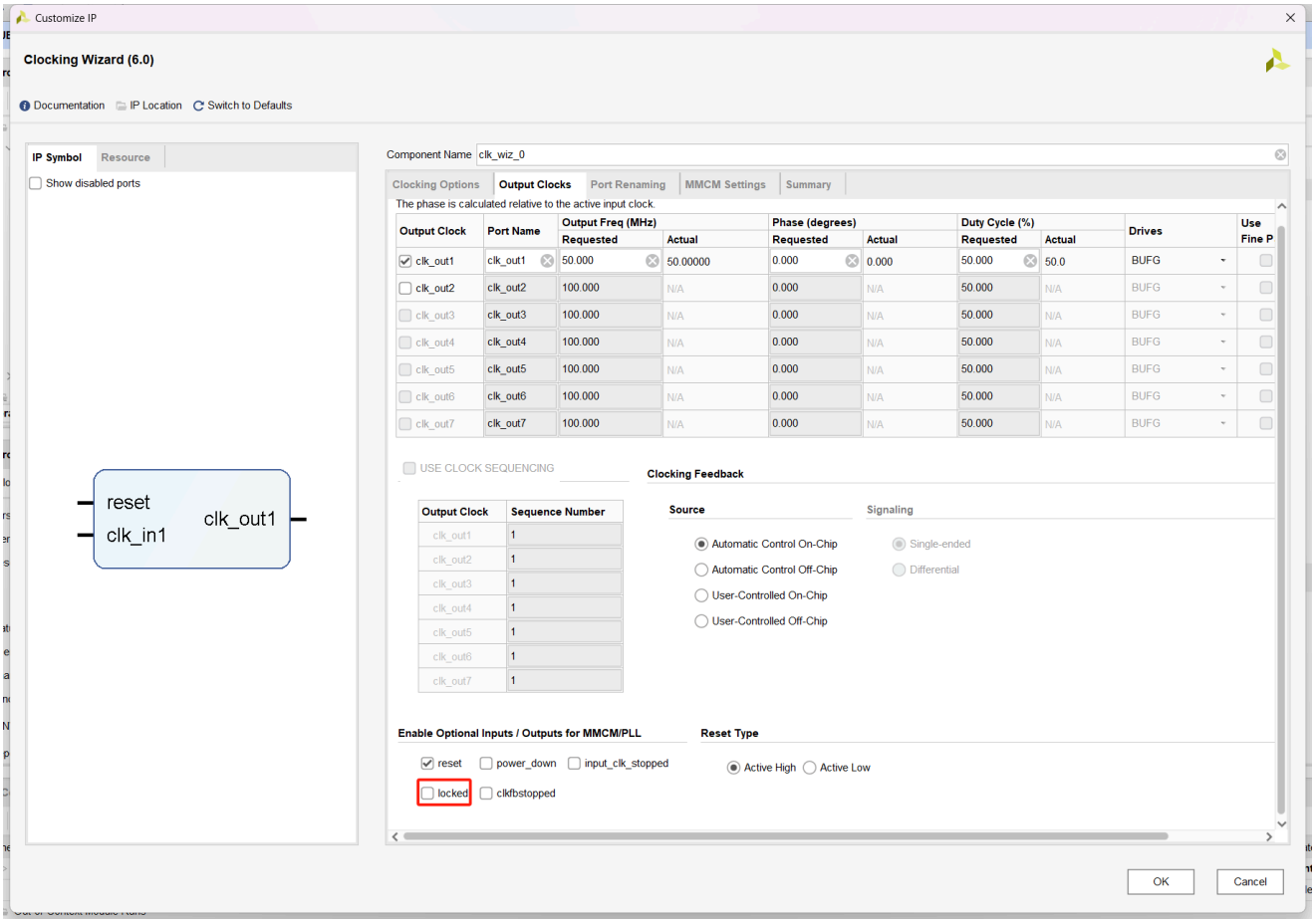
输入频率更改为125MHz


Customize IP
Clocking Wizard (6.0)
Documentation
IP Location
Switch to Defaults
IP Symbol
Resource
Show disabled ports
reset
clk_in1
clk_out1
locked
Component Name
clk_wiz_0
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
Clock Monitor
Enable Clock Monitoring
Primitive
MMCM
PLL
Clocking Features
Frequency Synthesis
Minimize Power
Phase Alignment
Spread Spectrum
Dynamic Reconfig
Dynamic Phase Shift
Safe Clock Startup
Jitter Optimization
Balanced
Minimize Output Jitter
Maximize Input Jitter filtering
Dynamic Reconfig Interface Options
AXI4Lite
DRP
Phase Duty Cycle Config
Write DRP registers
Input Clock Information
Input Clock
Port Name
Input Frequency(MHz)
Jitter Options
Input Jitter
Source
Primary
clk_in1
125.000
10.000 - 800.000
UI
0.010
Single ended clock capable pin
Secondary
clk_in2
100.000
60.000 - 120.000
0.010
Single ended clock capable pin
OK
Cancel

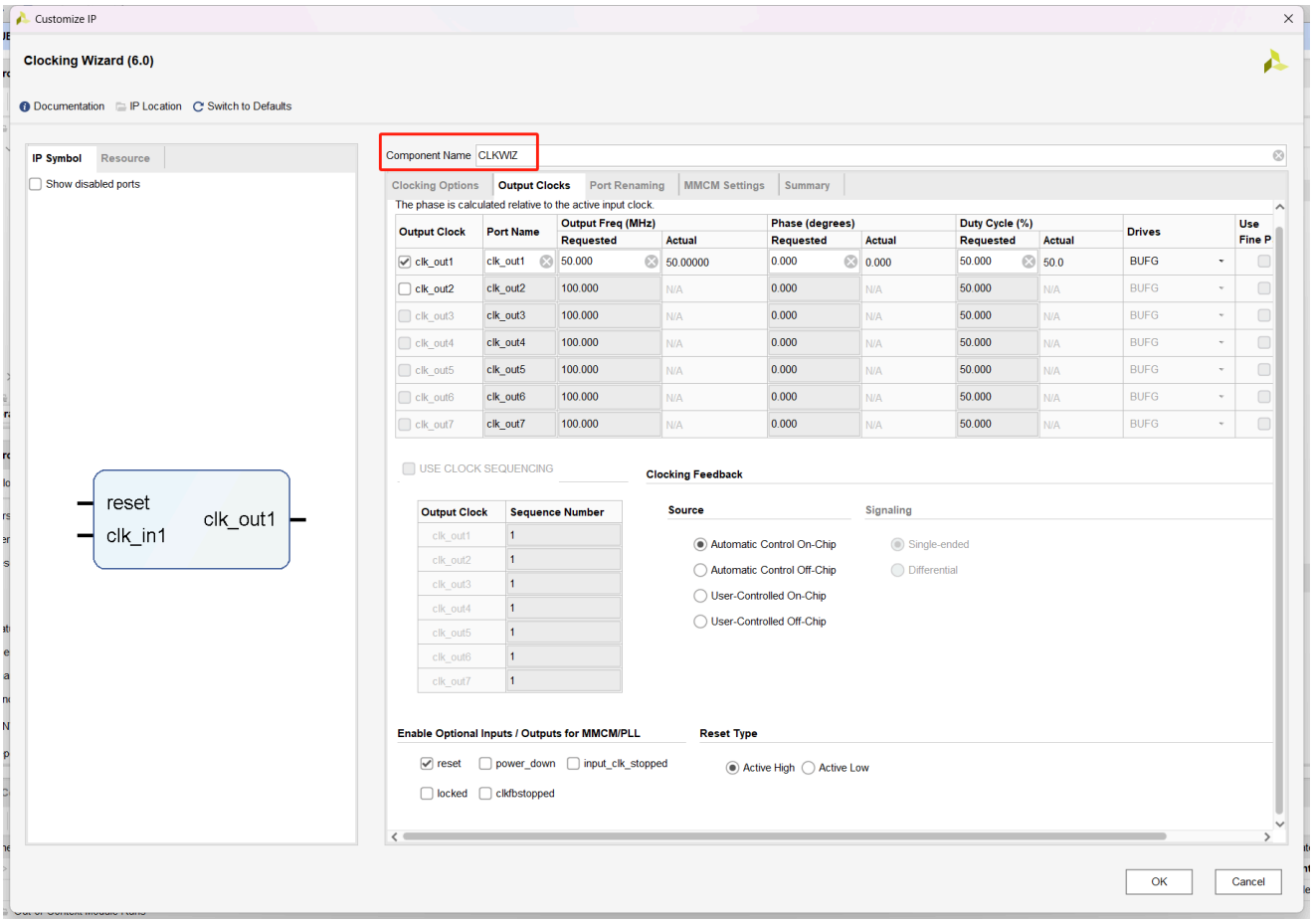
输出更改为50MHz


Customize IP
Clocking Wizard (6.0)
Documentation
IP Location
Switch to Defaults
IP Symbol
Resource
Show disabled ports
reset
clk_in1
clk_out1
locked
Component Name
clk_wiz_0
Clocking Options
Output Clocks
Port Renaming
MMCM Settings
Summary
The phase is calculated relative to the active input clock.
Output Clock
Port Name
Output Freq (MHz)
Requested
Actual
Phase (degrees)
Requested
Actual
Duty Cycle (%)
Requested
Actual
Drives
Use Fine P
clk_out1
clk_out1
50.000
50.00000
0.000
0.000
50.000
50.0
BUFG
clk_out2
clk_out2
100.000
N/A
0.000
N/A
50.000
N/A
BUFG
clk_out3
clk_out3
100.000
N/A
0.000
N/A
50.000
N/A
BUFG
clk_out4
clk_out4
100.000
N/A
0.000
N/A
50.000
N/A
BUFG
clk_out5
clk_out5
100.000
N/A
0.000
N/A
50.000
N/A
BUFG
clk_out6
clk_out6
100.000
N/A
0.000
N/A
50.000
N/A
BUFG
clk_out7
clk_out7
100.000
N/A
0.000
N/A
50.000
N/A
BUFG
USE CLOCK SEQUENCING
Output Clock
Sequence Number
Clocking Feedback
Source
Signaling
Automatic Control On-Chip
Automatic Control Off-Chip
User-Controlled On-Chip
User-Controlled Off-Chip
Single-ended
Differential
Enable Optional Inputs / Outputs for MMCM/PLL
reset
power_down
input_clk_stopped
locked
clkfbstopped
Reset Type
Active High
Active Low
OK
Cancel

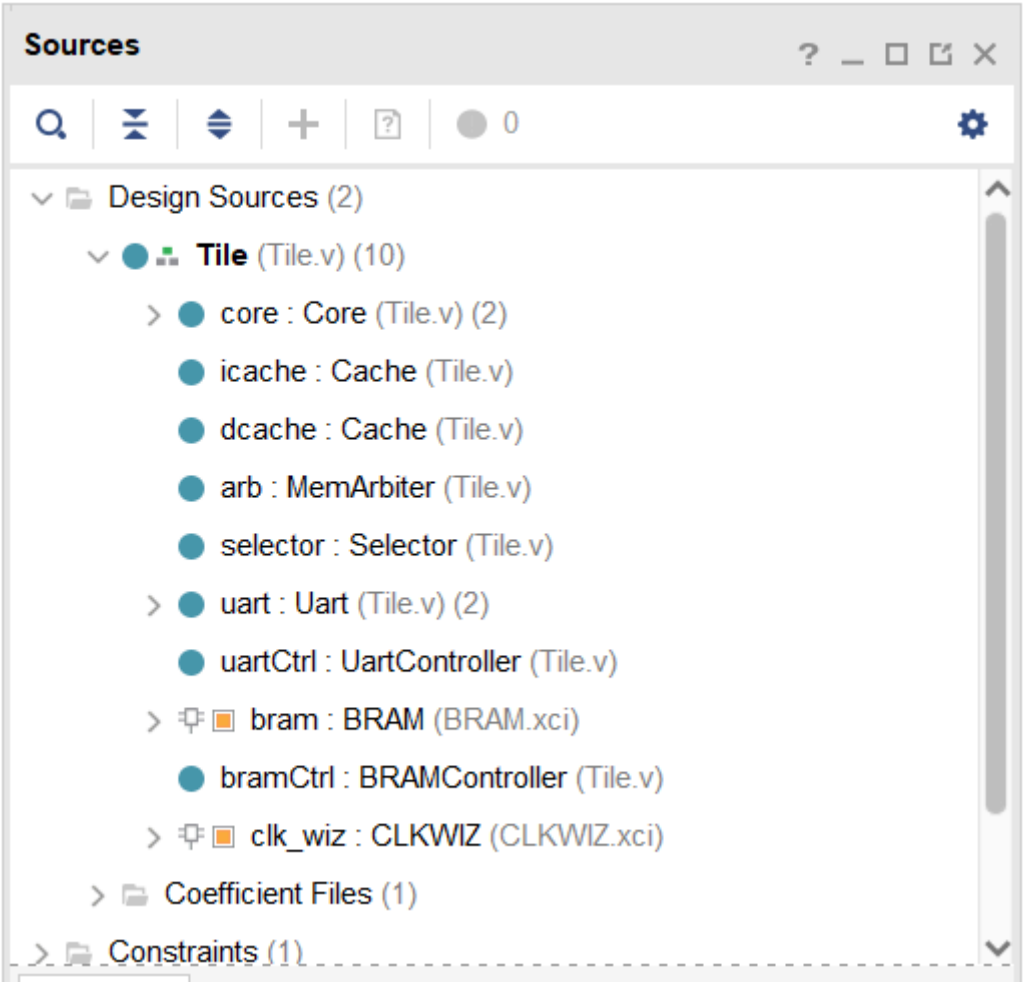
取消勾选“locked”选项



更改IP核名称为“CLKWIZ”

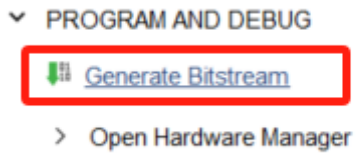


点击“OK”和“generate”完成生成

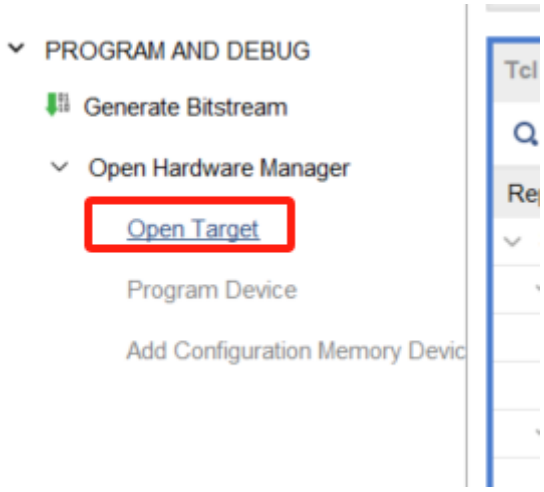


生成BitStream进行烧写

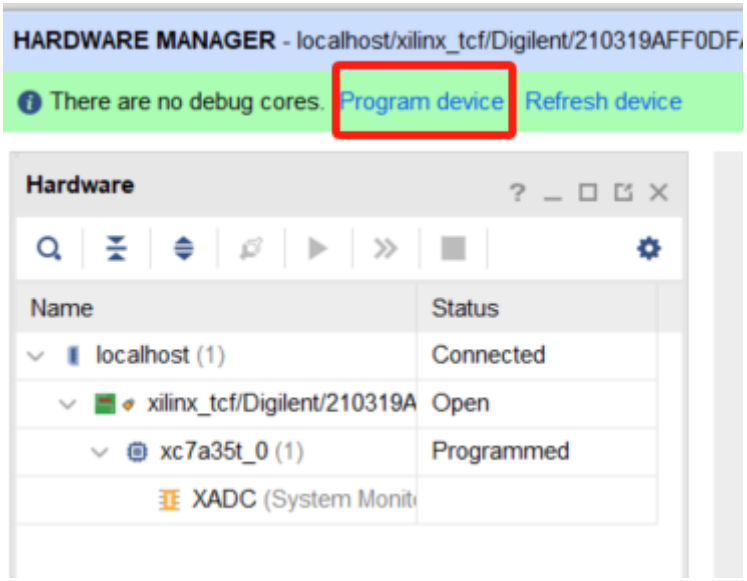
生成比特流



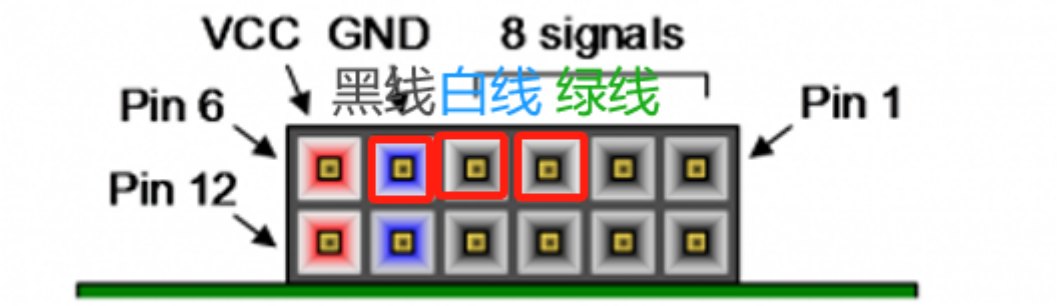
连接设备



烧写比特流

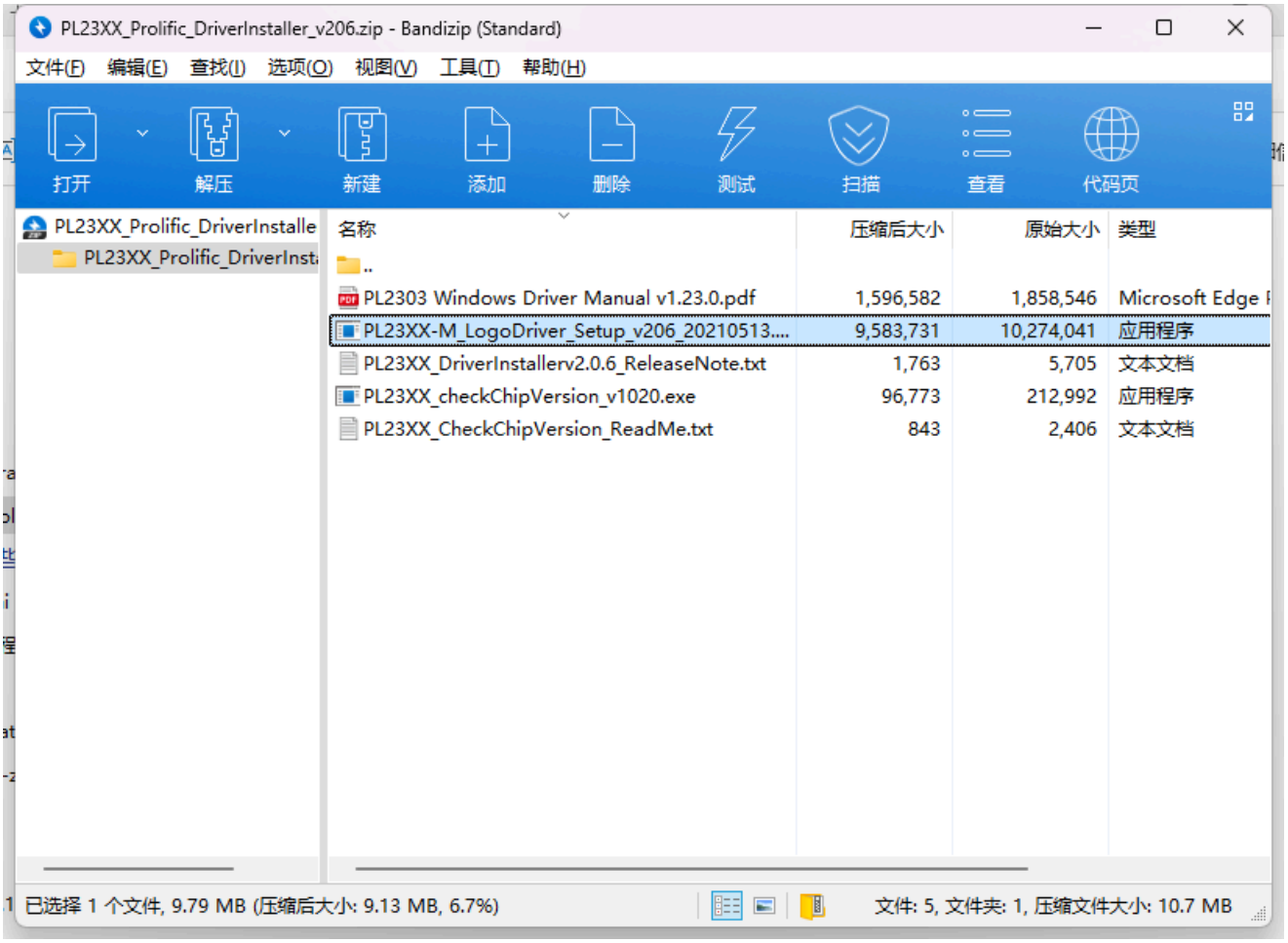


连接IO引脚

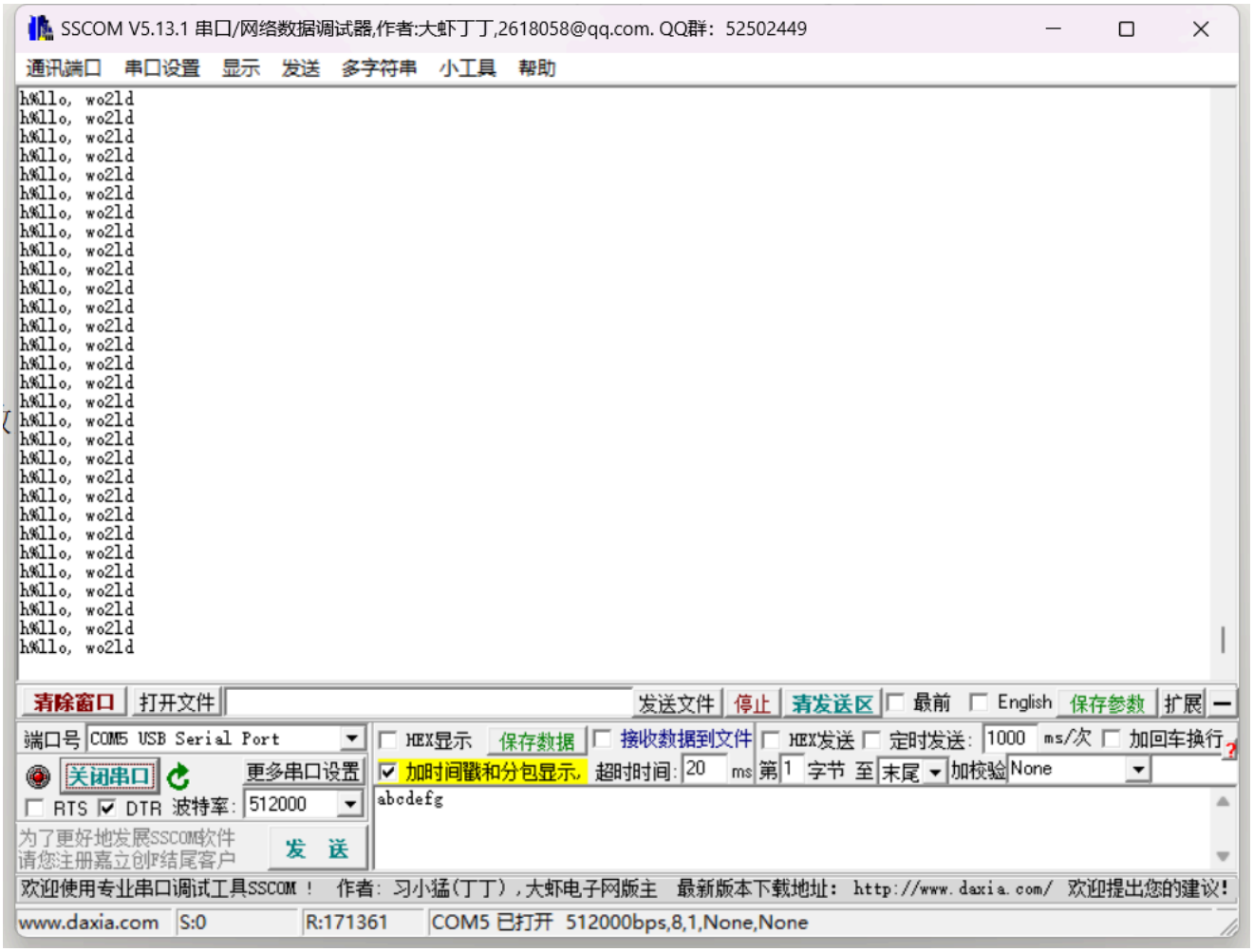


观察结果

安装驱动


PL23XX_Prolific_DriverInstaller_v206.zip - Bandizip (Standard)
文件(F) 编辑(E) 查找(I) 选项(O) 视图(V) 工具(T) 帮助(H)
打开
解压
新建
添加
删除
测试
扫描
查看
代码页
PL23XX_Prolific_DriverInstalle
PL23XX_Prolific_DriverInst
名称
压缩后大小
原始大小
类型
..
PL2303 Windows Driver Manual v1.23.0.pdf 1,596,582 1,858,546 Microsoft Edge
PL23XX-M_LogoDriver_Setup_v206_20210513.... 9,583,731 10,274,041 应用程序
PL23XX_DriverInstallerv2.0.6_ReleaseNote.txt 1,763 5,705 文本文档
PL23XX_checkChipVersion_v1020.exe 96,773 212,992 应用程序
PL23XX_CheckChipVersion_ReadMe.txt 843 2,406 文本文档
已选择 1 个文件, 9.79 MB (压缩后大小: 9.13 MB, 6.7%)
文件: 5, 文件夹: 1, 压缩文件大小: 10.7 MB

查看效果


SSCOM V5.13.1 串口/网络数据调试器,作者:大虾丁丁,2618058@qq.com. QQ群：52502449
通讯端口 串口设置 显示 发送 多字符串 小工具 帮助
h&llo, wo2ld
清除窗口 打开文件 发送文件 停止 清发送区 最前 English 保存参数 扩展
端口号 COM5 USB Serial Port
HEX显示 保存数据 接收数据到文件 HEX发送 定时发送: 1000 ms/次 加回车换行
关闭串口 更多串口设置
加时间戳和分包显示, 超时时间: 20 ms 第 1 字节 至 末尾 加校验 None
RTS DTR 波特率: 512000
abcdefg
为了更好地发展SSCOM软件
请您注册嘉立创P结尾客户
发 送
欢迎使用专业串口调试工具SSCOM ！ 作者：习小猛(丁丁)，大虾电子网版主 最新版本下载地址： http://www.daxia.com/ 欢迎提出您的建议!
www.daxia.com S:0 R:171361 COM5 已打开 512000bps,8,1,None,None