SystemVerilog Language Construct	Design Compiler	Synplify-Pro
`begin_keyword**, **`end_keyword compatibility directives	yes	no
Package import before module port list	yes	no
Parameterized tasks and functions, using parameterized static classes	yes	no
Enumerated type methods (**.next**, **.prev**, etc.)	yes	no
`__FILE__** and **`__LINE__ debug macros	yes	no
priority and **unique** modifier to **if**...**else**	yes	ignored
Cross module references (XMRs)[1]	no	yes
real data type	no	yes
Increment or decrement operator on right-hand side of assignment statement	no	yes
Nets declared from **typedef struct** definitions	no	yes
Extern module declarations	no	yes
$onehot, **$onehot0**, **$countones**	no	yes
Interface modport expressions	no	yes
Immediate assertions	ignored	yes
let macros	ignored	yes
Checkers	no	ignored
expect statements	no	ignored

[1] The HDL Compiler (DC) reference manual says that cross-module references are supported “if the hierarchical name remains inside the module that contains the name, and each item on the hierarchical path is part of the module containing the reference.” This restriction means that references to interface port contents are legal, but references to the contents of some other module are illegal.