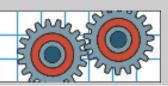
Serial CRC

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Verification IP's

SystemVerilog, Vera, E, SystemC, Verilog





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Serial CRC

Below code is 16-bit CRC-CCITT implementation, with following features

- Width = 16 bits
- Truncated polynomial = 0x1021
- Initial value = 0xFFFF
- Input data is NOT reflected
- Output CRC is NOT reflected
- No XOR is performed on the output CRC

```
// Design Name : serial_crc_ccitt
 3 // File Name : serial crc.v
 4 // Function : CCITT Serial CRC
 5 // Coder : Deepak Kumar Tala
 6 //-----
 7 module serial_crc_ccitt (
 8 clk
 9 reset
10 enable ,
11 init
12 data in ,
13 crc_out
15 //-----Input Ports-----
16 input clk
17 input reset
18 input enable ;
19 input init
20 input data_in ;
21 //-----Output Ports-----
22 output [15:0] crc_out;
23 //-----Internal Variables-----
24 reg [15:0] lfsr;
25 //-----Code Start-----
26 assign crc_out = lfsr;
27 // Logic to CRC Calculation
28 always @ (posedge clk)
29 if (reset) begin
    lfsr <= 16'hFFFF;
31 end else if (enable) begin
    if (init) begin
32
33
      lfsr <= 16'hFFFF;</pre>
   end else begin
34
       lfsr[0] <= data_in ^ lfsr[15];</pre>
35
36
       lfsr[1] <= lfsr[0];
37
       lfsr[2] <= lfsr[1];
       lfsr[3] <= lfsr[2];
38
39
       lfsr[4] <= lfsr[3];
       lfsr[5] <= lfsr[4] ^ data_in ^ lfsr[15];</pre>
40
41
       lfsr[6] <= lfsr[5];
       lfsr[7] <= lfsr[6];
42
43
       lfsr[8] <= lfsr[7];
       lfsr[9] <= lfsr[8];
44
45
       lfsr[10] <= lfsr[9];
46
       lfsr[11] <= lfsr[10];
       lfsr[12] <= lfsr[11] ^ data_in ^ lfsr[15];</pre>
47
48
       lfsr[13] <= lfsr[12];
49
       lfsr[14] <= lfsr[13];
50
       lfsr[15] <= lfsr[14];
51 end
52 end
53
54 endmodule
```