Setup I/O piso.sv

```
1  module piso #(
2    parameter [7:0] DATA_WIDTH = 16
3  ) (
4    input   logic                   clk,
5    input   logic                   rst_n,
6    input   logic                   load_i,
7    input   logic [DATA_WIDTH-1:0]  loaddata_i,
8    output  logic                   serial_o
9  );
10
11 logic [DATA_WIDTH-1:0] data_d, data_q;
12
13 always_comb begin
14   if (load_i)
15     data_d = loaddata_i;
16   else
17     data_d = (data_q >> 1);
18 end
19
20 always_ff @(posedge clk or negedge rst_n) begin
21   if (!rst_n) begin
22     data_q <= '0;
23   end else begin
24     data_q <= data_d;
25   end
26 end
27
28 assign serial_o = data_q[0];
29
30 endmodule
```