Name	Version	Description	clang- 2.0.3	clang- 3.1.5	clang- 4.0.4	clang- 4.0.5	gcc-1.0.7	gcc-2.0.3	gcc-3.1.5	gcc-4.0.4	gcc-4.0.5
а	2.0		N	N	N	N	Υ	Υ	Υ	Υ	Υ
a	2.1	'A' (Atomic Instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
b	1.0	'B' (the collection of the Zba, Zbb, Zbs extensions)	N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
С	2.0	'C' (Compressed Instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
d	2.0		N	N	N	N	Υ	Υ	Υ	Υ	Υ
d	2.2	'D' (Double-Precision Floating-Point)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
e	1.9		N	N	N	N	Υ	Υ	Υ	Υ	Υ
e	2.0	Implements RV{32,64}E (provides 16 rather than 3	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
f	2.0		N	N	N	N	Υ	Υ	Υ	Υ	Υ
f	2.2	'F' (Single-Precision Floating-Point)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
h	1.0	'H' (Hypervisor)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
i	2.0		N	N	N	N	Υ	Υ	Υ	Υ	Υ
i	2.1	'I' (Base Integer Instruction Set)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
m	2.0	'M' (Integer Multiplication and Division)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
р	0.15		N	N	N	N	N	N	N	N	Υ
sdext	1.0	'Sdext' (External Debugging Extension)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
sdtrig	1.0	'Sdtrig' (Debugging Triggers)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
sha	1.0	'Sha' (Augmented Hypervisor)	N	N	Υ	Υ	N	N	N	N	N
shcounterenw	1.0	'Shcounterenw' (Support writeable hcounteren en	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
shgatpa	1.0	'Sgatpa' (SvNNx4 mode supported for all modes su	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
shtvala	1.0	'Shtvala' (htval provides all needed values)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
shvsatpa	1.0	'Svsatpa' (vsatp supports all modes supported by s	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
shvstvala	1.0	'Shvstvala' (vstval provides all needed values)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
shvstvecd	1.0	'Shvstvecd' (vstvec supports Direct mode)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
smaia	1.0	'Smaia' (Advanced Interrupt Architecture Machine	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
smcdeleg	1.0		N	N	Υ	Υ	N	N	N	N	N
smcsrind	1.0	'Smcsrind' (Indirect CSR Access Machine Level)	N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
smctr	1.0	'Smctr' (Control Transfer Records Machine Level)	N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
smdbltrp	1.0	'Smdbltrp' (Double Trap Machine Level)	N	N	Υ	Υ	N	N	N	N	Υ
smepmp	1.0	'Smepmp' (Enhanced Physical Memory Protection	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
smmpm	0.8	'Smmpm' (Machine-level Pointer Masking for M-m		N	N	N	Υ	Υ	N	N	N
smmpm	1.0	'Smmpm' (Machine-level Pointer Masking for M-m		Υ	Υ	Υ	N	N	Υ	Υ	Υ
smnpm	0.8	'Smnpm' (Machine-level Pointer Masking for next		N	N	N	Υ	Υ	N	N	N
smnpm	1.0	'Smnpm' (Machine-level Pointer Masking for next		Υ	Υ	Υ	N	N	Υ	Υ	Υ
smrnmi	0.5	_	Υ	N	N	N	N	Υ	N	N	N

smrnmi	1.0	'Smrnmi' (Resumable Non-Maskable Interrupts)	N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
smstateen	1.0	'Smstateen' (Machine-mode view of the state-ena	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
smwg	0.3	'Smwg' (The Smwg extension adds the mlwid CSR,	, Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
smwgd	0.3	'Smwgd' (The Smwgd extension adds the mwidde	ΙY	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
SS	1.12	'Ss' (Supervisor Architecture)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
SS	1.13	'Ss' (Supervisor Architecture)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
ssaia	1.0	'Ssaia' (Advanced Interrupt Architecture Superviso	Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
ssccfg	1.0	'Ssccfg' (Counter Configuration Supervisor Level)	N	N	Υ	Υ	N	N	N	N	N
ssccptr	1.0	'Ssccptr' (Main memory supports page table reads	s <b>Y</b>	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
sscofpmf	1.0	'Sscofpmf' (Count Overflow and Mode-Based Filte	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
sscounterenw	1.0	'Sscounterenw' (Support writeable scounteren en	ίΥ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
sscsrind	1.0	'Sscsrind' (Indirect CSR Access Supervisor Level)	N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
ssctr	1.0	'Ssctr' (Control Transfer Records Supervisor Level)	N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
ssdbltrp	1.0	'Ssdbltrp' (Double Trap Supervisor Level)	N	N	Υ	Υ	N	N	N	N	Υ
ssnpm	0.8	'Ssnpm' (Supervisor-level Pointer Masking for nex	tΥ	N	N	N	Y	Υ	N	N	N
ssnpm	1.0	'Ssnpm' (Supervisor-level Pointer Masking for nex	1 N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
sspm	0.8	'Sspm' (Indicates Supervisor-mode Pointer Maskir	۱Y	N	N	N	Υ	Υ	N	N	N
sspm	1.0	'Sspm' (Indicates Supervisor-mode Pointer Maskir	n N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
sspmp	0.9		N	N	N	N	N	N	N	N	Υ
ssqosid	1.0	'Ssqosid' (Quality-of-Service (QoS) Identifiers)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
ssstateen	1.0	'Ssstateen' (Supervisor-mode view of the state-en	ίΥ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
ssstrict	1.0	'Ssstrict' (No non-conforming extensions are preso	ŧΥ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
sstc	1.0	'Sstc' (Supervisor-mode timer interrupts)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
sstvala	1.0	'Sstvala' (stval provides all needed values)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
sstvecd	1.0	'Sstvecd' (stvec supports Direct mode)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
ssu64xl	1.0	'Ssu64xI' (UXLEN=64 supported)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
sswg	0.3	'Sswg' (The Sswg extension adds the [H]S-mode re	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
supm	0.8	'Supm' (Indicates User-mode Pointer Masking)	Υ	N	N	N	Υ	Υ	N	N	N
supm	1.0	'Supm' (Indicates User-mode Pointer Masking)	N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
sv39	1.12		N	N	N	N	Υ	Υ	Υ	Υ	Υ
sv48	1.12		N	N	N	N	Υ	Υ	Υ	Υ	Υ
sv57	1.12		N	N	N	N	Υ	Υ	Υ	Υ	Υ
svade	1.0	'Svade' (Raise exceptions on improper A/D bits)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
svadu	1.0	'Svadu' (Hardware A/D updates)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
svbare	1.0	'Svbare' \$(satp mode Bare supported)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
svinval	1.0	'Svinval' (Fine-Grained Address-Translation Cache	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
svnapot	1.0	'Svnapot' (NAPOT Translation Contiguity)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ

svpbmt	1.0	'Svpbmt' (Page-Based Memory Types)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
svptead	1.0		N	N	N	N	Υ	Υ	Υ	Υ	Υ
svukte	0.4	'Svukte' (Address-Independent Latency of User-M	(N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
svvptc	1.0	'Svvptc' (Obviating Memory-Management Instruc	t N	N	Υ	Υ	N	N	N	N	Y
V	0.10		N	N	N	N	Υ	Υ	Υ	Υ	Υ
V	1.0	'V' (Vector Extension for Application Processors)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xcvalu	1.0	'XCValu' (CORE-V ALU Operations)	Υ	Υ	Υ	Υ	N	N	N	Y	Υ
xcvbi	1.0	'XCVbi' (CORE-V Immediate Branching)	Υ	Υ	Υ	Υ	N	N	N	Y	Υ
xcvbitmanip	1.0	'XCVbitmanip' (CORE-V Bit Manipulation)	Υ	Υ	Υ	Υ	N	N	N	N	N
xcvelw	1.0	'XCVelw' (CORE-V Event Load Word)	Υ	Υ	Υ	Υ	N	N	N	Υ	Υ
xcvmac	1.0	'XCVmac' (CORE-V Multiply-Accumulate)	Υ	Υ	Υ	Υ	N	N	N	Υ	Υ
xcvmem	1.0	'XCVmem' (CORE-V Post-incrementing Load & Sto	ıΥ	Υ	Υ	Υ	N	N	N	N	N
xcvsimd	1.0	'XCVsimd' (CORE-V SIMD ALU)	Υ	Υ	Υ	Υ	N	N	N	Y	Υ
xqcia	0.2	'Xqcia' (Qualcomm uC Arithmetic Extension)	N	N	Υ	Υ	N	N	N	N	N
xqciac	0.2	'Xqciac' (Qualcomm uC Load-Store Address Calcul	a N	N	Υ	Υ	N	N	N	N	N
xqcicli	0.2	'Xqcicli' (Qualcomm uC Conditional Load Immedia	ı N	N	Υ	Υ	N	N	N	N	N
xqcicm	0.2	'Xqcicm' (Qualcomm uC Conditional Move Extens	i N	N	Υ	Υ	N	N	N	N	N
xqcics	0.2	'Xqcics' (Qualcomm uC Conditional Select Extension	c N	N	Υ	Υ	N	N	N	N	N
xqcicsr	0.2	'Xqcicsr' (Qualcomm uC CSR Extension)	N	N	Υ	Υ	N	N	N	N	N
xqciint	0.2	'Xqciint' (Qualcomm uC Interrupts Extension)	N	N	Υ	Υ	N	N	N	N	N
xqcilo	0.2	'Xqcilo' (Qualcomm uC Large Offset Load Store Ex	t N	N	Υ	Υ	N	N	N	N	N
xqcilsm	0.2	'Xqcilsm' (Qualcomm uC Load Store Multiple Exte	r N	N	Υ	Υ	N	N	N	N	N
xqcisls	0.2	'Xqcisls' (Qualcomm uC Scaled Load Store Extension	c N	N	Υ	Υ	N	N	N	N	N
xsfcease	0.1	'XSfcease' (SiFive sf.cease Instruction)	N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfcease	1.0	'XSfcease' (SiFive sf.cease Instruction)	N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfmm128t	0.6	'XSfmm128t' TE=128 configuration	N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfmm16t	0.6	'XSfmm16t' TE=16 configuration	N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfmm32a	0.6	'XSfmm32a' (TEW=32-bit accumulation) operands	N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfmm32a16f	0.6	'XSfmm32a16f' (TEW=32-bit accumulation) opera	r N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfmm32a32f	0.6	'XSfmm32a32f' (TEW=32-bit accumulation) opera	r N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfmm32a4i	0.6	'XSfmm32a4i' (TEW=32-bit accumulation) operan	c N	Υ	N	N	N	N	Υ	N	N
xsfmm32a8f	0.6	'XSfmm32a8f' (TEW=32-bit accumulation) operan	(N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfmm32a8i	0.6	'XSfmm32a8i' (TEW=32-bit accumulation) operan	c N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfmm32ea	0.6	'XSfmm32ea' (TEW=32-bit accumulation) instruct		Υ	N	N	N	N	Υ	N	N
xsfmm32t	0.6	'XSfmm32t' TE=32 configuration	N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfmm64a64f	0.6	'XSfmm64a64f' (TEW=64-bit accumulation) opera	r N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfmm64t	0.6	'XSfmm64t' TE=64 configuration	N	Υ	Υ	Υ	N	N	Y	Υ	Υ

xsfmmbase	0.6	'XSfmmbase' All non arithmetic instructions for all N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfpgflushdlone	0.1	'XSfpgflushdlone' (Cache Flush/Power Down InstruY	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xsfpmpmt	0.1	'Xsfpmpmt' (SiFive PMP-based Memory Types Extention	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfsci	1.0	'XSfsci' (SiFive Custom Scalar Coprocessor Interfac N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfvcp	0.1	N	N	N	N	Υ	Υ	Υ	Υ	Υ
xsfvcp	1.0	'XSfvcp' (SiFive Custom Vector Coprocessor Interfa Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xsfvfbfa	0.1	'XSfvfbfa' (SiFive custom additional BF16 vector cc N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfvfbfexp16e	0.1	'Xsfvfbfexp16e' (SiFive Vector Floating-Point Expor	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfvfexp16e	0.1	'Xsfvfexp16e' (SiFive Vector Floating-Point Expone N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfvfexp32e	0.1	'Xsfvfexp32e' (SiFive Vector Floating-Point Expone N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfvfexpa	0.2	'Xsfvfexpa' (SiFive Vector Floating-Point Exponenti <mark> N</mark>	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfvfexpa64e	0.2	'Xsfvfexpa64e' (SiFive Vector Floating-Point Expon N	Υ	Υ	Υ	N	N	Υ	Υ	Υ
xsfvfhbfmin	0.1	'Xsfvfhbfmin' (SiFive custom minimal BF16 vector :Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xsfvfnrclipxfqf	0.1	'XSfvfnrclipxfqf' (SiFive FP32-to-int8 Ranged Clip Ir Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xsfvfnrclipxfqf	1.0	'XSfvfnrclipxfqf' (SiFive FP32-to-int8 Ranged Clip Ir Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xsfvfwmaccqqq	0.1	'XSfvfwmaccqqq' (SiFive Matrix Multiply Accumula Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xsfvfwmaccqqq	1.0	'XSfvfwmaccqqq' (SiFive Matrix Multiply Accumula Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xsfvqdotq	0.1	'Xsfvqdotq' (SiFive Vector Quad-Widening 4D Dot Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xsfvqmaccdod	0.1	'XSfvqmaccdod' (SiFive Int8 Matrix Multiplication Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xsfvqmaccdod	1.0	'XSfvqmaccdod' (SiFive Int8 Matrix Multiplication Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xsfvqmaccqoq	0.1	'XSfvqmaccqoq' (SiFive Int8 Matrix Multiplication   Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xsfvqmaccqoq	1.0	'XSfvqmaccqoq' (SiFive Int8 Matrix Multiplication   Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xsifivecdiscarddlo	or 0.1	'XSiFivecdiscarddlone' (SiFive sf.cdiscard.d.l1 Instr <mark>N</mark>	Υ	Υ	Υ	N	N	N	Υ	Υ
xsifivecdiscarddlo	or 1.0	'XSiFivecdiscarddlone' (SiFive sf.cdiscard.d.l1 Instr <mark>N</mark>	Υ	Υ	Υ	N	N	N	N	N
xsifivecdiscarddlo	or 'XSiFived	cd (Cache Flush/Power Down Instructions)	N	N	N	N	N	N	N	N
xsifivecflushdlone	e 0.1	'XSiFivecflushdlone' (Cache Flush/Power Down Ins Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xsifivecflushdlone	e 1.0	'XSiFivecflushdlone' (SiFive sf.cflush.d.l1 Instructio N	Υ	Υ	Υ	N	N	N	N	N
xtheadba	1.0	'xtheadba' (T-Head address calculation instruction Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xtheadbb	1.0	'xtheadbb' (T-Head basic bit-manipulation instruct Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xtheadbs	1.0	'xtheadbs' (T-Head single-bit instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xtheadcmo	1.0	'xtheadcmo' (T-Head cache management instructi Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xtheadcondmov	1.0	'xtheadcondmov' (T-Head conditional move instru Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xtheadfmemidx	1.0	'xtheadfmemidx' (T-Head FP Indexed Memory Ope Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xtheadfmv	1.0	N	N	N	N	Υ	Υ	Υ	Υ	Υ
xtheadint	1.0	N	N	N	N	Υ	Υ	Υ	Υ	Υ
xtheadmac	1.0	'xtheadmac' (T-Head Multiply-Accumulate Instruc	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xtheadmemidx	1.0	'xtheadmemidx' (T-Head Indexed Memory Operat Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ

xtheadmempair	1.0	'xtheadmempair' (T-Head two-GPR Memory Opera	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xtheadsync	1.0	'xtheadsync' (T-Head multicore synchronization in	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
xtheadvdot	1.0	'xtheadvdot' (T-Head Vector Extensions for Dot)	Υ	Υ	Υ	Υ	N	N	N	N	N
xtheadvector	1.0		N	N	N	N	N	N	N	Υ	Υ
xventanacondops	1.0	'XVentanaCondOps' (Ventana Conditional Ops)	Υ	Υ	Υ	Υ	N	N	N	Υ	Υ
xwchc	2.2	'Xwchc' (WCH/QingKe additional compressed opco	N	N	Υ	Υ	N	N	N	N	N
za128rs	1.0	'Za128rs' (Reservation Set Size of at Most 128 Byte	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
za64rs	1.0	'Za64rs' (Reservation Set Size of at Most 64 Bytes)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zaamo	0.2	'Zaamo' (Atomic Memory Operations)	Υ	Υ	N	N	N	N	N	N	N
zaamo	1.0	'Zaamo' (Atomic Memory Operations)	N	N	Υ	Υ	N	N	Υ	Υ	Υ
zabha	1.0	'Zabha' (Byte and Halfword Atomic Memory Opera	Υ	Υ	Υ	Υ	N	N	N	N	N
zacas	1.0	'Zacas' (Atomic Compare-And-Swap Instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zalasr	0.1	'Zalasr' (Load-Acquire and Store-Release Instruction	Υ	Υ	Υ	Υ	N	N	N	N	N
zalasr	1.0		N	N	N	N	N	N	N	Υ	Υ
zalrsc	0.2	'Zalrsc' (Load-Reserved/Store-Conditional)	Υ	Υ	N	N	N	N	N	N	N
zalrsc	1.0	'Zalrsc' (Load-Reserved/Store-Conditional)	N	N	Υ	Υ	N	N	Υ	Υ	Υ
zama16b	1.0	'Zama16b' (Atomic 16-byte misaligned loads, store	Υ	Υ	Υ	Υ	N	Υ	Υ	Υ	Υ
zawrs	1.0	'Zawrs' (Wait on Reservation Set)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zba	0.93		N	N	N	N	Υ	Υ	Υ	Υ	Υ
zba	1.0	'Zba' (Address Generation Instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zbb	0.93		N	N	N	N	Υ	Υ	Υ	Υ	Υ
zbb	1.0	'Zbb' (Basic Bit-Manipulation)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zbc	1.0	'Zbc' (Carry-Less Multiplication)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zbkb	1.0	'Zbkb' (Bitmanip instructions for Cryptography)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zbkc	1.0	'Zbkc' (Carry-less multiply instructions for Cryptog	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zbkx	1.0	'Zbkx' (Crossbar permutation instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zbs	1.0	'Zbs' (Single-Bit Instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zca	1.0	'Zca' (part of the C extension, excluding compresse	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zcb	1.0	'Zcb' (Compressed basic bit manipulation instructi	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zcd	1.0	'Zcd' (Compressed Double-Precision Floating-Point	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zce	1.0	'Zce' (Compressed extensions for microcontrollers	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zcf	1.0	'Zcf' (Compressed Single-Precision Floating-Point I	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zclsd	1.0		N	N	N	N	N	N	N	Υ	Υ
zcmop	1.0	'Zcmop' (Compressed May-Be-Operations)	Υ	Υ	Υ	Υ	N	Υ	Υ	Υ	Υ
zcmp	1.0	'Zcmp' (sequenced instuctions for code-size reduc	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zcmt	1.0	'Zcmt' (table jump instuctions for code-size reduct	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zdinx	1.0	'Zdinx' (Double in Integer)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ

zfa	0.1		N	N	N	N	Υ	N	N	N	N
zfa	0.2		N	N	N	N	Υ	Υ	Υ	Υ	Υ
zfa	1.0	'Zfa' (Additional Floating-Point)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zfbfmin	0.8		N	N	N	N	Υ	Υ	Υ	Υ	Υ
zfbfmin	1.0	'Zfbfmin' (Scalar BF16 Converts)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zfh	1.0	'Zfh' (Half-Precision Floating-Point)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zfhmin	1.0	'Zfhmin' (Half-Precision Floating-Point Minimal)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zfinx	1.0	'Zfinx' (Float in Integer)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zhinx	1.0	'Zhinx' (Half Float in Integer)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zhinxmin	1.0	'Zhinxmin' (Half Float in Integer Minimal)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zibi	0.1	'Zibi' (Branch with Immediate)	N	N	Υ	Υ	N	N	N	N	Υ
zic64b	1.0	'Zic64b' (Cache Block Size Is 64 Bytes)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zicbom	1.0	'Zicbom' (Cache-Block Management Instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zicbop	1.0	'Zicbop' (Cache-Block Prefetch Instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zicboz	1.0	'Zicboz' (Cache-Block Zero Instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
ziccamoa	1.0	'Ziccamoa' (Main Memory Supports All Atomics in	ı Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
ziccif	1.0	'Ziccif' (Main Memory Supports Instruction Fetch	١Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zicclsm	1.0	'Zicclsm' (Main Memory Supports Misaligned Load	c Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
ziccrse	1.0	'Ziccrse' (Main Memory Supports Forward Progre	s <b>Y</b>	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zicfilp	0.2		N	N	N	N	Υ	N	N	N	N
zicfilp	0.4	'Zicfilp' (Landing pad)	Υ	N	N	N	N	N	N	N	N
zicfilp	1.0	'Zicfilp' (Landing pad)	N	Υ	Υ	Υ	N	Υ	Υ	Υ	Υ
zicfiss	0.2		N	N	N	N	Y	N	N	N	N
zicfiss	0.4	'Zicfiss' (Shadow stack)	Υ	N	N	N	N	N	N	N	N
zicfiss	1.0	'Zicfiss' (Shadow stack)	N	Y	Υ	Υ	N	Υ	Υ	Υ	Υ
zicntr	1.0		N	N	N	N	Y	Υ	Υ	N	N
zicntr	2.0	'Zicntr' (Base Counters and Timers)	Υ	Υ	Υ	Υ	N	Υ	Υ	Υ	Υ
zicond	1.0	'Zicond' (Integer Conditional Operations)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zicsr	2.0	'zicsr' (CSRs)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zifencei	2.0	'Zifencei' (fence.i)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zihintntl	1.0	'Zihintntl' (Non-Temporal Locality Hints)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zihintpause	1.0		N	N	N	N	Υ	Υ	Υ	N	N
zihintpause	2.0	'Zihintpause' (Pause Hint)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zihpm	1.0		N	N	N	N	Υ	Υ	Υ	N	N
zihpm	2.0	'Zihpm' (Hardware Performance Counters)	Υ	Υ	Υ	Υ	N	Υ	Υ	Υ	Υ
zilsd	1.0		N	N	N	N	N	N	N	Υ	Υ
zimop	1.0	'Zimop' (May-Be-Operations)	Υ	Υ	Υ	Υ	N	Υ	Υ	Υ	Υ

zjid	0.0	'Zjid' (Instruction/Data Cache Synchronization)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zk	1.0	'Zk' (Standard scalar cryptography extension)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zkn	1.0	'Zkn' (NIST Algorithm Suite)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zknd	1.0	'Zknd' (NIST Suite: AES Decryption)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zkne	1.0	'Zkne' (NIST Suite: AES Encryption)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zknh	1.0	'Zknh' (NIST Suite: Hash Function Instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zkr	1.0	'Zkr' (Entropy Source Extension)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zks	1.0	'Zks' (ShangMi Algorithm Suite)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zksed	1.0	'Zksed' (ShangMi Suite: SM4 Block Cipher Instruct	iΥ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zksh	1.0	'Zksh' (ShangMi Suite: SM3 Hash Function Instruc	t Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zkt	1.0	'Zkt' (Data Independent Execution Latency)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zmmul	1.0	'Zmmul' (Integer Multiplication)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
ztso	0.1	'Ztso' (Memory Model - Total Store Order)	Υ	Υ	N	N	N	N	N	N	N
ztso	1.0	'Ztso' (Memory Model - Total Store Order)	N	N	Υ	Υ	N	N	N	Υ	Υ
zvbb	1.0	'Zvbb' (Vector basic bit-manipulation instructions	) Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zvbc	1.0	'Zvbc' (Vector Carryless Multiplication)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zvbc32e	0.7	'Zvbc32e' (Vector Carryless Multiplication with 32	N	N	Υ	Υ	N	N	N	N	N
zve32d	1.0		N	N	N	N	Υ	Υ	Υ	N	N
zve32f	1.0	'Zve32f' (Vector Extensions for Embedded Process	s Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zve32x	1.0	'Zve32x' (Vector Extensions for Embedded Proces	s <b>Y</b>	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zve64d	1.0	'Zve64d' (Vector Extensions for Embedded Proces	ξY	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zve64f	1.0	'Zve64f' (Vector Extensions for Embedded Process	s Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zve64x	1.0	'Zve64x' (Vector Extensions for Embedded Proces	s Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zvfbfmin	0.8		N	N	N	N	Υ	Υ	Υ	Υ	Υ
zvfbfmin	1.0	'Zvbfmin' (Vector BF16 Converts)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zvfbfwma	0.8		N	N	N	N	Υ	Υ	Υ	Υ	Υ
zvfbfwma	1.0	'Zvfbfwma' (Vector BF16 widening mul-add)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zvfh	0.1		N	N	N	N	Υ	Υ	Υ	N	N
zvfh	1.0	'Zvfh' (Vector Half-Precision Floating-Point)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zvfhmin	1.0	'Zvfhmin' (Vector Half-Precision Floating-Point Mi	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zvfofp4min	0.1	'Zvfofp4min' (OFP4 conversion extension Zvfofp4	n <b>N</b>	N	Υ	Υ	N	N	N	Υ	Υ
zvfofp8min	0.2	'Zvfofp8min' (OFP8 conversion extension Zvfofp8	n <b>N</b>	N	Υ	Υ	N	N	N	Υ	Υ
zvkb	0.1	'Zvkb' (Vector Bit-manipulation used in Cryptogra	ŗΥ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zvkb	1.0	'Zvkb' (Vector Bit-manipulation used in Cryptogra	ŗΥ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zvkg	0.1	'Zvkg' (Vector GCM instructions for Cryptography	) Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zvkg	1.0	'Zvkg' (Vector GCM instructions for Cryptography	) Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
zvkgs	0.7	'Zvkgs' (Vector-Scalar GCM instructions for Crypto	N	N	Y	Υ	N	N	N	N	N

zvkn	1.0	'Zvkn' (shorthand for 'Zvkned', 'Zvknhb', 'Zvkb', ar	ıΥ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvknc	1.0	'Zvknc' (shorthand for 'Zvknc' and 'Zvbc')	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvkned	1.0	'Zvkned' (Vector AES Encryption & Decryption (Sir	n Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvknf	0.1		N	N	N	N	Y	Υ	Υ	Υ	Υ	
zvkng	1.0	'zvkng' (shorthand for 'Zvkn' and 'Zvkg')	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvknha	0.1	'Zvknha' (Vector SHA-2 (SHA-256 only))	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvknha	1.0	'Zvknha' (Vector SHA-2 (SHA-256 only))	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvknhb	0.1	'Zvknhb' (Vector SHA-2 (SHA-256 and SHA-512))	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvknhb	1.0	'Zvknhb' (Vector SHA-2 (SHA-256 and SHA-512))	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvkns	0.1	'Zvkns' (Vector AES Encryption & Decryption (Sing	gΙΥ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvks	1.0	'Zvks' (shorthand for 'Zvksed', 'Zvksh', 'Zvkb', and	'.Y	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvksc	1.0	'Zvksc' (shorthand for 'Zvks' and 'Zvbc')	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvksed	0.1	'Zvksed' (SM4 Block Cipher Instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvksed	1.0	'Zvksed' (SM4 Block Cipher Instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvksg	1.0	'Zvksg' (shorthand for 'Zvks' and 'Zvkg')	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvksh	0.1	'Zvksh' (SM3 Hash Function Instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvksh	1.0	'Zvksh' (SM3 Hash Function Instructions)	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvkt	1.0	'Zvkt' (Vector Data-Independent Execution Latence	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvl1024b	1.0	'Zvl' (Minimum Vector Length) 1024	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvl128b	1.0	'Zvl' (Minimum Vector Length) 128	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvl16384b	1.0	'Zvl' (Minimum Vector Length) 16384	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvl2048b	1.0	'Zvl' (Minimum Vector Length) 2048	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvl256b	1.0	'Zvl' (Minimum Vector Length) 256	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvl32768b	1.0	'Zvl' (Minimum Vector Length) 32768	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvl32b	1.0	'Zvl' (Minimum Vector Length) 32	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvl4096b	1.0	'Zvl' (Minimum Vector Length) 4096	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvl512b	1.0	'Zvl' (Minimum Vector Length) 512	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvl64b	1.0	'ZvI' (Minimum Vector Length) 64	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvl65536b	1.0	'Zvl' (Minimum Vector Length) 65536	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvl8192b	1.0	'Zvl' (Minimum Vector Length) 8192	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ	
zvlsseg	0.10		N	N	N	N	Υ	Υ	Υ	Υ	Υ	
zvlsseg	1.0		N	N	N	N	Υ	Υ	Υ	Υ	Υ	
zvqdotq	0.0	'Zvqdotq' (Vector quad widening 4D Dot Product)	N	N	Y	Υ	N	N	N	N	N	