**Labprotokoll/innleveringsskjema**

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| **Innleveringsfrist:** | Se Canvas |
| **Innlevering** | Lab1: Brytere, lys, multipleksere og 7-segment. |
| **Navn:** | **Student1 og student2** |
| **Innlevert** (It’s L) | * Zippet prosjekt: Lab1\_dekoder\_7Seg\_DE2\_nn.zip * Dette dokumentet: Lab1\_protokoll |

**Oppgave 1: 7-segment decoder**

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| **Lim inn VHDL-kode:** 7-segment dekoder |
| LIBRARY ieee;  USE ieee.std\_logic\_1164.all;  ENTITY Dekoder\_7Seg\_nn IS  PORT( c :IN std\_logic\_vector(2 downto 0);  Syv\_seg\_kode : OUT std\_logic\_vector(6 downto 0));  END;  ARCHITECTURE behavior OF Dekoder\_7Seg\_nn IS  BEGIN  WITH c SELECT  Syv\_seg\_kode <= "0001001" WHEN "000",  "0001000" WHEN "001",  "1000111" WHEN "010",  "1000111" WHEN "011",  "1000000" WHEN "100",  "1111111" WHEN OTHERS;  END; |
| **Lim inn bilde fra RTL-viewer** |
| A screenshot of a video game  Description automatically generated |

**Oppgave 2:** Testbenk i Modelsim

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| **Lim inn kode: VHDL kode for simuleringsfilen (ta bare med prosessene)** |
| test\_7\_seg : PROCESS  BEGIN  c <= "000" AFTER 0 NS,  "001" AFTER 1\*500 NS,  "010" AFTER 2\*500 NS,  "011" AFTER 3\*500 NS,  "100" AFTER 4\*500 NS,  "101" AFTER 5\*500 NS,  "110" AFTER 6\*500 NS,  "111" AFTER 7\*500 NS;  WAIT FOR 8\*500 ns;  END PROCESS test\_7\_seg; |
| Simulering:  A picture containing wall, indoor  Description automatically generated |
| Analyse av simulering:  Ved å undersøke signalene ser det ut til at syv-segment kodene korresponderer til riktige input verdier og går i syklus |

**Oppgave 3: 7-segment-dekoderen testes på DE2-kortet**

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| **Lim inn VHDL-kode:** Dekoder\_7Seg\_DE2 |
| LIBRARY ieee;  USE ieee.std\_logic\_1164.ALL;  ENTITY Dekoder\_7Seg\_DE2\_nn IS  PORT(sw : in std\_logic\_vector(17 DOWNTO 0);  HEX0 : out std\_logic\_vector(6 DOWNTO 0));  END;  ARCHITECTURE struct OF Dekoder\_7seg\_DE2\_nn IS  COMPONENT Dekoder\_7Seg\_nn IS  PORT( c : IN std\_logic\_vector(2 DOWNTO 0);  Syv\_seg\_kode : OUT std\_logic\_vector(6 DOWNTO 0));  END COMPONENT;  BEGIN  dekoder\_7seg : component Dekoder\_7Seg\_nn  port map(  c(2) => sw(17),  c(1) => sw(16),  c(0) => sw(15),  Syv\_seg\_kode => HEX0  );  END; |
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**Lever også .zip-fil av prosjektkatalogen fra oppgave 3.**