Lab 3

Wien Bridge Oscillators

Purpose

The purpose of this set of experiments is to enable the students to the design of typical RC oscillators. The important design parameters (objectives) for this design are:

- The output signal frequency;
- The frequency stability;
- The signal purity (distortion);
- The signal amplitude.

Theory

The Wien bridge oscillator is an RC oscillator characterized by very good frequency stability and very good amplitude stability if it is well designed.

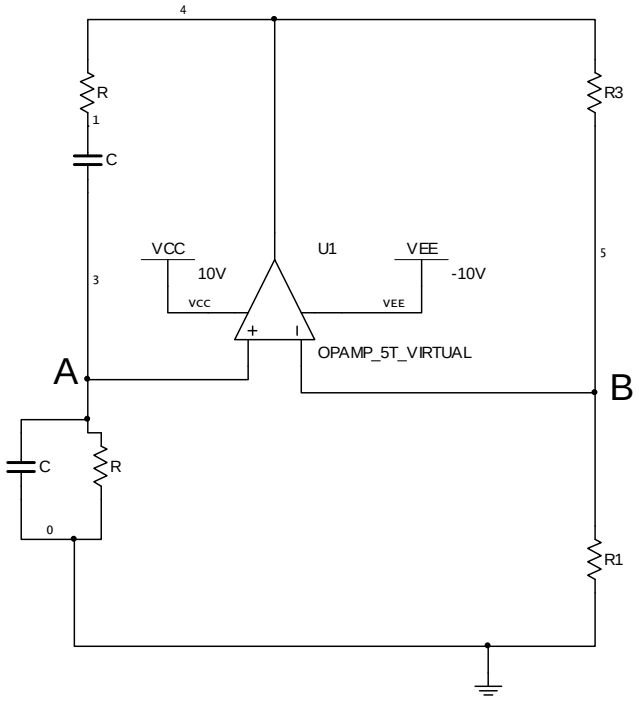


Figure 3- 1 Wien bridge oscillator

From Figure 3- 1, we see that the operational amplifier (op amp) is measuring the difference between the two voltages V_A and V_B and it is connected in such a way that it will try to make that difference as small as possible to bring the bridge to equilibrium.

Question I:

- find the frequency of oscillation and a relation between R1 and R3 when the bridge is at equilibrium ($V_A - V_B = 0$).

The results of question I are valid if and only if the op amp is ideal (infinite gain). A more realistic approach is to consider the amplification as finite. In order to study this system, we will use methods from feedback theory.

Question II:

- find the open loop gain $A_L(s)$ from the following circuit.

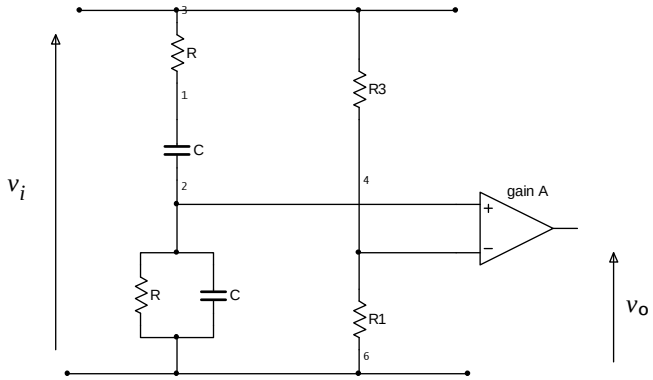


Figure 3- 2 Open loop gain

Use $\omega_0 = \frac{1}{RC}$ and $R3 = (2+\delta)R1$ in order to simplify the expression of $A_L(s)$. You should find:

$$A_L(s) = \frac{-A}{3+\delta}\frac{s^2 - s\delta\omega_0 + \omega_0^2}{s^2 + 3s\omega_0 + \omega_0^2}$$

- Plot its pole and zero diagram.

Question III:

When the output of the op amp is connected to top of the bridge, we obtain a closed loop.

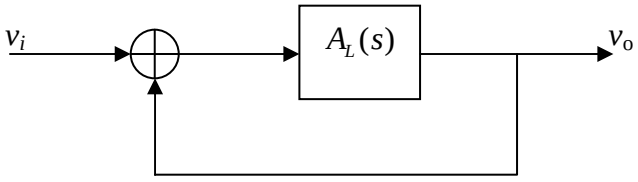


Figure 3- 3 Closed loop

The closed loop gain is given by:

$$G(s) = \frac{v_o(s)}{v_i(s)} = \frac{A_L(s)}{1 - A_L(s)}$$

We can remark that, since $A_L(s)$ is a ratio of two polynomials:

$$A_L(s) = \frac{-A}{3+\delta}\frac{N(s)}{D(s)}$$

The poles of the closed loop transfer function $G(s)$ are given by the following equation:

$$1 - A_L(s) = 0 \text{ or } D(s) + \frac{A}{3+\delta}N(s) = 0$$

So, when the gain of the op amp is very small, the closed loop poles are the same as those of the open loop transfer function $A_L(s)$. When the gain is very large (the usual case), they move toward the zeroes of $A_L(s)$.

The location of the poles of $G(s)$ for different values of the gain *A* is called the "*root locus*" of the system. The system is a sinusoidal oscillator if and only if there is only one pair of closed loop poles on the $j\omega$ axis. The other closed loop poles (if they exist) must be stable. In our case, there is only one pair. If they are on the left half of the *s*-plane, the system is stable and oscillations will not start. If they are on the right half, we will have exponentially growing oscillations that will bring the system to nonlinear operation.

- Find the gain A_0 necessary to have pure imaginary poles. What is their frequency (imaginary part)?

You should find: $A_0 = \frac{9}{\delta} + 3$

- What is the pole location when $A < A_0$ and when $A > A_0$?

We define an "*indirect frequency stability*" coefficient S_F as:

$$S_F = \omega_0 \left.\frac{d\phi}{d\omega}\right|_{\omega=\omega_0}$$

where ϕ is the phase (argument) of the open loop gain $A_L(s)\big|_{s=j\omega}$. In the case of the Wien bridge oscillator, this stability coefficient is given by:

$$S_F = -\frac{2\sqrt{\omega_1\omega_2}}{\omega_1+\omega_2} - 2Q_{Tz}$$

where $-\omega_1$ and $-\omega_2$ are the two poles of $A_L(s)$ and Q_{Tz} is the "Q" of the zeroes:

$$Q_{Tz} = \frac{1}{\delta}$$

Practical part

1. Oscillator without automatic gain control (AGC)

a) Design:

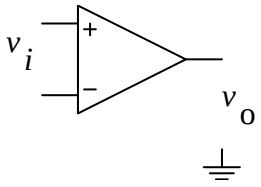
* Compute S_F for δ=1 (R3 = 3R1).

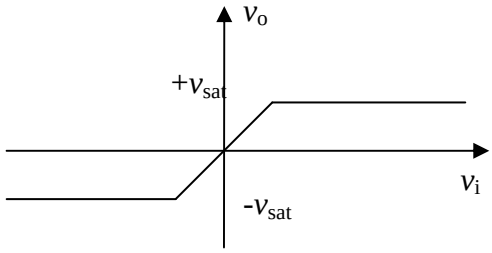
* What is the necessary gain A_0?

* The op amp used in this experiment is the OPAMP_5T_VIRTUAL from the analog group, ANALOG_VIRTUAL family. Its differential gain is 200 000, which is very large. For this case, find the closed loop pole location

* Will this system be a "good" oscillator?

The op amp characteristic is roughly piecewise linear.





* In this case, for the pole location that you have found, would the output be sinusoidal?

* What will be the output amplitude?

* Give an estimate of the output frequency.

b) Implementation:

* Implement the Wien bridge according to Figure 3- 1 with an oscillation frequency $f_0 = \frac{\omega_0}{2\pi} = 1\,\text{kHz}$, δ= 1. Set R = 1 kΩ. The other two resistors should be selected in the ten kΩ range. For this part, use values from the E24 series.

* Connect an oscilloscope and a frequency meter at the output of the op amp.

* Sketch the output waveform.

* Measure its frequency.

* Use the distortion meter, set its frequency at the value measured by the frequency meter and measure the waveform distortion.

2. AGC using FET transistor

a) Design:

The previous design gave a very unsatisfactory oscillator due to the large value of δ. The only way to have a good and very stable oscillator is to choose δ as small as possible.

However, from the equation $A_0 = \frac{9}{\delta} + 3$, we see that if $\delta = 0$, then we need an infinite gain in order to have an oscillation. Since all op amps have very large but finite gain, this condition is impossible to achieve. This means that a Wien bridge oscillator design with $\delta = 0$ (R3 = 2R1) cannot work.

General rule for sinusoidal oscillator design:

- Design the oscillator such that the oscillations always occur at start up (when we turn the power supply on): *Set the closed loop poles at the right of the $j\omega$ axis.* At start up, we will have growing oscillations.
- For some selected amplitude of the output waveform, your design should reduce the gain so that the poles move toward the left of the *s*-plane.

We see that we need some kind of automatic gain control in all sinusoidal oscillators.

In the case of the Wien bridge designed around an op amp, the gain of the amplifier is fixed (if we do not allow the amplitude of the output to reach saturation). However, the condition $A_0 = \frac{9}{\delta} + 3$ shows that we can act on the value of δ in order to have an automatic gain control.

A_0 being fixed, if $\delta > 0$ (but very small), we will have growing oscillations at start up. If we make $\delta < 0$, the closed loop poles will move to the left of the $j\omega$ axis, the amplitude of the oscillation will decay.

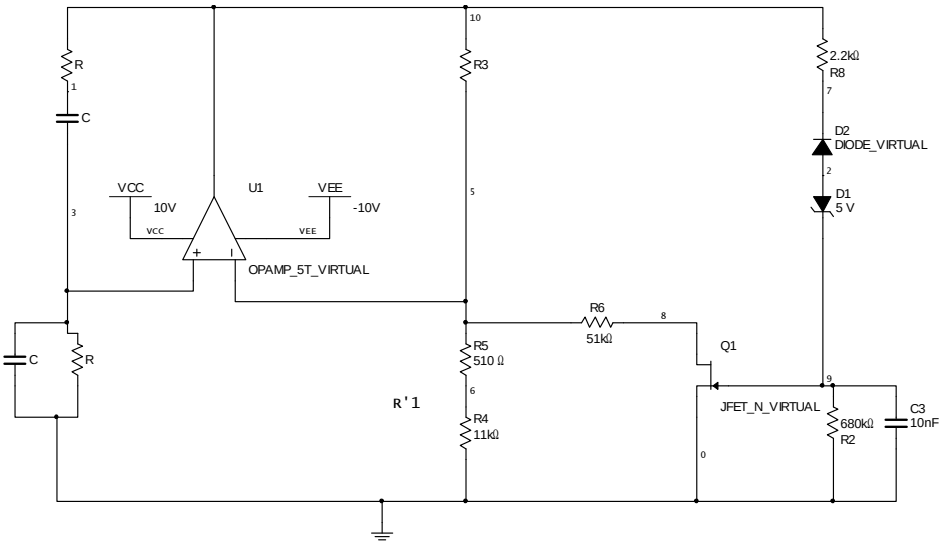


Figure 3- 4 AGC using FET

Using the above defined principle, we are going to make the resistance *R*1 of Figure 3- 1 variable with the output amplitude. In the above figure (Figure 3- 4), the resistance *R*'1 is the

sum of the two resistances $R4$ and $R5$. The resistance $R1$ is the parallel connection of $R'1$ and the series connection of R6 and R_{DS}, $R1 = R'1//(R6 + R_{DS})$. R_{DS} is the resistance of the channel of the FET. If the drain to source voltage is limited to a few hundreds of millivolts, this resistance is given by the following expression:

$$R_{DS} = \frac{V_p^2}{2I_{DSS}\left(\left|V_p\right| + v_{GS}\right)} \qquad V_p \le v_{GS} \le 0$$

The advantage of this method of amplitude stabilization is its low distortion due to the gradual variation of $R1$.

* Explain in a few lines the principle of this method of amplitude stabilization.

In order to simplify the different expressions, let us call $R0 = R3/2$.

* Draw the curve of R_{DS} versus v_{GS} (use $V_p = -2$ V and $I_{DSS} = 0.4$ mA).

In order to minimize the voltage across the channel of the FET, we select $R6$ to be quite large ($R6 = 10R0$).

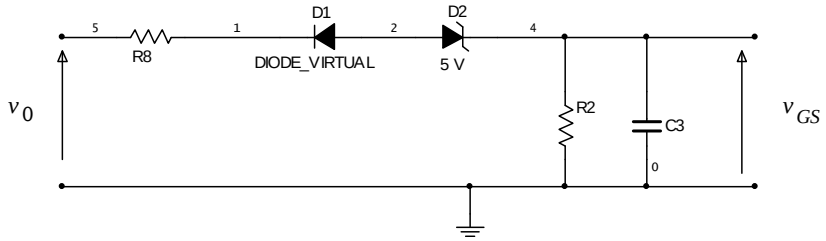
* At start up, C3 is discharged and $v_{GS} = 0$. In this case, we would like to have growing oscillations ($\delta > 0$). What relation should $R'1$ satisfy?

* The amplitude of the output increases. At some point, the Zener diode turns on. The value of R_{DS} will change until the relation $A_0 = \frac{9}{\delta} + 3$ is satisfied. Since A_0 is very large, this relation is satisfied by a very small value of δ. We can safely assume $\delta = 0$. So, $R1 = R'1//\left(R6 + R_{DS}\right) \approx R0$. What is the value of R_{DS} when we have equality?

* In order to have the previous relation satisfied, we must have: $R'1 > R0$.

* With the two inequalities select an appropriate value for $R'1$ as a function of $R0$ ($R'1 = kR0$). Select k.

The circuit at the input of the FET is a peak detector.



* The time constant $R2C3$ must be much larger than the period of the oscillation. The transfer between the voltage v_{GS} and the output amplitude V_0 ($v_0(t) = V_0 \cos \omega_0 t$) is then a piecewise linear characteristic. Make a plot of it.

* The resistor R8 is used to limit the current flowing in the above circuit.

* Design a Wien bridge with FET AGC and f_0 = 1 kHz, $R0$ = 11 kΩ.

* Predict the output amplitude from the two curves you have drawn.

b) Implementation:

* Implement the circuit of Figure 3- 4.

* Visualize the output waveform on the oscilloscope.

* Measure the output frequency.

* Measure its distortion.

* Change the power supply values (double click on VCC and VEE) to + and – 15 V. Do your measurements change?

* Write an overall conclusion.