MOSTEK®

2048 x 8-BIT PROM

Electrically Programmable/Ultraviolet Erasable ROM

MK2716 (T)-5/6/7/8

FEATURES

- ☐ Replacement for popular 2048 x 8 bit 2716 type EPROM
- ☐ Single +5 volt power supply during READ operation
- ☐ Fast Access Time in READ mode

P/N	Access Time
MK2716-5	300ns
MK2716-6	350ns
MK2716-7	390ns
MK2716-8	450ns

- ☐ Low Power Dissipation: 525 mW max active
- ☐ Power Down mode: 132 mW max standby
- ☐ Three State Output OR-tie capability
- ☐ Five modes of operation for greater system flexibility (see Table)
- ☐ Single programming requirement: single location programming with one 50 msec pulse
- ☐ Pin Compatible with Mostek's Wide Word Memory Family
- ☐ TTL compatible in all operating modes
- ☐ Standard 24 pin DIP with transparent lid

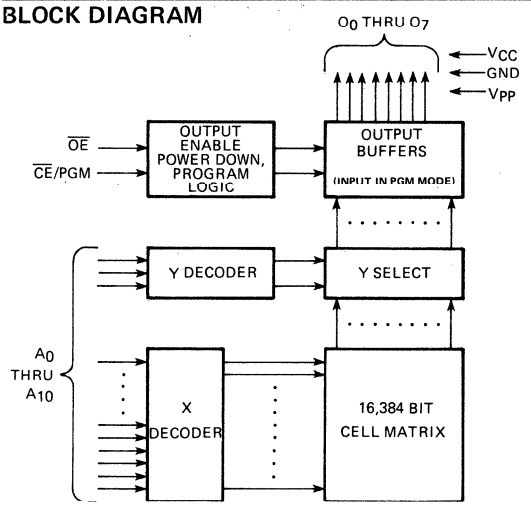
DESCRIPTION

The MK2716 is a 2048 x 8 bit electrically programmable/ultraviolet erasable Read Only Memory. The circuit is fabricated with Mostek's advanced N-channel silicon gate technology for the highest performance and reliability. The MK2716 offers significant advances over hardwired logic in cost, system flexibility, turnaround time and performance.

The MK2716 has many useful system oriented features including a STANDBY mode of operation which lowers the device power from 525 mW maximum active power to 132 mW maximum for an overall savings of 75%.

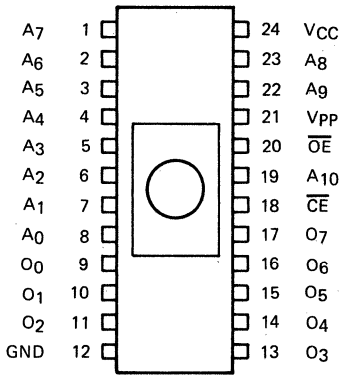
PROMs

BLOCK DIAGRAM



NOTE: Pin 18 and 20 have been renamed for compatibility with presently available 16K, 32K and 64K ROMs and future generation 32K and 64K EPROMs. All other specifications for this device remain unaffected by this change.

PIN OUT



A0 - A10	ADDRESSES
CE/PGM	CHIP ENABLE/PROGRAM
OE	OUTPUT ENABLE
O0 - O7	OUTPUTS

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to VSS (Except VPP) ..... -0.3V to +6V
Voltage on VPP supply pin relative to VSS ..... -0.3V to +28V
Operating Temperature TA (Ambient) ..... 0°C ≤ TA ≤70°C
Storage Temperature (Ambient) ..... -55°C ≤ TA ≤+125°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

RECOMMENDED D.C. OPERATING CONDITIONS AND CHARACTERISTICS[1,2,4,8]

(0°C ≤ TA ≤ 70°C) (VCC = +5V ±5%, VPP = VCC)[3]

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IH}	Input High Voltage	2.0		Vcc+1	Volts	
V_{IL}	Input Low Voltage	-0.1		0.8	Volts	
I_{CC1}	VCC Standby Power Supply Current ($\overline{OE}$ = VIL; $\overline{CE}$ = VIH)		10	25	mA	2
I_{CC2}	VCC Active Power Supply Current ($\overline{OE}$ = $\overline{CE}$ = VIL)		57	100	mA	2
I_{PP1}	VPP Current (VPP = 5.25V)			6	mA	2,3
V_{OH}	Output High Voltage (IOH = -400 μA)	2.4			Volts	
V_{OL}	Output Low Voltage (IOL = 2.1mA)			.45	Volts	
I_{IL}	Input Leakage Current (VIN = 5.25V)			10	μA	
I_{OL}	Output Leakage Current (VOUT = 5.25V)			10	μA	

AC CHARACTERISTICS[1,2,5]

(0°C ≤ TA ≤ 70°C) (VCC = +5V ± 5%, VPP = VCC)[3]

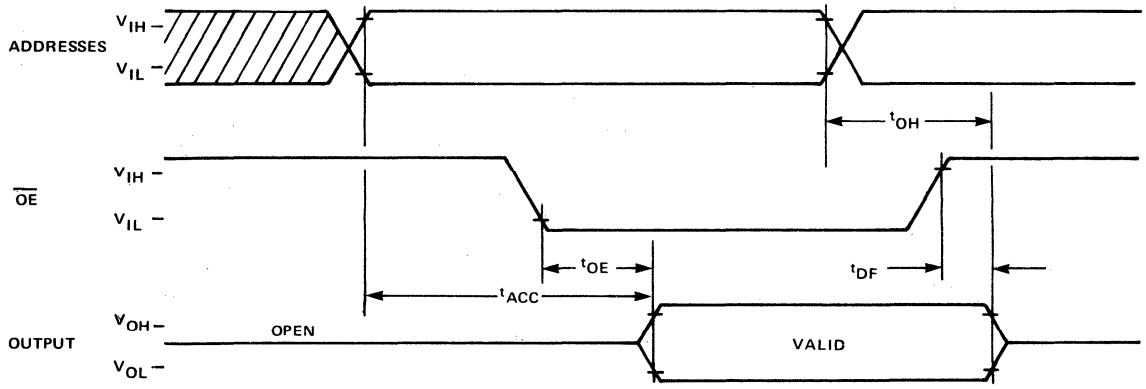
		-5		-6		-7		-8			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{ACC}	Address to Output Delay ($\overline{CE}$ = $\overline{OE}$ = VIL)		300		350		390		450	ns	
t_{CE}	$\overline{CE}$ to Output Delay ($\overline{OE}$ = VIL)		300		350		390		450	ns	6
t_{OE}	Output Enable to Output Delay ($\overline{CE}$ = VIL)		120		120		120		120	ns	10
t_{DF}	Chip Deselect to Output Float ($\overline{CE}$ = VIL)	0	100	0	100	0	100	0	100	ns	9
t_{OH}	Address to Output Hold ($\overline{CE}$ = $\overline{OE}$ = VIL)	0		0		0		0		ns	

CAPACITANCE
(TA = 25°C)[8]

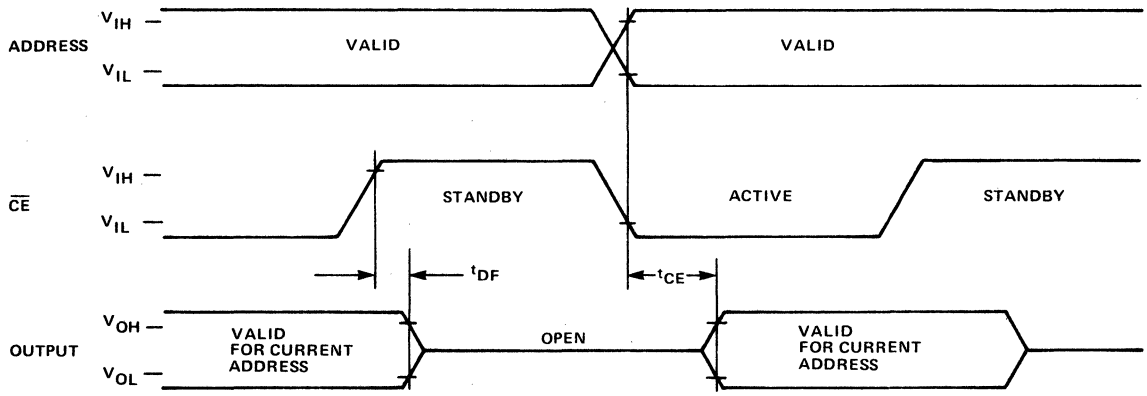
SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{IN}	Input Capacitance	4	6	pF	7
C_{OUT}	Output Capacitance	8	12	pF	7

NOTES:
1. VCC must be applied on or before VPP and Removed after or at the same times as VPP.
2. VPP and VCC may be connected together except during programming, in which case the supply current is the sum of ICC and IPP1.
3. The tolerance on VPP is to allow use of a driver circuit to switch VPP from VCC to +25V in the READ and PROGRAM mode respectively.
4. All voltages with respect to VSS.
5. Load conditions = ITTL load and 100pF., tr = tf = 20ns, reference levels are 1V or 2V for inputs and .8V and 2V for outputs.
6. tOE is referenced to $\overline{CE}$ or the addresses, whichever occurs last.
7. Effective Capacitance calculated from the equation C = △ △V where △V = 3V
8. Typical numbers are for TA = 25°C and VCC = 5.0V
9. tDF is applicable to both $\overline{CE}$ and $\overline{OE}$, whichever occurs first.
10. OE may follow up to tACC - tOE after the falling edge of $\overline{CE}$ without effecting tACC

TIMING DIAGRAMS
READ CYCLE ($\overline{CE}$ = V_{IL})



STANDBY POWER DOWN MODE
($\overline{OE}$ = V_{IL})



PROMs

PROGRAM OPERATION[8]

D.C. ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS[1,2]

(TA = 25°C ± 5°C) (VCC = 5V ±5%, VPP = 25V ±1V)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
IIL	Input Leakage Current		10	μA	3
VIL	Input Low Level	-0.1	0.8	Volts	
VIH	Input High Level	2.0	VCC +1	Volts	
ICC	VCC Power Supply Current		100	mA	
IPP1	VPP Supply Current		5	mA	4
IPP2	VPP Supply Current during Programming Pulse		30	mA	5

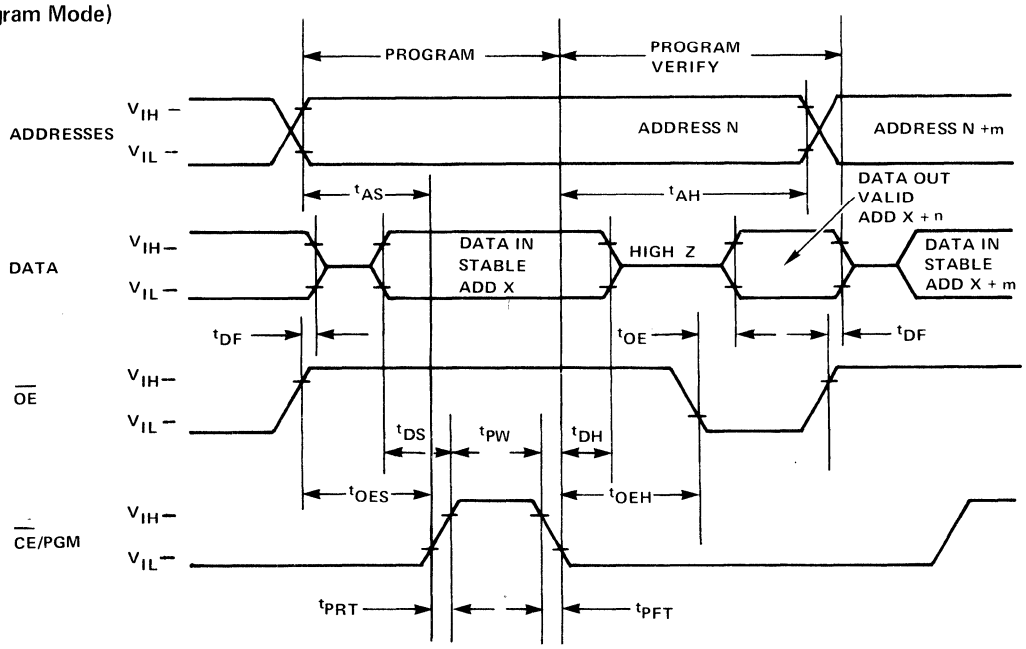
A.C. CHARACTERISTICS AND OPERATING CONDITIONS[1,2,6,7]

(TA = 25°C ± 5°C) (VCC = 5V ± 5%, VPP = 25V ± 1V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{OEH}	$\overline{OE}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Output Enable to Output Float	0		120	ns	4
t_{OE}	Output Enable to Output Delay			120	ns	4
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

NOTES:
1. VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into a board with VPP at 25V.
2. Care must be taken to prevent overshoot of the VPP supply when switching to +25V.
3. 0.45V ≤ VIN ≤ 5.25V
4. $\overline{CE}$/PGM VIL
5. $\overline{CE}$/PGM VIH
6. tT = 20nsec
7. 1V or 2V for inputs and.8V or 2V for outputs are used as timing reference levels.
8. Although speed selections are made for READ operation all programming specifications are the same for all dash numbers.

TIMING DIAGRAM
(Program Mode)



MODE SELECTION

MODE	PIN	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	VPP (21)	OUTPUTS
READ		VIL	VIL	+5	Valid Out
STANDBY		VIH	Don't Care	+5	Open
PROGRAM		Pulsed VIL to VIH	VIH	+25	Input
PROGRAM VERIFY		VIL	VIL	+25	Valid Out
PROGRAM INHIBIT		VIL	VIH	+25	Open
VCC(24) = 5V all modes					

DESCRIPTION CONTINUED

Programming can be done with a single TTL level pulse, and may be done on any individual location either sequencially or at random. The three-state output controlled by the $\overline{OE}$ input allows OR-tie capability for construction of large arrays. A single power supply requirement of +5 volts makes the MK2716 ideally suited for use with Mostek's new 5 volt only microprocessors such as the MK3880 (Z80). The MK2716 is packaged in the industry standard 24-pin dual-in line package with a transparent hermetically sealed lid. This allows the user to expose the chip to ultraviolet light to erase the data pattern. A new pattern may then be written into the device by following the program procedures outlined in this data sheet.

The MK2716 is specifically designed to fit those applications where fast turnaround time and pattern experimentatin are required. Since data may be altered in the device (erase and reprogram) it allows for early debugging of the system program. Since single location programming is available the MK2716 can have its data content increased (assuming all 2048 bytes were not programmed) at any time for easy updating of system capabilities in the field. Once the data/program is fixed and the intention is to produce large numbers of systems, Mostek also supplies a pin compatible mask programmable ROM, the MK34000. To transfer the program data to ROM, the user need only send the PROM along with device information to MOSTEK, from which the ROM with the desired pattern can be generated. This means a reduction in the possibility of error when converting data to other forms (cards, tape, etc.) for this purpose. However, data may still be input by any of these traditional means such as paper tape, card deck, etc.

READ OPERATION

The MK2716 has five basic modes of operation. Under normal operating conditions (non-programming) there are two modes including READ and STANDBY. A READ operation is accomplished by maintaining pin 18 ($\overline{CE}$) at VIL and pin 21 (VPP) at +5 volts. If $\overline{OE}$ (pin 20) is held active low after addressing (A0 - A10) have stabilized then valid output data will appear on the output pins at access time tACC (address access). In this mode, access time may be referenced to $\overline{OE}$ (tOE) depending on when $\overline{OE}$ occurs (see timing diagrams).

POWER DOWN operation is accomplished by taking pin 18 ($\overline{CE}$) to a TTL high level (VIH). The power is reduced by 75% from 525mW maximum to 132mW. In power down VPP must be at +5 volts and the outputs will be open-circuit regardless of the condition of $\overline{OE}$. Access time from a high to low transition of $\overline{CE}$ (tCE) is the same as from addresses (tACC). (See STANDBY Timing Diagram).

PROGRAMMING INSTRUCTIONS

The MK2716 as shipped from Mostek will be completely erased. In this initial state and after any subsequent erasure, all bits will be at a '1' level (output high). Information is introduced by selectively programming '0's into the proper bit locations. Once a '0' has been programmed into the chip it may be changed only by erasing the entire chip with UV light.

Word address selection is done by the same decode circuitry used in the READ mode. The MK2716 is put into the PROGRAM mode by maintaining VPP at +25V, and $\overline{OE}$ at VIH. In this mode the output pins serve as inputs (8 bits in parallel) for the required program data. Logic levels for other inputs and the VCC supply voltage are the same as in the READ mode.

The program a "byte" (8 bits) of data, a TTL active high level pulse is applied to the $\overline{CE}$/PGM pin once addresses and data are stabilized on the inputs. Each location must have a pulse applied with only one pulse per location required. Any individual location, a sequence of locations or locations at random may be programmed in this manor. The program pulse has a minimum width of 45 msec and a maximum of 55msec, and must not be programmed with a high level D.C. signal applied to the $\overline{CE}$/PGM pin.

PROGRAM INHIBIT is another useful mode of operation when programming multiple parallel addressed MK2716's with different data. It is necessary only to maintain $\overline{OE}$ at VIH, VPP at +25, allow addresses and data to stabilize and pulse the $\overline{CE}$/PGM pin of the device to be programmed. Data may then be changed and the next device pulsed. The devices with $\overline{CE}$/PGM at VIL will not be programmed.

PROGRAM VERIFY allows the MK2716 program data to be verified without having to reduce VPP from +25V to +5V. VPP should only be used in the PROGRAM/PROGRAM INHIBIT and PROGRAM VERIFY modes and must be at +5V in all other modes.

MK2716 ERASING PROCEDURE

The MK2716 may be erased by exposure to high intensity ultraviolet light, illuminating the chip thru the transparent window. This exposure to ultraviolet light induces the flow of a photo current from the floating gate thereby discharging the gate to its initial state. An ultraviolet source of 2537Å yielding a total integrated dosage of 15 Watt-seconds/cm^2 is required. Note that all bits of the MK2716 will be erased. The erasure time is approximately 15 to 20 minutes utilizing a ultra-violet lamp with a 12000μW/cm^2 power rating. The lamp should be used without short wave filters, and the MK2716 to be erased should be placed about one inch away from the lamp tubes. It should be noted that as the distance between the lamp and the chip is doubled, the exposure time required goes up by a factor of 4. The UV content of sunlight is insufficient to provide a practical means of erasing the MK2716. However, it is not recommended that the MK2716 be operated or stored in direct sunlight, as the UV content of sunlight may cause erasure of some bits in a short period of time.