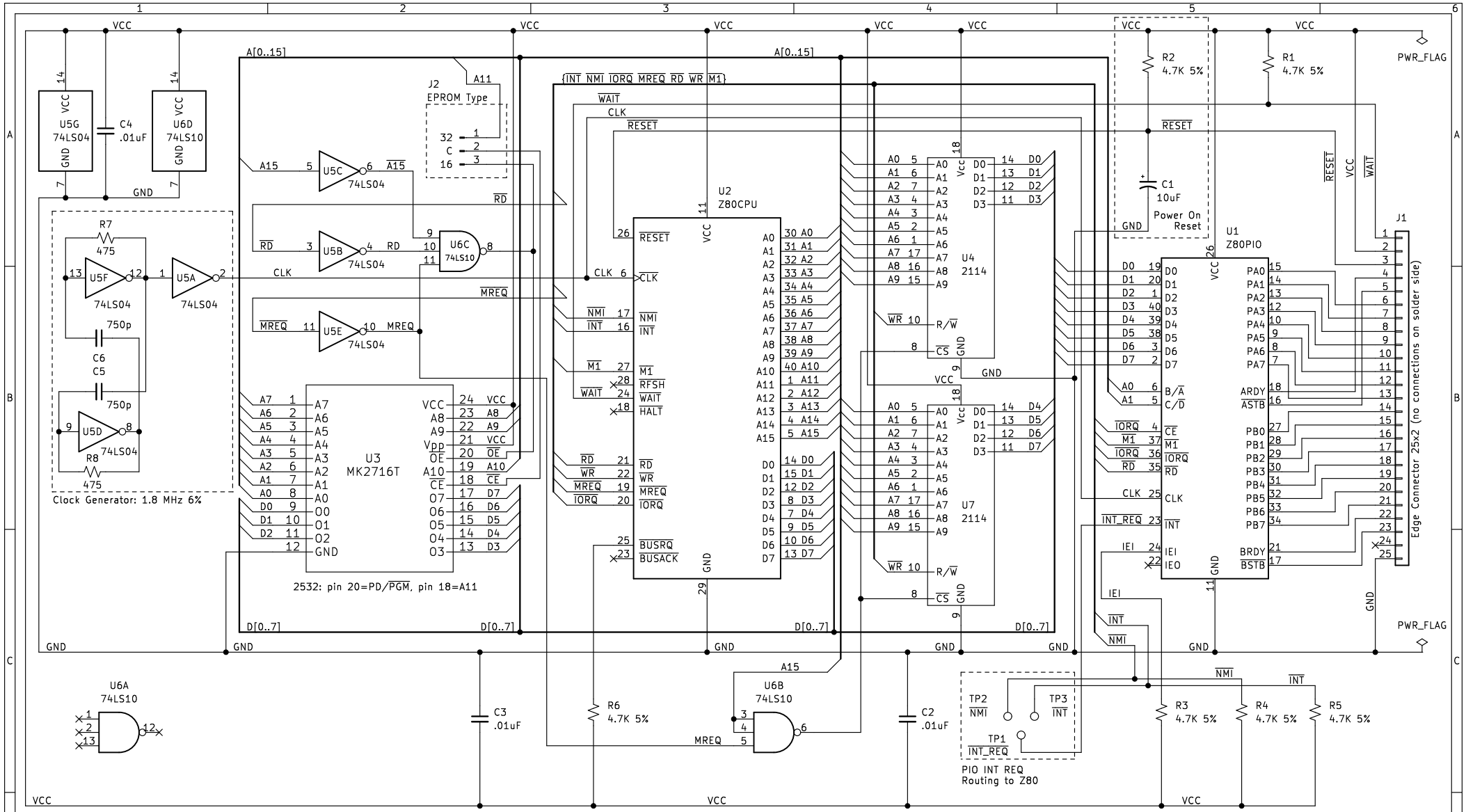

PIO: *I/O addresses 0–3, with A15–A2 don't care ($\overline{IORQ}$ low)*
0: Port A Data; 1: Port B Data; 2: Port A Control; 3: Port B Control
RAM: *FC00–FFFF (2114: 1Kx8) (aliased if A15=1, with A14–A10 don't care)*
EPROM: 0000–07FF (2716: 2Kx8) (aliased if A15=0, with A14–A11 don't care)
0000–0FFF (2532: 4Kx8) (aliased if A15=0, with A14–A12 don't care)
Jumper J2: 1–2 A11 –> 2532 EPROM U3 pin 18 A11
2–3 $\overline{OE/CE}$ signal = ~[MREQ+RD+A15] –> 2716 EPROM U3 pin 18 $\overline{CE}$
NOTE: 2532 pin 20 is PD/$\overline{PGM}$, which acts as a Power Down / $\overline{CE}$ in read mode.
Pin 20 always receives the $\overline{OE/CE}$ signal = ~[MREQ+RD+A15]
NOTE: The sample board does not have C1 installed. The 10uF shown matches that used in the John Bell Engineering 80–153 6502 Microcomputer. It should provide a $\overline{RESET}$ low level for between 8.2 and 24 msec from power on.

Reverse engineering from sample board
by Sig Nin, Morgan Hill, CA
07/27/2022 Verified by continuity check
NOTE: EPROM 2716 2Kx8 or 2532 4Kx8
John Bell Jr.

Sheet: /
File: z–80_Computer_John_Bell_80–280.kicad_sch

Title: 80–280 Z80 Computer

Size: A4	Date: 2022–08–09	**Rev: 1.8**
KiCad E.D.A. kicad (6.0.6)		Id: 1/1