ECE 585

MSD Memory Controller Testplan

GROUP-24

Seggari Koushik

Sigicherla Srikanth

R. Jitendra Prasad

Cheedu Venkat sahith Reddy

Test intention:

We are simulating the scheduler portion of a memory controller. When testing the memory controller scheduler against the specified standards, the testbench should try to completely evaluate the memory controller's operation and performance.

In this project, we simulated the Microcontroller scheduler with **closed page policy-no bank parallelism.**

Test flow:

Initially, we have defined the inputs as time, core, operation, and address in struct mode format. The array structure has the size of 16, with index starting from zero.

In address mapping, 2 bits are assigned for byte select, 4 bits are assigned for lower column, 1 bit for channel, 3 bits for bank groups, 2 bits for banks, 6 bits for high column, 16 bits are assigned for row. There are a total of 34 bits. To extract information from addresses, the length of each entry is as follows:

Byte-select: [0:1], low column: [5:2], channel: [6:6], bank group: [9:7], bank: [11:10], high column: [17:12], row: [33:18] all these are extracting information from request part of address

We give the request at every Pos-edge clk of cpu cycle and according to that request we issue the DRAM command.

Test steps:

- 1.1 If the processed request and the next request is having the same bank group and the same bank respectively, then the ACT command for the next request will be issued after Trp clock cycles since the row needs to be pre-charged.

  ACT0 | ACT1 (TRCD)
  RD0 | RD1 (TCL + T Brust)

  +PRE (TRP)

- 1.2 If the processed request and the next request is not having the same bank group and the different bank respectively, then the ACT command for the next request will be issued in next clock cycle after We need NOT to wait till TRP to issue next ACT Command.

ACT0 | ACT1 (TRCD)

RD0 | RD1 (TCL + T Brust)

PRE (TRP)

Expected output for the given input:

INPUT:

Time Core Operation Address

1 2 0 0x01FFFF009

(Row: 7FF, Columnh:3F ,Bank: 0,BG:0 ,Channel:0 , ColumnL:2 ,Byte-Select: 1)

2 10 1 0x10FFFF052

(Row: 43FF, Columnh:3F ,Bank: 0,BG:0 ,Channel:1 , ColumnL:4 ,Byte-Select: 2)

3 12 2 0x10FDFF433

(Row: 43F7, Columnh:3F ,Bank: 1,BG:0 ,Channel:0 , ColumnL:C ,Byte-Select: 1)

If the processed instruction and next instruction have same bank group and same bank, and the ACT command for the next instruction will be issued after waiting Trp clock cycle:

2 ACT0 0 0 7FF

2 ACT1 0 0 7FF

80 Read0 0 0 3F (T_{RCD}) (Where, $T_{RCD} = T_{RP}$ x 2 + ACT (Here, T_{RP} = 39 clock cycles, ACT = 2 clock cycles))

80 Read1 0 0 3F (T_{RCD})

176 PRE 0 0 (($T_{CL} + T_{Burst}$)x 2 +80) (T_{CL} = 40, T_{Burst} = 8)

(T_{RP} x 2 + 176) = (39 x 2) + 176 = 254 clock cycles

Hence the ACT command for the next instruction is given after 254 clock cycle i.e 256.

256 ACT0 0 0 43FF

256 ACT1 0 0 43FF

334 Read0 0 0 3F (T_{RCD}) ($T_{RCD} = T_{RP}$ x 2 + ACT (T_{RP} = 39, ACT = 256)

334 Read1 0 0 3F (T_{RCD})

430 PRE 0 0 (($T_{CL} + T_{Burst}$)x 2 +334) (T_{CL} = 40, T_{Burst} = 8)

If the processed instruction and next instruction have same bank group and different banks, the process need not wait for TRP ACT command for the next instruction will be issued at the next DIMM clock cycle

432 ACT0 0 1 43F7

432 ACT1 0 1 43F7

510 Read0 0 1 3F (T_{RCD}) ($T_{RCD} = T_{RP}$ x 2 + ACT (T_{RP} = 39, ACT = 432)

510 Read1 0 1 3F (T_{RCD})

606 PRE 0 0 (($T_{CL} + T_{Burst}$)x 2 +510) (T_{CL} = 40, T_{Burst} = 8)