

A

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There are three wiring harness exceptions (EXCEPTION #1, 2, 3).
See page 4 for those wiring harness exceptions.

Rev. 1
[initial release]

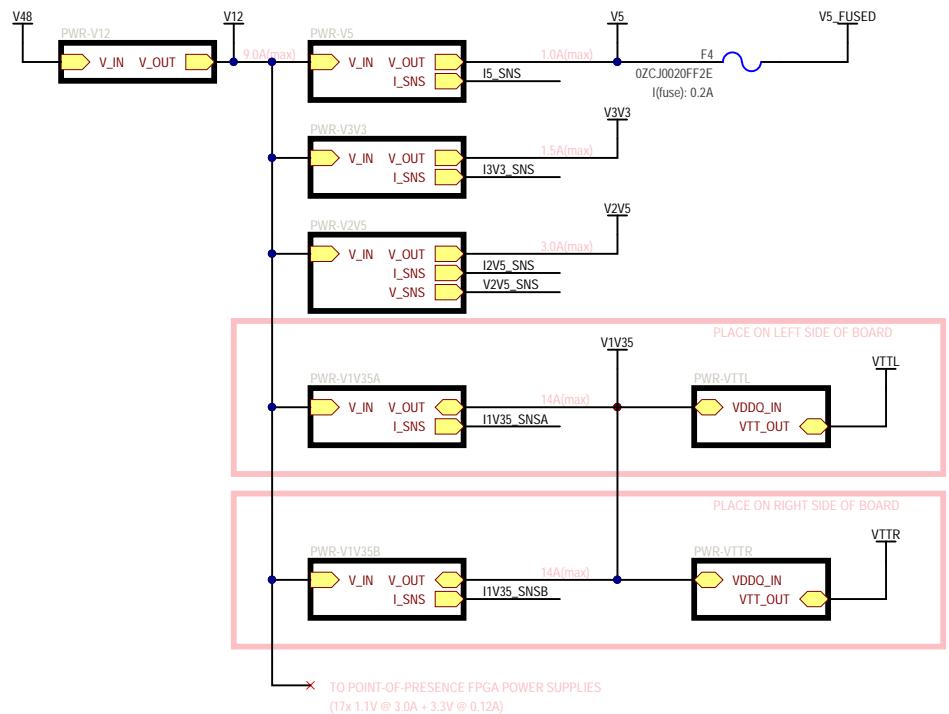
Rev. 2 CHANGE LOG
[not tracked / rev. 1 boards not in service]

Rev. 3 CHANGE LOG

- IL.CFG.LR.VTT missing power connection fixed
- CFG FPGA LED cathode undervoltage voltage fixed
- Increased undervoltage lock out (UVLO) voltage
- Removed board-to-board JTAG to improve JTAG signal integrity
- Added series termination to all MCLK pins
- Added a series termination to all MIB buses
- Added series termination to FMC CLK
- Changed FPGA clock to 125 MHz
- DNP'd pull-up resistor on MCU BOOT pin (already had pull-down)

Known issues [SIGLABS INTERNAL - SEE GIT ISSUE TRACKING FOR MORE DETAILS]:

- MCU Power Down Reset not being pulled properly
- Mechanical thru hole tolerance issue
- wrong silk screen revision
- no longer need option pads for connector VCCIO nets
- add PROG_N pull-ups (removes necessity for array reset by software)
- G13.D6 doesn't match between top and bottom connectors
- ESD protection needed on SLK_SEL, PROG_N, MCU_RST_N
- Inductors still buzzing
- Solder resist slivers
- global clock and reset nets needs length matching
- clock input not on true differential input



MCU ANALOG INPUTS

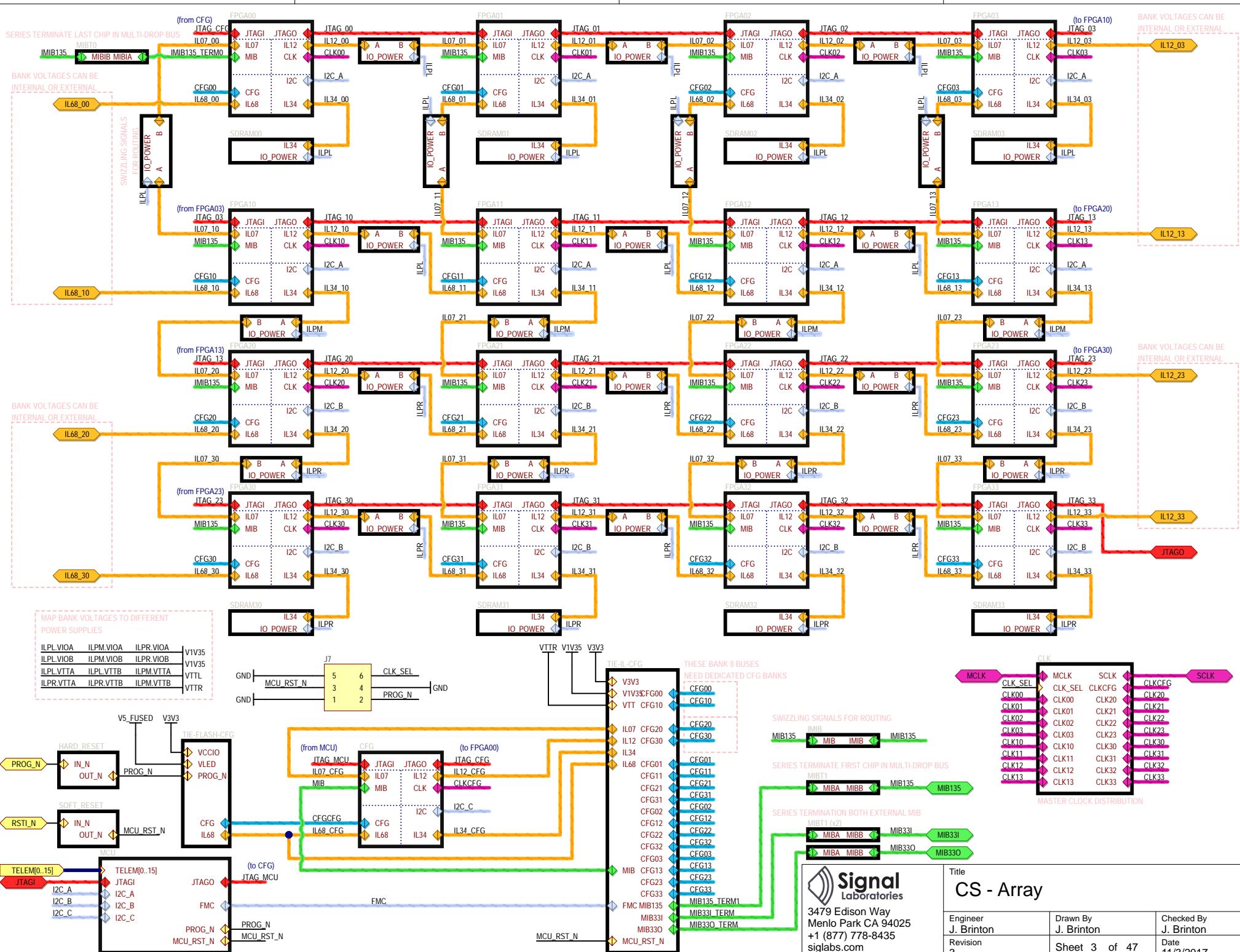
I3V3_SNS	NT1	A B	TELEM0
I2V5_SNS	NT2	A B	TELEM1
V2V5_SNS	NT3	A B	TELEM2
I1V35_SNSA	NT4	A B	TELEM3
V1V35	NT5	A B	TELEM4
I1V35_SNSB	NT6	A B	TELEM5
IL68_30.LR.VTT	NT7	A B	TELEM6
IL68_30.VIOLR	NT8	A B	TELEM7
IL68_10.LR.VTT	NT9	A B	TELEM8
IL68_10.VIOLR	NT10	A B	TELEM9
IL12_13.LR.VTT	NT11	A B	TELEM10
IL12_13.VIOLR	NT12	A B	TELEM11
IL12_33.LR.VTT	NT13	A B	TELEM12
IL12_33.VIOLR	NT14	A B	TELEM13
IL12_33.VIOLR	NT15	A B	TELEM14
I5_SNS	NT16	A B	TELEM15



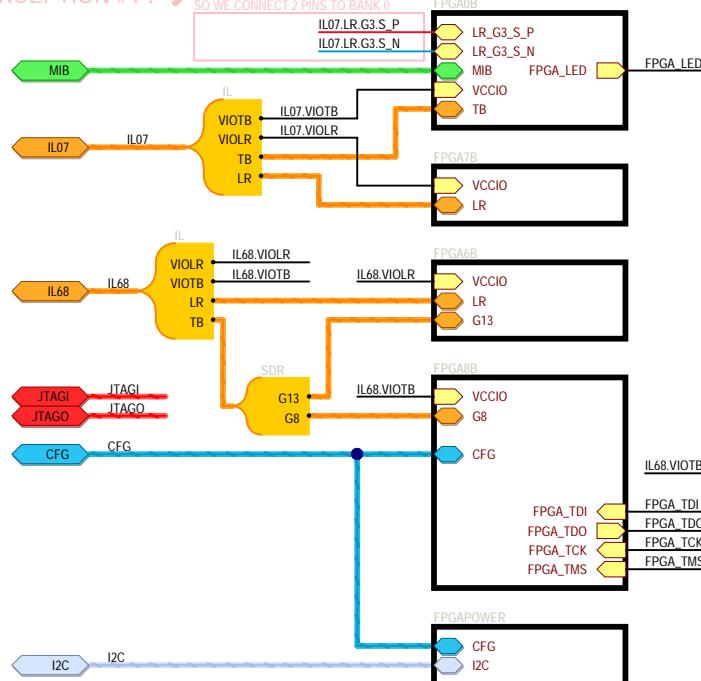
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Title
CS - Main

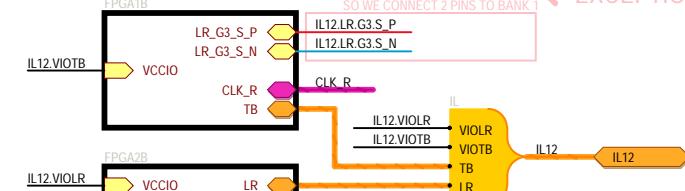
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EXCEPTION #1 ! → BANK 7 DOES NOT HAVE ENOUGH PINS
SO WE CONNECT 2 PINS TO BANK 0

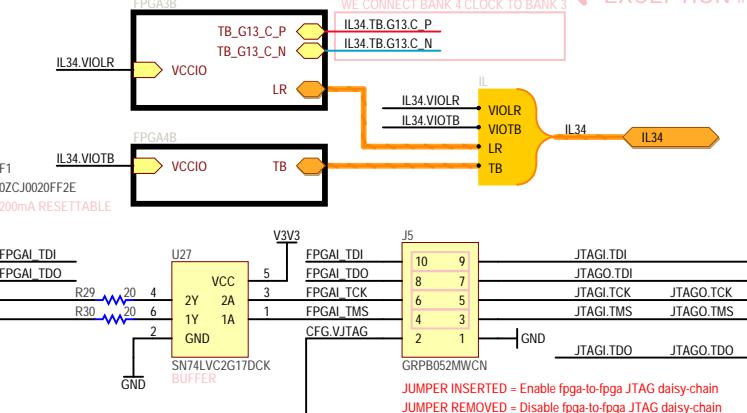


BANK 2 DOES NOT HAVE ENOUGH PINS
SO WE CONNECT 2 PINS TO BANK 1

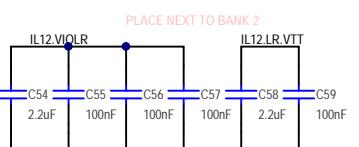
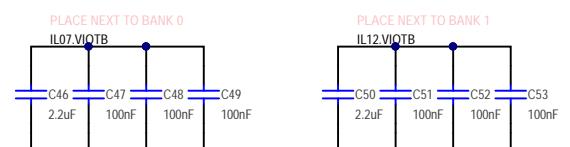
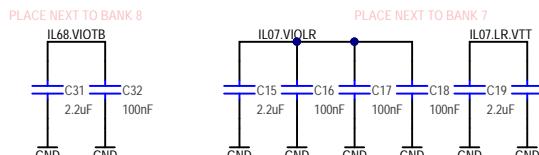
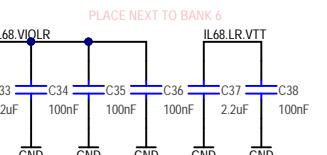
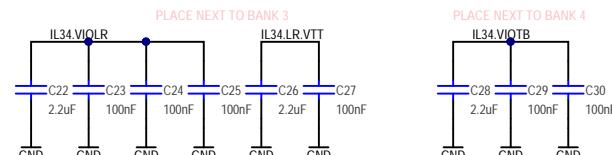
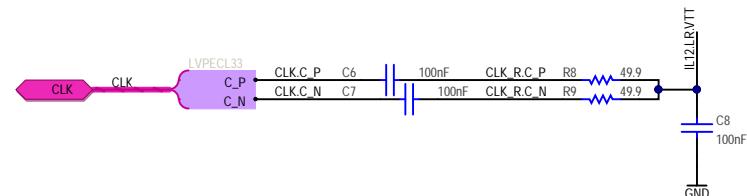
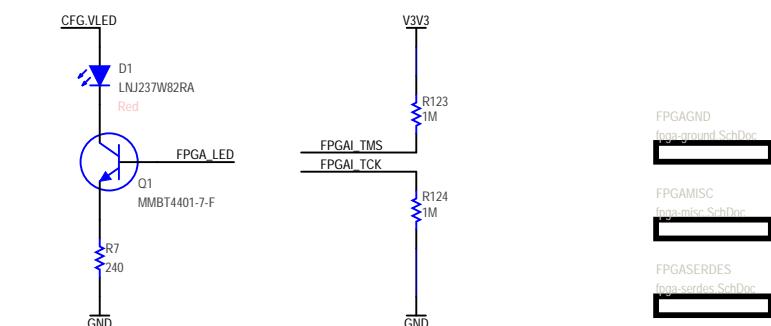
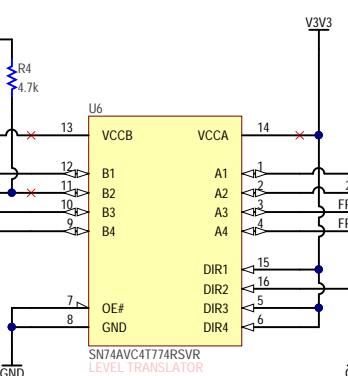
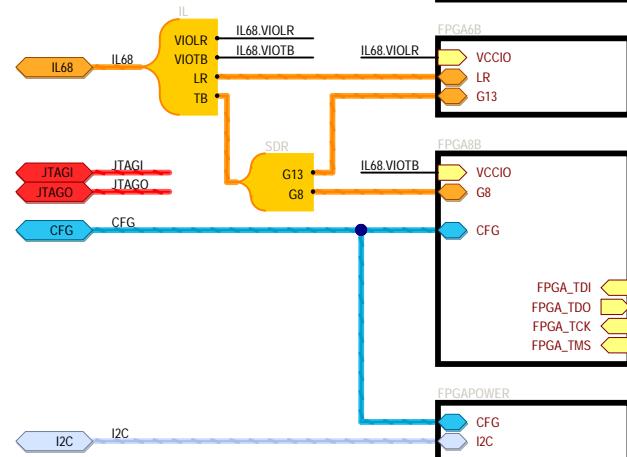


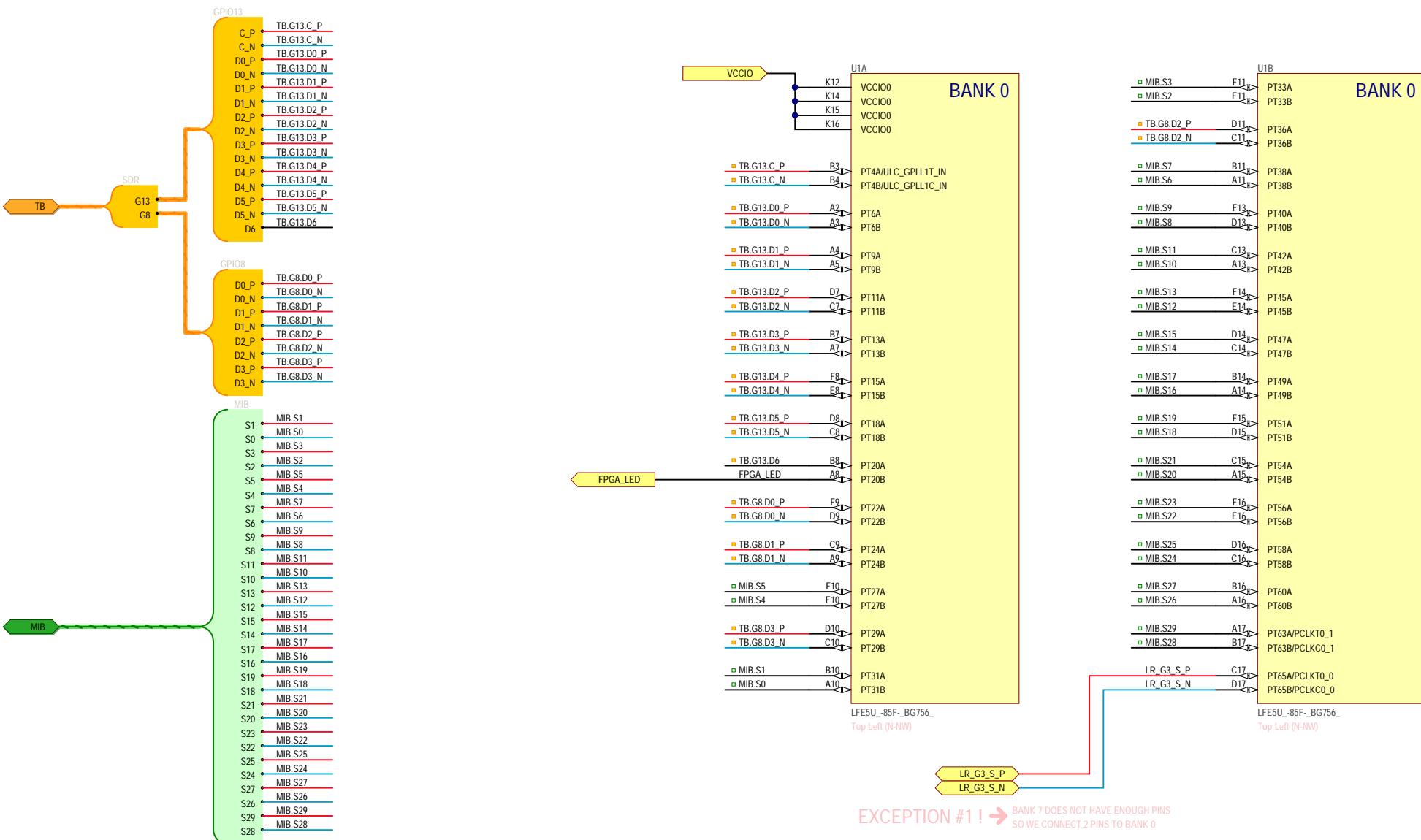
EXCEPTION #2 !

BANK 4 DOES NOT HAVE CLOCK INPUT SO
WE CONNECT BANK 4 CLOCK TO BANK 3



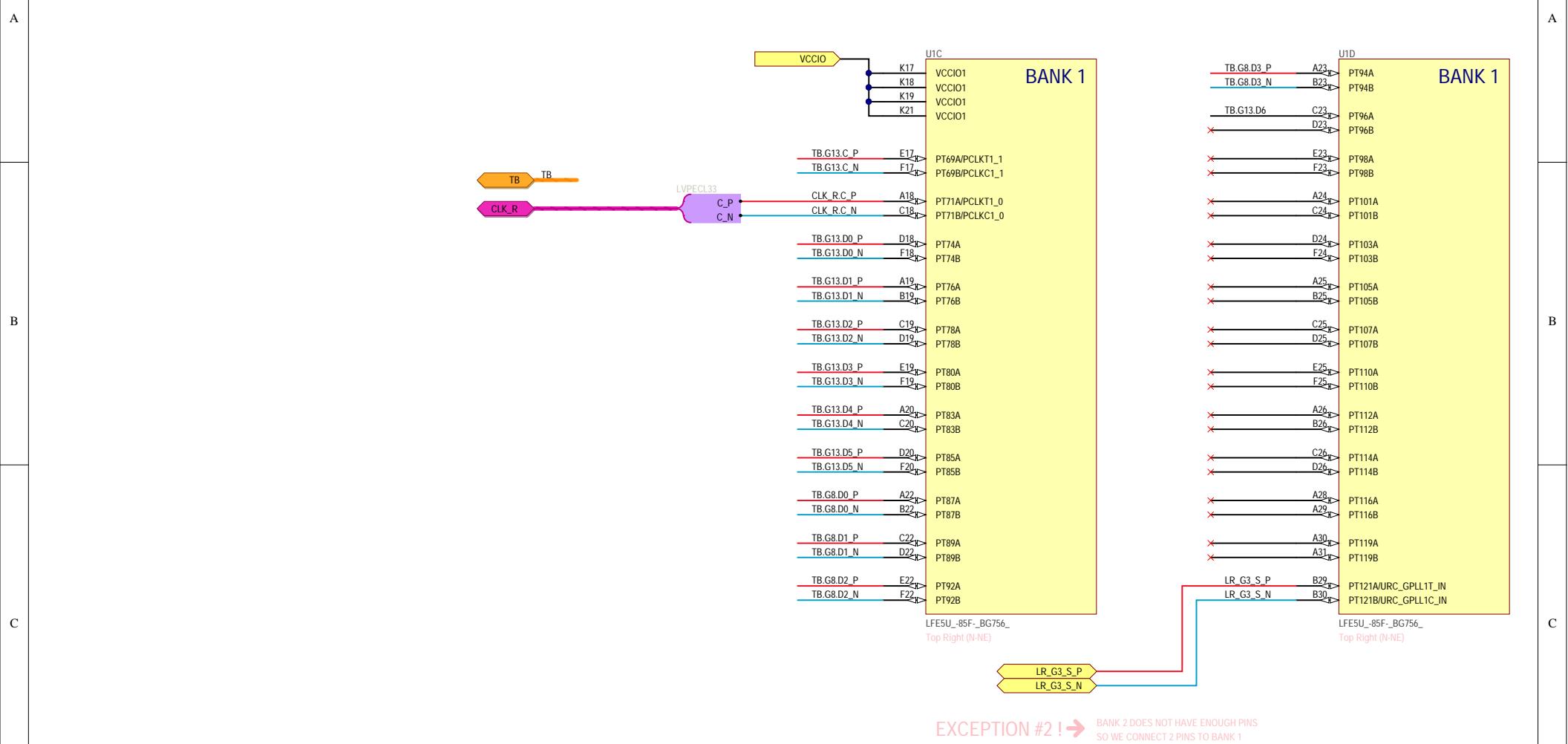
EXCEPTION #3 !

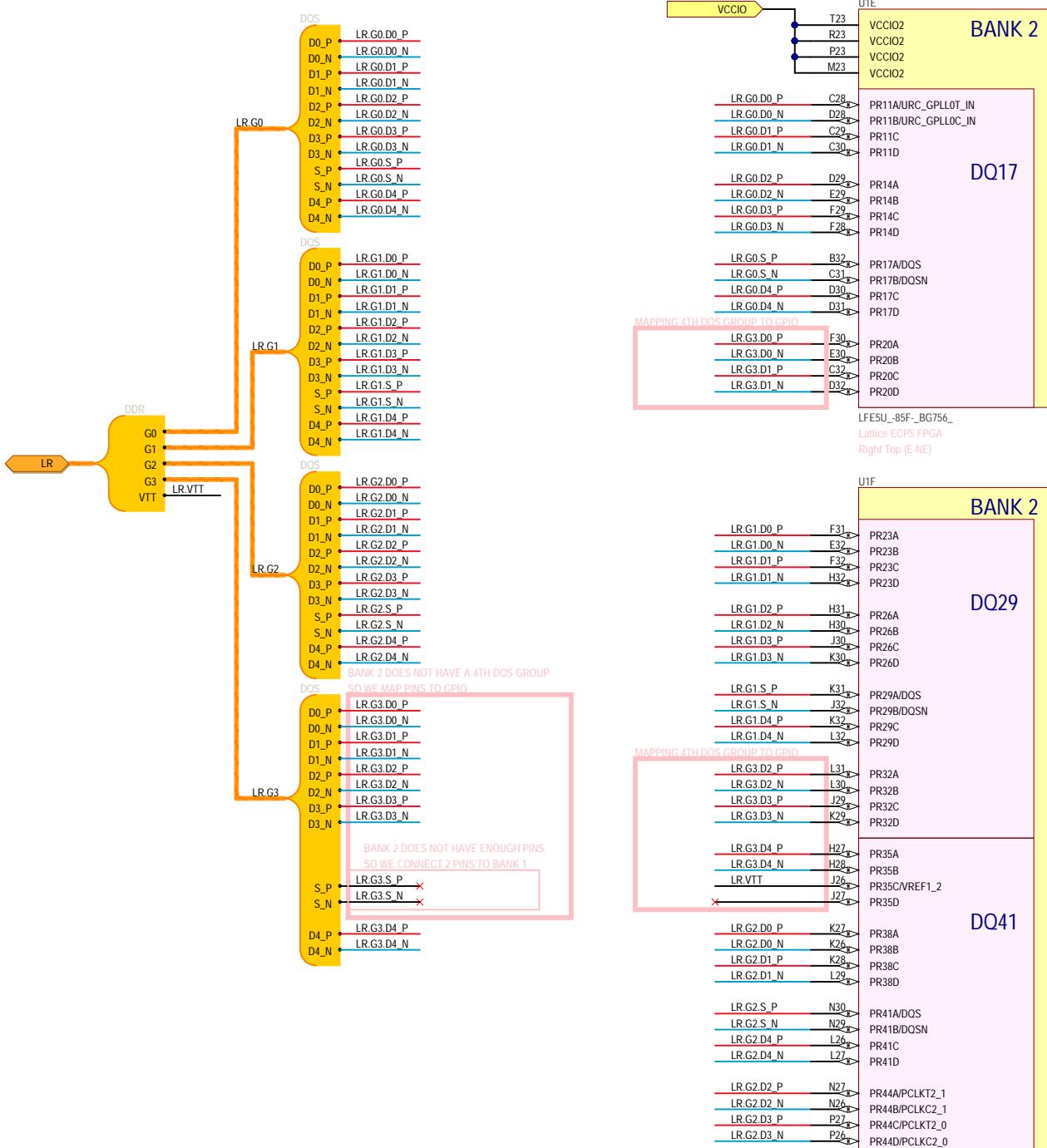




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Title	CS - FPGA - Bank 0		
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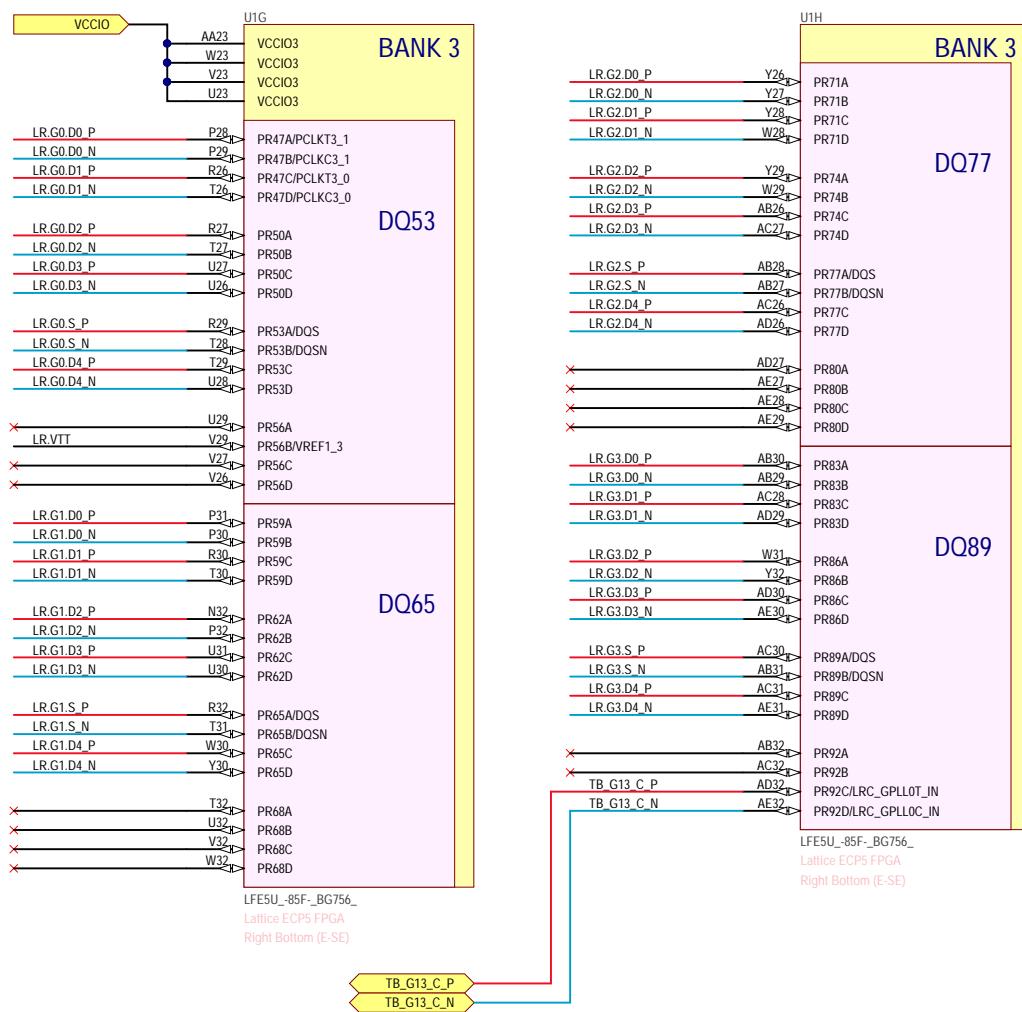


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A

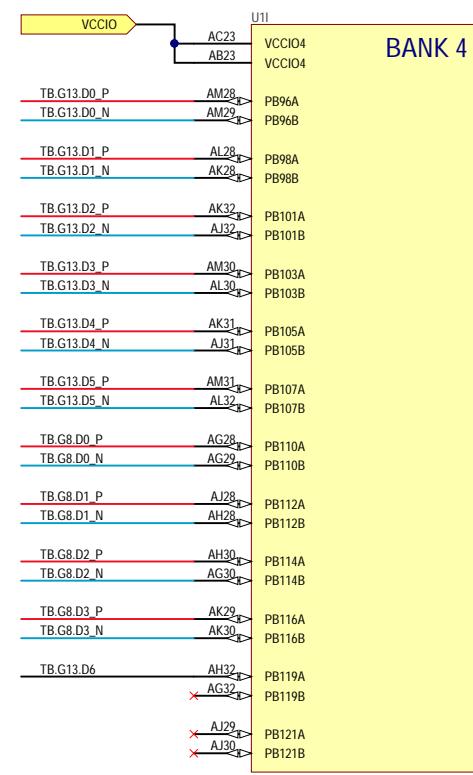
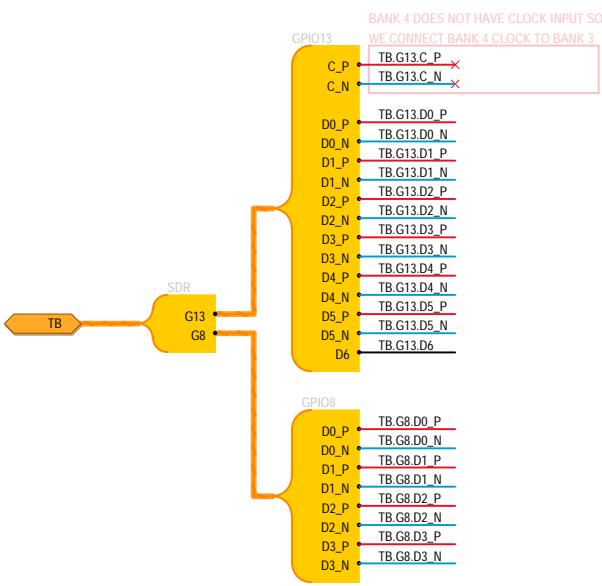


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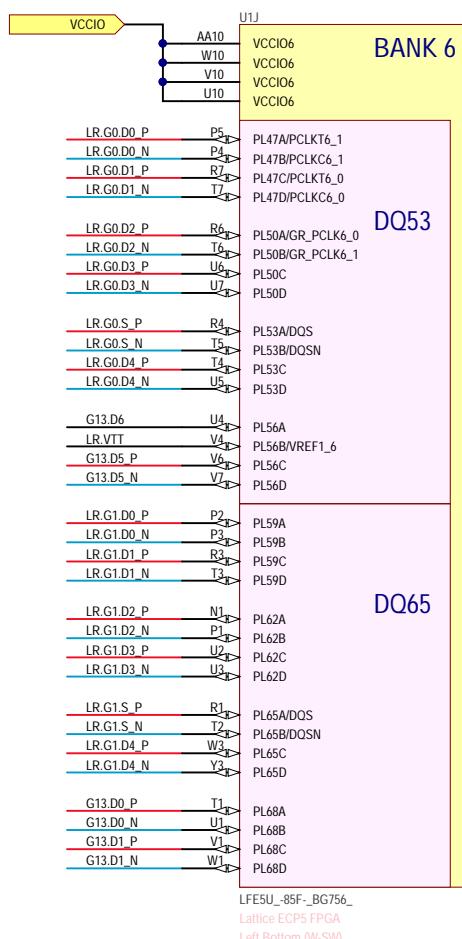
C

D



LFE5U-85F-BG756-
Lattice ECP5 FPGA
Right Bottom (S-SE)

A



G13 G13
LR LR

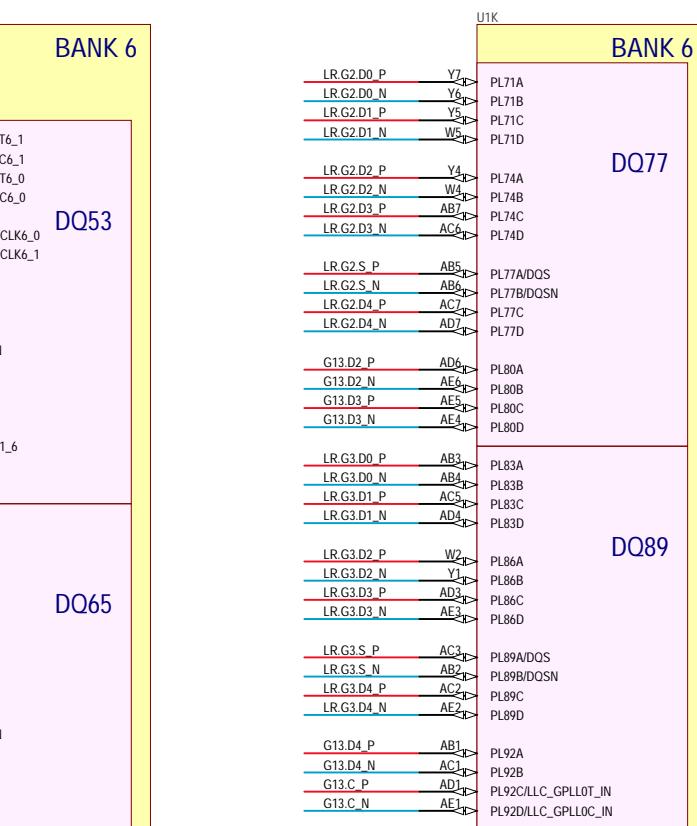
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Title
CS - FPGA - Bank 6

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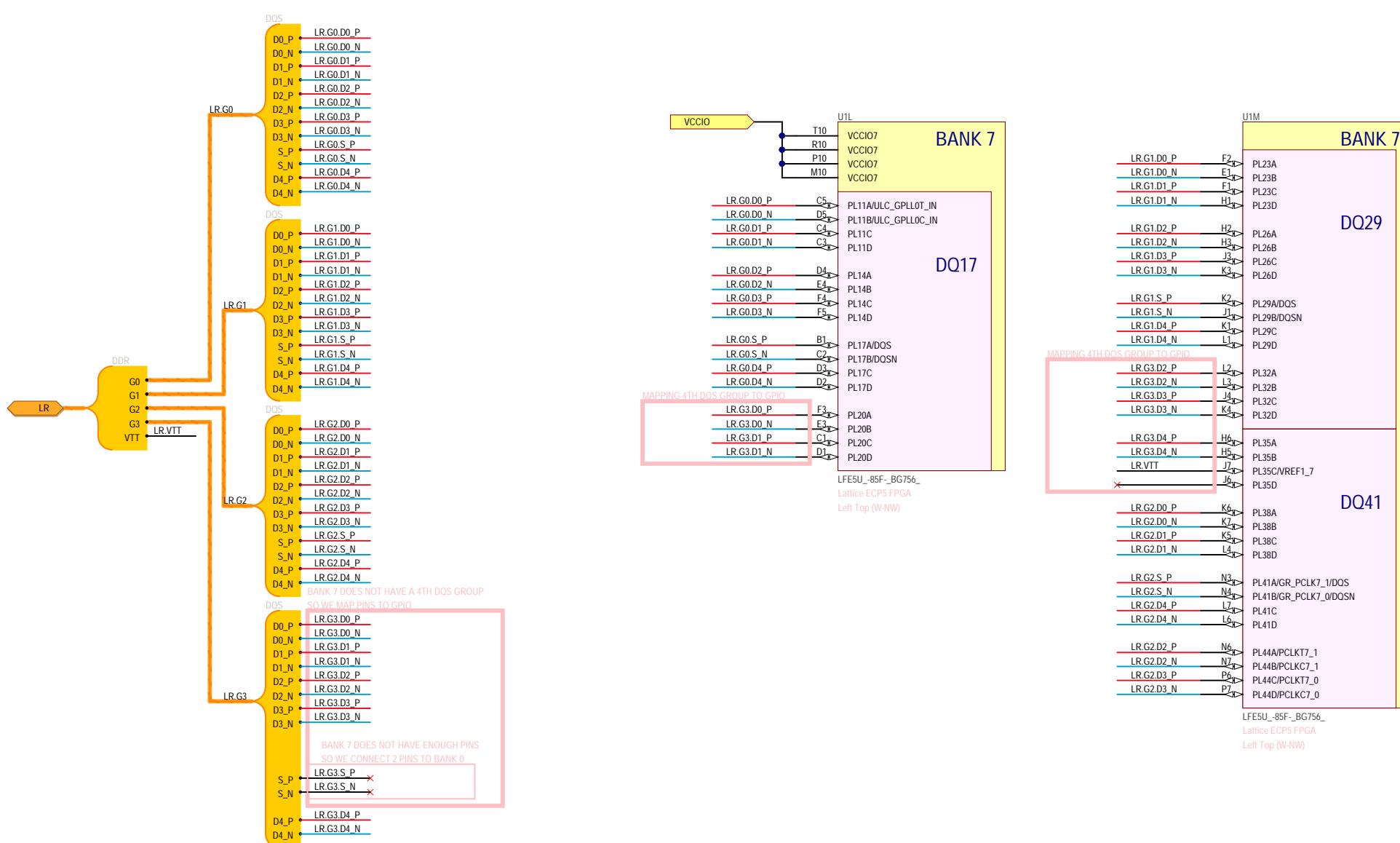
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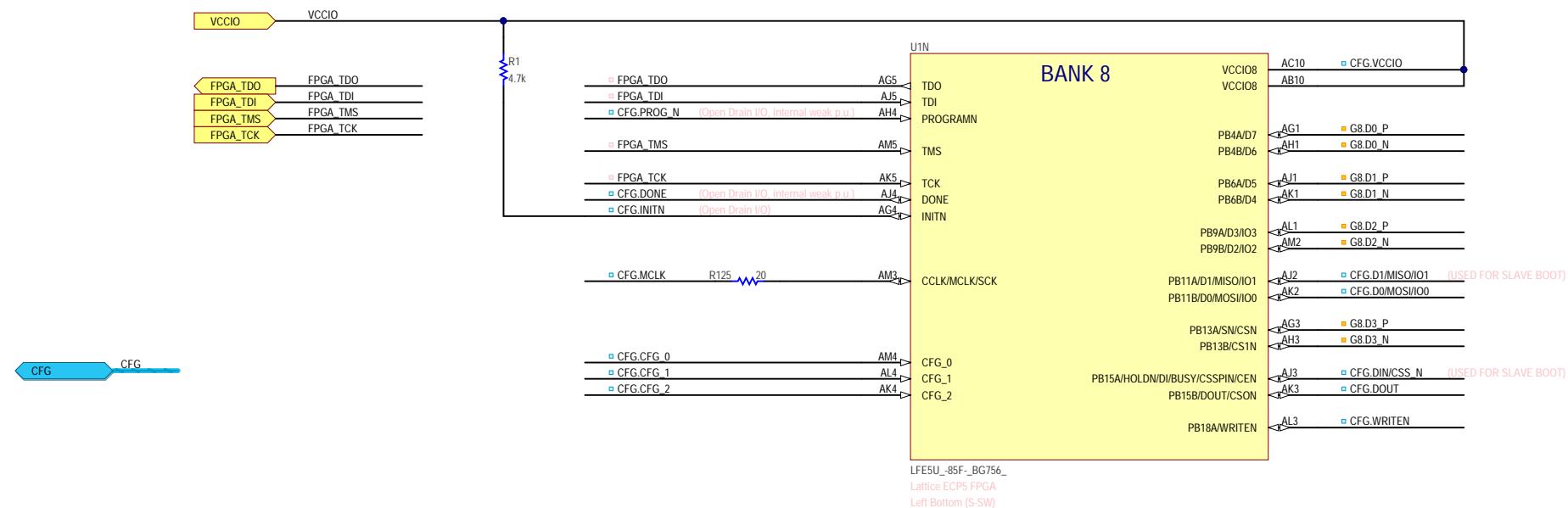
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C

D



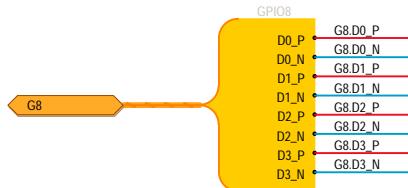
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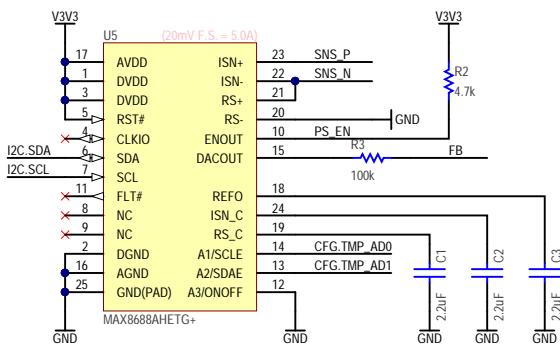


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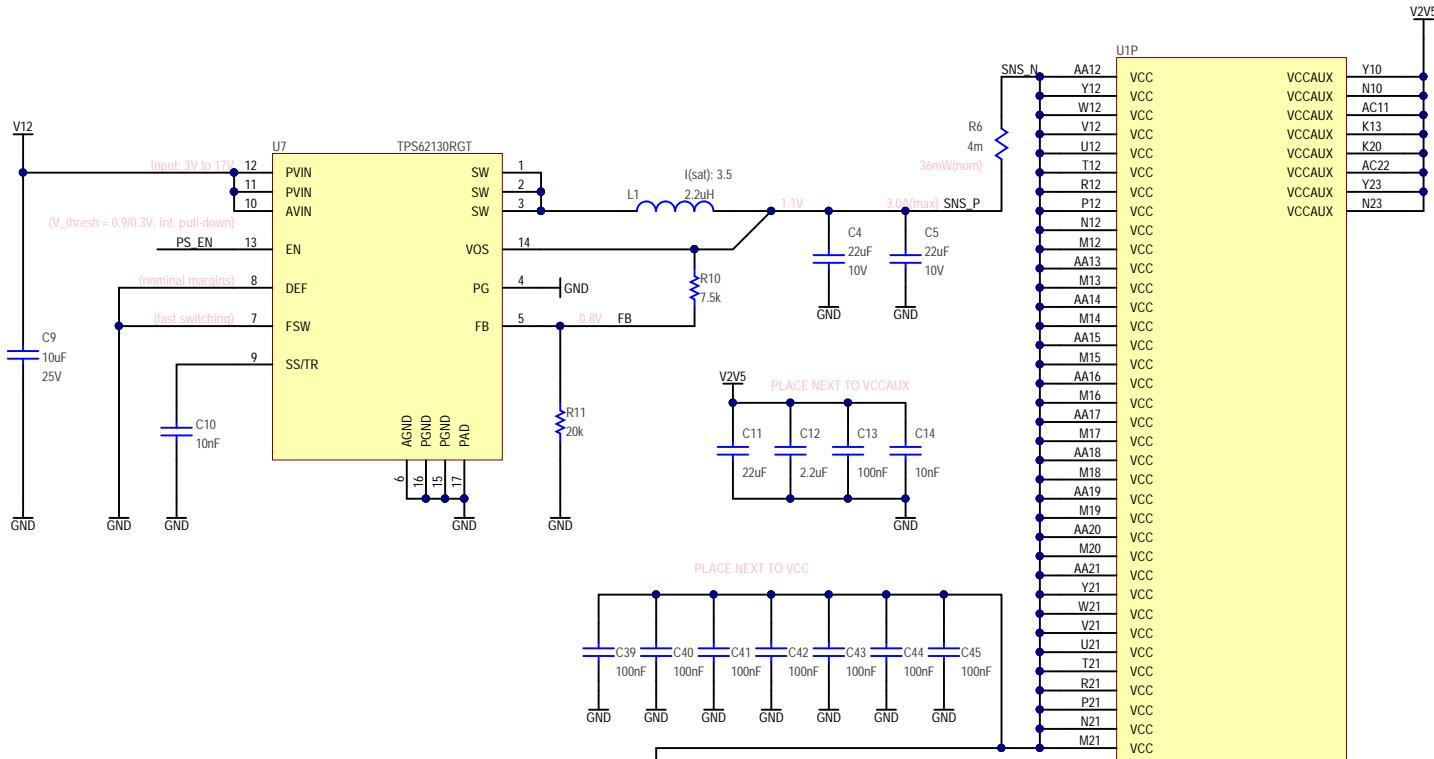
C

D



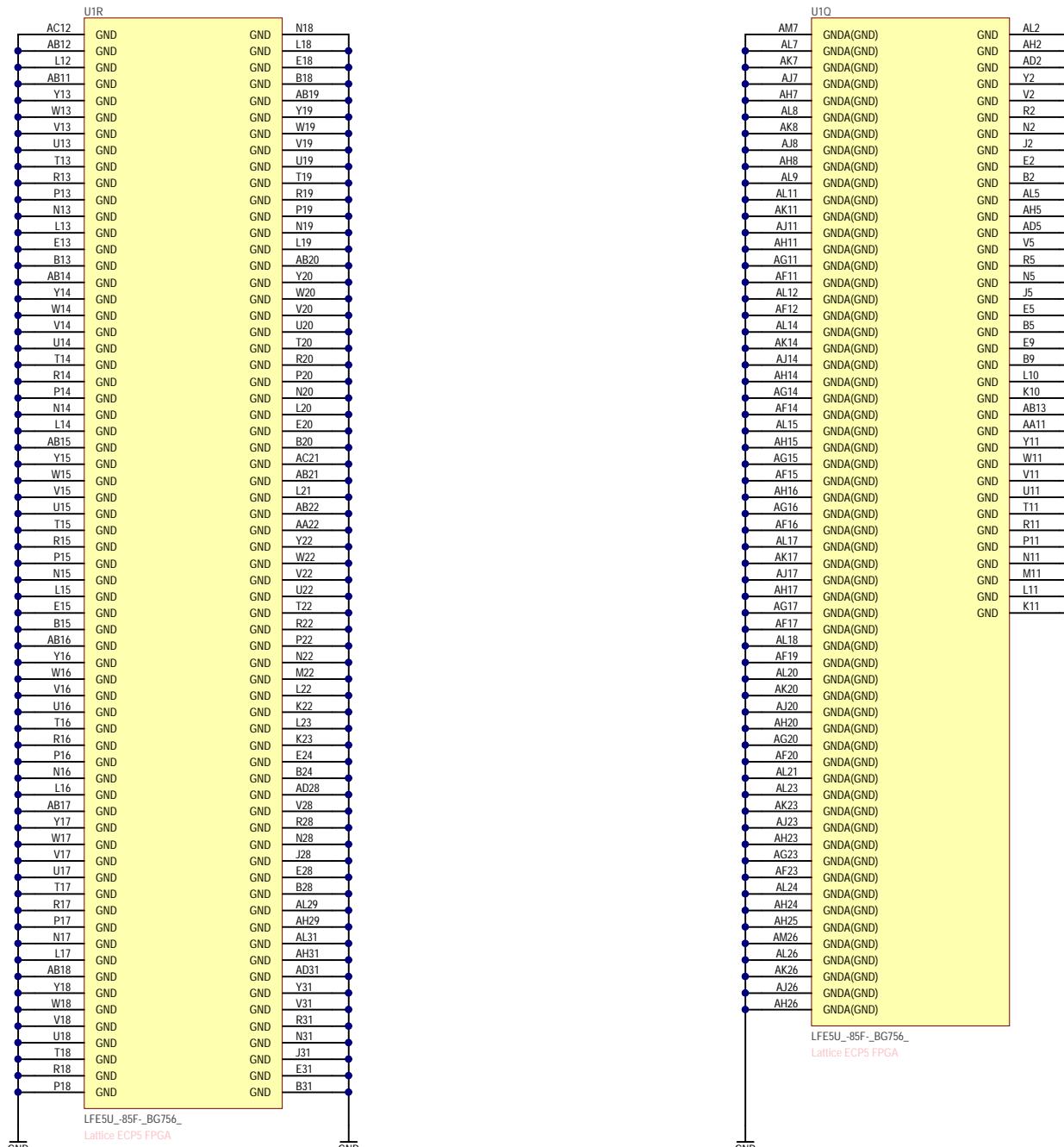


The diagram illustrates the connection between the I₂C bus and the CFG pin. The I₂C bus (SCL and SDA) is connected to the CFG pin via a logic inverter labeled I₂C-3V3.



LFE5U -85F- BG/56

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A

A

B

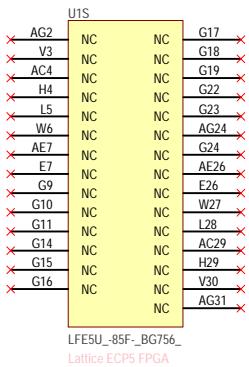
B

C

C

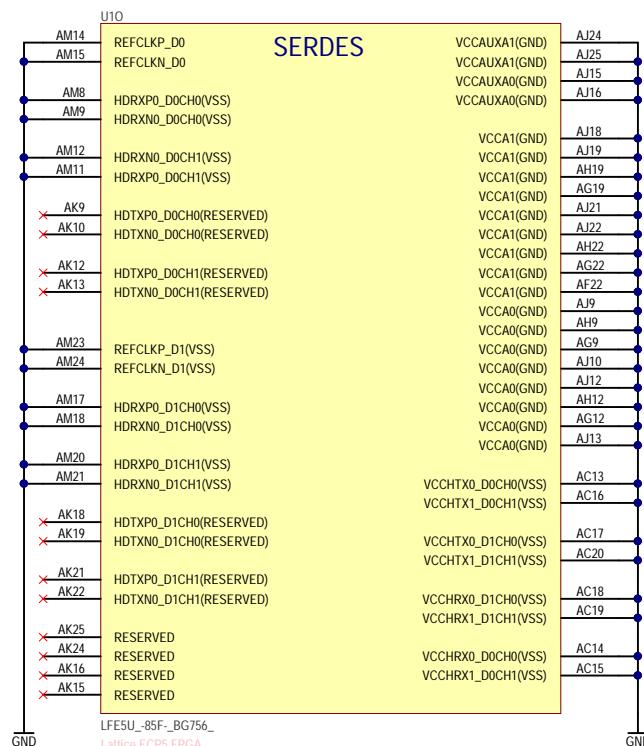
D

D



Title
CS - FPGA - Misc

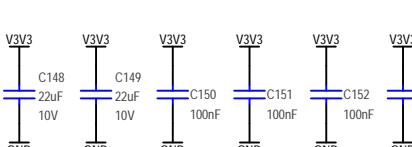
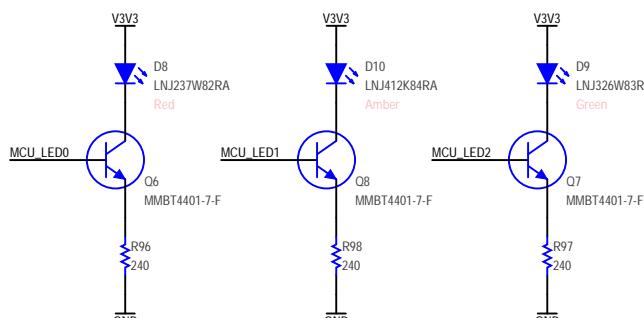
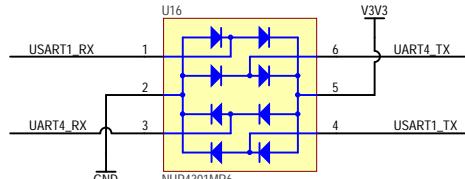
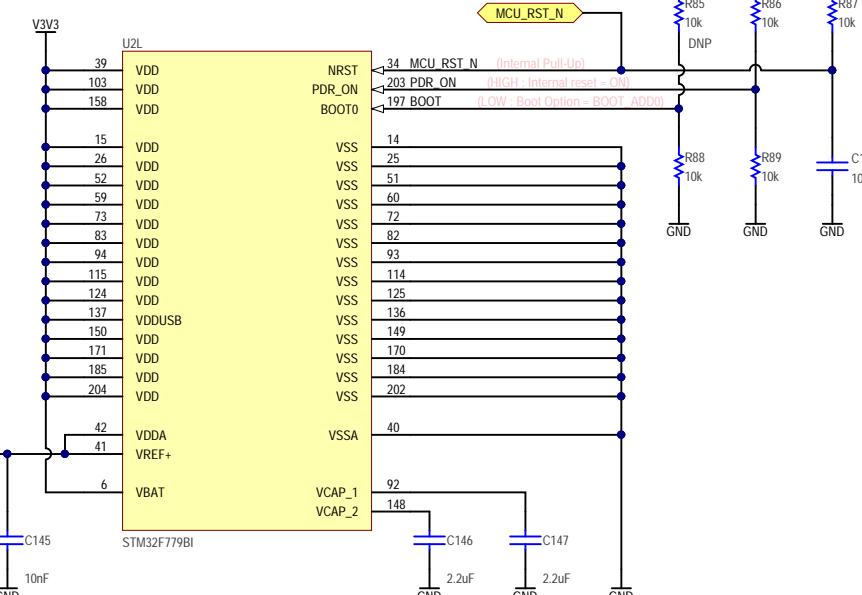
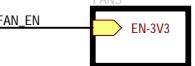
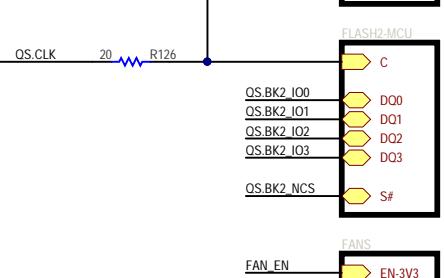
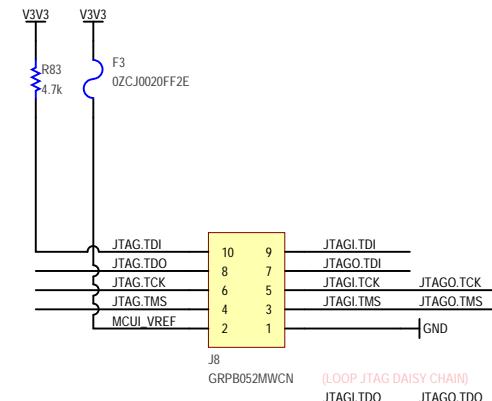
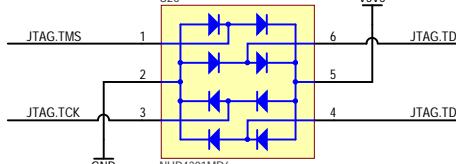
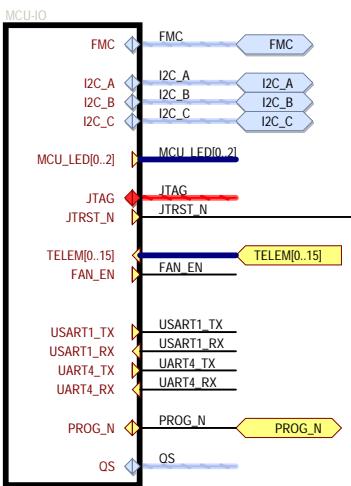
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Title CS - FPGA - SERDES

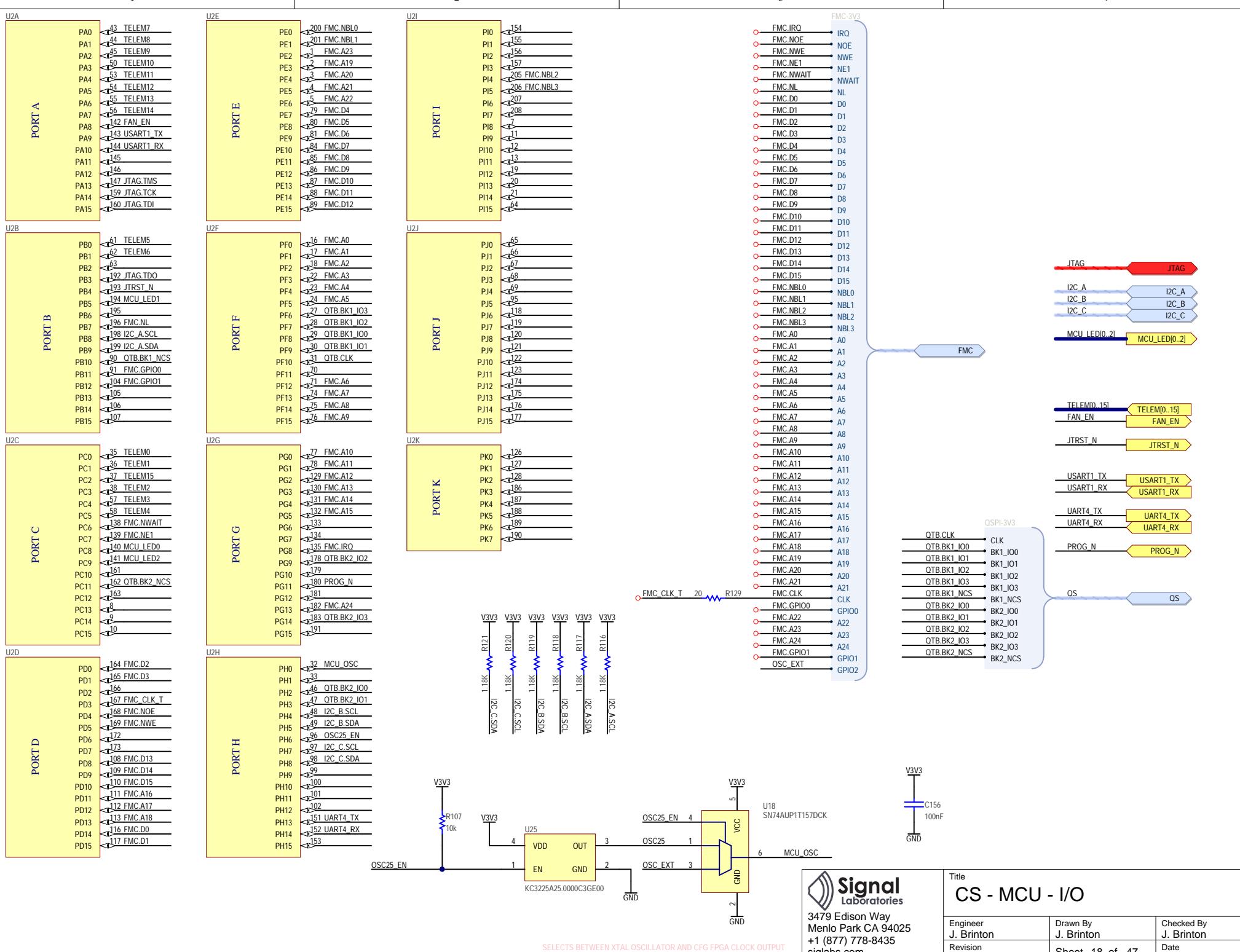
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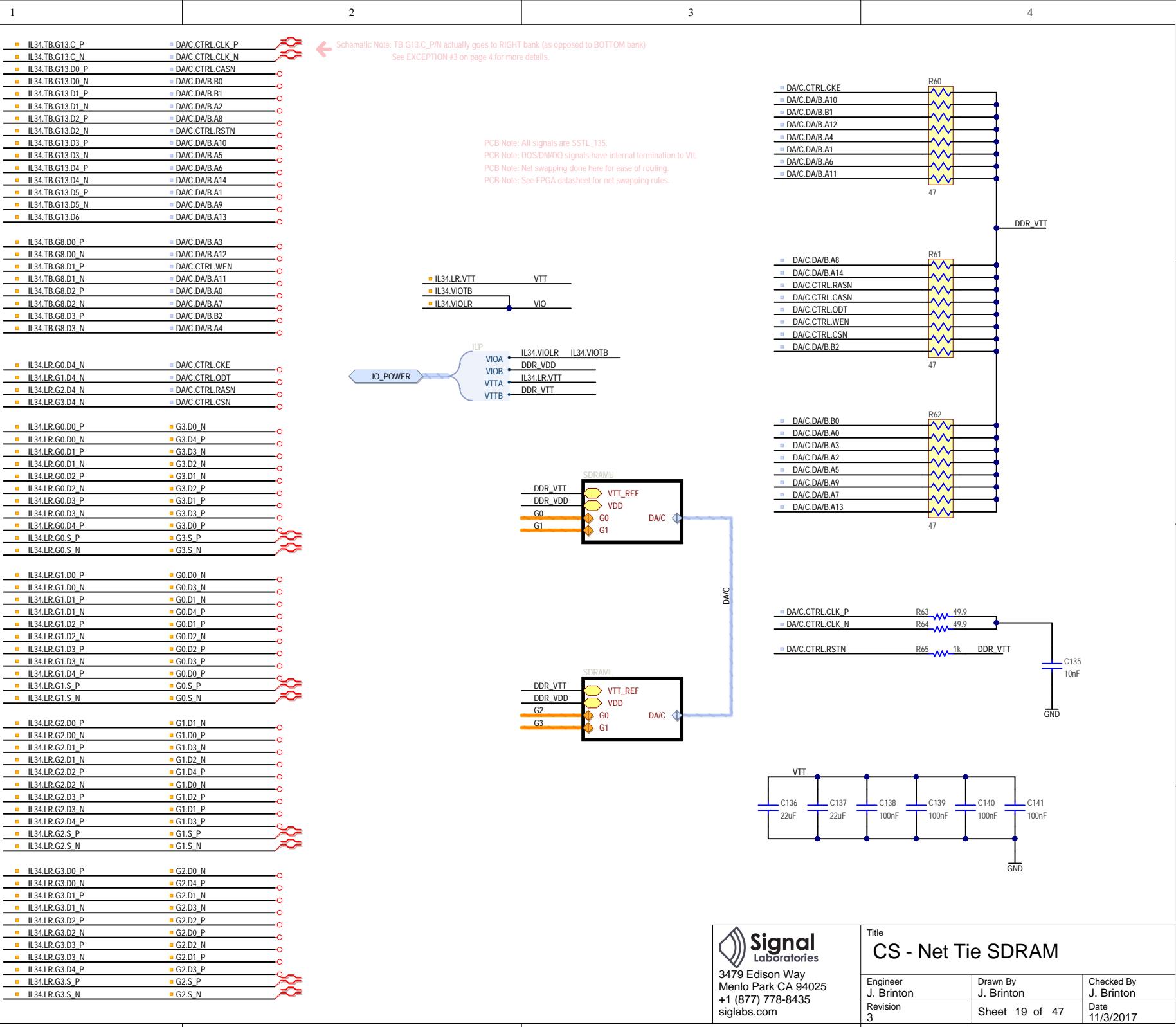


CS - MCU

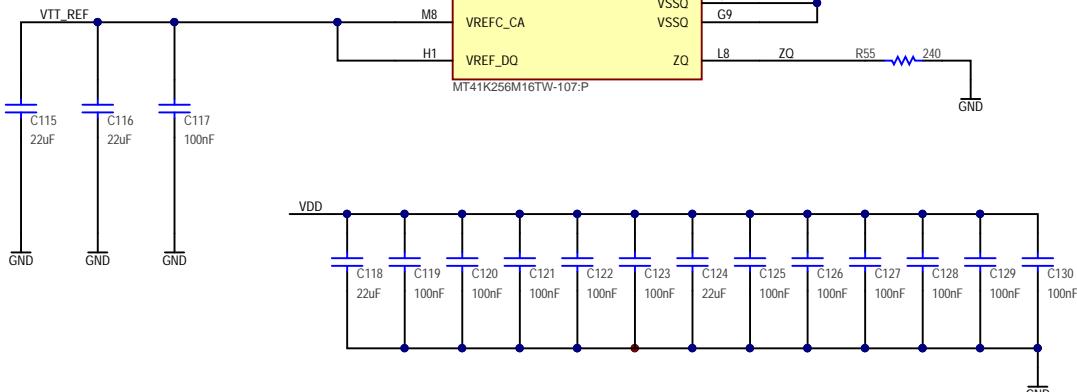
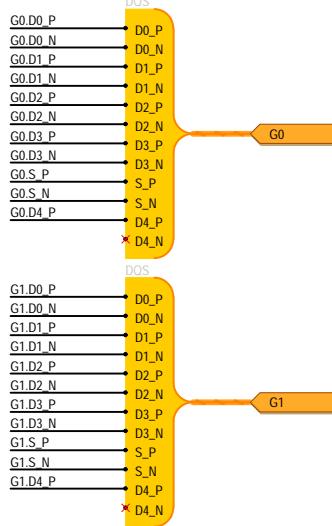
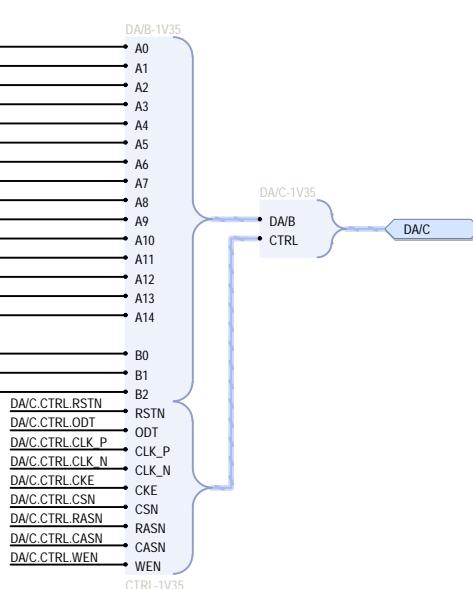
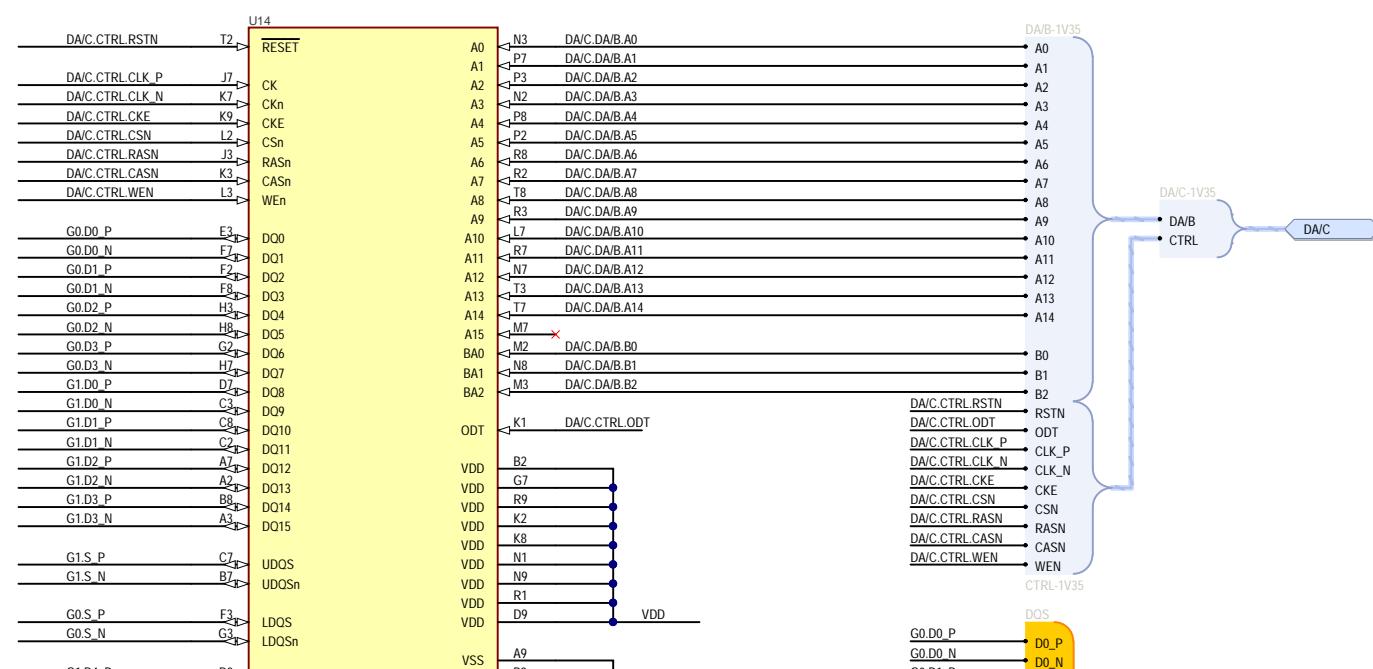
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IL12.TB.G13.D0_P	CFG10.MCLK
IL12.TB.G13.D0_N	CFG10.PROG_N
IL12.TB.G13.D1_P	CFG10.DIN/CSS_N
IL12.TB.G13.D1_N	CFG10.DONE
IL12.TB.G13.D2_P	CFG10.DONE
IL12.TB.G13.D2_N	CFG10.DONE
IL12.TB.G13.D3_P	CFG00.DONE
IL12.TB.G13.D3_N	CFG10.INITN
IL12.TB.G13.D4_P	CFG10.DONE
IL12.TB.G13.D4_N	CFG00.MCLK
IL12.TB.G13.D5_P	CFG00.DOUT
IL12.TB.G13.D5_N	CFG00.PROG_N
IL12.TB.G13.D6_P	CFG00.DIN/CSS_N
IL12.TB.G13.C_P	CFG10.DONE
IL12.TB.G13.C_N	CFG10.DONE
IL12.TB.G8.D0_P	CFG10.DONE
IL12.TB.G8.D0_N	CFG10.DONE
IL12.TB.G8.D1_P	CFG10.DONE
IL12.TB.G8.D1_N	CFG10.DONE
IL12.TB.G8.D2_P	CFG10.DONE
IL12.TB.G8.D2_N	CFG10.DONE
IL12.TB.G8.D3_P	CFG10.DONE
IL12.TB.G8.D3_N	CFG10.DONE
IL12.R.G3.S_P	see exception (page 4)
IL12.R.G3.S_N	see exception (page 4)
IL12.VIOTB	CFG00.VCCIO

CONFIG FPGA "BANK 1"

IL34.TB.G13.D0_P	CFG20.MCLK
IL34.TB.G13.D0_N	CFG20.PROG_N
IL34.TB.G13.D1_P	CFG20.DONE
IL34.TB.G13.D1_N	CFG20.DIN/CSS_N
IL34.TB.G13.D2_P	CFG20.DONE
IL34.TB.G13.D2_N	CFG20.DIN/CSS_N
IL34.TB.G13.D3_P	CFG20.DONE
IL34.TB.G13.D3_N	CFG20.DONE
IL34.TB.G13.D4_P	CFG20.DONE
IL34.TB.G13.D4_N	CFG20.DONE
IL34.TB.G13.D5_P	CFG30.INITN
IL34.TB.G13.D5_N	CFG30.MCLK
IL12.TB.G13.C_P	CFG20.DONE
IL12.TB.G13.C_N	CFG20.DONE
IL34.TB.G13.D6_P	CFG30.DONE
IL34.TB.G13.D6_N	CFG30.PROG_N
IL34.TB.G13.D7_N	CFG30.DIN/CSS_N
IL34.TB.G13.D8_P	CFG20.INITN
IL34.TB.G13.D8_N	CFG20.DONE
IL34.VIOTR	CFG20.VCCIO

CONFIG FPGA "BANK 4"

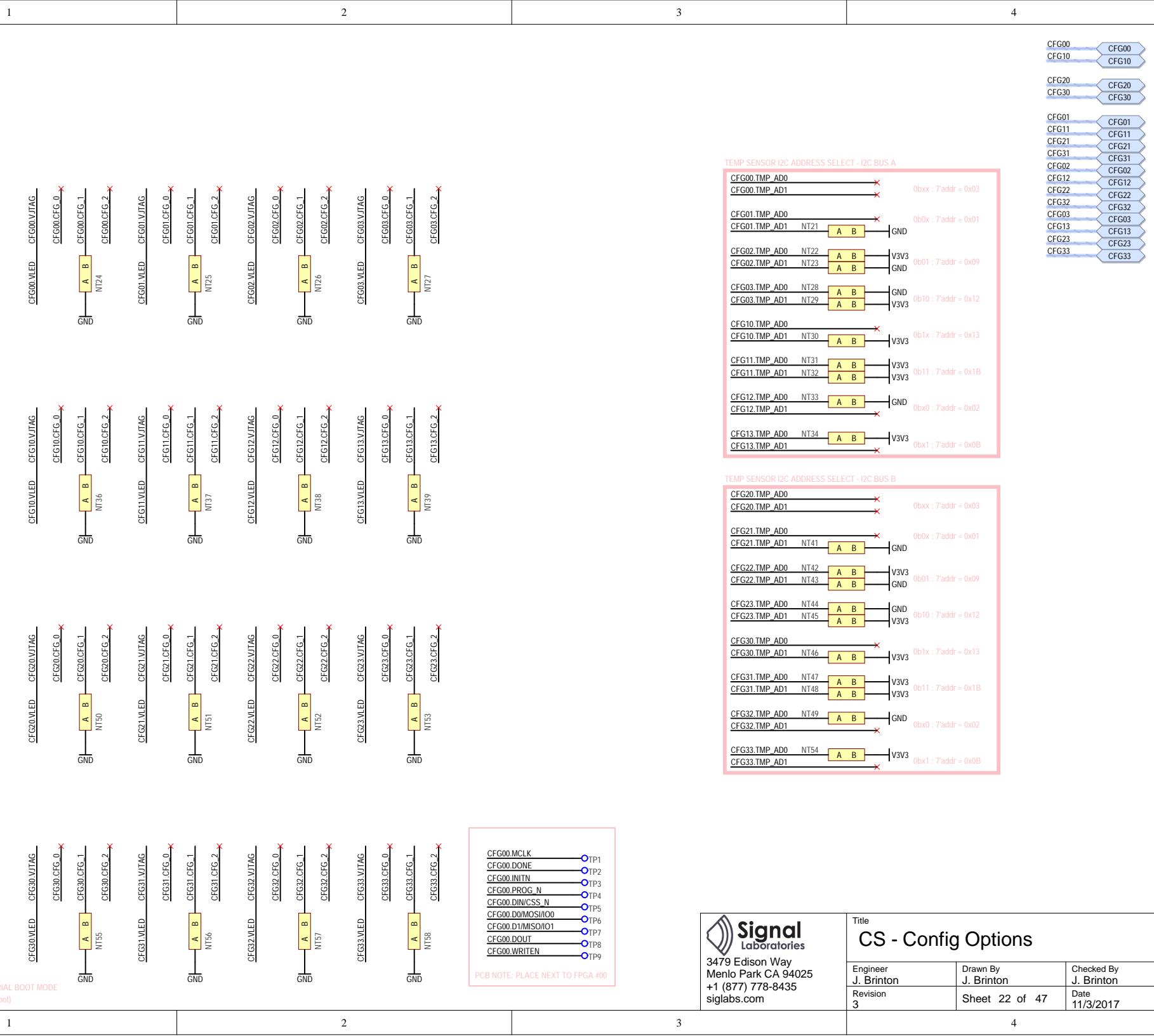
IL07.LR.G0.D0_P	CFG02.MCLK
IL07.LR.G0.D0_N	CFG02.PROG_N
IL07.LR.G0.D1_P	CFG03.DIN/CSS_N
IL07.LR.G0.D1_N	CFG03.INITN
IL07.LR.G0.D2_P	CFG21.INITN
IL07.LR.G0.D2_N	CFG02.DONE
IL07.LR.G0.D3_P	CFG01.MCLK
IL07.LR.G0.D3_N	CFG02.DIN/CSS_N
IL07.LR.G0.D4_P	CFG03.DONE
IL07.LR.G0.D4_N	CFG11.DIN/CSS_N
IL07.LR.G0.S_P	CFG11.DONE
IL07.LR.G0.S_N	CFG11.PROG_N
IL07.LR.G1.D0_P	CFG11.MCLK
IL07.LR.G1.D0_N	CFG21.DONE
IL07.LR.G1.D1_P	CFG21.MCLK
IL07.LR.G1.D1_N	CFG22.PROG_N
IL07.LR.G1.D2_P	CFG22.INITN
IL07.LR.G1.D2_N	CFG01.PROG_N
IL07.LR.G1.D3_P	CFG12.MCLK
IL07.LR.G1.D3_N	CFG12.PROG_N
IL07.LR.G1.D4_P	CFG12.DIN/CSS_N
IL07.LR.G1.D4_N	CFG12.DONE
IL07.LR.G1.S_P	CFG12.DONE
IL07.LR.G1.S_N	CFG13.DIN/CSS_N
IL07.LR.G2.D0_P	CFG33.DIN/CSS_N
IL07.LR.G2.D0_N	CFG33.PROG_N
IL07.LR.G2.D1_P	CFG31.INITN
IL07.LR.G2.D1_N	CFG13.MCLK
IL07.LR.G2.D2_P	CFG13.DONE
IL07.LR.G2.D2_N	CFG13.PROG_N
IL07.LR.G2.D3_P	CFG33.DIN/CSS_N
IL07.LR.G2.D3_N	CFG33.MCLK
IL07.LR.G2.D4_P	CFG31.DONE
IL07.LR.G2.D4_N	CFG31.DIN/CSS_N
IL07.LR.G2.D5_P	CFG31.DONE
IL07.LR.G2.D5_N	CFG31.DIN/CSS_N
IL07.LR.G2.D6_P	CFG31.DONE
IL07.LR.G2.D6_N	CFG31.DIN/CSS_N
IL07.LR.G2.D7_P	CFG31.DONE
IL07.LR.G2.D7_N	CFG31.DIN/CSS_N
IL07.LR.G2.D8_P	CFG31.DONE
IL07.LR.G2.D8_N	CFG31.DIN/CSS_N
IL07.LR.G2.D9_P	CFG31.DONE
IL07.LR.G2.D9_N	CFG31.DIN/CSS_N
IL07.LR.G2.DA_P	CFG31.DONE
IL07.LR.G2.DA_N	CFG31.DIN/CSS_N
IL07.LR.G2.DB_P	CFG31.DONE
IL07.LR.G2.DB_N	CFG31.DIN/CSS_N
IL07.LR.G2.DC_P	CFG31.DONE
IL07.LR.G2.DC_N	CFG31.DIN/CSS_N
IL07.LR.G2.DD_P	CFG31.DONE
IL07.LR.G2.DD_N	CFG31.DIN/CSS_N
IL07.LR.G2.DE_P	CFG31.DONE
IL07.LR.G2.DE_N	CFG31.DIN/CSS_N
IL07.LR.G2.DF_P	CFG31.DONE
IL07.LR.G2.DF_N	CFG31.DIN/CSS_N
IL07.LR.G2.DG_P	CFG31.DONE
IL07.LR.G2.DG_N	CFG31.DIN/CSS_N
IL07.LR.G2.DH_P	CFG31.DONE
IL07.LR.G2.DH_N	CFG31.DIN/CSS_N
IL07.LR.G2.DI_P	CFG31.DONE
IL07.LR.G2.DI_N	CFG31.DIN/CSS_N
IL07.LR.G2.DJ_P	CFG31.DONE
IL07.LR.G2.DJ_N	CFG31.DIN/CSS_N
IL07.LR.G2.DK_P	CFG31.DONE
IL07.LR.G2.DK_N	CFG31.DIN/CSS_N
IL07.LR.G2.DL_P	CFG31.DONE
IL07.LR.G2.DL_N	CFG31.DIN/CSS_N
IL07.LR.G2.DM_P	CFG31.DONE
IL07.LR.G2.DM_N	CFG31.DIN/CSS_N
IL07.LR.G2.DN_P	CFG31.DONE
IL07.LR.G2.DN_N	CFG31.DIN/CSS_N
IL07.LR.G2.DO_P	CFG31.DONE
IL07.LR.G2.DO_N	CFG31.DIN/CSS_N
IL07.LR.G2.DP_P	CFG31.DONE
IL07.LR.G2.DP_N	CFG31.DIN/CSS_N
IL07.LR.G2.DQ_P	CFG31.DONE
IL07.LR.G2.DQ_N	CFG31.DIN/CSS_N
IL07.LR.G2.DR_P	CFG31.DONE
IL07.LR.G2.DR_N	CFG31.DIN/CSS_N
IL07.LR.G2.DS_P	CFG31.DONE
IL07.LR.G2.DS_N	CFG31.DIN/CSS_N
IL07.LR.G2.DT_P	CFG31.DONE
IL07.LR.G2.DT_N	CFG31.DIN/CSS_N
IL07.LR.G2.DU_P	CFG31.DONE
IL07.LR.G2.DU_N	CFG31.DIN/CSS_N
IL07.LR.G2.DV_P	CFG31.DONE
IL07.LR.G2.DV_N	CFG31.DIN/CSS_N
IL07.LR.G2.DW_P	CFG31.DONE
IL07.LR.G2.DW_N	CFG31.DIN/CSS_N
IL07.LR.G2.DX_P	CFG31.DONE
IL07.LR.G2.DX_N	CFG31.DIN/CSS_N
IL07.LR.G2.DY_P	CFG31.DONE
IL07.LR.G2.DY_N	CFG31.DIN/CSS_N
IL07.LR.G2.DZ_P	CFG31.DONE
IL07.LR.G2.DZ_N	CFG31.DIN/CSS_N
IL07.VIOLR	V1V35

IL34.LR.G0.D0_P	CFG20.MCLK
IL34.LR.G0.D0_N	CFG20.PROG_N
IL34.LR.G0.D1_P	CFG20.DONE
IL34.LR.G0.D1_N	CFG20.DIN/CSS_N
IL34.LR.G0.D2_P	CFG20.DONE
IL34.LR.G0.D2_N	CFG20.DIN/CSS_N
IL34.LR.G0.D3_P	CFG20.DONE
IL34.LR.G0.D3_N	CFG20.DONE
IL34.LR.G0.D4_P	CFG20.DONE
IL34.LR.G0.D4_N	CFG20.DONE
IL34.LR.G0.D5_P	CFG20.DONE
IL34.LR.G0.D5_N	CFG20.DONE
IL34.LR.G0.D6_P	CFG20.DONE
IL34.LR.G0.D6_N	CFG20.DONE
IL34.LR.G0.D7_P	CFG20.DONE
IL34.LR.G0.D7_N	CFG20.DONE
IL34.LR.G0.D8_P	CFG20.DONE
IL34.LR.G0.D8_N	CFG20.DONE
IL34.LR.G0.D9_P	CFG20.DONE
IL34.LR.G0.D9_N	CFG20.DONE
IL34.VIOLR	CFG20.VCCIO

COLORED BLOCKS REPRESENT
DIFFERENT INPUT HARNESSES

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IL68.LR.G0.D0_N	MIB33I.S14
IL68.LR.G0.D1_P	MIB33I.S1
IL68.LR.G0.D1_N	MIB33I.S0
IL68.LR.G0.D2_P	MIB33I.S3
IL68.LR.G0.D2_N	MIB33I.S2
IL68.LR.G0.D3_P	MIB33I.S5
IL68.LR.G0.D3_N	MIB33I.S4
IL68.LR.G0.D4_P	MIB33I.S7
IL68.LR.G0.D4_N	MIB33I.S6
IL68.LR.G0.D5_P	MIB33I.S9
IL68.LR.G0.D5_N	MIB33I.S8
IL68.LR.G0.D6_P	MIB33I.S11
IL68.LR.G0.D6_N	MIB33I.S10
IL68.LR.G1.D1_P	MIB33I.S13
IL68.LR.G1.D1_N	MIB33I.S12
IL68.LR.G1.D2_P	FMC.D3
IL68.LR.G1.D2_N	FMC.D2
IL68.LR.G1.D3_P	MIB33I.S17
IL68.LR.G1.D3_N	MIB33I.S16
IL68.LR.G1.D4_P	MIB33I.S19
IL68.LR.G1.D4_N	MIB33I.S18
IL68.LR.G1.D5_P	MIB33I.S21
IL68.LR.G1.D5_N	MIB33I.S20
IL68.LR.G2.D0_P	MIB33I.S23
IL68.LR.G2.D0_N	MIB33I.S22
IL68.LR.G2.D1_P	MIB33I.S25
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IL68.LR.G2.D2_P	MIB33I.S27
IL68.LR.G2.D2_N	MIB33I.S26
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IL68.LR.G2.D3_N	MIB33I.S28
IL68.LR.G2.D4_P	MIB33I.S31
IL68.LR.G2.D4_N	MIB33I.S30
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IL68.LR.G2.D6_N	MIB33I.S33
IL68.LR.G2.D7_P	MIB33I.S36
IL68.LR.G2.D7_N	MIB33I.S35
IL68.LR.G2.D8_P	MIB33I.S38
IL68.LR.G2.D8_N	MIB33I.S37
IL68.LR.G2.D9_P	MIB33I.S40
IL68.LR.G2.D9_N	MIB33I.S39
IL68.LR.G2.DA_P	MIB33I.S42
IL68.LR.G2.DA_N	MIB33I.S41
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IL68.LR.G2.DB_N	MIB33I.S43
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IL68.LR.G2.DC_N	MIB33I.S45
IL68.LR.G2.DD_P	MIB33I.S48
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IL68.LR.G2.DE_P	MIB33I.S50
IL68.LR.G2.DE_N	MIB33I.S49
IL68.LR.G2.DF_P	MIB33I.S52
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IL68.LR.G2.DT_P	MIB33I.S80
IL68.LR.G2.DT_N	MIB33I.S79
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IL68.LR.G2.DW_N	MIB33I.S85
IL68.LR.G2.DX_P	MIB33I.S88
IL68.LR.G2.DX_N	MIB33I.S87
IL68.LR.G2.DY_P	MIB33I.S90
IL68.LR.G2.DY_N	MIB33I.S89
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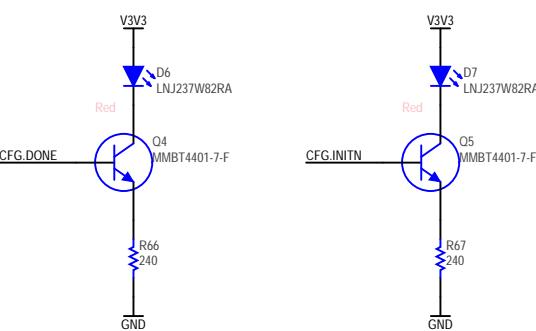
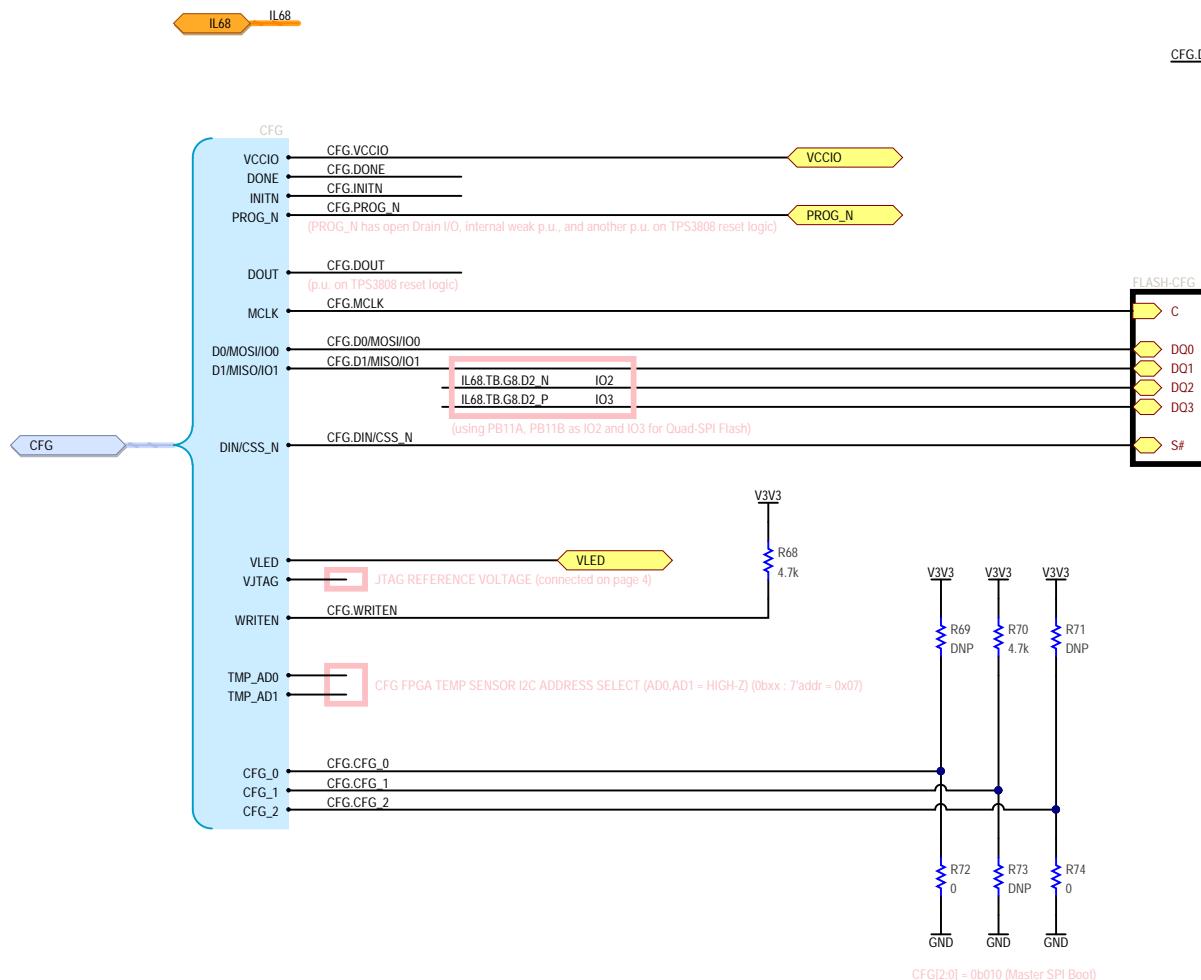
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IL07.TB.G13.DU_P	FMC.D1
IL07.TB.G13.DU_N	FMC.D1
IL07.TB.G13.DV_P	FMC.D1
IL07.TB.G13.DV_N	FMC.D1
IL07.TB.G13.DW_P	FMC.D1</



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CS - Config Options

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	J. Brinton
Revision 3	Sheet 22 of 47	Date 11/3/2017



A

A

B

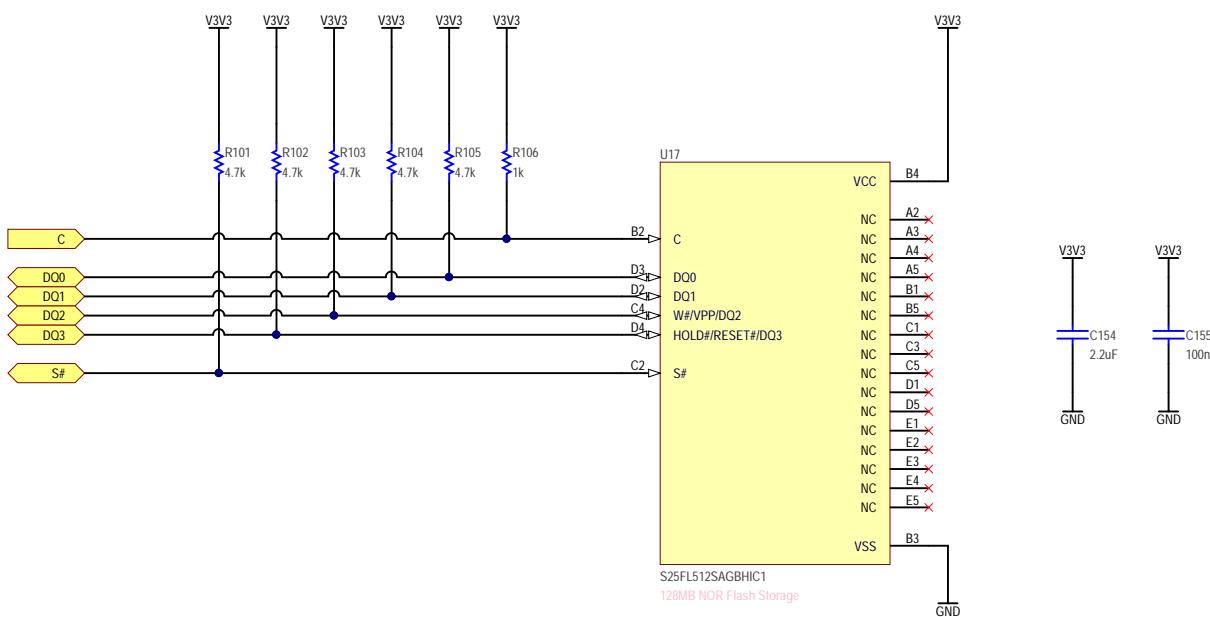
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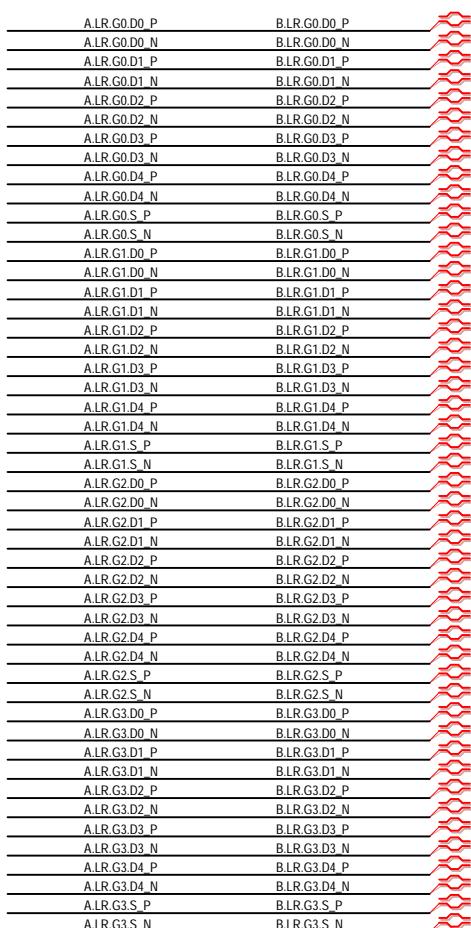
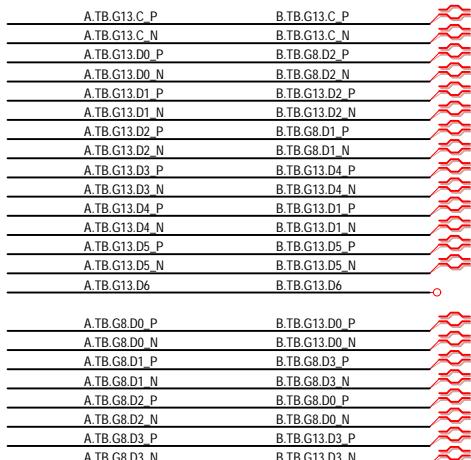
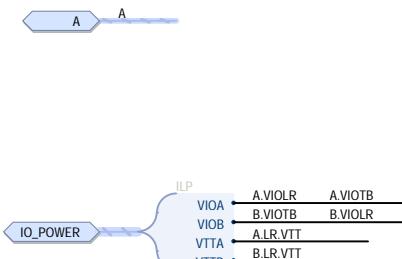
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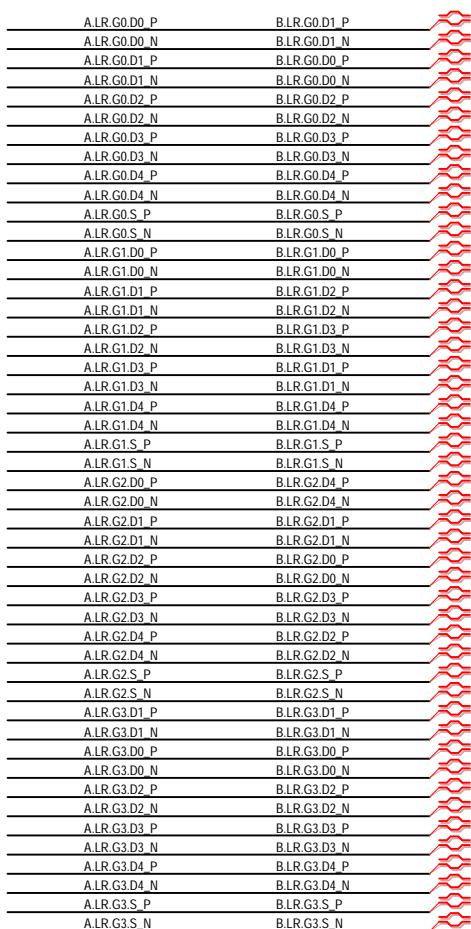
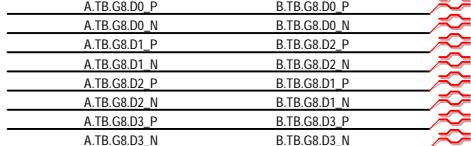
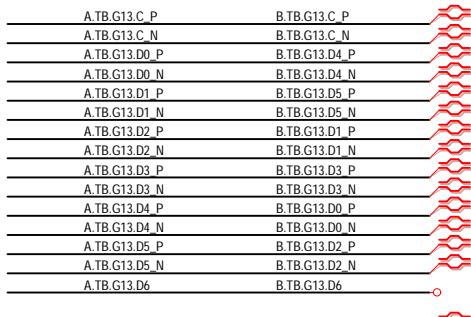
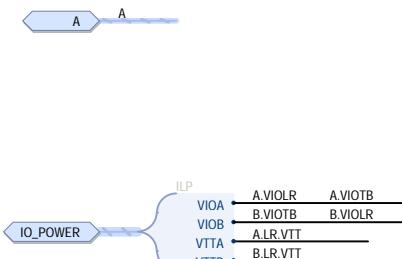
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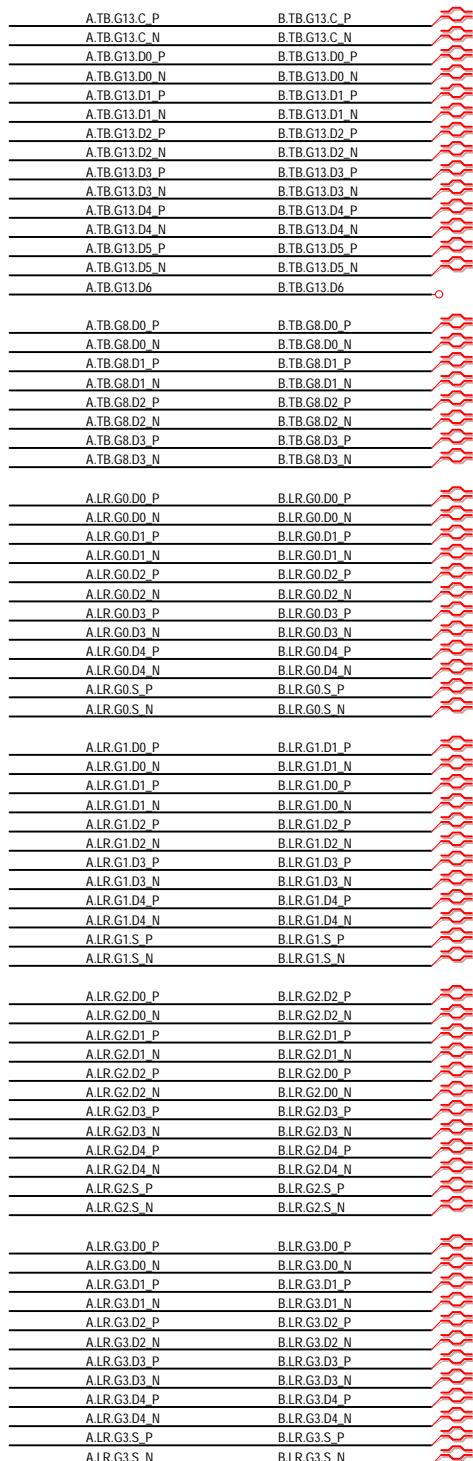
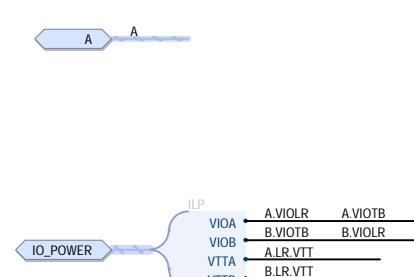


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CS - Net Tie 12:68

Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 3	Sheet 26 of 47	Date 11/3/2017

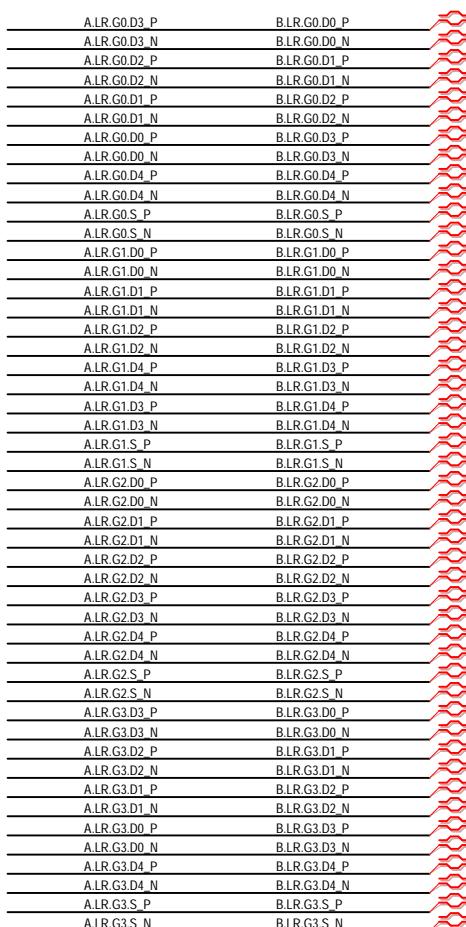
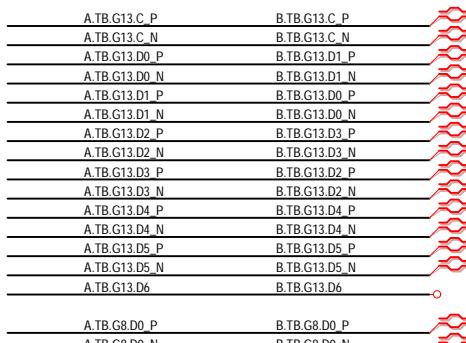
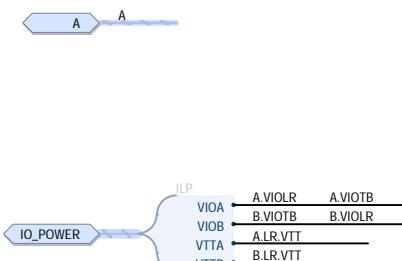


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CS - Net Tie 68:07

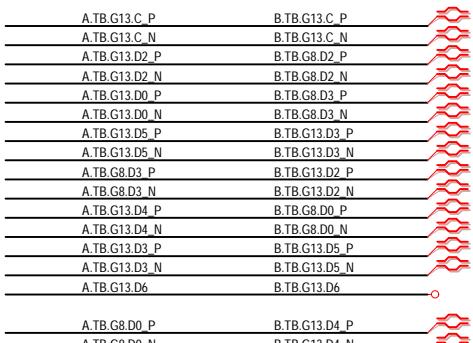
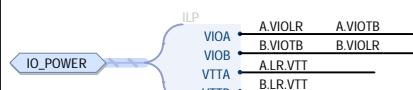
Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 3	Sheet 27 of 47	Date 11/3/2017



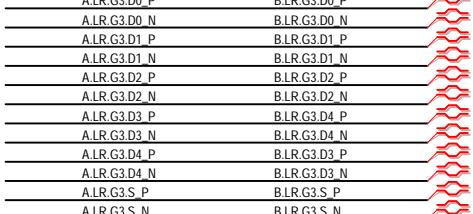
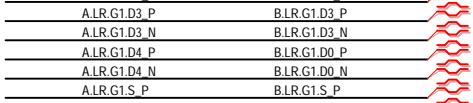
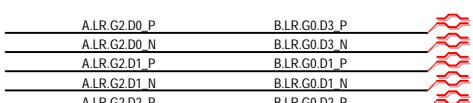
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Title
CS - Net Tie 07:07

Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 3	Sheet 29 of 47	Date 11/3/2017

A

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MIB.S1	IMIB.S5
MIB.S0	IMIB.S22
MIB.S3	IMIB.S16
MIB.S2	IMIB.S7
MIB.S5	IMIB.S1
MIB.S4	IMIB.S20
MIB.S7	IMIB.S2
MIB.S6	IMIB.S19
MIB.S9	IMIB.S17
MIB.S8	IMIB.S26
MIB.S11	IMIB.S29
MIB.S10	IMIB.S23
MIB.S13	IMIB.S14
MIB.S12	IMIB.S15
MIB.S15	IMIB.S12
MIB.S14	IMIB.S13
MIB.S17	IMIB.S9
MIB.S16	IMIB.S3
MIB.S19	IMIB.S6
MIB.S18	IMIB.S27
MIB.S21	IMIB.S28
MIB.S20	IMIB.S4
MIB.S23	IMIB.S10
MIB.S22	IMIB.S0
MIB.S25	IMIB.S24
MIB.S24	IMIB.S25
MIB.S27	IMIB.S18
MIB.S26	IMIB.S8
MIB.S29	IMIB.S11
MIB.S28	IMIB.S21



PIN SWAPPING TO REDUCE ROUTING COMPLEXITY



Title
CS - Net Tie IMIB

Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 3	Sheet 30 of 47	Date 11/3/2017

A

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MIBIA.S1		MIBIB.S1
MIBIA.S0		MIBIB.S0
MIBIA.S3		MIBIB.S3
MIBIA.S2		MIBIB.S2
MIBIA.S5		MIBIB.S5
MIBIA.S4		MIBIB.S4
MIBIA.S7		MIBIB.S7
MIBIA.S6		MIBIB.S6
MIBIA.S9		MIBIB.S9
MIBIA.S8		MIBIB.S8
MIBIA.S11	20	R128
MIBIA.S10		MIBIB.S10
MIBIA.S13		MIBIB.S13
MIBIA.S12		MIBIB.S12
MIBIA.S15		MIBIB.S15
MIBIA.S14		MIBIB.S14
MIBIA.S17		MIBIB.S17
MIBIA.S16		MIBIB.S16
MIBIA.S19		MIBIB.S19
MIBIA.S18		MIBIB.S18
MIBIA.S21		MIBIB.S21
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MIBIA.S22		MIBIB.S22
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MIBIA.S27		MIBIB.S27
MIBIA.S26		MIBIB.S26
MIBIA.S29		MIBIB.S29
MIBIA.S28		MIBIB.S28



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Title
CS - Net Tie MIBT0

Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 3	Sheet 31 of 47	Date 11/3/2017

A

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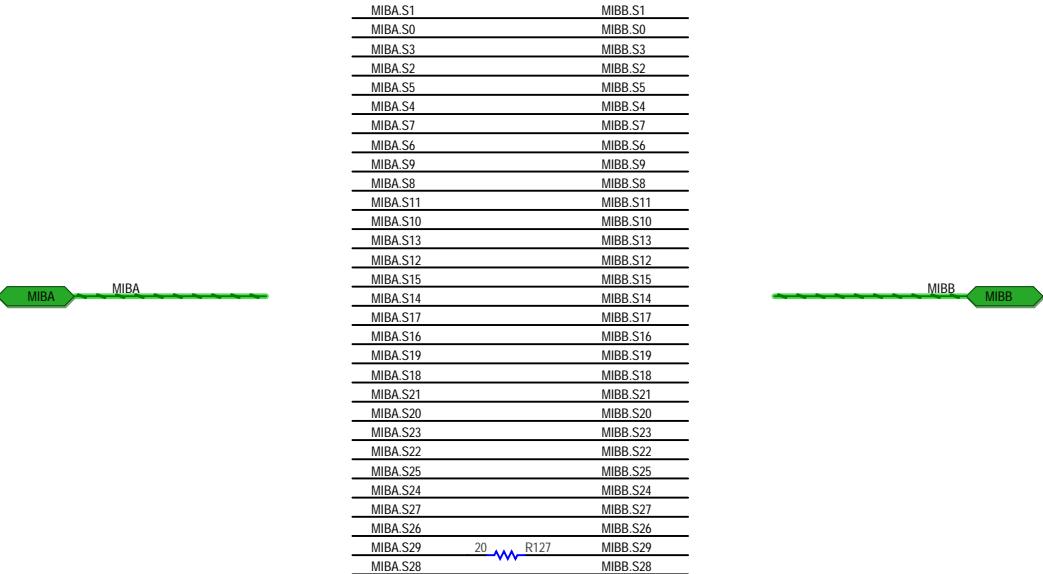
B

C

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CS - Net Tie MIBT1

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	J. Brinton
Revision 3	Sheet 32 of 47	Date 11/3/2017

1

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3

4

J4A
SEAM-40-11.0-S-10-2-A-K-TR

1	GND
2	■ IL0.TB.G13.C_P
3	■ IL0.TB.G13.C_N
4	GND
5	■ IL0.TB.G13.D3_P
6	■ IL0.TB.G13.D3_N
7	GND
8	■ IL0.TB.G13.D1_P
9	■ IL0.TB.G13.D1_N
10	GND
11	GND
12	■ IL0.TB.G13.D2_P
13	■ IL0.TB.G13.D2_N
14	GND
15	■ IL0.TB.G13.D6
16	×
17	GND
18	■ IL0.TB.G13.D0_N
19	■ IL0.TB.G13.D0_P
20	GND
21	GND
22	■ IL0.TB.G13.D5_P
23	■ IL0.TB.G13.D5_N
24	GND
25	■ IL0.TB.G8.D2_N
26	■ IL0.TB.G8.D2_P
27	GND
28	■ IL0.TB.G8.D3_P
29	■ IL0.TB.G8.D3_N
30	GND
31	GND
32	■ IL0.TB.G8.D0_P
33	■ IL0.TB.G8.D0_N
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35	■ IL0.TB.G8.D1_N
36	■ IL0.TB.G8.D1_P
37	GND
38	■ IL0.TB.G13.D4_N
39	■ IL0.TB.G13.D4_P
40	GND
41	GND
42	■ IL0.LR.G0.D2_N
43	■ IL0.LR.G0.D2_P
44	GND
45	■ IL0.LR.G0.D1_P
46	■ IL0.LR.G0.D1_N
47	GND
48	■ IL0.LR.G0.D0_N
49	■ IL0.LR.G0.D0_P
50	GND

60	GND
59	■ IL0.LR.G0.D3_P
58	■ IL0.LR.G0.D3_N
57	GND
56	■ IL0.LR.G0.D4_N
55	■ IL0.LR.G0.D4_P
54	GND
53	■ IL0.LR.G0.S_P
52	■ IL0.LR.G0.S_N
51	GND
61	GND
62	■ IL0.LR.G1.D0_N
63	■ IL0.LR.G1.D0_P
64	GND
65	■ IL0.LR.G1.D2_N
66	■ IL0.LR.G1.D2_P
67	GND
68	■ IL0.LR.G1.D3_N
69	■ IL0.LR.G1.D3_P
70	GND
71	GND
72	■ IL0.LR.G1.D1_N
73	■ IL0.LR.G1.D1_P
74	GND
75	■ IL0.LR.G1.D4_N
76	■ IL0.LR.G1.D4_P
77	GND
78	■ IL0.LR.G1.S_P
79	■ IL0.LR.G1.S_N
80	GND
81	GND
82	■ IL0.LR.G2.D2_P
83	■ IL0.LR.G2.D2_N
84	GND
85	■ IL0.LR.G2.D4_P
86	■ IL0.LR.G2.D4_N
87	GND
88	■ IL0.LR.G2.D1_N
89	■ IL0.LR.G2.D1_P
90	GND
91	GND
92	■ IL0.LR.G2.D0_P
93	■ IL0.LR.G2.D0_N
94	GND
95	■ IL0.LR.G2.D3_N
96	■ IL0.LR.G2.D3_P
97	GND
98	■ IL0.LR.G2.S_P
99	■ IL0.LR.G2.S_N
100	GND

101	GND
102	■ IL0.LR.G3.D0_N
103	■ IL0.LR.G3.D0_P
104	GND
105	■ IL0.LR.G3.D2_N
106	■ IL0.LR.G3.D2_P
107	GND
108	■ IL0.LR.G3.D4_N
109	■ IL0.LR.G3.D4_P
110	GND
111	GND
112	■ IL0.VTREF.L.T
113	■ IL0.VTREF.L.T
114	GND
115	■ IL0.VTREF.L.T
116	■ IL0.VTREF.L.T
117	GND
118	■ IL0.VTREF.L.T
119	■ IL0.VTREF.L.T
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122	×
123	×
124	GND
125	×
126	GND
127	GND
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138	×
139	×
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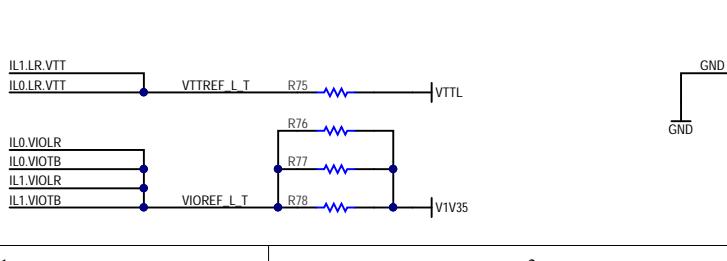
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163	■ VTTREF.L.T
164	GND
165	■ VTTREF.L.T
166	■ VTTREF.L.T
167	GND
168	■ VTTREF.L.T
169	■ VTTREF.L.T
170	GND
171	GND
172	■ VTTREF.L.T
173	■ VTTREF.L.T
174	GND
175	■ VIOREF.L.T
176	■ VIOREF.L.T
177	GND
178	■ VIOREF.L.T
179	■ VIOREF.L.T
180	GND
181	GND
182	■ VIOREF.L.T
183	■ VIOREF.L.T
184	GND
185	■ VIOREF.L.T
186	■ VIOREF.L.T
187	GND
188	■ VIOREF.L.T
189	■ VIOREF.L.T
190	GND
191	GND
192	■ VIOREF.L.T
193	■ VIOREF.L.T
194	GND
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197	GND
198	■ VIOREF.L.T
199	■ VIOREF.L.T
200	GND

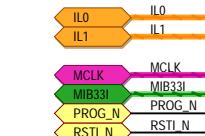
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207	GND
208	■ IL1.LR.G0.D3_P
209	■ IL1.LR.G0.D3_N
210	GND
211	GND
212	■ IL1.LR.G0.D4_P
213	■ IL1.LR.G0.D4_N
214	GND
215	■ IL1.LR.G0.D0_N
216	■ IL1.LR.G0.D0_P
217	GND
218	■ IL1.LR.G0.S.N
219	■ IL1.LR.G0.S.P
220	GND
221	GND
222	■ IL1.LR.G1.D1_P
223	■ IL1.LR.G1.D1_N
224	GND
225	■ IL1.LR.G1.D2_N
226	■ IL1.LR.G1.D2_P
227	GND
228	■ IL1.LR.G1.D4_P
229	■ IL1.LR.G1.D4_N
230	GND
231	GND
232	■ IL1.LR.G1.D3_P
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236	■ IL1.LR.G1.D0_P
237	GND
238	■ IL1.LR.G1.S.P
239	■ IL1.LR.G1.S.N
240	GND
241	GND
242	■ IL1.LR.G2.D4_P
243	■ IL1.LR.G2.D4_N
244	GND
245	■ IL1.LR.G2.D2_N
246	■ IL1.LR.G2.D2_P
247	GND
248	■ IL1.LR.G2.D0_N
249	■ IL1.LR.G2.D0_P
250	GND

251	GND
252	■ IL1.LR.G2.D3_N
253	■ IL1.LR.G2.D3_P
254	GND
255	■ IL1.LR.G2.D1_P
256	■ IL1.LR.G2.D1_N
257	GND
258	■ IL1.LR.G2.S.N
259	■ IL1.LR.G2.S.P
260	GND
261	GND
262	■ IL1.LR.G3.D0_N
263	■ IL1.LR.G3.D0_P
264	GND
265	■ IL1.LR.G3.D2_P
266	■ IL1.LR.G3.D2_N
267	GND
268	■ IL1.LR.G3.D1_P
269	■ IL1.LR.G3.D1_N
270	GND
271	GND
272	■ IL1.LR.G3.D3_N
273	■ IL1.LR.G3.D3_P
274	GND
275	■ IL1.LR.G3.D4_N
276	■ IL1.LR.G3.D4_P
277	GND
278	■ IL1.LR.G3.S.P
279	■ IL1.LR.G3.S.N
280	GND
281	GND
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283	■ IL1.TB.G13.C.P
284	GND
285	■ IL1.TB.G13.D5_P
286	■ IL1.TB.G13.D5_N
287	GND
288	■ IL1.TB.G13.D4_N
289	■ IL1.TB.G13.D4_P
290	GND
291	GND
292	■ IL1.TB.G13.D1_P
293	■ IL1.TB.G13.D1_N
294	GND
295	■ IL1.TB.G13.D3_P
296	■ IL1.TB.G13.D3_N
297	GND
298	■ IL1.TB.G13.D2_N
299	■ IL1.TB.G13.D2_P
300	GND

301	GND
302	■ IL1.TB.G8.D3.N
303	■ IL1.TB.G8.D3.P
304	GND
305	■ IL1.TB.G8.D0.N
306	■ IL1.TB.G8.D0.P
307	GND
308	■ IL1.TB.G8.D2.P
309	■ IL1.TB.G8.D2.N
310	GND
311	GND
312	■ IL1.TB.G13.D0.P
313	■ IL1.TB.G13.D0.N
314	GND
315	■ IL1.TB.G8.D1.N
316	■ IL1.TB.G8.D1.P
317	GND
318	■ IL1.TB.G13.D6
319	■ IL1.TB.G13.D6
320	GND
321	GND
322	×
323	×
324	GND
325	×
326	×
327	GND
328	×
329	×
330	GND
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335	×
336	×
337	GND
338	×
339	×
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349	×
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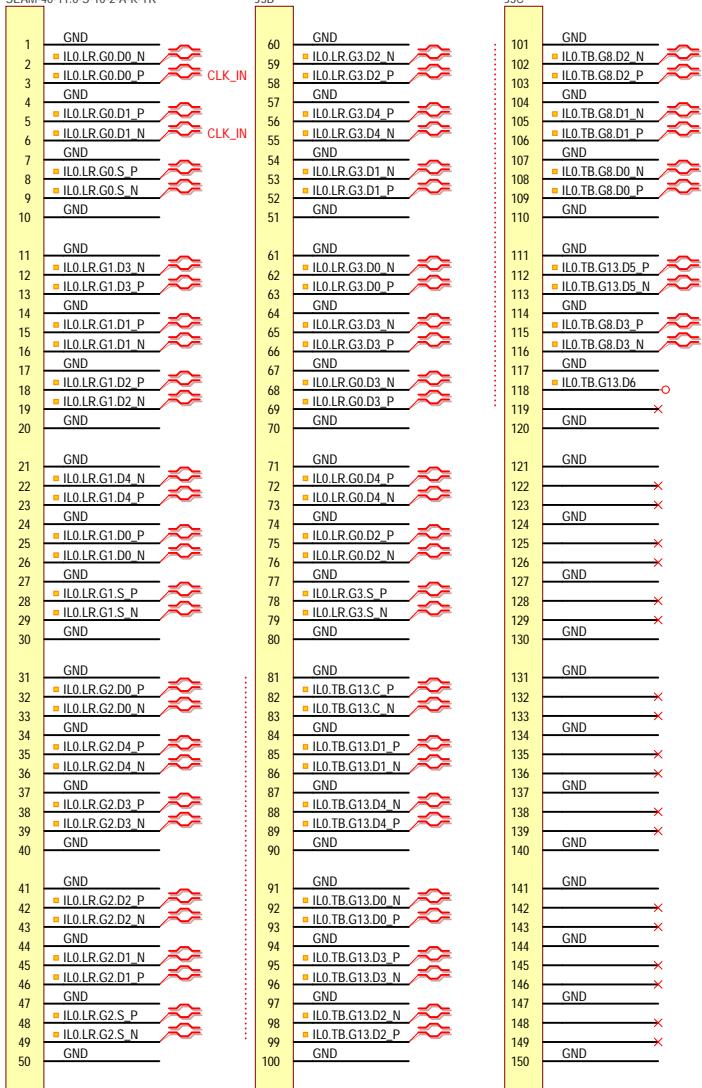
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383	GND
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385	GND
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387	GND
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389	GND
390	×
391	GND
392	×
393	GND
394	×
395	GND
396	×
397	GND
398	×
399	GND
400	×





V48
V48

J3A
SEAM-40-11.0-S-10-2-A-K-TR



J3B

J3C

J3D

J3E

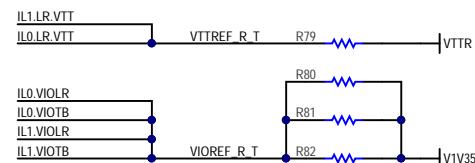
J3F

J3G

J3H

NOT USED

GND
GND



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Menlo Park CA 94025
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siglabs.com

Title CS - Right Top

Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 3	Sheet 34 of 47	Date 11/3/2017



A

J2A
SEAF-40-06-S-10-2-A-K-TR

1	GND
2	■ IL0.TB.G13.C.N
3	■ IL0.TB.G13.C.P
4	GND
5	■ IL0.TB.G13.D5.N
6	■ IL0.TB.G13.D5.P
7	GND
8	■ IL0.TB.G13.D1.P
9	■ IL0.TB.G13.D1.N
10	GND
11	GND
12	■ IL0.TB.G13.D0.N
13	■ IL0.TB.G13.D0.P
14	GND
15	■ IL0.TB.G13.D2.N
16	■ IL0.TB.G13.D2.P
17	GND
18	■ IL0.TB.G13.D4.P
19	■ IL0.TB.G13.D4.N
20	GND
21	GND
22	■ IL0.TB.G13.D3.N
23	■ IL0.TB.G13.D3.P
24	GND
25	■ IL0.TB.G8.D1.P
26	■ IL0.TB.G8.D1.N
27	GND
28	■ IL0.TB.G8.D3.N
29	■ IL0.TB.G8.D3.P
30	GND
31	GND
32	■ IL0.TB.G8.D2.N
33	■ IL0.TB.G8.D2.P
34	GND
35	■ IL0.TB.G8.D0.P
36	■ IL0.TB.G8.D0.N
37	GND
38	■ IL0.TB.G13.D6
39	■ GND
40	GND
41	GND
42	■ IL0.LR.G0.D3.P
43	■ IL0.LR.G0.D3.N
44	GND
45	■ IL0.LR.G0.D2.N
46	■ IL0.LR.G0.D2.P
47	GND
48	■ IL0.LR.G0.D4.P
49	■ IL0.LR.G0.D4.N
50	GND

DNP

60	GND
59	■ IL0.LR.G0.D0.P
58	■ IL0.LR.G0.D0.N
57	GND
56	■ IL0.LR.G0.D1.P
55	■ IL0.LR.G0.D1.N
54	GND
53	■ IL0.LR.G0.S.P
52	■ IL0.LR.G0.S.N
51	GND

DNP

101	GND
102	■ IL0.LR.G3.D4.P
103	■ IL0.LR.G3.D4.N
104	GND
105	■ IL0.LR.G3.D0.N
106	■ IL0.LR.G3.D0.P
107	GND
108	■ IL0.LR.G3.D2.P
109	■ IL0.LR.G3.D2.N
110	GND

DNP

151	GND
152	■ IL0.LR.G0.D0.N
153	GND
154	■ IL0.LR.G0.D0.P
155	GND
156	■ IL0.LR.G0.D0.N
157	GND
158	■ IL0.LR.G0.D0.P
159	GND
160	GND

DNP

201	GND
202	■ IL1.LR.G0.D2.P
203	■ IL1.LR.G0.D2.N
204	GND
205	■ IL1.LR.G0.D0.N
206	■ IL1.LR.G0.D0.P
207	■ IL1.LR.G0.D1.N
208	■ IL1.LR.G0.D1.P
209	GND
210	GND

DNP

251	GND
252	■ IL1.LR.G2.D1.P
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254	GND
255	■ IL1.LR.G2.D4.P
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260	GND

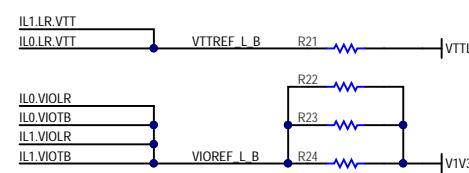
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306	■ IL1.TB.G8.D2.P
307	GND
308	■ IL1.TB.G8.D0.N
309	■ IL1.TB.G8.D0.P
310	GND

DNP

351	GND
352	■ IL1.TB.G8.D3.P
353	■ IL1.TB.G8.D3.N
354	GND
355	■ IL1.TB.G8.D2.N
356	■ IL1.TB.G8.D2.P
357	GND
358	■ IL1.TB.G8.D0.N
359	■ IL1.TB.G8.D0.P
360	GND

DNP



Title

CS - Left Bottom

Engineer

J. Brinton

Drawn By
Checked By
J. Brinton

Revision

3

Sheet

35 of 47

Date

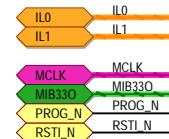
11/3/2017

A

B

C

D



V48
V48

J1A
SEAF-40-06-S-10-2-A-K-TR

1	GND	
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3	ILO.LR.G0.D3.N	
4	GND	
5	ILO.LR.G0.D2.N	
6	ILO.LR.G0.D2.P	
7	GND	
8	ILO.LR.G0.S.P	
9	ILO.LR.G0.S.N	
10	GND	
11	GND	
12	ILO.LR.G1.D2.P	
13	ILO.LR.G1.D2.N	
14	GND	
15	ILO.LR.G1.D1.P	
16	ILO.LR.G1.D1.N	
17	GND	
18	ILO.LR.G1.D4.P	
19	ILO.LR.G1.D4.N	
20	GND	
21	GND	
22	ILO.LR.G1.D3.P	
23	ILO.LR.G1.D3.N	
24	GND	
25	ILO.LR.G1.D0.P	
26	ILO.LR.G1.D0.N	
27	GND	
28	ILO.LR.G1.S.P	
29	ILO.LR.G1.S.N	
30	GND	
31	GND	
32	ILO.LR.G2.D1.P	
33	ILO.LR.G2.D1.N	
34	GND	
35	ILO.LR.G2.D2.N	
36	ILO.LR.G2.D2.P	
37	GND	
38	ILO.LR.G2.D0.P	
39	ILO.LR.G2.D0.N	
40	GND	
41	GND	
42	ILO.LR.G2.D3.N	
43	ILO.LR.G2.D3.P	
44	GND	
45	ILO.LR.G2.D4.P	
46	ILO.LR.G2.D4.N	
47	GND	
48	ILO.LR.G2.S.P	
49	ILO.LR.G2.S.N	
50	GND	

J1B

60	GND	
59	ILO.LR.G3.D0.P	
58	ILO.LR.G3.D0.N	
57	GND	
56	ILO.LR.G3.D2.P	
55	ILO.LR.G3.D2.N	
54	GND	
53	ILO.LR.G3.D1.N	
52	ILO.LR.G3.D1.P	
51	GND	
61	GND	
62	ILO.LR.G3.D3.P	
63	ILO.LR.G3.D3.N	
64	GND	
65	ILO.LR.G3.D4.P	
66	ILO.LR.G3.D4.N	
67	GND	
68	ILO.LR.G0.D4.N	
69	ILO.LR.G0.D4.P	
70	GND	

J1C

101	GND	
102	ILO.TB.G8.D1.P	
103	ILO.TB.G8.D1.N	
104	GND	
105	ILO.TB.G8.D2.P	
106	ILO.TB.G8.D2.N	
107	GND	
108	ILO.TB.G8.D3.P	
109	ILO.TB.G8.D3.N	
110	GND	

J1D

151	GND	
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154	GND	
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158	MIB33O.S27	
159	MIB33O.S7	
160	GND	

J1E

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203	MIB33O.S25	
204	GND	
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206	MIB33O.S26	
207	GND	
208	MIB33O.S0	
209	MIB33O.S11	
210	GND	

J1F

251	GND	
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253	MIB33O.S55	
254	GND	
255	MIB33O.S12	
256	MIB33O.S15	
257	GND	
258	MIB33O.S10	
259	MIB33O.S20	
260	GND	

NOT USED

J1G

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304	GND	
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306	ILO.TB.G8.D1.N	
307	GND	
308	ILO.TB.G8.D3.P	
309	ILO.TB.G8.D3.N	
310	GND	

J1H

351	GND	
352	ILO.LR.G1.D3.P	
353	ILO.LR.G1.D3.N	
354	GND	
355	ILO.LR.G1.D4.P	
356	ILO.LR.G1.D4.N	
357	GND	
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360	GND	

DNP

DNP

DNP

DNP

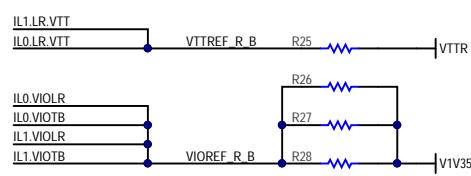
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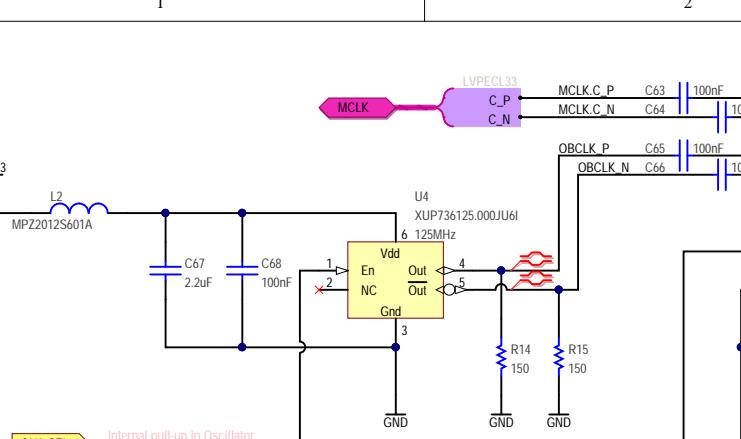
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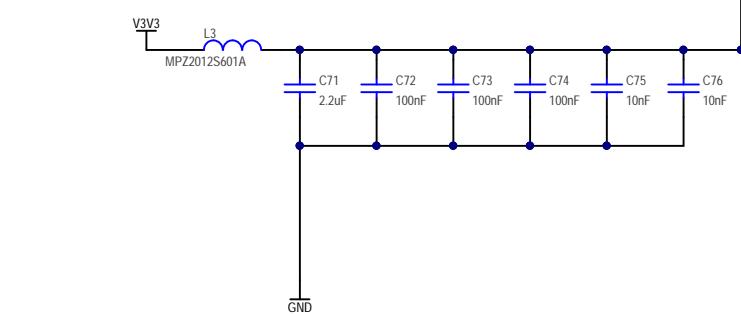
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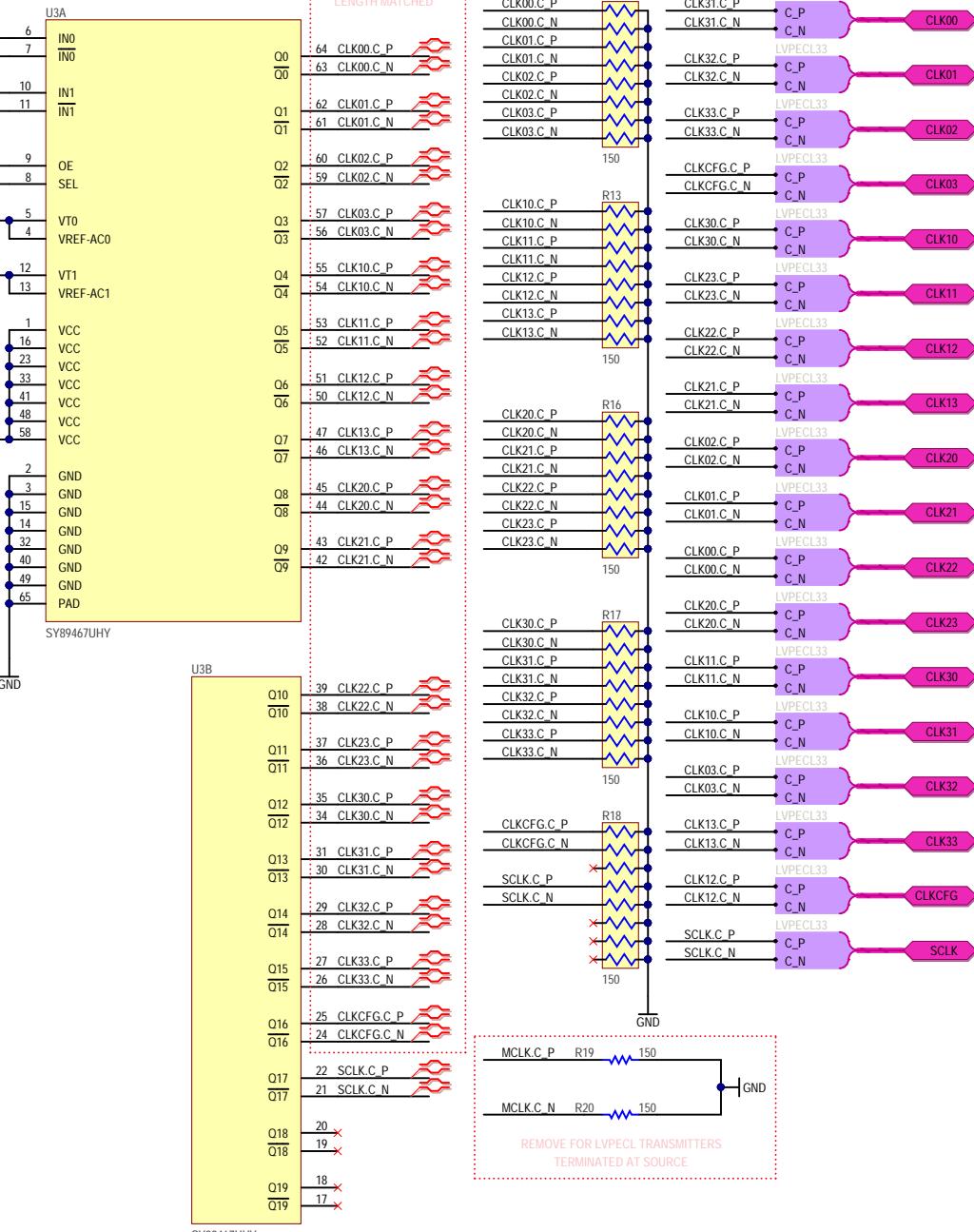
A



B



C



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CS - Clock Fanout

Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 3	Sheet 37 of 47	Date 11/3/2017

A

A

B

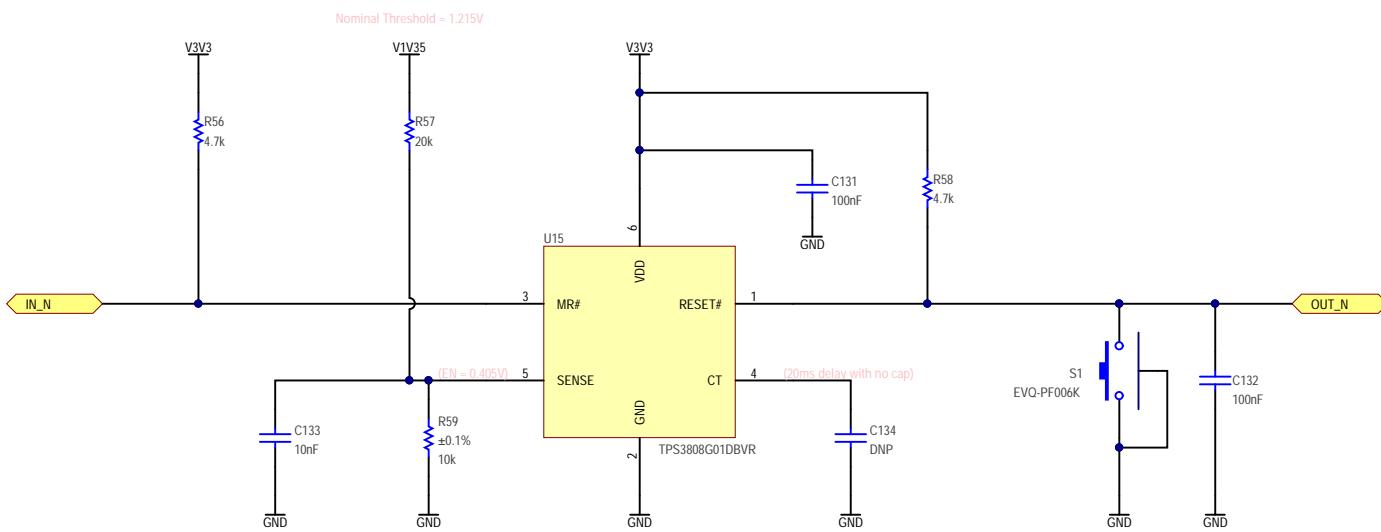
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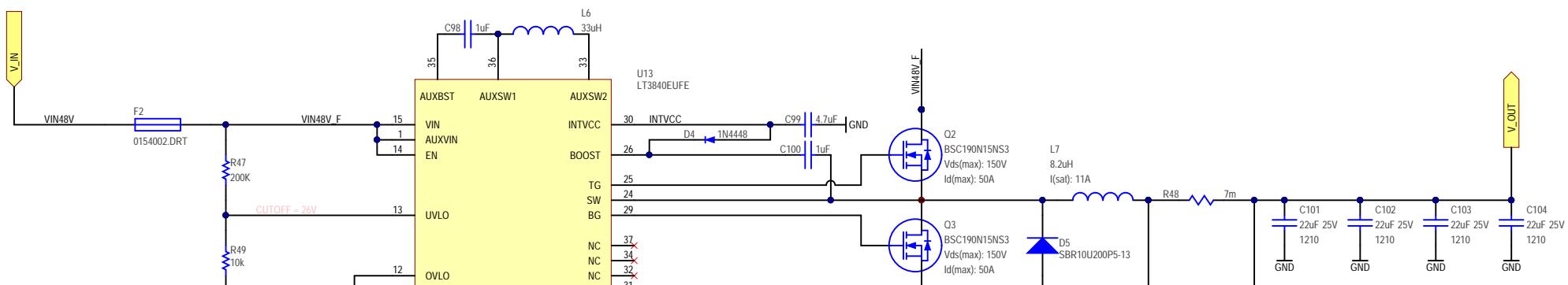
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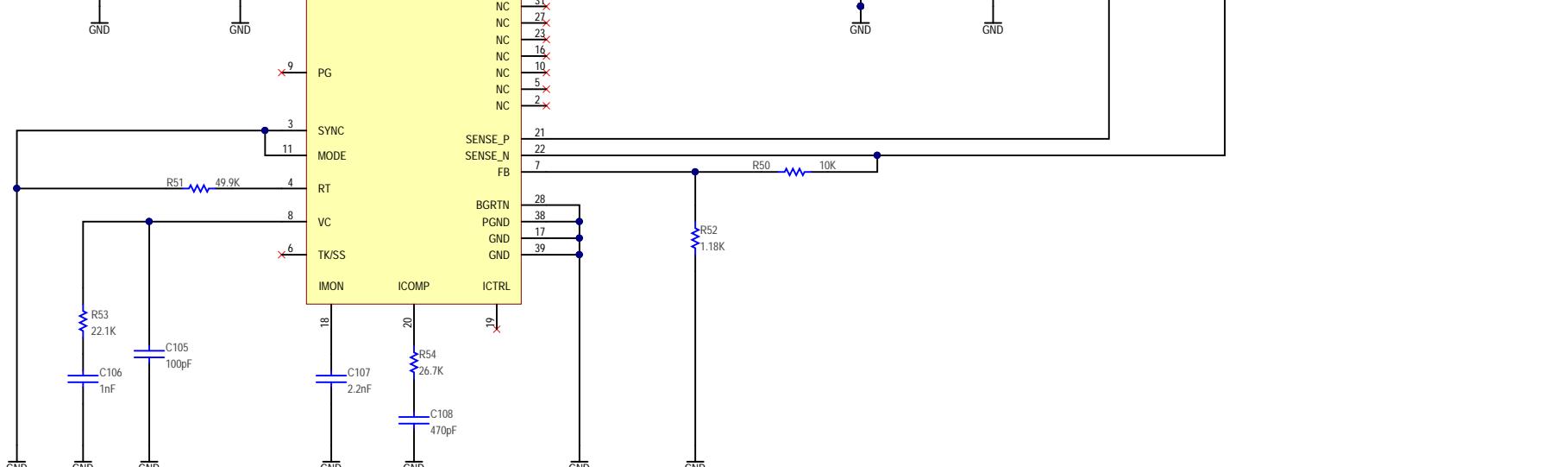
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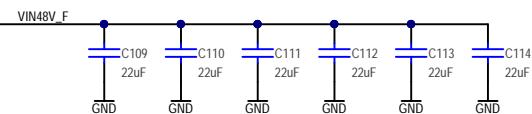
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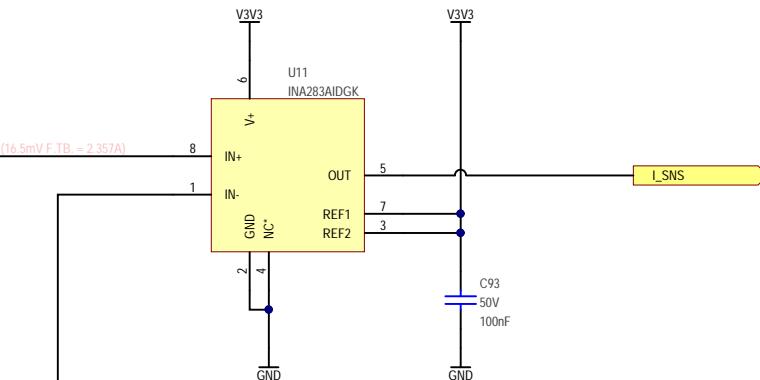


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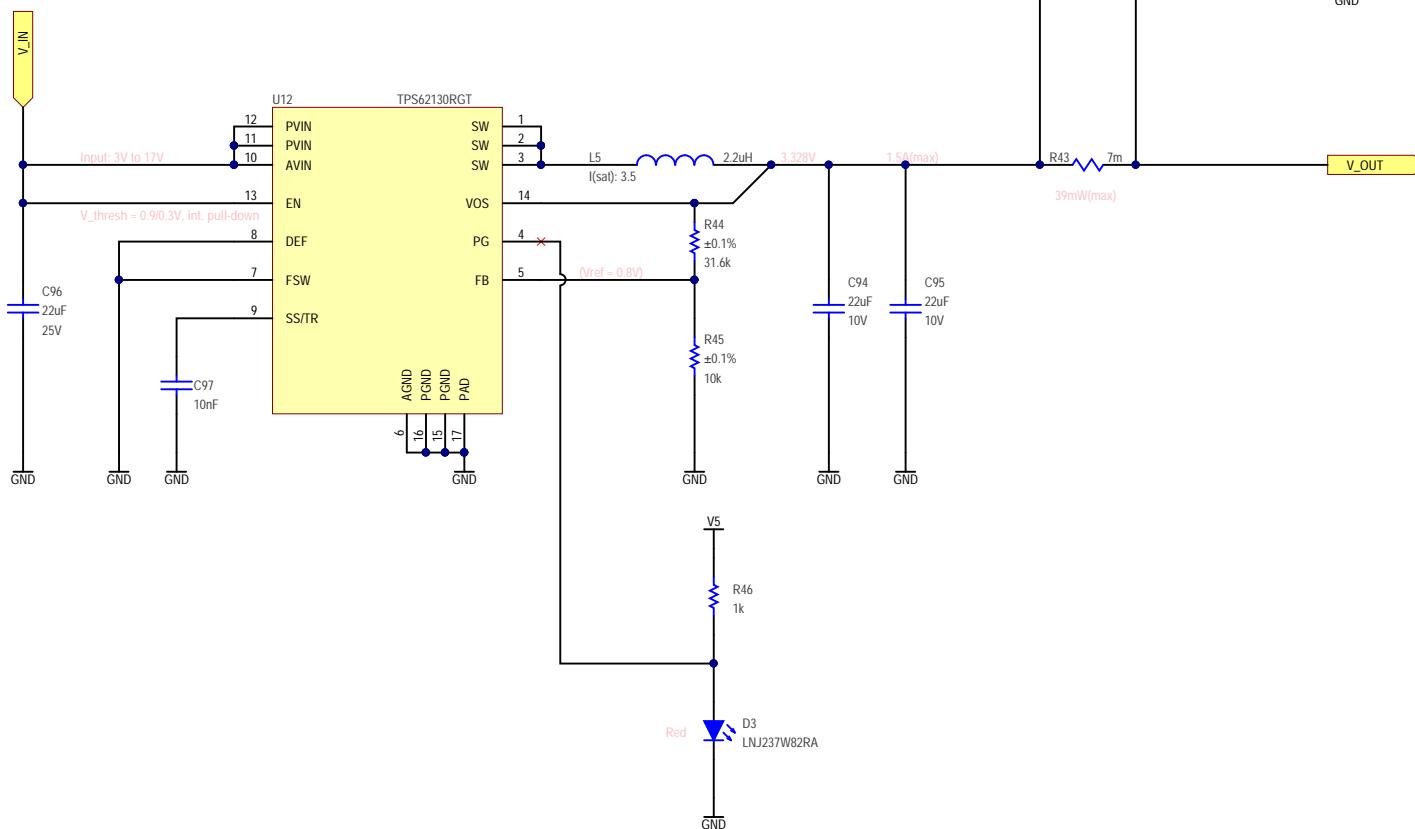
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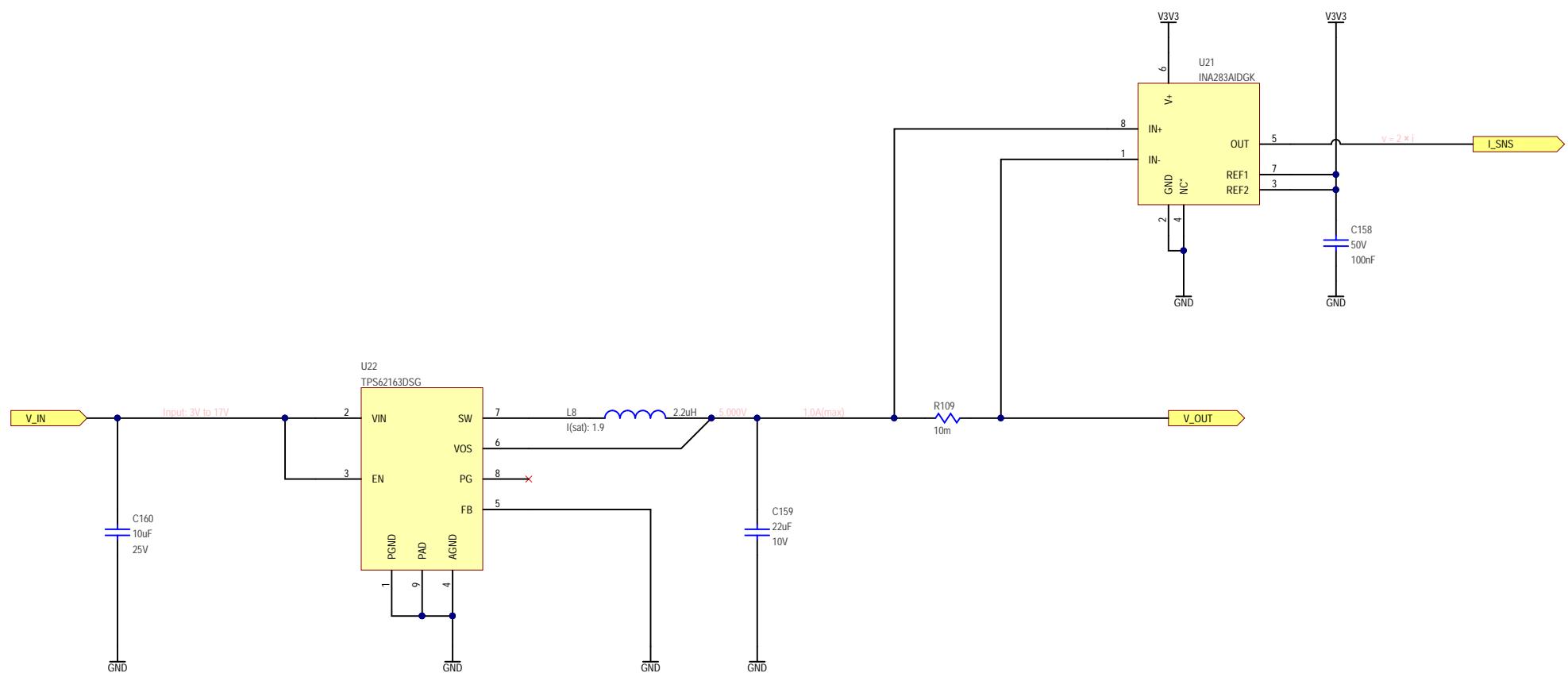
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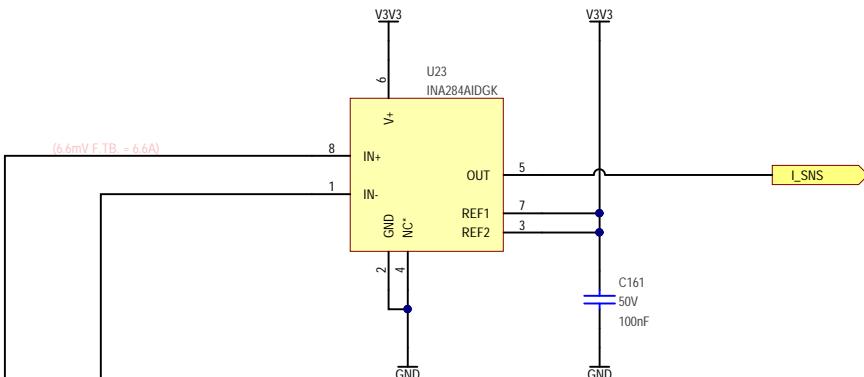
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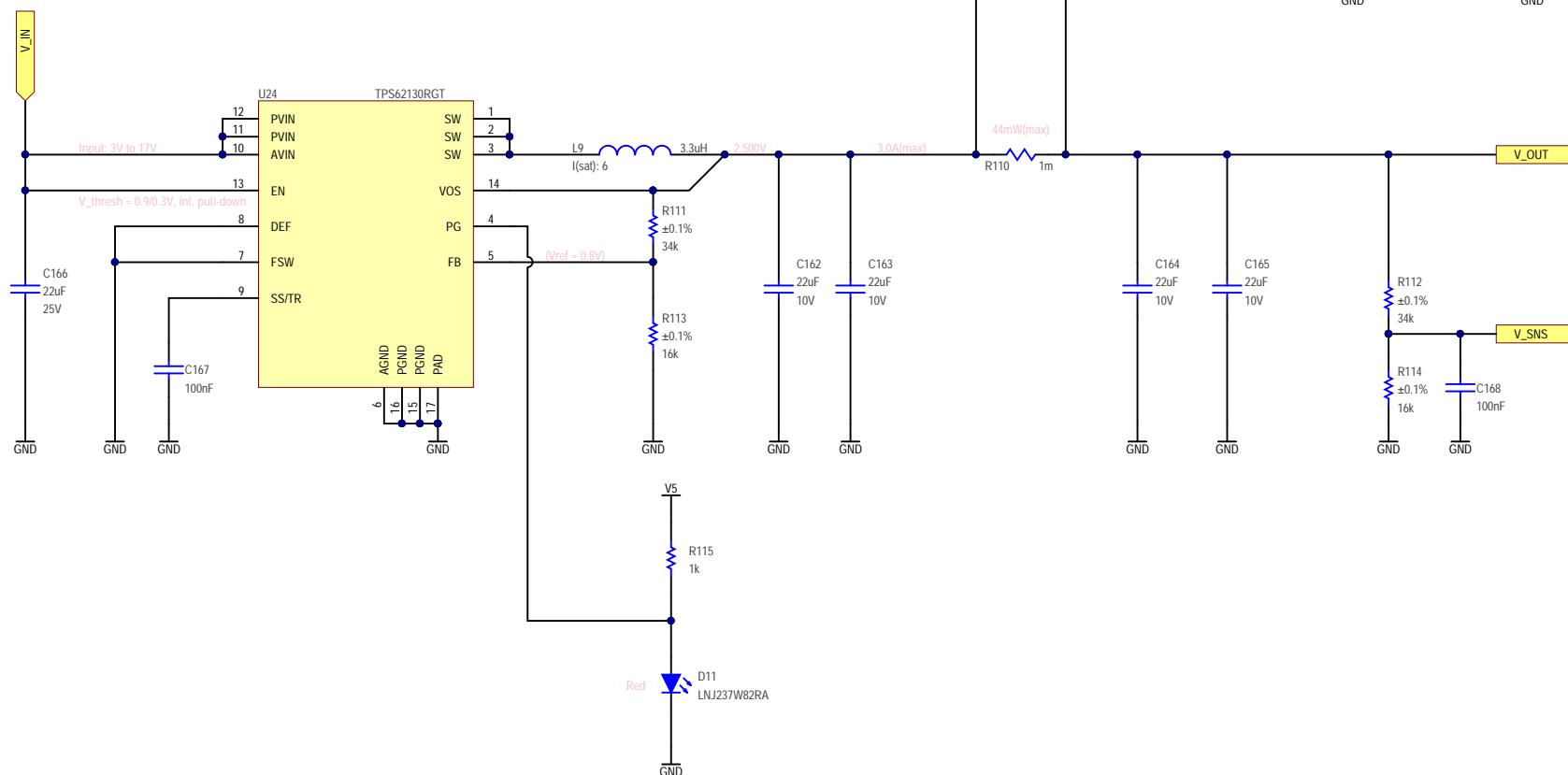
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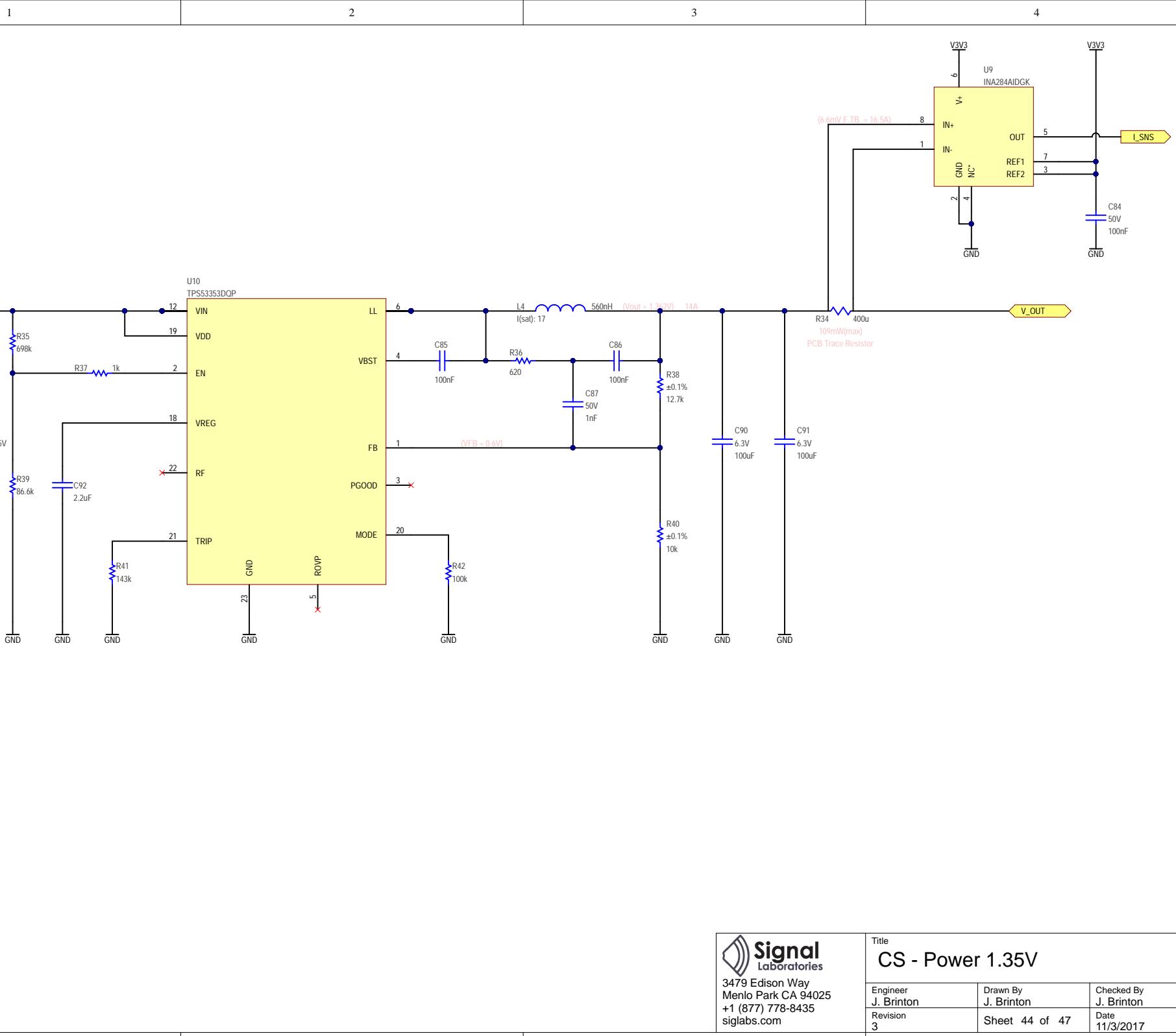
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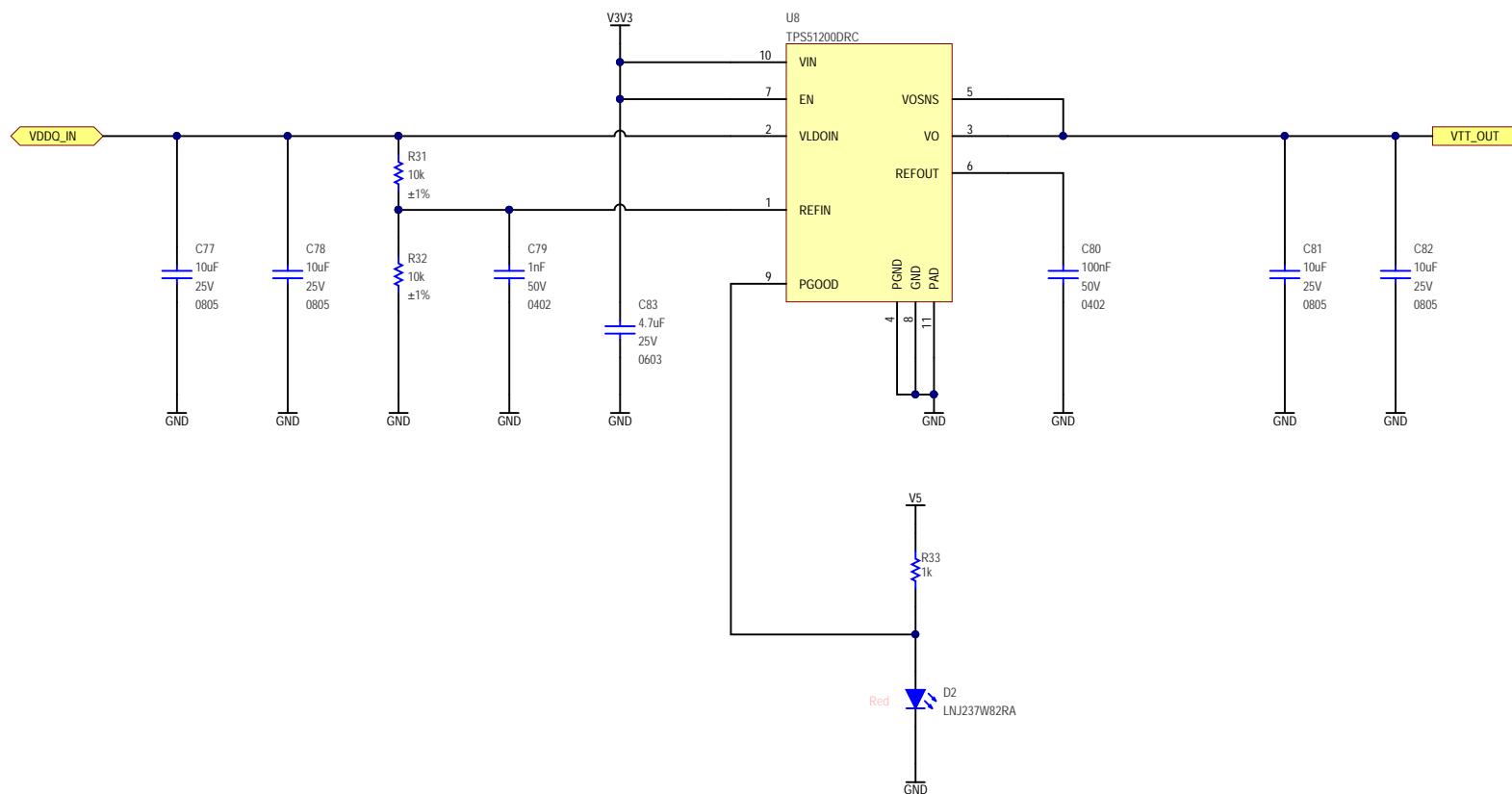
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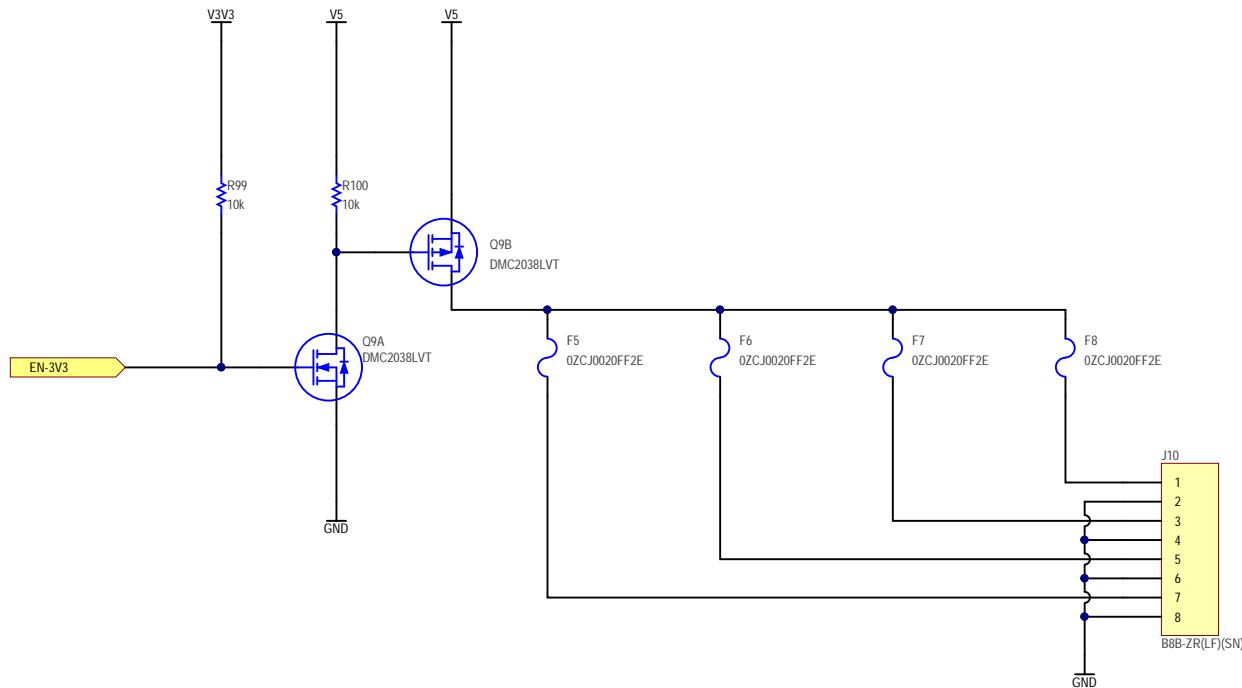
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