PCB Fabrication Variables Impacting Signal Integrity
2016 Edition

TTM Technologies

Global Presence | Local Knowledge

PCB Fabrication Variables Impacting SI Agenda

- PCB Fabrication Variables Impacting Signal Integrity
  - Dielectric Materials - Laminate
  - Glass Fabric Styles (spread, super spread, flat, etc)
  - Dielectric Thickness Variation DRC
  - Signal Thickness and Width Characteristics
  - Signal Roughness Characteristics
  - Interconnect Backdrilling

Why are We Here Today? High Speed Transmission over Copper

Global network bandwidth forecast

- Bandwidth is expected to double every 18 to 24 months. In addition to building additional infrastructure, service providers upgrade existing routers, switches and even the "last mile" to provide higher capacity.
- Current 12+ Gbps and 25+ Gbps activity is much more prevalent driving PCBs to use higher speed materials, high performance foils, denser components and techniques.
- We need a comprehensive approach and even closer NPI coordination between OEM and Fabrication than ever before from design outset.

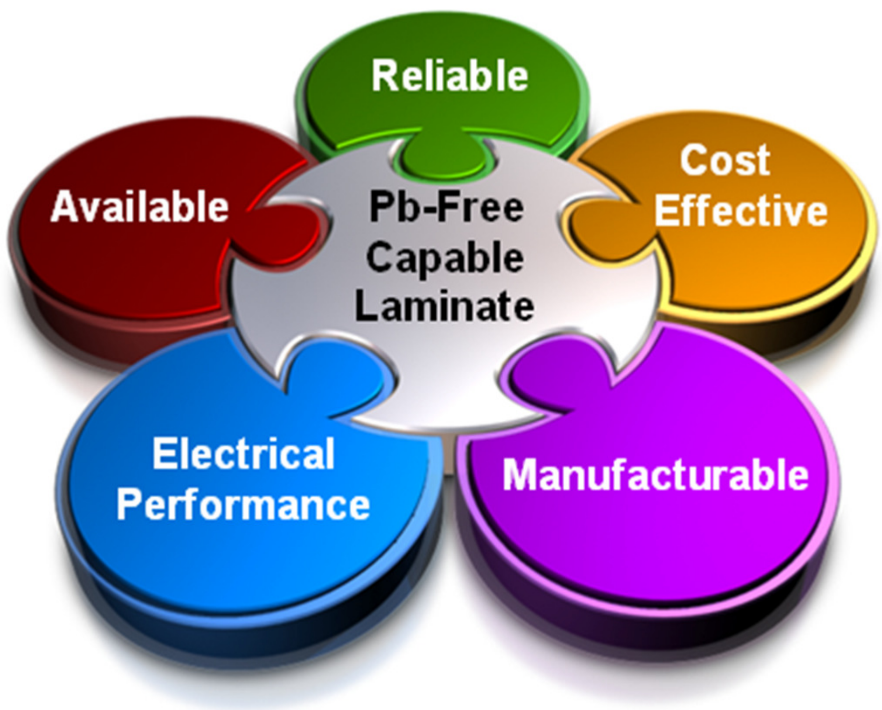
The Impact of Signal Length to High Speed

- One of the many aspects to all of this that largely goes unknown when discussing how the PCB factors into total system loss is signal length
  - An example of this is we have production products operating at 25-28 Gbps using Tier 2 materials due to the short total signal lengths whereas most customers go directly to a tier 3 material
- As a PCB fabricator we have a deep knowledge of manufacturing but much less on total electrical performance so the more detail we receive the more effective we will be able to assist

Laminate and Fabrics

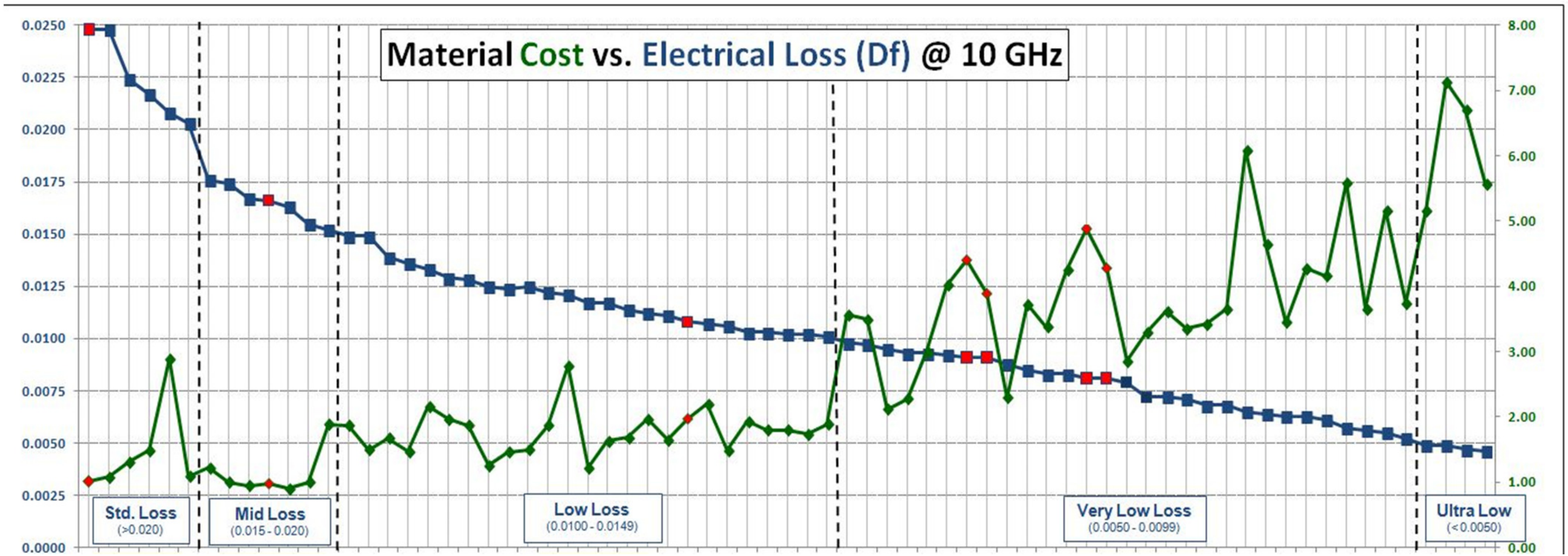
PCB Laminate Testing is the Foundation to High Speed

- Each must be checked off – reliability cannot be compromised for Si



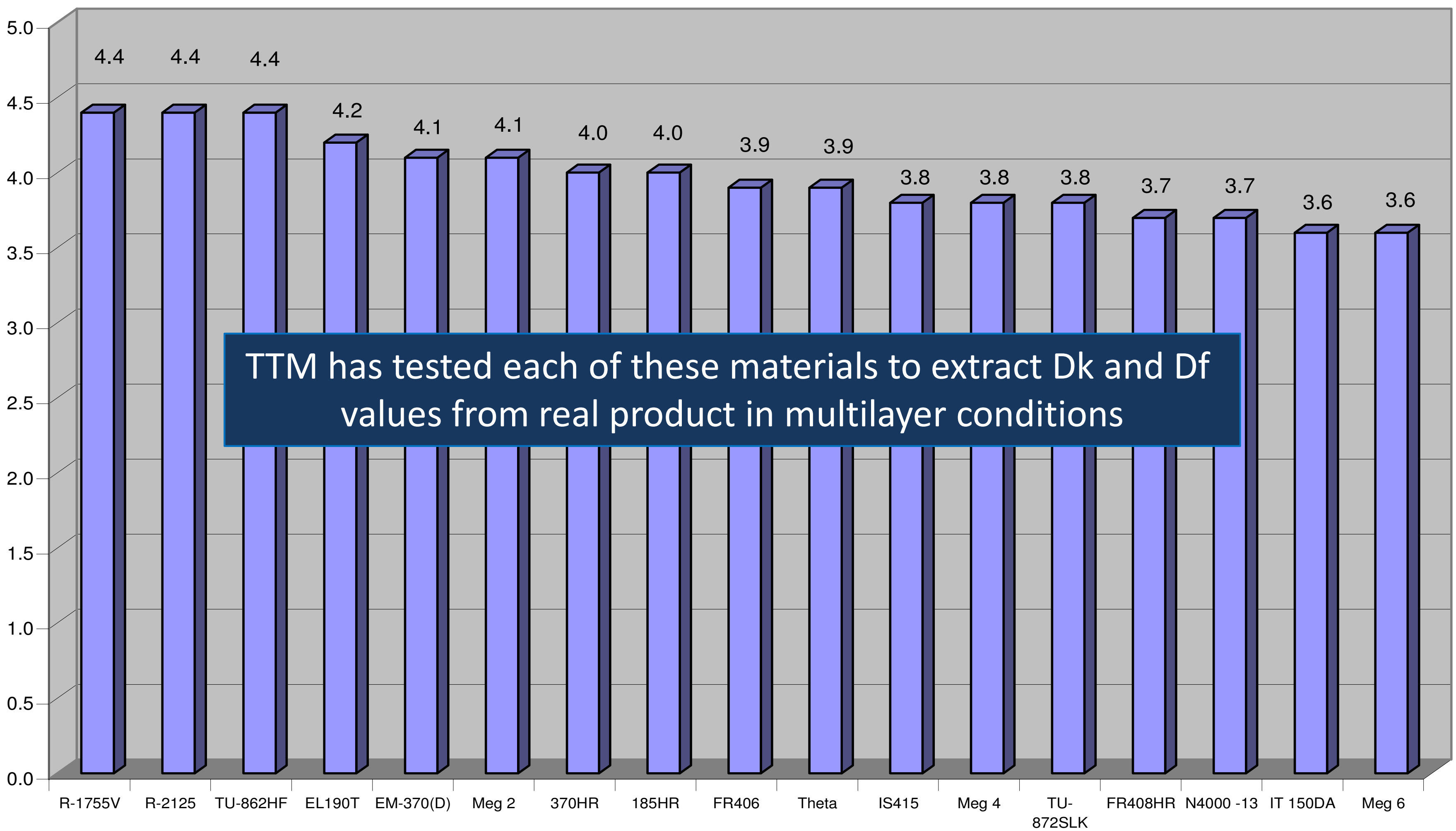
Tier	Classification	Df range*
4	Ultra Low Loss	< 0.0050
3	Very Low Loss	0.0050 - 0.0099
2	Low Loss	0.0100 – 0.0149
1.5	Mid Loss	0.0150 – 0.0200
1	Standard Loss	> 0.0200

Material Cost vs Loss Evaluations



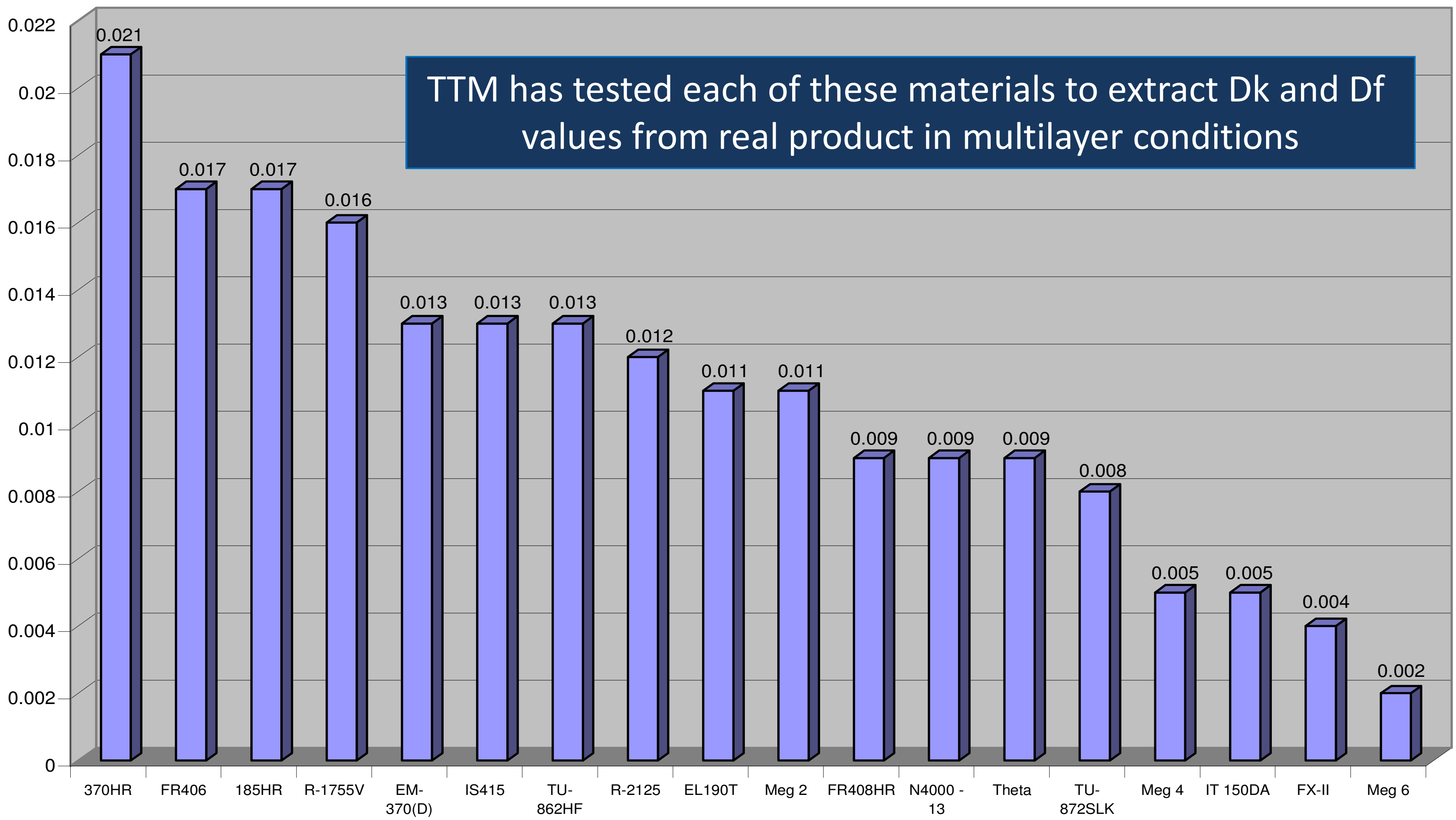
Over 70 material offerings evaluated

Material Summary – Dk Comparison *(2Ghz – Supplier Data Sheets)*



TTM has tested each of these materials to extract Dk and Df values from real product in multilayer conditions

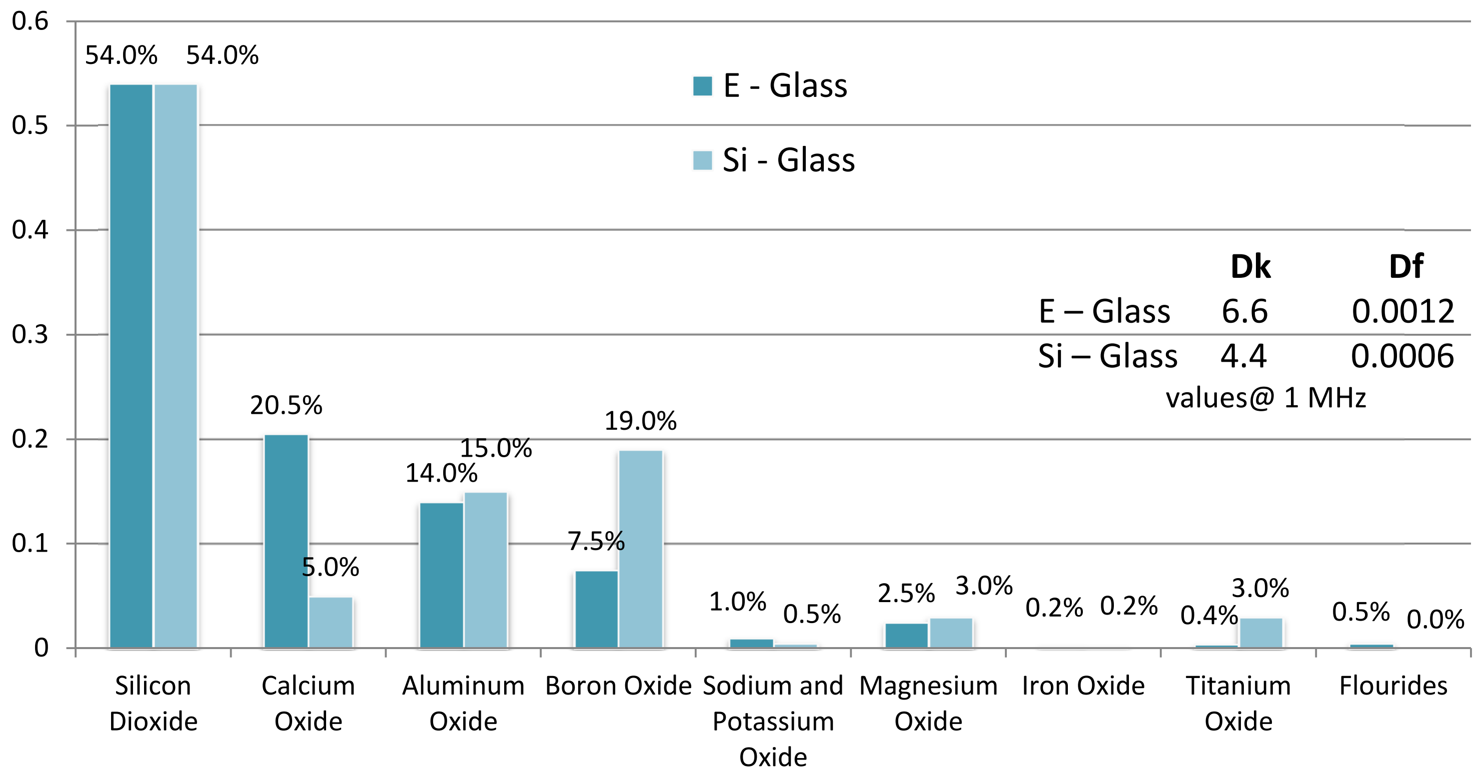
Material Summary – Df Comparison *(2Ghz – Supplier Data Sheets)*



TTM has tested each of these materials to extract Dk and Df values from real product in multilayer conditions

Fiberglass Composition between E-Glass and Si-Glass

- E-Glass is the standard fabric used in the majority of PCBs
- Si-Glass composition reduces the Dk of the fabric to enable an improved overall Dk and also closer to the resin system used



Fabric Styles – A Large List that We Mostly Can't Get!

Style	Fabric Count Warp x Fill [Per inch]	Yarn [US System]	Thickness (mils) (Reference Only)	Nominal Weight [OSY]	Weight Tolerance [OSY]	Availability[1]
101	75 x 75	D1800 1/0 X D1800 1/0	0.96	0.48	0.45 - 0.51	1
104	60 x 52	D900 1/0 X D1800 1/0	1.1	0.55	0.53 - 0.57	1
106	56 x 56	D900 1/0 X D900 1/0	1.3	0.72	0.69 - 0.75	1
1078	54 x 54	D450 1/0 X D450 1/0	1.7	1.41	1.38 - 1.45	1
1080	60 x 47	D450 1/0 X D450 1/0	2.1	1.38	1.33 - 1.43	1
1081	70 x 60	D450 1/0 X D450 1/0	2.4	1.72	1.66 - 1.78	1
1280	60 x 60	D450 1/0 X D450 1/0	2.2	1.55	1.49 - 1.61	1
1500	49 x 42	E110* 1/0 X E110* 1/0	5.9	4.84	4.65 - 5.03	1
1501	46 x 45	E110* 1/0 X E110* 1/0	5.5	4.86	4.67 - 5.05	1
1504	60 x 50					1
1651	51 x 27					1
1652	52 x 52					1
1674	40 x 32					1
1675	40 x 32					1
1678	40 x 40					1
2113	60 x 56					1
2114	56 x 48					1
2116	60 x 58	E225 1/0 X E225 1/0	3.7	3.06	2.97 - 3.15	1
2117	66 x 55	E225 1/0 X E225 1/0	3.7	3.18	3.08 - 3.27	1
2125	40 x 39	E225 1/0 X G150* 1/0	3.6	2.54	2.44 - 2.68	1
2157	60 X 35	E225 1/0 X G75 1/0	5.1	4.36	4.18 - 4.54	1
2165	60 x 52	E-225 1/0 X G150* 1/0	4.0	3.55	3.43 - 3.72	1
2166	60 X 38	E225 1/0 X G75 1/0	5.5	4.60	4.41 - 4.79	1
2313	60 x 64	E225 1/0 X D450 1/0	3.3	2.40	2.33 - 2.47	1
3070	70 x 70	DE300 1/0 X DE300 1/0	3.1	2.76	2.68 - 2.84	1
3080	51 x 30	DE300 1/0 X DE300 1/0	2.3	1.57	1.52 -1.63	1
3313	60 x 62	DE300 1/0 X DE300 1/0	3.3	2.40	2.33 - 2.47	1
7628	44 x 31	G75 1/0 X G75 1/0	6.8	6.00	5.84 - 6.16	1
7629	44 x 34	G75 1/0 X G75 1/0	7.1	6.19	6.03 - 6.35	1
7635	44 x 29	G75 1/0 X G50* 1/0	7.9	6.85	6.68 - 7.02	1
7642	44 x 20	G75 1/0 X G37* 1/0 (texturized)	10.0	6.72	6.52 - 6.92	1

Availability is largely determined by the specific laminator and demand

Typical PCB Glass Styles

106
1080
2113
3070
2116
1652
7628

High Speed Styles

1035
1067
1078
1086
3313
1652

TTM-CF Materials Test Program – Results Summary

Materials	Production Ready	Development
Tier 1 Std. loss, (>0.0200 Df)	**Isola, -370HR & -370HR AP** **Nelco, -29** (marginal CAF-R) **Panasonic, R-1755 V** (CN) **Panasonic, R-2125**	**EMC, EM-827**
Tier 1.5 Mid loss, (0.0150 – 0.0200 Df)	**EMC, EM-370(D)** (*HF*) **TUC, TU-862 HF** (*HF*)	**Doosan, DS7402H** (*HF*) **TUC, TU-865** (*HF*)
Tier 2 Low loss, (0.0100 – 0.0149 Df)	**Doosan, DS7409D(X) & (XC)** **EMC, EM-828G** (*HF*) **EMC, EM-888, EM-888S** (*HF*) **Hitachi, HE-679G** (*HF*, formerly Theta) **Isola, FR408HR** (marginal CAF-R) **Nelco, -13EP &-13EP SI** (marginal CAF-R) **Panasonic, Megtron 2** (*HF*) **Panasonic, Megtron 4** **Shengyi, S7439 (Synamic 4)** UL V-1 **TUC, TU-872 SLK**	**Isola, I-Speed High Tg** **ITEQ, IT-170GRA1** (*HF*) **Nan Ya, NPG-170D** (*HF*) **Panasonic Megtron 4S or M** (?) **TUC, TU-862S** (*HF*) **Ventec, VT-464L** (*HF*)
Tier 3 Very low loss, (0.0050 – 0.0099 Df)	**Doosan, DS7409DV** **EMC, EM-888K** (*HF*) **Panasonic, Megtron 6 K, 6 G, 6 N** **TUC, TU-883** a.k.a. T2 (*HF*) UL V-1	**EMC, EM-891** **Isola, I-Tera MT 40** **ITEQ, IT-150DA** **ITEQ, IT-968** **Nelco, N4800-20 & -20 SI** **Nelco, Meteorwave 1000** **Panasonic Megtron 7** **Shengyi, S7338 & S7335**
Tier 4 Ultra low loss, (<0.0050 Df)		**Doosan, DS7409DV (N)** **EMC, EM-891K** **Isola, Tachyon-100G** **Nelco, Meteorwave 4000** **Panasonic Megtron 7N** **TUC, TU-933** a.k.a. T3 (NE glass)

***HF* = Halogen free**

Fiber Weave Mitigation

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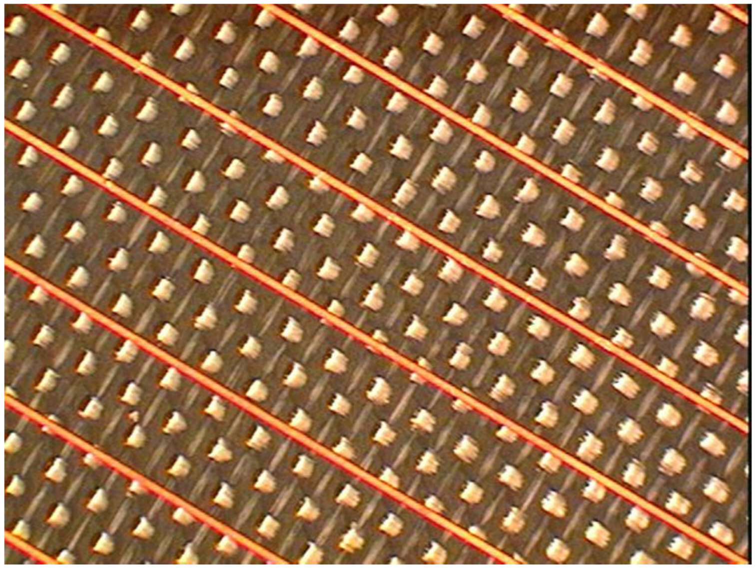
Fiber Weave Effect (FWE) Mitigation Overview

- It is well documented that high speed differential signals, generally speaking in the 10 Gbps and above range, may be impacted by what is known as fiber weave effect (FWE) when using conventional woven glass laminates that are typical in the PCB industry.
- The significance of this on end product performance can only be determined by our customer engineers and architects

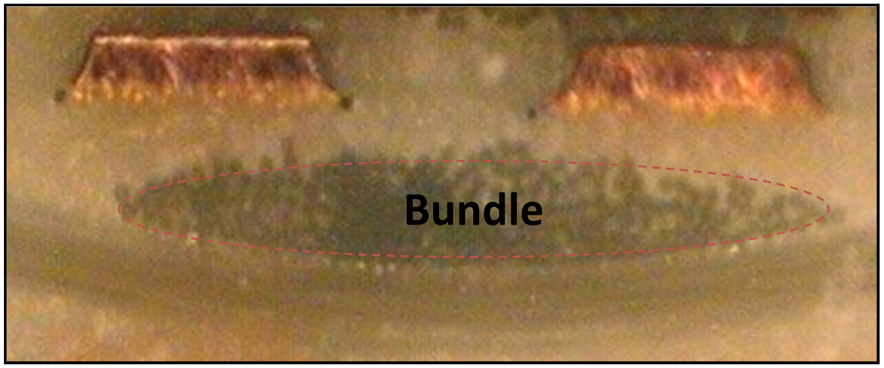


Fiber Weave Impact on Delay - Simulation

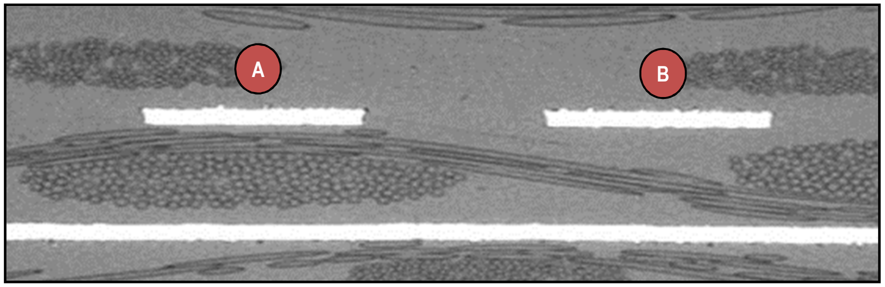
- The location of the signals relative to the glass yarn cannot be controlled and can create differential pair skew

Calculated Delay (tpd)	Er
Picoseconds/inch *	Dk
153.91	3.30
156.23	3.40
B 158.51	3.50
160.75	3.60
162.97	3.70
165.16	3.80
167.32	3.90
169.45	4.00
171.56	4.10
173.64	4.20
175.69	4.30
A 177.72	4.40
179.73	4.50
181.72	4.60

Simulated prop delay based on localized Dk variations.



Cross sectional view of differential signal pair with very equal proximity and alignment to the fiberglass yarn bundle.

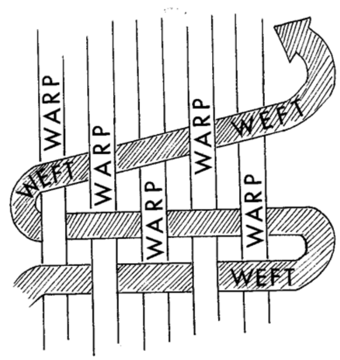


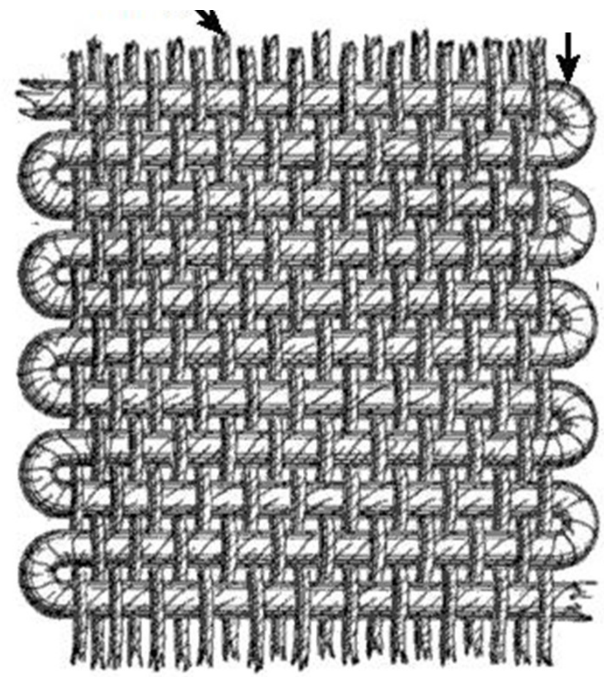
Cross sectional view of a differential signal pair with varying level of fiber weave effect and simulated Dk and delay per Table

Key Fabric Terms and Definitions

- **Standard Weave** – Classic, Plain "over-under" weave
- **Expanded Weave** – Glass Spread in one Direction
- **Spread Glass** – Glass Spread in both directions
- **Mechanically Spread (MS) Glass** – Glass is Mechanically Spread in both directions.
- **Flat Glass** – Glass is made from fibers with little or no twist
- **Square Weave** – Glass that has an equal number of yarn strands in both directions

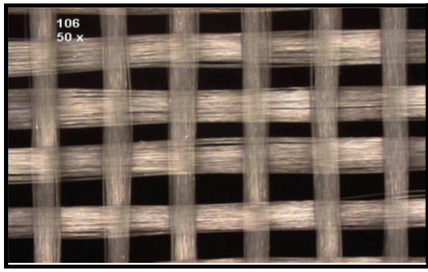
Definitions and Terminology of Fiberglass Yarns



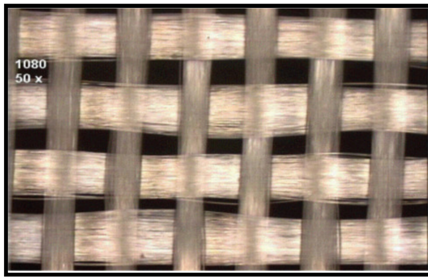


Fiberglass yarns are woven to create the cloth. In the weaving process the **woof** (aka, **weft** and **fill**) is the term used for the thread or yarn which is drawn through the **warp** (or **grain**) direction. **Warp** is the lengthwise or longitudinal thread in a roll, while **weft** is the transverse thread. A single thread of **weft**, crossing the **warp**, is called a pick.

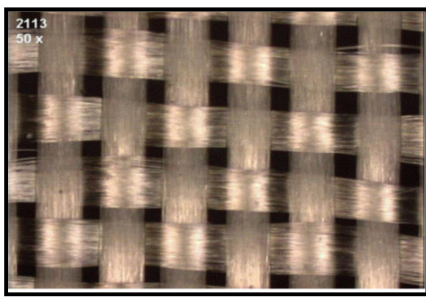
Traditional PCB Glass Fabric Styles



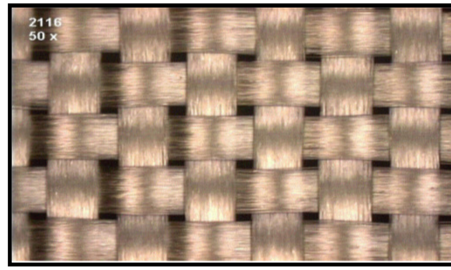
Glass Style: 106
Plain Weave
Count: 56x56 (ends/in)
Thickness: 0.0015 (in)
Resin Content: 75%



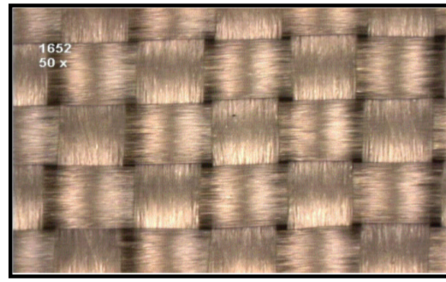
Glass Style: 1080
Plain Weave
Count: 60x47 (ends/in)
Thickness: 0.0025 (in)
Resin Content: 65%



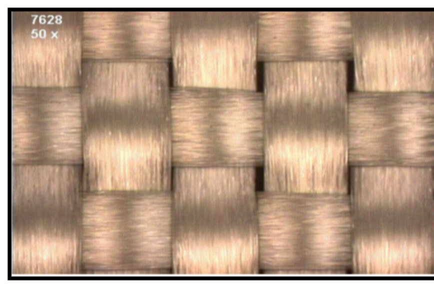
Glass Style: 2113
Plain Weave
Count: 60x56 (ends/in)
Thickness: 0.0029 (in)
Resin Content: 57%



Glass Style: 2116
Plain Weave
Count: 60x58 (ends/in)
Thickness: 0.0038 (in)
Resin Content: 56%



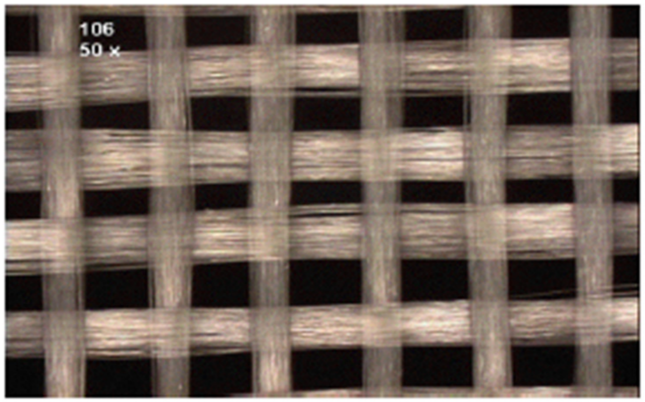
Glass Style: 1652
Plain Weave
Count: 52x52 (ends/in)
Thickness: 0.0045 (in)
Resin Content: 50%



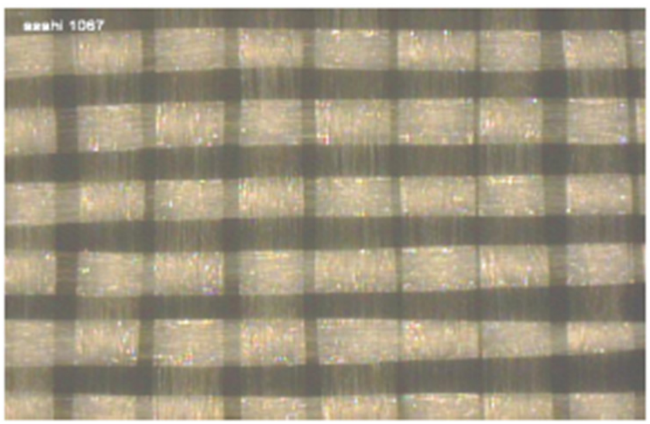
Glass Style: 7628
Plain Weave
Count: 44x32 (ends/in)
Thickness: 0.0068 (in)
Resin Content: 42%

*Plain weave yarn consists of yarns interlaced in an alternating fashion. One over and one under every yarn.

Standard and Spread Weave Examples



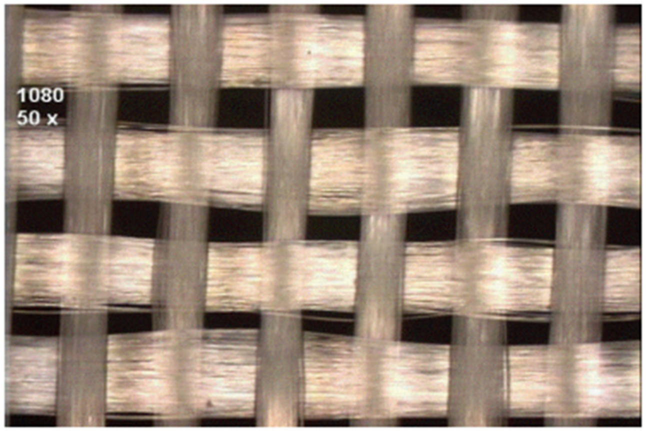
106
Warp & Fill Count: 56 x 56 (ends/in)
Thickness: 0.0015” / 0.038 mm



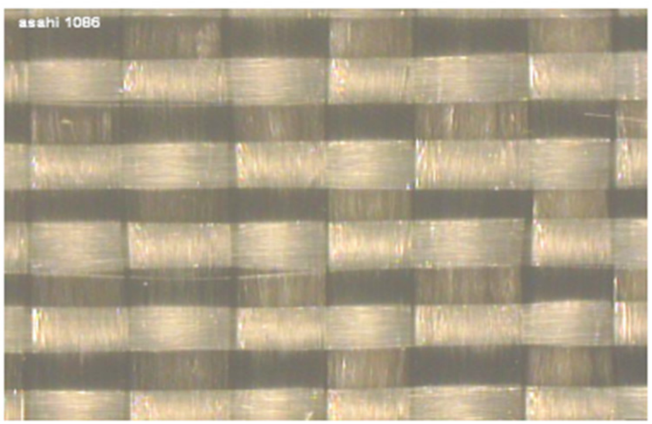
1067
Warp & Fill Count: 70 x 70 (ends/in)
Thickness: 0.0013” / 0.032 mm

Photos courtesy of Isola R & D Laboratories

Standard and Spread Weave Examples



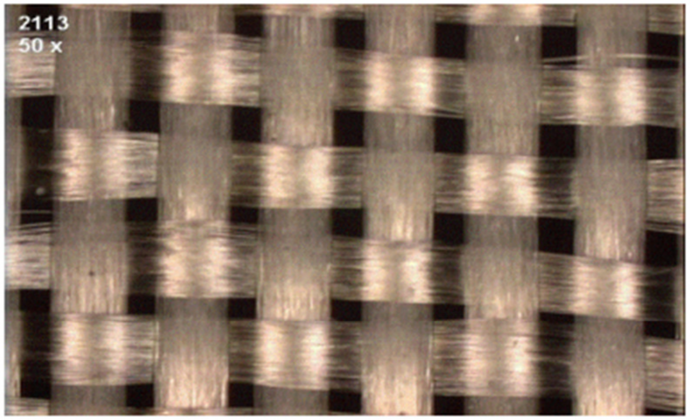
1080
Warp & Fill Count: 60 x 47 (ends/in)
Thickness: 0.0025” / 0.064 mm



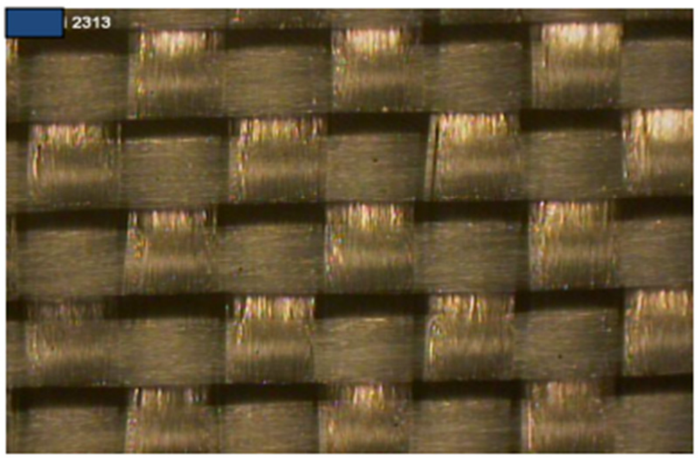
1086
Warp & Fill Count: 60 x 60 (ends/in)
Thickness: 0.002” / 0.050 mm

Photos courtesy of Isola R & D Laboratories

Standard and Spread Weave Examples



2113
Warp & Fill Count: 60 x 56 (ends/in)
Thickness: 0.0029” / 0.074 mm



2313
Warp & Fill Count: 60 x 64 (ends/in)
Thickness: 0.0032” / 0.080 mm

Photos courtesy of Isola R & D Laboratories

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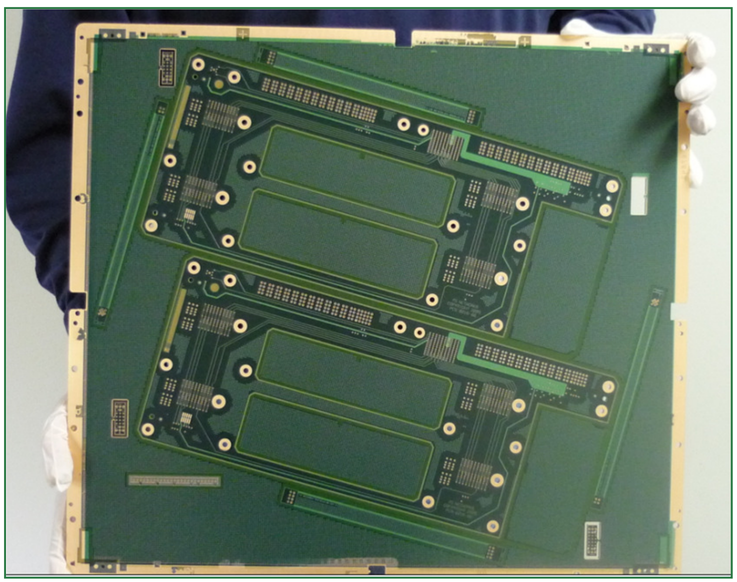
Fiber Weave Mitigation - Gerber Data Rotation

- Gerber rotation of the finished design
  - Rotate the finished Gerber design to a specific angle (usually 10 -15 degrees)
  - Causes the imaged data to be tilted within the manufacturing panel relative to the glass weave so it will always be “off bundle”
  - Can significantly impact PCB cost due to panel utilization reduction



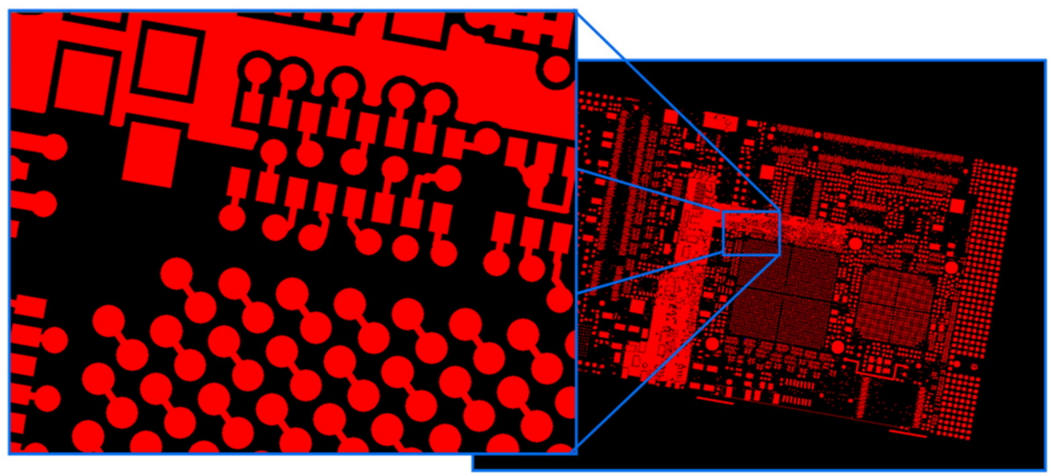
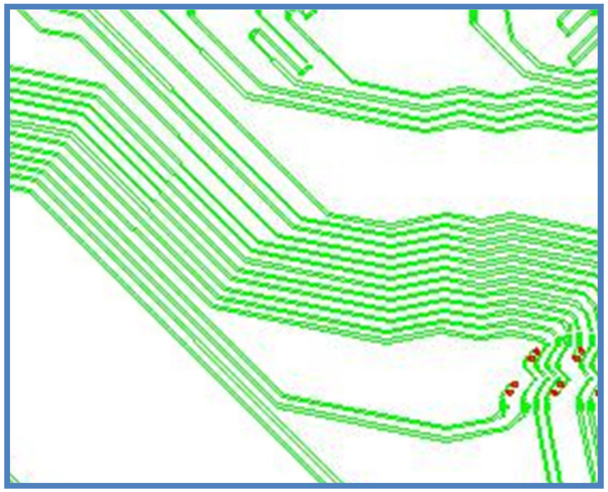


Illustration of gerber data that has been successfully rotated 10° within the CAM system.

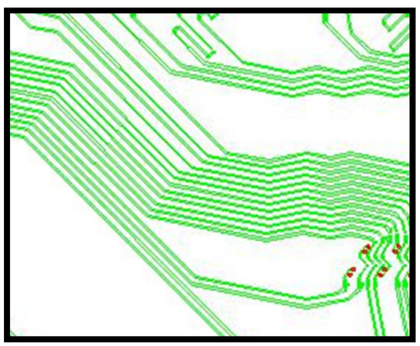
Fiber Weave Mitigation – Off Angle Routing

- Manually routing high speed circuitry at non-orthogonal angles such as zig-zag patterns, serpentine to assure they do not “track” or follow along the fiberglass yarn bundles.
  - Provides complete control from the design standpoint – no fabricator CAM editing required that can be prone to variation supplier to supplier
  - Complete assurance fiber weave is mitigated
  - Cost increase (from added design time) is absorbed one time and not over the life of the product as with other methods such as unique glass or panel utilization loss.

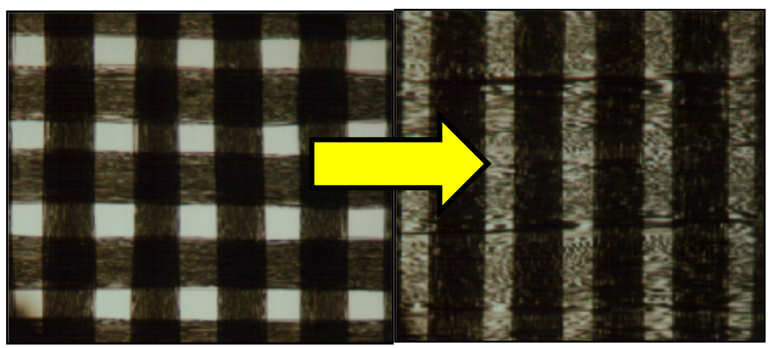


Fiber Weave Mitigation Options Summary

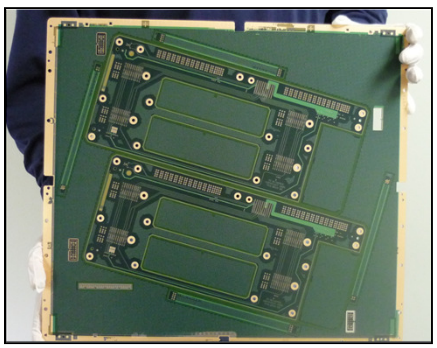
Mitigation Option	PCB Cost Impact	Mitigation Impact
Non Woven Laminate	High	Excellent
Close Glass Fabric Selection	None	Minimal
Spread Glass or LD Glass	Low to Med.	Good
Non Orthogonal Signal Routing	None	Excellent
Design Data Rotation	Low to High	Excellent



Off Angle Routing



Enhanced Glass Fabrics



10 degree data rotation

Signal Characteristics

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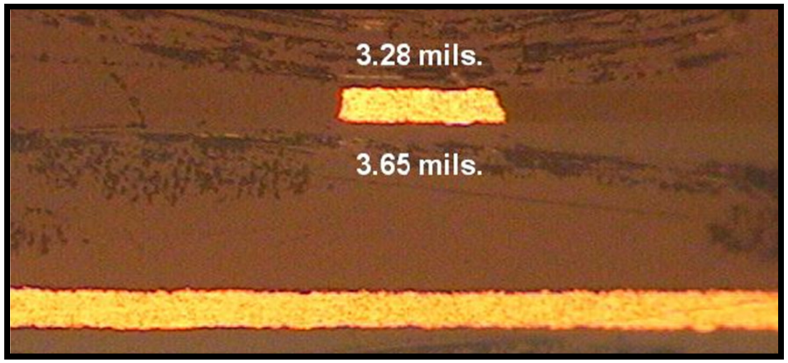
Signal Values & General Tolerances for Simulation Purposes

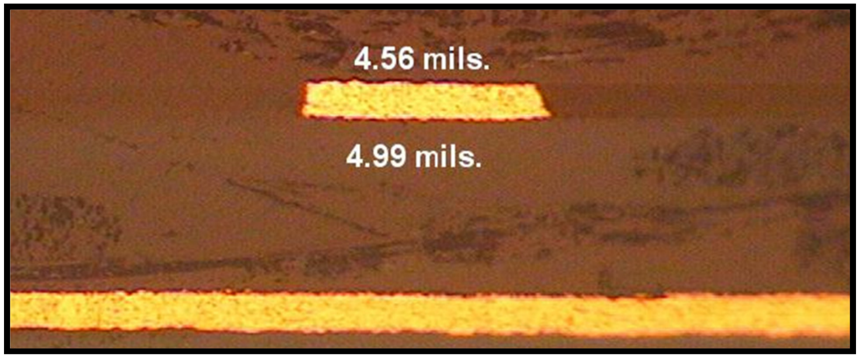
Characteristic	Tolerance - Value
Signal Width - Unplated	+/- .0005
Signal Thickness - Unplated	½ oz = .6 mils, 1 oz = 1.2 mils
Signal Width Plated	+/- .001 Typical
Signal Thickness Plated	1.8 – 2.7 mils (single plate)
Prepreg Thickness	+/- .001” Typical
Core Thickness	+/- .0005” Typical
Impedance	+/- 10%, +/- 7.5% with experience
Trapezoidal Signal Shape	See Subsequent Slides
Soldermask Df	.026
Soldermask Dk	3.87
Soldermask Thickness	.0007”

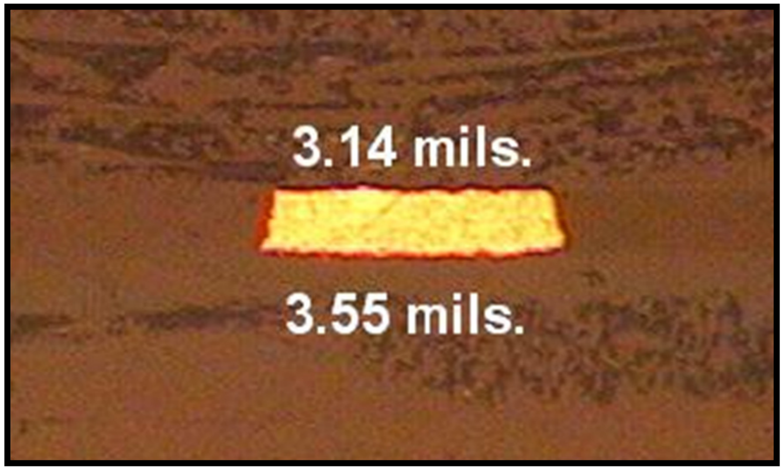
Typical Characteristics without wrap plating – review specific design guidelines

½ oz Copper Internal Signal Characteristics

- ½ oz copper trapezoid shape ~ .40 -.50 mils total
- Copper thickness ~ .55 -.65 mils

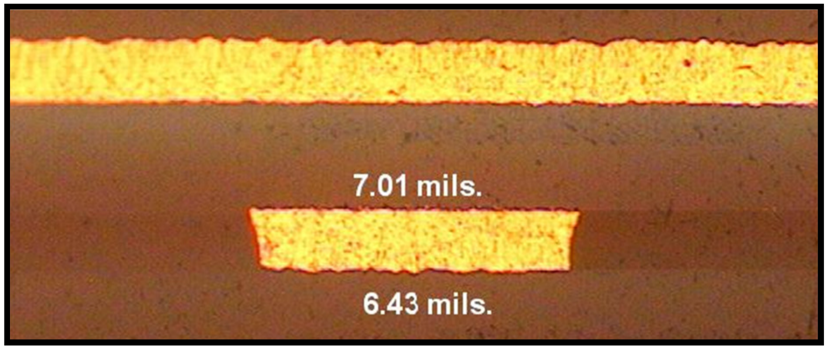


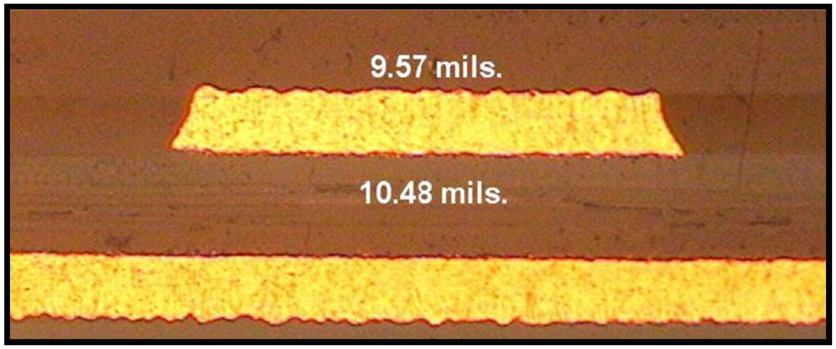


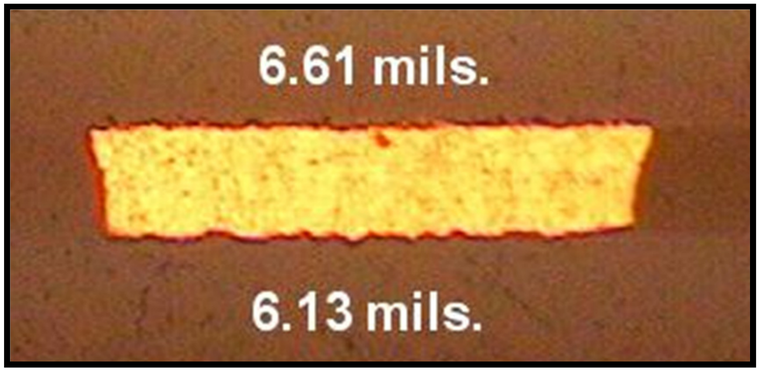


1 oz Copper Signal Internal Characteristics

- 1 oz copper trapezoid shape ~ .50 -.90 mils total
- Copper thickness ~ 1.10-1.25 mils







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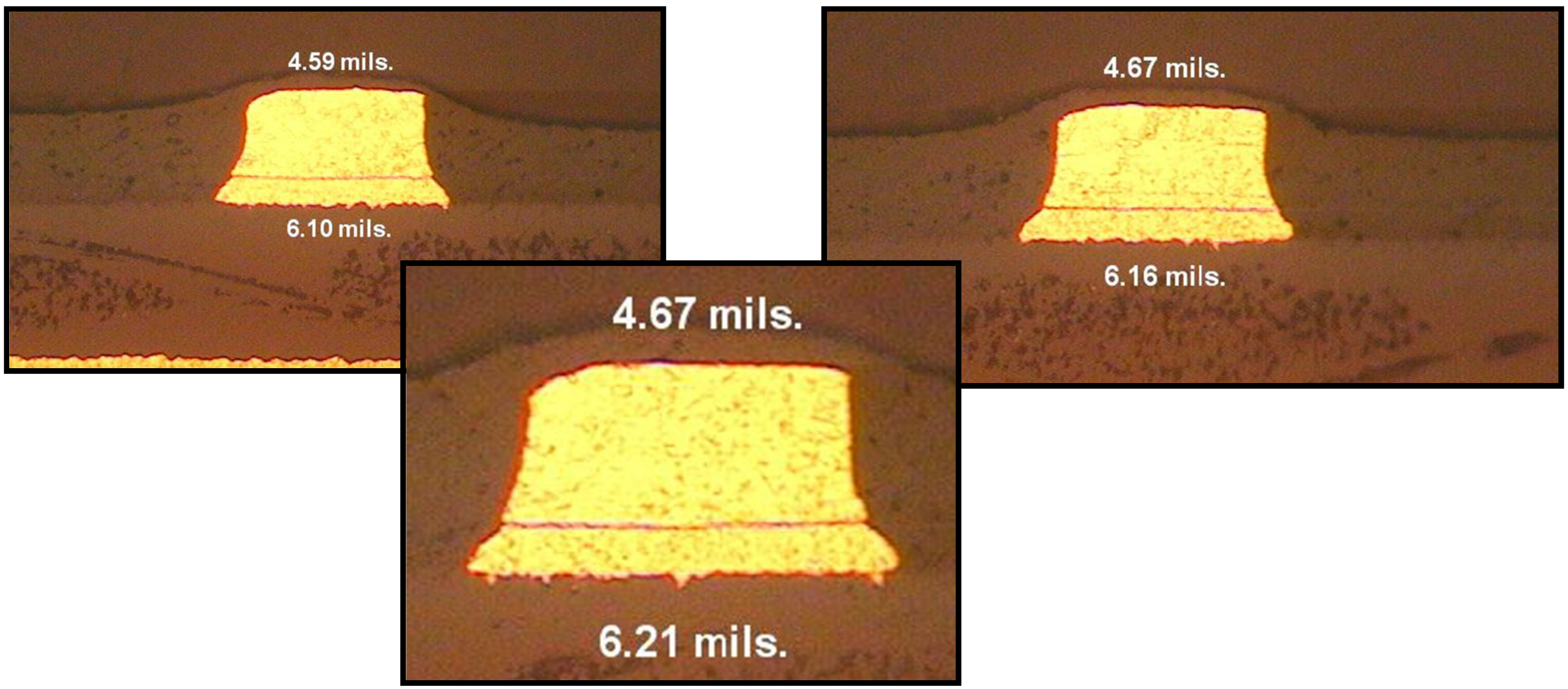
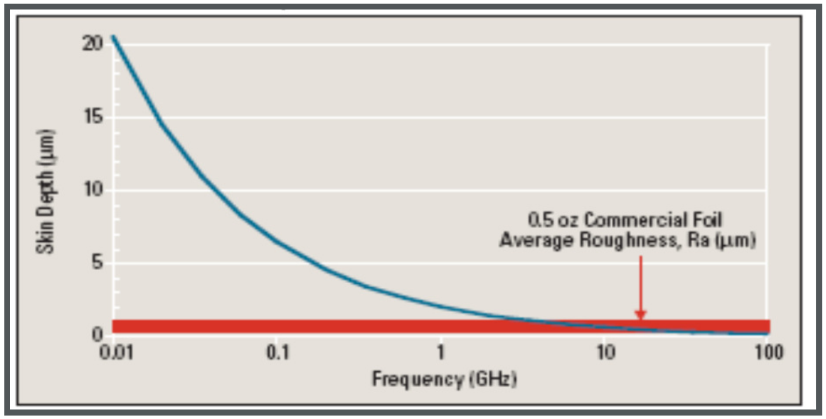
Plated Layer Signal Characteristics

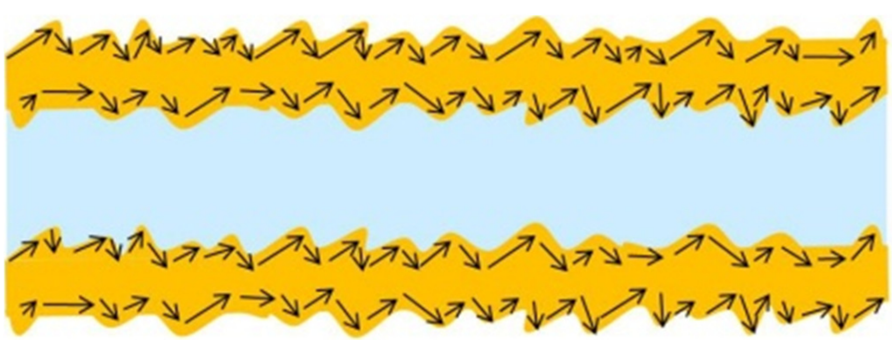
- Plated signal copper trapezoid shape ~ 1.25 -1.5 mils total
- Finished Copper thickness ~ 1.8-2.7 mils typically (½ oz starting foil)
- Assumes ½ oz copper foil + 1.2-2.0 mils plating (current density dpnt)

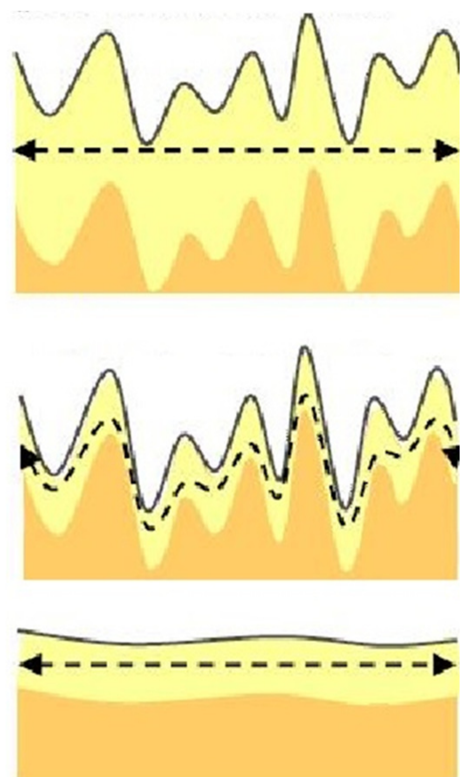


Internal Copper Foil Roughness
Skin Depth / Effective Track Length

- **Copper roughness versus signal quality**
  - As signal speeds increase the signal moves closer to the surface "skin depth"
  - Improvements ***must not*** sacrifice bond







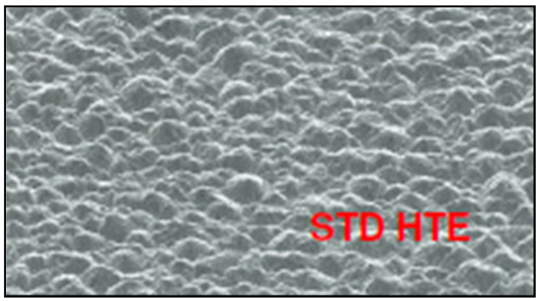
Low Frequency

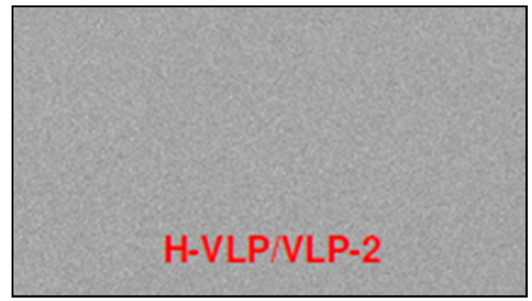
High Frequency

High Frequency (preferred)

Copper Roughness – Balancing Signal Integrity with Reliability

- Smooth copper foils are desired for electrical performance but must be balanced with adhesion and reliability
- Industry standards have not kept pace with the variety of foils





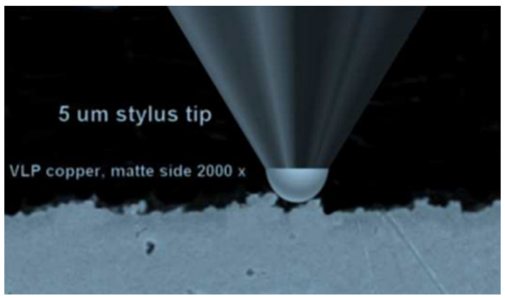
Foil Profile Type	Max. Foil Profile (Microns)	Max. Foil Profile (μ Inches)
S – Standard	N/A	N/A
L – Low Profile	10.2	400
V – Very Low Profile	5.1	200
X – No Treatment or Roughness	N/A	N/A

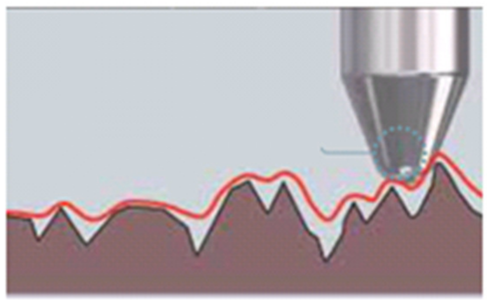
IPC 4562 Sub-Committee 3-12A is addressing HVLP, RTF, foil types

Note: No Provisions for RTF or HVLP

IPC Committee 3-12A currently working on a NDT Method

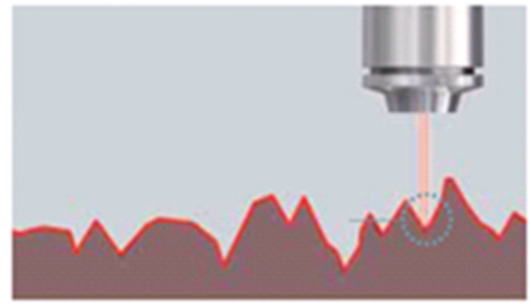
IPC and Team has established a NIST Standard





Low mag lens, larger beam spot, high S-filter value

vs.



High mag lens, smaller beam spot, low S-filter value

Spec for NDT test method passed GR & R study. Spec was written and submitted for approval to IPC (Next step would be to submit test method and standards to NIST)

Copper Foil Roughness Examples (core side)

Material Type	Standard Copper Roughness (µm)		RTF Copper Roughness (µm)		VLP Copper Roughness (µm)		HVLP Copper Roughness (µm)	
	0.5 oz	1.0 oz	0.5 oz	1.0 oz	0.5 oz	1.0 oz	0.5 oz	1.0 oz
Low Loss E	NA	NA	NA	NA	≤ 4.0	≤ 5.0	NA	NA
Low Loss K	NA	NA	NA	NA	NA	NA	≤ 2.0	≤ 2.0
Low Loss M	6.0	8.0	4.0	5.0	NA	NA	1.5	1.5
Low Loss G	6.0	8.0	4.0	5.0	NA	NA	1.5	1.5

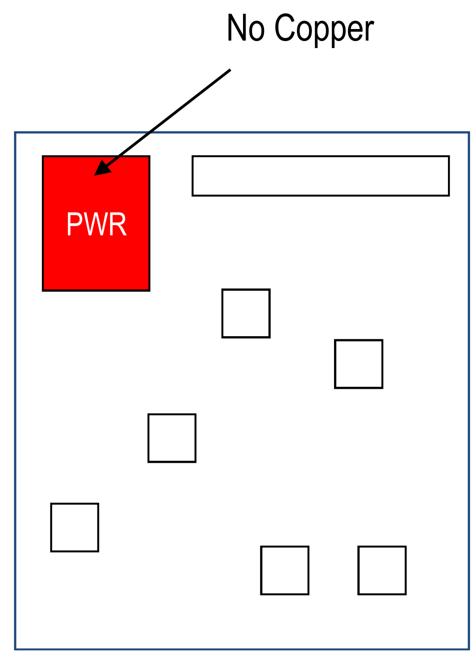
PCB Density Analysis

PCB Simulation Tool - Density Analyzer Design Rule Check

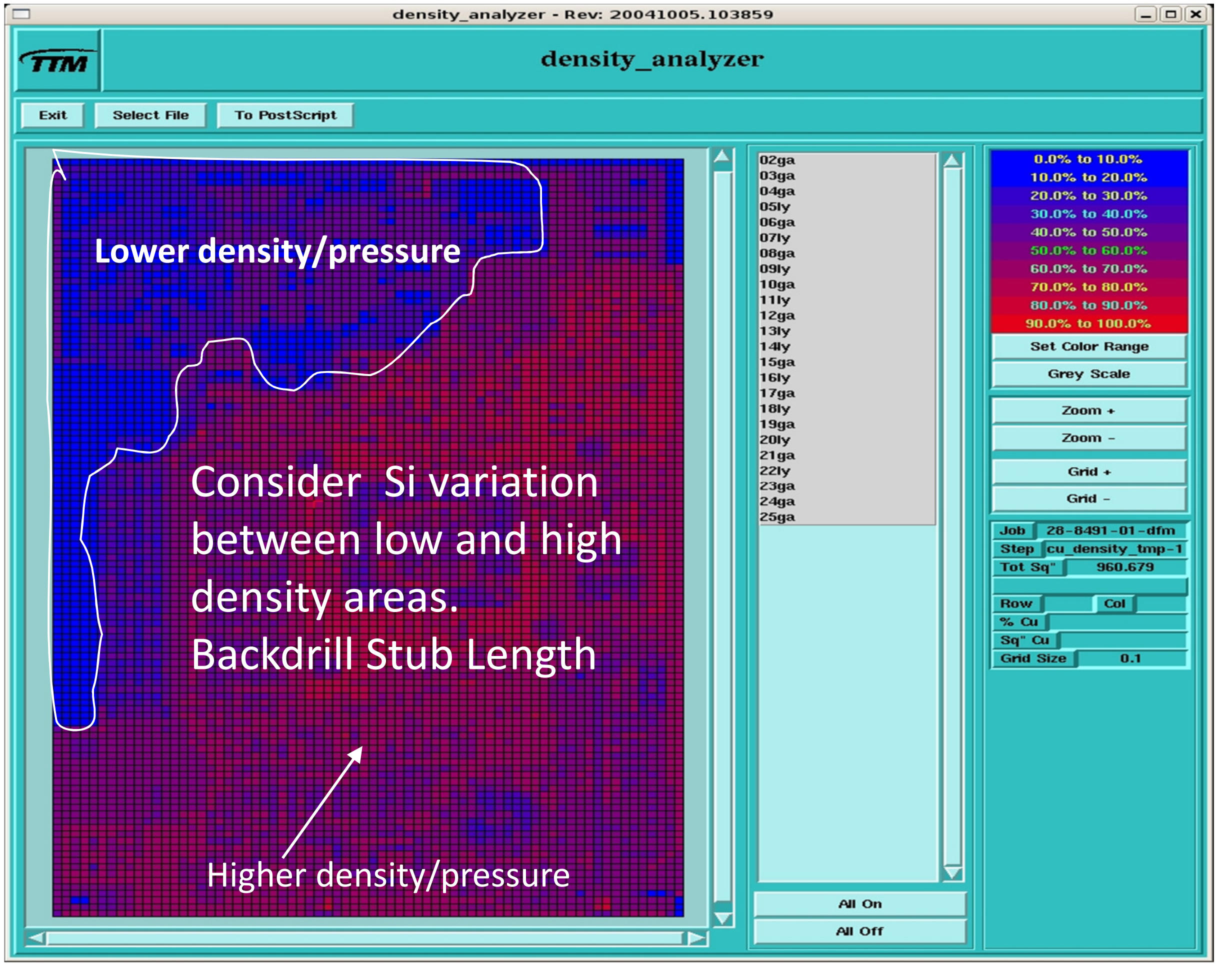
- **Synopsis**
  - Analyze, prior to fabrication, the copper density of the entire PCB structure in all three axis to identify variations such that either manufacturing or design modifications can be made to improve yield and/or Si performance

- **Inspiration and drivers for capability**
  - Increasing layer count high speed data products
  - Thinner dielectrics, < 4.0 mils all layers
  - Thicker copper, 1 oz signals and 2 oz planes
  - Large form factor, 20 inch parts – very long signals
  - Slow/low flow lead free and low loss materials

Cross section of severe density variation in a 10 layer PCB



Density Analyzer – PCB Density Analysis Matrix



- Provides a composite image of the total copper density for all layers with variation indicated by color shading
- Density Analysis is the basis for requesting internal layer thieving to improve prepreg thickness variation

Interconnects Backdrilling

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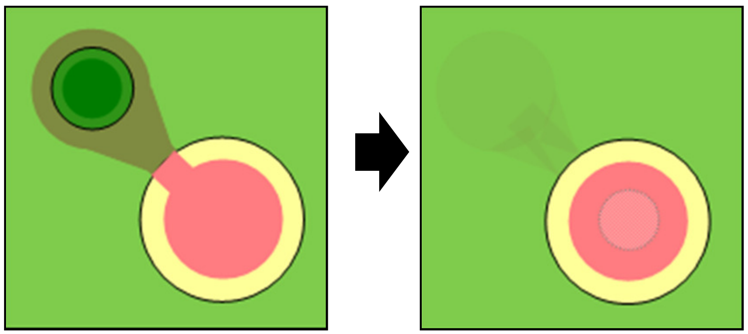
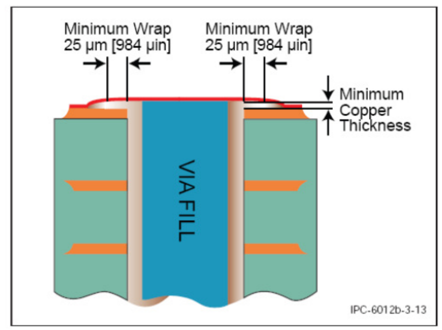
Typical Methods to Improve High Speed Interconnects

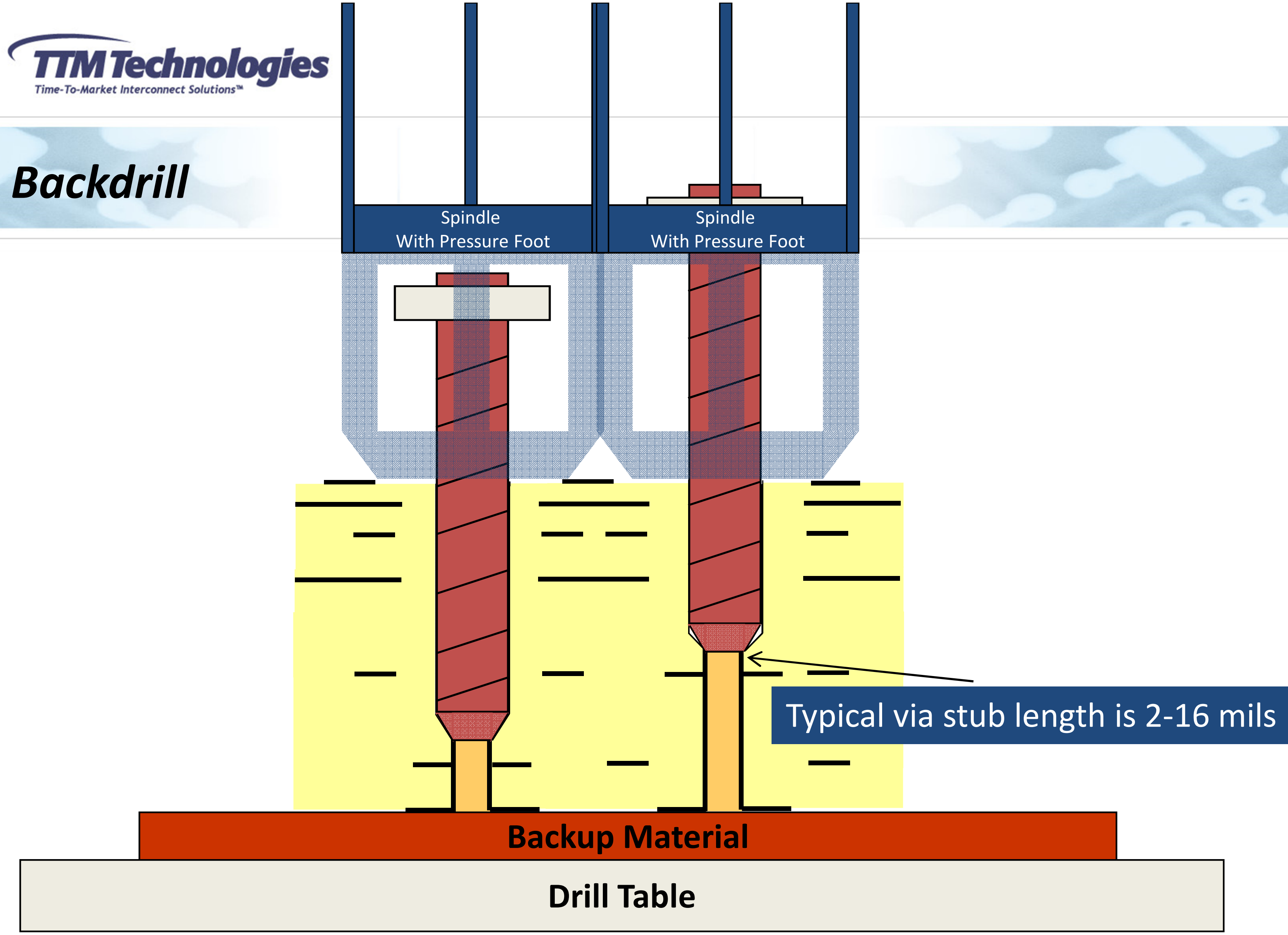
- **Via in Pad Plated Over (VIPPO)** – eliminates the dog bone (stub)





- **Backdrilling (counter-boring)**
  - Improvements to achieve 7 +/-5 mils (12 mil max stub length) in development/prototypes (more on this on another slide)
- **Blind Vias** (direct from device pads to routing layer with no stub)
  - Most accurate and direct approach however has significant cost implications
  - Can be formed using controlled depth drilling, laser drilling or mechanically drilled using sequential lamination process (more on this on another slide)

Backdrill



Spindle
With Pressure Foot
Spindle
With Pressure Foot
Typical via stub length is 2-16 mils
Backup Material
Drill Table

Backdrilling Impact on Insertion Loss - Example

Item	Layer	Pass/Fail	Loss @4GHz (dB/inch)	Max Loss @ 4GHz	Loss @8GHz (dB/inch)	Max Loss @ 8GHz	Impedance (Ohms)
No Backdrill	L7	Fail	0.463	0.48	0.983	0.96	89.8
	L9	Fail	0.478	0.48	1.063	0.96	91.4
	L14	Fail	0.463	0.48	1.048	0.96	91.3
	L16	Fail	0.475	0.48	0.994	0.96	90.4
Backdrill	L7	Pass	0.45	0.48	0.902	0.96	92.1
	L9	Pass	0.444	0.48	0.871	0.96	91.5
	L14	Pass	0.446	0.48	0.89	0.96	91.6
	L16	Pass	0.446	0.48	0.896	0.96	90.4

- Material – EMC EM-888
- Board thickness - .112”
- 22 layers

Backdrilling Design Guideline

- Development work in process to improve +/- 7 mil depth control to +/- 5 mils or better

Back Drill Design Guideline | January 2012

Legend	Item	Target	Tolerance	TTM Current
d1	Primary Drill Diameter (Non-Plated)	Per Primary Drill File	Per Primary Drill File	Per Primary Drill File
d2	Back Drill Diameter	Per Back Drill File	+/- 0.002" (0.05mm)	D1+ .008" preferred D1+ .006" abs min
d3	Antipad Diameter	d2 +0.020" (0.50mm)	+/- 0.002" (0.05mm)	D2+ .016" minimum (.008" min hole to metal)
d4	Back Drill to adjacent copper features (trace or copper plane)	See Tolerance	No evidence of exposed copper in back drill area. Tangency is not allowed.	.008" min hole to metal
h1	Stub Length	.009" (.229mm) from MNC surface	+/- 0.007" (.127mm)	.002" - .016" from MNC layer
h2	Back Drill Depth	Cannot hit MNC layer	+/- 0.007" (0.20mm)	If stack-up and print tolerance will allow, we prefer .009" min. from MNC layer

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Insertion Loss Testing at the PCB Fabrication Level

- Measuring PCB insertion loss at the fabrication stage is not practical using tools such as a VNA – generally considered a lab level assessment
- TTM has multiple facilities in both NA and AP with insertion loss measurement capability including SPP and SET2DIL
- Measuring loss currently remains a specialized capability both generally in the industry as well as at TTM
- When a product has critical performance requirements in terms of loss we need it to be specified as a dB loss per inch at X frequency
- Assuming all of the characteristics we just spoke of are maintained gives you a sense of good performance but unless it is validated through measurement it will not be certain – similar to TDR

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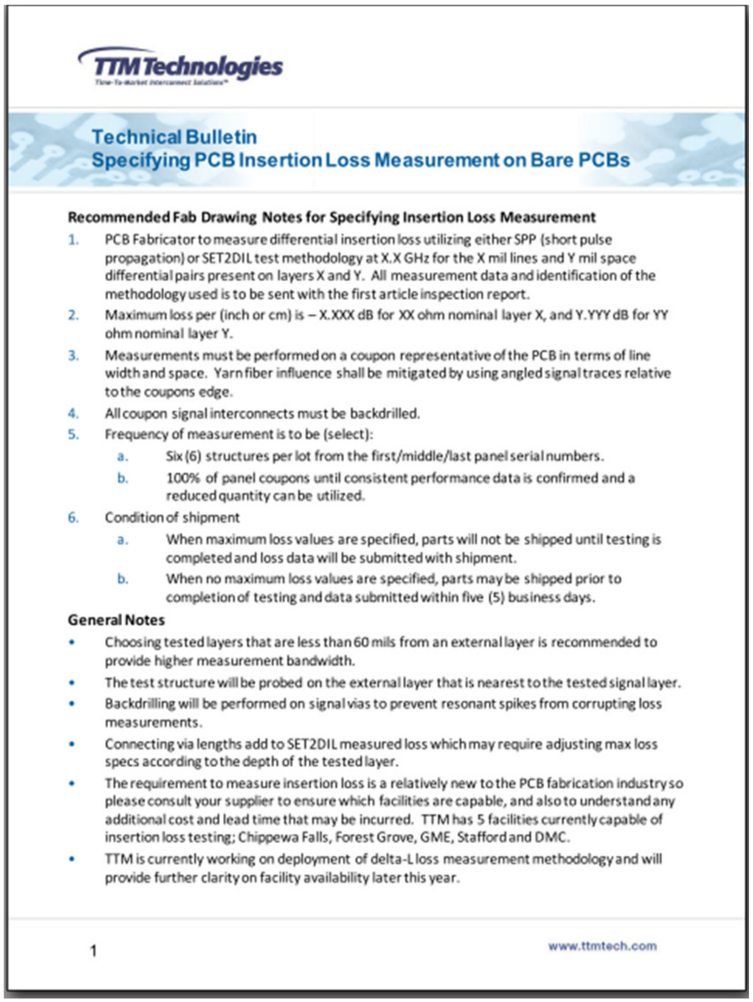
Insertion Loss Tech Bulletin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Technical Bulletin
Specifying PCB Insertion Loss Measurement on Bare PCBs

Recommended Fab Drawing Notes for Specifying Insertion Loss Measurement

1. PCB Fabricator to measure differential insertion loss utilizing either SPP (short pulse propagation) or SET2DIL test methodology at X.X GHz for the X mil lines and Y mil space differential pairs present on layers X and Y. All measurement data and identification of the methodology used is to be sent with the first article inspection report.
2. Maximum loss per (inch or cm) is – X.XXX dB for XX ohm nominal layer X, and Y.YYY dB for YY ohm nominal layer Y.
3. Measurements must be performed on a coupon representative of the PCB in terms of line width and space. Yarn fiber influence shall be mitigated by using angled signal traces relative to the coupons edge.
4. All coupon signal interconnects must be backdrilled.
5. Frequency of measurement is to be (select):
   a. Six (6) structures per lot from the first/middle/last panel serial numbers.
   b. 100% of panel coupons until consistent performance data is confirmed and a reduced quantity can be utilized.
6. Condition of shipment
   a. When maximum loss values are specified, parts will not be shipped until testing is completed and loss data will be submitted with shipment.
   b. When no maximum loss values are specified, parts may be shipped prior to completion of testing and data submitted within five (5) business days.

General Notes

- Choosing tested layers that are less than 60 mils from an external layer is recommended to provide higher measurement bandwidth.
- The test structure will be probed on the external layer that is nearest to the tested signal layer.
- Backdrilling will be performed on signal vias to prevent resonant spikes from corrupting loss measurements.
- Connecting via lengths add to SET2DIL measured loss which may require adjusting max loss specs according to the depth of the tested layer.
- The requirement to measure insertion loss is a relatively new to the PCB fabrication industry so please consult your supplier to ensure which facilities are capable, and also to understand any additional cost and lead time that may be incurred. TTM has 5 facilities currently capable of insertion loss testing; Chippewa Falls, Forest Grove, GME, Stafford and DMC.
- TTM is currently working on deployment of delta-L loss measurement methodology and will provide further clarity on facility availability later this year.

1 www.ttmtech.com

- Provides guidance on fab drawing notes and language to be used
- Working on deployment of Delta-L methodology

TTM Technologies is working to provide advanced, reliable, cost effective technology solutions for current and future PCB requirements

Thank You for Attending

Q & A