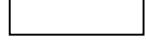


MAIN
main.SchDoc



MECH
mechanical.SchDoc



NOTE: DO ECPS DESIGN CHECKLIST!
NOTE: ANALYZE JTAG PULL-UPS/DOWNS
NOTE: ANALYZE DDR3 TERMINATION

A
A

Todo:

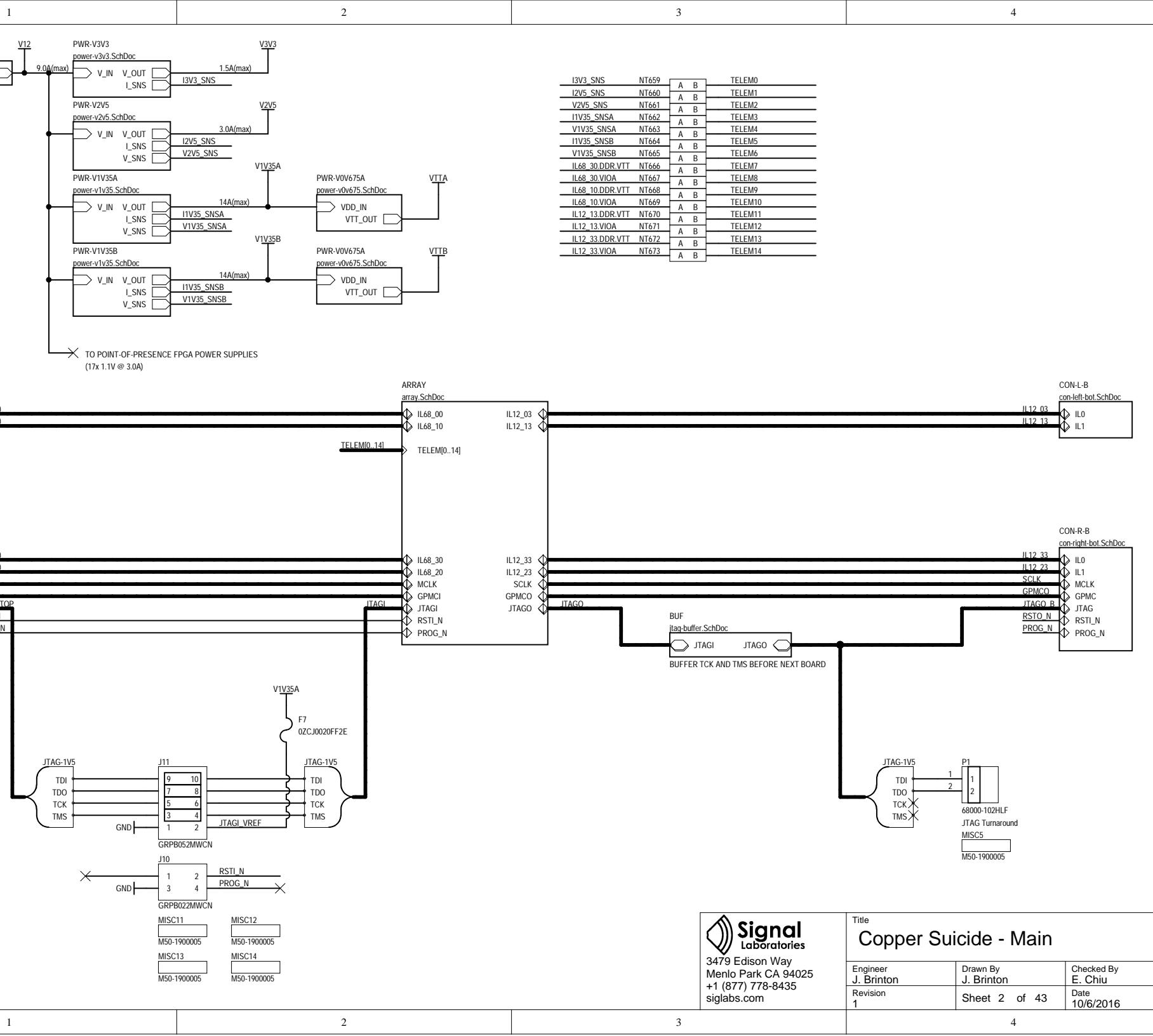
Done- ** pins need to get mapped to connectors
 Done- ** pins need to get mapped between fpgas (see map.SchDoc)
 Done- ** need soft reset buffer
 Done- ** need high-speed clock buffer
 Done- ** would like to use right angle "programming jumpers (J7)" to access JTAG when boards are stacked.
 Done- ** would like to add some LEDs
 * component placement
 ** can hopefully use some tricks to copy routing across FPGAs (rooms don't work on "sub parts spread across multiple child sheets in hierarchical design")
 * routing
 * review (especially of configuration and programming)
 Done- 5V supply has caps from low side gate to drain. This has to be a mistake
 Done- Swapping groups for DDR data lines (only within DQS group)
 Done- Check power to unused SERDES
 Done- Add global (non-GPMC) bus between all array FPGAs
 Done- Mclk source needs to be pinned out on connector J3
 Done- V48 needs to be pinned out on J3
 Done- Add 3.3V power supply (linear reg)
 Done- DDR3 chip termination R packs are 39k??
 Done- Add reset button
 Done- Change 2.5V switcher inductor to 3A
 Done- Add jumper on 48V in
 Done- Add power input barrel jack
 Done- Add current sense resistors on supply rail PS outputs
 Done- Add local JTAG connector to access entire board JTAG chain
 Done- Review for single board operation

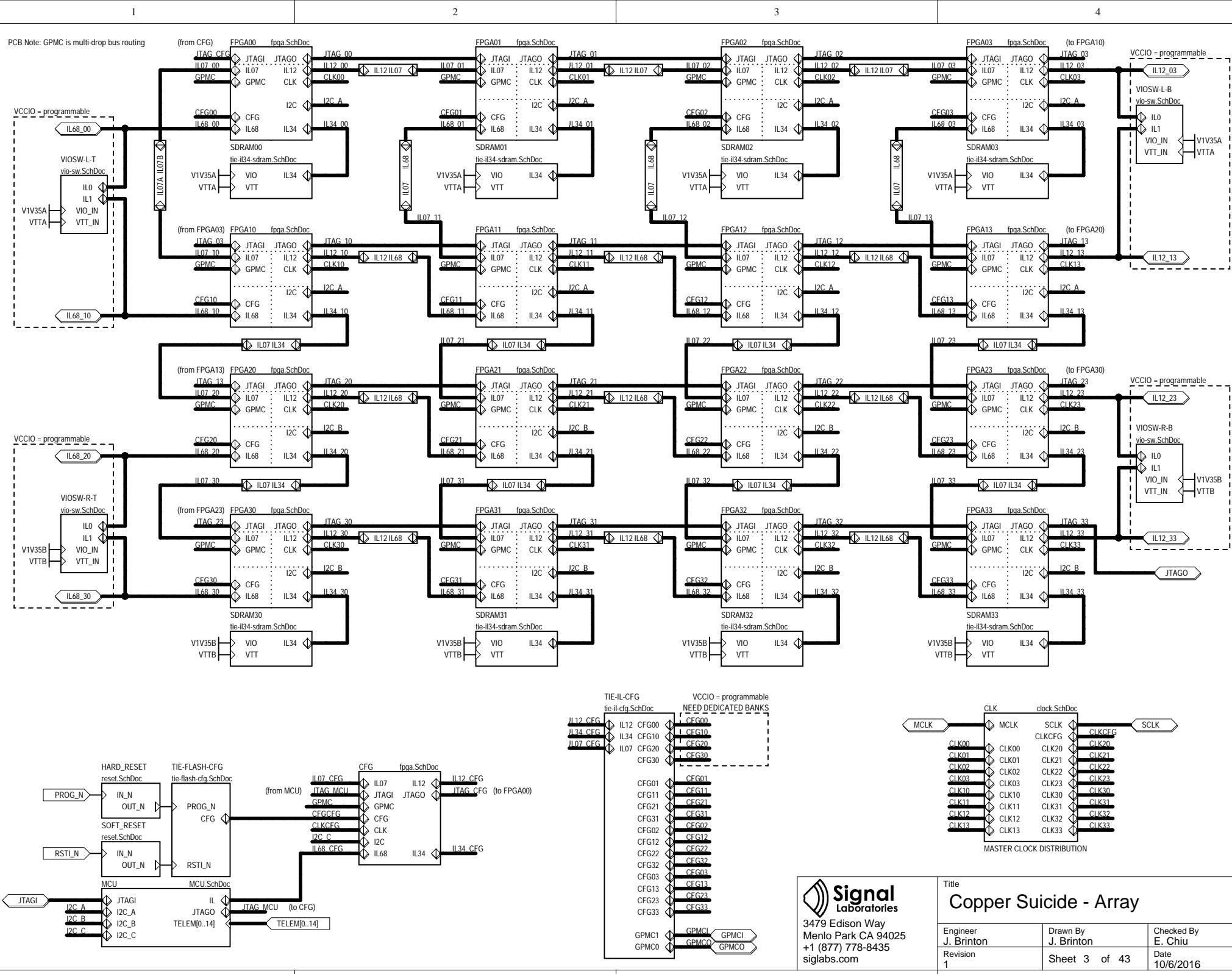
B
B

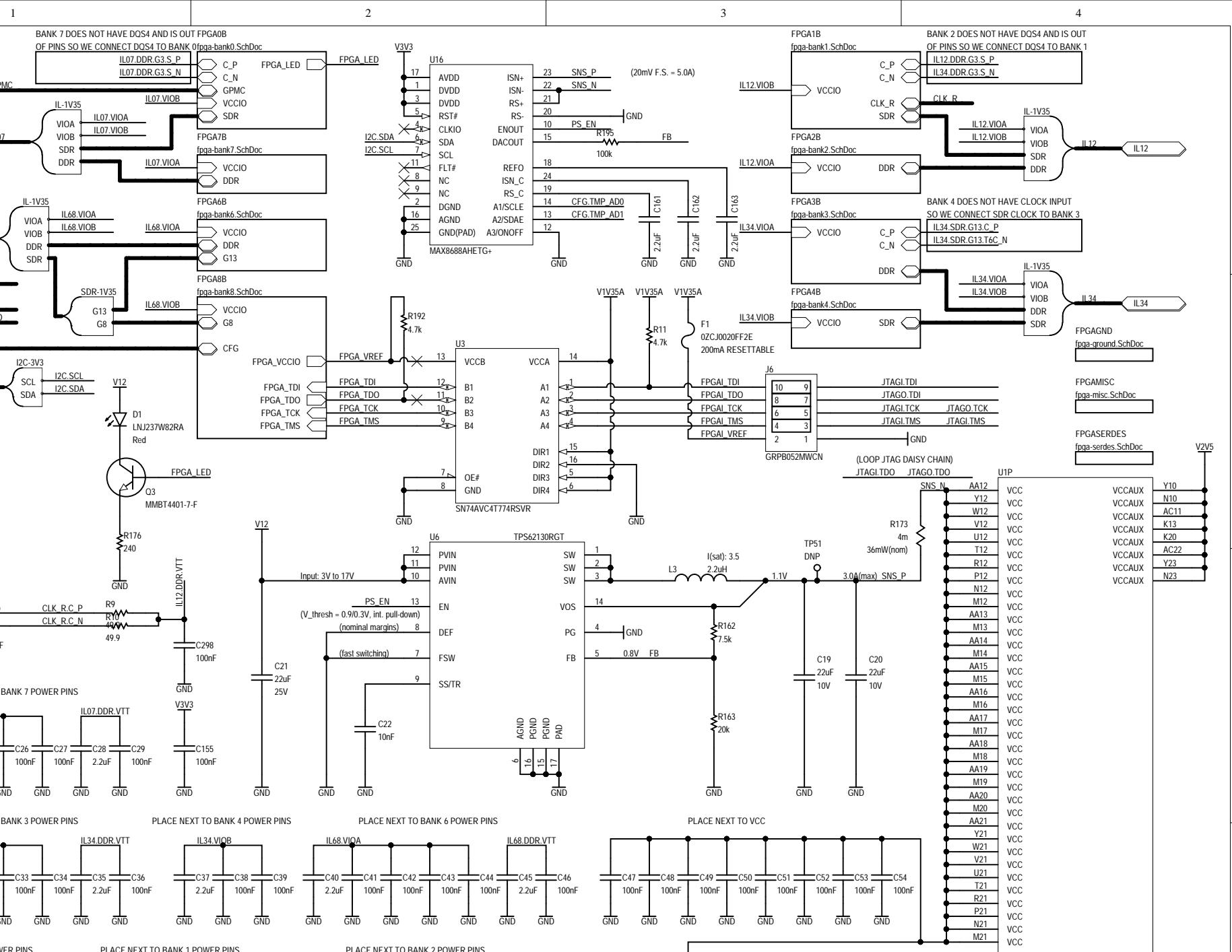
Done:
 DDR3 checked

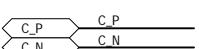
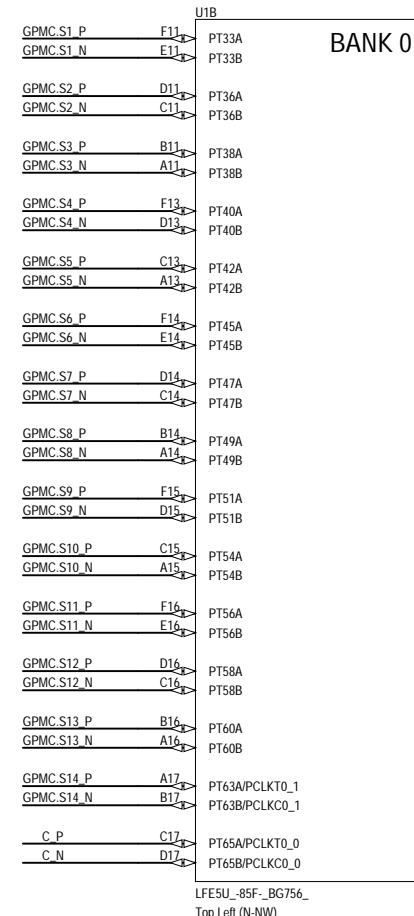
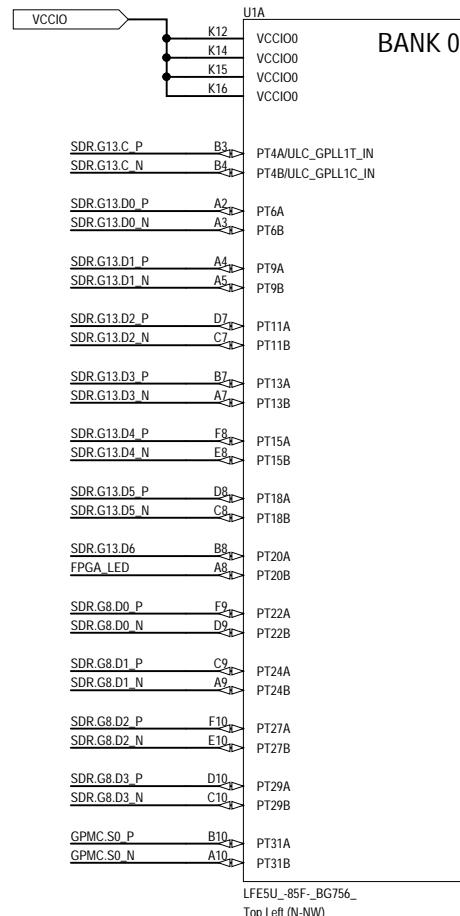
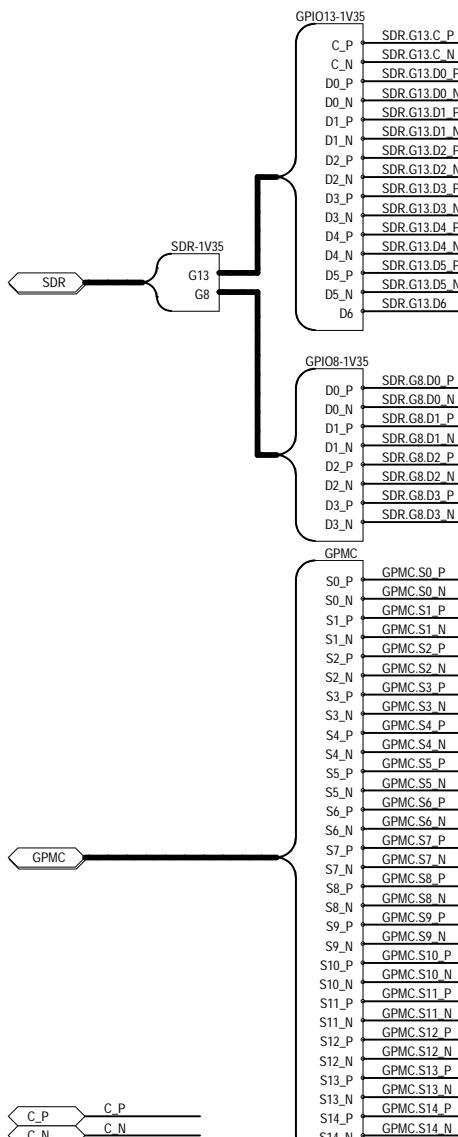


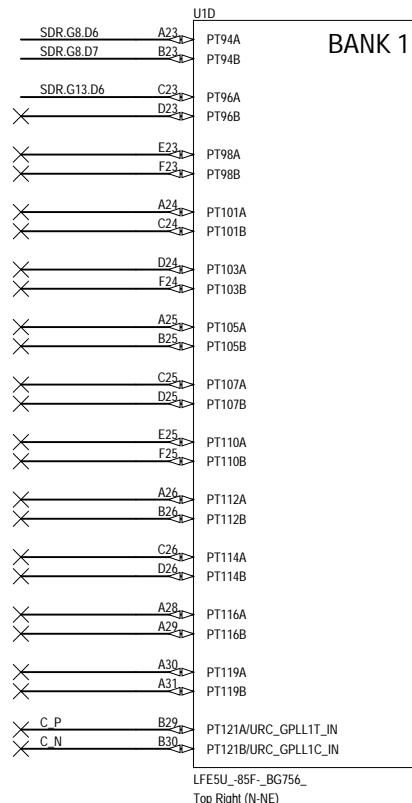
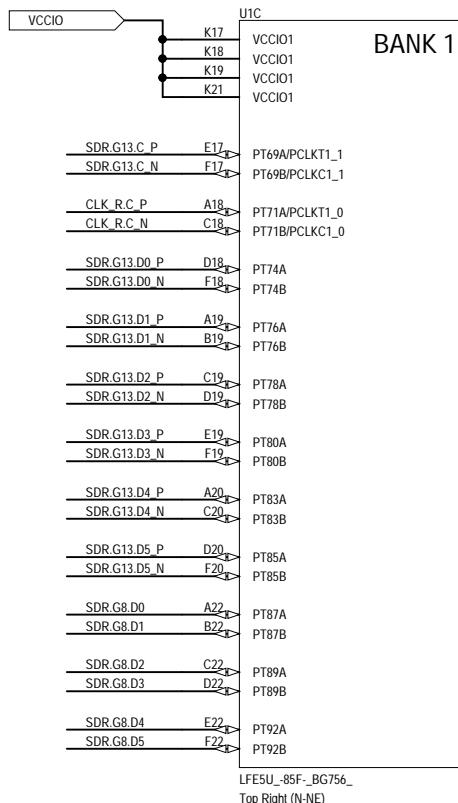
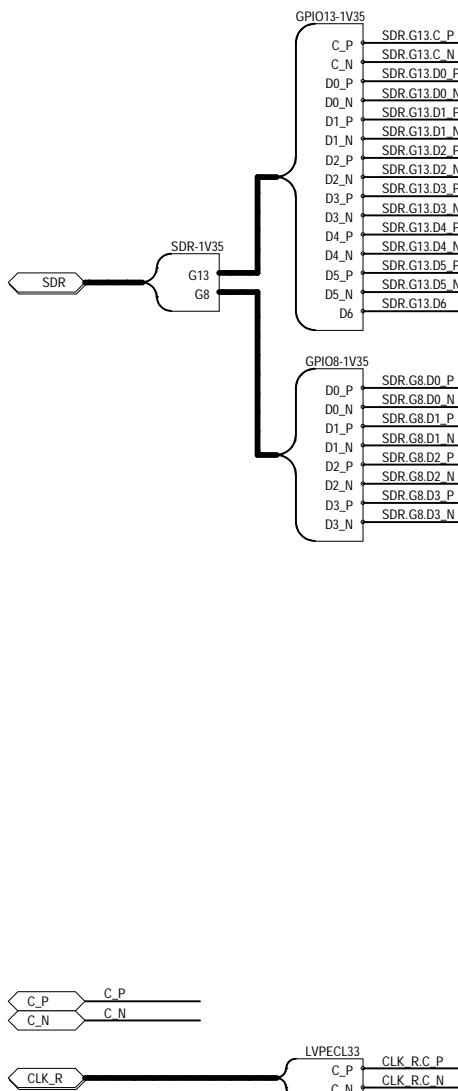
Title		
Copper Suicide - Top		
Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision	Sheet 1 of 43	Date
1		10/6/2016

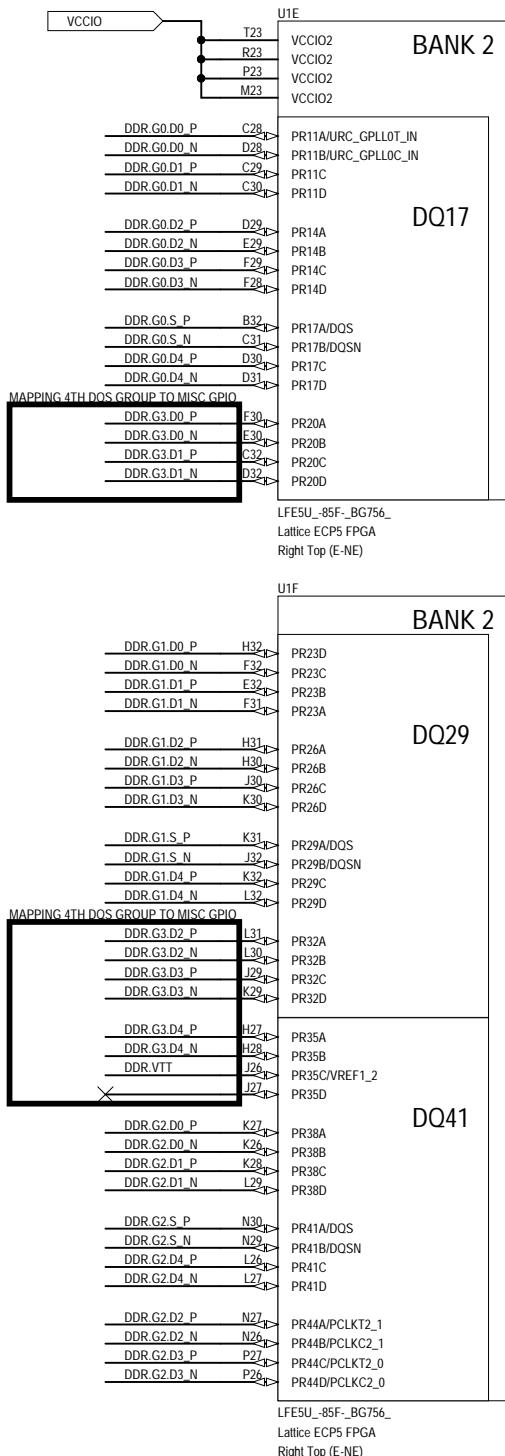
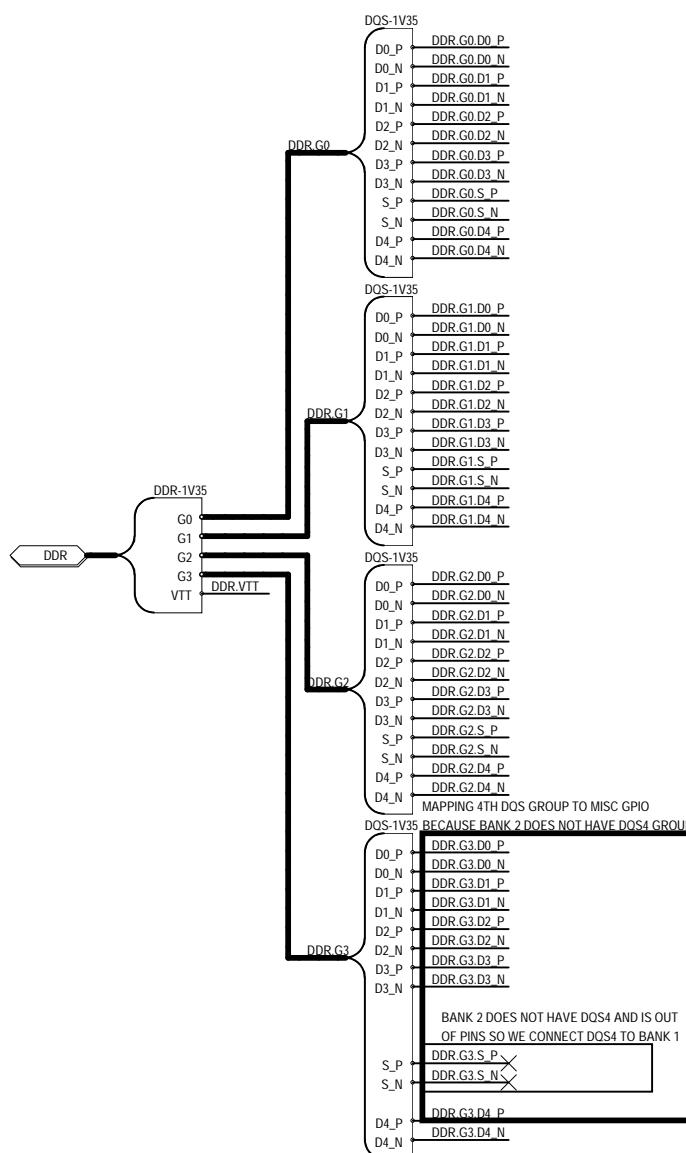


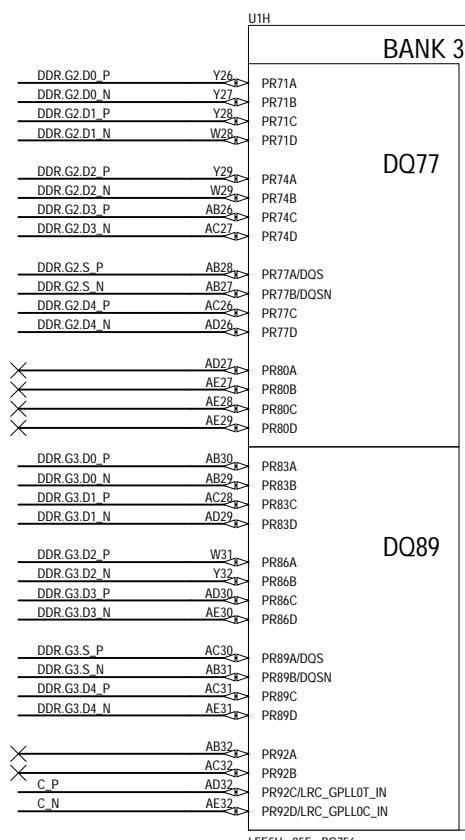
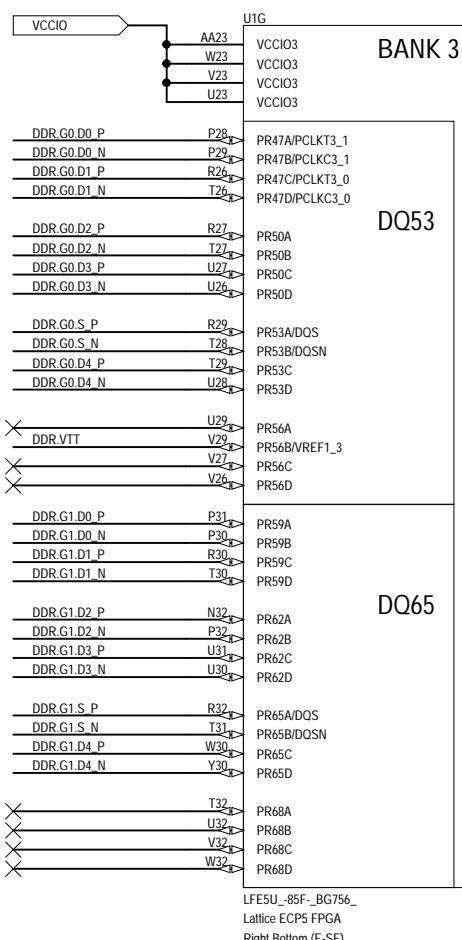
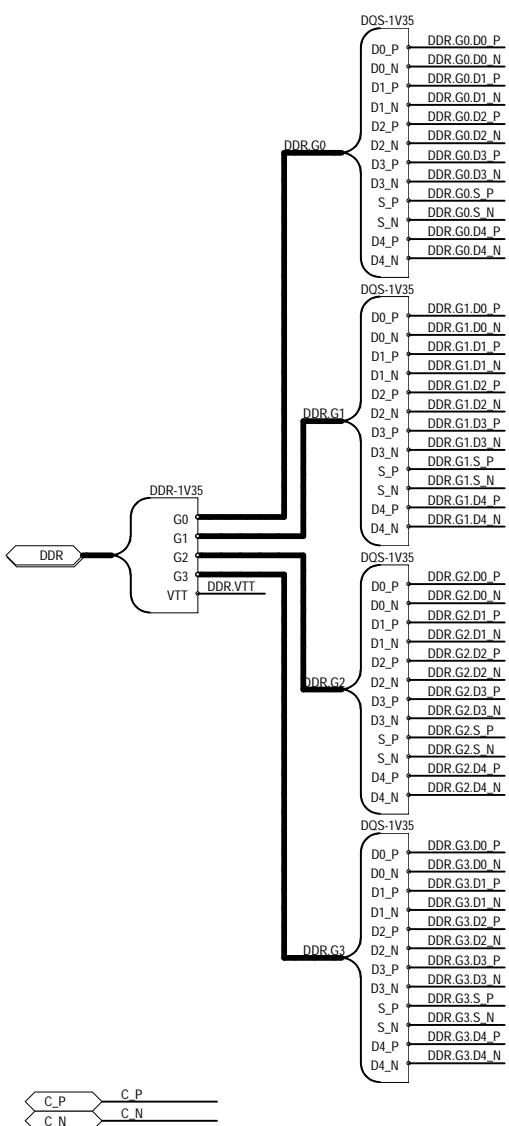


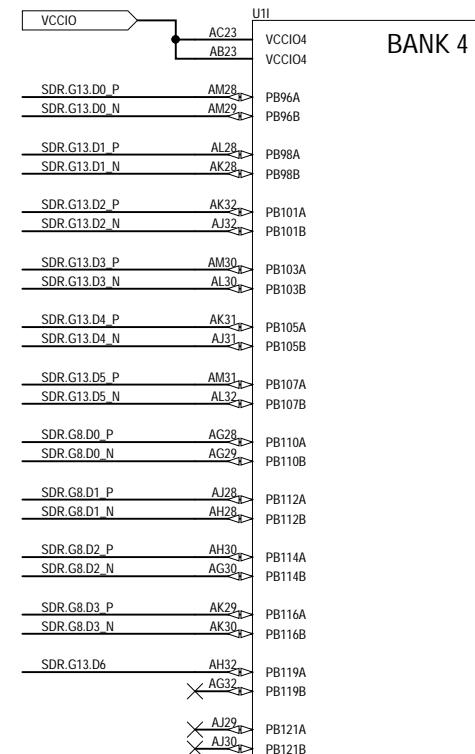
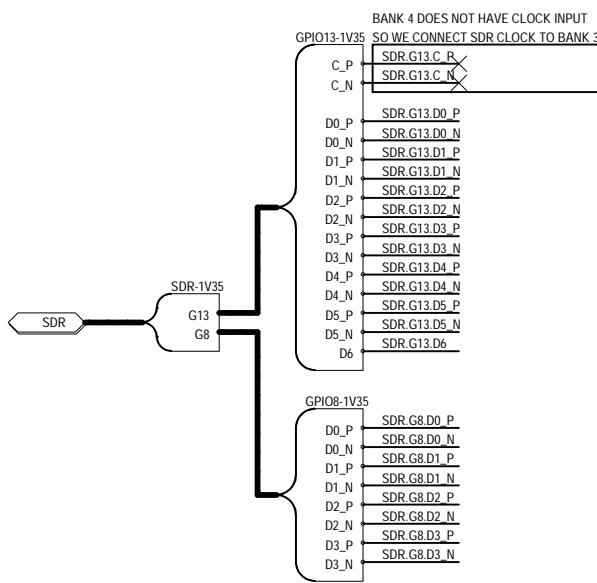


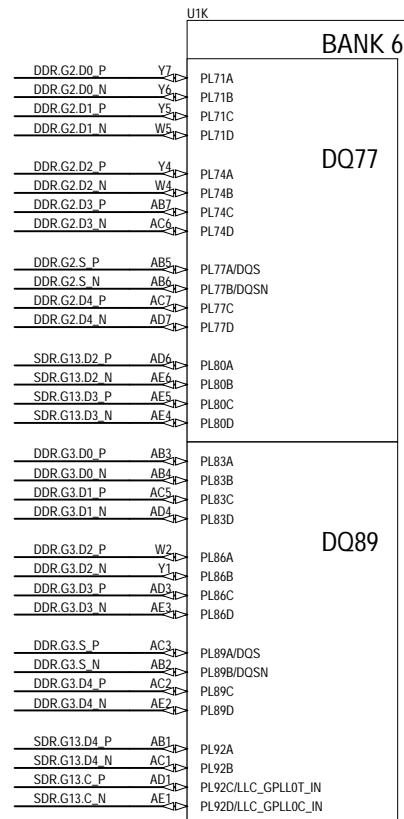
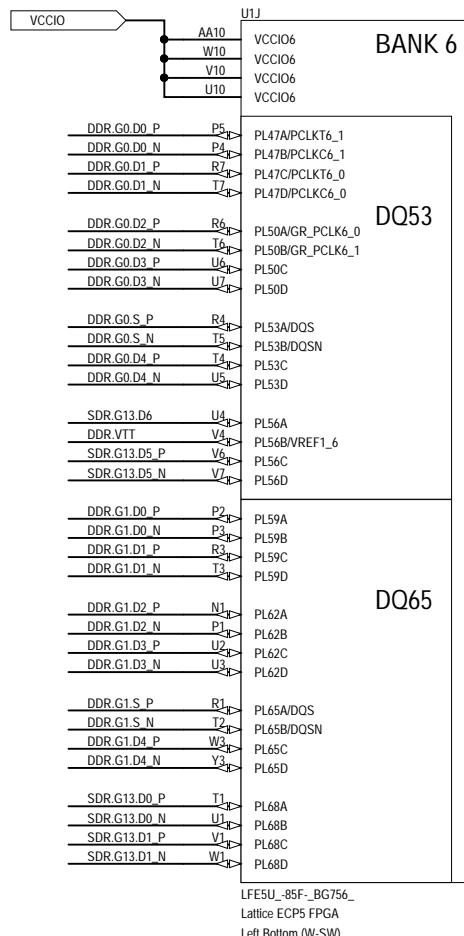
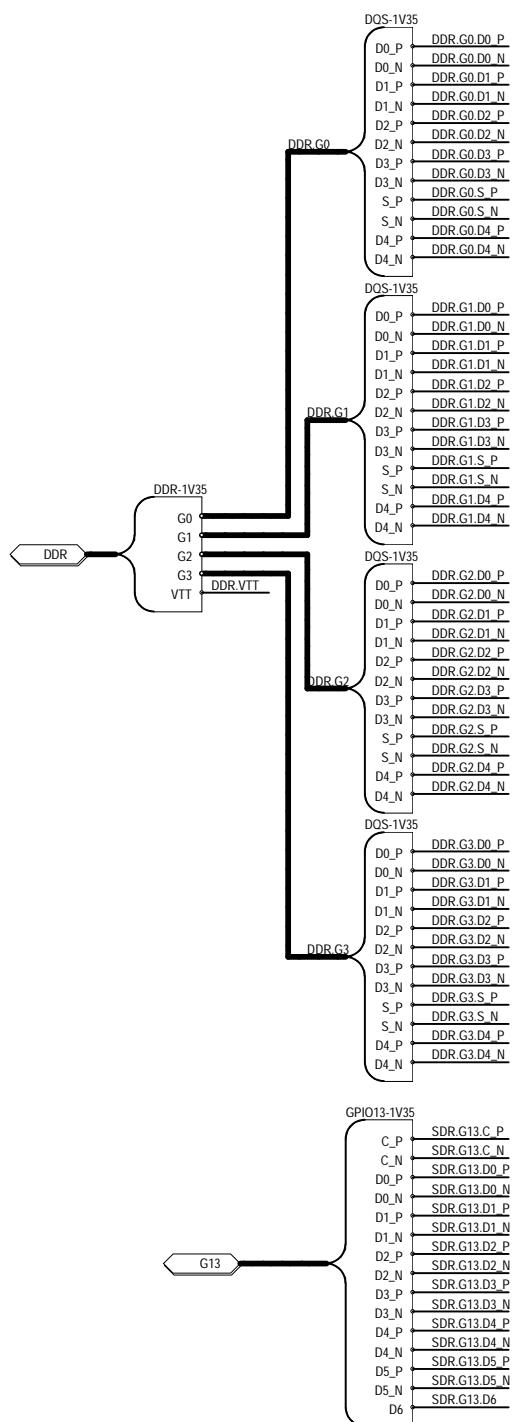


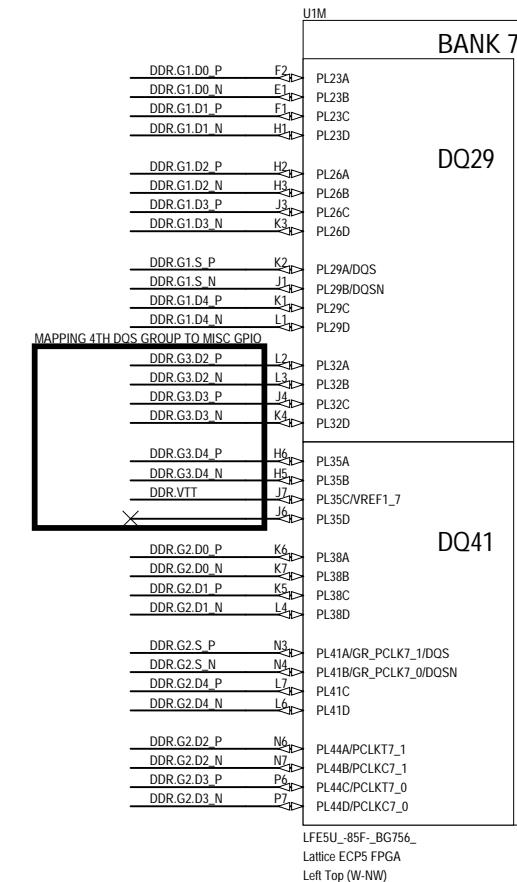
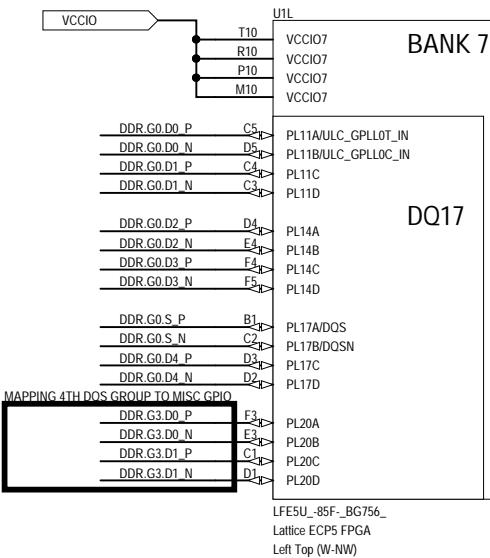
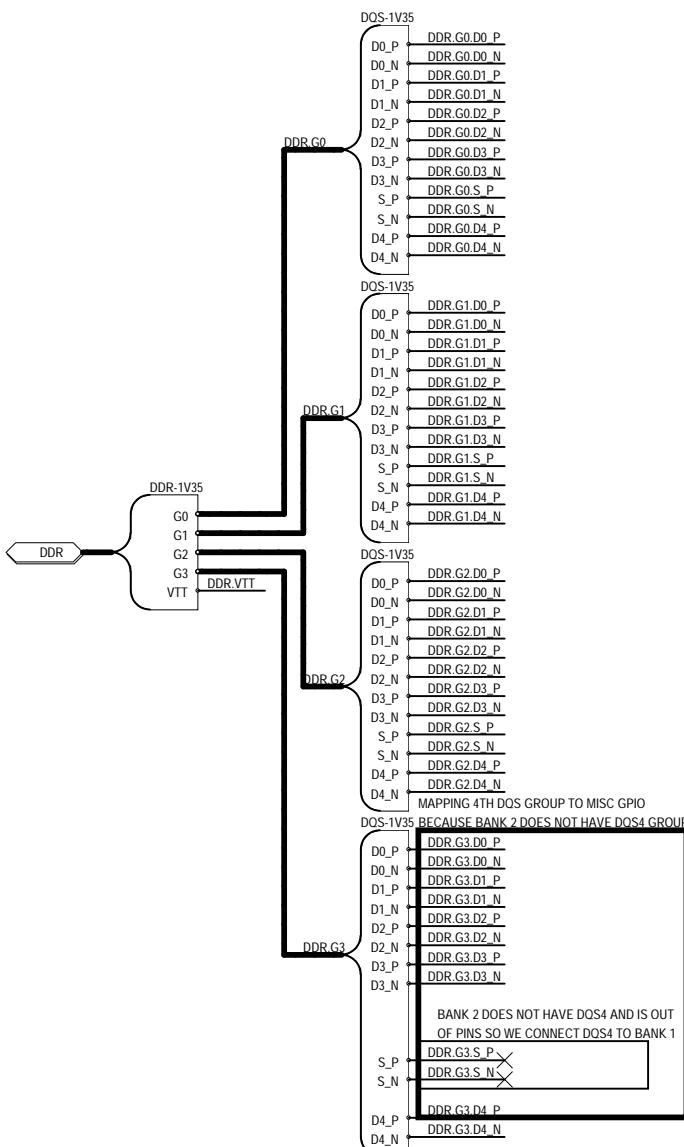


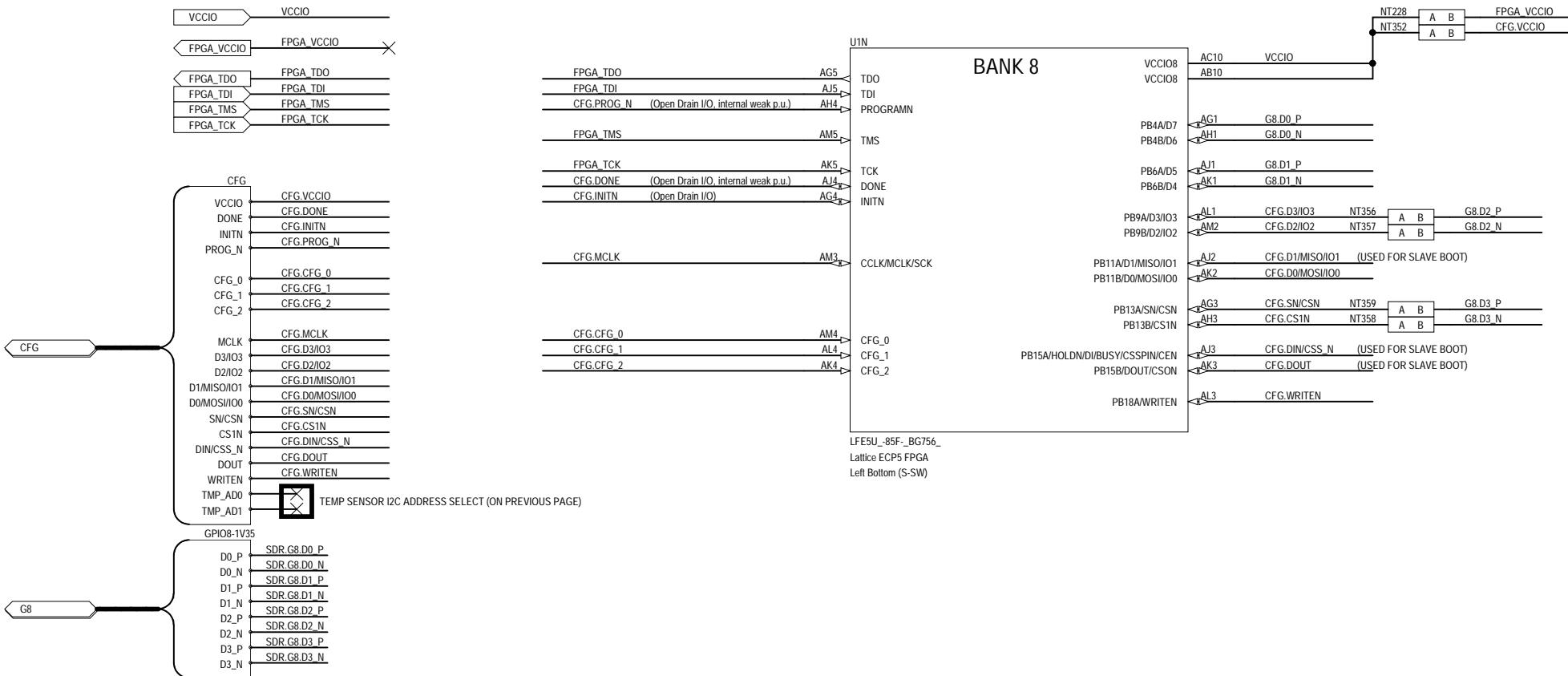












A

B

C

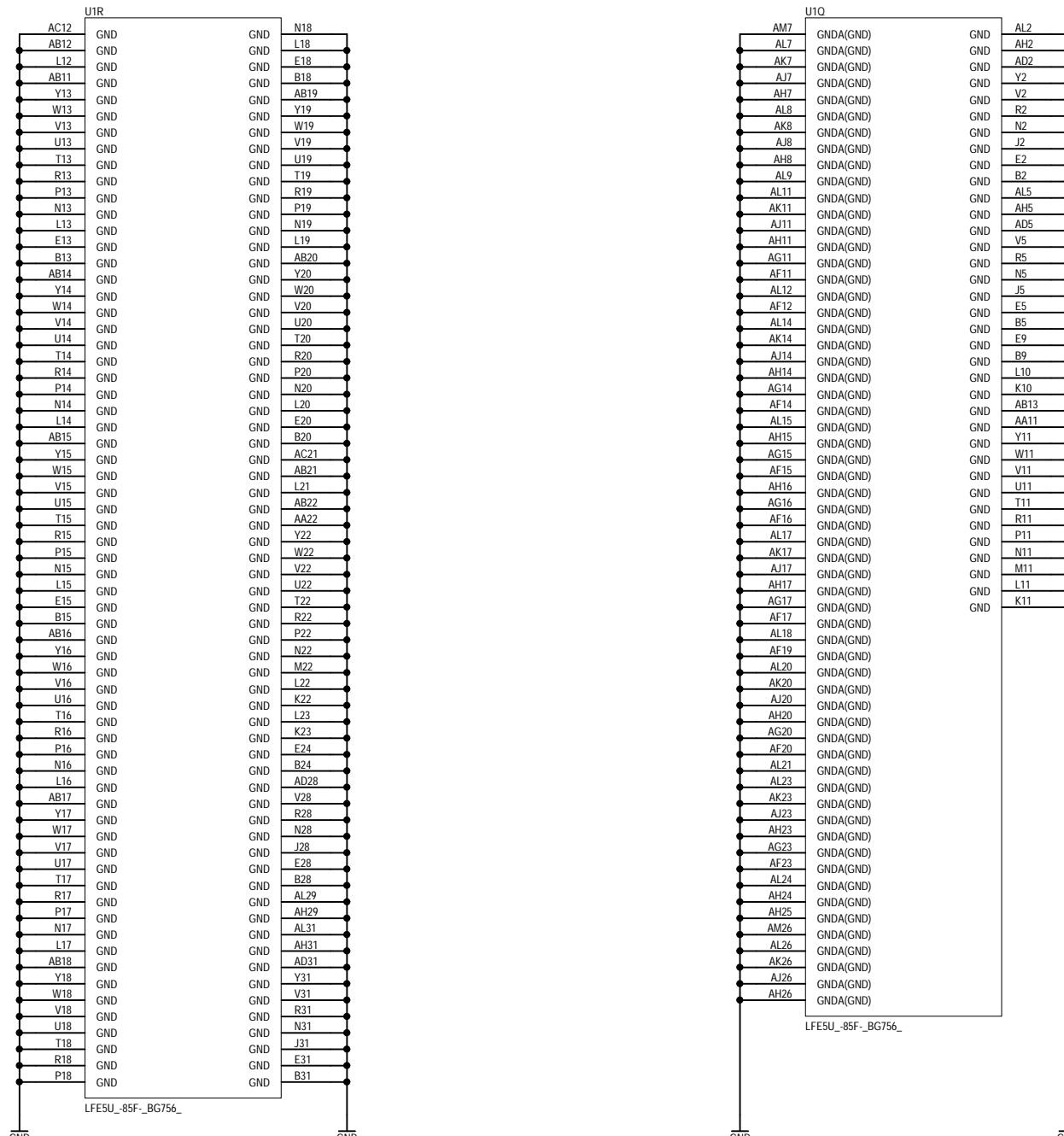
D

A

B

C

D



Copper Suicide - FPGA - Ground		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 13 of 43	Date 10/6/2016

A

A

B

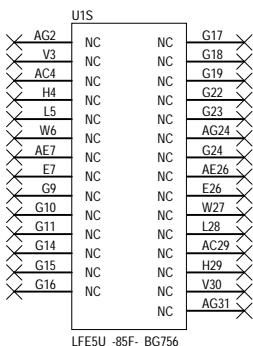
B

C

C

D

D



A

A

B

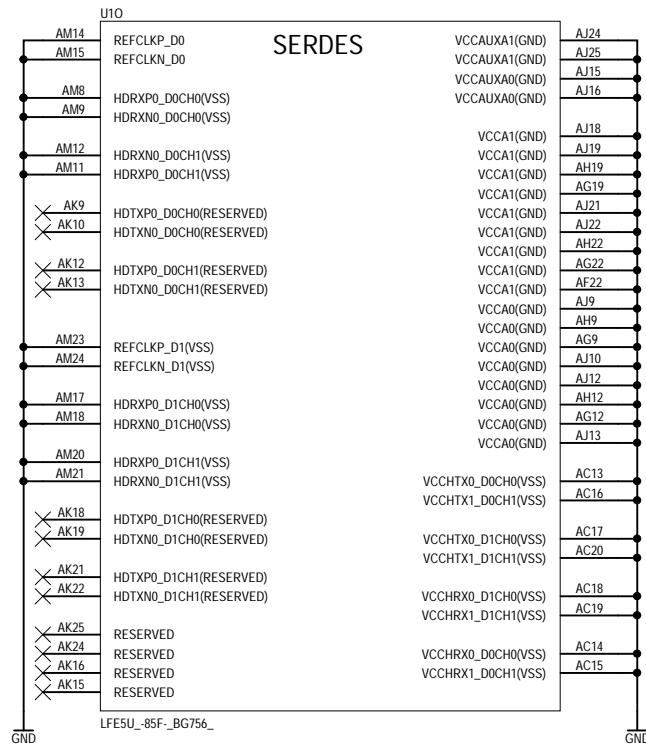
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C

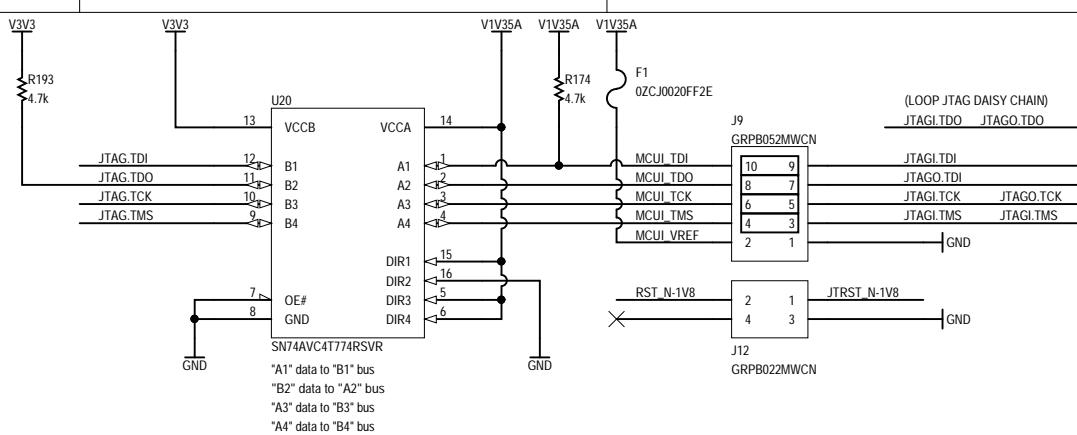
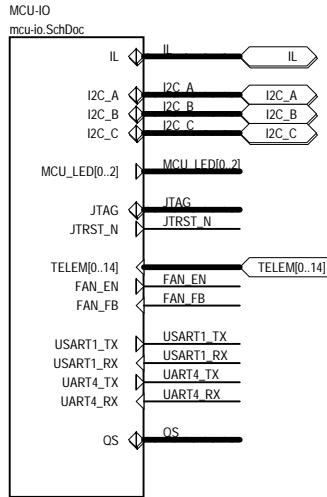
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D

D

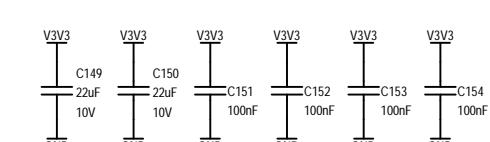
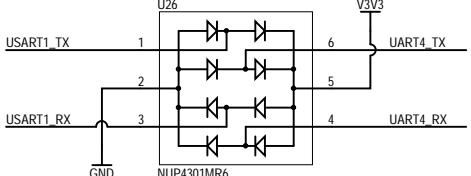
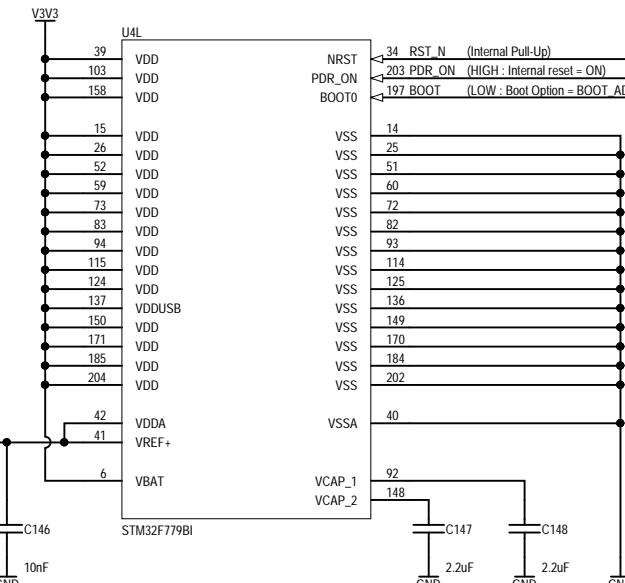
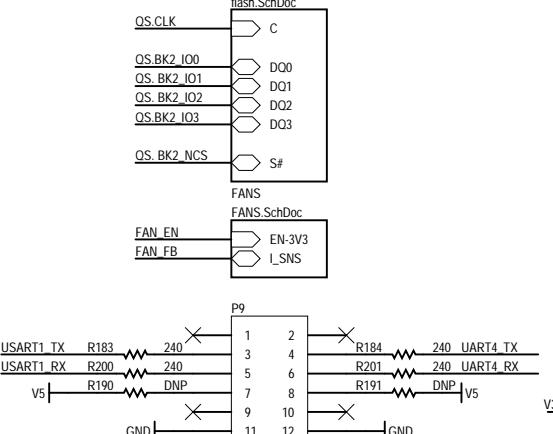
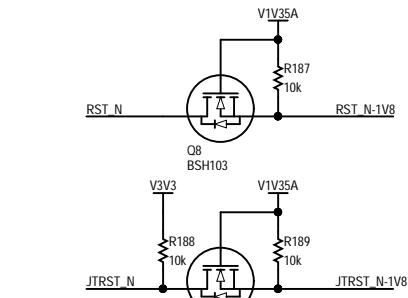


Title		
Copper Suicide - FPGA - SERDES		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 15 of 43	Date 10/6/2016

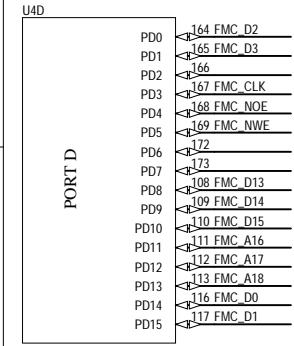
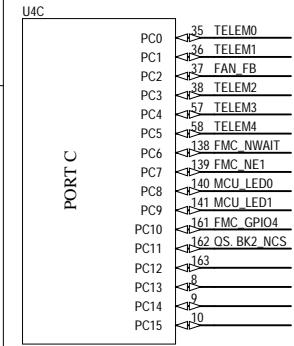
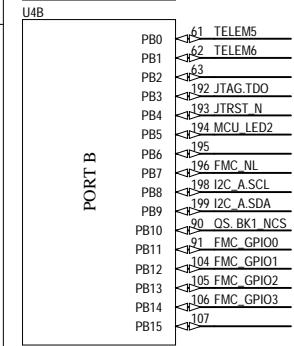
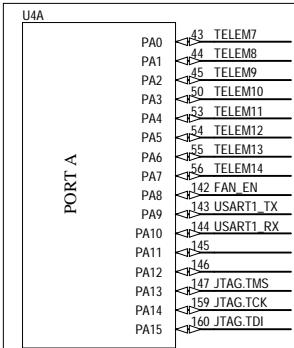


(LOOP JTAG DAISY CHAIN)

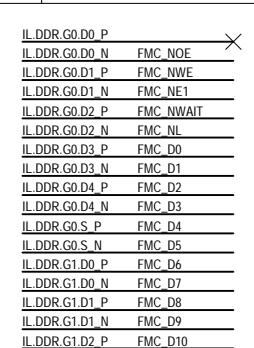
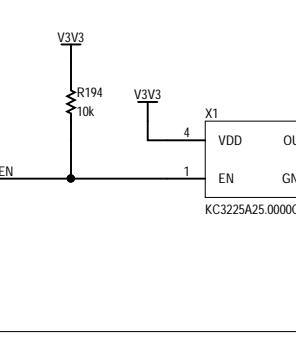
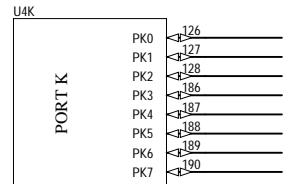
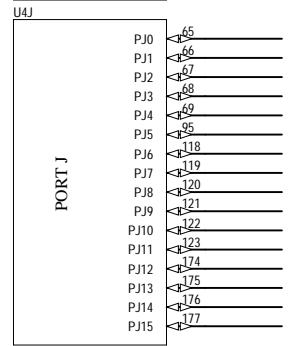
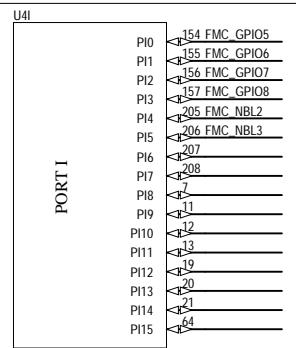
JTAGI.TDI — JTAGO.TDI
JTAGO.TDI — JTAGO.TDO
JTAGO.TCK — JTAGO.TCK
JTAGI.TMS — JTAGI.TMS



1 2 3 4



1 2 3 4



1 2 3 4



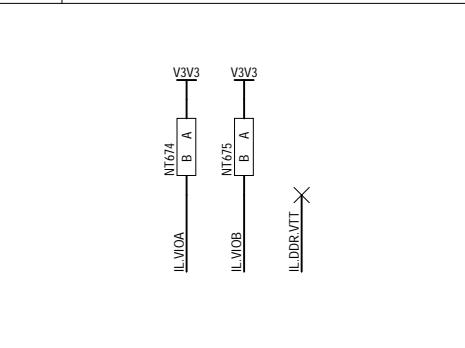
1 2 3 4



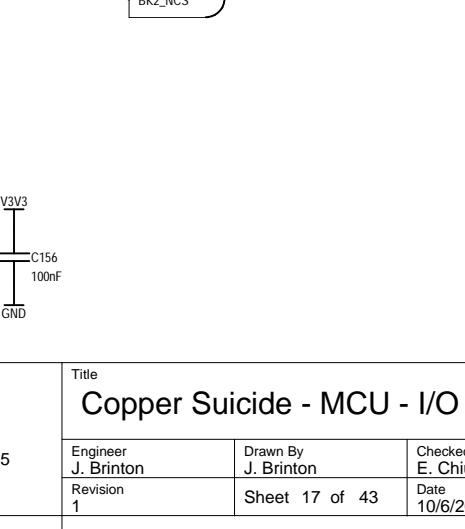
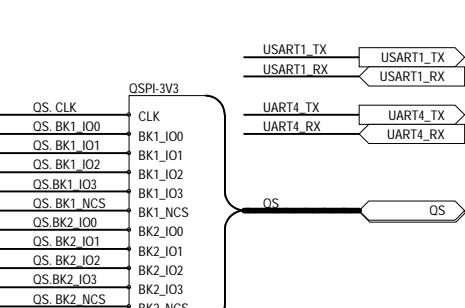
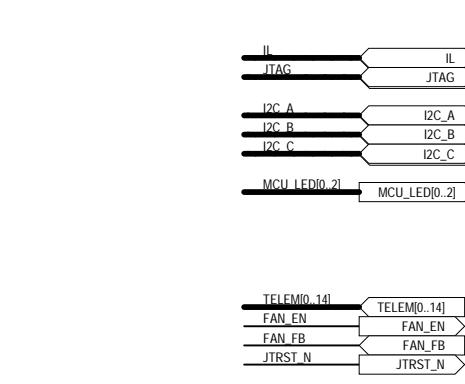
1 2 3 4



1 2 3 4



1 2 3 4



1 2 3 4



Title

Copper Suicide - MCU - I/O

Engineer
J. Brinton

Drawn By
J. Brinton

Checked By
E. Chiu

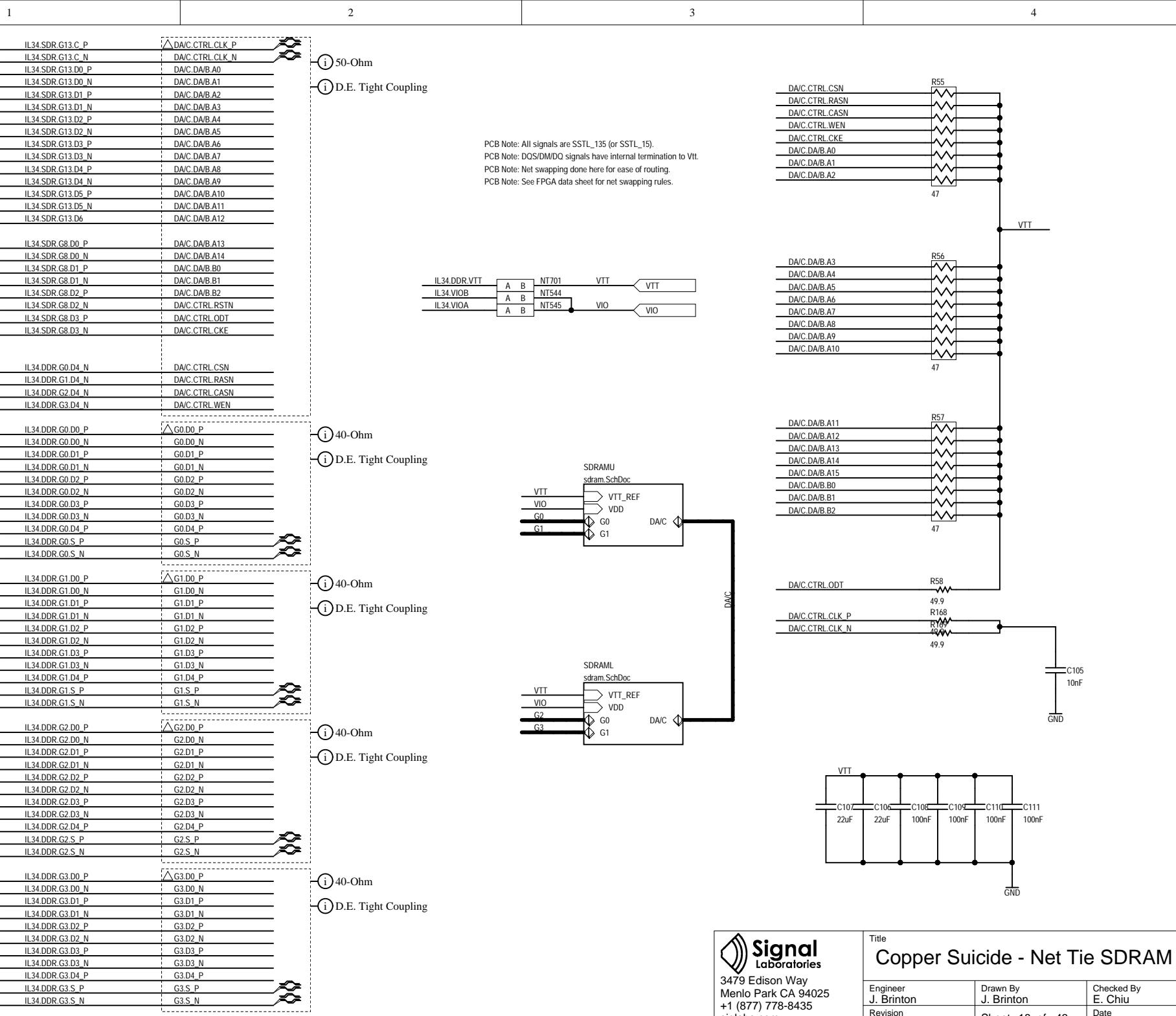
Revision

1

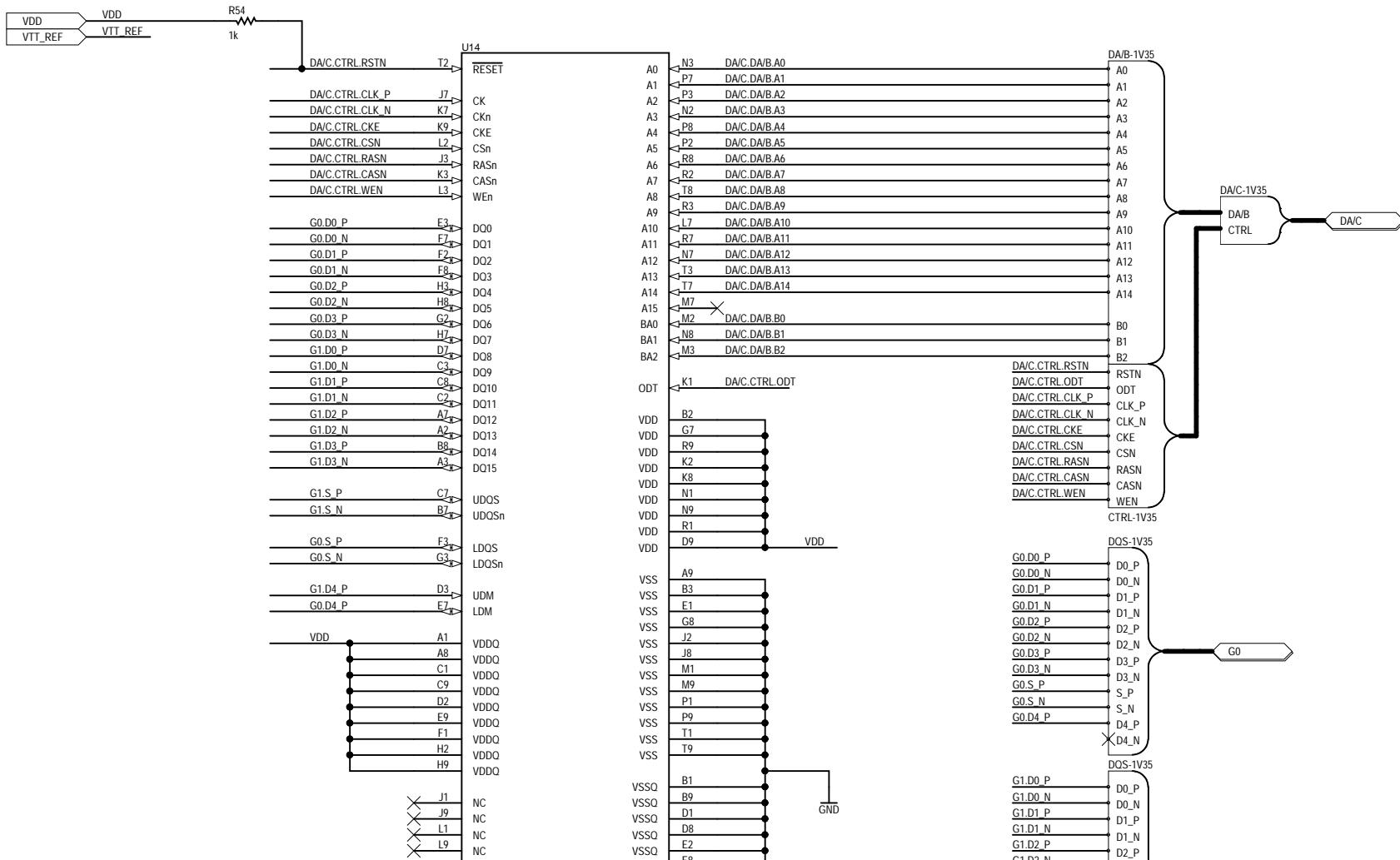
Sheet

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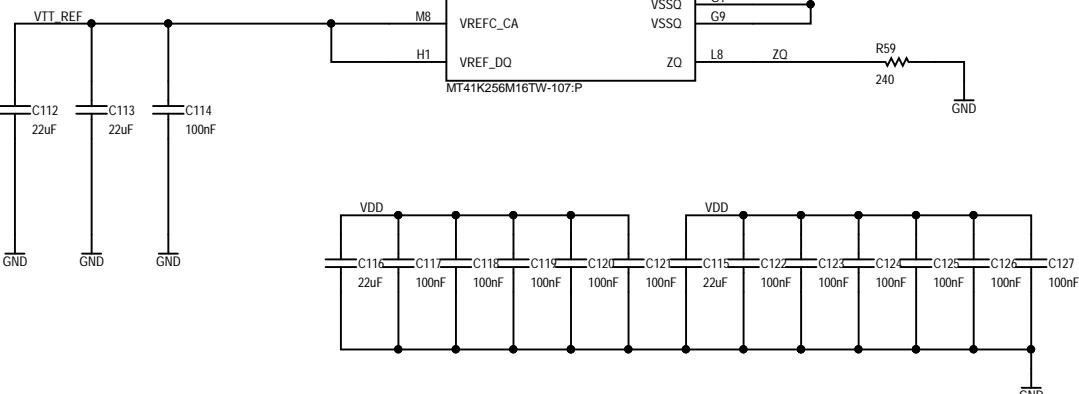
Date
10/6/2016



A



B



C

VCCIO = programmable, NEEDS DEDICATED BANK

IL12.SDR.G13.C_P	NT2	A B	CFG10.MCLK
IL12.SDR.G13.C_N	NT3	A B	CFG10.DONE
IL12.SDR.G13.D_P	NT4	A B	CFG10.INITN
IL12.SDR.G13.D_N	NT5	A B	CFG10.PROG_N
IL12.SDR.G13.D1_P	NT6	A B	CFG10.DIN/CSS_N
IL12.SDR.G13.D1_N	NT7	A B	CFG10.DOUT
IL12.SDR.G13.D2_P	NT8	A B	CFG10.D1/MISO/I01
IL12.SDR.G13.D2_N	NT9	A B	CFG10.D0/MOSI/I00
IL12.SDR.G13.D3_P	NT10	A B	CFG10.WRITEN
IL12.SDR.G13.D3_N	NT11	A B	
IL12.SDR.G13.D4_P	NT12	A B	CFG00.MCLK
IL12.SDR.G13.D4_N	NT13	A B	CFG00.DONE
IL12.SDR.G13.D5_P	NT14	A B	CFG00.INITN
IL12.SDR.G13.D5_N	NT15	A B	CFG00.PROG_N
IL12.SDR.G13.D6	NT16	A B	CFG00.DIN/CSS_N
IL12.SDR.G8.D0_P	NT17	A B	CFG00.DOUT
IL12.SDR.G8.D0_N	NT18	A B	CFG00.D1/MISO/I01
IL12.SDR.G8.D1_P	NT19	A B	CFG00.D0/MOSI/I00
IL12.SDR.G8.D1_N	NT20	A B	CFG00.WRITEN
IL12.SDR.G8.D2_P	NT21	A B	
IL12.SDR.G8.D2_N	NT22	A B	
IL12.SDR.G8.D3_P	NT23	A B	
IL12.SDR.G8.D3_N	NT24	A B	
IL12.DDR.G3.S_P	NT71	A B	
IL12.DDR.G3.S_N	NT212	A B	
IL12.VIOB	NT232	A B	CFG00.VCCIO

VCCIO = programmable, NEEDS DEDICATED BANK

IL07.SDR.G13.C_P	NT355	A B	CFG20.MCLK
IL07.SDR.G13.C_N	NT360	A B	CFG20.DONE
IL07.SDR.G13.D1_P	NT361	A B	CFG20.INITN
IL07.SDR.G13.D1_N	NT362	A B	CFG20.PROG_N
IL07.SDR.G13.D2_P	NT363	A B	CFG20.DIN/CSS_N
IL07.SDR.G13.D2_N	NT364	A B	CFG20.DOUT
IL07.SDR.G13.D3_P	NT365	A B	CFG20.D1/MISO/I01
IL07.SDR.G13.D3_N	NT366	A B	CFG20.D0/MOSI/I00
IL07.SDR.G13.D4_P	NT367	A B	CFG20.WRITEN
IL07.SDR.G13.D4_N	NT368	A B	
IL07.SDR.G13.D5_P	NT369	A B	CFG30.MCLK
IL07.SDR.G13.D5_N	NT370	A B	CFG30.DONE
IL07.SDR.G13.D6	NT371	A B	CFG30.INITN
IL07.SDR.G8.D0_P	NT372	A B	CFG30.PROG_N
IL07.SDR.G8.D0_N	NT373	A B	CFG30.DIN/CSS_N
IL07.SDR.G8.D1_P	NT374	A B	CFG30.DOUT
IL07.SDR.G8.D1_N	NT375	A B	CFG30.D1/MISO/I01
IL07.SDR.G8.D2_P	NT376	A B	CFG30.D0/MOSI/I00
IL07.SDR.G8.D2_N	NT377	A B	CFG30.WRITEN
IL07.SDR.G8.D3_P	NT378	A B	
IL07.SDR.G8.D3_N	NT379	A B	
IL07.DDR.G3.S_P	NT426	A B	
IL07.DDR.G3.S_N	NT213	A B	
IL07.VIOB	NT233	A B	CFG20.VCCIO

IL34.SDR.G13.C_P	NT218	A B	GPMC0.S0_P
IL34.SDR.G13.C_N	NT219	A B	GPMC0.S0_N
IL34.SDR.G13.D0_P	NT220	A B	GPMC0.S1_P
IL34.SDR.G13.D0_N	NT221	A B	GPMC0.S1_N
IL34.SDR.G13.D1_P	NT222	A B	GPMC0.S2_P
IL34.SDR.G13.D1_N	NT223	A B	GPMC0.S2_N
IL34.SDR.G13.D2_P	NT224	A B	GPMC0.S3_P
IL34.SDR.G13.D2_N	NT225	A B	GPMC0.S3_N
IL34.SDR.G13.D3_P	NT226	A B	GPMC0.S4_P
IL34.SDR.G13.D3_N	NT227	A B	GPMC0.S4_N
IL34.SDR.G13.D4_P	NT229	A B	GPMC0.S5_P
IL34.SDR.G13.D4_N	NT230	A B	GPMC0.S5_N
IL34.SDR.G13.D5_P	NT231	A B	GPMC0.S6_P
IL34.SDR.G13.D5_N	NT236	A B	GPMC0.S6_N
IL34.SDR.G13.D6	NT237	A B	CFG22.D0/MOSI/I00
IL34.SDR.G8.D0_P	NT242	A B	GPMC0.S7_P
IL34.SDR.G8.D0_N	NT243	A B	GPMC0.S7_N
IL34.SDR.G8.D1_P	NT248	A B	GPMC0.S8_P
IL34.SDR.G8.D1_N	NT249	A B	GPMC0.S8_N
IL34.SDR.G8.D2_P	NT254	A B	GPMC0.S9_P
IL34.SDR.G8.D2_N	NT255	A B	GPMC0.S9_N
IL34.SDR.G8.D3_P	NT260	A B	GPMC0.S10_P
IL34.SDR.G8.D3_N	NT262	A B	GPMC0.S10_N
IL34.DDR.G3.S_P	NT541	A B	GPMC0.S11_P
IL34.DDR.G3.S_N	NT542	A B	GPMC0.S11_N
IL34.VIOB	NT264	A B	V1V35A

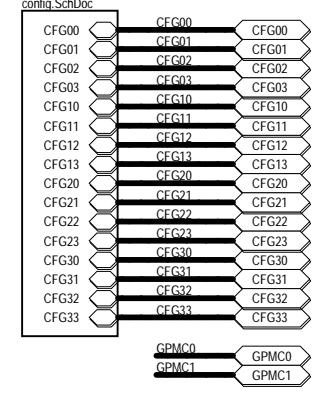
IL34.DDR.G0.D0_P	NT261	A B	GPMC1.S0_P
IL34.DDR.G0.D0_N	NT263	A B	GPMC1.S0_N
IL34.DDR.G0.D1_P	NT265	A B	GPMC1.S1_P
IL34.DDR.G0.D1_N	NT266	A B	GPMC1.S1_N
IL34.DDR.G0.D2_P	NT267	A B	GPMC1.S2_P
IL34.DDR.G0.D2_N	NT268	A B	GPMC1.S2_N
IL34.DDR.G0.D3_P	NT269	A B	GPMC1.S3_P
IL34.DDR.G0.D3_N	NT270	A B	GPMC1.S3_N
IL34.DDR.G0.D4_P	NT271	A B	GPMC1.S4_P
IL34.DDR.G0.D4_N	NT272	A B	GPMC1.S4_N
IL34.DDR.G0.S_P	NT273	A B	GPMC1.S5_P
IL34.DDR.G0.S_N	NT274	A B	GPMC1.S5_N
IL34.DDR.G1.D0_P	NT275	A B	GPMC1.S6_P
IL34.DDR.G1.D0_N	NT276	A B	GPMC1.S6_N
IL34.DDR.G1.D1_P	NT277	A B	GPMC1.S7_P
IL34.DDR.G1.D1_N	NT278	A B	GPMC1.S7_N
IL34.DDR.G1.D2_P	NT279	A B	GPMC1.S8_P
IL34.DDR.G1.D2_N	NT280	A B	GPMC1.S8_N
IL34.DDR.G1.D3_P	NT281	A B	GPMC1.S9_P
IL34.DDR.G1.D3_N	NT514	A B	GPMC1.S9_N
IL34.DDR.G1.D4_P	NT515	A B	GPMC1.S10_P
IL34.DDR.G1.D4_N	NT516	A B	GPMC1.S10_N
IL34.DDR.G1.L_S_P	NT517	A B	GPMC1.S11_P
IL34.DDR.G1.S_N	NT518	A B	GPMC1.S11_N
IL34.DDR.G2.D0_P	NT519	A B	GPMC1.S12_P
IL34.DDR.G2.D0_N	NT520	A B	GPMC1.S12_N
IL34.DDR.G2.D1_P	NT521	A B	GPMC1.S13_P
IL34.DDR.G2.D1_N	NT522	A B	GPMC1.S13_N
IL34.DDR.G2.D2_P	NT523	A B	GPMC1.S14_P
IL34.DDR.G2.D2_N	NT524	A B	GPMC1.S14_N
IL34.DDR.G2.D3_P	NT525	A B	CFG22.D0/MOSI/I00
IL34.DDR.G2.D3_N	NT526	A B	CFG32.WRITEN
IL34.DDR.G2.D4_P	NT527	A B	CFG03.D0/MOSI/I00
IL34.DDR.G2.D4_N	NT528	A B	CFG03.WRITEN
IL34.DDR.G2.S_P	NT529	A B	CFG13.D0MOSI/I00
IL34.DDR.G2.S_N	NT530	A B	CFG13.WRITEN
IL34.DDR.G3.D0_P	NT531	A B	CFG23.D0/MOSI/I00
IL34.DDR.G3.D0_N	NT532	A B	CFG23.WRITEN
IL34.DDR.G3.D1_P	NT533	A B	CFG33.D0MOSI/I00
IL34.DDR.G3.D1_N	NT534	A B	CFG33.WRITEN
IL34.DDR.G3.D2_P	NT535	A B	GPMC0.S12_P
IL34.DDR.G3.D2_N	NT536	A B	GPMC0.S12_N
IL34.DDR.G3.D3_P	NT537	A B	GPMC0.S13_P
IL34.DDR.G3.D3_N	NT538	A B	GPMC0.S13_N
IL34.DDR.G3.D4_P	NT539	A B	GPMC0.S14_P
IL34.DDR.G3.D4_N	NT540	A B	GPMC0.S14_N
IL34.DDR.VTT	NT622	A B	CFG22.WRITEN

(D1/MISO/I01 IS USED FOR SOFT RESET)
PIN SWAPPING TO REDUCE ROUTING COMPLEXITY



Title	Copper Suicide - Net Tie CFG		
Engineer	J. Brinton	Drawn By	E. Chiu
Revision	1	Sheet	20 of 43

BOOT config SchDoc

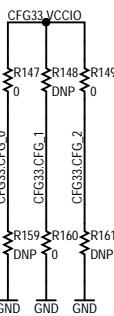
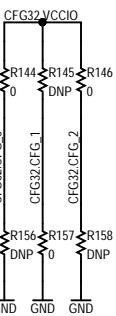
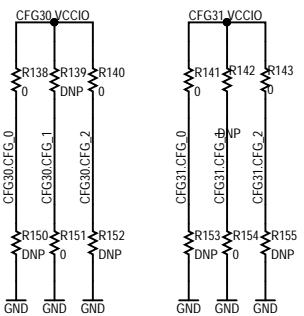
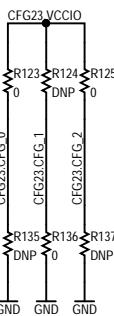
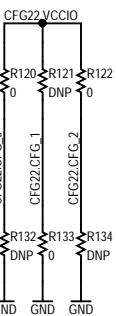
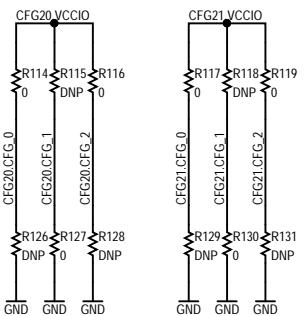
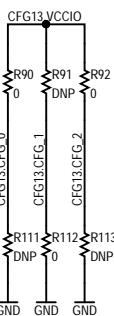
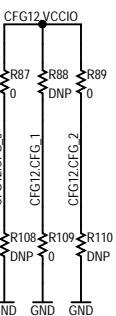
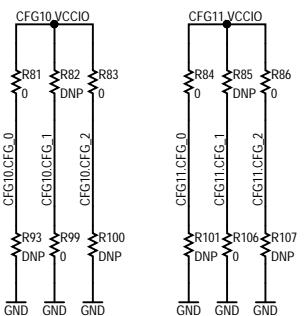
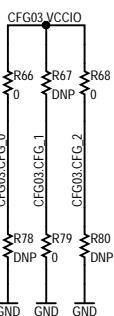
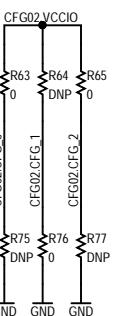
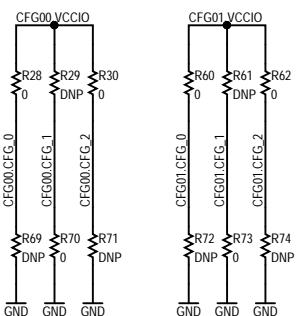


B

C

D

A



CFG00.MCLK	TP42
CFG00.DONE	TP43
CFG00.INITN	TP44
CFG00.PROG_N	TP45
CFG00.DIN/CSS_N	TP46
CFG00.DOUT	TP47
CFG00.D1/MISO/I01	TP48
CFG00.D0/MOSI/I00	TP49
CFG00.SN/CSN	TP50

PCB NOTE: PLACE NEXT TO FPGA #00

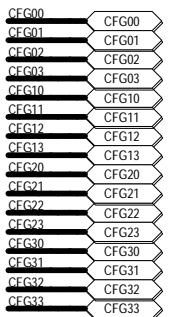
CFG[2:0] = 0b101 (Slave Serial Boot)

TEMP SENSOR I2C ADDRESS SELECT - I2C BUS A

CFG00.TMP_ADO	NT635	A B	GND	0b00 : 7'addr = 0x48
CFG01.TMP_ADO	NT637	A B	X	0b0x : 7'addr = 0x49
CFG02.TMP_ADO	NT638	A B	V3V3	0b01 : 7'addr = 0x4A
CFG03.TMP_ADO	NT640	A B	GND	0b10 : 7'addr = 0x4B
CFG10.TMP_ADO	NT642	A B	X	0b1x : 7'addr = 0x4C
CFG11.TMP_ADO	NT643	A B	V3V3	0b11 : 7'addr = 0x4D
CFG12.TMP_ADO	NT645	A B	GND	0bx0 : 7'addr = 0x4E
CFG13.TMP_ADO	NT646	A B	X	0bx1 : 7'addr = 0x4F

TEMP SENSOR I2C ADDRESS SELECT - I2C BUS B

CFG20.TMP_ADO	NT647	A B	GND	0b00 : 7'addr = 0x48
CFG21.TMP_ADO	NT648	A B	GND	0b0x : 7'addr = 0x49
CFG21.TMP_ADO	NT649	A B	X	0b1x : 7'addr = 0x4A
CFG22.TMP_ADO	NT650	A B	V3V3	0b01 : 7'addr = 0x4B
CFG23.TMP_ADO	NT652	A B	GND	0b10 : 7'addr = 0x4C
CFG23.TMP_ADO	NT653	A B	V3V3	0b11 : 7'addr = 0x4D
CFG30.TMP_ADO	NT654	A B	X	0b1x : 7'addr = 0x4E
CFG31.TMP_ADO	NT655	A B	V3V3	0b0x0 : 7'addr = 0x4F
CFG32.TMP_ADO	NT657	A B	GND	0bx1 : 7'addr = 0x50
CFG33.TMP_ADO	NT658	A B	X	0bx2 : 7'addr = 0x51



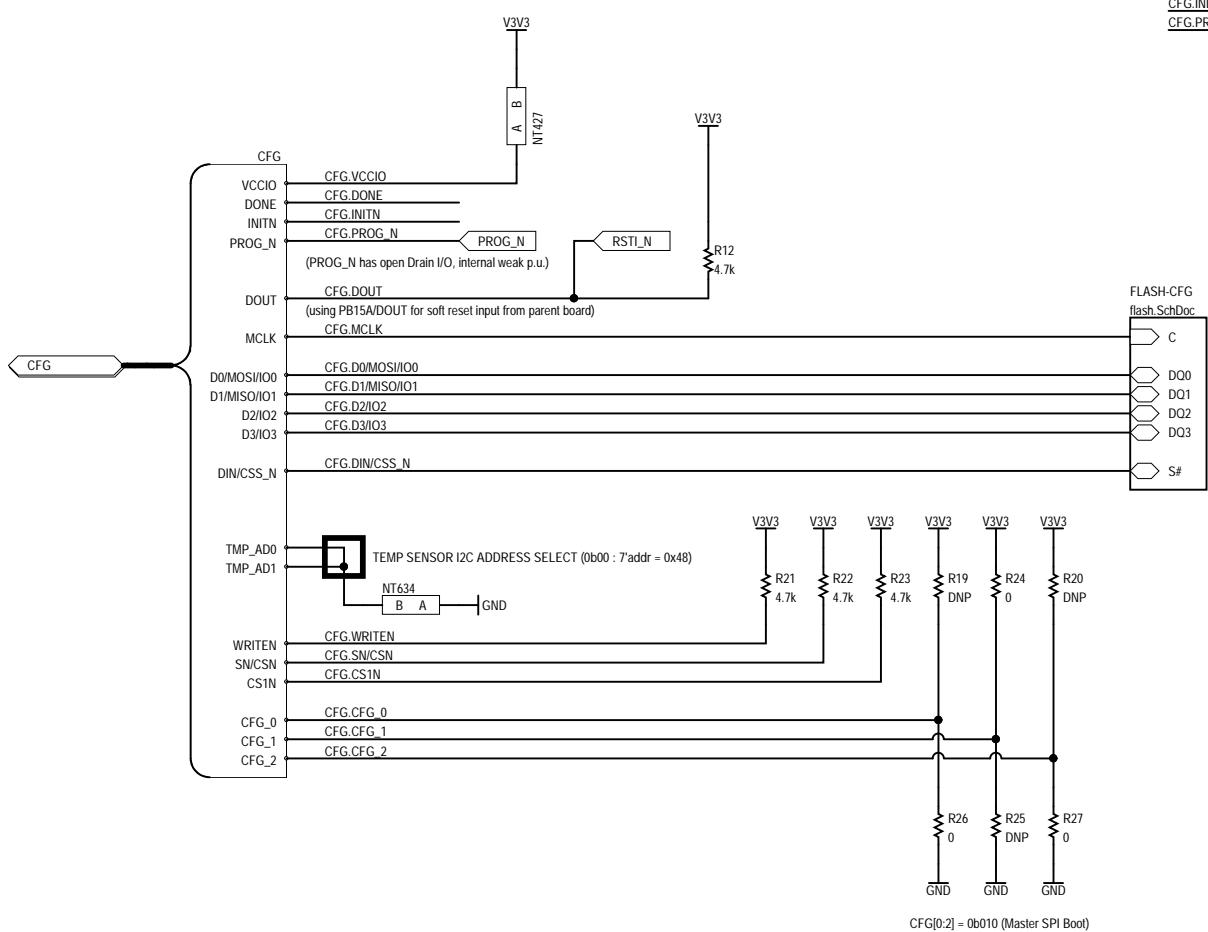
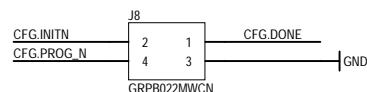
A

B

C

D

PCB NOTE: Place head next to JTAG per programming header



A

B

C

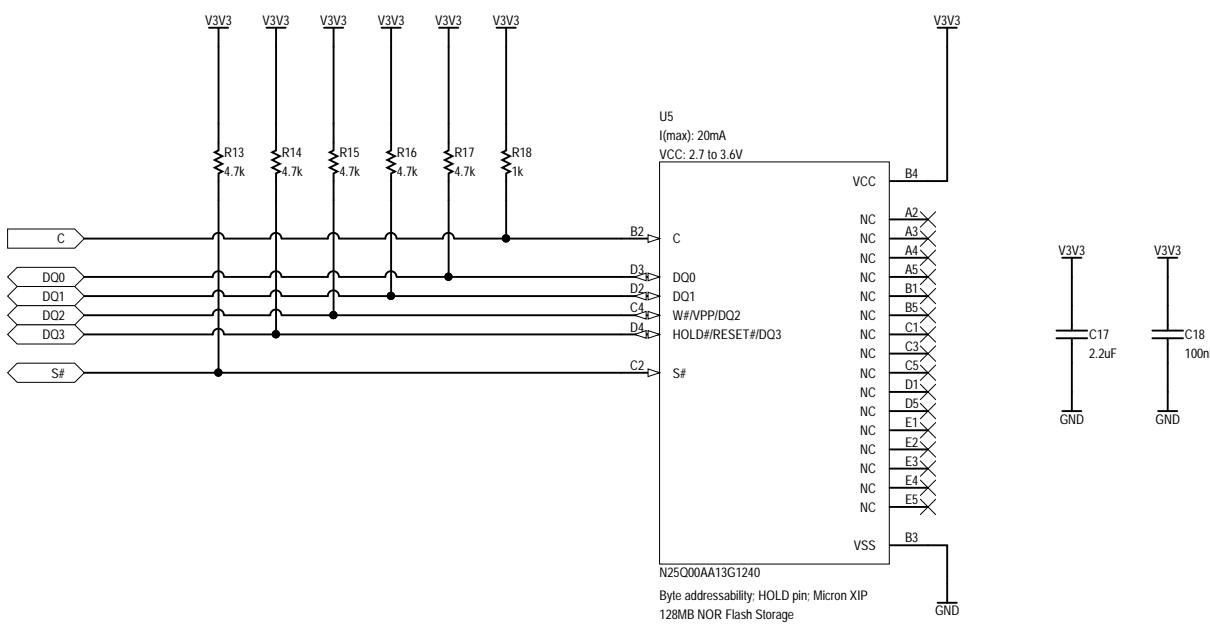
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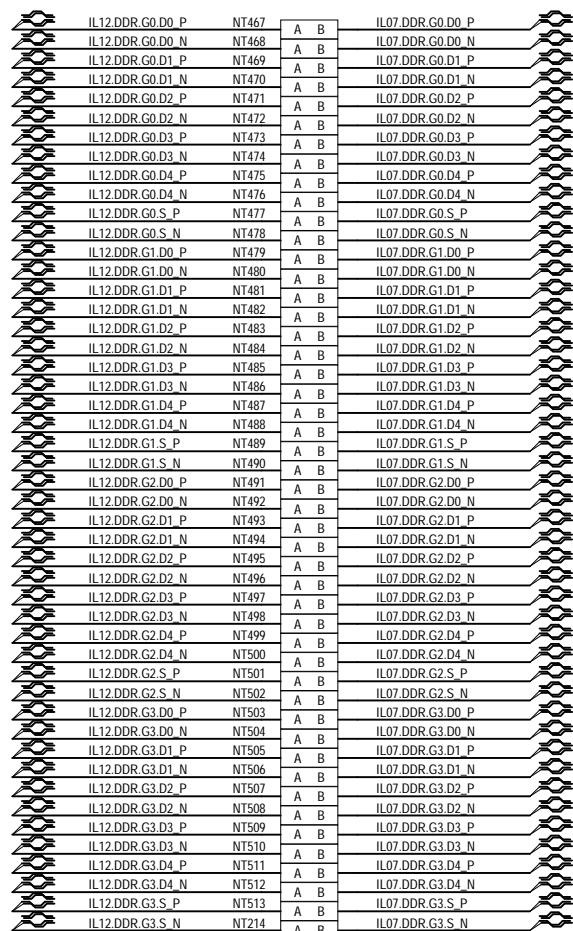
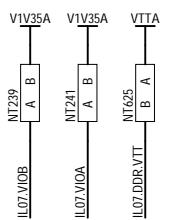
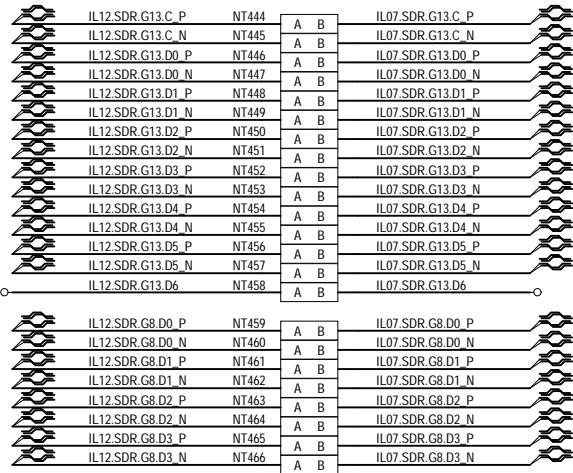
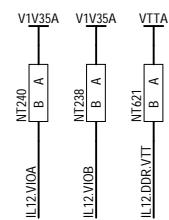
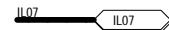
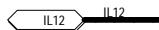
A

B

C

D





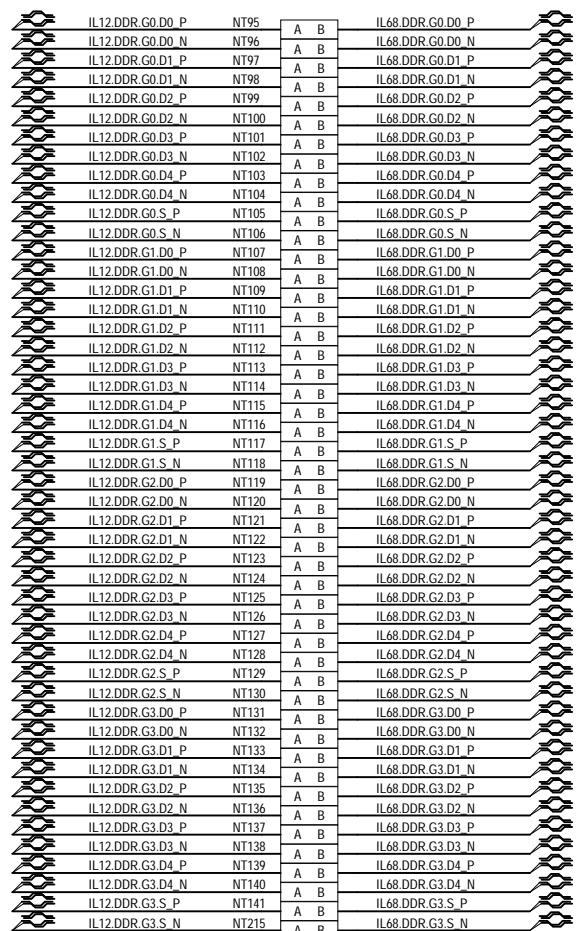
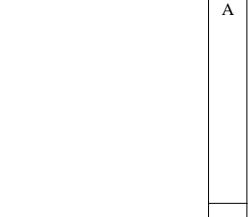
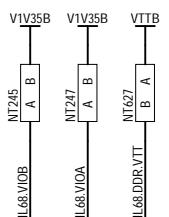
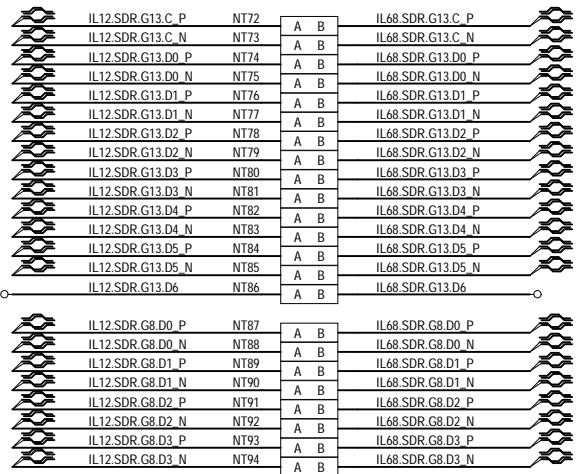
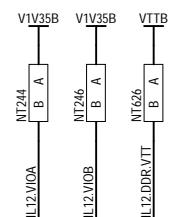
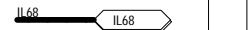
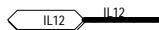
PIN SWAPPING TO REDUCE ROUTING COMPLEXITY



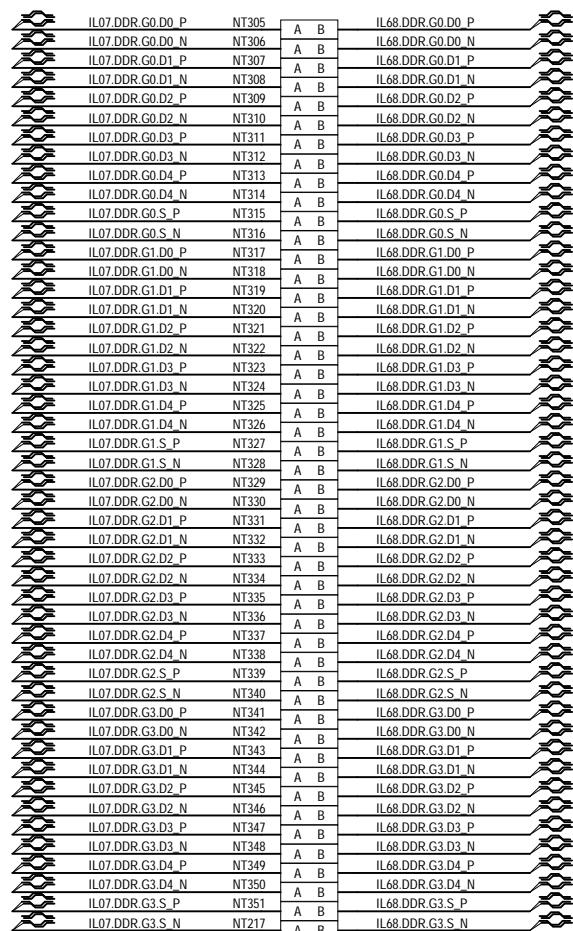
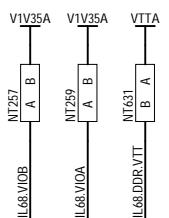
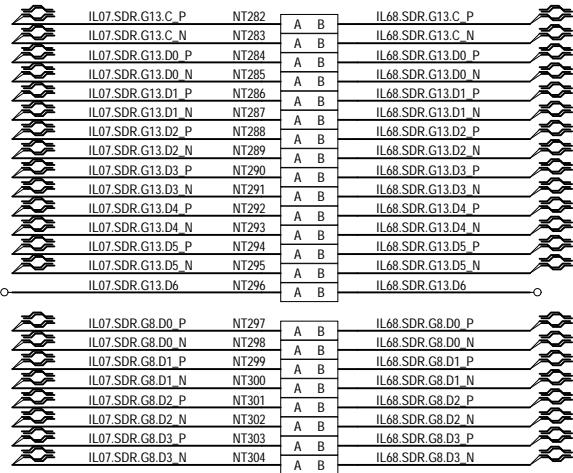
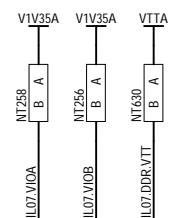
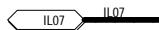
3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siglabs.com

Title
Copper Suicide - Net Tie 12:07

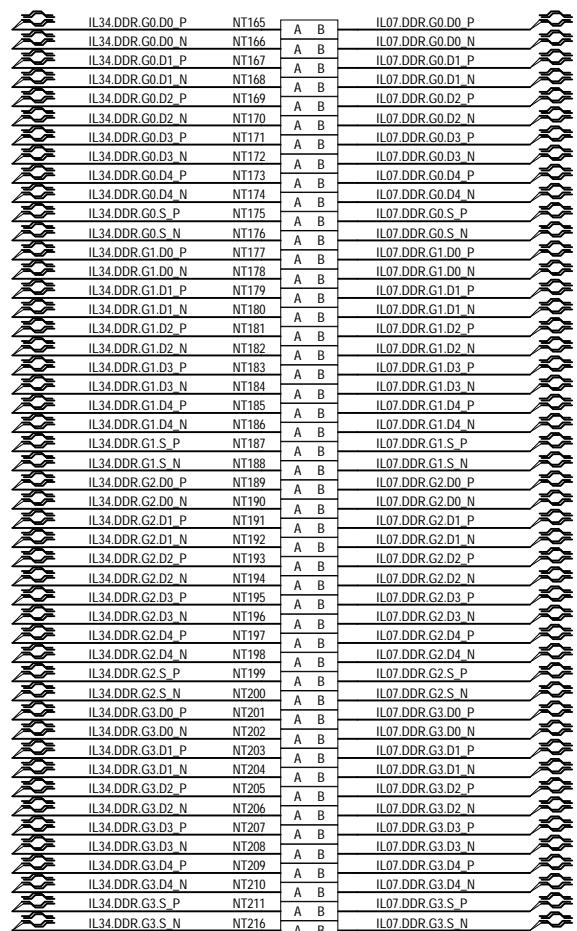
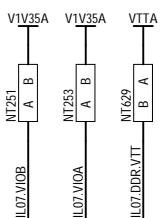
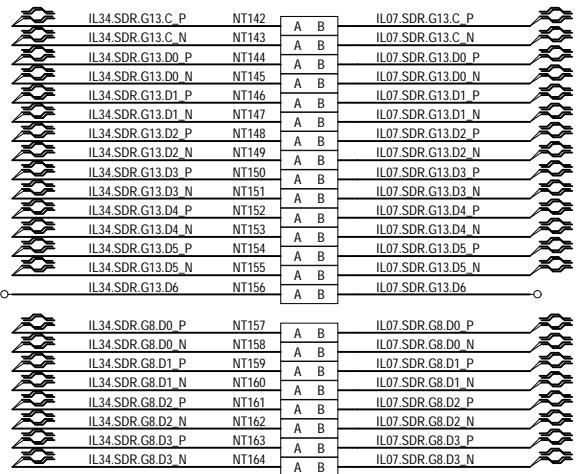
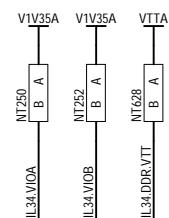
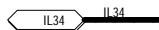
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 24 of 43	Date 10/6/2016



PIN SWAPPING TO REDUCE ROUTING COMPLEXITY

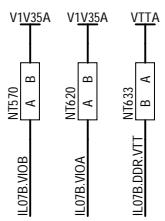
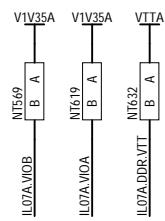
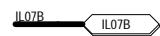
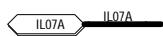


PIN SWAPPING TO REDUCE ROUTING COMPLEXITY



PIN SWAPPING TO REDUCE ROUTING COMPLEXITY

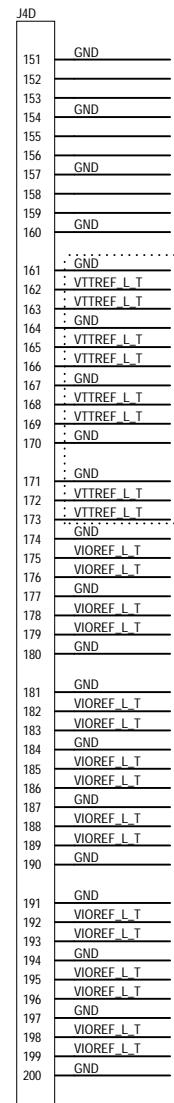
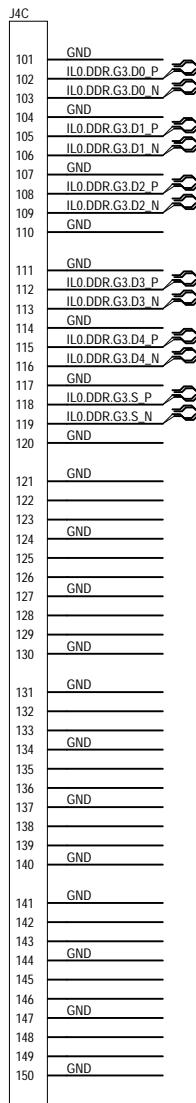
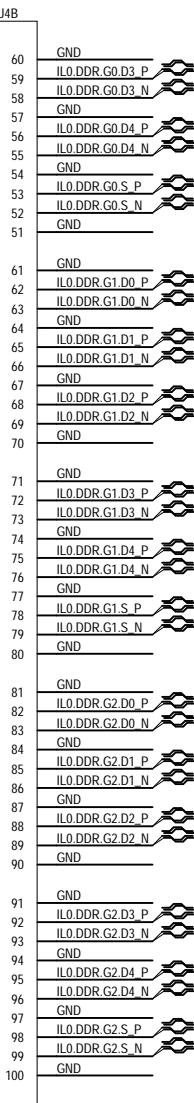
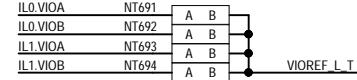
Title		
Copper Suicide - Net Tie 34:07		
Revision 1	Sheet 27 of 43	Date 10/6/2016



B

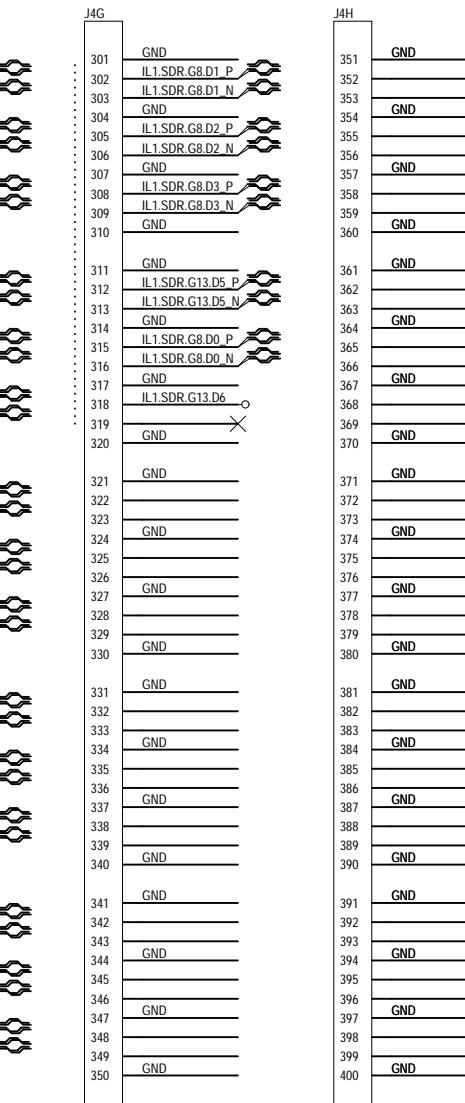
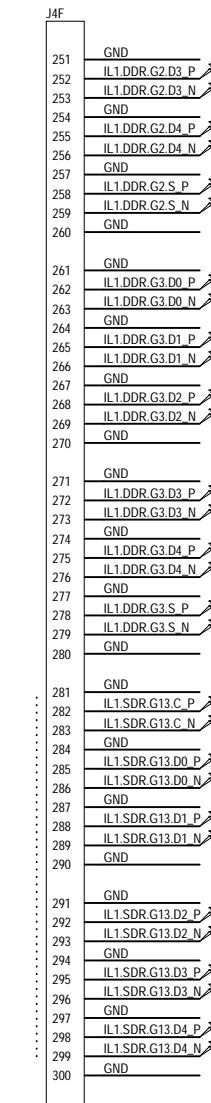
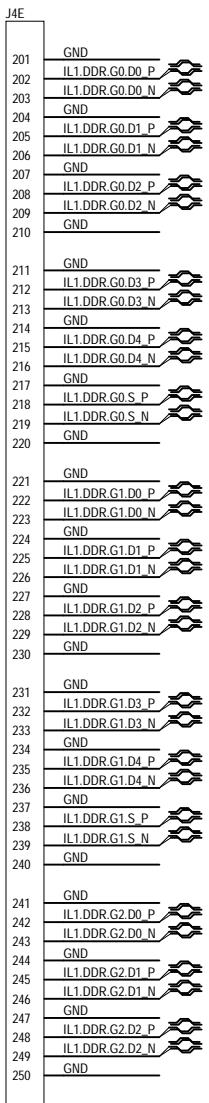
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IL07A.SDR.G13.D0_N	NT549	A B	IL07B.SDR.G13.D0_N	
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IL07A.SDR.G13.D1_N	NT551	A B	IL07B.SDR.G13.D1_N	
IL07A.SDR.G13.D2_P	NT552	A B	IL07B.SDR.G13.D2_P	
IL07A.SDR.G13.D2_N	NT553	A B	IL07B.SDR.G13.D2_N	
IL07A.SDR.G13.D3_P	NT554	A B	IL07B.SDR.G13.D3_P	
IL07A.SDR.G13.D3_N	NT555	A B	IL07B.SDR.G13.D3_N	
IL07A.SDR.G13.D4_P	NT556	A B	IL07B.SDR.G13.D4_P	
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IL07A.SDR.G13.D5_P	NT558	A B	IL07B.SDR.G13.D5_P	
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IL07A.SDR.G8.D1_P	NT563	A B	IL07B.SDR.G8.D1_P	
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IL07A_DDR.G0.D2_N	NT576	A B	IL07B_DDR.G0.D2_N	
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IL07A_DDR.G2.D3_N	NT602	A B	IL07B_DDR.G2.D3_N	
IL07A_DDR.G2.D4_P	NT603	A B	IL07B_DDR.G2.D4_P	
IL07A_DDR.G2.D4_N	NT604	A B	IL07B_DDR.G2.D4_N	
IL07A_DDR.G2.S_P	NT605	A B	IL07B_DDR.G2.S_P	
IL07A_DDR.G2.S_N	NT606	A B	IL07B_DDR.G2.S_N	
IL07A_DDR.G3.D0_P	NT607	A B	IL07B_DDR.G3.D0_P	
IL07A_DDR.G3.D0_N	NT608	A B	IL07B_DDR.G3.D0_N	
IL07A_DDR.G3.D1_P	NT609	A B	IL07B_DDR.G3.D1_P	
IL07A_DDR.G3.D1_N	NT610	A B	IL07B_DDR.G3.D1_N	
IL07A_DDR.G3.D2_P	NT611	A B	IL07B_DDR.G3.D2_P	
IL07A_DDR.G3.D2_N	NT612	A B	IL07B_DDR.G3.D2_N	
IL07A_DDR.G3.D3_P	NT613	A B	IL07B_DDR.G3.D3_P	
IL07A_DDR.G3.D3_N	NT614	A B	IL07B_DDR.G3.D3_N	
IL07A_DDR.G3.D4_P	NT615	A B	IL07B_DDR.G3.D4_P	
IL07A_DDR.G3.D4_N	NT616	A B	IL07B_DDR.G3.D4_N	
IL07A_DDR.G3.S_P	NT617	A B	IL07B_DDR.G3.S_P	
IL07A_DDR.G3.S_N	NT618	A B	IL07B_DDR.G3.S_N	

PIN SWAPPING TO REDUCE ROUTING COMPLEXITY



Referenced Input Reference Voltage

Referenced Input Reference Voltage

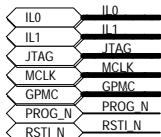


1

2

3

4



V48BB
V48BB

J3A
SEAM-40-11.0-S-10-2-A-K-TR

J3B

1	GND
2	IL0.DDR.G0.D3.P
3	IL0.DDR.G0.D3.N
4	GND
5	IL0.DDR.G0.D4.P
6	IL0.DDR.G0.D4.N
7	GND
8	IL0.DDR.G0.S.P
9	IL0.DDR.G0.S.N
10	GND
11	GND
12	IL0.DDR.G1.D0.P
13	IL0.DDR.G1.D0.N
14	GND
15	IL0.DDR.G1.D1.P
16	IL0.DDR.G1.D1.N
17	GND
18	IL0.DDR.G1.D2.P
19	IL0.DDR.G1.D2.N
20	GND
21	GND
22	IL0.DDR.G1.D3.P
23	IL0.DDR.G1.D3.N
24	GND
25	IL0.DDR.G1.D4.P
26	IL0.DDR.G1.D4.N
27	GND
28	IL0.DDR.G1.S.P
29	IL0.DDR.G1.S.N
30	GND
31	GND
32	IL0.DDR.G2.D0.P
33	IL0.DDR.G2.D0.N
34	GND
35	IL0.DDR.G2.D1.P
36	IL0.DDR.G2.D1.N
37	GND
38	IL0.DDR.G2.D2.P
39	IL0.DDR.G2.D2.N
40	GND
41	GND
42	IL0.DDR.G2.D3.P
43	IL0.DDR.G2.D3.N
44	GND
45	IL0.DDR.G2.D4.P
46	IL0.DDR.G2.D4.N
47	GND
48	IL0.DDR.G2.S.P
49	IL0.DDR.G2.S.N
50	GND

J3C

1	GND
2	IL0.DDR.G3.D0.P
3	IL0.DDR.G3.D0.N
4	GND
5	IL0.DDR.G3.D1.P
6	IL0.DDR.G3.D1.N
7	GND
8	IL0.DDR.G3.D2.P
9	IL0.DDR.G3.D2.N
10	GND
11	GND
12	IL0.DDR.G3.D3.P
13	IL0.DDR.G3.D3.N
14	GND
15	IL0.DDR.G3.D4.P
16	IL0.DDR.G3.D4.N
17	GND
18	IL0.DDR.G3.S.P
19	IL0.DDR.G3.S.N
20	GND
21	GND
22	IL0.DDR.G0.D0.P
23	IL0.DDR.G0.D0.N
24	GND
25	IL0.DDR.G0.D1.P
26	IL0.DDR.G0.D1.N
27	GND
28	IL0.DDR.G1.S.P
29	IL0.DDR.G1.S.N
30	GND
31	GND
32	IL0.DDR.G1.D3.C.P
33	IL0.DDR.G1.D3.C.N
34	GND
35	IL0.SDR.G13.D0.P
36	IL0.SDR.G13.D0.N
37	GND
38	IL0.SDR.G2.D2.P
39	IL0.SDR.G2.D2.N
40	GND
41	GND
42	IL0.SDR.G13.D2.P
43	IL0.SDR.G13.D2.N
44	GND
45	IL0.SDR.G13.D3.P
46	IL0.SDR.G13.D3.N
47	GND
48	IL0.SDR.G13.D4.P
49	IL0.SDR.G13.D4.N
50	GND

J3D

1	GND
2	IL0.SDR.G8.D1.P
3	IL0.SDR.G8.D1.N
4	GND
5	IL0.SDR.G8.D2.P
6	IL0.SDR.G8.D2.N
7	GND
8	IL0.SDR.G8.D3.P
9	IL0.SDR.G8.D3.N
10	GND
11	GND
12	IL0.SDR.G13.D5.P
13	IL0.SDR.G13.D5.N
14	GND
15	IL0.SDR.G8.D0.P
16	IL0.SDR.G8.D0.N
17	GND
18	IL0.SDR.G8.D1.N
19	GND
20	GND
21	GND
22	JTAG.TDI
23	JTAG.TMS
24	GND
25	IL0.SDR.G8.D2.P
26	IL0.SDR.G8.D2.N
27	GND
28	MCLK.C.P
29	MCLK.C.N
30	GND
31	GND
32	PROG_N
33	RSTI_N
34	GND
35	V48BB
36	V48BB
37	VIOREF_R.T
38	VIOREF_R.T
39	VIOREF_R.T
40	GND
41	GND
42	VIOREF_R.T
43	VIOREF_R.T
44	GND
45	VIOREF_R.T
46	VIOREF_R.T
47	GND
48	VIOREF_R.T
49	VIOREF_R.T
50	GND

J3E

1	GND
2	GPMC.S9.P
3	GPMC.S9.N
4	GND
5	GPMC.S10.P
6	GPMC.S10.N
7	GND
8	GPMC.S11.P
9	GPMC.S11.N
10	GND
11	GND
12	VTTREF_R.T
13	VTTREF_R.T
14	GND
15	VTTREF_R.T
16	VTTREF_R.T
17	GND
18	VTTREF_R.T
19	VTTREF_R.T
20	GND
21	GND
22	JTAG.TCK
23	JTAG.TDO
24	GND
25	GPMC.S4.P
26	GPMC.S4.N
27	GND
28	GPMC.S5.P
29	GPMC.S5.N
30	GND
31	GND
32	GND
33	GND
34	GND
35	GND
36	GND
37	GND
38	GND
39	GND
40	GND

J3F

1	GND
2	GPMC.S0.P
3	GPMC.S0.N
4	GND
5	GPMC.S1.P
6	GPMC.S1.N
7	GND
8	GPMC.S2.P
9	GPMC.S2.N
10	GND
11	GND
12	IL0.SDR.G13.D5.P
13	IL0.SDR.G13.D5.N
14	GND
15	V48BB
16	V48BB
17	V48BB
18	V48BB
19	V48BB
20	V48BB
21	GND
22	GND
23	GND
24	GND
25	GND
26	GND
27	GND
28	GND
29	GND
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31	GND
32	GND
33	GND
34	GND
35	GND
36	GND
37	GND
38	GND
39	GND
40	GND

J3G

1	GND
2	GND
3	GND
4	GND
5	GND
6	GND
7	GND
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10	GND
11	GND
12	GND
13	GND
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31	GND
32	GND
33	GND
34	GND
35	GND
36	GND
37	GND
38	GND
39	GND
40	GND

J3H

1	GND
2	IL1.DDR.G1.D3.P
3	IL1.DDR.G1.D3.N
4	GND
5	IL1.DDR.G1.D4.P
6	IL1.DDR.G1.D4.N
7	GND
8	IL1.DDR.G1.S.P
9	IL1.DDR.G1.S.N
10	GND
11	GND
12	IL1.DDR.G2.D0.P
13	IL1.DDR.G2.D0.N
14	GND
15	IL1.DDR.G2.D1.P
16	IL1.DDR.G2.D1.N
17	GND
18	IL1.DDR.G2.D2.P
19	IL1.DDR.G2.D2.N
20	GND
21	GND
22	IL1.DDR.G2.D3.P
23	IL1.DDR.G2.D3.N
24	GND
25	IL1.DDR.G2.D4.P
26	IL1.DDR.G2.D4.N
27	GND
28	IL1.DDR.G2.S.P
29	IL1.DDR.G2.S.N
30	GND
31	GND
32	IL1.DDR.G3.D0.P
33	IL1.DDR.G3.D0.N
34	GND
35	IL1.DDR.G3.D1.P
36	IL1.DDR.G3.D1.N
37	GND
38	IL1.DDR.G3.D2.P
39	IL1.DDR.G3.D2.N
40	GND

IL1.DDR.VTT NT695
IL0.DDR.VTT NT696 A B VTTREF_R.T

IL0.VIOA NT697
IL0.VIOB NT698 A B VIREF_R.T

IL1.VIOA NT699 A B VIREF_R.T

IL1.VIOB NT700 A B VIREF_R.T

GND
GND

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3479 Edison Way
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siglabs.com

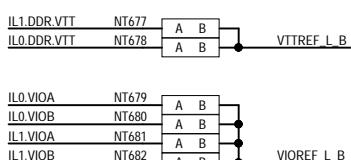
Title

Copper Suicide - Right Top

Engineer
J. BrintonDrawn By
J. BrintonChecked By
E. ChiuRevision
1

Sheet 30 of 43

Date
10/6/2016



GND

GND



Title

Copper Suicide - Left Bottom

Engineer

J. Brinton

Drawn By

J. Brinton

Checked By

E. Chiu

Revision

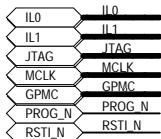
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Sheet

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Date

10/6/2016



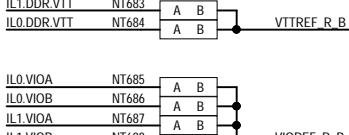
V48BB
V48BB

A
J1A
SEAF-40-06-S-10-2-A-K-TR

1	GND	60	GND	101	GND	151	GND	201	GND	251	GND	301	GND	351	GND
2	IL0.DDR.G0.D3.P	59	IL0.DDR.G3.D0.P	102	IL0.SDR.G8.D1.P	152	GPMC.S12.P	202	GPMC.S9.P	252	GPMC.S0.P	302	IL0.SDR.G13.D5.P	352	IL1.DDR.G1.D3.P
3	IL0.DDR.G0.D3.N	58	IL0.DDR.G3.D0.N	103	IL0.SDR.G8.D1.N	153	GPMC.S12.N	203	GPMC.S9.N	253	GPMC.S0.N	303	IL0.SDR.G13.D5.N	353	IL1.DDR.G1.D3.N
4	GND	57	IL0.DDR.G3.D1.P	104	IL0.SDR.G8.D2.P	154	GND	204	GPMC.S10.P	254	GPMC.S1.P	304	IL0.SDR.G13.D6	354	GND
5	IL0.DDR.G0.D4.P	56	IL0.DDR.G3.D1.N	105	IL0.SDR.G8.D2.N	155	GND	205	GPMC.S10.N	255	GPMC.S1.N	305	GND	355	IL1.DDR.G1.D4.P
6	IL0.DDR.G0.D4.N	55	GND	106	IL0.SDR.G8.D3.P	156	GND	206	GPMC.S11.P	256	GPMC.S2.P	306	GND	356	IL1.DDR.G1.D4.N
7	GND	54	IL0.DDR.G3.D2.P	107	IL0.SDR.G8.D3.N	157	GND	207	GPMC.S11.N	257	GPMC.S2.N	307	GND	357	GND
8	IL0.DDR.G0.S.P	53	IL0.DDR.G3.D2.N	108	IL0.SDR.G8.D3.N	158	GPMC.S14.P	208	GPMC.S11.P	258	GPMC.S2.N	308	IL0.SDR.G8.D0.N	358	IL1.DDR.G1.S.P
9	IL0.DDR.G0.S.N	52	GND	109	GND	159	GPMC.S14.N	209	GPMC.S11.N	259	GND	309	GND	359	IL1.DDR.G1.S.N
10	GND	51	GND	110	GND	160	GND	210	GND	260	GND	310	GND	360	GND
11	GND	61	GND	111	GND	161	GND	211	GND	261	GND	311	GND	361	GND
12	IL0.DDR.G1.D0.P	62	IL0.DDR.G3.D3.P	112	IL0.SDR.G13.D5.P	162	: VITREF.R.B	212	JTAG.TDI	262	GPMC.S3.P	312	IL0.SDR.G8.D1.P	362	IL1.DDR.G2.D0.P
13	IL0.DDR.G1.D0.N	63	IL0.DDR.G3.D3.N	113	IL0.SDR.G13.D5.N	163	: VITREF.R.B	213	JTAG.TMS	263	GPMC.S3.N	313	IL0.SDR.G8.D1.N	363	IL1.DDR.G2.D0.N
14	GND	64	GND	114	GND	164	: GND	214	JTAG.TCK	264	GND	314	GND	364	GND
15	IL0.DDR.G1.D1.P	65	IL0.DDR.G3.D4.P	115	IL0.SDR.G8.D0.P	165	: VITREF.R.B	215	JTAG.TDO	265	GPMC.S4.P	315	IL0.SDR.G8.D2.P	365	IL1.DDR.G2.D1.P
16	IL0.DDR.G1.D1.N	66	IL0.DDR.G3.D4.N	116	IL0.SDR.G8.D0.N	166	: GND	216	GND	266	GPMC.S4.N	316	IL0.SDR.G8.D2.N	366	IL1.DDR.G2.D1.N
17	GND	67	GND	117	IL0.SDR.G13.D6	167	: VITREF.R.B	217	MCLK.C.P	267	GND	317	GND	367	GND
18	IL0.DDR.G1.D2.P	68	IL0.DDR.G3.S.P	118	GND	168	: VITREF.R.B	218	MCLK.C.N	268	GPMC.S5.P	318	IL0.SDR.G8.D3.P	368	IL1.DDR.G2.D2.P
19	IL0.DDR.G1.D2.N	69	IL0.DDR.G3.S.N	119	GND	169	: GND	219	GND	269	GPMC.S5.N	319	IL0.SDR.G8.D3.N	369	IL1.DDR.G2.D2.N
20	GND	70	GND	120	GND	170	: Reference Input Reference Voltage	220	GND	270	GND	320	GND	370	GND
21	GND	71	GND	121	GND	171	: VITREF.R.B	221	PROG.N	271	GND	321	GND	371	GND
22	IL0.DDR.G1.D3.P	72	IL0.DDR.G0.D0.P	122	GND	172	: VITREF.R.B	222	RSTI.N	272	GPMC.S6.P	322	IL1.DDR.G0.D0.P	372	IL1.DDR.G2.D3.P
23	IL0.DDR.G1.D3.N	73	IL0.DDR.G0.D0.N	123	GND	173	: VITREF.R.B	223	GND	273	GPMC.S6.N	323	IL1.DDR.G0.D0.N	373	IL1.DDR.G2.D3.N
24	GND	74	GND	124	GND	174	GND	224	V48BB	274	GND	324	GND	374	GND
25	IL0.DDR.G1.D4.P	75	IL0.DDR.G0.D1.P	125	GND	175	: VIREF.R.B	225	V48BB	275	GPMC.S7.P	325	IL1.DDR.G0.D1.P	375	IL1.DDR.G2.D4.P
26	IL0.DDR.G1.D4.N	76	IL0.DDR.G0.D1.N	126	GND	176	: VIREF.R.B	226	V48BB	276	GPMC.S7.N	326	IL1.DDR.G0.D1.N	376	IL1.DDR.G2.D4.N
27	GND	77	GND	127	GND	177	GND	227	GND	277	GND	327	GND	377	GND
28	IL0.DDR.G1.S.P	78	IL0.DDR.G0.D2.P	128	GND	178	: VIREF.R.B	228	V48BB	278	GPMC.S8.P	328	IL1.DDR.G0.D2.P	378	IL1.DDR.G2.S.P
29	IL0.DDR.G1.S.N	79	IL0.DDR.G0.D2.N	129	GND	179	: VIREF.R.B	229	V48BB	279	GPMC.S8.N	329	IL1.DDR.G0.D2.N	379	IL1.DDR.G2.S.N
30	GND	80	GND	130	GND	180	GND	230	GND	280	GND	330	GND	380	GND
31	GND	81	GND	131	GND	181	GND	231	V48BB	281	IL0.SDR.G13.C.P	331	GND	381	GND
32	IL0.DDR.G2.D0.P	82	IL0.SDR.G13.C.N	132	GND	182	: VIREF.R.B	232	V48BB	282	IL0.SDR.G13.C.N	332	IL1.DDR.G3.D0.P	382	IL1.DDR.G3.D0.N
33	IL0.DDR.G2.D0.N	83	IL0.SDR.G13.C.N	133	GND	183	: VIREF.R.B	233	GND	283	GND	333	GND	383	GND
34	GND	84	GND	134	GND	184	GND	234	V48BB	284	IL0.SDR.G13.D0.P	334	GND	384	GND
35	IL0.DDR.G2.D1.P	85	IL0.SDR.G13.D0.P	135	GND	185	: VIREF.R.B	235	V48BB	285	IL0.SDR.G13.D0.N	335	IL1.DDR.G0.D4.P	385	IL1.DDR.G3.D1.P
36	IL0.DDR.G2.D1.N	86	IL0.SDR.G13.D0.N	136	GND	186	GND	236	GND	286	GND	336	IL1.DDR.G0.D4.N	386	IL1.DDR.G3.D1.N
37	GND	87	GND	137	GND	187	: VIREF.R.B	237	V48BB	287	IL0.SDR.G13.D1.P	337	GND	387	GND
38	IL0.DDR.G2.D2.P	88	IL0.SDR.G13.D1.P	138	GND	188	: VIREF.R.B	238	V48BB	288	IL0.SDR.G13.D1.N	338	IL1.DDR.G0.S.P	388	IL1.DDR.G3.D2.P
39	IL0.DDR.G2.D2.N	89	IL0.SDR.G13.D1.N	139	GND	189	: VIREF.R.B	239	GND	289	GND	339	IL1.DDR.G0.S.N	389	IL1.DDR.G3.D2.N
40	GND	90	GND	140	GND	190	GND	240	GND	290	GND	340	GND	390	GND
41	GND	91	GND	141	GND	191	GND	241	V48BB	291	IL0.SDR.G13.D2.P	341	GND	391	GND
42	IL0.DDR.G2.D3.P	92	IL0.SDR.G13.D2.P	142	GND	192	: VIREF.R.B	242	V48BB	292	IL0.SDR.G13.D2.N	342	IL1.DDR.G1.D0.P	392	IL1.DDR.G3.D3.P
43	IL0.DDR.G2.D3.N	93	IL0.SDR.G13.D2.N	143	GND	193	: VIREF.R.B	243	GND	293	GND	343	GND	393	GND
44	GND	94	GND	144	GND	194	GND	244	V48BB	294	IL0.SDR.G13.D3.P	344	GND	394	GND
45	IL0.DDR.G2.D4.P	95	IL0.SDR.G13.D3.P	145	GND	195	: VIREF.R.B	245	V48BB	295	IL0.SDR.G13.D3.N	345	IL1.DDR.G1.D1.P	395	IL1.DDR.G3.D4.P
46	IL0.DDR.G2.D4.N	96	IL0.SDR.G13.D3.N	146	GND	196	: VIREF.R.B	246	GND	296	GND	346	IL1.DDR.G1.D1.N	396	IL1.DDR.G3.D4.N
47	GND	97	GND	147	GND	197	: VIREF.R.B	247	V48BB	297	IL0.SDR.G13.D4.P	347	GND	397	IL1.DDR.G3.S.P
48	IL0.DDR.G2.S.P	98	IL0.SDR.G13.D4.P	148	GND	198	: VIREF.R.B	248	V48BB	298	IL0.SDR.G13.D4.N	348	IL1.DDR.G1.D2.N	398	IL1.DDR.G3.S.N
49	IL0.DDR.G2.S.N	99	IL0.SDR.G13.D4.N	149	GND	199	GND	249	GND	299	GND	349	GND	399	GND
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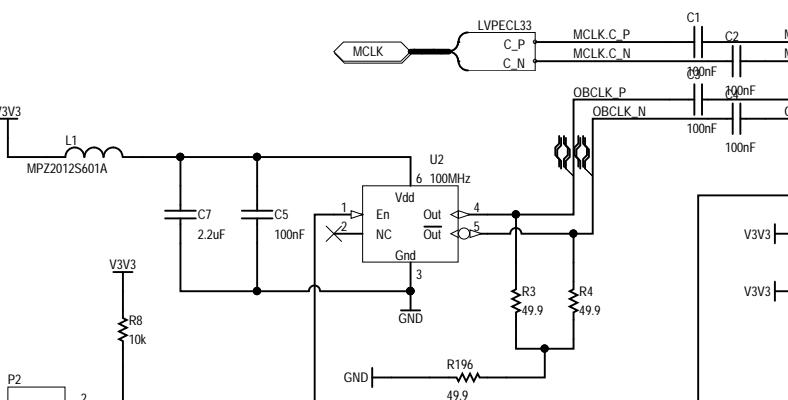
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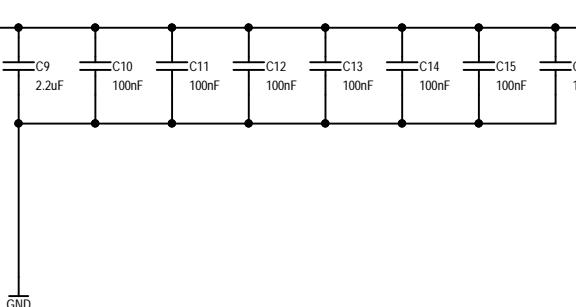


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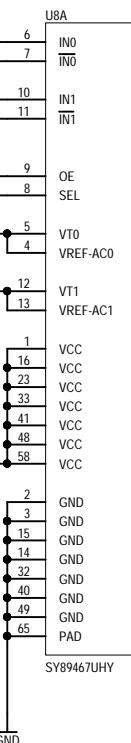
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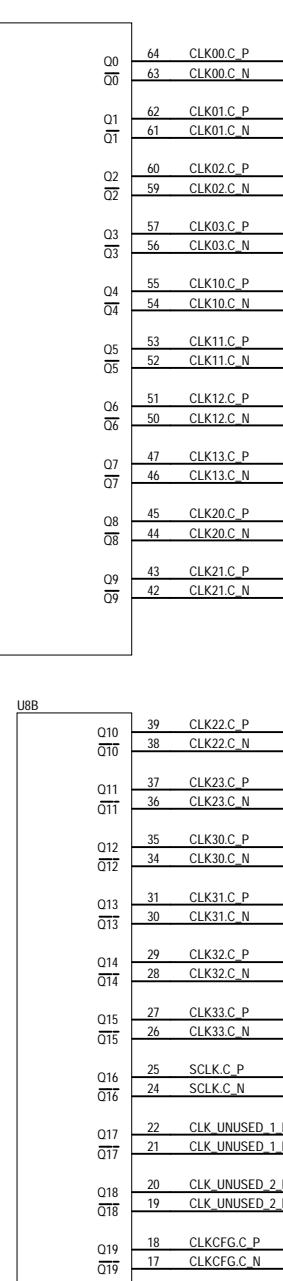


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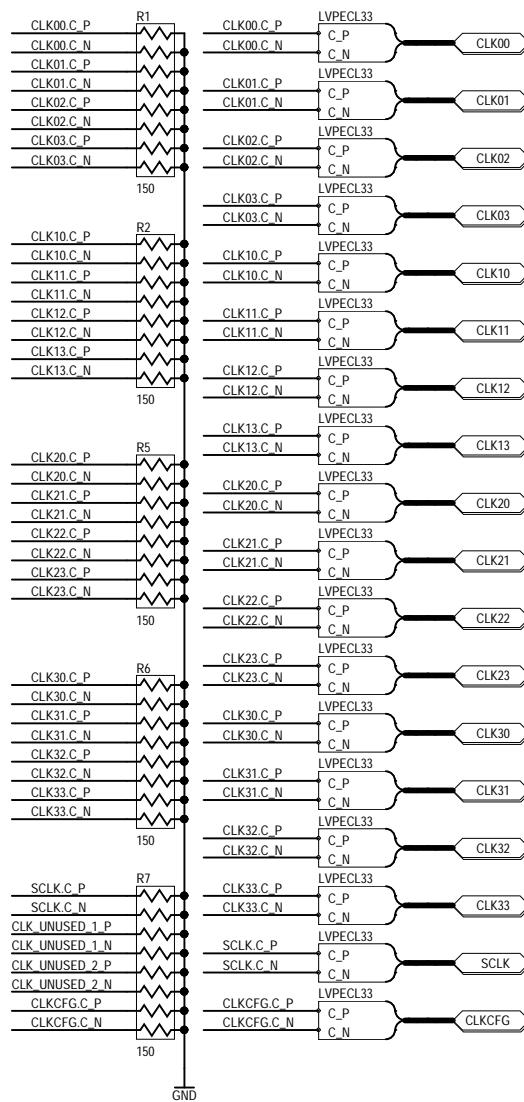


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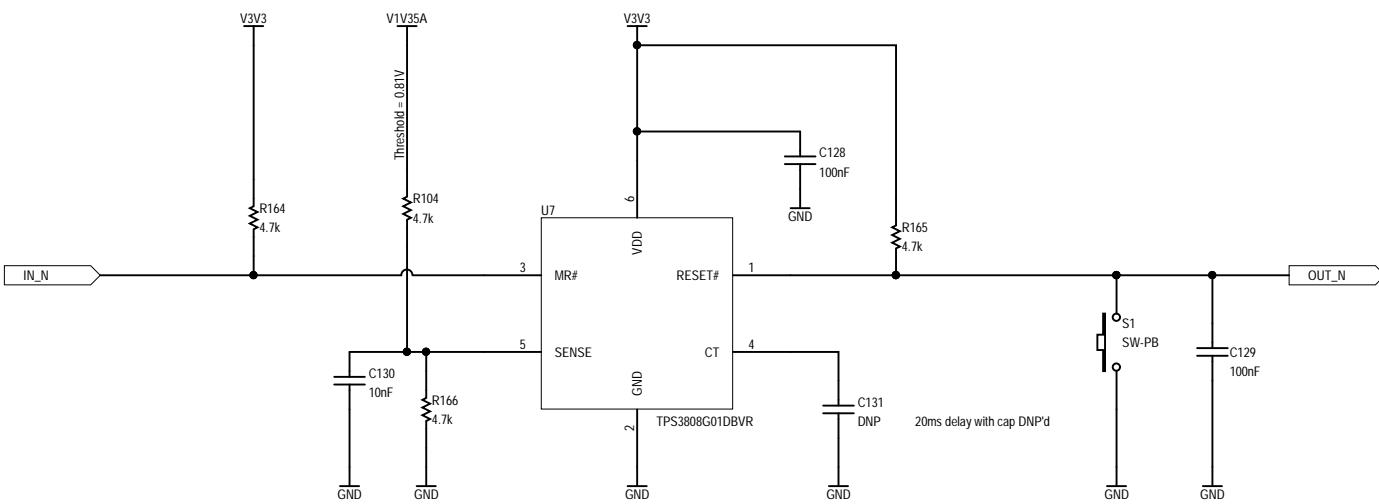
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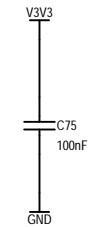
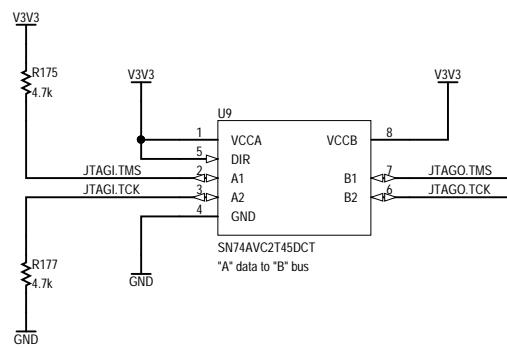
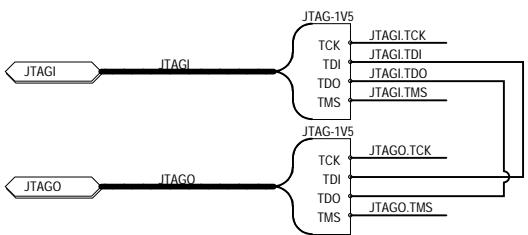
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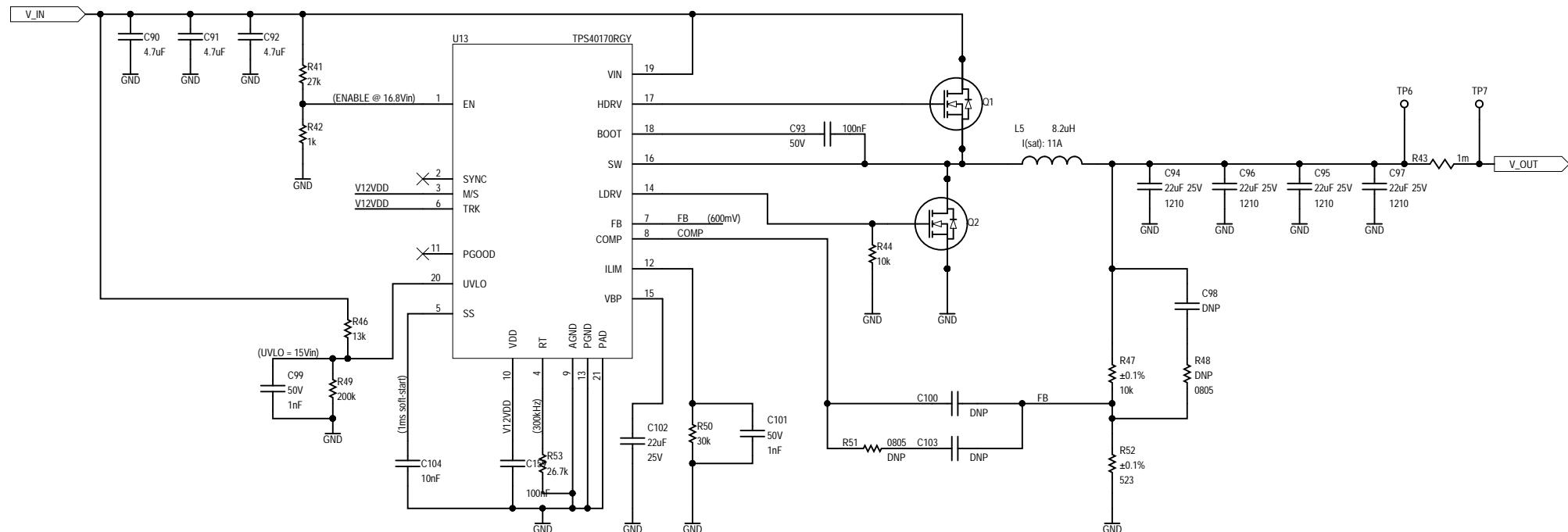
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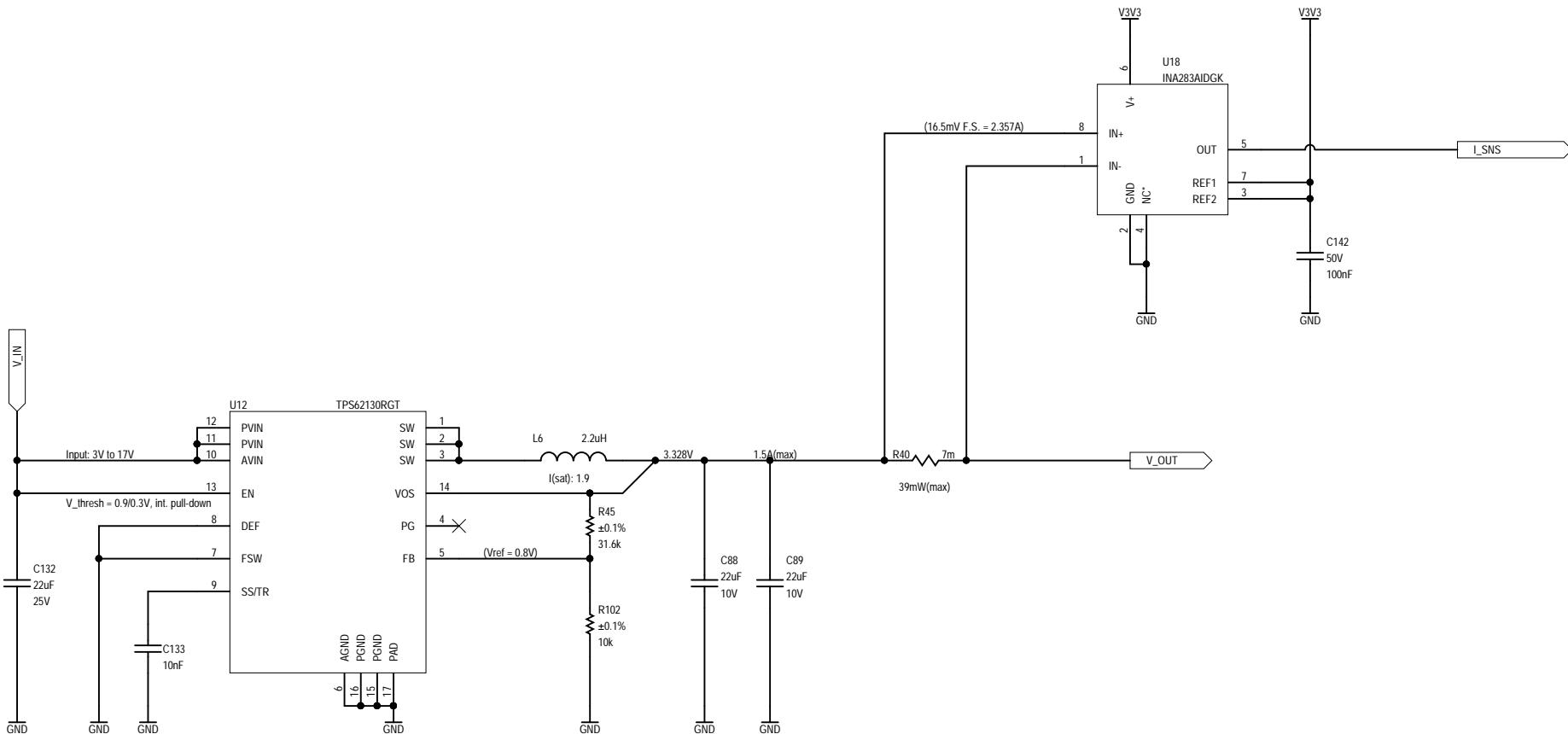
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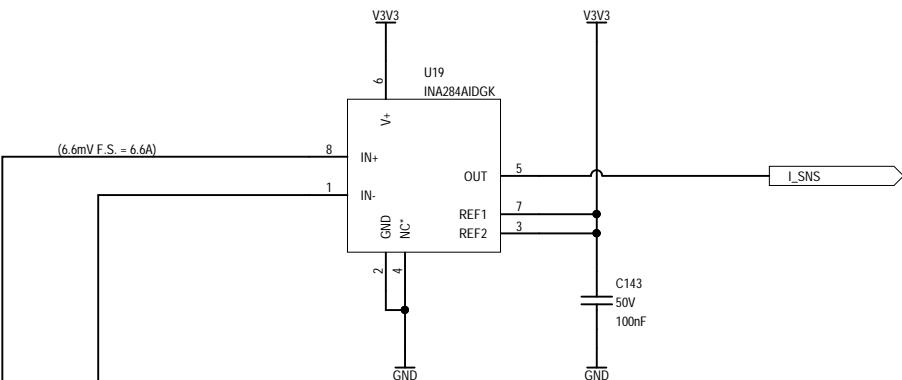
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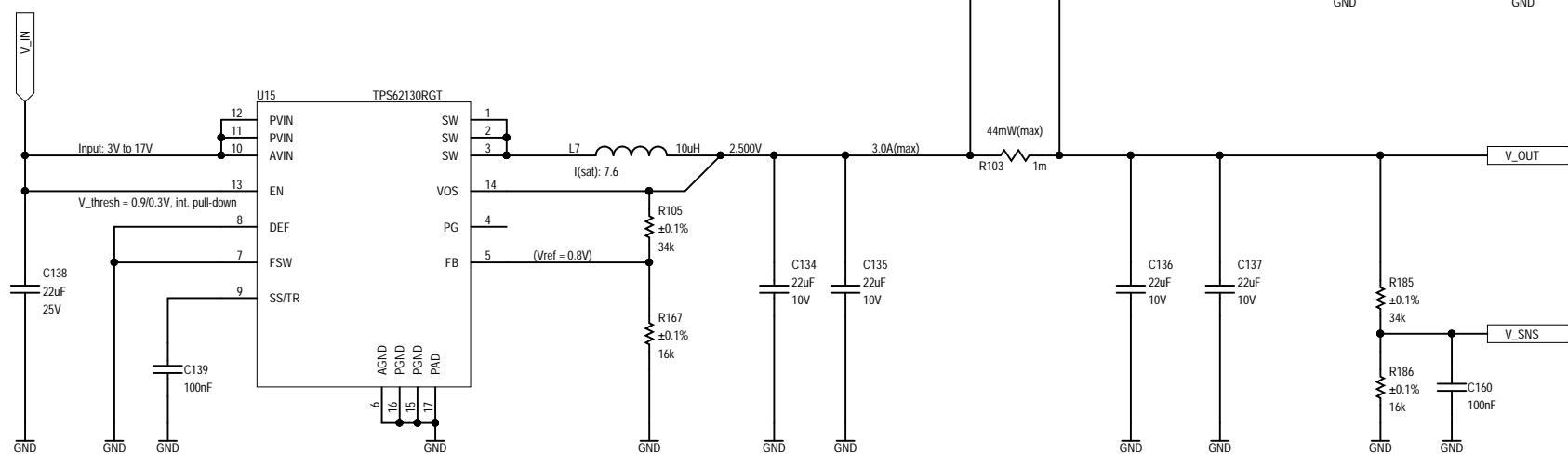




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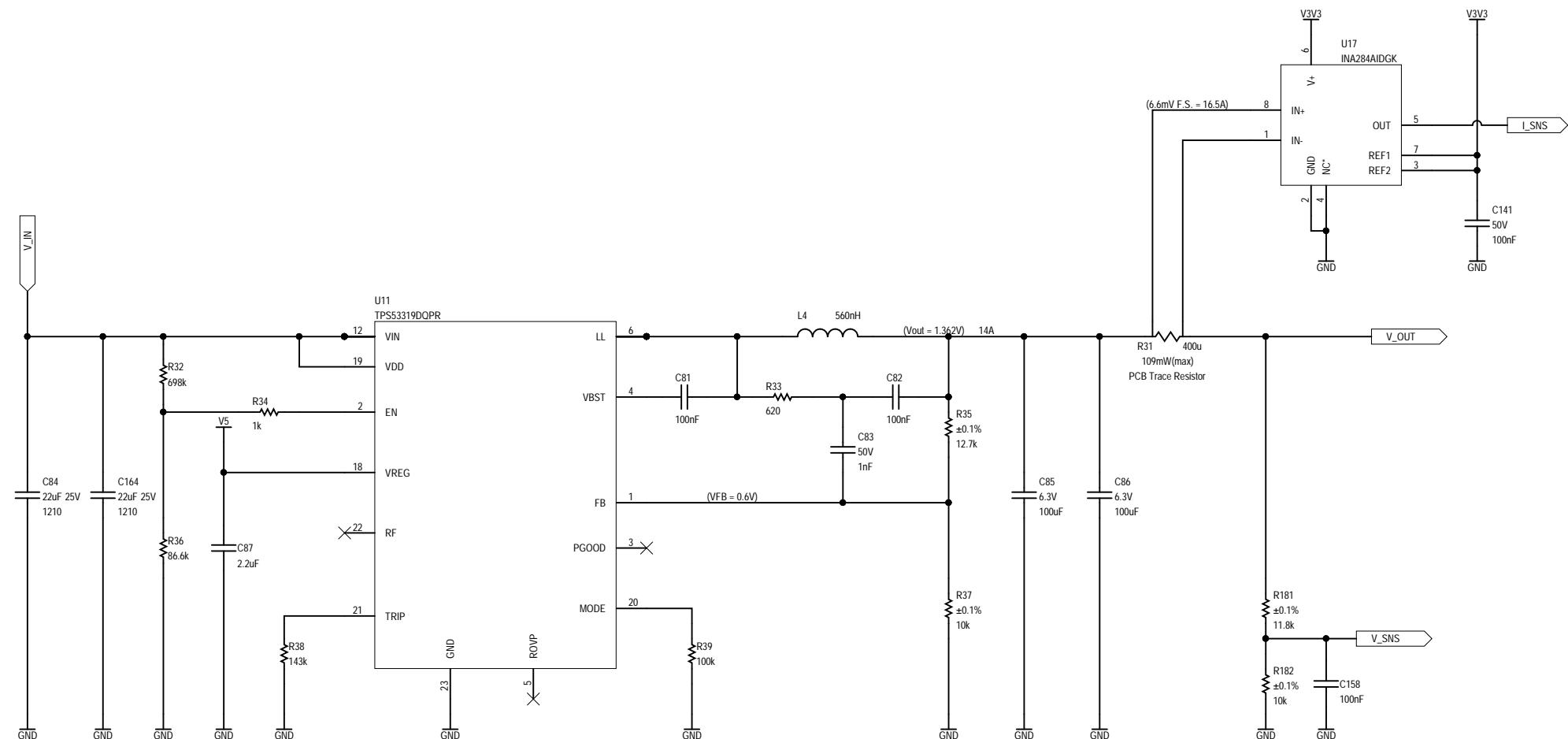


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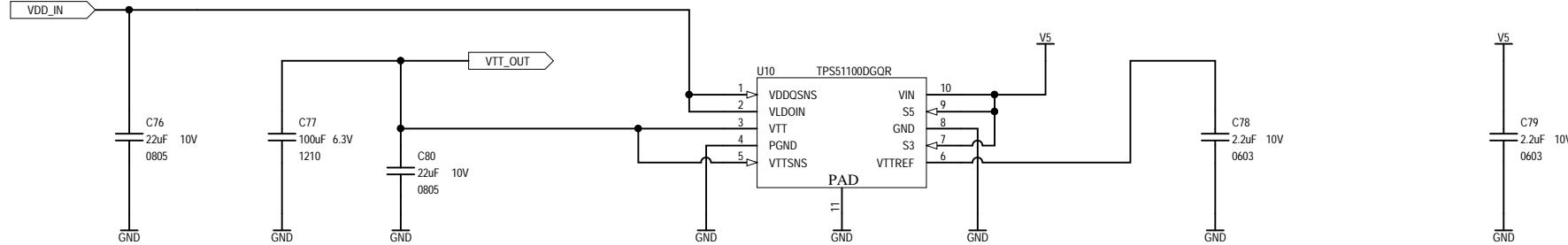


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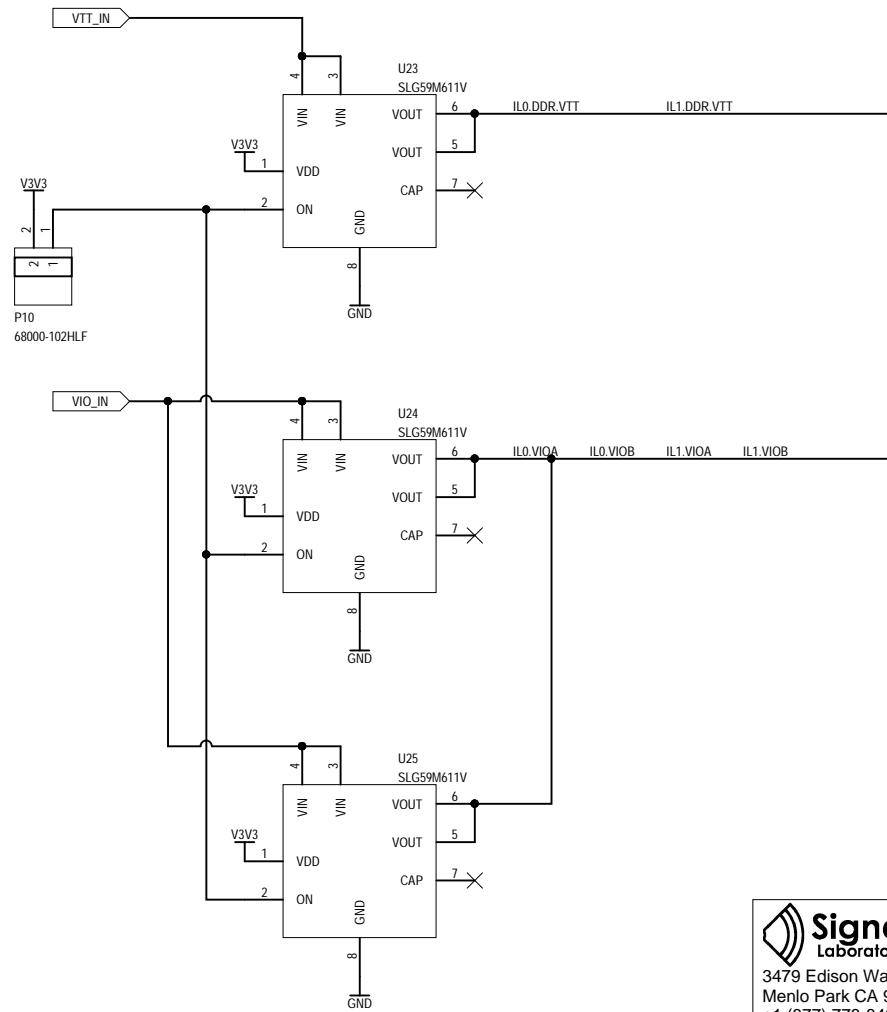
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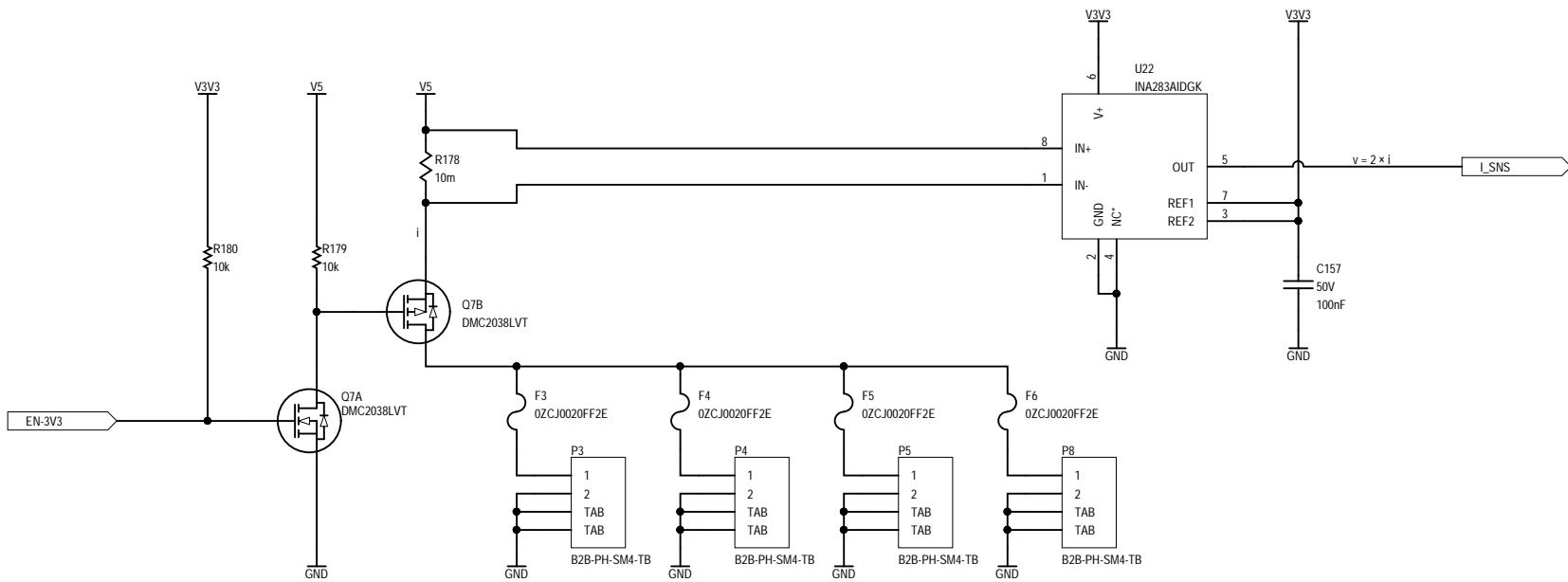
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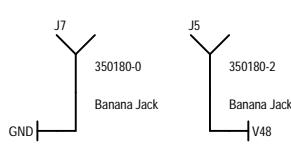


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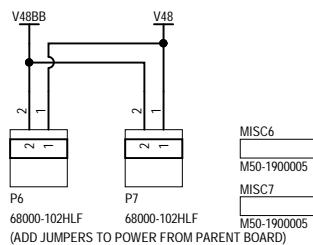
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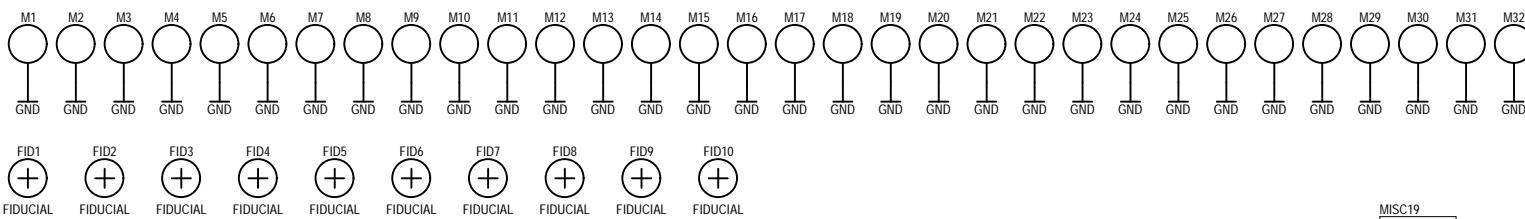


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