Copper Suicide™ User Manual
Scalable FPGA Development Board

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1 Abstract

Copper Suicide is a scalable FPGA development board based on the Lattice Semiconductor ECP5 FPGA. It consists of an Arm Cortex-M7 processor, 1 configuration FPGA, 8 gigabytes of DDR3 SDRAM, and 16 general purpose FPGAs in a square 2-dimensional architecture. The design measures 200x200 mm and is extensible by stacking additional boards on top or bottom.

2 Overview

Copper Suicide is designed to have the most flexibility between interconnections, and the highest data rate. There are 3 primary ways to communicate with the FPGA. First, each chip has 4 edge buses. These connect to adjacent FPGA's. On the left/right board edges they connect to DRAM chips. On the top/bottom board edges they connect to either top or bottom board-to-board connectors. Second, the Memory and Interupt Bus (MIB) is a 29-pin multi-drop bus which connects all 17 FPGAs. Third, there is a 5-pin programming bus connecting each FPGA to the configuration FPGA.

There is an additional 41-bit SRAM memory interface between the MCU and configuration FPGA. This bus may also be used as a general purpose interface between the MCU and configuration FPGA.

There are two more dedicated MIB from the configuration FPGA, one to the bottom board connector and one to the top.

Also, each FPGA has a dedicated point-of-presence power supply controller which allows monitoring and adjustment of individual FPGA current and voltages. Global power supply voltages and currents are also monitored.

Finally, 128 megabytes of NOR Flash is provided on the configuration FPGA, and 256 megabytes on the MCU. Indicator LEDs are connected to the MCU and each FPGA.

2.1 Block Diagram

The FPGA block diagram, Figure 1, shows all FPGA and ARM connections.

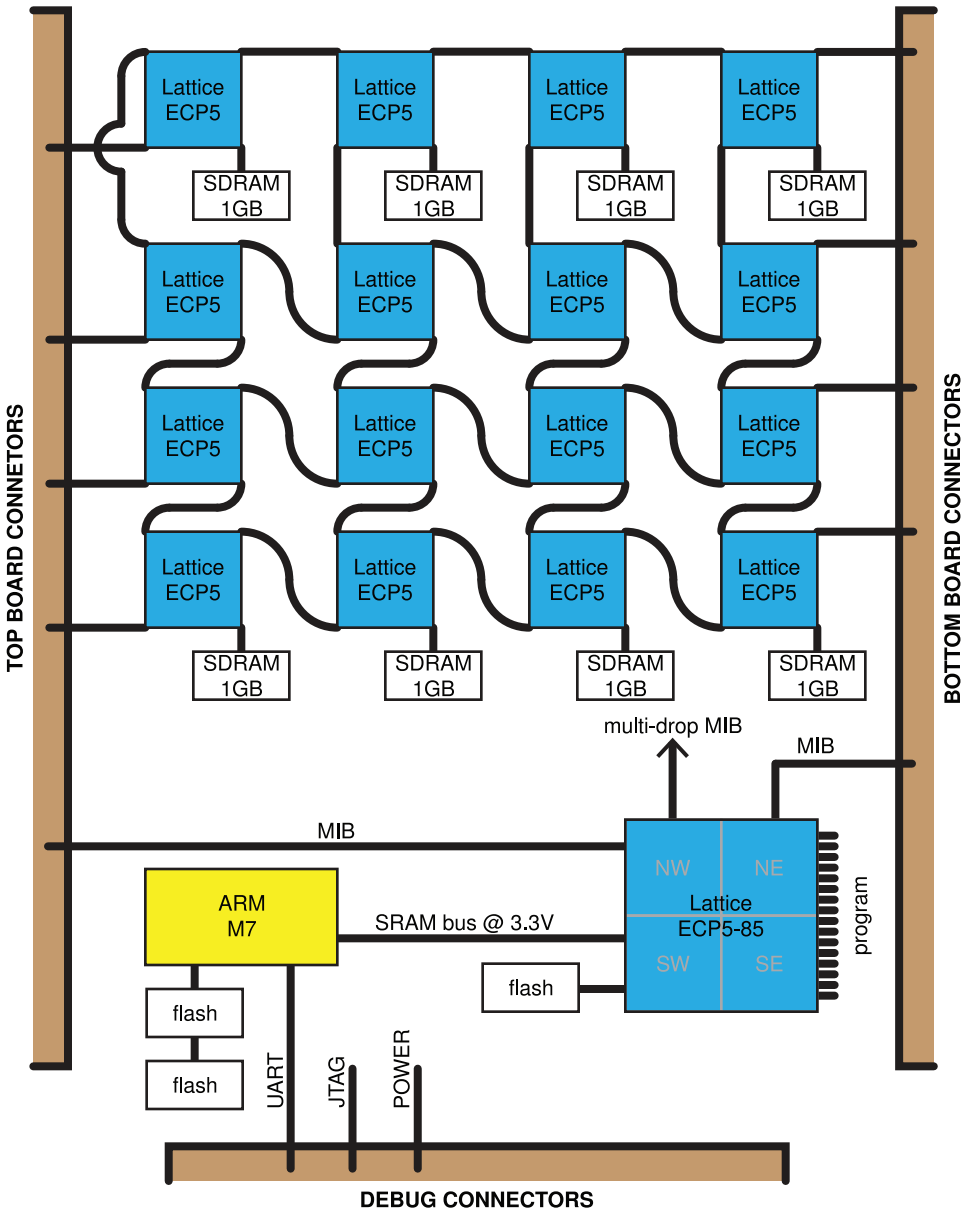


Figure 1: Copper Suicide Block Diagram

2.2 FPGA Harnesses

For simplicity of design, all FPGAs share the same schematic. Figure 2 shows the FPGA interconnections. Figure 3 shows the harness wiring bundles.

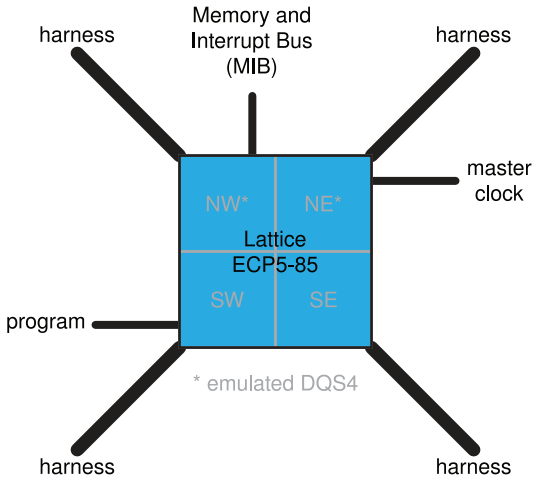


Figure 2: Copper Suicide FPGA

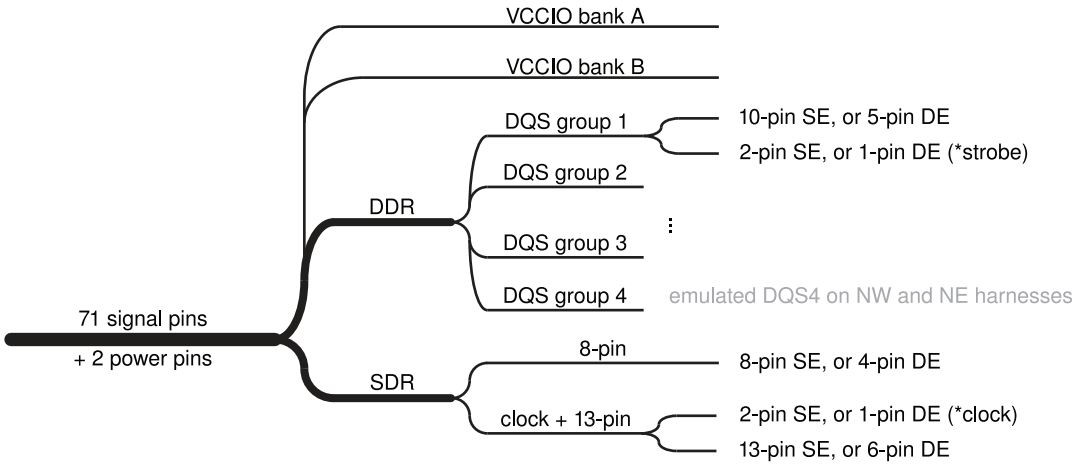


Figure 3: Copper Suicide Harness

2.3 JTAG

The JTAG daisy-chain starts with the MCU and then connects to the configuration FPGA and then the rest of the array, figure 4. Each device may be removed from the daisy chain with jumpers on the side of the board. If there is a need to connect to a single device the same jumpers may be used as a direct JTAG connection. The daisy-chain loops back around from the last FPGA in the array to the MCU.

By default the MCU disables JTAG and instead uses SWD programming. When in SWD mode the MCU must be bypassed to read from the array.

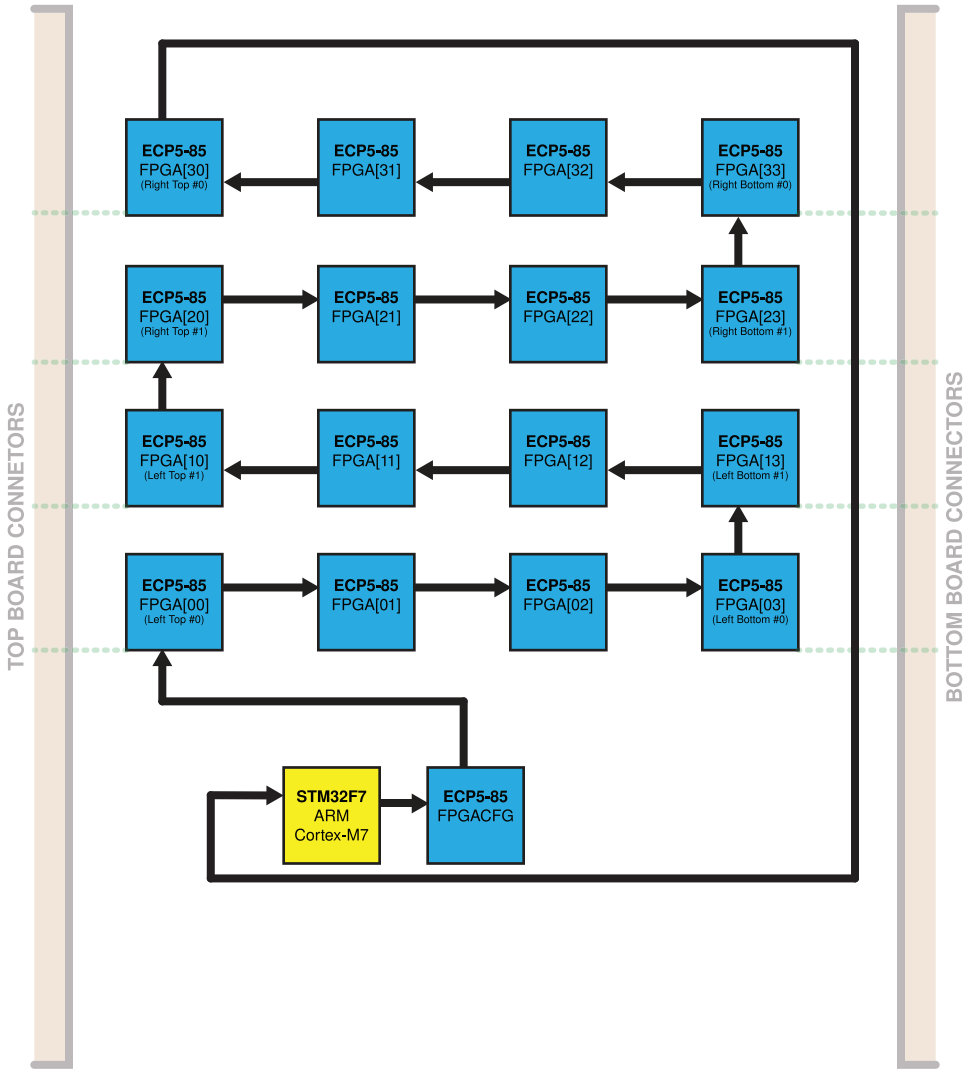


Figure 4: Copper Suicide JTAG Block Diagram

2.3.1 headers

There are 18 JTAG connectors which include the MCU, the configuration FPGA, and the 16 FPGA arrray. The connectors are 10-pin, 50mil pitch, male, unshrouded right-angle thru-hole connectors (Sullins part number GRPB052VWVN).

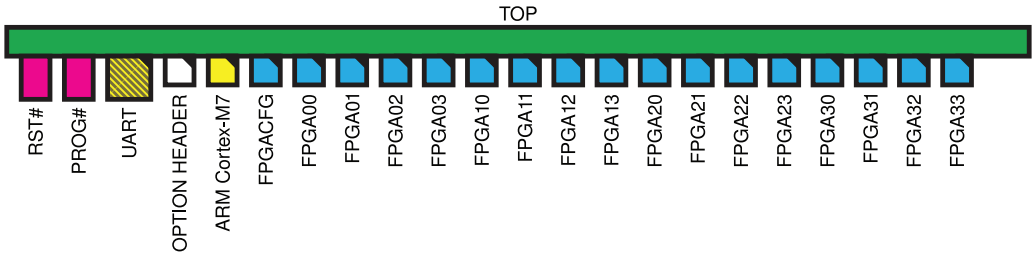
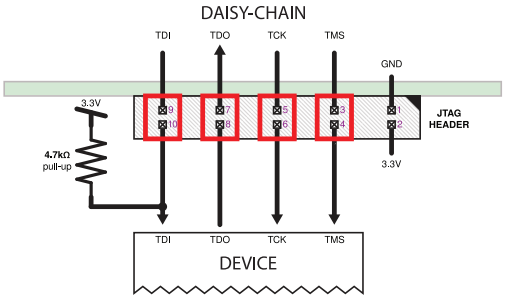
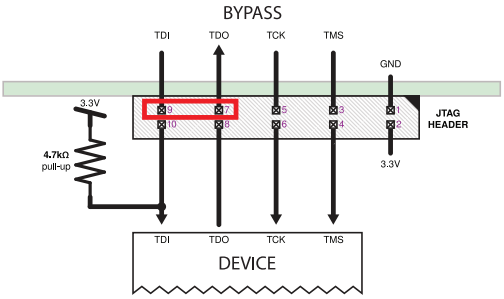


Figure 5: Copper Suicide Debug Headers

They can be jumpered (inserted into the daisy chain) or bypassed (taken out of the daisy chain) with 50mil pitch jumpers (Harwin P/N M50-2000005).



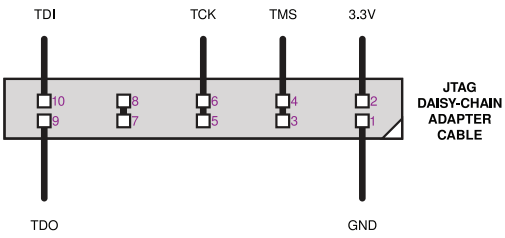
(a) JTAG daisy-chain jumper configuration



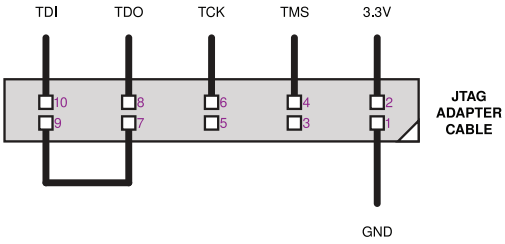
(b) JTAG bypass jumper configuration

2.3.2 JTAG Adapter Cables

The JTAG connectors are non standard and an adapter cable is used to connect it to the Lattice provided JTAG programmer (Lattice P/N HW-USBN-2B). There are two JTAG Adapter Cables. First, a non-daisy chain cable shorts the daisy-chain loop and allows the programmer to access just one device. Second, a daisy-chain programming cable connects to all devices which have been connected in the chain. The JTAG adapter cables use 50mil pitch female connectors (Amphenol/FCI part number 20021311-00010T4LF).



(a) JTAG daisy-chain cable



(b) JTAG cable