MAIN
main.SchDoc

MECH
mechanical.SchDoc

NOTE: DO ECP5 DESIGN CHECKLIST!!

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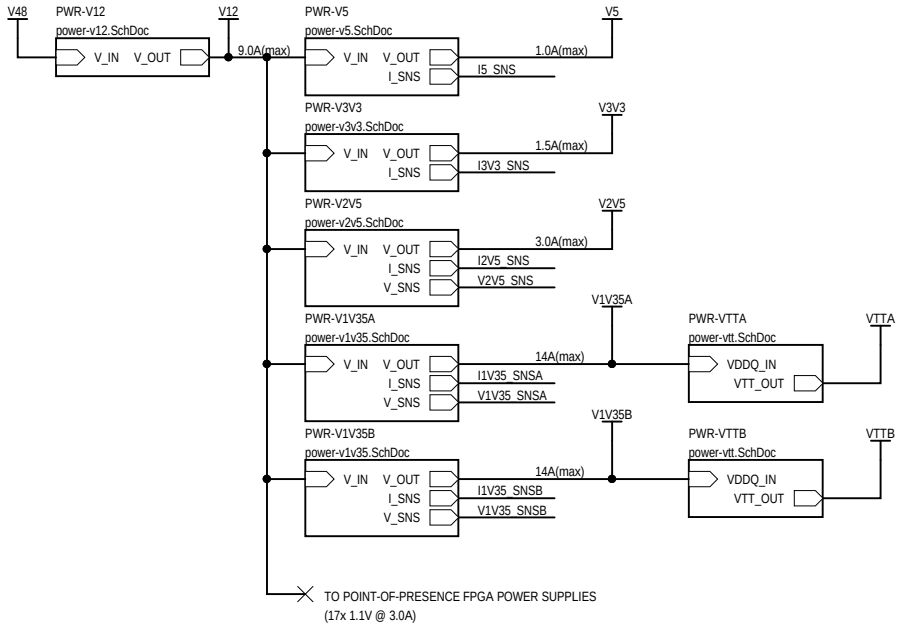
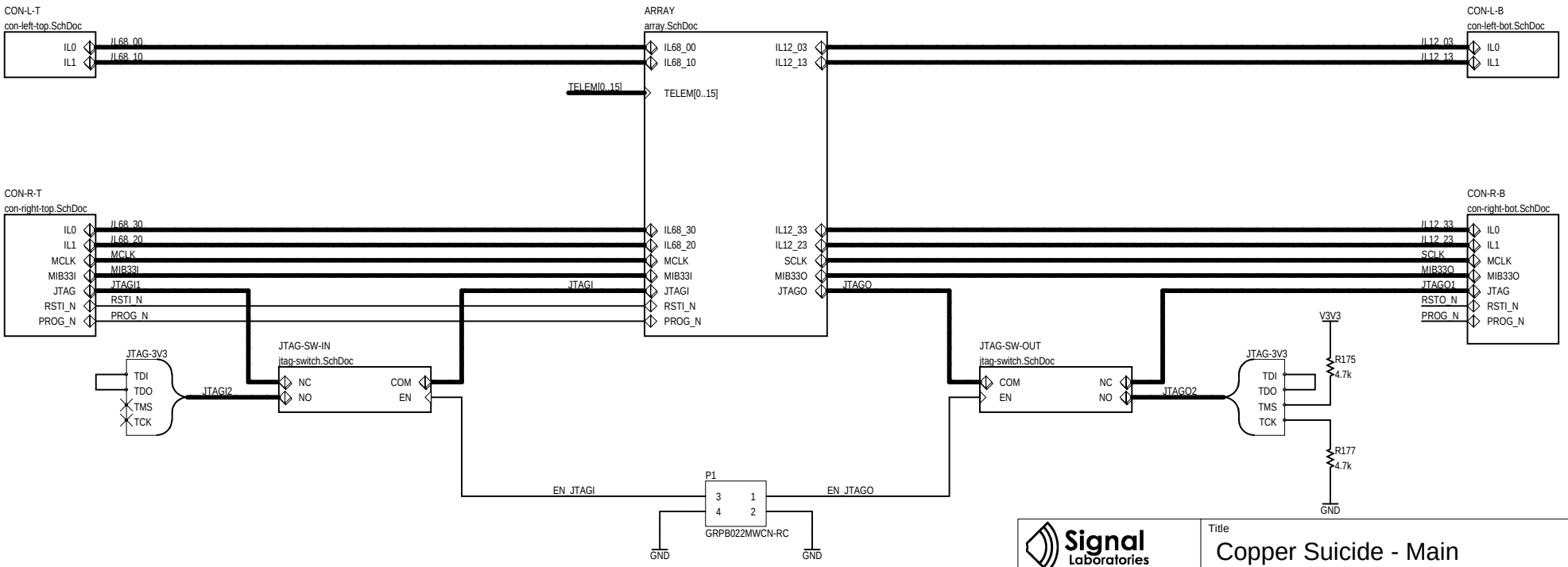
Title
Copper Suicide - Top

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 1 of 43	Date: 3/27/2017



I3V3_SNS	NT659	A B	TELEM0
I2V5_SNS	NT660	A B	TELEM1
V2V5_SNS	NT661	A B	TELEM2
I1V35_SNSA	NT662	A B	TELEM3
V1V35_SNSA	NT663	A B	TELEM4
I1V35_SNSB	NT664	A B	TELEM5
V1V35_SNSB	NT665	A B	TELEM6
IL68_30.DDR.VTT	NT666	A B	TELEM7
IL68_30.VIOA	NT667	A B	TELEM8
IL68_10.DDR.VTT	NT668	A B	TELEM9
IL68_10.VIOA	NT669	A B	TELEM10
IL12_13.DDR.VTT	NT670	A B	TELEM11
IL12_13.VIOA	NT671	A B	TELEM12
IL12_33.DDR.VTT	NT672	A B	TELEM13
IL12_33.VIOA	NT673	A B	TELEM14
I5_SNS	NT17	A B	TELEM15



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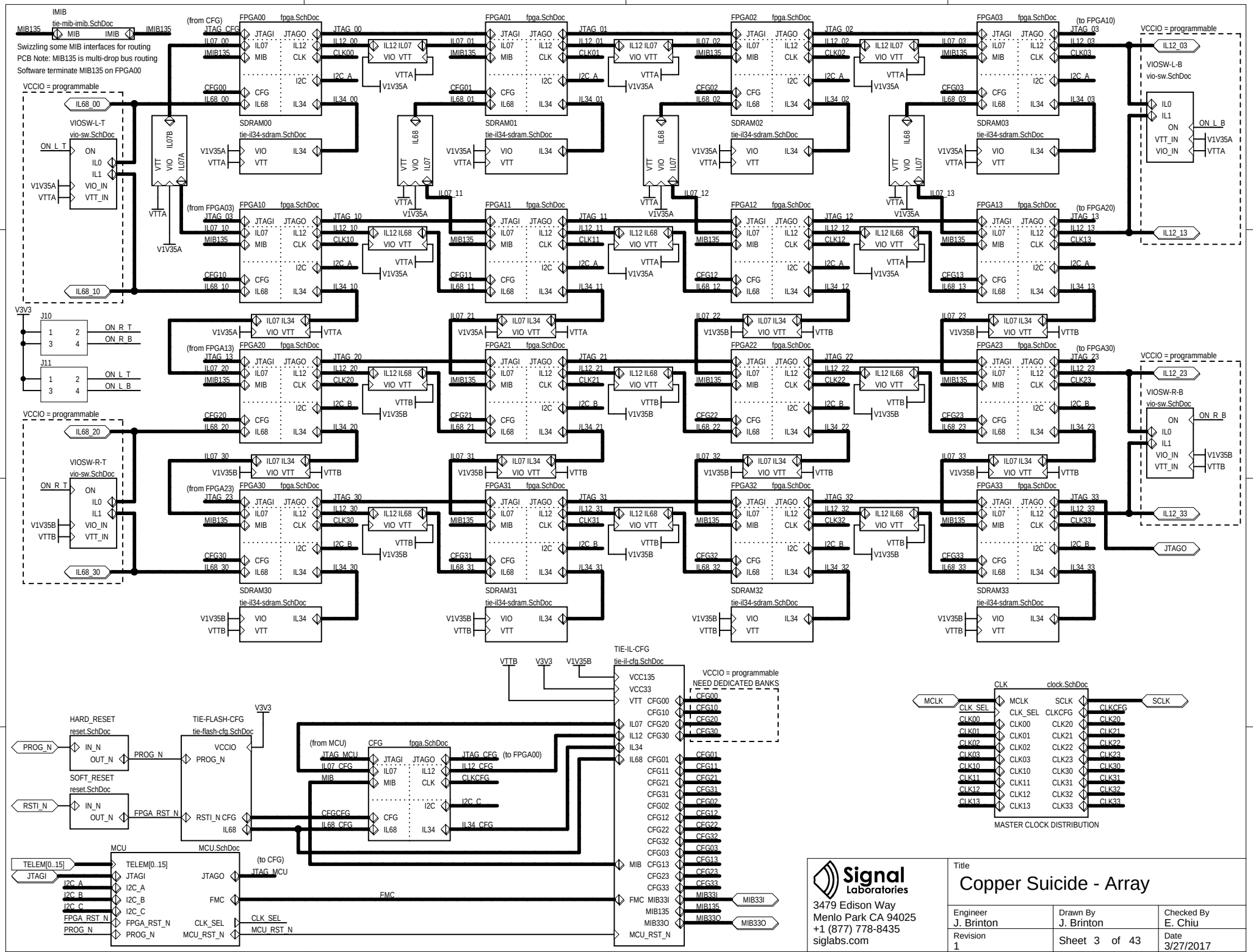
Title
Copper Suicide - Main

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 2 of 43	Date: 3/27/2017



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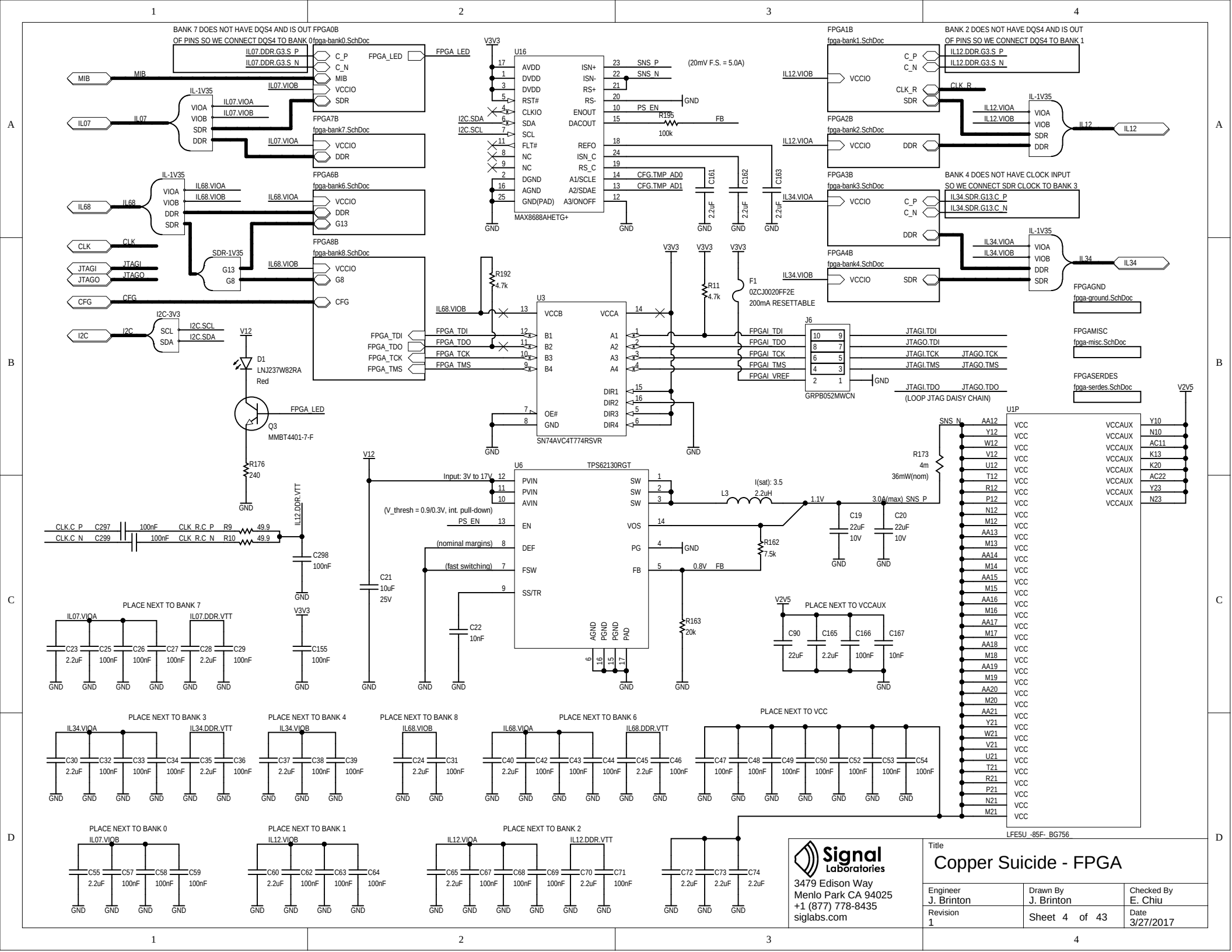
Title
Copper Suicide - Array

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 3 of 43	Date: 3/27/2017


BANK 7 DOES NOT HAVE DQS4 AND IS OUT OF PINS SO WE CONNECT DQS4 TO BANK 0
fpga-bank0.SchDoc
FPGA7B
fpga-bank7.SchDoc
FPGA6B
fpga-bank6.SchDoc
FPGA8B
fpga-bank8.SchDoc
FPGA1B
fpga-bank1.SchDoc
BANK 2 DOES NOT HAVE DQS4 AND IS OUT OF PINS SO WE CONNECT DQS4 TO BANK 1
FPGA2B
fpga-bank2.SchDoc
FPGA3B
fpga-bank3.SchDoc
BANK 4 DOES NOT HAVE CLOCK INPUT SO WE CONNECT SDR CLOCK TO BANK 3
FPGA4B
fpga-bank4.SchDoc
MAX8688AHETG+
SN74AVC4T774RSVR
TPS62130RGT
LFE5U -85F- BG756
GRPB052MWCN
0ZCJ0020FF2E
200mA RESETTABLE
LNJ237W82RA
MMBT4401-7-F
FPGAGND
fpga-ground.SchDoc
FPGAMISC
fpga-misc.SchDoc
FPGASERDES
fpga-serdes.SchDoc
(20mV F.S. = 5.0A)
(LOOP JTAG DAISY CHAIN)
PLACE NEXT TO BANK 7
PLACE NEXT TO VCCAUX
PLACE NEXT TO BANK 3
PLACE NEXT TO BANK 4
PLACE NEXT TO BANK 8
PLACE NEXT TO BANK 6
PLACE NEXT TO VCC
PLACE NEXT TO BANK 0
PLACE NEXT TO BANK 1
PLACE NEXT TO BANK 2
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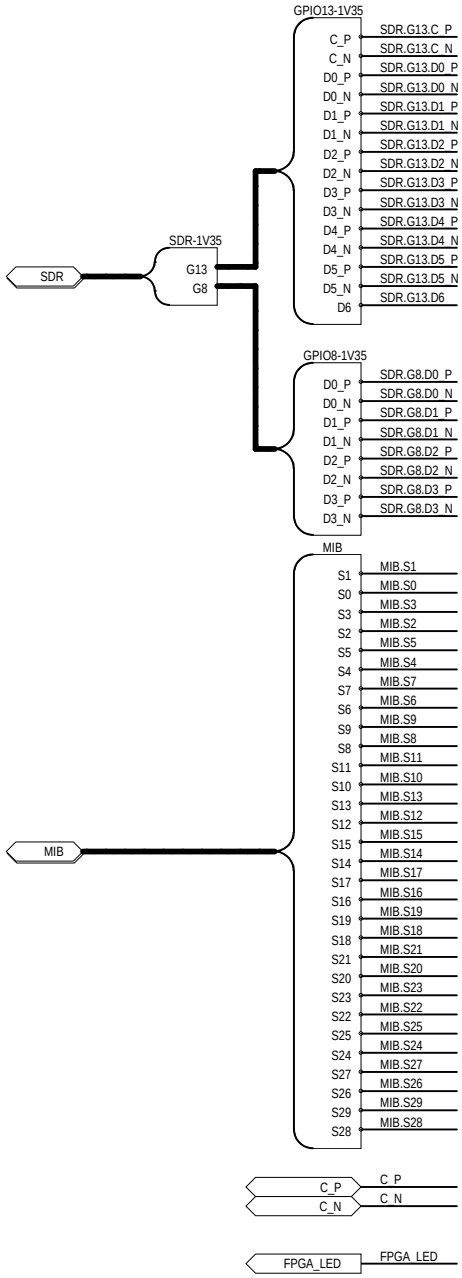
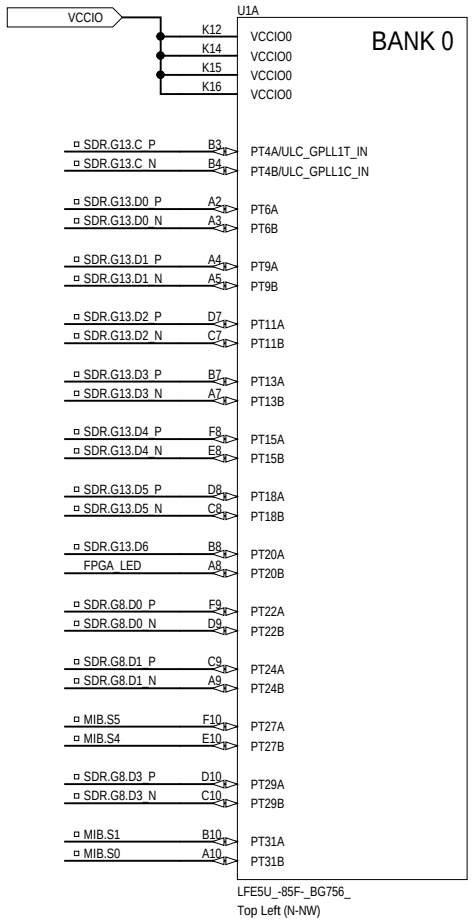
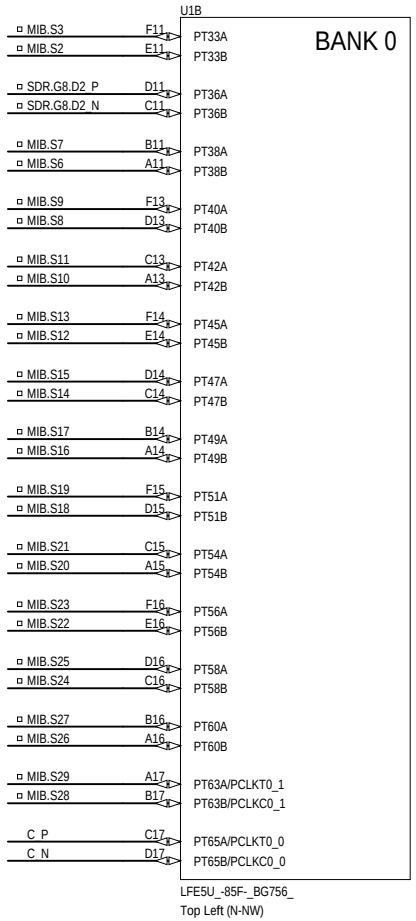
Title
Copper Suicide - FPGA
Engineer
J. Brinton
Drawn By
J. Brinton
Checked By
E. Chiu
Revision
1
Sheet 4 of 43
Date
3/27/2017







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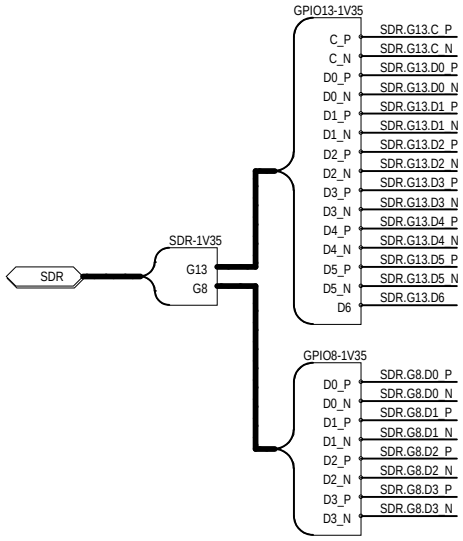
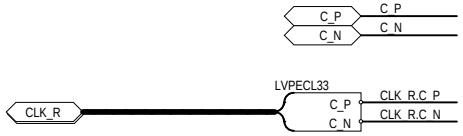
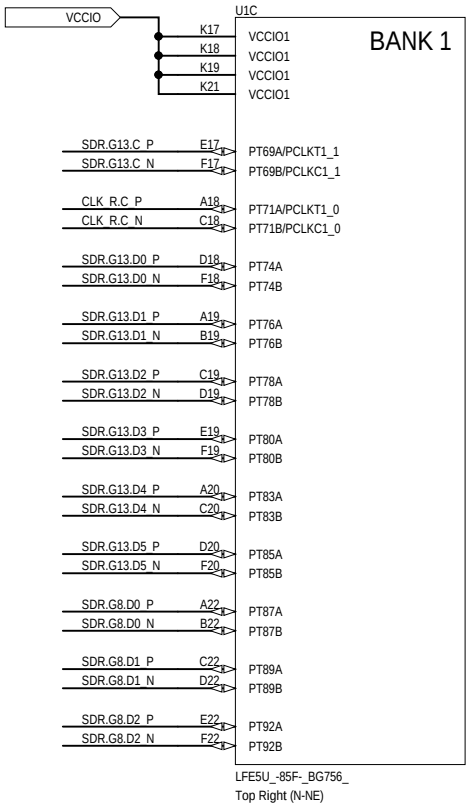
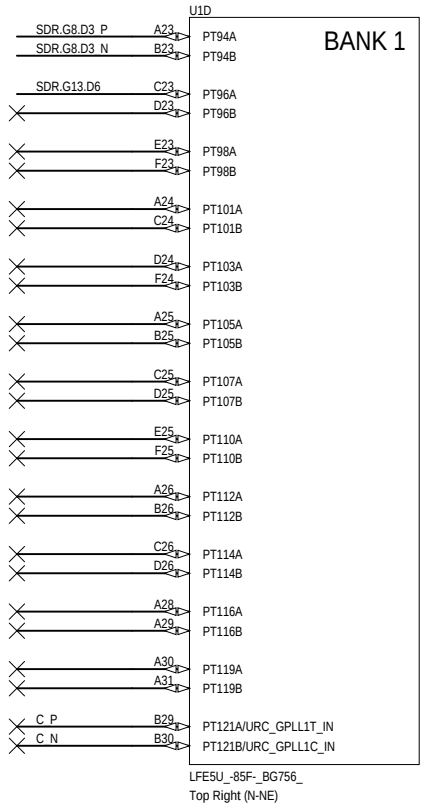
Title
Copper Suicide - FPGA - Bank 0

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 5 of 43	Date: 3/27/2017









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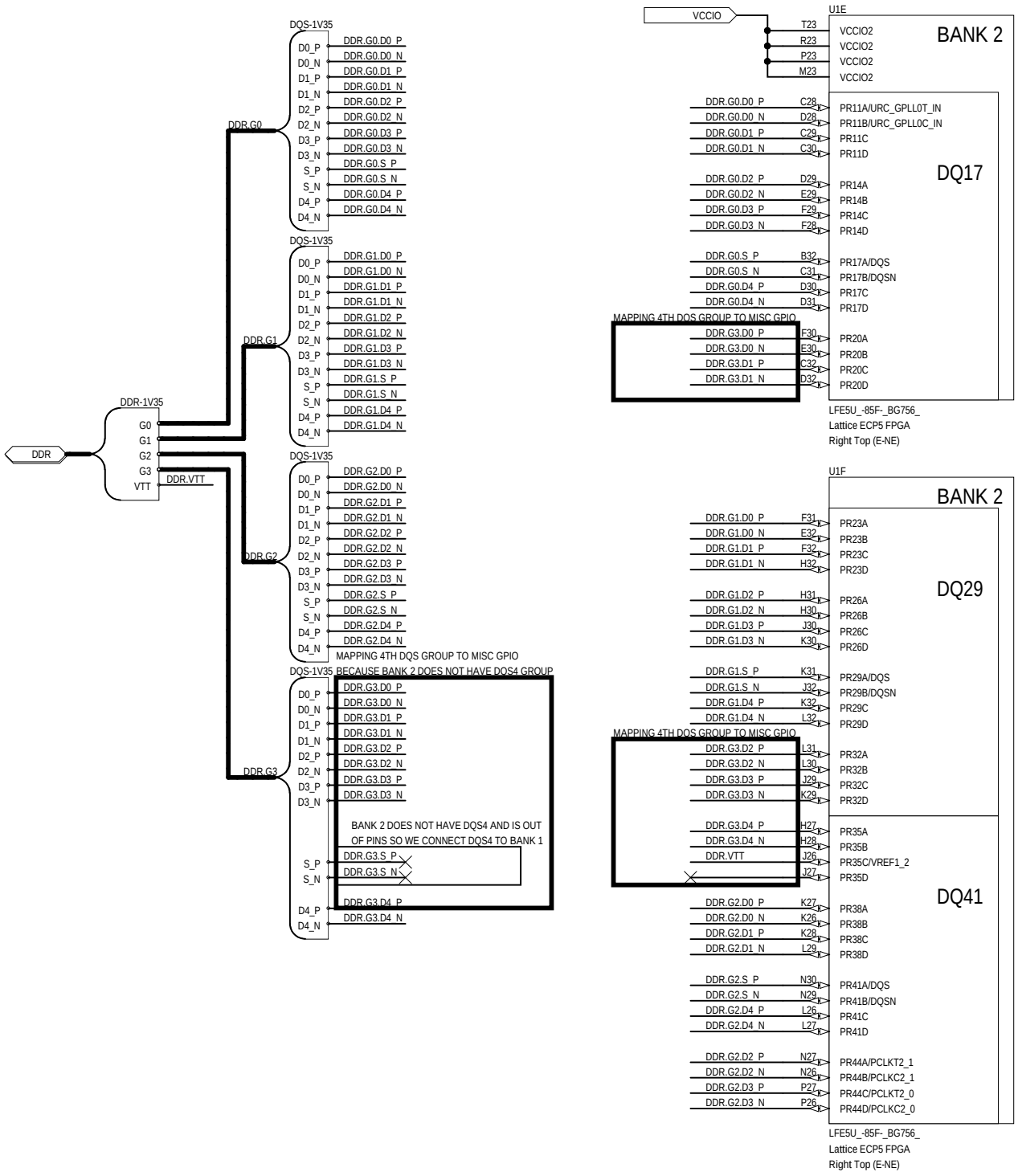
Title: Copper Suicide - FPGA - Bank 1

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 6 of 43	Date: 3/27/2017



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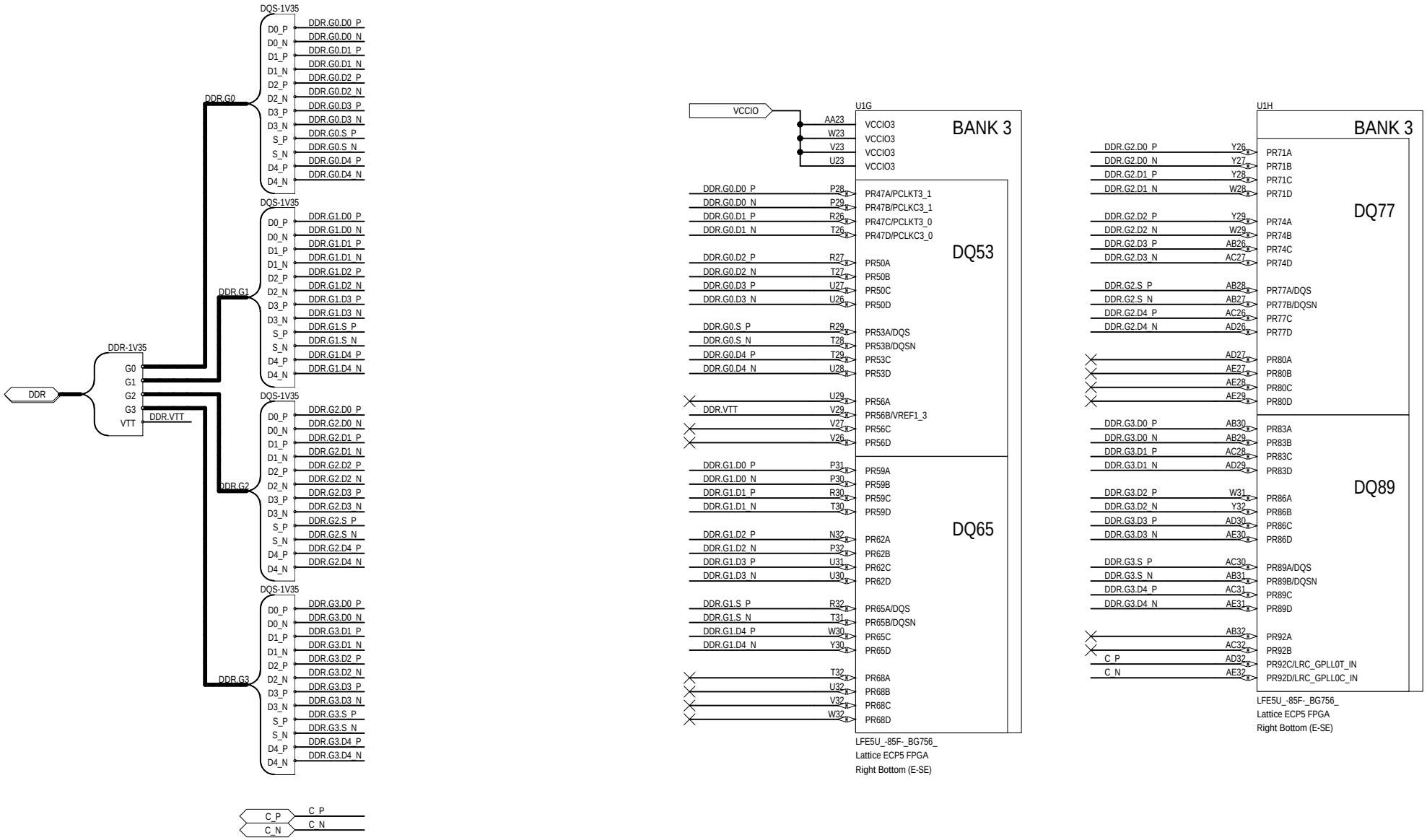
Title: Copper Suicide - FPGA - Bank 2

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 7 of 43	Date: 3/27/2017



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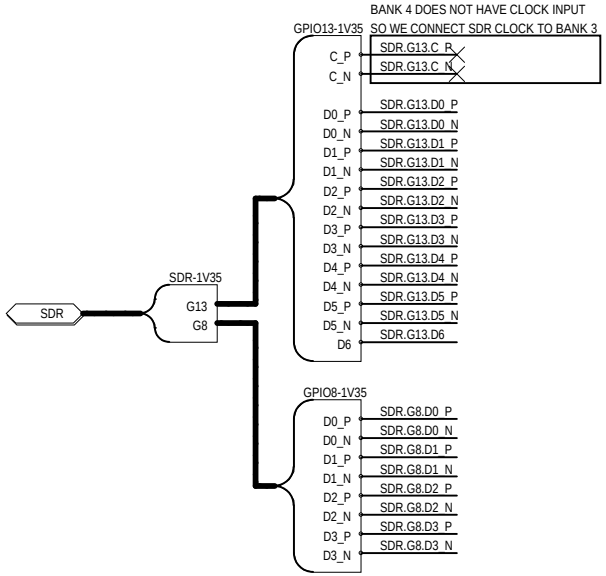
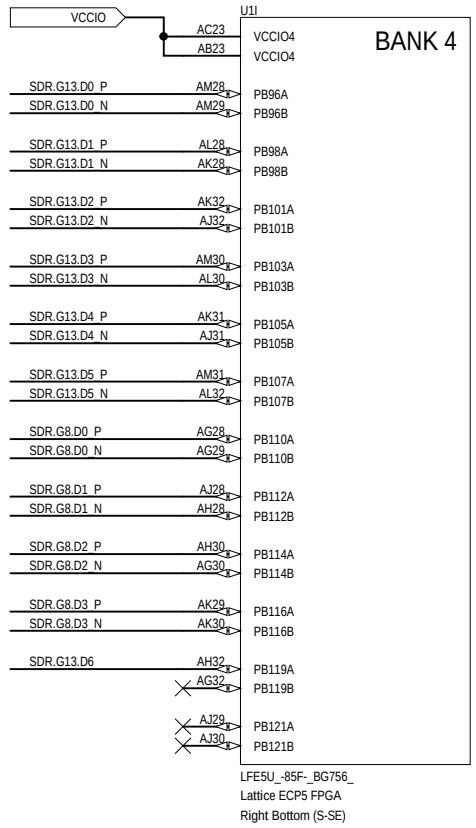
Title: Copper Suicide - FPGA - Bank 3

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 8 of 43	Date: 3/27/2017





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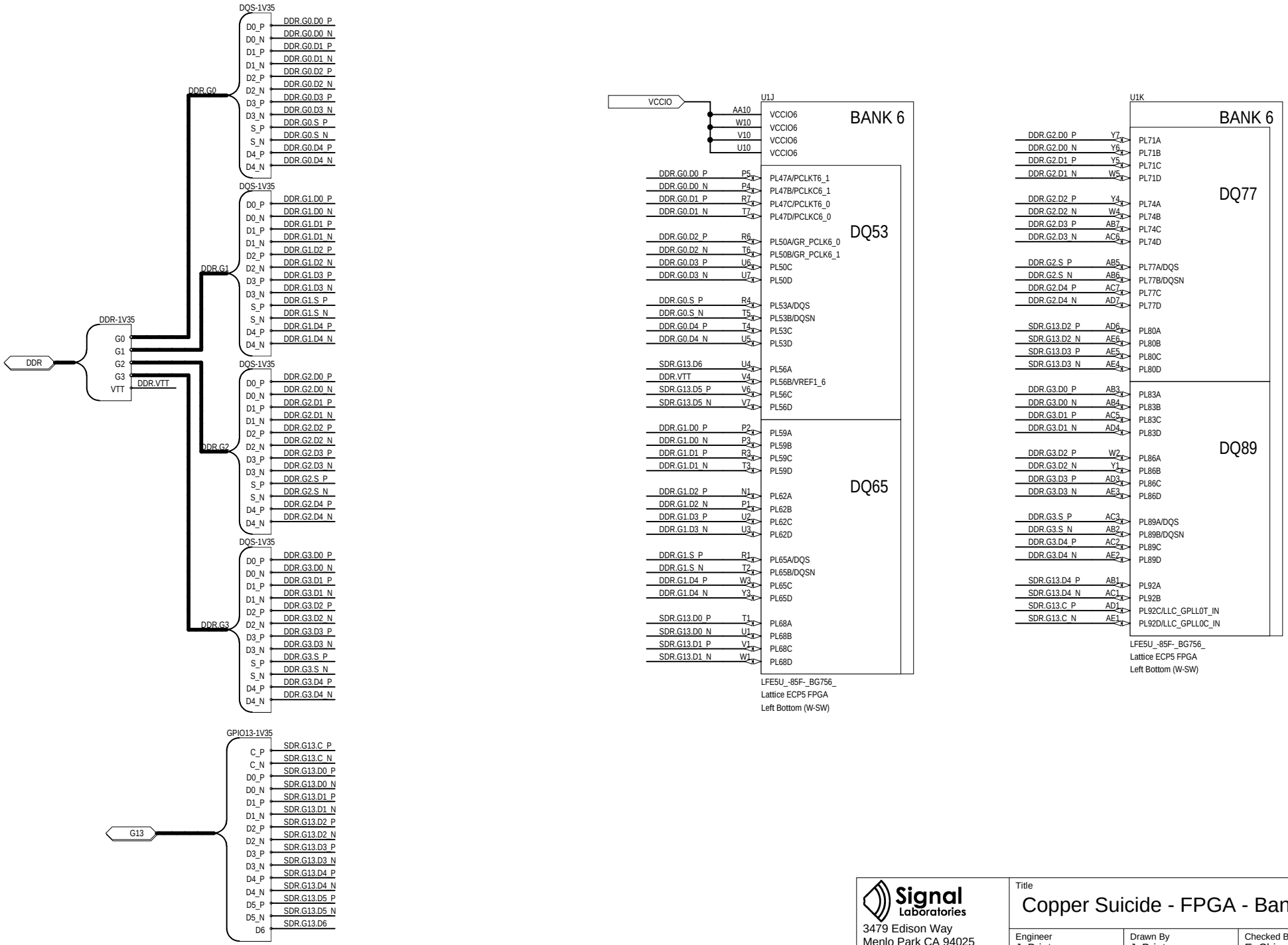
Title: Copper Suicide - FPGA - Bank 4

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 9 of 43	Date: 3/27/2017



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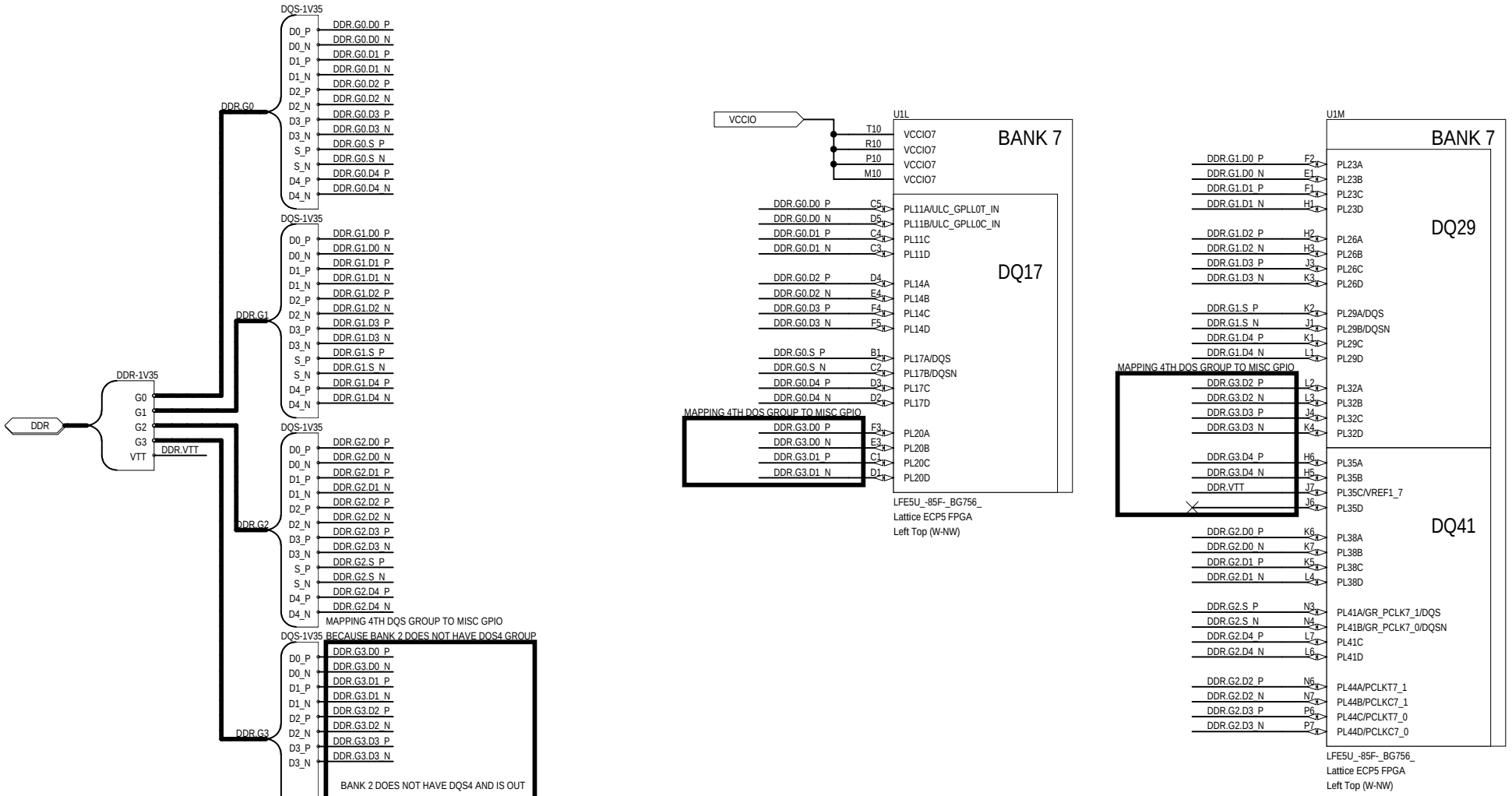
Title: Copper Suicide - FPGA - Bank 6

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 10 of 43	Date: 3/27/2017



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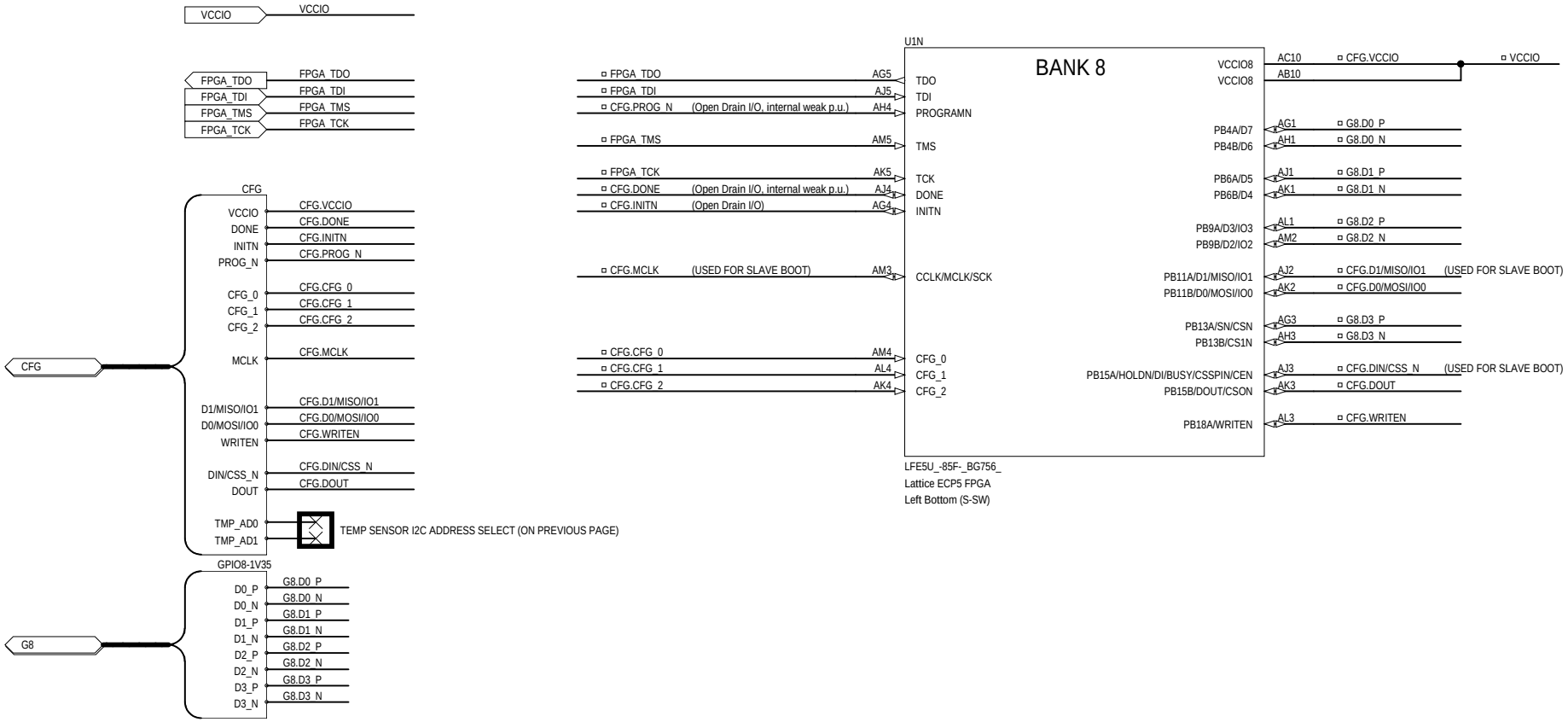
Title: Copper Suicide - FPGA - Bank 7

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 11 of 43	Date: 3/27/2017



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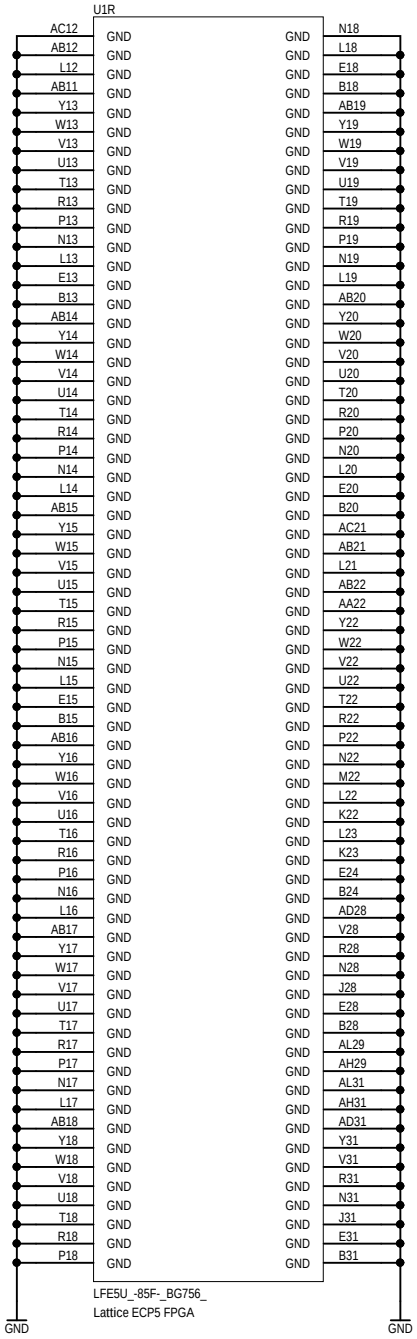
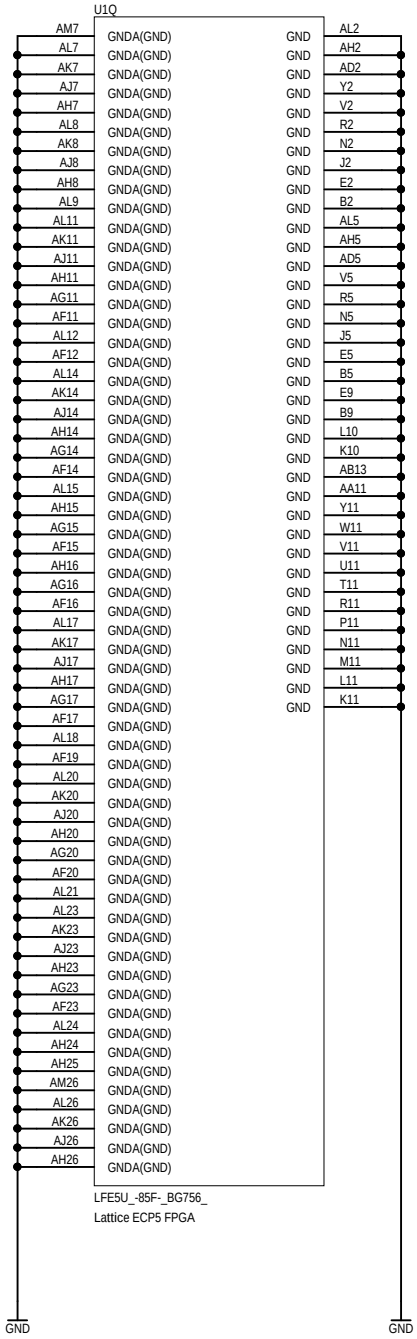
Title: Copper Suicide - FPGA - Bank 8

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 12 of 43	Date: 3/27/2017





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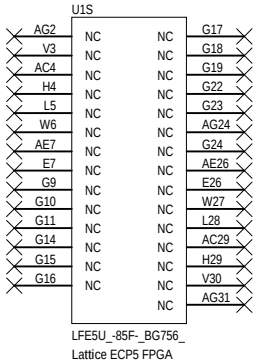
Title: Copper Suicide - FPGA - Ground

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 13 of 43	Date: 3/27/2017



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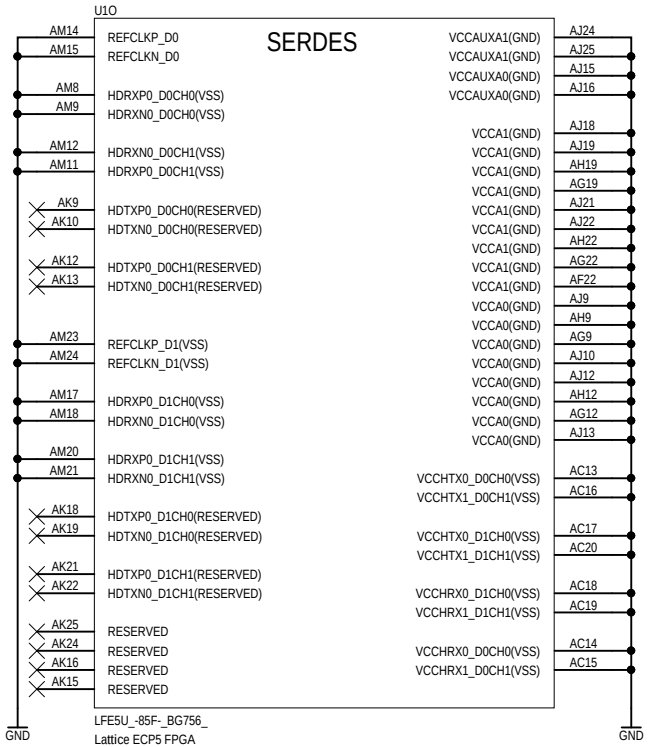
Title: Copper Suicide - FPGA - Misc

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 14 of 43	Date: 3/27/2017



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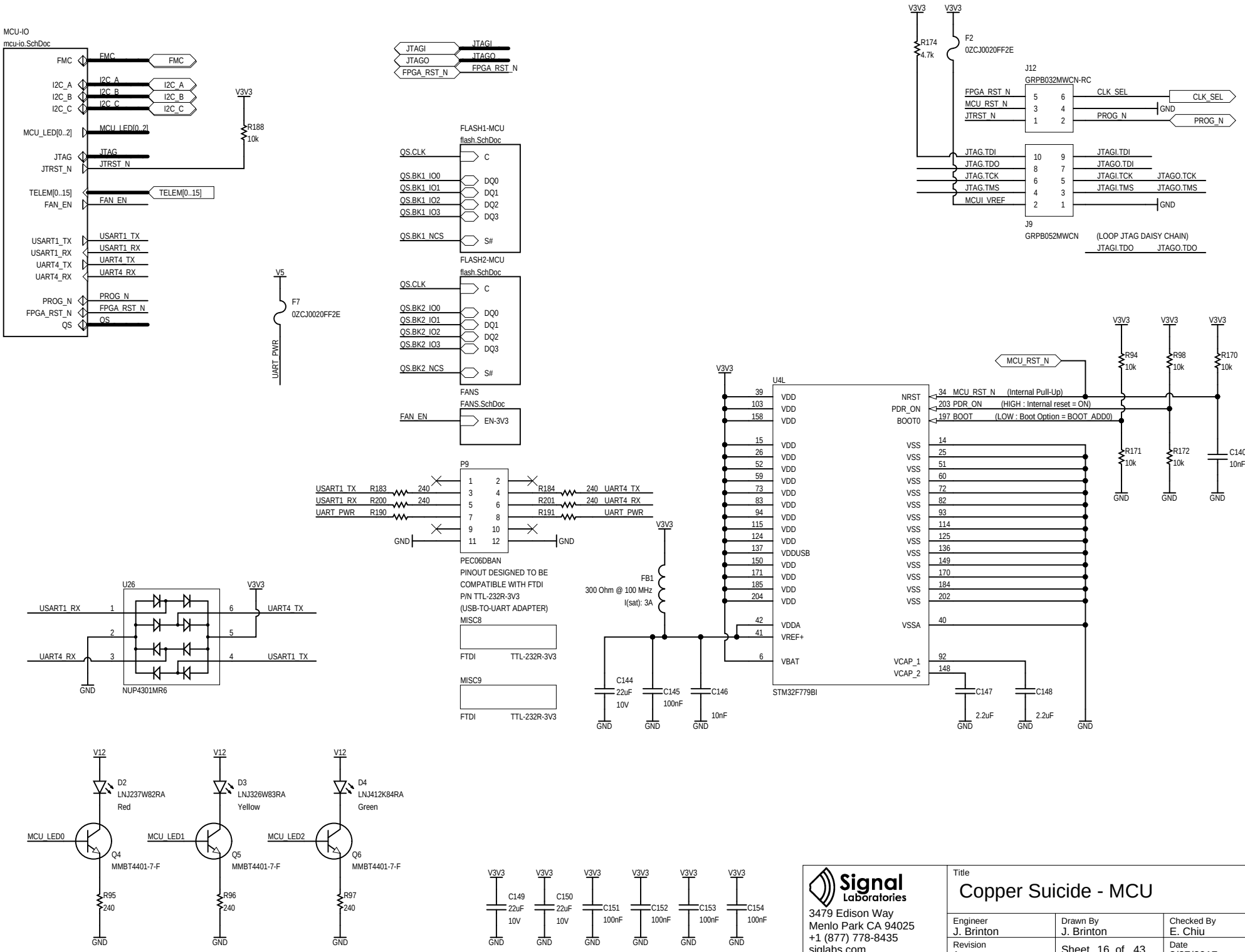
Title: Copper Suicide - FPGA - SERDES

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 15 of 43	Date: 3/27/2017


MCU-IO
mcu-io.SchDoc
FMC
I2C_A
I2C_B
I2C_C
MCU_LED[0..2]
JTAG
JTRST_N
TELEM[0..15]
FAN_EN
USART1_TX
USART1_RX
UART4_TX
UART4_RX
PROG_N
FPGA_RST_N
QS
V3V3
R188
10k
JTAGI
JTAGO
FPGA_RST_N
FLASH1-MCU
flash.SchDoc
QS.CLK
QS.BK1_IO0
QS.BK1_IO1
QS.BK1_IO2
QS.BK1_IO3
QS.BK1_NCS
C
DQ0
DQ1
DQ2
DQ3
S#
FLASH2-MCU
flash.SchDoc
QS.BK2_IO0
QS.BK2_IO1
QS.BK2_IO2
QS.BK2_IO3
QS.BK2_NCS
FANS
FANS.SchDoc
FAN_EN
EN-3V3
V5
F7
0ZCJ0020FF2E
UART_PWR
R174
4.7k
F2
0ZCJ0020FF2E
J12
GRPB032MWCN-RC
CLK_SEL
GND
PROG_N
JTAG.TDI
JTAG.TDO
JTAG.TCK
JTAG.TMS
MCUI_VREF
JTAGI.TDI
JTAGO.TDI
JTAGI.TCK
JTAGO.TCK
JTAGI.TMS
JTAGO.TMS
J9
GRPB052MWCN
(LOOP JTAG DAISY CHAIN)
JTAGI.TDO
JTAGO.TDO
P9
USART1_TX
USART1_RX
UART_PWR
R183
R200
R190
R184
R201
R191
240
UART4_TX
UART4_RX
PEC06DBAN
PINOUT DESIGNED TO BE
COMPATIBLE WITH FTDI
P/N TTL-232R-3V3
(USB-TO-UART ADAPTER)
MISC8
FTDI
TTL-232R-3V3
MISC9
U26
NUP4301MR6
FB1
300 Ohm @ 100 MHz
I(sat): 3A
U4L
STM32F779BI
VDD
VDDUSB
VDDA
VREF+
VBAT
VSS
VSSA
VCAP_1
VCAP_2
NRST
PDR_ON
BOOT0
MCU_RST_N
(Internal Pull-Up)
(HIGH : Internal reset = ON)
(LOW : Boot Option = BOOT_ADD0)
R94
R98
R170
R171
R172
C140
10nF
C144
22uF
10V
C145
100nF
C146
C147
2.2uF
C148
D2
LNJ237W82RA
Red
D3
LNJ326W83RA
Yellow
D4
LNJ412K84RA
Green
MCU_LED0
MCU_LED1
MCU_LED2
Q4
Q5
Q6
MMBT4401-7-F
R95
R96
R97
C149
22uF
C150
22uF
C151
100nF
C152
100nF
C153
100nF
C154
100nF
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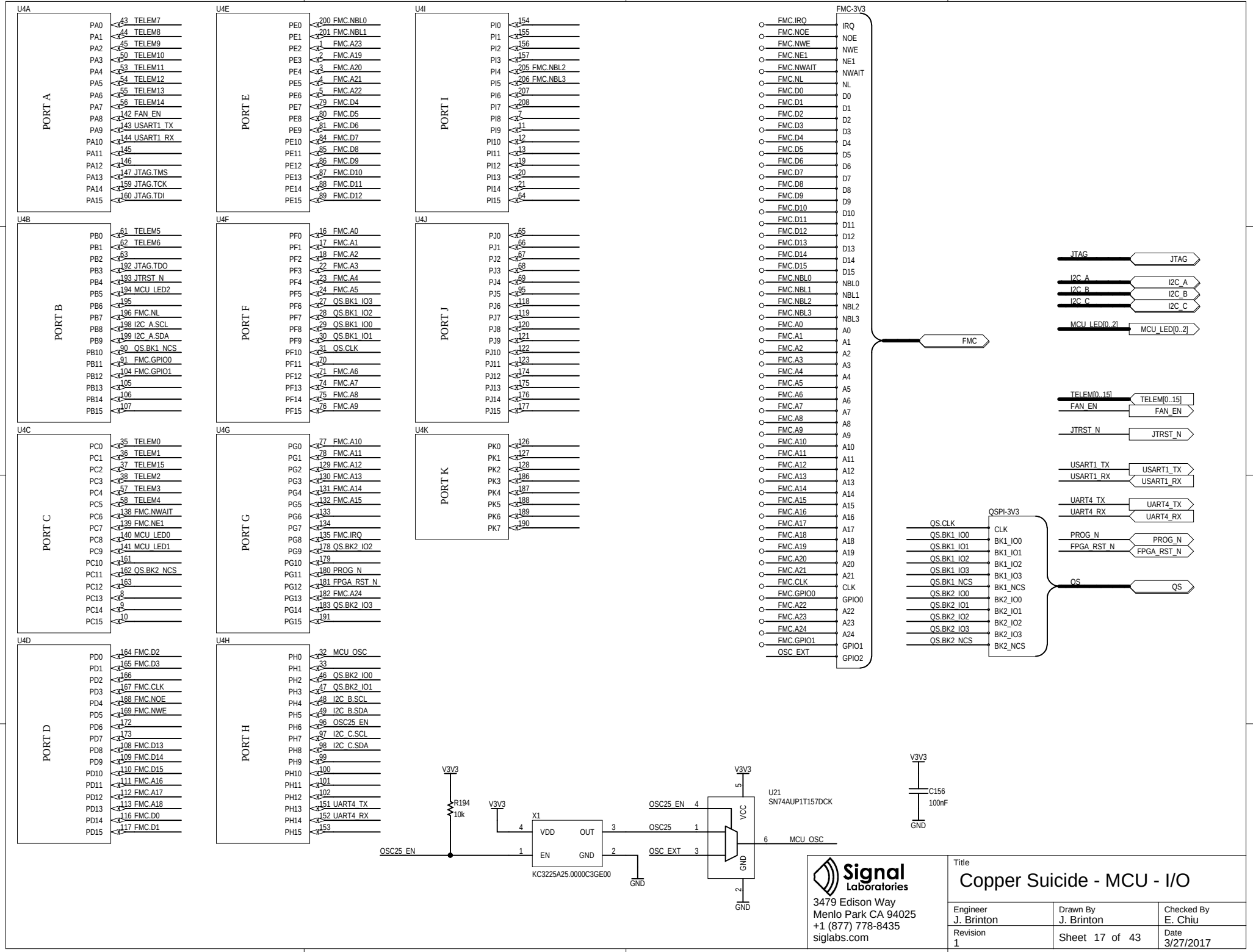
Title
Copper Suicide - MCU
Engineer
J. Brinton
Drawn By
J. Brinton
Checked By
E. Chiu
Revision
1
Sheet 16 of 43
Date
3/27/2017



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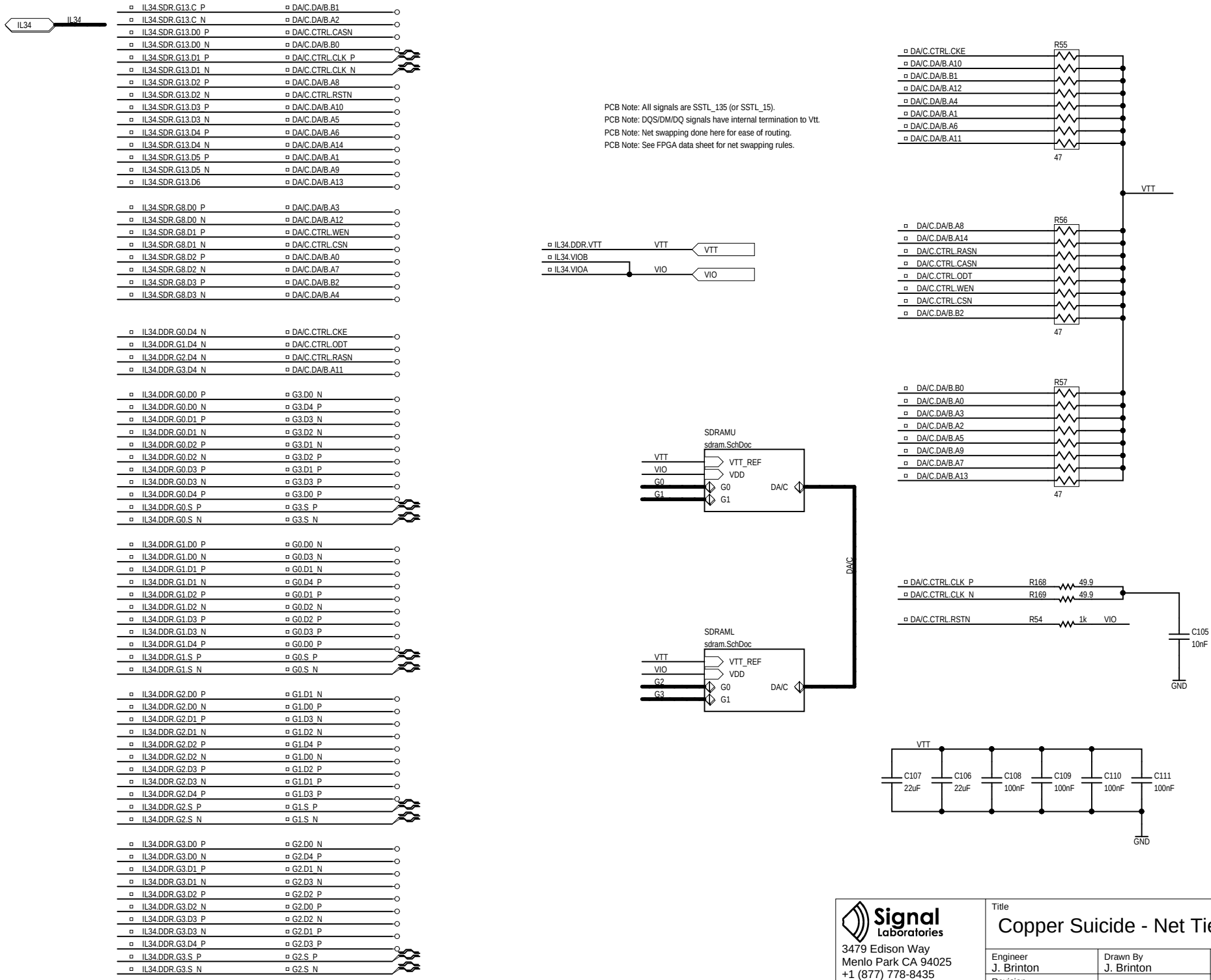
Title
Copper Suicide - MCU - I/O

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 17 of 43	Date: 3/27/2017



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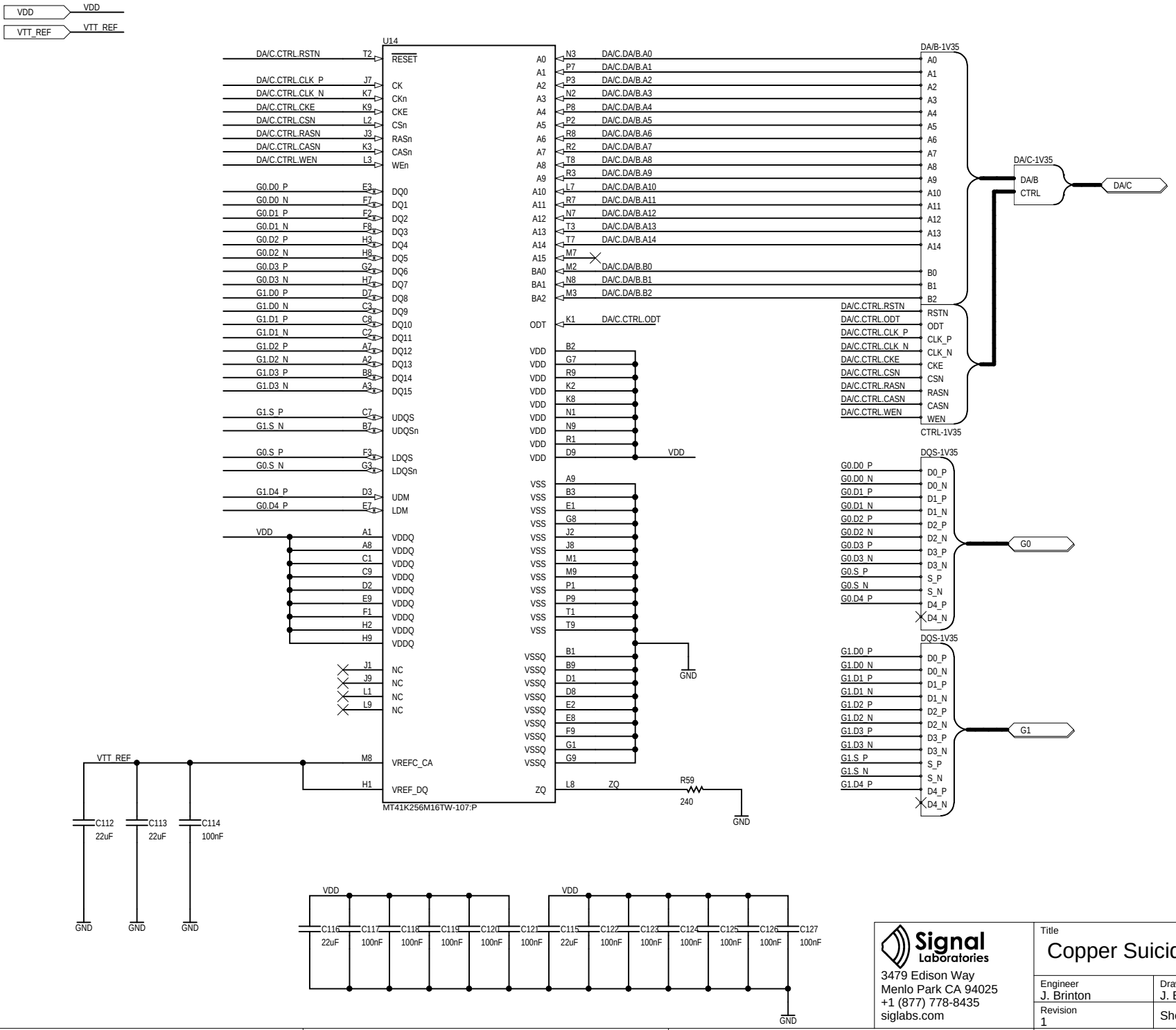
Title: Copper Suicide - Net Tie SDRAM

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 18 of 43	Date: 3/27/2017



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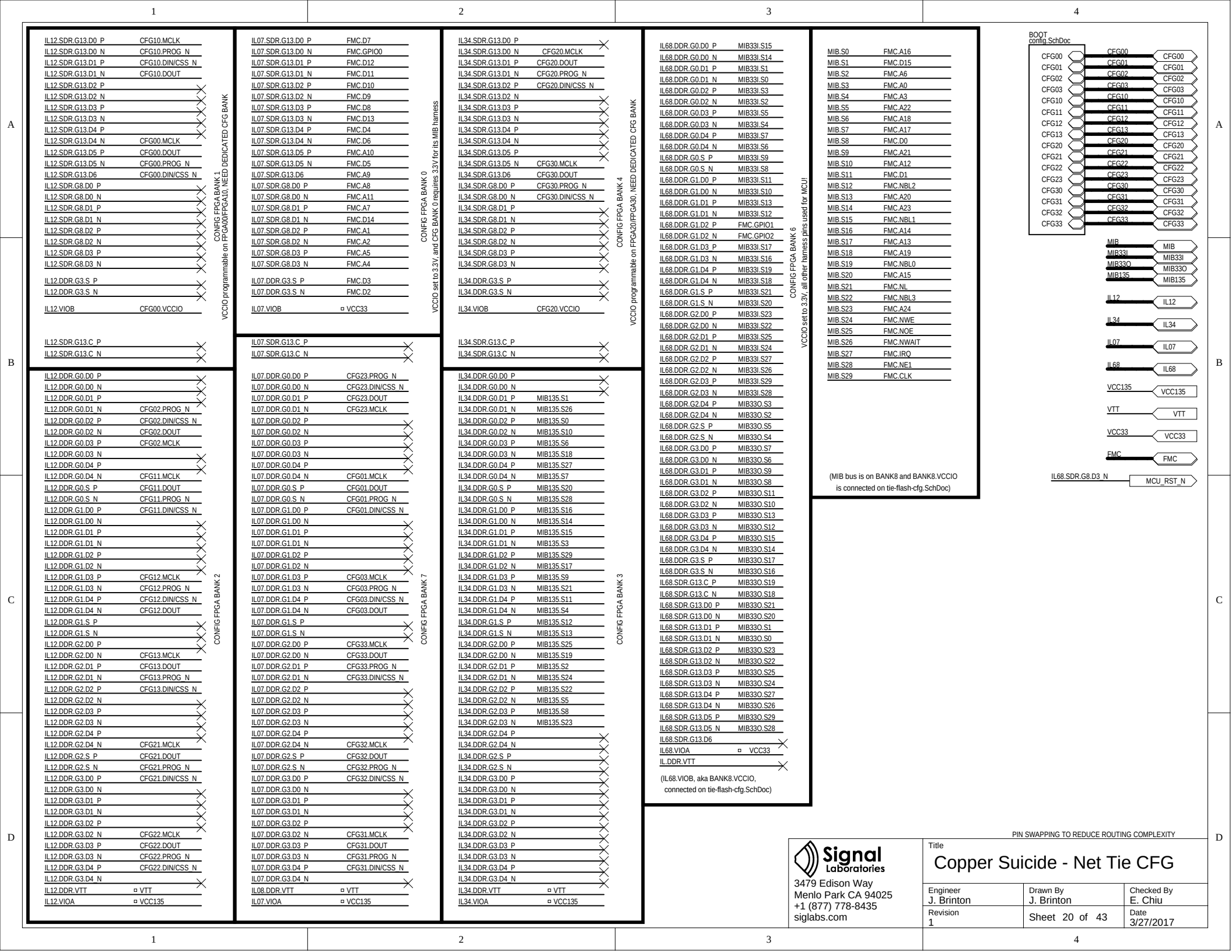
Title: Copper Suicide - SDRAM

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 19 of 43	Date: 3/27/2017


IL12.SDR.G13.D0_P CFG10.MCLK
IL12.SDR.G13.D0_N CFG10.PROG_N
IL12.SDR.G13.D1_P CFG10.DIN/CSS_N
IL12.SDR.G13.D1_N CFG10.DOUT
IL12.SDR.G13.D2_P
IL12.SDR.G13.D2_N
IL12.SDR.G13.D3_P
IL12.SDR.G13.D3_N
IL12.SDR.G13.D4_P
IL12.SDR.G13.D4_N CFG00.MCLK
IL12.SDR.G13.D5_P CFG00.DOUT
IL12.SDR.G13.D5_N CFG00.PROG_N
IL12.SDR.G13.D6 CFG00.DIN/CSS_N
IL12.SDR.G8.D0_P
IL12.SDR.G8.D0_N
IL12.SDR.G8.D1_P
IL12.SDR.G8.D1_N
IL12.SDR.G8.D2_P
IL12.SDR.G8.D2_N
IL12.SDR.G8.D3_P
IL12.SDR.G8.D3_N
IL12.DDR.G3.S_P
IL12.DDR.G3.S_N
IL12.VIOB CFG00.VCCIO
CONFIG FPGA BANK 1
VCCIO programmable on FPGA00/FPGA10, NEED DEDICATED CFG BANK
IL12.SDR.G13.C_P
IL12.SDR.G13.C_N
IL07.SDR.G13.D0_P FMC.D7
IL07.SDR.G13.D0_N FMC.GPIO0
IL07.SDR.G13.D1_P FMC.D12
IL07.SDR.G13.D1_N FMC.D11
IL07.SDR.G13.D2_P FMC.D10
IL07.SDR.G13.D2_N FMC.D9
IL07.SDR.G13.D3_P FMC.D8
IL07.SDR.G13.D3_N FMC.D13
IL07.SDR.G13.D4_P FMC.D4
IL07.SDR.G13.D4_N FMC.D6
IL07.SDR.G13.D5_P FMC.A10
IL07.SDR.G13.D5_N FMC.D5
IL07.SDR.G13.D6 FMC.A9
IL07.SDR.G8.D0_P FMC.A8
IL07.SDR.G8.D0_N FMC.A11
IL07.SDR.G8.D1_P FMC.A7
IL07.SDR.G8.D1_N FMC.D14
IL07.SDR.G8.D2_P FMC.A1
IL07.SDR.G8.D2_N FMC.A2
IL07.SDR.G8.D3_P FMC.A5
IL07.SDR.G8.D3_N FMC.A4
IL07.DDR.G3.S_P FMC.D3
IL07.DDR.G3.S_N FMC.D2
IL07.VIOB VCC33
CONFIG FPGA BANK 0
VCCIO set to 3.3V, and CFG BANK 0 requires 3.3V for its MIB harness
IL07.SDR.G13.C_P
IL07.SDR.G13.C_N
IL34.SDR.G13.D0_P
IL34.SDR.G13.D0_N CFG20.MCLK
IL34.SDR.G13.D1_P CFG20.DOUT
IL34.SDR.G13.D1_N CFG20.PROG_N
IL34.SDR.G13.D2_P CFG20.DIN/CSS_N
IL34.SDR.G13.D2_N
IL34.SDR.G13.D3_P
IL34.SDR.G13.D3_N
IL34.SDR.G13.D4_P
IL34.SDR.G13.D4_N
IL34.SDR.G13.D5_P
IL34.SDR.G13.D5_N CFG30.MCLK
IL34.SDR.G13.D6 CFG30.DOUT
IL34.SDR.G8.D0_P CFG30.PROG_N
IL34.SDR.G8.D0_N CFG30.DIN/CSS_N
IL34.SDR.G8.D1_P
IL34.SDR.G8.D1_N
IL34.SDR.G8.D2_P
IL34.SDR.G8.D2_N
IL34.SDR.G8.D3_P
IL34.SDR.G8.D3_N
IL34.DDR.G3.S_P
IL34.DDR.G3.S_N
IL34.VIOB CFG20.VCCIO
CONFIG FPGA BANK 4
VCCIO programmable on FPGA20/FPGA30, NEED DEDICATED CFG BANK
IL34.SDR.G13.C_P
IL34.SDR.G13.C_N
IL68.DDR.G0.D0_P MIB33I.S15
IL68.DDR.G0.D0_N MIB33I.S14
IL68.DDR.G0.D1_P MIB33I.S1
IL68.DDR.G0.D1_N MIB33I.S0
IL68.DDR.G0.D2_P MIB33I.S3
IL68.DDR.G0.D2_N MIB33I.S2
IL68.DDR.G0.D3_P MIB33I.S5
IL68.DDR.G0.D3_N MIB33I.S4
IL68.DDR.G0.D4_P MIB33I.S7
IL68.DDR.G0.D4_N MIB33I.S6
IL68.DDR.G0.S_P MIB33I.S9
IL68.DDR.G0.S_N MIB33I.S8
IL68.DDR.G1.D0_P MIB33I.S11
IL68.DDR.G1.D0_N MIB33I.S10
IL68.DDR.G1.D1_P MIB33I.S13
IL68.DDR.G1.D1_N MIB33I.S12
IL68.DDR.G1.D2_P FMC.GPIO1
IL68.DDR.G1.D2_N FMC.GPIO2
IL68.DDR.G1.D3_P MIB33I.S17
IL68.DDR.G1.D3_N MIB33I.S16
IL68.DDR.G1.D4_P MIB33I.S19
IL68.DDR.G1.D4_N MIB33I.S18
IL68.DDR.G1.S_P MIB33I.S21
IL68.DDR.G1.S_N MIB33I.S20
IL68.DDR.G2.D0_P MIB33I.S23
IL68.DDR.G2.D0_N MIB33I.S22
IL68.DDR.G2.D1_P MIB33I.S25
IL68.DDR.G2.D1_N MIB33I.S24
IL68.DDR.G2.D2_P MIB33I.S27
IL68.DDR.G2.D2_N MIB33I.S26
IL68.DDR.G2.D3_P MIB33I.S29
IL68.DDR.G2.D3_N MIB33I.S28
IL68.DDR.G2.D4_P MIB33O.S3
IL68.DDR.G2.D4_N MIB33O.S2
IL68.DDR.G2.S_P MIB33O.S5
IL68.DDR.G2.S_N MIB33O.S4
IL68.DDR.G3.D0_P MIB33O.S7
IL68.DDR.G3.D0_N MIB33O.S6
IL68.DDR.G3.D1_P MIB33O.S9
IL68.DDR.G3.D1_N MIB33O.S8
IL68.DDR.G3.D2_P MIB33O.S11
IL68.DDR.G3.D2_N MIB33O.S10
IL68.DDR.G3.D3_P MIB33O.S13
IL68.DDR.G3.D3_N MIB33O.S12
IL68.DDR.G3.D4_P MIB33O.S15
IL68.DDR.G3.D4_N MIB33O.S14
IL68.DDR.G3.S_P MIB33O.S17
IL68.DDR.G3.S_N MIB33O.S16
IL68.SDR.G13.C_P MIB33O.S19
IL68.SDR.G13.C_N MIB33O.S18
IL68.SDR.G13.D0_P MIB33O.S21
IL68.SDR.G13.D0_N MIB33O.S20
IL68.SDR.G13.D1_P MIB33O.S1
IL68.SDR.G13.D1_N MIB33O.S0
IL68.SDR.G13.D2_P MIB33O.S23
IL68.SDR.G13.D2_N MIB33O.S22
IL68.SDR.G13.D3_P MIB33O.S25
IL68.SDR.G13.D3_N MIB33O.S24
IL68.SDR.G13.D4_P MIB33O.S27
IL68.SDR.G13.D4_N MIB33O.S26
IL68.SDR.G13.D5_P MIB33O.S29
IL68.SDR.G13.D5_N MIB33O.S28
IL68.SDR.G13.D6
IL68.VIOA VCC33
IL.DDR.VTT
(IL68.VIOB, aka BANK8.VCCIO, connected on tie-flash-cfg.SchDoc)
CONFIG FPGA BANK 6
VCCIO set to 3.3V, all other harness pins used for MCU!
MIB.S0 FMC.A16
MIB.S1 FMC.D15
MIB.S2 FMC.A6
MIB.S3 FMC.A0
MIB.S4 FMC.A3
MIB.S5 FMC.A22
MIB.S6 FMC.A18
MIB.S7 FMC.A17
MIB.S8 FMC.D0
MIB.S9 FMC.A21
MIB.S10 FMC.A12
MIB.S11 FMC.D1
MIB.S12 FMC.NBL2
MIB.S13 FMC.A20
MIB.S14 FMC.A23
MIB.S15 FMC.NBL1
MIB.S16 FMC.A14
MIB.S17 FMC.A13
MIB.S18 FMC.A19
MIB.S19 FMC.NBL0
MIB.S20 FMC.A15
MIB.S21 FMC.NL
MIB.S22 FMC.NBL3
MIB.S23 FMC.A24
MIB.S24 FMC.NWE
MIB.S25 FMC.NOE
MIB.S26 FMC.NWAIT
MIB.S27 FMC.IRQ
MIB.S28 FMC.NE1
MIB.S29 FMC.CLK
(MIB bus is on BANK8 and BANK8.VCCIO is connected on tie-flash-cfg.SchDoc)
BOOT config.SchDoc
CFG00 CFG01 CFG02 CFG03 CFG10 CFG11 CFG12 CFG13 CFG20 CFG21 CFG22 CFG23 CFG30 CFG31 CFG32 CFG33
MIB MIB33I MIB33O MIB135
IL12 IL34 IL07 IL68
VCC135 VTT VCC33 FMC
IL68.SDR.G8.D3_N MCU_RST_N
IL12.DDR.G0.D0_P
IL12.DDR.G0.D0_N
IL12.DDR.G0.D1_P
IL12.DDR.G0.D1_N CFG02.PROG_N
IL12.DDR.G0.D2_P CFG02.DIN/CSS_N
IL12.DDR.G0.D2_N CFG02.DOUT
IL12.DDR.G0.D3_P CFG02.MCLK
IL12.DDR.G0.D3_N
IL12.DDR.G0.D4_P
IL12.DDR.G0.D4_N CFG11.MCLK
IL12.DDR.G0.S_P CFG11.DOUT
IL12.DDR.G0.S_N CFG11.PROG_N
IL12.DDR.G1.D0_P CFG11.DIN/CSS_N
IL12.DDR.G1.D0_N
IL12.DDR.G1.D1_P
IL12.DDR.G1.D1_N
IL12.DDR.G1.D2_P
IL12.DDR.G1.D2_N
IL12.DDR.G1.D3_P CFG12.MCLK
IL12.DDR.G1.D3_N CFG12.PROG_N
IL12.DDR.G1.D4_P CFG12.DIN/CSS_N
IL12.DDR.G1.D4_N CFG12.DOUT
IL12.DDR.G1.S_P
IL12.DDR.G1.S_N
IL12.DDR.G2.D0_P
IL12.DDR.G2.D0_N CFG13.MCLK
IL12.DDR.G2.D1_P CFG13.DOUT
IL12.DDR.G2.D1_N CFG13.PROG_N
IL12.DDR.G2.D2_P CFG13.DIN/CSS_N
IL12.DDR.G2.D2_N
IL12.DDR.G2.D3_P
IL12.DDR.G2.D3_N
IL12.DDR.G2.D4_P
IL12.DDR.G2.D4_N CFG21.MCLK
IL12.DDR.G2.S_P CFG21.DOUT
IL12.DDR.G2.S_N CFG21.PROG_N
IL12.DDR.G3.D0_P CFG21.DIN/CSS_N
IL12.DDR.G3.D0_N
IL12.DDR.G3.D1_P
IL12.DDR.G3.D1_N
IL12.DDR.G3.D2_P
IL12.DDR.G3.D2_N CFG22.MCLK
IL12.DDR.G3.D3_P CFG22.DOUT
IL12.DDR.G3.D3_N CFG22.PROG_N
IL12.DDR.G3.D4_P CFG22.DIN/CSS_N
IL12.DDR.G3.D4_N
IL12.DDR.VTT VTT
IL12.VIOA VCC135
CONFIG FPGA BANK 2
IL07.DDR.G0.D0_P CFG23.PROG_N
IL07.DDR.G0.D0_N CFG23.DIN/CSS_N
IL07.DDR.G0.D1_P CFG23.DOUT
IL07.DDR.G0.D1_N CFG23.MCLK
IL07.DDR.G0.D2_P
IL07.DDR.G0.D2_N
IL07.DDR.G0.D3_P
IL07.DDR.G0.D3_N
IL07.DDR.G0.D4_P
IL07.DDR.G0.D4_N CFG01.MCLK
IL07.DDR.G0.S_P CFG01.DOUT
IL07.DDR.G0.S_N CFG01.PROG_N
IL07.DDR.G1.D0_P CFG01.DIN/CSS_N
IL07.DDR.G1.D0_N
IL07.DDR.G1.D1_P
IL07.DDR.G1.D1_N
IL07.DDR.G1.D2_P
IL07.DDR.G1.D2_N
IL07.DDR.G1.D3_P CFG03.MCLK
IL07.DDR.G1.D3_N CFG03.PROG_N
IL07.DDR.G1.D4_P CFG03.DIN/CSS_N
IL07.DDR.G1.D4_N CFG03.DOUT
IL07.DDR.G1.S_P
IL07.DDR.G1.S_N
IL07.DDR.G2.D0_P CFG33.MCLK
IL07.DDR.G2.D0_N CFG33.DOUT
IL07.DDR.G2.D1_P CFG33.PROG_N
IL07.DDR.G2.D1_N CFG33.DIN/CSS_N
IL07.DDR.G2.D2_P
IL07.DDR.G2.D2_N
IL07.DDR.G2.D3_P
IL07.DDR.G2.D3_N
IL07.DDR.G2.D4_P
IL07.DDR.G2.D4_N CFG32.MCLK
IL07.DDR.G2.S_P CFG32.DOUT
IL07.DDR.G2.S_N CFG32.PROG_N
IL07.DDR.G3.D0_P CFG32.DIN/CSS_N
IL07.DDR.G3.D0_N
IL07.DDR.G3.D1_P
IL07.DDR.G3.D1_N
IL07.DDR.G3.D2_P
IL07.DDR.G3.D2_N CFG31.MCLK
IL07.DDR.G3.D3_P CFG31.DOUT
IL07.DDR.G3.D3_N CFG31.PROG_N
IL07.DDR.G3.D4_P CFG31.DIN/CSS_N
IL07.DDR.G3.D4_N
IL08.DDR.VTT VTT
IL07.VIOA VCC135
CONFIG FPGA BANK 7
IL34.DDR.G0.D0_P
IL34.DDR.G0.D0_N
IL34.DDR.G0.D1_P MIB135.S1
IL34.DDR.G0.D1_N MIB135.S26
IL34.DDR.G0.D2_P MIB135.S0
IL34.DDR.G0.D2_N MIB135.S10
IL34.DDR.G0.D3_P MIB135.S6
IL34.DDR.G0.D3_N MIB135.S18
IL34.DDR.G0.D4_P MIB135.S27
IL34.DDR.G0.D4_N MIB135.S7
IL34.DDR.G0.S_P MIB135.S20
IL34.DDR.G0.S_N MIB135.S28
IL34.DDR.G1.D0_P MIB135.S16
IL34.DDR.G1.D0_N MIB135.S14
IL34.DDR.G1.D1_P MIB135.S15
IL34.DDR.G1.D1_N MIB135.S3
IL34.DDR.G1.D2_P MIB135.S29
IL34.DDR.G1.D2_N MIB135.S17
IL34.DDR.G1.D3_P MIB135.S9
IL34.DDR.G1.D3_N MIB135.S21
IL34.DDR.G1.D4_P MIB135.S11
IL34.DDR.G1.D4_N MIB135.S4
IL34.DDR.G1.S_P MIB135.S12
IL34.DDR.G1.S_N MIB135.S13
IL34.DDR.G2.D0_P MIB135.S25
IL34.DDR.G2.D0_N MIB135.S19
IL34.DDR.G2.D1_P MIB135.S2
IL34.DDR.G2.D1_N MIB135.S24
IL34.DDR.G2.D2_P MIB135.S22
IL34.DDR.G2.D2_N MIB135.S5
IL34.DDR.G2.D3_P MIB135.S8
IL34.DDR.G2.D3_N MIB135.S23
IL34.DDR.G2.D4_P
IL34.DDR.G2.D4_N
IL34.DDR.G2.S_P
IL34.DDR.G2.S_N
IL34.DDR.G3.D0_P
IL34.DDR.G3.D0_N
IL34.DDR.G3.D1_P
IL34.DDR.G3.D1_N
IL34.DDR.G3.D2_P
IL34.DDR.G3.D2_N
IL34.DDR.G3.D3_P
IL34.DDR.G3.D3_N
IL34.DDR.G3.D4_P
IL34.DDR.G3.D4_N
IL34.DDR.VTT VTT
IL34.VIOA VCC135
CONFIG FPGA BANK 3
PIN SWAPPING TO REDUCE ROUTING COMPLEXITY
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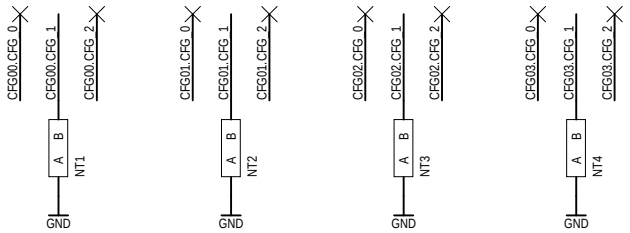
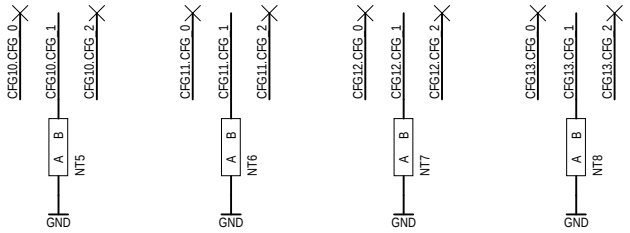
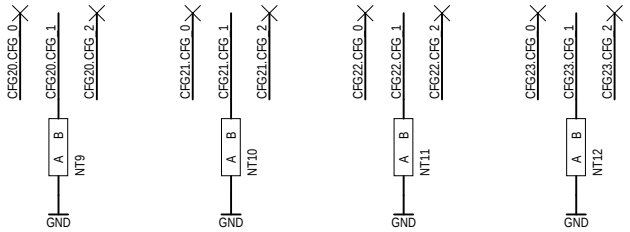
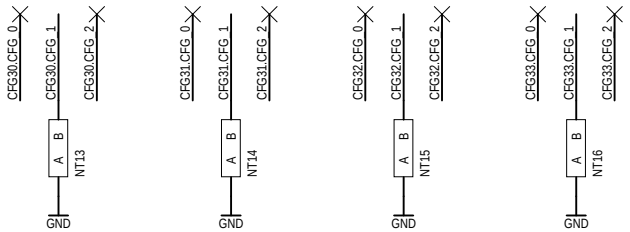
siglabs.com
Title
Copper Suicide - Net Tie CFG
Engineer J. Brinton
Drawn By J. Brinton
Checked By E. Chiu
Revision 1
Sheet 20 of 43
Date 3/27/2017

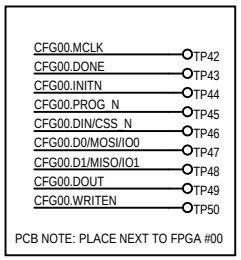




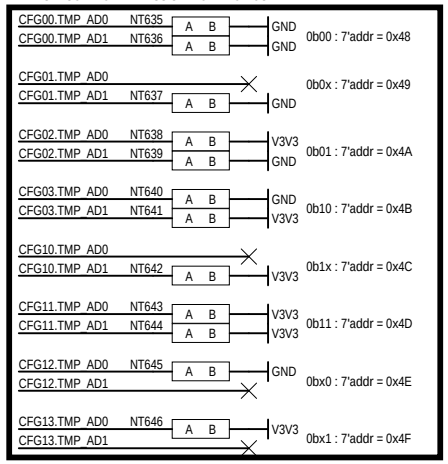




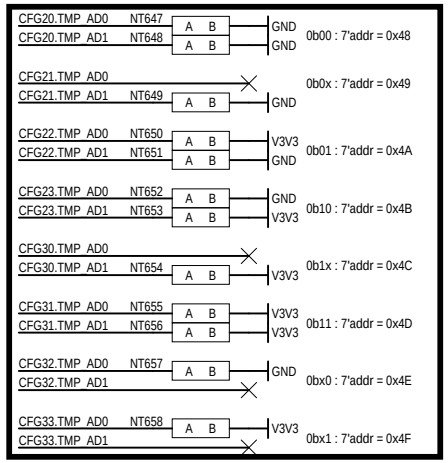
CFG[2:0] = 0b101 (Slave Serial Boot)

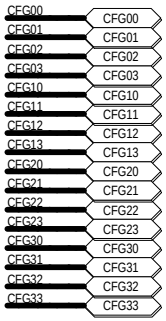


TEMP SENSOR I2C ADDRESS SELECT - I2C BUS A



TEMP SENSOR I2C ADDRESS SELECT - I2C BUS B





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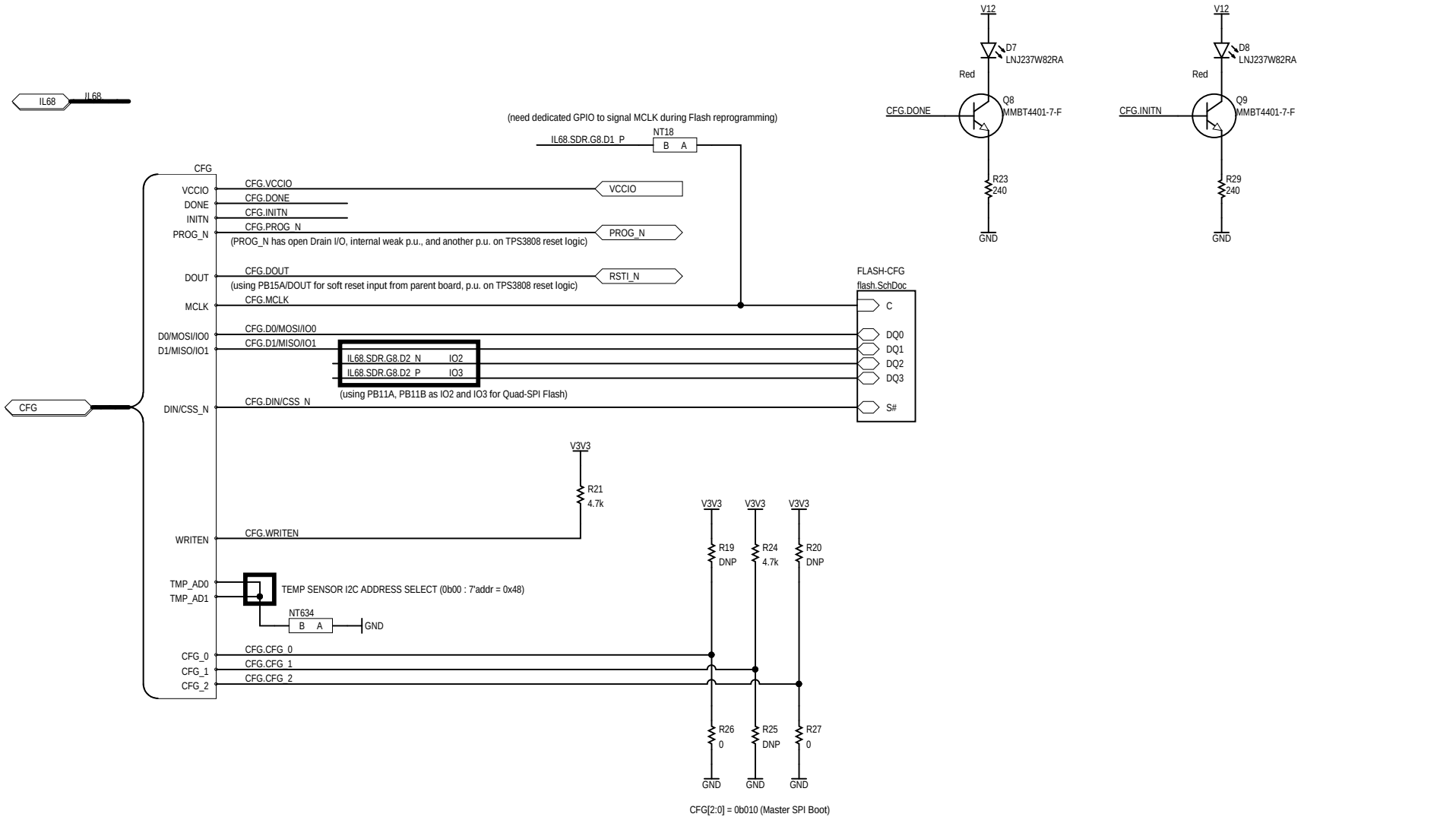
Title
Copper Suicide - Config Options

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision 1	Sheet 21 of 43	Date 3/27/2017



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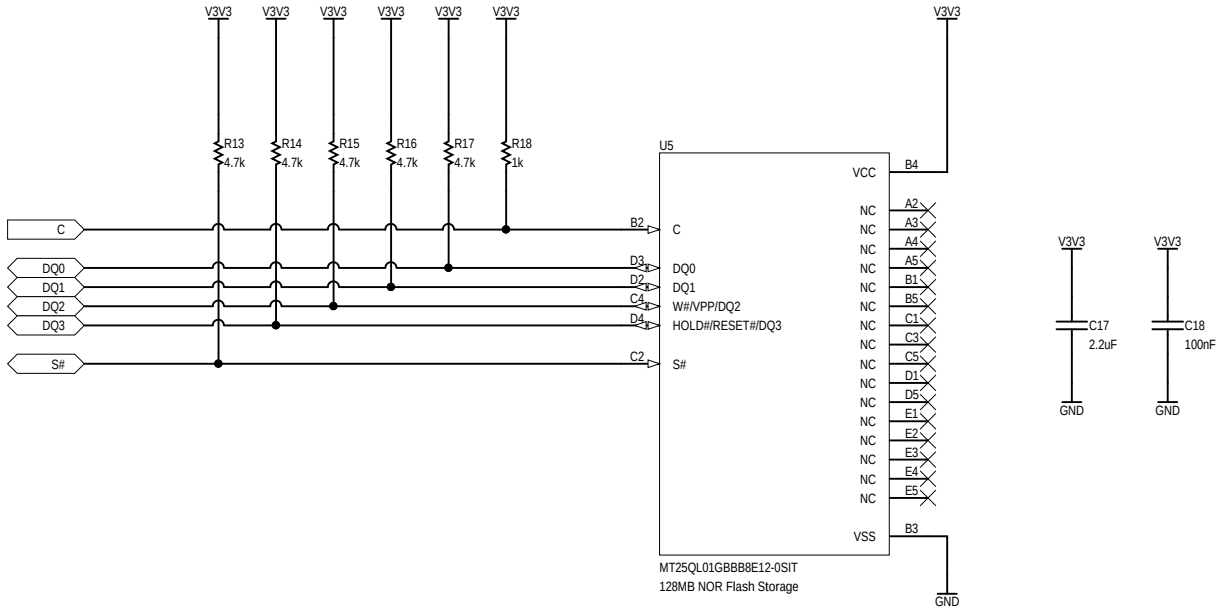
Title
Copper Suicide - Net Tie - Flash

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 22 of 43	Date: 3/27/2017



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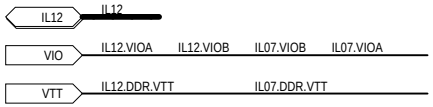
Title: Copper Suicide - Flash

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 23 of 43	Date: 3/27/2017



IL12.SDR.G13.C_P	IL07.SDR.G13.C_P
IL12.SDR.G13.C_N	IL07.SDR.G13.C_N
IL12.SDR.G13.D0_P	IL07.SDR.G8.D2_P
IL12.SDR.G13.D0_N	IL07.SDR.G8.D2_N
IL12.SDR.G13.D1_P	IL07.SDR.G13.D2_P
IL12.SDR.G13.D1_N	IL07.SDR.G13.D2_N
IL12.SDR.G13.D2_P	IL07.SDR.G8.D1_P
IL12.SDR.G13.D2_N	IL07.SDR.G8.D1_N
IL12.SDR.G13.D3_P	IL07.SDR.G13.D4_P
IL12.SDR.G13.D3_N	IL07.SDR.G13.D4_N
IL12.SDR.G13.D4_P	IL07.SDR.G13.D1_P
IL12.SDR.G13.D4_N	IL07.SDR.G13.D1_N
IL12.SDR.G13.D5_P	IL07.SDR.G13.D5_P
IL12.SDR.G13.D5_N	IL07.SDR.G13.D5_N
IL12.SDR.G13.D6	IL07.SDR.G13.D6

IL12.SDR.G8.D0_P	IL07.SDR.G13.D0_P
IL12.SDR.G8.D0_N	IL07.SDR.G13.D0_N
IL12.SDR.G8.D1_P	IL07.SDR.G8.D3_P
IL12.SDR.G8.D1_N	IL07.SDR.G8.D3_N
IL12.SDR.G8.D2_P	IL07.SDR.G8.D0_P
IL12.SDR.G8.D2_N	IL07.SDR.G8.D0_N
IL12.SDR.G8.D3_P	IL07.SDR.G13.D3_P
IL12.SDR.G8.D3_N	IL07.SDR.G13.D3_N

IL12.DDR.G0.D0_P	IL07.DDR.G0.D0_P
IL12.DDR.G0.D0_N	IL07.DDR.G0.D0_N
IL12.DDR.G0.D1_P	IL07.DDR.G0.D1_P
IL12.DDR.G0.D1_N	IL07.DDR.G0.D1_N
IL12.DDR.G0.D2_P	IL07.DDR.G0.D2_P
IL12.DDR.G0.D2_N	IL07.DDR.G0.D2_N
IL12.DDR.G0.D3_P	IL07.DDR.G0.D3_P
IL12.DDR.G0.D3_N	IL07.DDR.G0.D3_N
IL12.DDR.G0.D4_P	IL07.DDR.G0.D4_P
IL12.DDR.G0.D4_N	IL07.DDR.G0.D4_N
IL12.DDR.G0.S_P	IL07.DDR.G0.S_P
IL12.DDR.G0.S_N	IL07.DDR.G0.S_N
IL12.DDR.G1.D0_P	IL07.DDR.G1.D0_P
IL12.DDR.G1.D0_N	IL07.DDR.G1.D0_N
IL12.DDR.G1.D1_P	IL07.DDR.G1.D1_P
IL12.DDR.G1.D1_N	IL07.DDR.G1.D1_N
IL12.DDR.G1.D2_P	IL07.DDR.G1.D2_P
IL12.DDR.G1.D2_N	IL07.DDR.G1.D2_N
IL12.DDR.G1.D3_P	IL07.DDR.G1.D3_P
IL12.DDR.G1.D3_N	IL07.DDR.G1.D3_N
IL12.DDR.G1.D4_P	IL07.DDR.G1.D4_P
IL12.DDR.G1.D4_N	IL07.DDR.G1.D4_N
IL12.DDR.G1.S_P	IL07.DDR.G1.S_P
IL12.DDR.G1.S_N	IL07.DDR.G1.S_N
IL12.DDR.G2.D0_P	IL07.DDR.G2.D0_P
IL12.DDR.G2.D0_N	IL07.DDR.G2.D0_N
IL12.DDR.G2.D1_P	IL07.DDR.G2.D1_P
IL12.DDR.G2.D1_N	IL07.DDR.G2.D1_N
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IL12.DDR.G2.S_N	IL07.DDR.G2.S_N
IL12.DDR.G3.D0_P	IL07.DDR.G3.D0_P
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IL12.DDR.G3.D4_P	IL07.DDR.G3.D4_P
IL12.DDR.G3.D4_N	IL07.DDR.G3.D4_N
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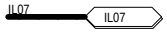

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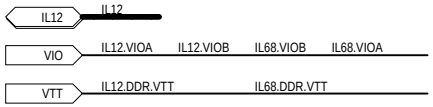
Title: Copper Suicide - Net Tie 12:07

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 24 of 43	Date: 3/27/2017



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IL12.SDR.G13.D1_P	IL68.SDR.G13.D5_P
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IL12.SDR.G13.D4_N	IL68.SDR.G13.D0_N
IL12.SDR.G13.D5_P	IL68.SDR.G13.D2_P
IL12.SDR.G13.D5_N	IL68.SDR.G13.D2_N
IL12.SDR.G13.D6	IL68.SDR.G13.D6

IL12.SDR.G8.D0_P	IL68.SDR.G8.D0_P
IL12.SDR.G8.D0_N	IL68.SDR.G8.D0_N
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IL12.SDR.G8.D1_N	IL68.SDR.G8.D2_N
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IL12.DDR.G1.D1_P	IL68.DDR.G1.D2_P
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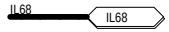

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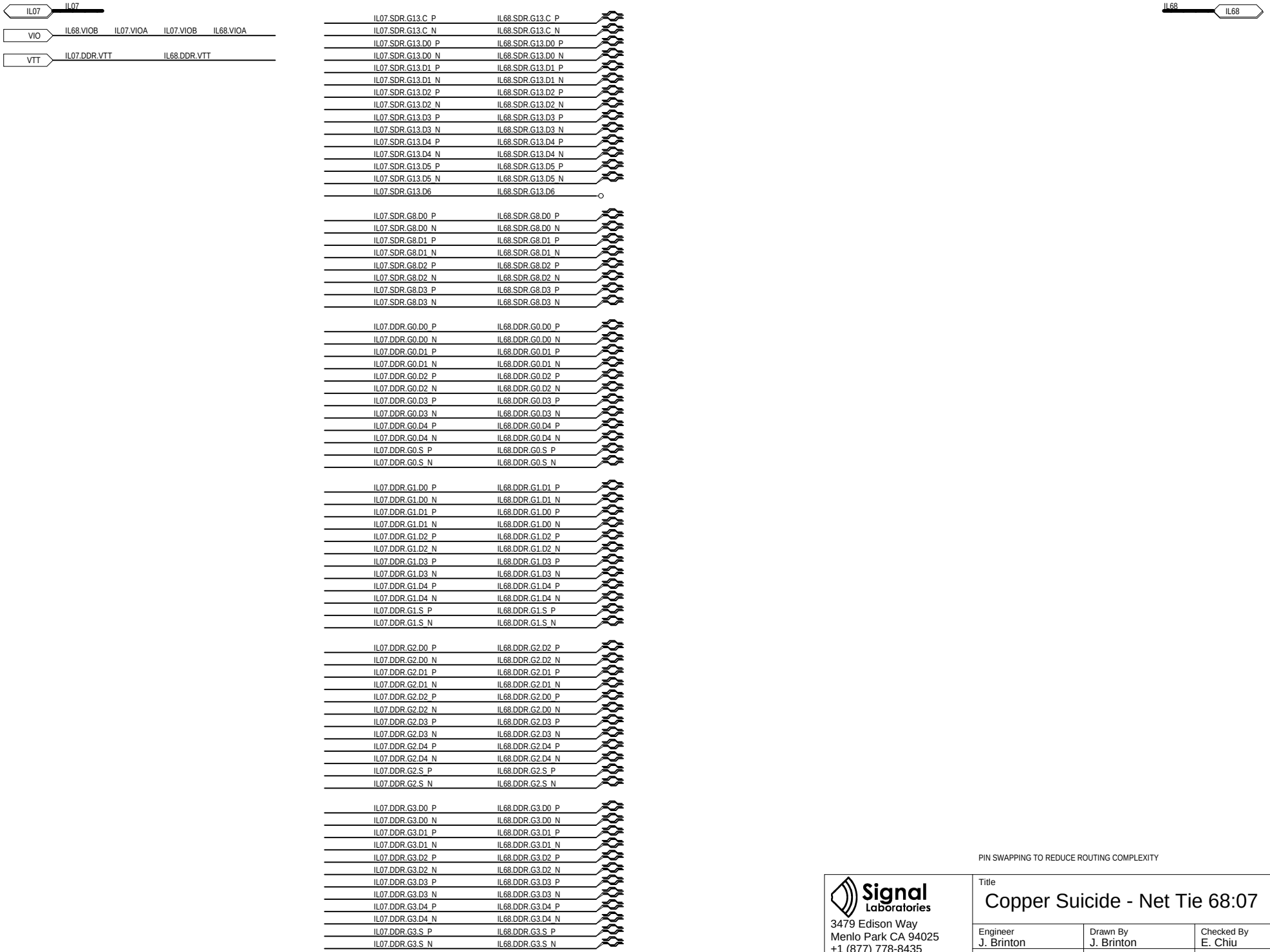
Title: Copper Suicide - Net Tie 12:68

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 25 of 43	Date: 3/27/2017



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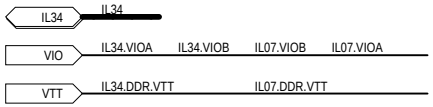
Title: Copper Suicide - Net Tie 68:07

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 26 of 43	Date: 3/27/2017



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IL34.SDR.G13.D0_N	IL07.SDR.G13.D1_N
IL34.SDR.G13.D1_P	IL07.SDR.G13.D0_P
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IL34.SDR.G13.D2_P	IL07.SDR.G13.D3_P
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IL34.DDR.G0.D4_P	IL07.DDR.G0.D4_P
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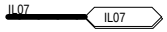

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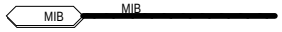
Title: Copper Suicide - Net Tie 34:07

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 27 of 43	Date: 3/27/2017



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MIB.S0	IMIB.S22
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MIB.S7	IMIB.S2
MIB.S6	IMIB.S19
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MIB.S16	IMIB.S3
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MIB.S22	IMIB.S0
MIB.S25	IMIB.S24
MIB.S24	IMIB.S25
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MIB.S29	IMIB.S11
MIB.S28	IMIB.S21

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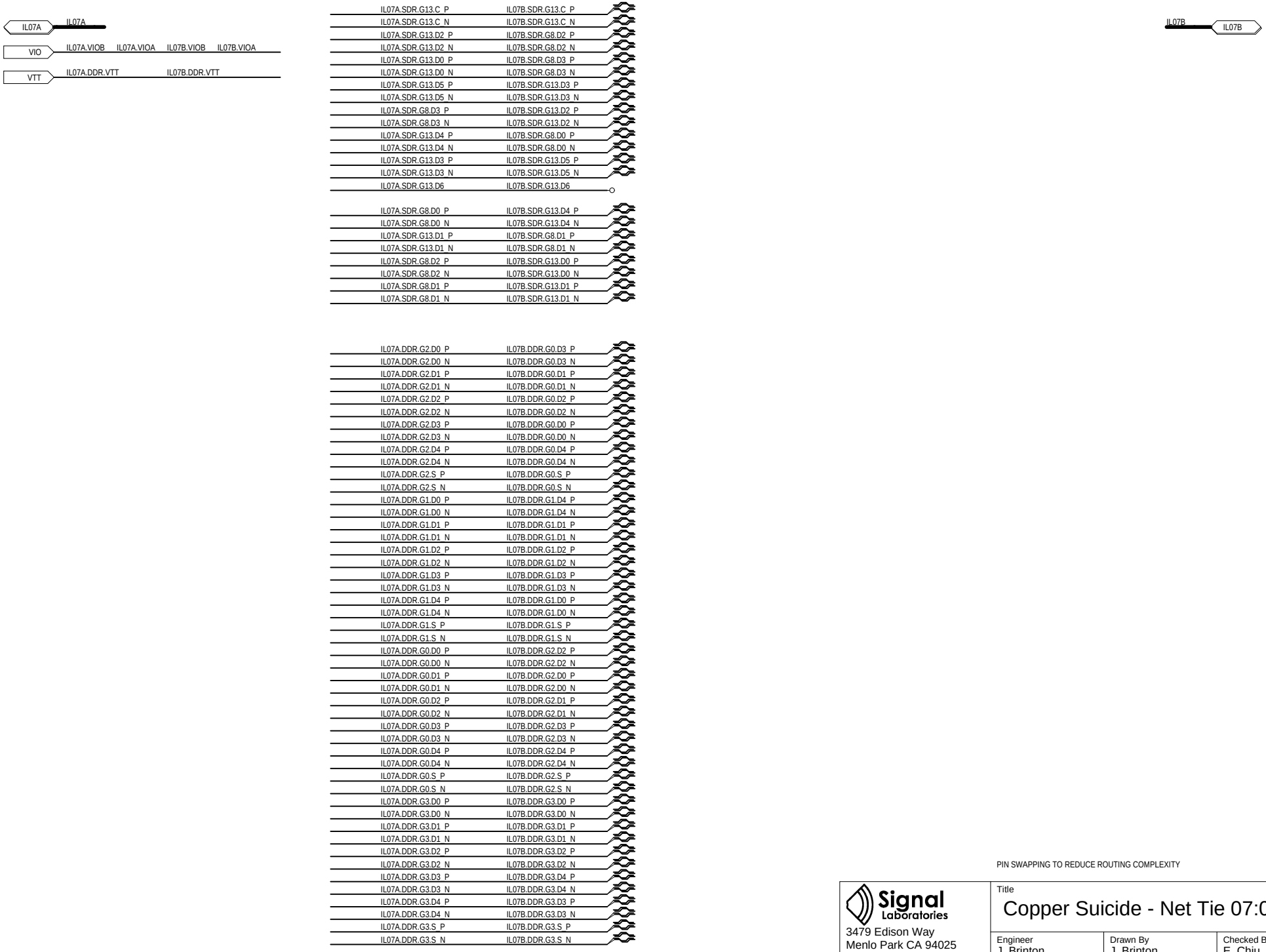
Title: Copper Suicide - Net Tie MIB

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 28 of 43	Date: 3/27/2017



PIN SWAPPING TO REDUCE ROUTING COMPLEXITY

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Menlo Park CA 94025
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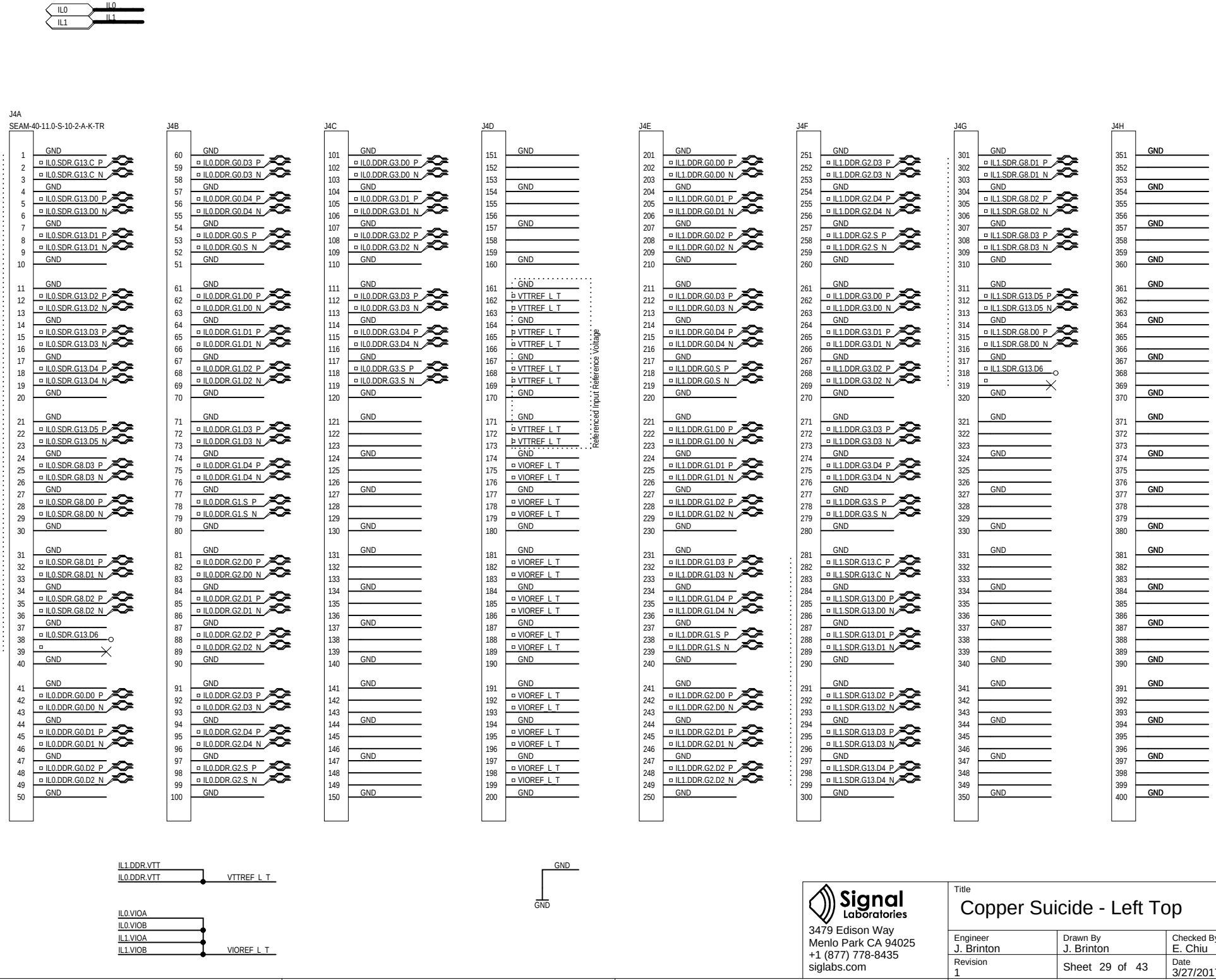
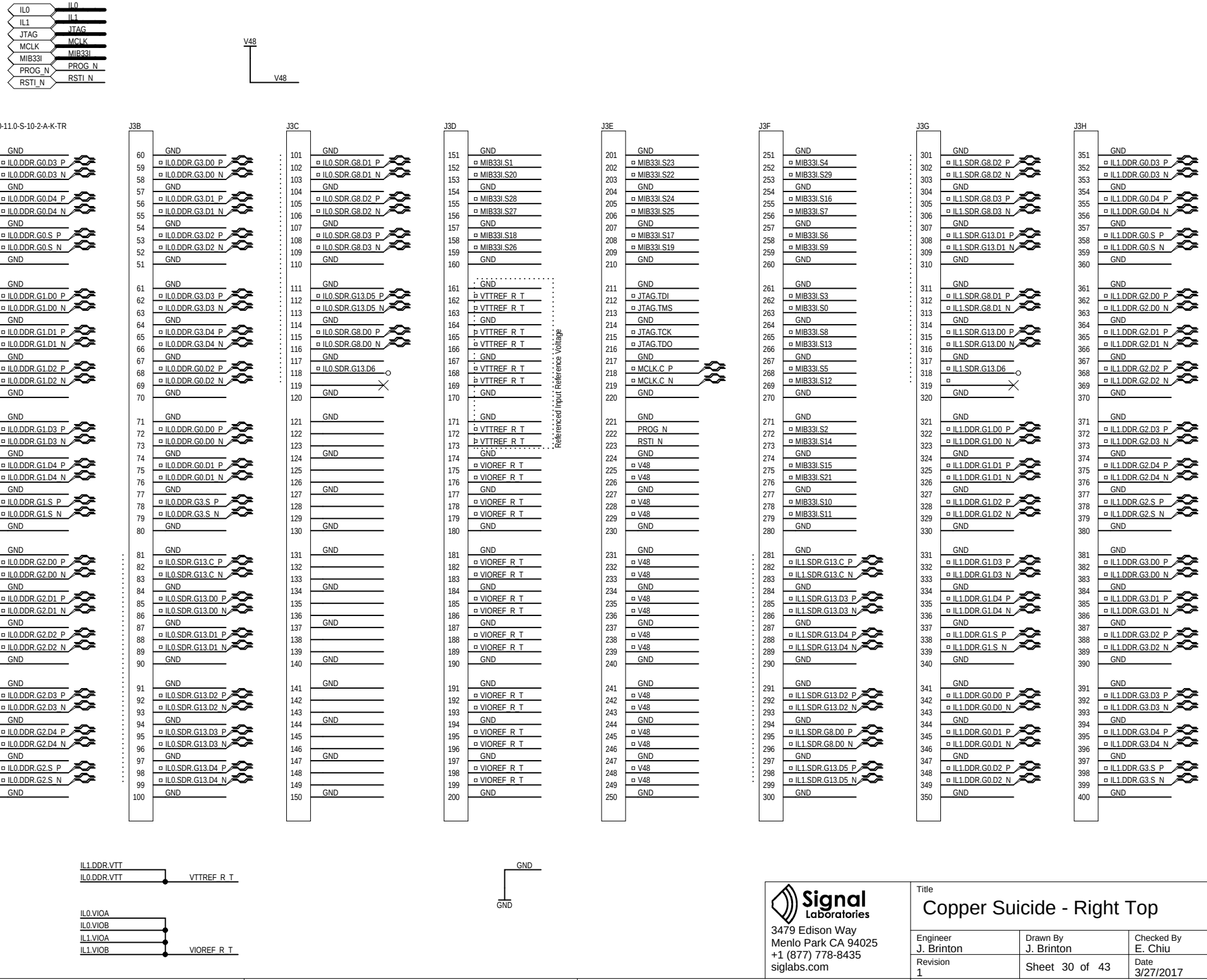
Title: Copper Suicide - Net Tie 07:07

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 28 of 43	Date: 3/27/2017



Signal Laboratories 3479 Edison Way Menlo Park CA 94025 +1 (877) 778-8435 siglabs.com	Title: Copper Suicide - Left Top		
Engineer: J. Brinton	Drawn By: J. Brinton	Checked By: E. Chiu	
Revision: 1	Sheet 29 of 43	Date: 3/27/2017	



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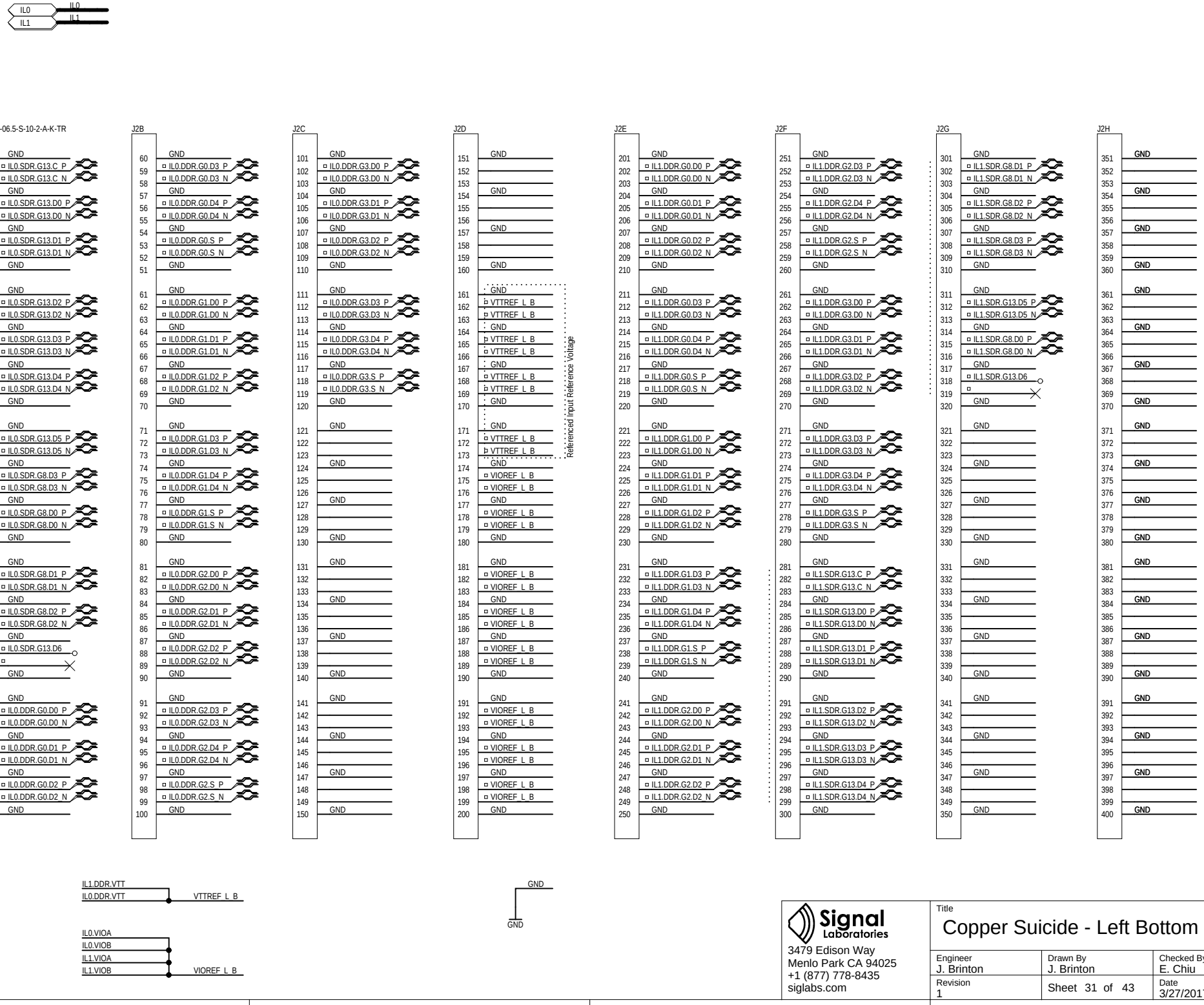
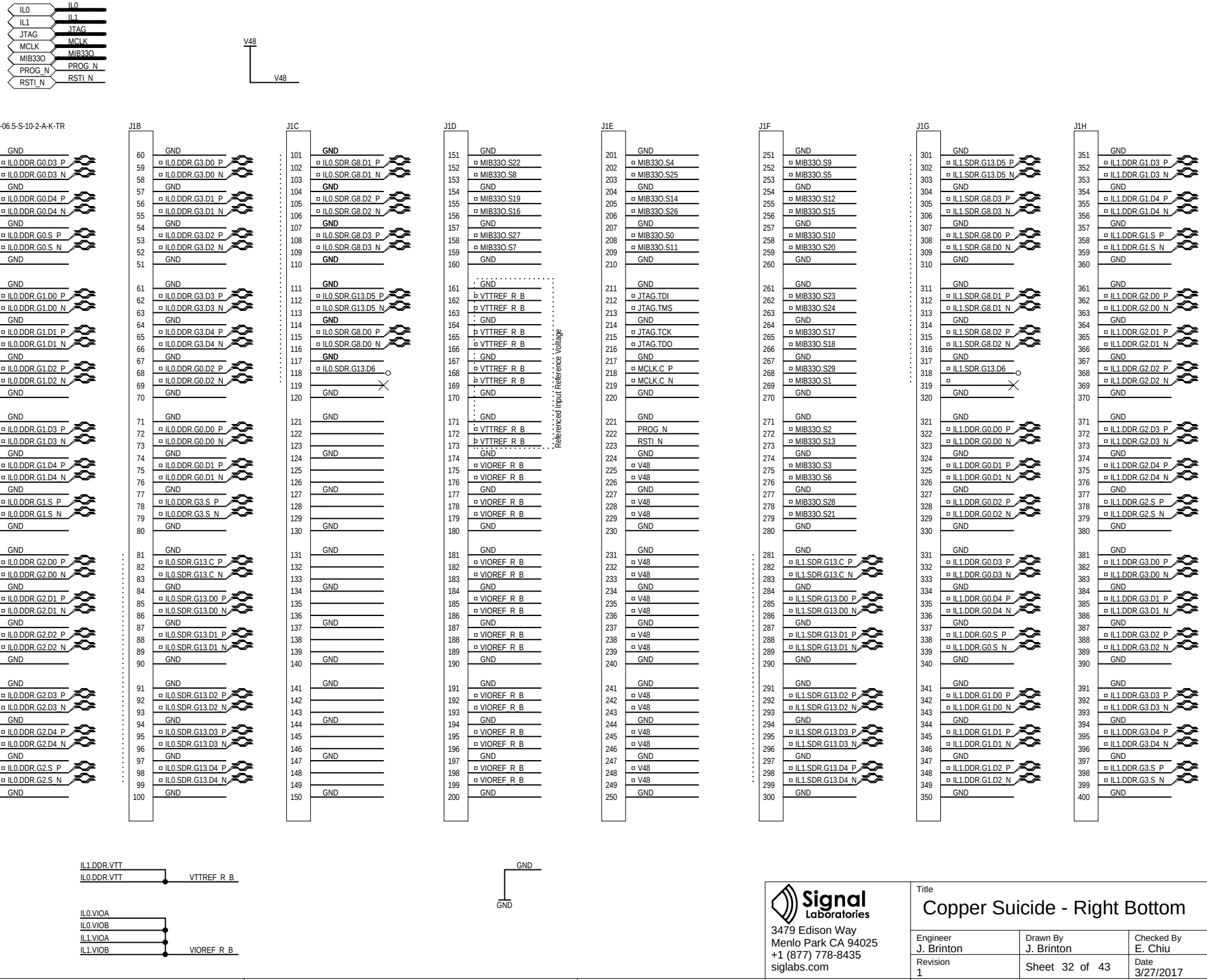
Title
Copper Suicide - Right Top

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 30 of 43	Date: 3/27/2017



Signal Laboratories 3479 Edison Way Menlo Park CA 94025 +1 (877) 778-8435 siglabs.com	Title: Copper Suicide - Left Bottom
Engineer: J. Brinton	Drawn By: J. Brinton
Checked By: E. Chiu	
Revision: 1	Sheet 31 of 43
Date: 3/27/2017	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J1C
J1D
J1E
J1F
J1G
J1H
Referenced Input Reference Voltage
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IL0.VIOB
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IL1.VIOB
VIOREF_R_B
GND
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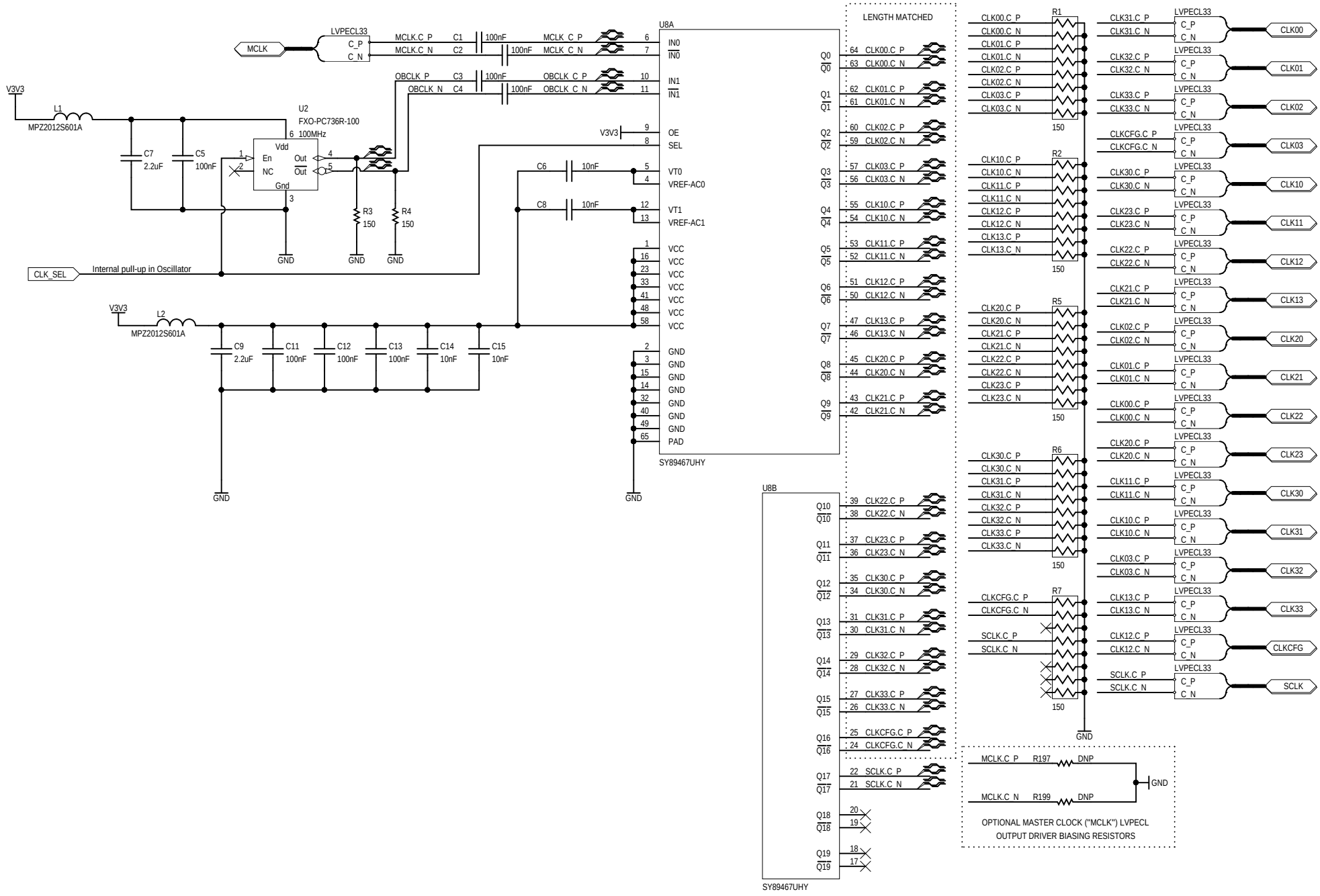
Title
Copper Suicide - Right Bottom
Engineer
J. Brinton
Drawn By
J. Brinton
Checked By
E. Chiu
Revision
1
Sheet 32 of 43
Date
3/27/2017



REVIEW COMPLETE: JDB 10/7/2016

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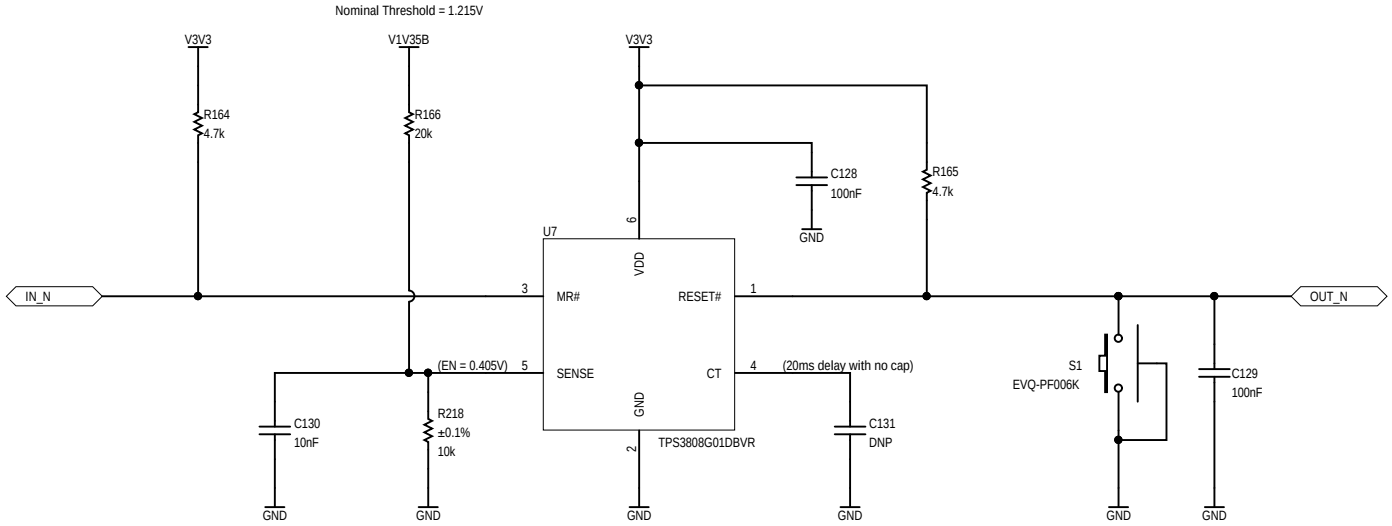
Title: Copper Suicide - Clock Fanout

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 33 of 43	Date: 3/27/2017



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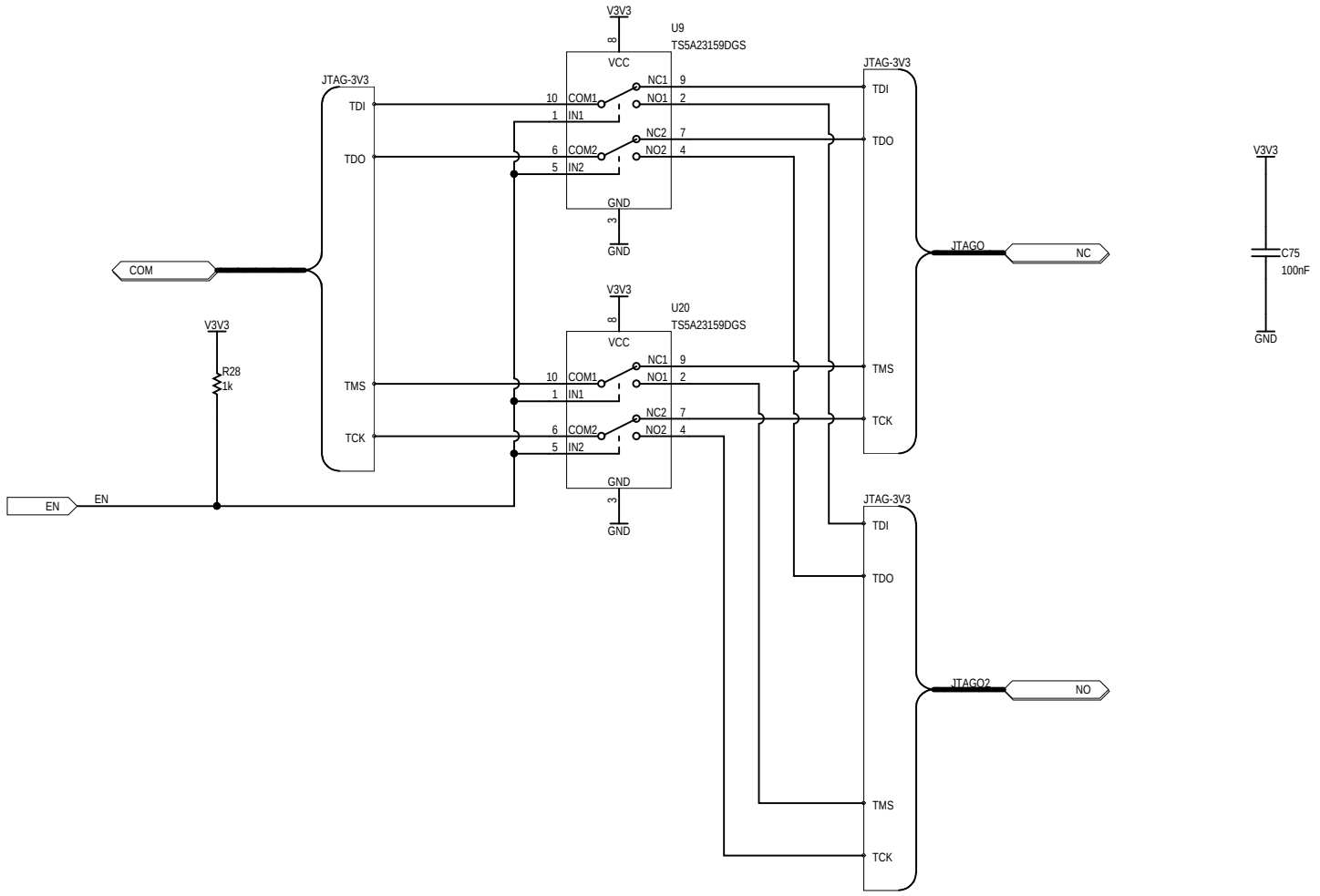
Title
Copper Suicide - Reset

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 34 of 43	Date: 3/27/2017



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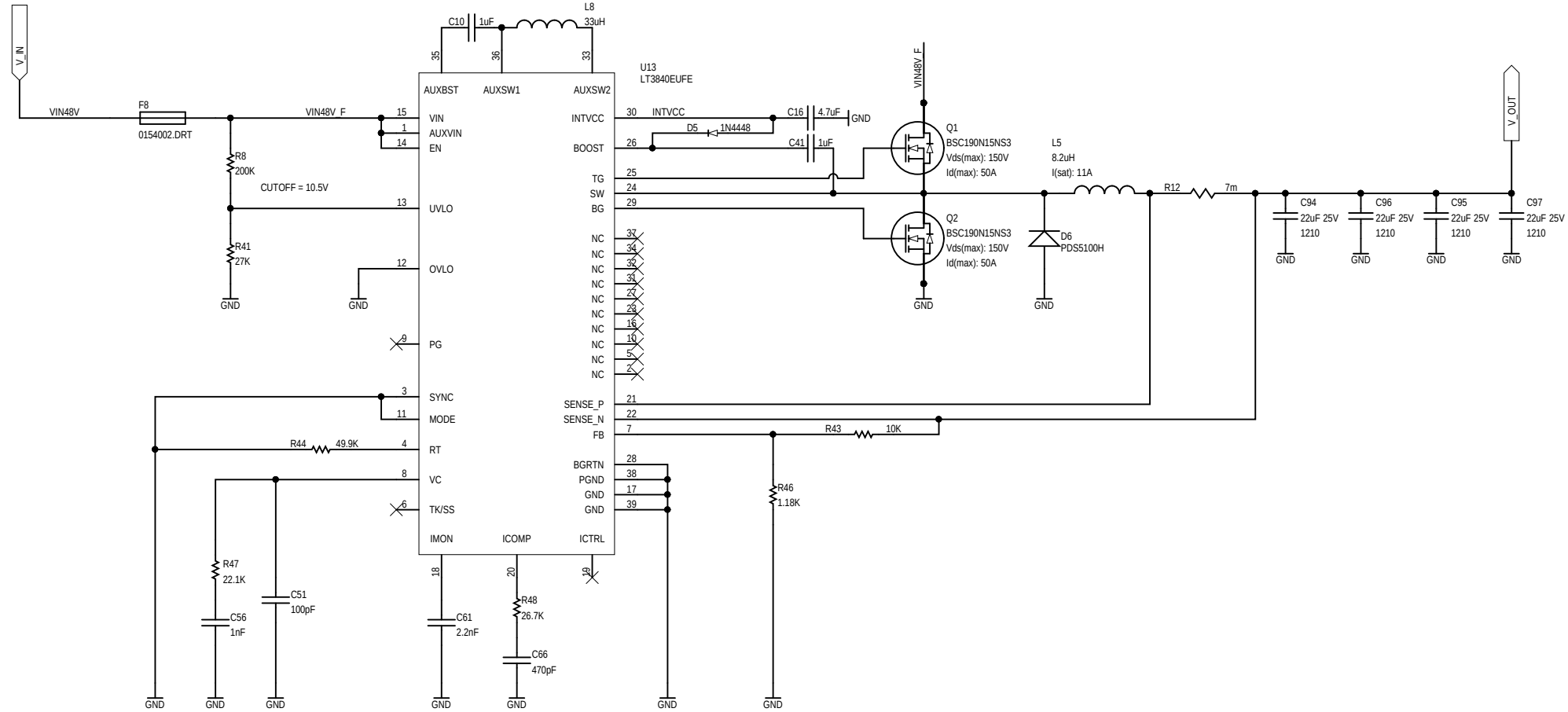
Title: Copper Suicide - JTAG Switch

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 35 of 43	Date: 3/27/2017



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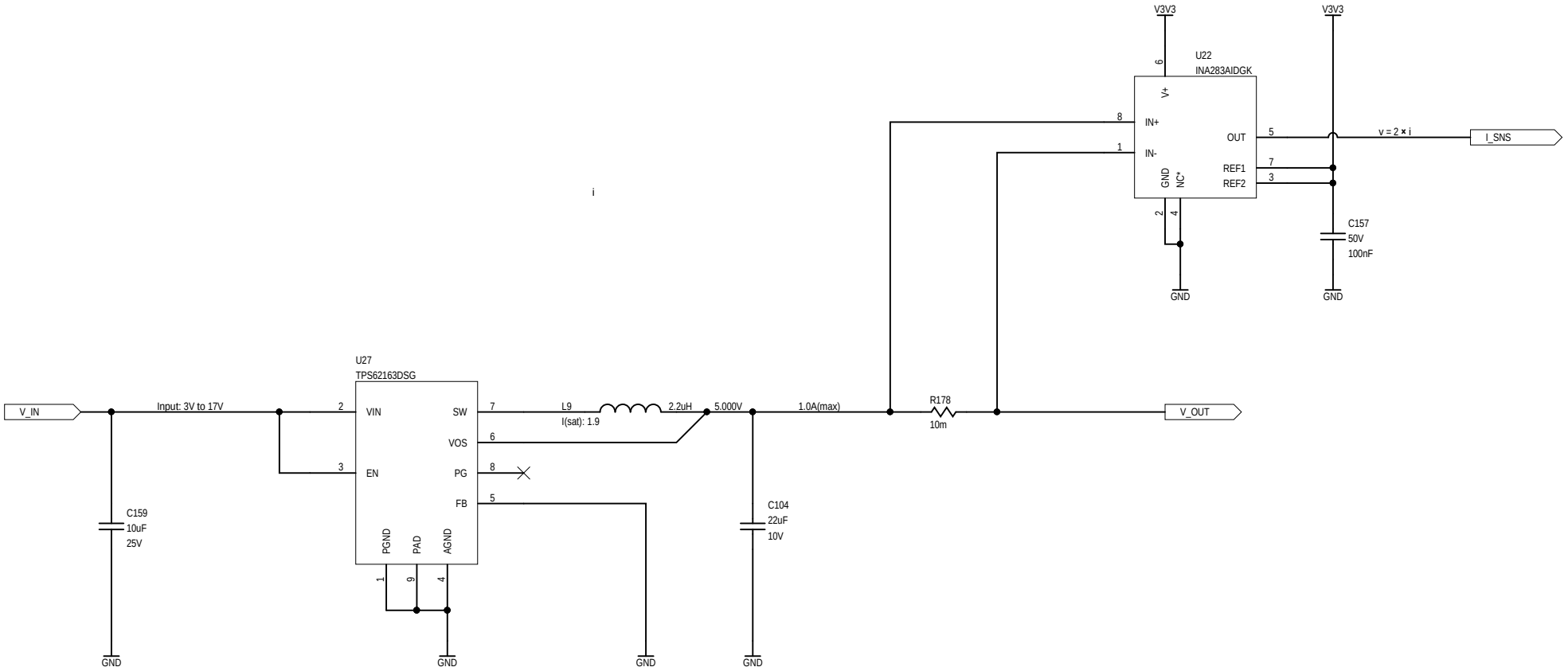
Title: Copper Suicide - Power 12V

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 36 of 43	Date: 3/27/2017



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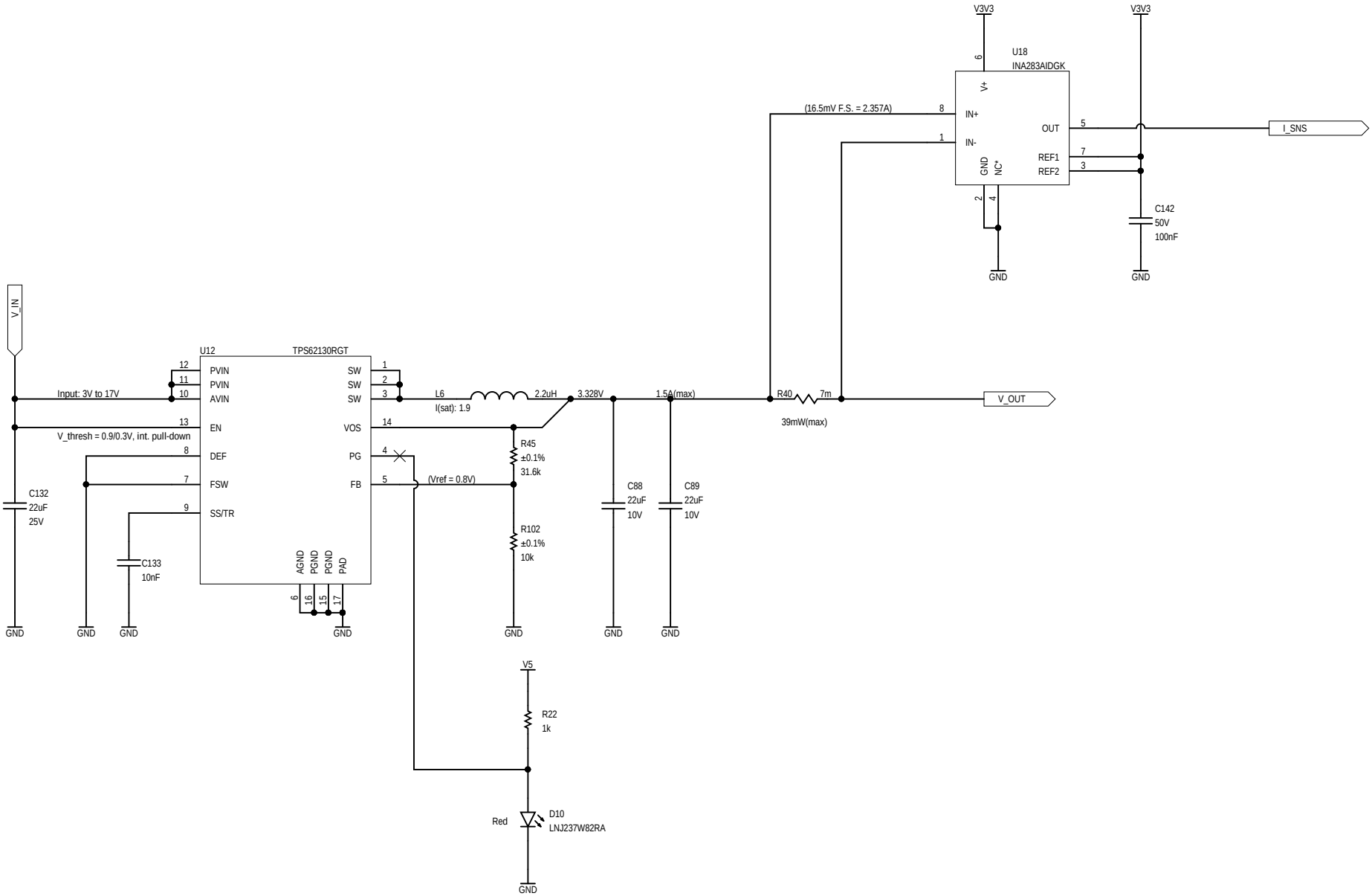
Title: Copper Suicide - Power 3.3V

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 37 of 43	Date: 3/27/2017



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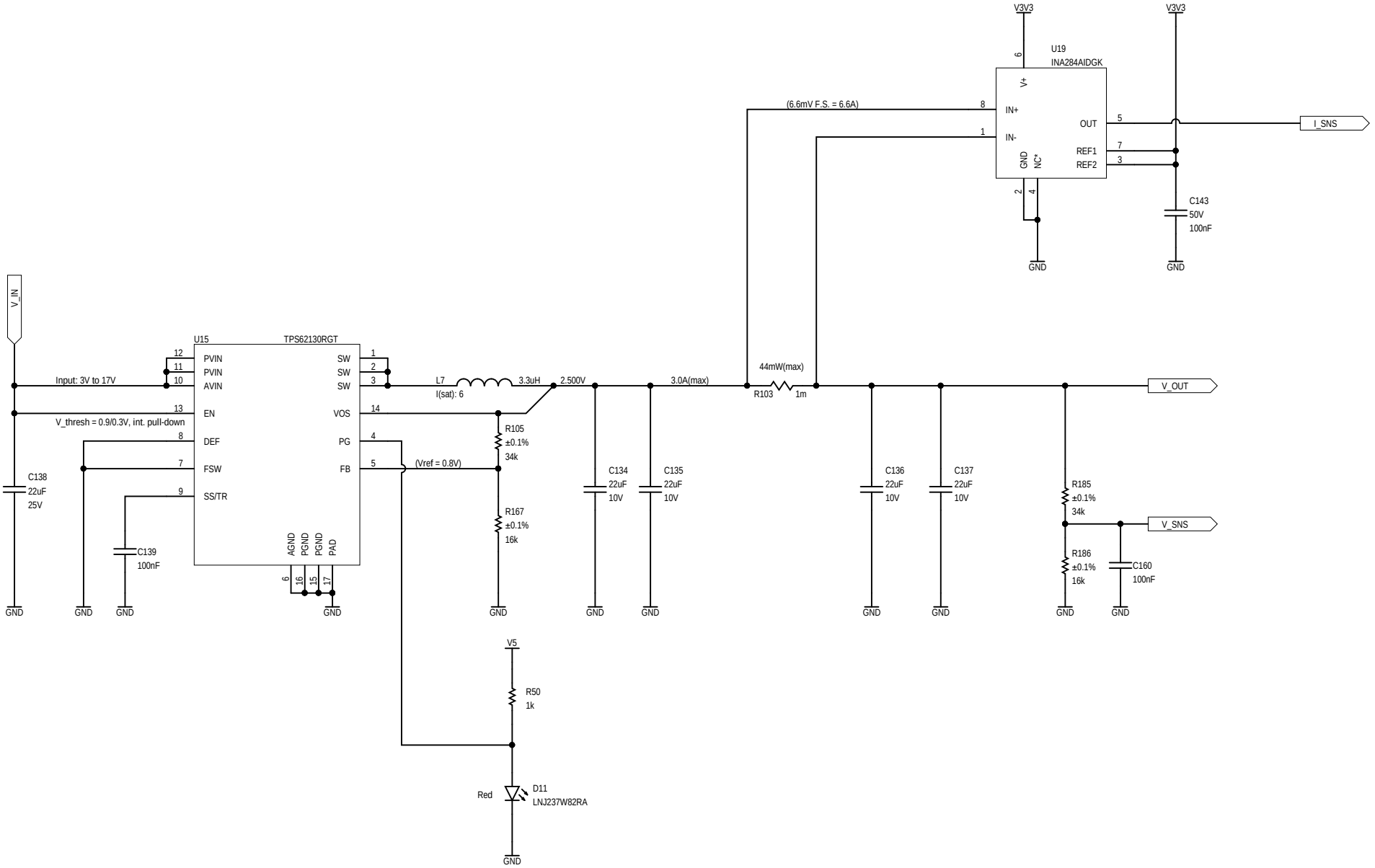
Title: Copper Suicide - Power 3.3V

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 37 of 43	Date: 3/27/2017


V3V3
V3V3
U19
INA284AIDGK
V+
IN+
IN-
OUT
REF1
REF2
GND
NC*
(6.6mV F.S. = 6.6A)
I_SNS
C143
50V
100nF
GND
GND
V_IN
U15
TPS62130RGT
PVIN
PVIN
AVIN
EN
DEF
FSW
SS/TR
SW
SW
SW
VOS
PG
FB
AGND
PGND
PGND
PAD
Input: 3V to 17V
V_thresh = 0.9/0.3V, int. pull-down
L7
3.3uH
I(sat): 6
2.500V
3.0A(max)
44mW(max)
R103
1m
V_OUT
R105
±0.1%
34k
(Vref = 0.8V)
R167
±0.1%
16k
C138
22uF
25V
C139
100nF
C134
22uF
10V
C135
22uF
10V
C136
22uF
10V
C137
22uF
10V
R185
±0.1%
34k
V_SNS
R186
±0.1%
16k
C160
100nF
V5
R50
1k
Red
D11
LNJ237W82RA
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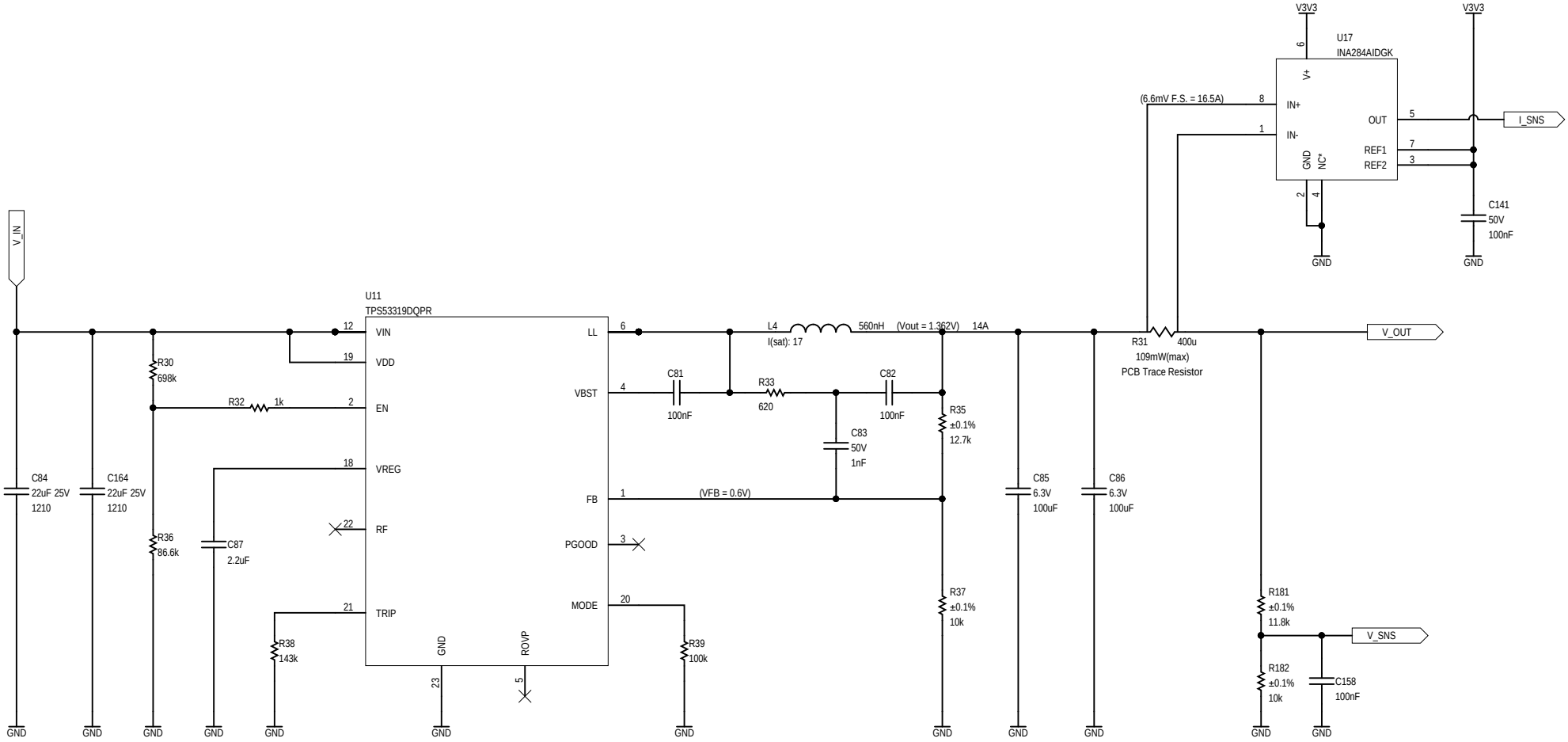
Title
Copper Suicide - Power 2.5V
Engineer
J. Brinton
Drawn By
J. Brinton
Checked By
E. Chiu
Revision
1
Sheet 38 of 43
Date
3/27/2017



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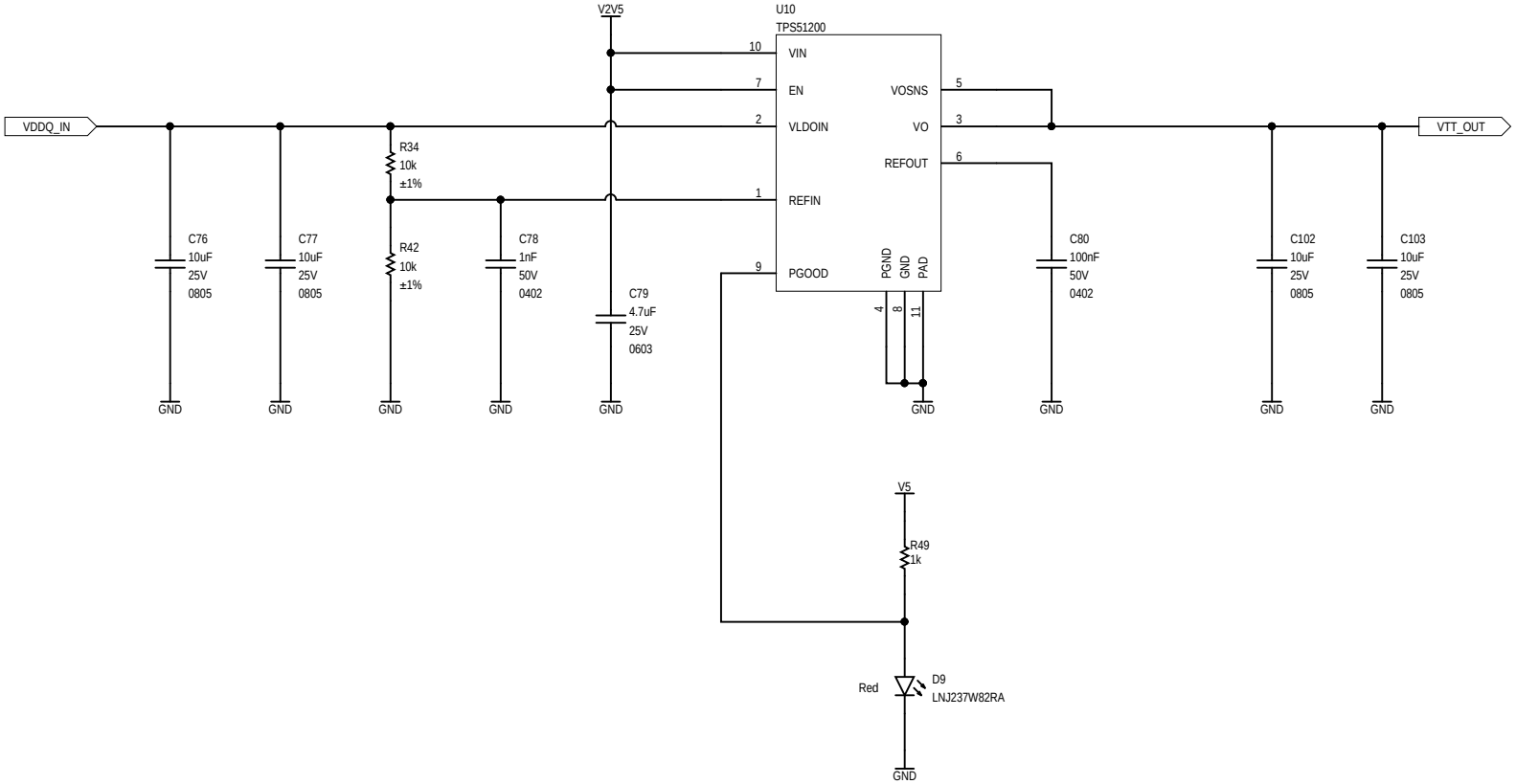
Title: Copper Suicide - Power 1.35V

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 39 of 43	Date: 3/27/2017



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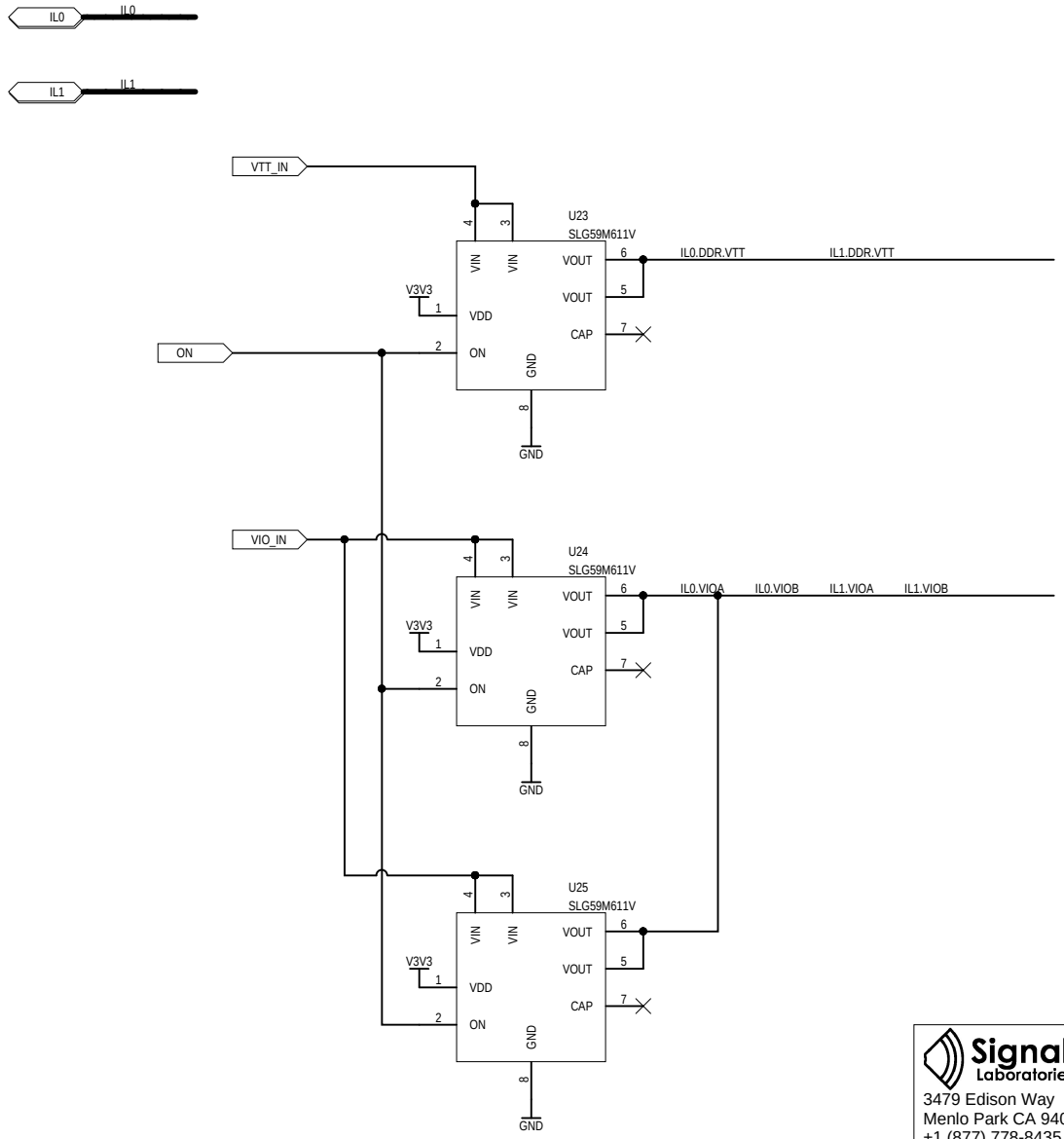
Title: Copper Suicide - VTT Power

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 40 of 43	Date: 3/27/2017



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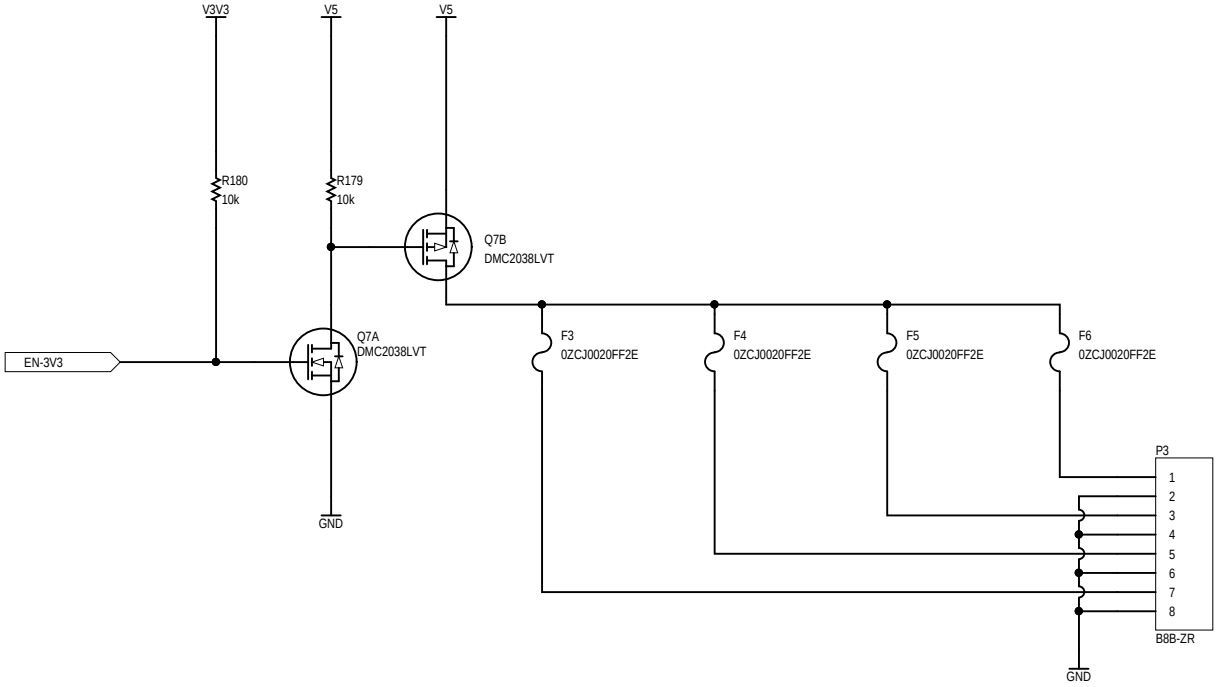
Title
Copper Suicide - Power Switch

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 41 of 43	Date: 3/27/2017



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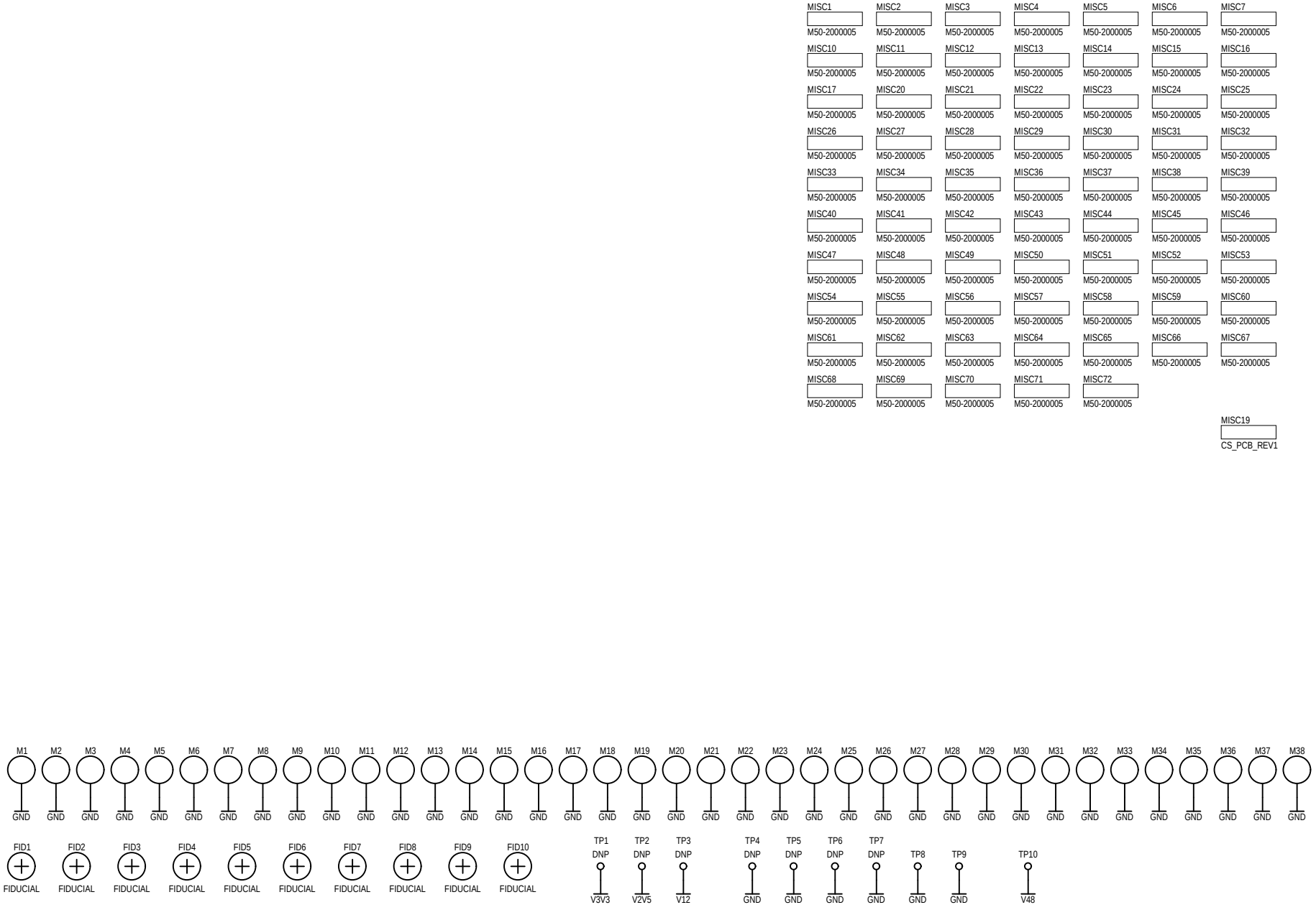
Title
Copper Suicide - Fan Switch

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 42 of 43	Date: 3/27/2017



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Title: Copper Suicide - Mechanical

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision: 1	Sheet 43 of 43	Date: 3/27/2017