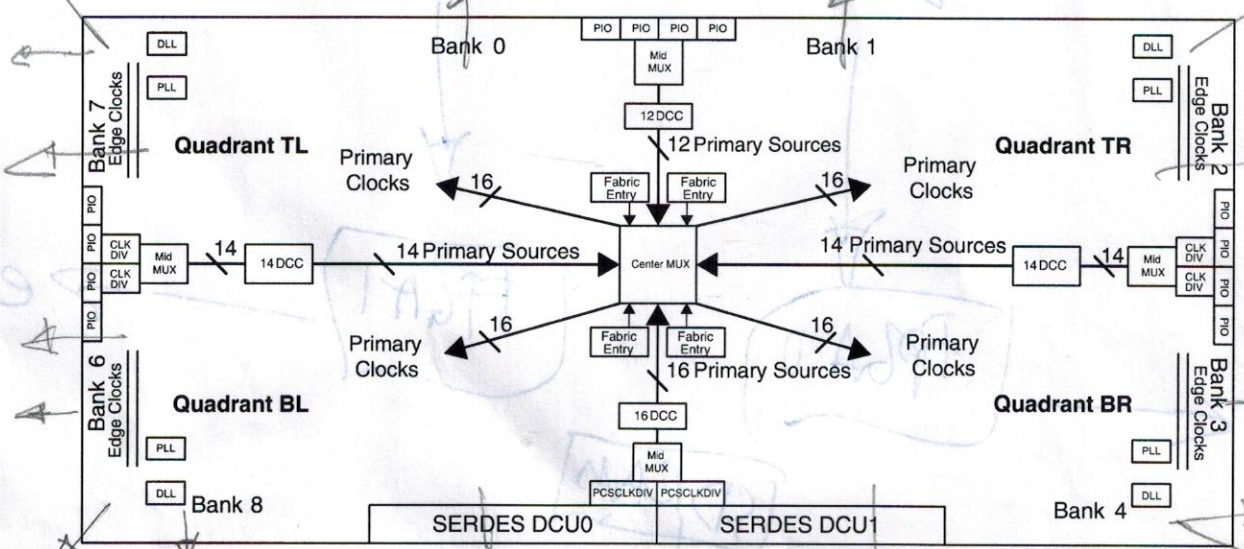
Clock Distribution Network

There are two main clock distribution networks for any member of the ECP5 product family, namely Primary Clock (PCLK) and Edge Clock (ECLK). These clock networks have the clock sources come from many different sources, such as Clock Pins, PLL outputs, DLLDEL outputs, Clock divider outputs, SERDES/PCS clocks and some on chip generated clock signal. There are clock dividers (CLKDIV) blocks to provide the slower clock from these clock sources. ECP5 also supports glitch-less dynamic enable function (DCC) for the PCLK Clock to save dynamic power. There are also some logics to allow dynamic glitch-less selection between two clocks for the PCLK network (DCS).

Overview of Clocking Network is shown in Figure 2-5, for LFE5UM-85 device.

Figure 2-5. LFE5UM-85 Clocking



Primary Clocks

The ECP5 device family provides low-skew, high fanout clock distribution to all synchronous elements in the FPGA fabric through the Primary Clock Network.

The primary clock network is divided into four clocking quadrants: Top Left (TL), Bottom Left (BL), Top Right (TR), and Bottom Right (BR). Each of these quadrants has 16 clocks that can be distributed to the fabric in the quadrant.

The Lattice Diamond software can automatically route each clock to one of the 4 quadrants up to a maximum of 16 clocks per quadrant. The user can change how the clocks are routed by specifying a preference in the Lattice Diamond software to locate the clock to specific. The ECP5 device provides the user with a maximum of 64 unique clock input sources that can be routed to the primary Clock network.

Primary clock sources are:

- Dedicated clock input pins
- PLL outputs
- CLKDIV outputs
- Internal FPGA fabric entries (with minimum general routing)
- SERDES/PCS/PCSDIV clocks
- OSC clock