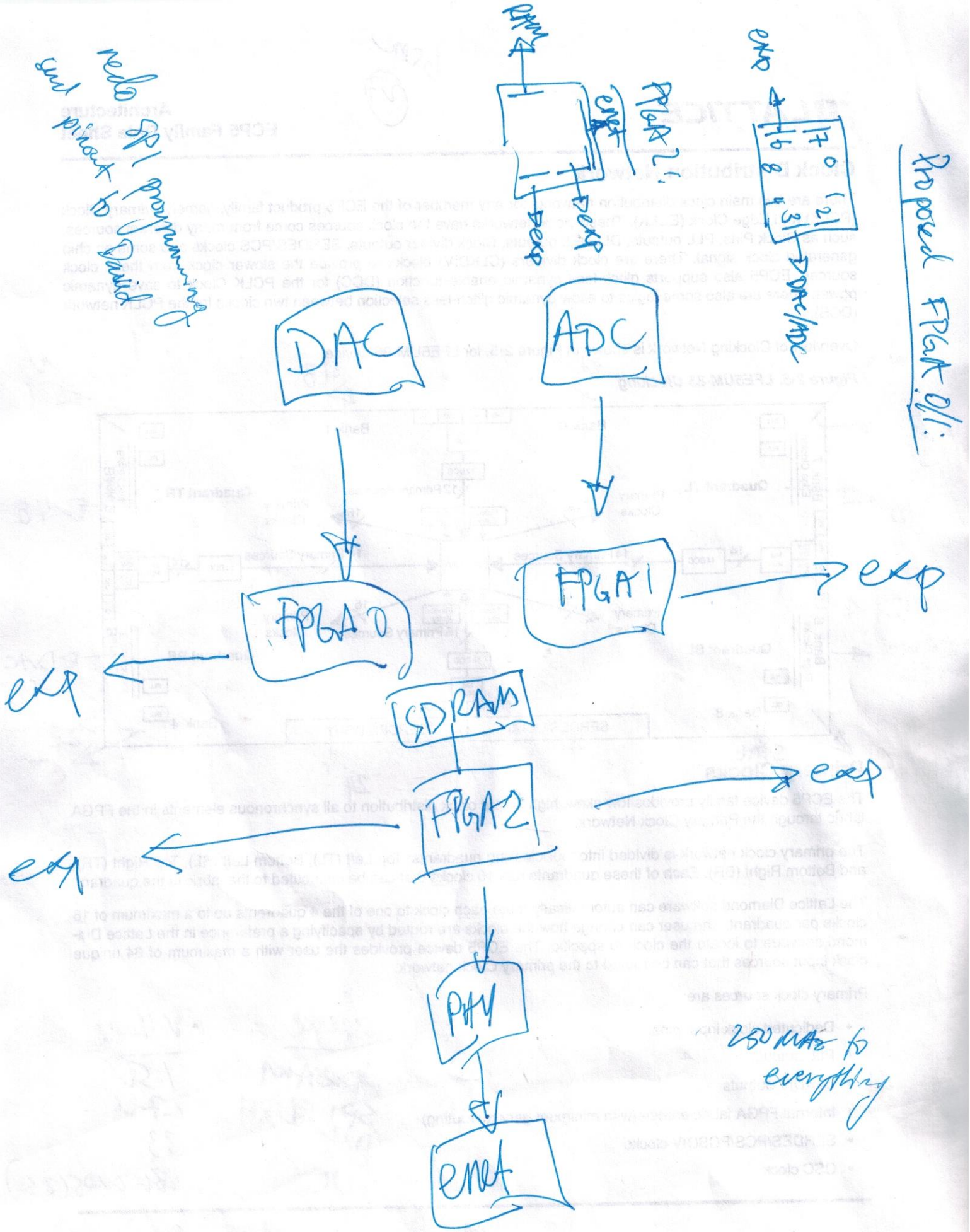

Proposed FPGA 0/1:
RAM
FPGA 2:
enet
exp
exp
exp
DAC/ADC
DAC
ADC
FPGA 0
FPGA 1
exp
exp
SDRAM
FPGA 2
exp
exp
PHY
enet
250 MHz to everything