ECP5 and ECP5-5G Hardware Checklist

December 2015 Technical Note TN1269

Introduction

When designing complex hardware using the ECP5™ and ECP5-5G™ FPGA, designers must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the ECP5 and ECP5-5G device. The document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

The device family consists of FPGA LUT densities ranging from 25K to 85K. This technical note assumes that the reader is familiar with the ECP5 and ECP5-5G device features as described in DS1044, ECP5 and ECP5-5G Family Data Sheet. The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Please refer to DS1044, ECP5 and ECP5-5G Family Data Sheet for the device-specific details.

The critical hardware areas covered in this technical note are:

- Power supplies as they relate to the ECP5 and ECP5-5G power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: Users should refer to the following documents for detailed recommendations.

- TN1260, ECP5 and ECP5-5G sysCONFIG Usage Guide
- TN1261, ECP5 and ECP5-5G SERDES/PCS Usage Guide
- TN1262, ECP5 and ECP5-5G sysIO Usage Guide
- TN1263, ECP5 and ECP5-5G sysClock PLL/DLL Design and Usage Guide
- TN1264, ECP5 and ECP5-5G Memory Usage Guide
- TN1265, ECP5 and ECP5-5G High-Speed I/O Interface
- TN1266, Power Consumption and Management for ECP5 and ECP5-5G Devices
- TN1267, ECP5 and ECP5-5G sysDSP Usage Guide
- TN1114, Electrical Recommendations for Lattice SERDES
- TN1033, High-Speed PCB Design Considerations
- TN1068, Decoupling and Bypass Filtering for Programmable Devices
- TN1084, LatticeSC SERDES Jitter

- HSPICE SERDES CML simulation package and die models in RLGC format (available under NDA, contact the license administrator at lic_admin@latticesemi.com)
- ECP5 and ECP5-5G-related pinout information can be found on the Lattice web site.

Power Supplies

All supplies including V_{CC}, V_{CCAUX} and V_{CCIO8} power supplies determine the ECP5 and ECP5-5G internal "power good" condition. These supplies need to be at a valid and stable level before the device can become operational. Several other supplies including V_{CCA}, V_{CCAUXA}, V_{CCHRX} and V_{CCHTX} are used in conjunction with on-board SERDES on LFE5UM/LFE5UM5G devices. Table 1 shows the power supplies and the appropriate voltage levels for each supply.

Table 1. ECP5 and ECP5-5G FPGA Power Supplies

Supply	Voltage (Nominal Value)	Description
VCC	1.1 V	FPGA core power supply
VCCA	1.1 V (LFE5UM) 1.2 V (LFE5UM5G)	Analog power supply for SERDES blocks (For LFE5UM/LFE5UM5G devices). Should be isolated and "clean" from excessive noise.
VCCAUX	2.5 V	Auxiliary power supply
VCCIO[0-4, 8][1]	1.2 V to 3.3 V	I/O power supply. Seven (eight on LFE5/LFE5UM5G-85 in 756 and 554 caBGA) general purpose I/O banks. Each bank has its own VCCIO supply: V_{CCIO8} is used in conjunction with pins dedicated and shared with device configuration, include JTAG $V_{CCIO0,1,2,3,4,6,}$ and $_{7}$ are optionally used based on per bank usage of I/O.
VCCHRX	1.1 V (LFE5UM) 1.2 V (LFE5UM5G)	Input terminate voltage supply for SERDES inputs (For LFE5UM/LFE5UM5G devices)
VCCHTX	1.1 V (LFE5UM) 1.2 V (LFE5UM5G)	CML output driver/termination voltage supply for SERDES outputs (for LFE5UM/LFE5UM5G devices)
VCCAUXA	2.5 V	Auxiliary power supply for SERDES (for LFE5UM/LFE5UM5G devices)

1. Bank 4 exists only on the LFE5/LFE5UM5G-85 device in 756 caBGA and 554 caBGA. It is not available in any other device/package combinations.

The ECP5 and ECP5-5G FPGA device has a power-up reset state machine that depends on various power supplies.

These supplies should come up monotonically. A power-up reset counter will begin to count after all of the approximate conditions are met:

- VCC reaches 0.9 V or above
- VCCAUX reaches 2.0 V or above
- VCCIO[8] reaches 0.95 V or above

Initialization of the device will not proceed until the last power supply has reached its minimum operating voltage.

ECP5 and ECP5-5G SERDES/PCS Power Supplies

Supplies dedicated to the operation of the SERDES/PCS include VCCA, VCCHRX, VCCHTX. All VCCA supply pins must always be powered to the recommended operating voltage range with the LFE5UM/LFE5UM5G devices. However, if no SERDES is used at all in the LFE5UM/LFE5UM5G device, all power supply pins for the SERDES can be connected to GND (VCCA, VCCAUXA, VCCHRX and VCCHTX).

When SERDES is used in the ECP5 and ECP5-5G devices, VCCHRX and VCCHTX can be left floating for unused SERDES channels. Unused channel outputs should be left tri-stated.

It is very important that the VCCA supply be low-noise and isolated from heavily loaded switching supplies. Please refer to TN1114, Electrical Recommendations for Lattice SERDES, for recommendations.

Power Estimation

Once the ECP5 and ECP5-5G device density, package and logic implementation is decided, power estimation for the system environment should be determined based on the software Power Calculator provided as part of the Lattice Diamond® design tool. When estimating power, the designer should keep two goals in mind:

1. Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current or maximum DC and AC current for the given system's environmental conditions.
2. The ability for the system environment and ECP5 and ECP5-5G device packaging to be able to support the specified maximum operating junction temperature. By determining these two criteria, the ECP5 and ECP5-5G device power requirements are taken into consideration early in the design phase.

Configuration Considerations

The ECP5 and ECP5-5G device includes provisions to program the FPGA via a JTAG interface or several modes utilizing the sysCONFIG port. The JTAG port includes a 4-pin interface. The interface requires the following PCB considerations.

Table 2. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
TDI	4.7K Pull-up to VCCIO8
TMS	4.7K Pull-up to VCCIO8
TDO	4.7K Pull-up to VCCIO8
TCK	4.7K Pull-down

Every PCB should have easy access to FPGA JTAG pins. This enables debugging in the final system. For best results, route the TCK, TMS, TDI and TDO signals to a common test header along with VCCIO8 and ground.

Using other programming modes requires the use of the CFG[2:0] input pins. For JTAG, the MODE pins are not used. The CFG[2:0] pins include weak internal pull-ups. It is recommended that 5-10K external resistors be used when using the sysCONFIG modes. Pull-up resistors should be connected to VCCIO8.

The use of external resistors is always needed if the configuration signals are being used to handshake to other devices. Recommended 4.7K pull-up resistors to VCCIO8 and pull-down to board ground should be used on the following pins.

Table 3. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	Pull-up
INITN	Pull-up
CCLK	Pull-down
CFG[0:2]	See Table 4. 1 = 4.7K pull-up, 0 = GND.

Table 4. Configuration Pins Needed per Programming Mode

Configuration Mode	Bus Size	Dedicated CFG[2:0]	Clock		Shared Pins	Dedicated Pins
			Pin	I/O		
SSPI	1 Bit	000	CCLK	Input	MISO, MOSI, SI, DOUT, HOLDN	PROGRAMN, INITN, DONE
MSPI	1 Bit	010	MCLK	Output	MISO, MOSI, CSSPIN, DOUT	PROGRAMN, INITN, DONE
	2 Bits				D[1:0], CSSPIN, DOUT	
	4 Bits				D[3:0], CSSPIN, DOUT	
SCM	1 Bit	101	CCLK	Input	DI, DOUT	PROGRAMN, INITN, DONE
SPCM (Parallel)	8 Bits	111	CCLK	Input	D[7:0], DOUT, CSON, BUSY, WRITEN, CSN, CS1N	PROGRAMN, INITN, DONE
JTAG	1 Bit	xxx	TCK	Input	N/A	TCK, TMS, TDI, TDO

I/O Pin Assignments

The VCCA provides a “quiet” supply for the internal PLLs and critical SERDES blocks. For the best jitter performance, careful pin assignment will keep “noisy” I/O pins away from “sensitive” pins. The leading causes of PCB related SERDES crosstalk is related to FPGA outputs located in close proximity to the sensitive SERDES power supplies. These supplies require cautious board layout to insure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet filtered supplies for the VCCA, however robust PCB layout is required to insure that noise does not infiltrate into these analog supplies.

Although coupling has been reduced in the device packages of ECP5 and ECP5-5G devices where little crosstalk is generated, the PCB board can cause significant noise injection from any I/O pin adjacent to SERDES data, reference clock, and power pins as well as other critical I/O pins such as clock signals. TN1114, Electrical Recommendations for Lattice SERDES, provides detailed guidelines for optimizing the hardware to reduce the likelihood of crosstalk to the analog supplies. PCB traces running in parallel for long distances need careful analysis. Simulate any suspicious traces using a PCB crosstalk simulation tool to determine if they will cause problems.

It is common practice for designers to select pinouts for their system very early in the design cycle. For the FPGA designer, this requires a detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/Os. Lattice provides detailed pinout information that can be downloaded from the Lattice website in .csv format for designers to use as a resource to create pinout information. For example, by navigating to the pinout.csv file, the user can gather the pinout details for all the different package offerings of the device in the family, including I/O banking, differential pairing, Dual Function of the pins, and input and output details.

Clock Inputs

The ECP5 and ECP5-5G device does not provide dedicated pins for clock inputs. All clock inputs are shared with the General Purpose I/O pin. When the pin is not used for clocking, the user can use it as a general purpose I/O pin.

However, when these pins are used for clocking purpose, the user needs to pay attention to minimize signal noise on these pins. Please refer to TN1265, ECP5 and ECP5-5G High-Speed I/O Interface.

The pins can be found under the Dual Function column of the pinlist csv file.

Pinout Considerations

The ECP5 and ECP5-5G supports many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to implementation of the PCB design. The pinout selection must be completed with an understanding of the interface building blocks of the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and PLL and DLL usage. Refer to TN1265, ECP5 and ECP5-5G High-Speed I/O Interface for rules pertaining to these interface types.

LVDS Pin Assignments

True LVDS inputs and outputs are available on I/O pins on the left and right sides of the devices. Top and I/O banks do not support True LVDS standard, but can support emulated LVDS outputs. True LVDS input pairing on left and right banks can be found under the Differential column in the pinlist csv file. True LVDS output pair are available on any A & B pair of the left and right banks.

Emulated LVDS output are available on pairs around all banks, but this will require external termination resistors. This is described in TN1262, ECP5 and ECP5-5G sysIO Usage Guide.

HSUL and SSTL Pin Assignments

The HSUL and SSTL interfaces are externally referenced I/O standards require an external reference voltage. The V_{REF} pin(s) should get high priority when assigning pins on the PCB. These pins can be found in the Dual Function column with VREF1 label. Each bank includes a separate VREF voltage. VREF1 sets the threshold for the referenced input buffers. Each I/O is individually configurable based on the bank's supply and reference voltages.

SERDES Pin Considerations

High-speed signaling requires careful PCB design. Maintaining good transmission line characteristics is a requirement. A continuous ground reference should be maintained with high-speed routing. This includes tightly matched differential routing with very few discontinuities. Please refer to TN1033, High-Speed PCB Design Considerations, for suggested methods and guidance.

When operating at 2.5 Gbps or above, use of the following FPGA I/O pins can cause increased jitter. Extra care must be given to these pins when used in combination with the high-speed SERDES interface. High-speed switching output assignments should be minimized or avoided on these pins when the SERDES interface is in use. Only static output or input configuration is recommended.

LFE5U to LFE5UM/LFE5UM5G and LFE5UM to LFE5UM5G Migration

Besides migrating design from one device to another device (i.e. 25K to 45K) on same package (i.e. caBGA554) within its own family in LFE5U and LFE5UM/LFE5UM5G, user can migrate from the non-SERDES (LFE5U) device to SERDES (LFE5UM/LFE5UM5G) device in the same package.

If the user anticipates his design may use SERDES at a later time of his product, he would first design, and making all the connections to, all SERDES circuit on board.

For example, if the user anticipates the need to use the two Dual SERDES on LFE5U-85 product, he has to design his board with LFE5UM//LFE5UM5G-85, which contains the SERDES ports, to the not-yet-populated SERDES circuit on the board. This requires all SERDES powers to be connected to power sources on the board. He can still put in the LFE5U-85 device because the two devices are pin compatible, other than the SERDES pins.

When designing LFE5U/UM with future migration to LFE5UM5G in mind to increase the SERDES thruput to 5G, care has to be taken that the VCCA/VCCHRX/VCCHTX need to be powered by 1.2V nominal supply voltage for LFE5UM5G. A different power rail needs to be implemented on the board for this future migration.

Table 5. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	VCC core @ 1.1 V +/-5%		
1.1.1	Use a PCB plane for VCC core with proper decoupling		
1.1.2	VCC core sized to meet power requirement calculation from software		
1.2	VCCA @ 1.1V +/- 5% (LFE5UM), @1.2 V +/- 5% (LFE5UM5G)		
1.2.1	VCCA “quiet” and isolated”		
1.2.2	VCCA pins should be ganged together and a solid PCB plane is recommended. This plane should not have adjacent non-SERDES signals passing above or below. It should also be isolated from the VCC core power plane.		
1.3	All VCCIO are between1.2 V to 3.3 V		
1.3.1	VCCIO8 used with configuration interfaces (i.e. memory devices). Need to match specifications.		
1.3.2	VCCIO[1:7] used based on user design		
1.4	VCCAUX and VCCAUXA @ 2.5 V +/- 5%		
1.6	Power estimation		
2	**SERDES Power Supplies**		
2.3	VCCHRX and VCCHTX connected for USED SERDES channels		
2.3.1	VCCHRX and VCCHTX are at 1.1 V +/- 5% (LFE5UM), 1.2V +/- 5% (LFE5UM5G)		
3	**Configuration**		
3.1	Pull-ups and pull-downs on configuration specific pins		
3.2	VCCIO8 bank voltage matches sysCONFIG peripheral devices such as SPI Flash		
3.3	Pull-up or pull-down on SPIFASTN pin		
4	**SERDES**		
4.1	Dedicated reference clock input from clock source meets the DC and AC requirements		
4.1.1	External AC coupling caps may be required for compatibility to common-mode levels		
4.1.2	Ref clock termination resistors may be needed for compatible signaling levels		
4.2	Maintain good high-speed transmission line routing		
4.2.1	Continuous ground reference plane to serial channels		
4.2.2	Tightly length matched differential traces		
4.2.3	Do not pass other signals on the PCB above or below the high-speed SERDES without isolation.		

Table 5. Hardware Checklist (Continued)

	Item	OK	NA
4.2.4	Keep non-SERDES signal traces from passing above or below the VCCA power plane without isolation.		
4.2.5	Avoid the aggressor pins mentioned previously in this document.		
5	**Special Pin Assignments**		
5.2	VREF assignments followed for single-ended SSTL inputs		
5.2.1	Properly decouple the VREF source		
6	**Critical Pinout Selection**		
6.1	Pinout has been chosen to address FPGA resource connections to I/O logic and clock resources per TN1265, ECP5 and ECP5-5G High-Speed I/O Interface.		
6.2	Shared general purpose I/Os are used as inputs for FPGA PLL and Clock inputs.		
7	**JTAG**		
7.1	Pull-down on TCK. See Table 3.		
7.2	Pull-up on TDI, TMS, TDO. See Table 3.		
8	**LPDDR3 and DDR3 Interface Requirements**		
8.1	DQ, DM, and DQS signals should be routed in a data group and should have similar routing and matched via counts. Using more than three vias is not recommended in the route between the FPGA controller and memory device.		
8.2	Maintain a maximum of ±50 mil between any DQ/DM and its associated DQS strobe within a DQ group. Use careful serpentine routing to meet this requirement.		
8.3	All data groups must reference a ground plane within the stack-up.		
8.4	DDR trace reference must be solid without slots or breaks. It should be continuous between the FPGA and the memory.		
8.5	Provide a separation of 3 W spacing between a data group and any other unrelated signals to avoid crosstalk issues. Use a minimum of 2 W spacing between all DDR traces excluding differential CK and DQS signals.		
8.6	Assigned FPGA I/O within a data group can be swapped to allow clean layout. Do not swap DQS assignments.		
8.7	Differential pair of DQS to DQS_N trace lengths should be matched at ±10 mil.		
8.8	Resistor terminations (DQ) placed in a fly-by fashion at the FPGA is highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mil.		
8.9	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±100 mil.		
8.10	Address/control signals and the associated CK and CK_N differential FPGA clock should be routed with a control trace matching ±100 mil.		
8.11	CK to CK_N trace lengths must be matched to within ±10 mil.		
8.12	Address and control signals can be referenced to a power plane if a ground plane is not available. Ground reference is preferred.		
8.13	Address and control signals should be kept on a different routing layer from DQ, DQS, and DM to isolate crosstalk between the signals.		
8.14	Differential terminations used by the CLK/CLKN pair must be located as close as possible to the memory.		
8.15	Address and control terminations placed after the memory component using a fly-by technique are highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mils.		

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
December 2015	1.2	Updated Power Supplies section. Revised Voltage (Nominal Value) for VCCA, VCCHRX and VCCHTX in Table 1, ECP5 and ECP5-5G FPGA Power Supplies.
		Updated LFE5U to LFE5UM/LFE5UM5G and LFE5UM to LFE5UM5G Migration section. — Changed section title. — Removed instances of LFE5U5G). — Added new paragraph content. — Revised items 1.2, 2.3.1and 4.2.4 in Table 5, Hardware Checklist
November 2015	1.1	Added support for ECP5-5G.
		Changed document title to ECP5 and ECP5-5G Hardware Checklist.
		Changed ECP5U and ECP5UM to LFE5U and LFE5UM.
		Updated Configuration Considerations section. Revised PCB recommendation for TDI, TMS and TDO in Table 2, JTAG Pin Recommendations
		Updated Technical Support Assistance section.
March 2014	01.0	Initial release.