

MAIN  
main.SchDoc

MECH  
mechanical.SchDoc

A

A

B

B

NOTE: DO ECP5 DESIGN CHECKLIST!  
NOTE: ANALYZE JTAG PULL-UPS/DOWNS  
NOTE: ANALYZE DDR3 TERMINATION

1. MATCH ALL DIFFERENTIAL PAIRS TO 0.2MM

C

C

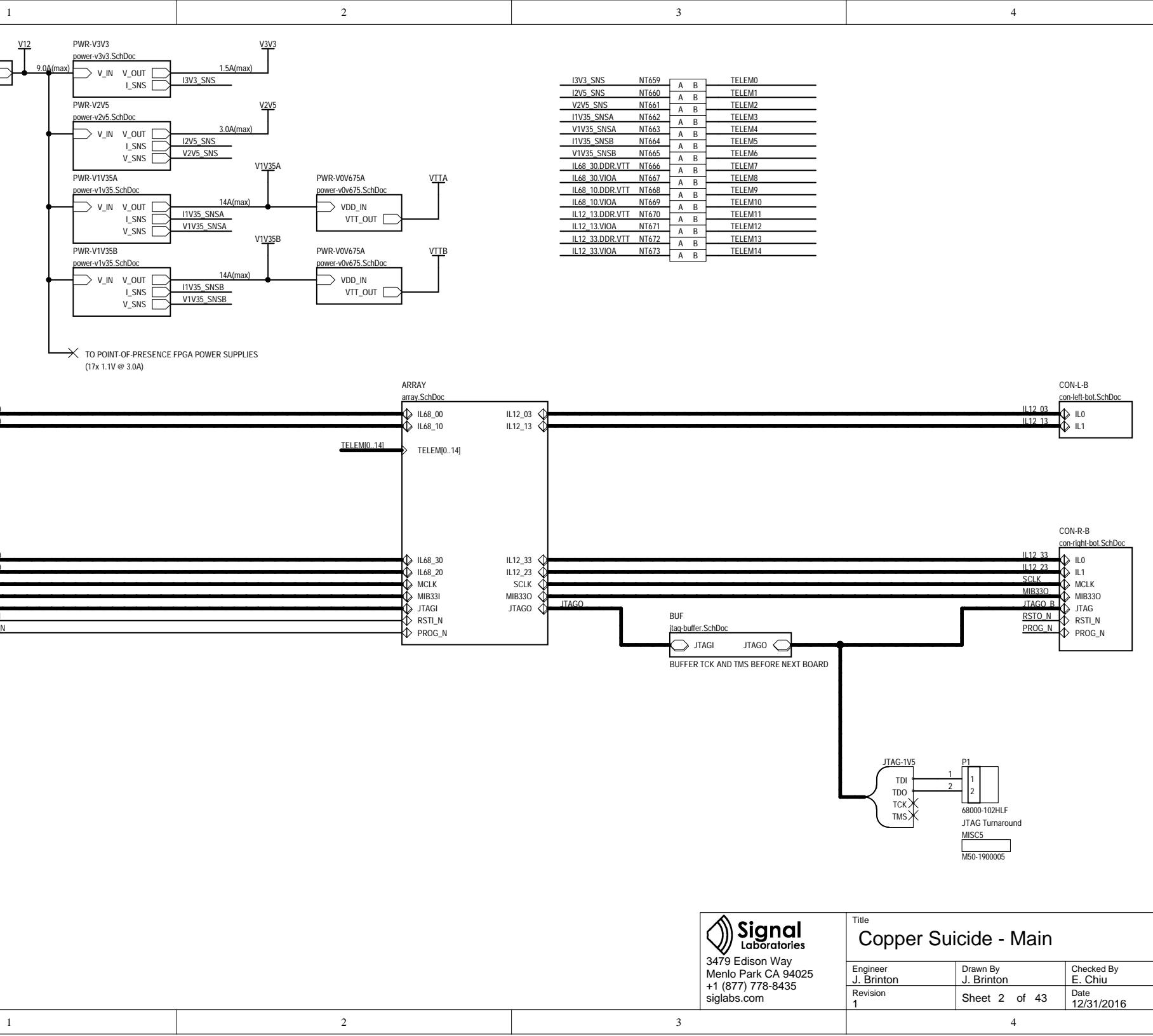
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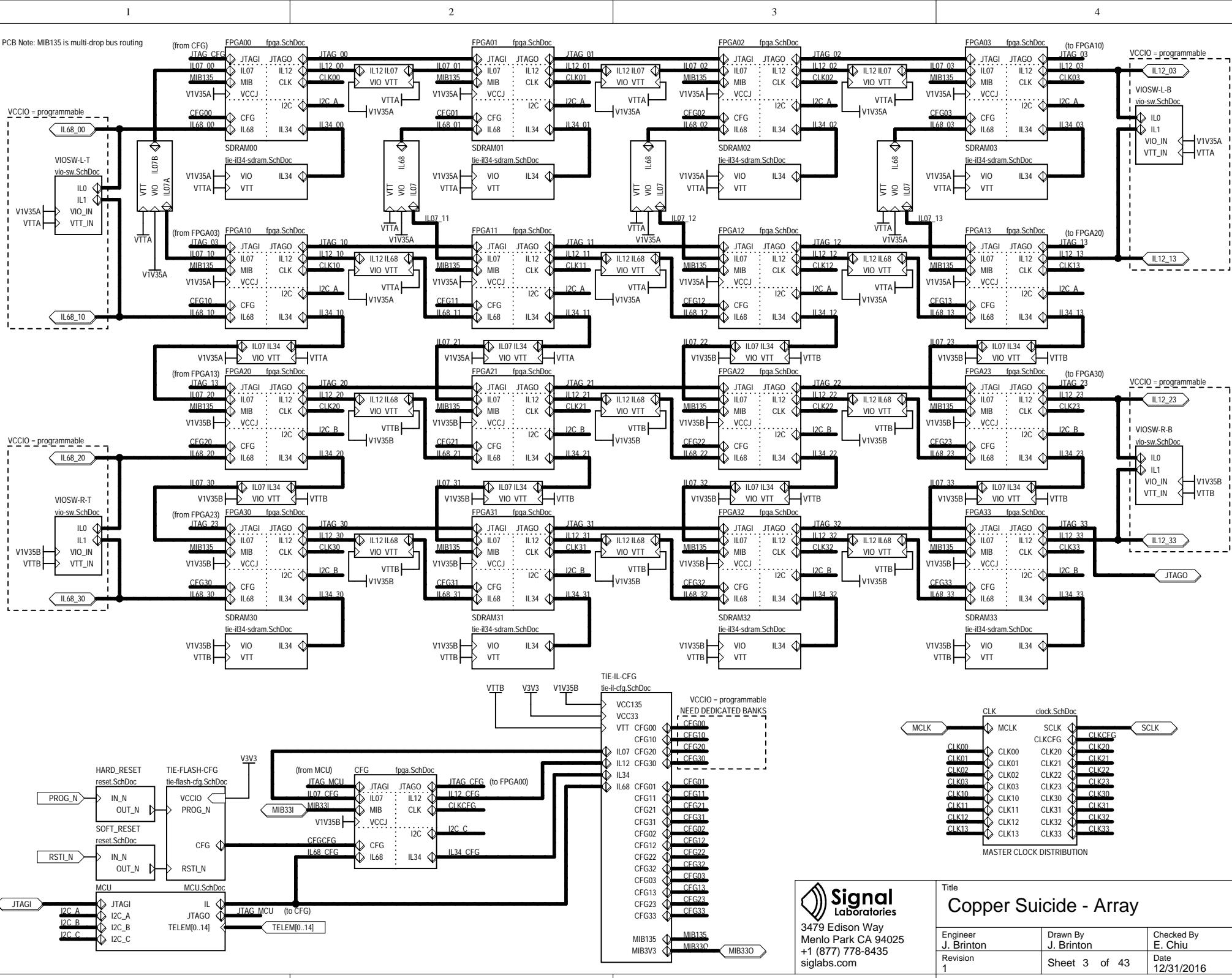
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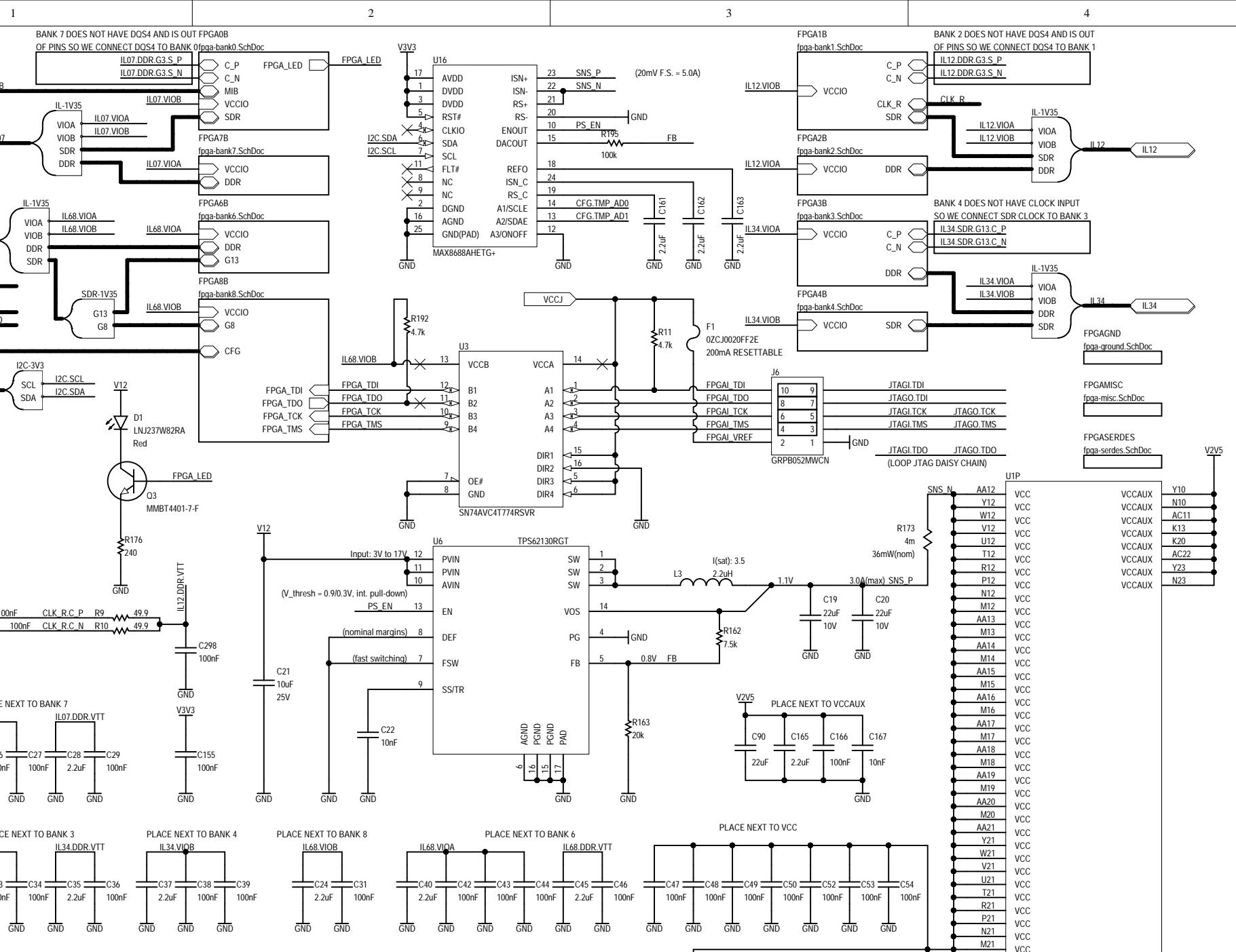


**Signal**  
Laboratories  
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Title		
<b>Copper Suicide - Top</b>		
Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision 1	Sheet 1 of 43	Date 12/31/2016







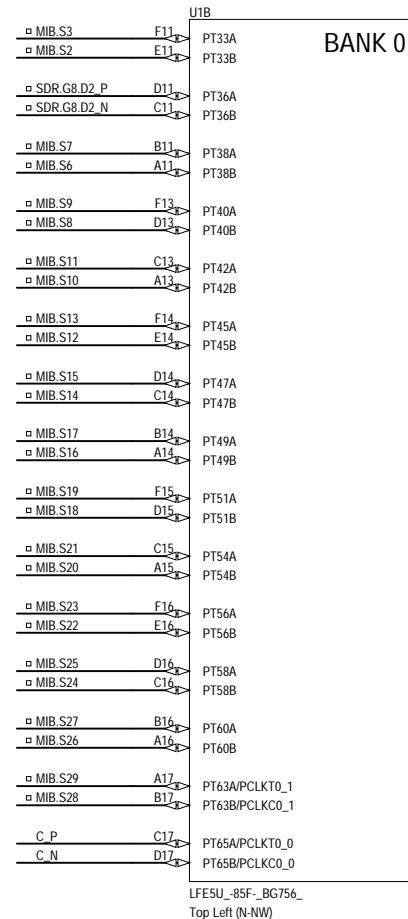
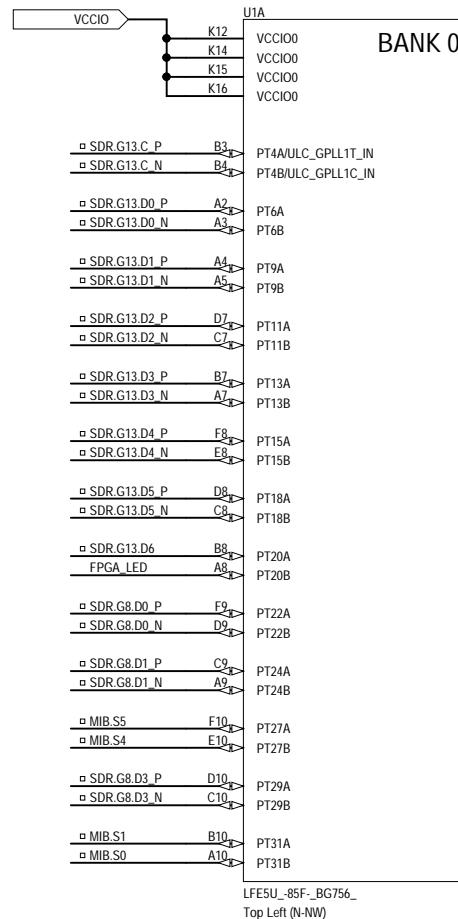
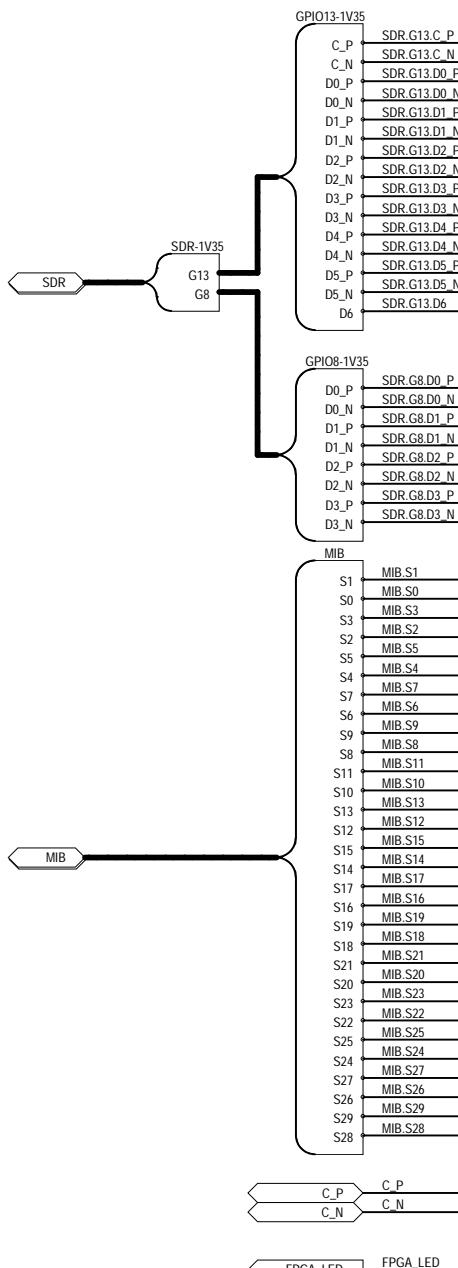
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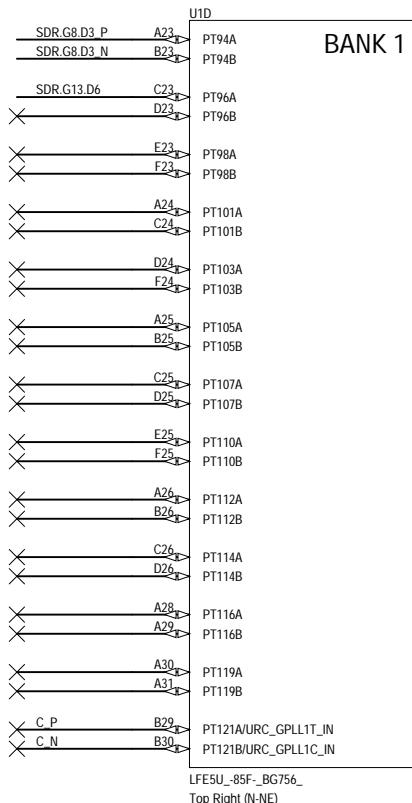
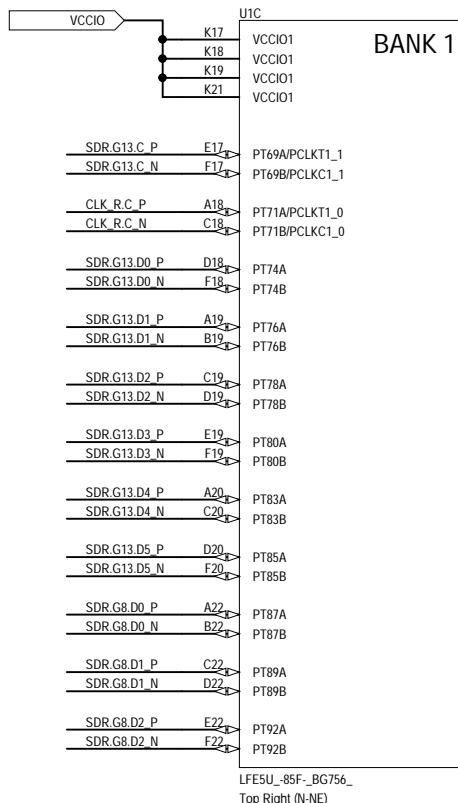
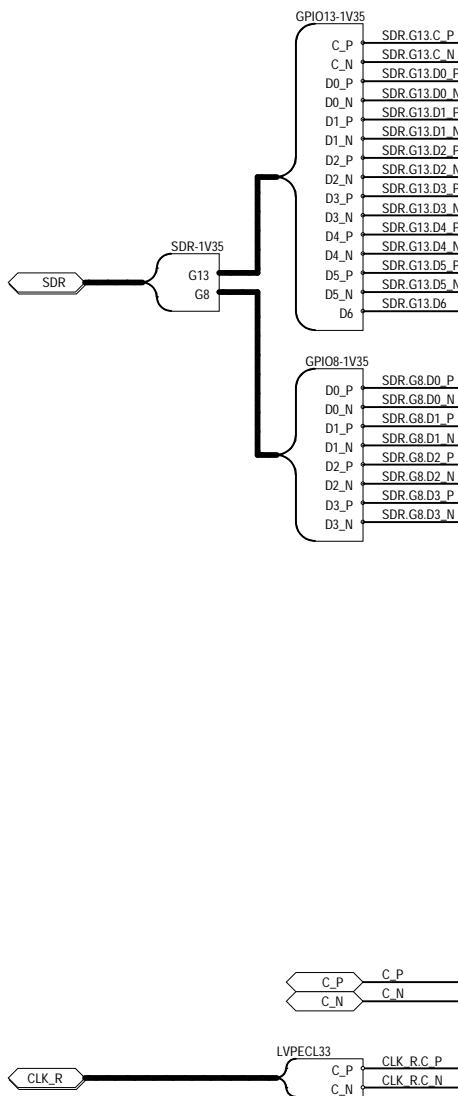
## Copper Suicide - FPGA

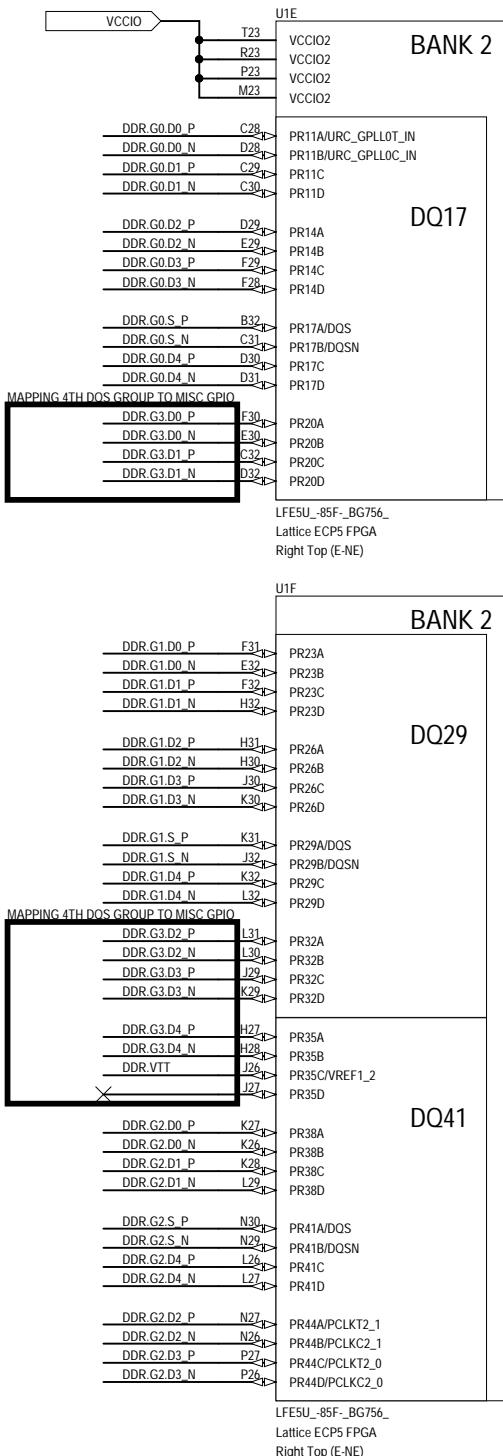
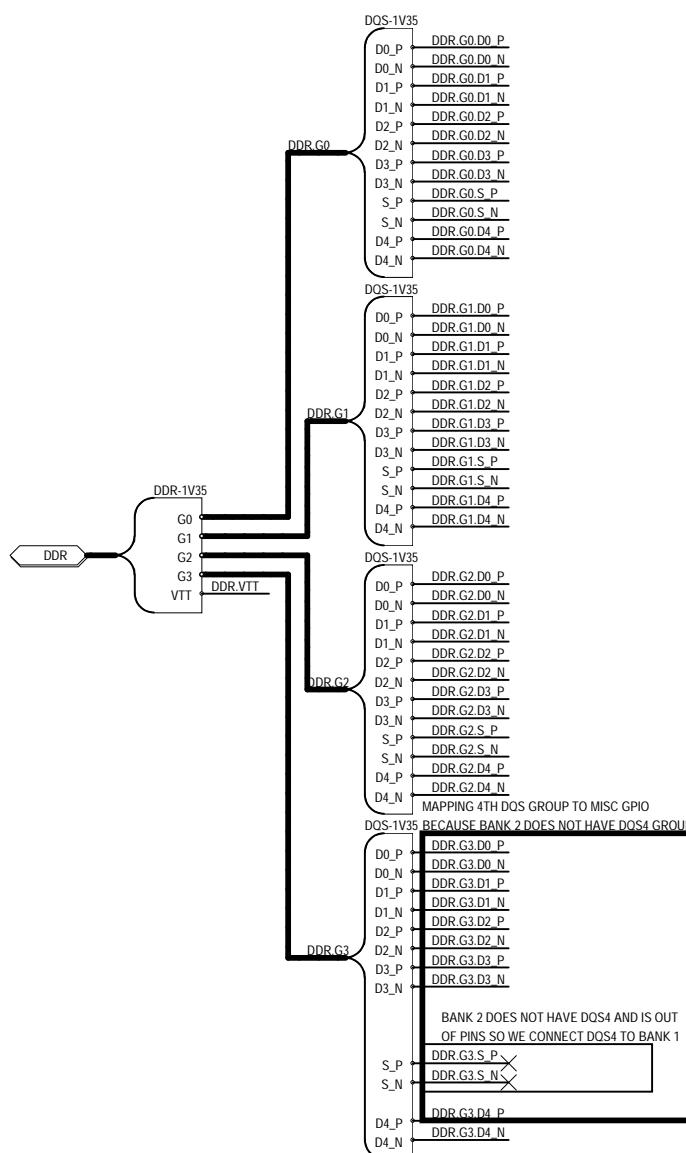


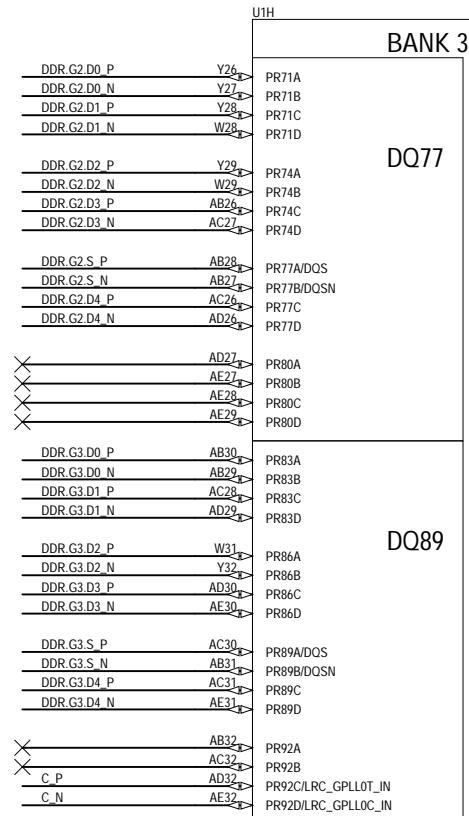
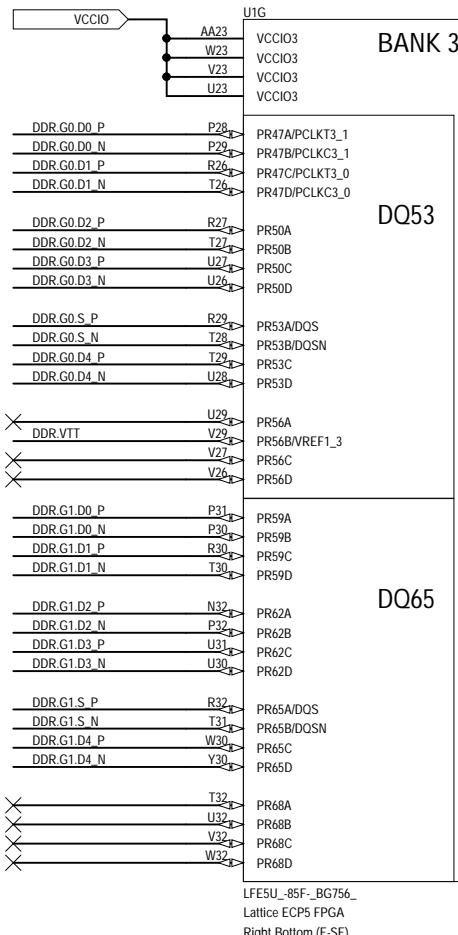
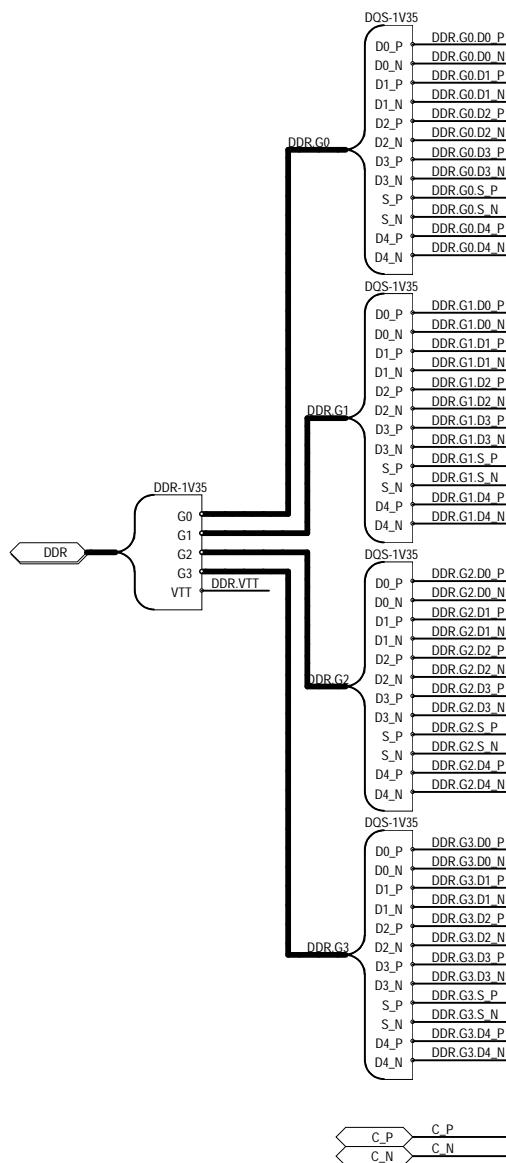
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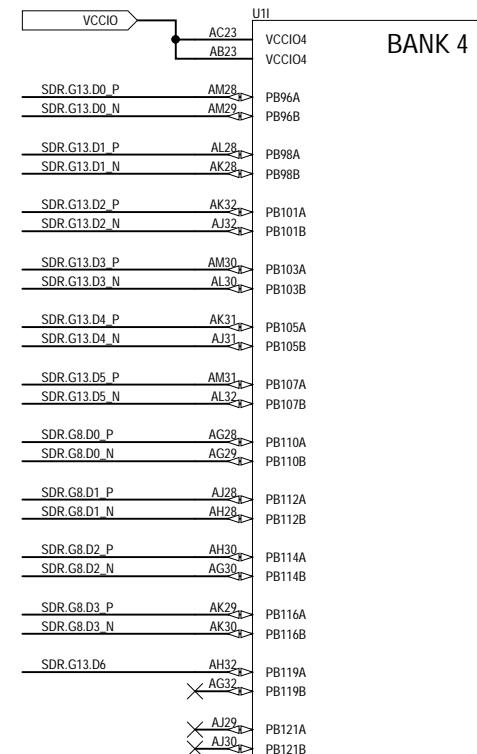
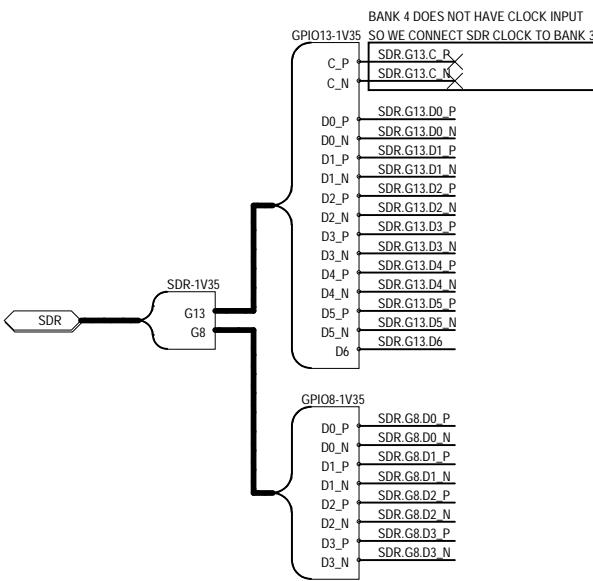
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 4 of 43	Date 12/31/2016



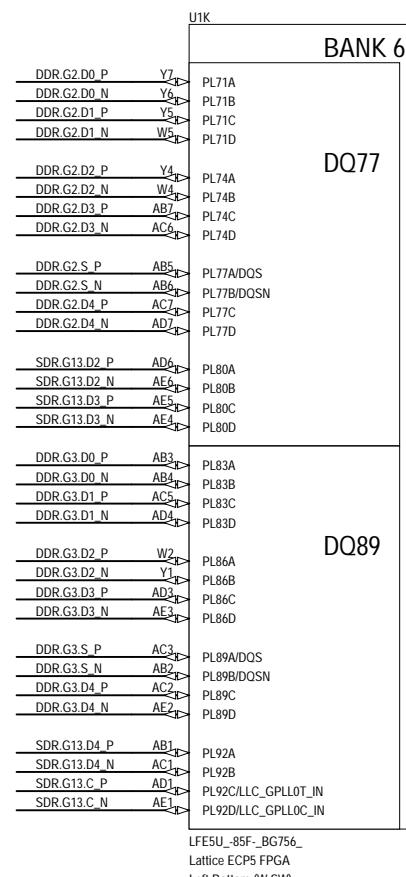
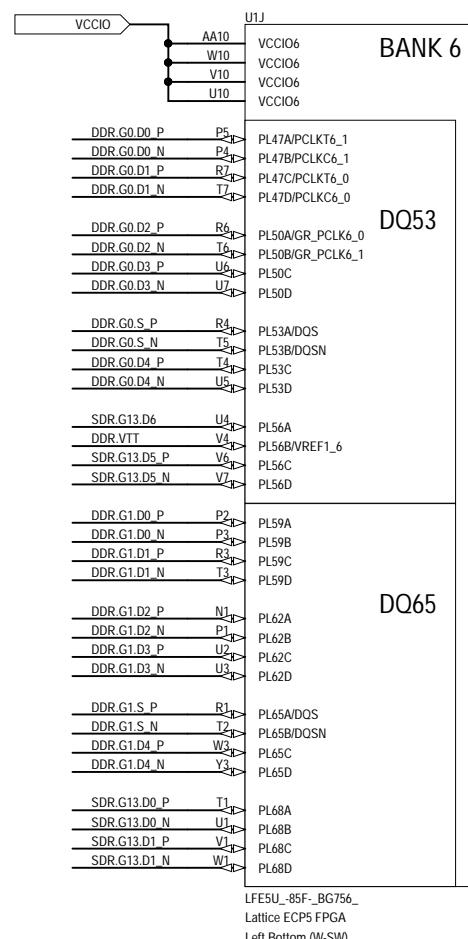
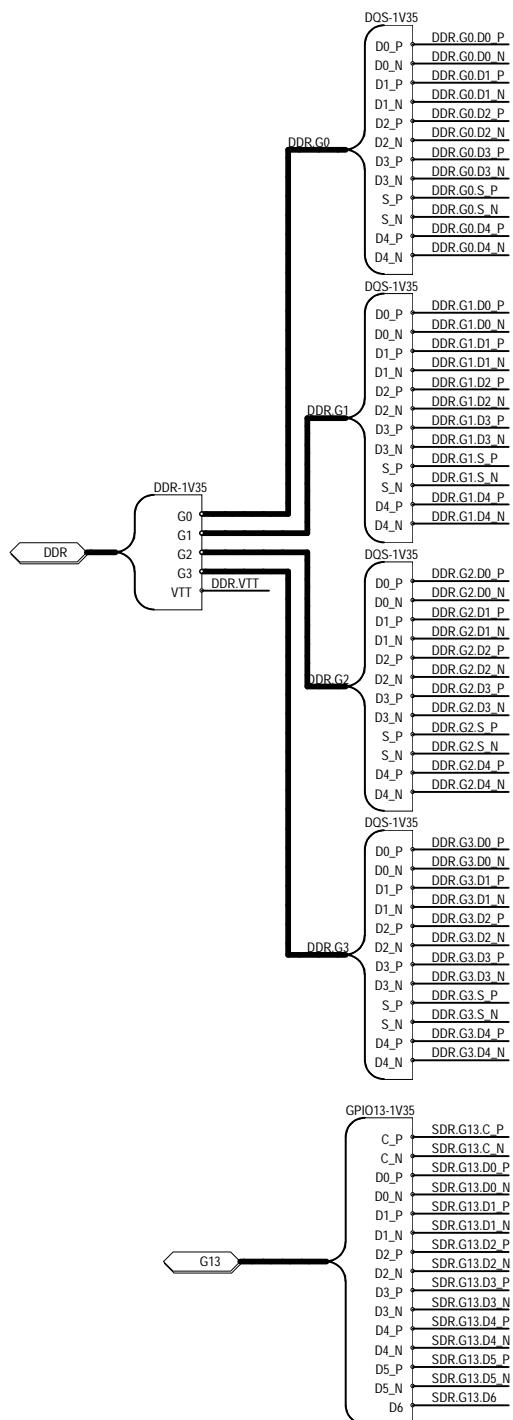


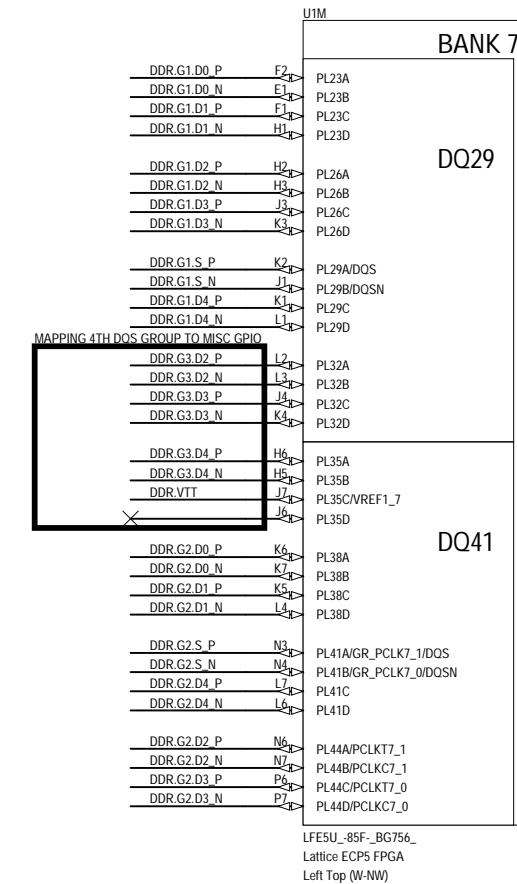
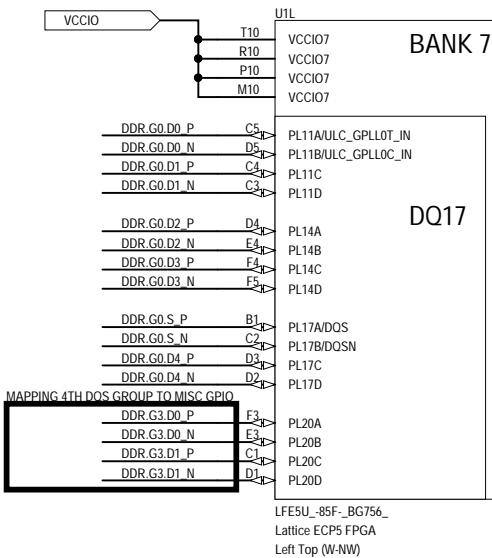
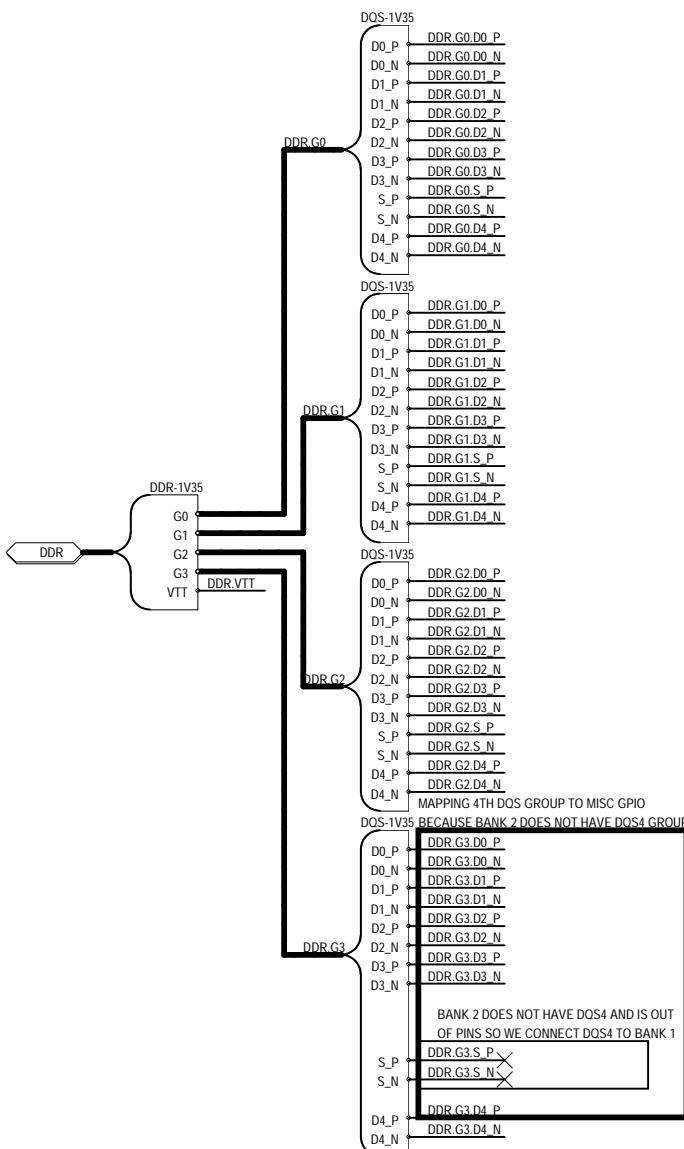




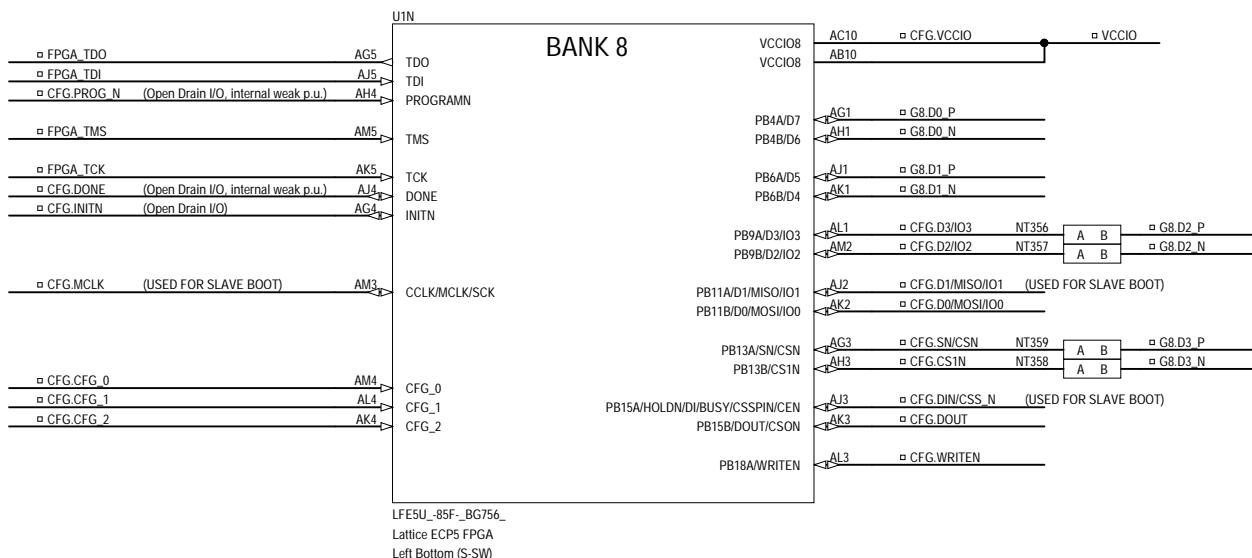
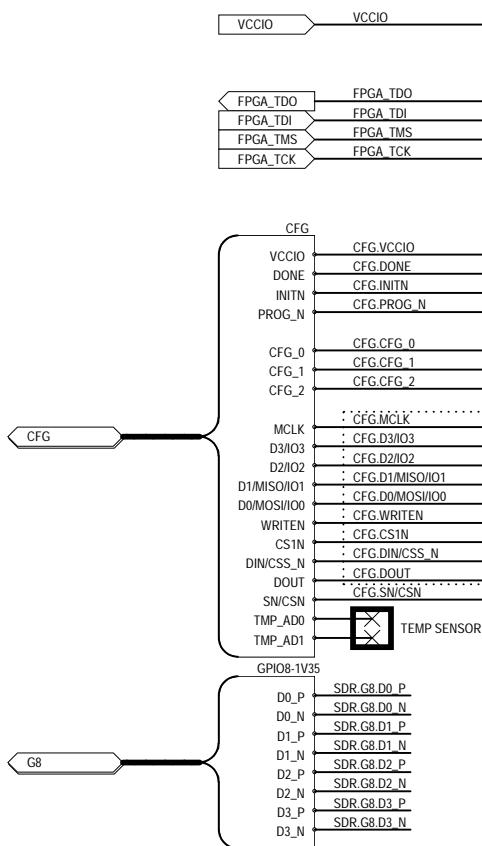


LFE5U-85F-BG756  
Lattice ECP5 FPGA  
Right Bottom (S-SE)





A



A

B

C

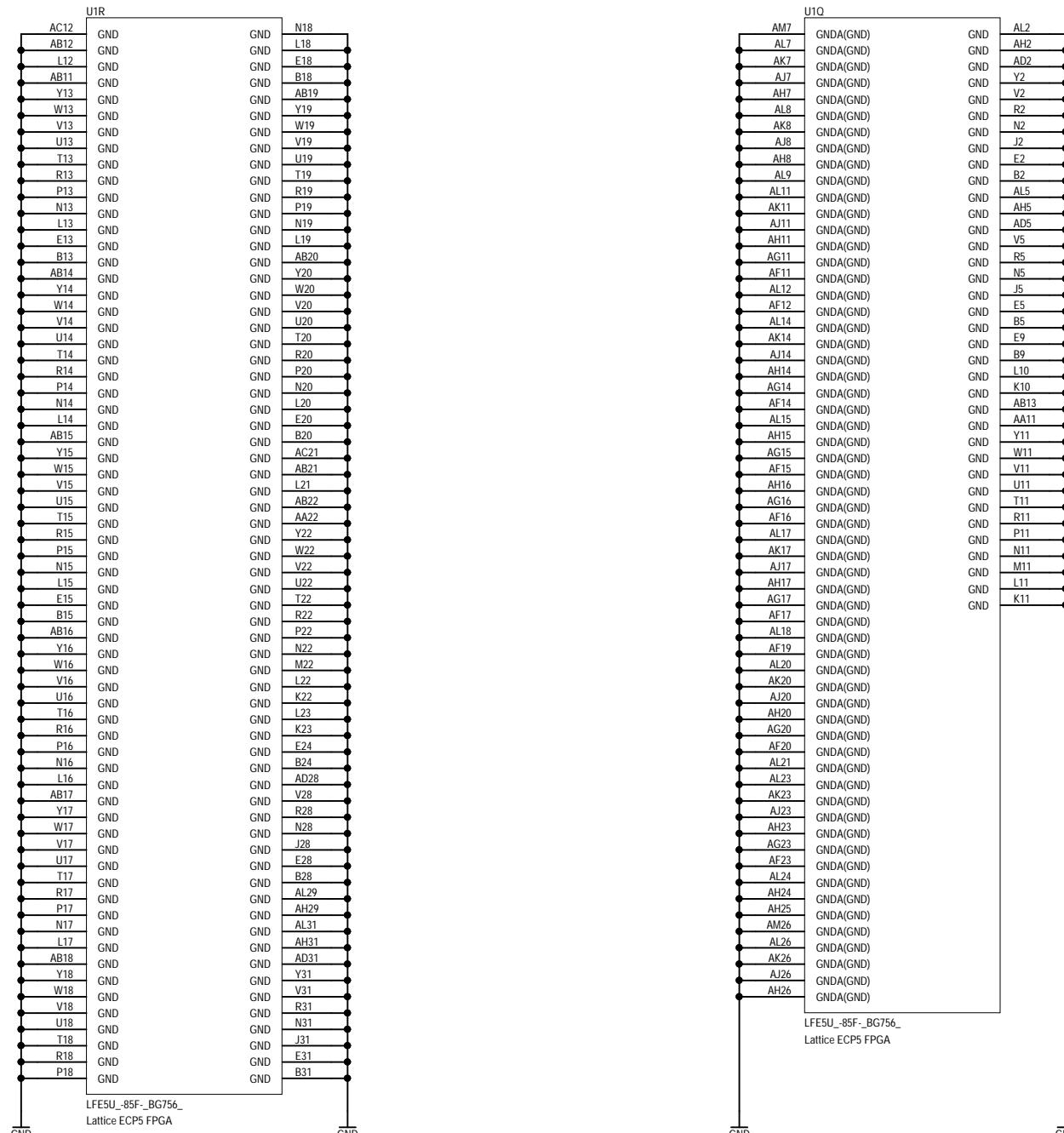
D

A

B

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D



Copper Suicide - FPGA - Ground		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 13 of 43	Date 12/31/2016

A

A

B

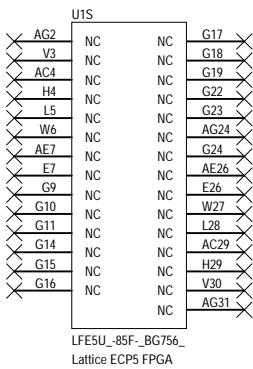
B

C

C

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D



Title		
Copper Suicide - FPGA - Misc		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 14 of 43	Date 12/31/2016

A

A

B

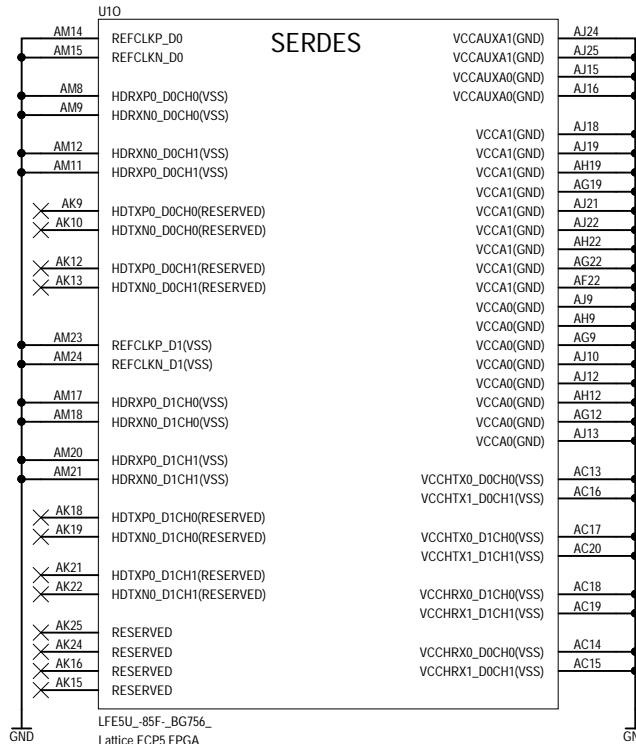
B

C

C

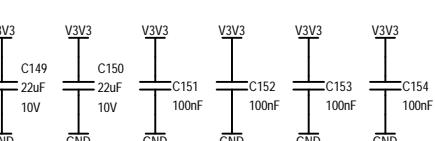
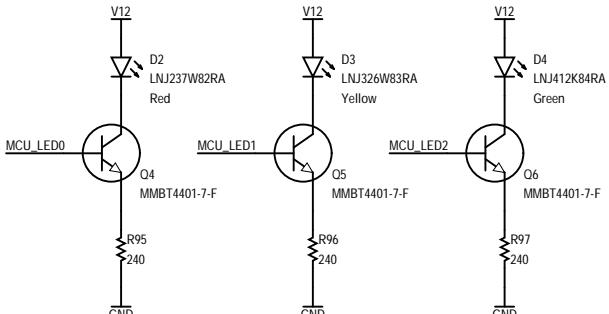
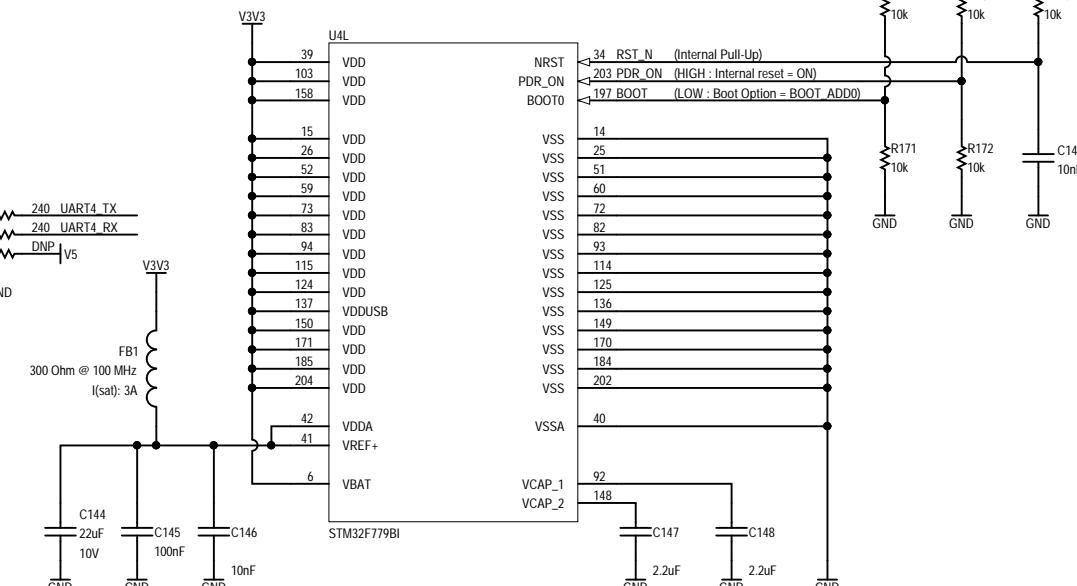
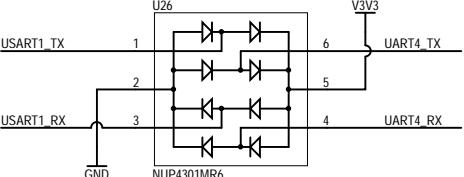
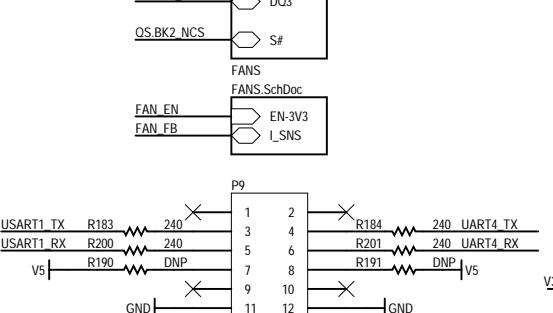
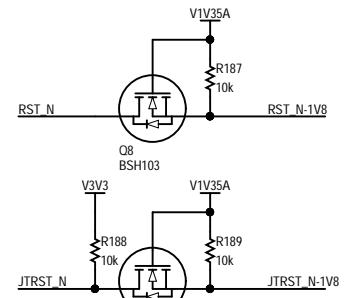
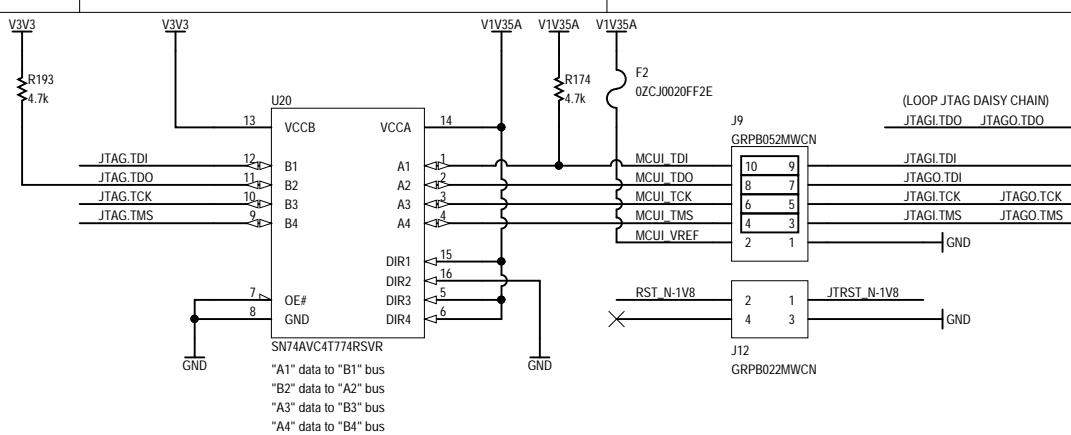
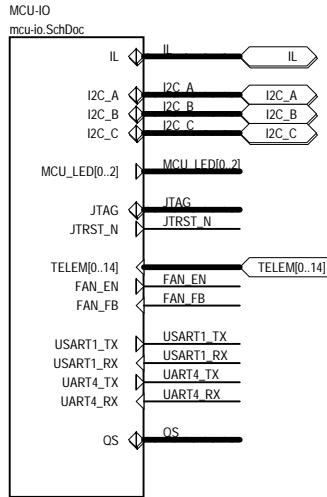
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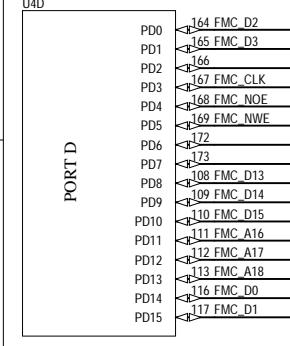
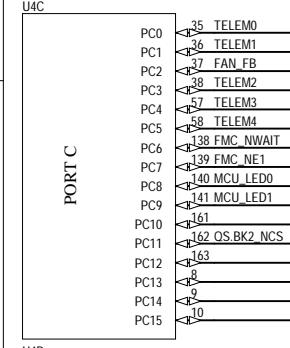
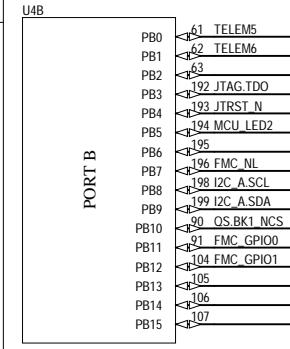
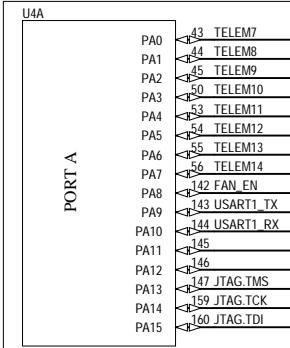


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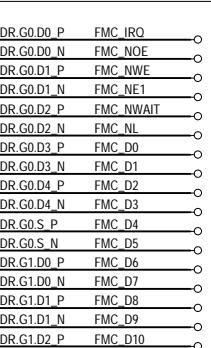
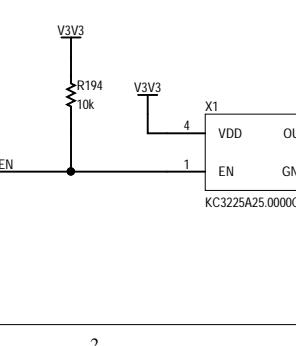
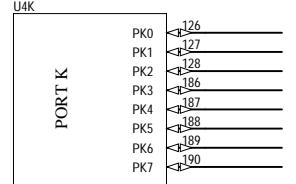
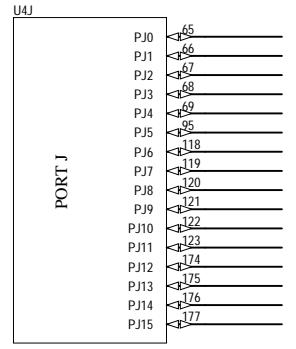
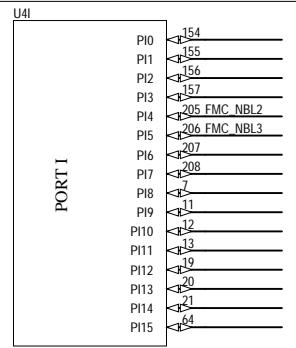
Title		
Copper Suicide - FPGA - SERDES		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 15 of 43	Date 12/31/2016



1 2 3 4

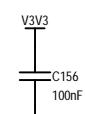
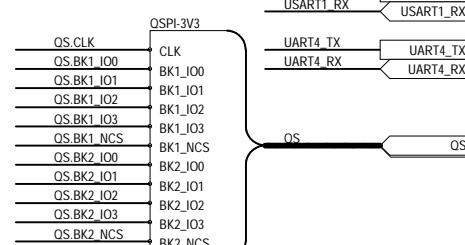
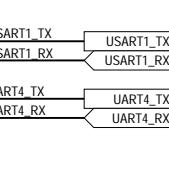
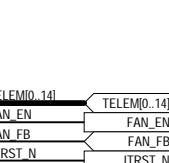
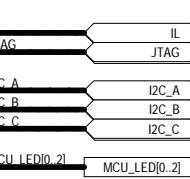
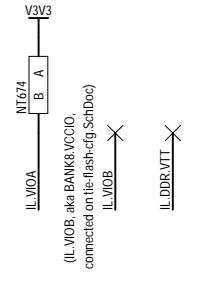


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1 2 3 4

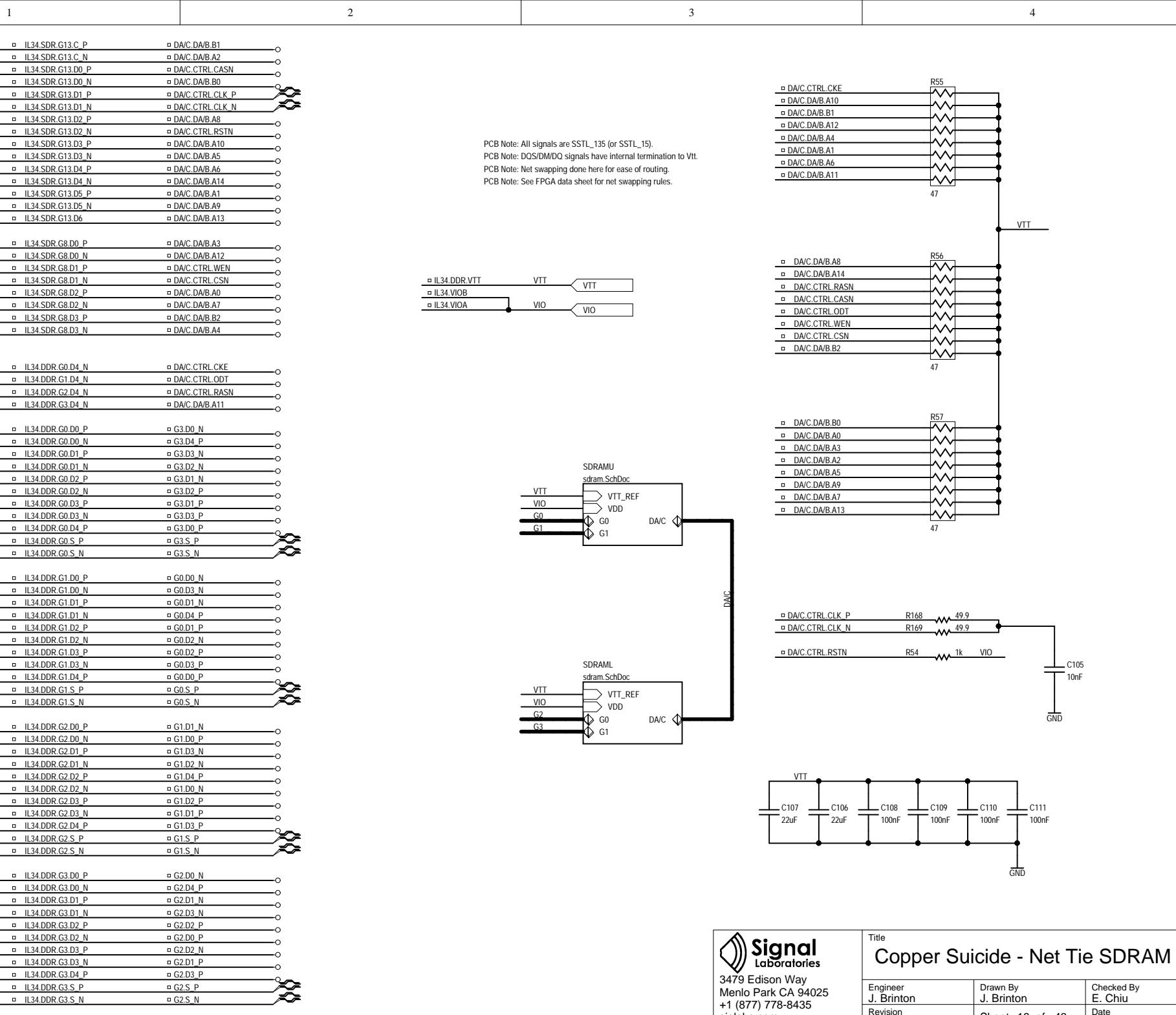
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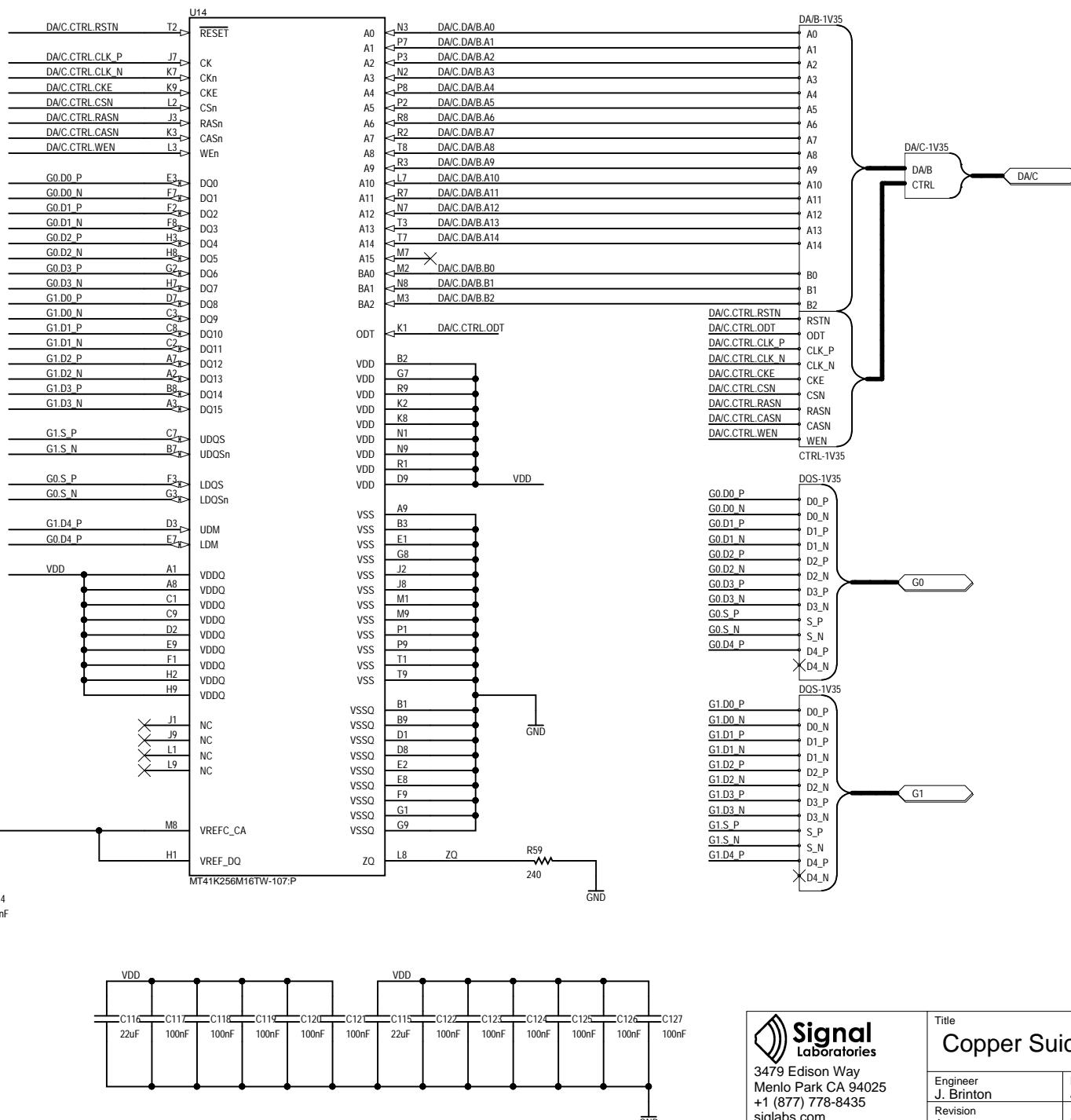


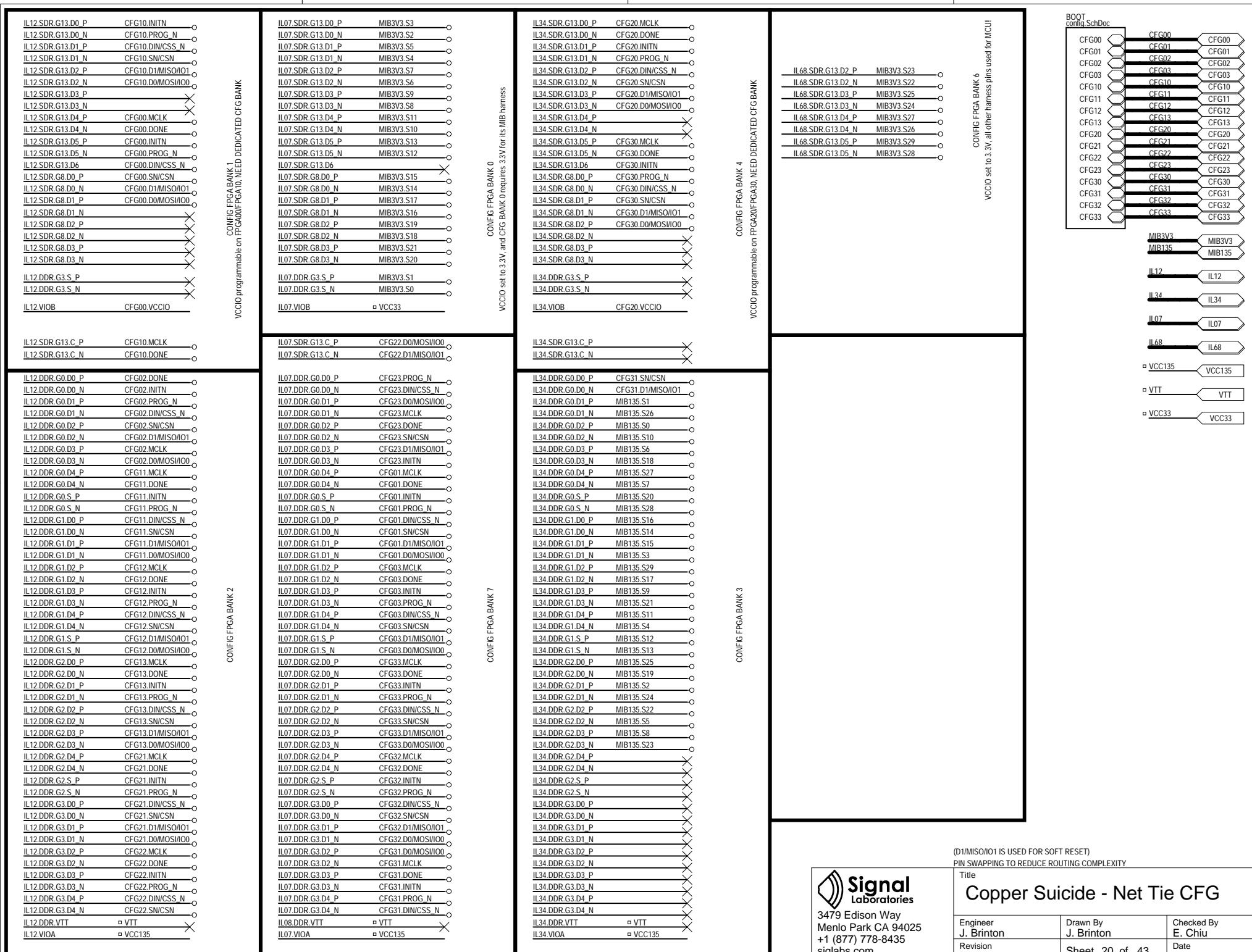
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Title Copper Suicide - MCU - I/O		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 17 of 43	Date 12/31/2016

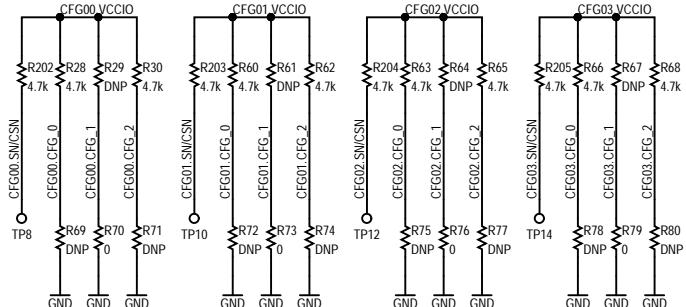
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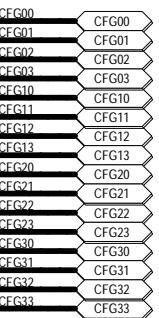


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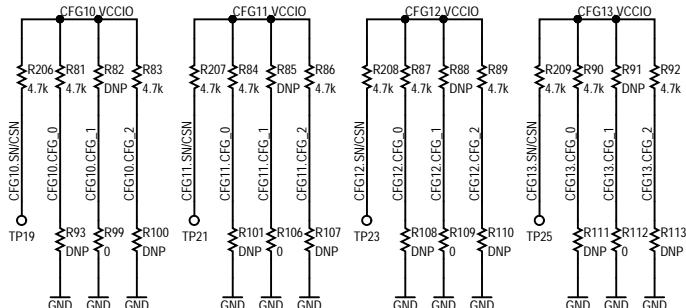


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CFG00.TMP_ADI	NT636	A B	GND	
CFG01.TMP_ADO	NT637	A B	X	0b0x : 7'addr = 0x49
CFG01.TMP_ADI	NT638	A B	GND	
CFG02.TMP_ADO	NT639	A B	V3V3	0b01 : 7'addr = 0x4A
CFG02.TMP_ADI	NT640	A B	GND	
CFG03.TMP_ADO	NT640	A B	V3V3	0b10 : 7'addr = 0x4B
CFG03.TMP_ADI	NT641	A B	V3V3	
CFG10.TMP_ADO	NT642	A B	X	0b1x : 7'addr = 0x4C
CFG10.TMP_ADI	NT643	A B	V3V3	
CFG11.TMP_ADO	NT643	A B	V3V3	0b11 : 7'addr = 0x4D
CFG11.TMP_ADI	NT644	A B	V3V3	
CFG12.TMP_ADO	NT645	A B	GND	0bx0 : 7'addr = 0x4E
CFG12.TMP_ADI	NT646	A B	X	
CFG13.TMP_ADO	NT646	A B	V3V3	0bx1 : 7'addr = 0x4F
CFG13.TMP_ADI	NT647	A B	X	



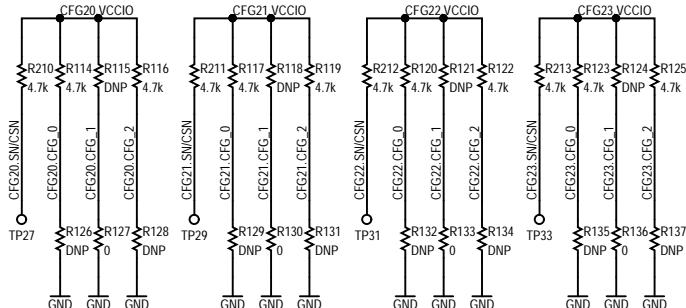
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## TEMP SENSOR I2C ADDRESS SELECT - I2C BUS B

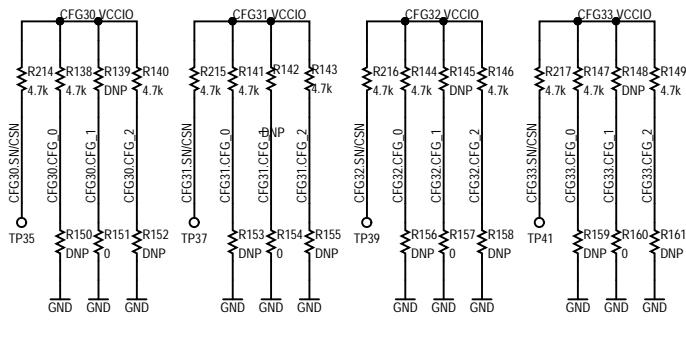
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CFG20.TMP_ADI	NT648	A B	GND	
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CFG21.TMP_ADI	NT650	A B	V3V3	0b01 : 7'addr = 0x4A
CFG22.TMP_ADO	NT651	A B	GND	
CFG22.TMP_ADI	NT652	A B	V3V3	0b10 : 7'addr = 0x4B
CFG23.TMP_ADO	NT653	A B	V3V3	
CFG23.TMP_ADI	NT654	A B	X	0b1x : 7'addr = 0x4C
CFG30.TMP_ADO	NT655	A B	V3V3	
CFG30.TMP_ADI	NT656	A B	V3V3	0b11 : 7'addr = 0x4D
CFG32.TMP_ADO	NT657	A B	GND	0bx0 : 7'addr = 0x4E
CFG32.TMP_ADI	NT658	A B	X	
CFG33.TMP_ADO	NT658	A B	V3V3	0bx1 : 7'addr = 0x4F

C

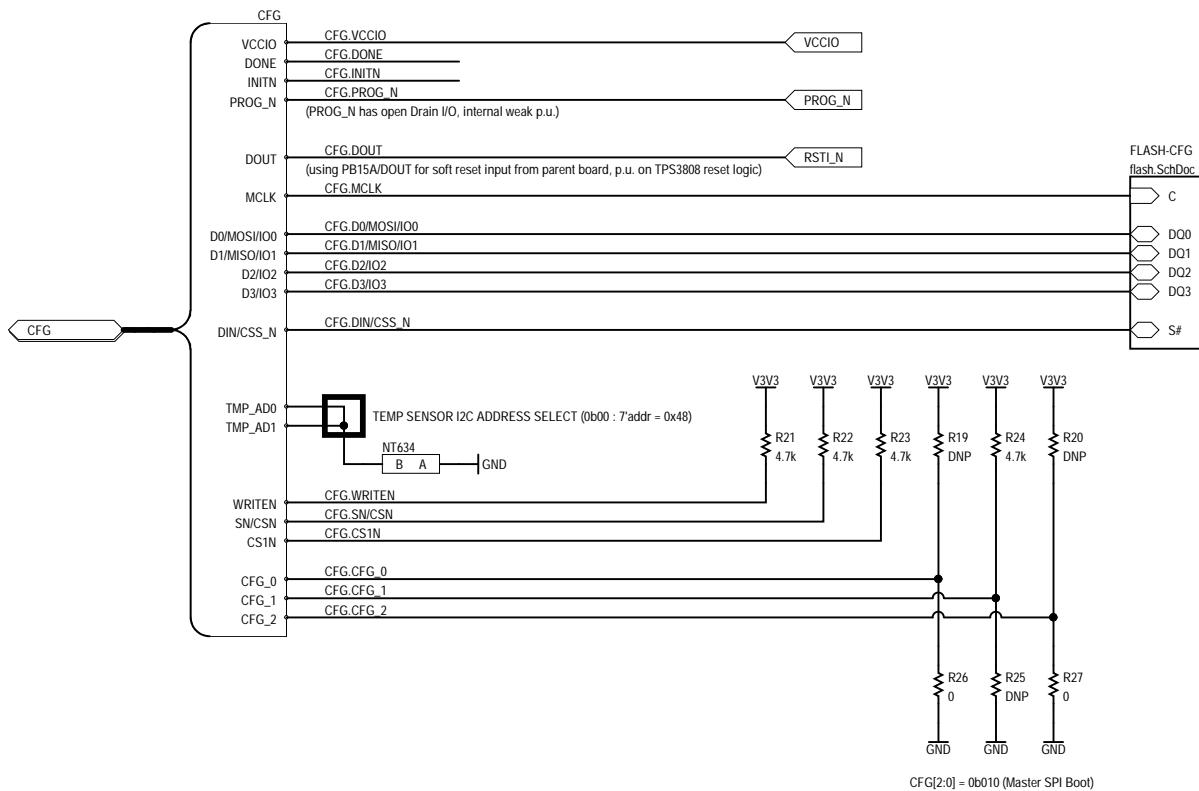
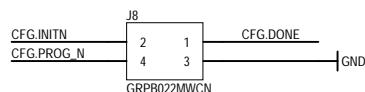


CFG00.SN/CSN	TP1
CFG00.MCLK	TP42
CFG00.DONE	TP43
CFG00.INITN	TP44
CFG00.PROG_N	TP45
CFG00.DIN/CSS_N	TP46
CFG00.D0/MOSI/IO0	TP47
CFG00.D1/MISO/I01	TP48
CFG00.DOUT	TP49
CFG00.WRITERN	TP50

PCB NOTE: PLACE NEXT TO FPGA #00



PCB NOTE: Place head next to JTAG per programming header



A

B

C

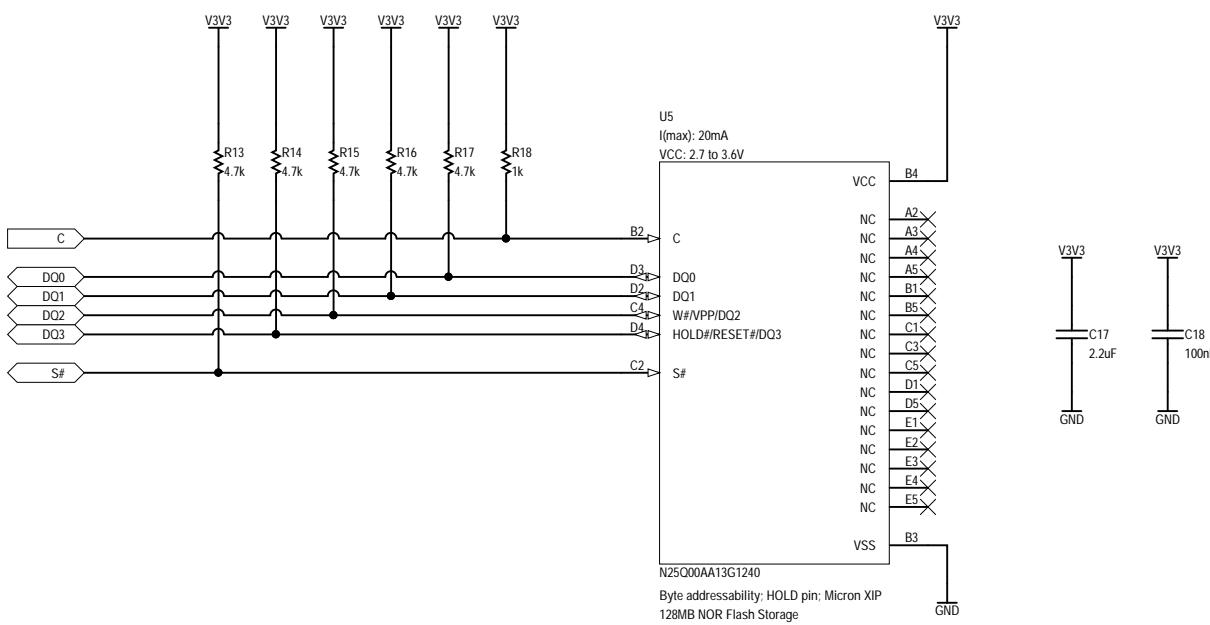
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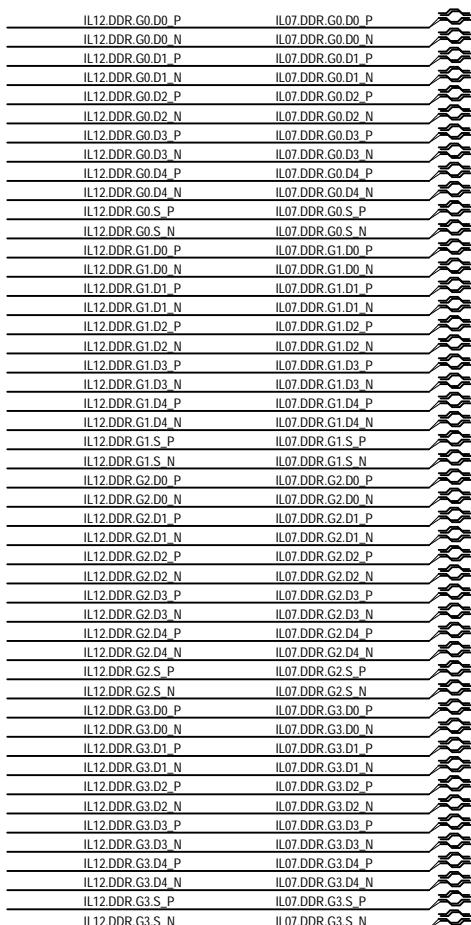
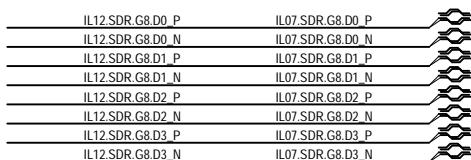
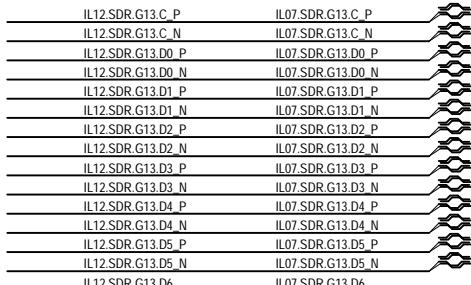
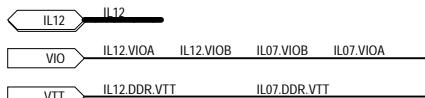
A

B

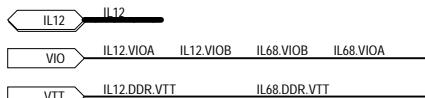
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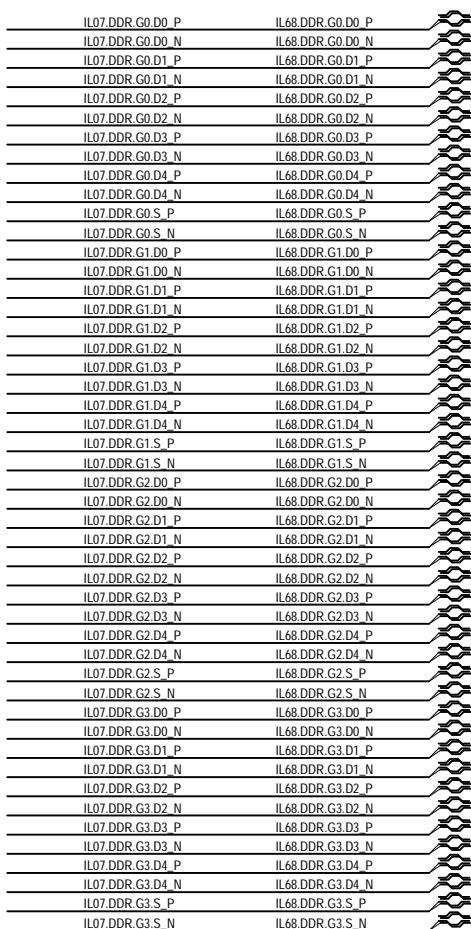
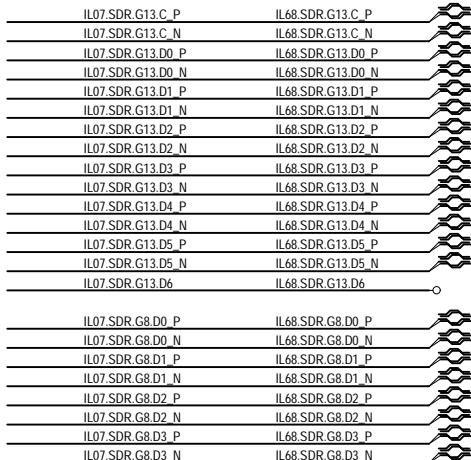
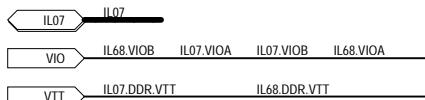




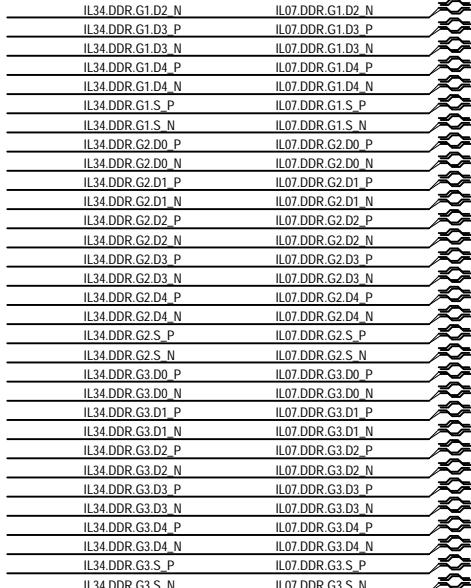
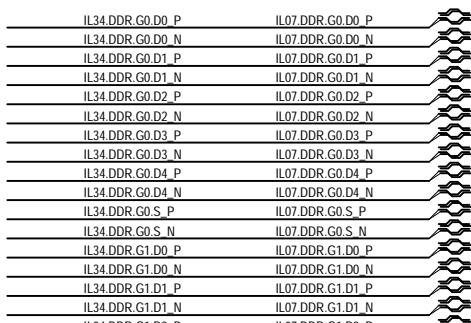
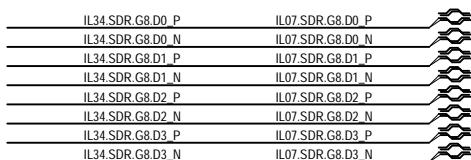
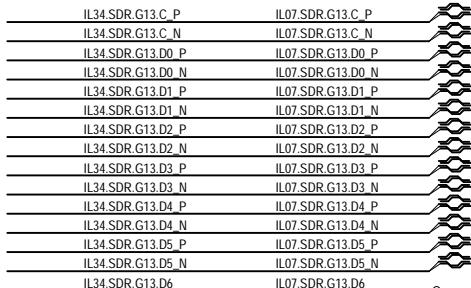
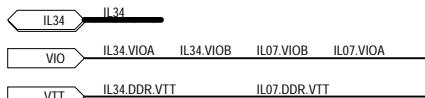
PIN SWAPPING TO REDUCE ROUTING COMPLEXITY



Copper Suicide - Net Tie 12:68		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 25 of 43	Date 12/31/2016



PIN SWAPPING TO REDUCE ROUTING COMPLEXITY



A

A

B

B

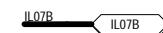
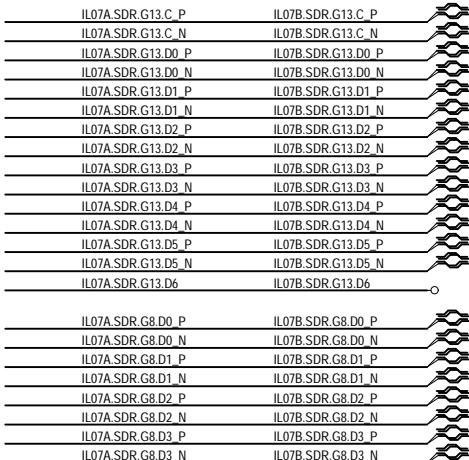
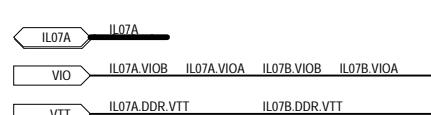
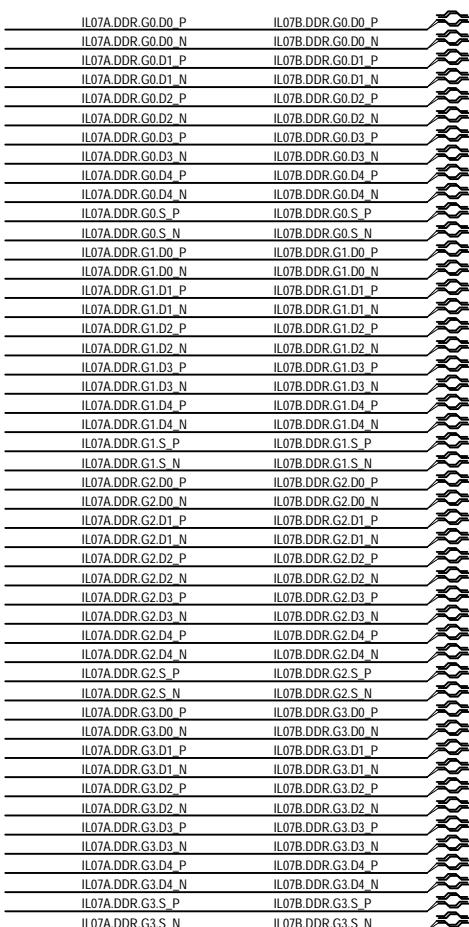
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C

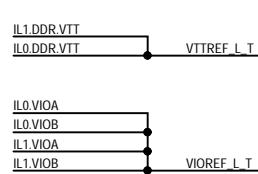
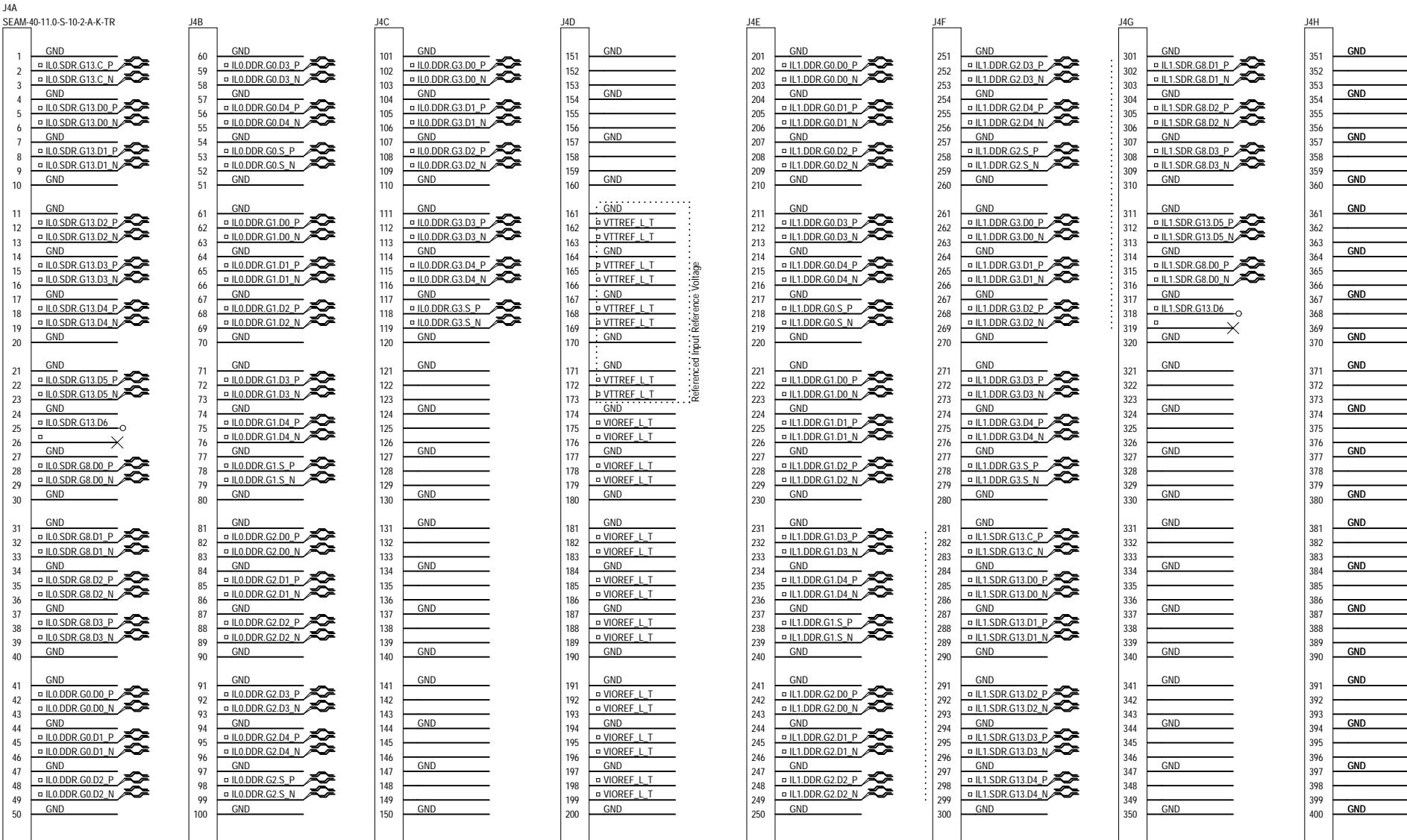
D

D

PIN SWAPPING TO REDUCE ROUTING COMPLEXITY

**A****A****B****B****C****C****D****D**

PIN SWAPPING TO REDUCE ROUTING COMPLEXITY

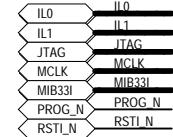


GND  
GND

 **Signal**  
Laboratories  
3479 Edison Way  
Menlo Park CA 94025  
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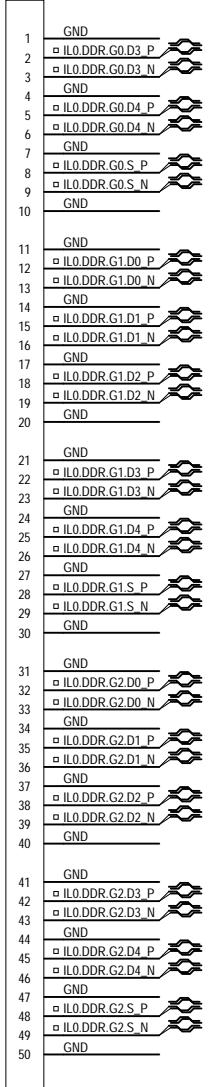
Title  
**Copper Suicide - Left Top**

Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 29 of 43	Date 12/31/2016

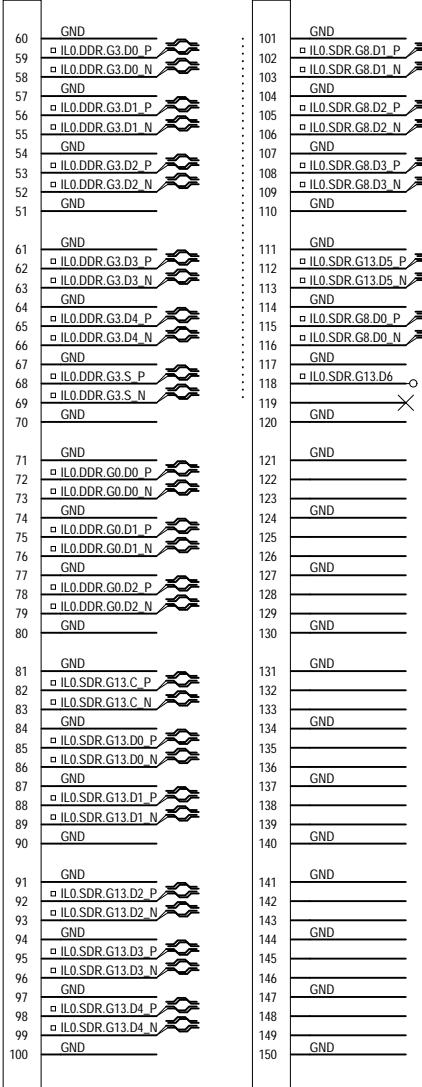


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V48BB

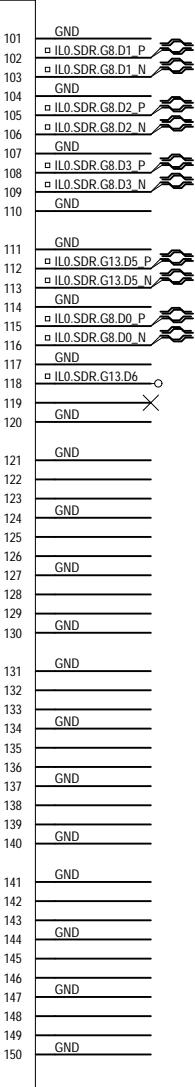
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SEAM-40-11.0-S-10-2-A-K-TR



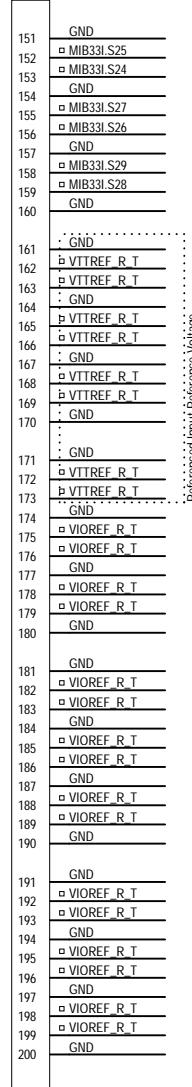
J3B



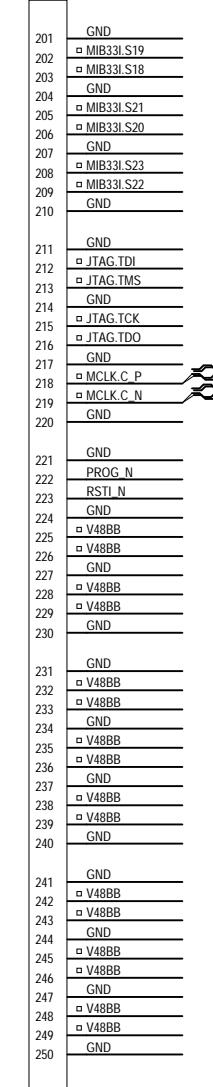
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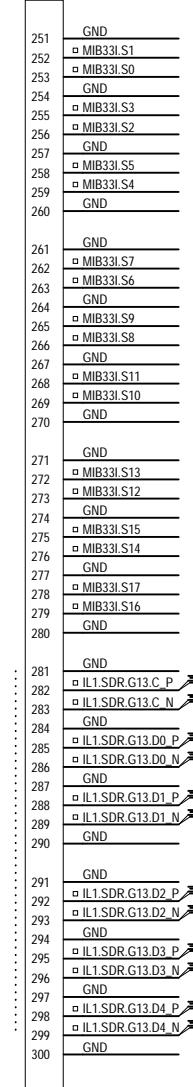
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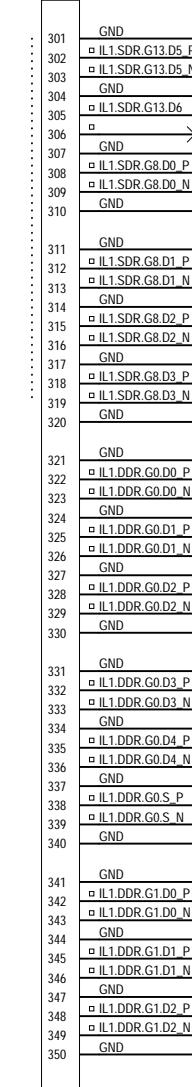
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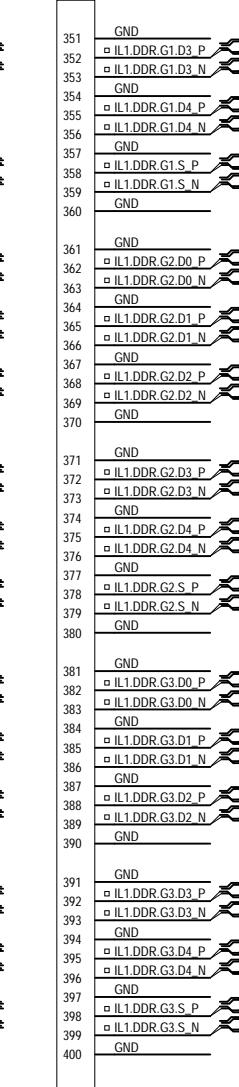
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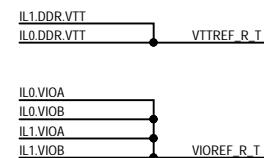
J3G



J3H



Referenced Input Reference Voltage



GND  
GND



## Copper Suicide - Right Top

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Title  
Engineer J. Brinton

Revision 1

Drawn By J. Brinton

Sheet 30 of 43

Checked By E. Chiu

Date 12/31/2016

J2A  
SEAF-40-06-S-10-2-A-K-TR

1 GND  
2 □ IL0.SDR.G13.C.P  
3 GND  
4 □ IL0.SDR.G13.D0.P  
5 □ IL0.SDR.G13.D0.N  
6 GND  
7 □ IL0.SDR.G13.D1.P  
8 □ IL0.SDR.G13.D1.N  
9 GND  
10 GND

11 GND  
12 □ IL0.SDR.G13.D2.P  
13 □ IL0.SDR.G13.D2.N  
14 GND  
15 □ IL0.SDR.G13.D3.P  
16 □ IL0.SDR.G13.D3.N  
17 GND  
18 □ IL0.SDR.G13.D4.P  
19 □ IL0.SDR.G13.D4.N  
20 GND

21 GND  
22 □ IL0.SDR.G13.D5.P  
23 □ IL0.SDR.G13.D5.N  
24 GND  
25 □ IL0.SDR.G13.D6  
26 GND  
27 □ IL0.SDR.G8.D0.P  
28 □ IL0.SDR.G8.D0.N  
29 GND  
30 GND

31 GND  
32 □ IL0.SDR.G8.D1.P  
33 □ IL0.SDR.G8.D1.N  
34 GND  
35 □ IL0.SDR.G8.D2.P  
36 □ IL0.SDR.G8.D2.N  
37 GND  
38 □ IL0.SDR.G8.D3.P  
39 □ IL0.SDR.G8.D3.N  
40 GND

41 GND  
42 □ IL0.DDR.G0.D0.P  
43 □ IL0.DDR.G0.D0.N  
44 GND  
45 □ IL0.DDR.G0.D1.P  
46 □ IL0.DDR.G0.D1.N  
47 GND  
48 □ IL0.DDR.G0.D2.P  
49 □ IL0.DDR.G0.D2.N  
50 GND

J2B

60 GND  
59 □ IL0.DDR.G0.D3.P  
58 GND  
57 □ IL0.DDR.G0.D3.N  
56 GND  
55 □ IL0.DDR.G0.D4.P  
54 GND  
53 □ IL0.DDR.G0.S.P  
52 GND  
51 GND

61 GND  
62 □ IL0.DDR.G1.D0.P  
63 □ IL0.DDR.G1.D0.N  
64 GND  
65 □ IL0.DDR.G1.D1.P  
66 □ IL0.DDR.G1.D1.N  
67 GND  
68 □ IL0.DDR.G1.D2.P  
69 □ IL0.DDR.G1.D2.N  
70 GND

71 GND  
72 □ IL0.DDR.G1.D3.P  
73 □ IL0.DDR.G1.D3.N  
74 GND  
75 □ IL0.DDR.G1.D4.P  
76 GND  
77 □ IL0.DDR.G1.S.P  
78 □ IL0.DDR.G1.S.N  
79 □ IL0.DDR.G1.S.N  
80 GND

81 GND  
82 □ IL0.DDR.G2.D0.P  
83 □ IL0.DDR.G2.D0.N  
84 GND  
85 □ IL0.DDR.G2.D1.P  
86 GND  
87 □ IL0.DDR.G2.D2.P  
88 □ IL0.DDR.G2.D2.N  
89 GND  
90 GND

91 GND  
92 □ IL0.DDR.G2.D3.P  
93 □ IL0.DDR.G2.D3.N  
94 GND  
95 □ IL0.DDR.G2.D4.P  
96 GND  
97 □ IL0.DDR.G2.S.P  
98 □ IL0.DDR.G2.S.N  
99 □ IL0.DDR.G2.S.N  
100 GND

J2C

101 GND  
102 □ IL0.DDR.G3.D0.P  
103 □ IL0.DDR.G3.D0.N  
104 GND  
105 □ IL0.DDR.G3.D1.P  
106 □ IL0.DDR.G3.D1.N  
107 GND  
108 □ IL0.DDR.G3.D2.P  
109 □ IL0.DDR.G3.D2.N  
110 GND

111 GND  
112 □ IL0.DDR.G3.D3.P  
113 □ IL0.DDR.G3.D3.N  
114 GND  
115 □ IL0.DDR.G3.D4.P  
116 □ IL0.DDR.G3.D4.N  
117 GND  
118 □ IL0.DDR.G3.S.P  
119 □ IL0.DDR.G3.S.N  
120 GND

121 GND  
122 □ IL0.VTREF.L.B  
123 GND  
124 GND  
125 □ IL0.VTREF.L.B  
126 GND  
127 □ IL0.VTREF.L.B  
128 GND  
129 □ IL0.VTREF.L.B  
130 GND

131 GND  
132 □ IL0.VTREF.L.B  
133 GND  
134 GND  
135 □ IL0.VTREF.L.B  
136 GND  
137 □ IL0.VTREF.L.B  
138 GND  
139 □ IL0.VTREF.L.B  
140 GND

141 GND  
142 □ IL0.VTREF.L.B  
143 GND  
144 GND  
145 □ IL0.VTREF.L.B  
146 GND  
147 □ IL0.VTREF.L.B  
148 GND  
149 □ IL0.VTREF.L.B  
150 GND

J2D

151 GND  
152 GND  
153 GND  
154 GND  
155 GND  
156 GND  
157 GND  
158 GND  
159 GND  
160 GND

161 GND  
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164 GND  
165 □ IL1.DDR.G0.D4.P  
166 □ IL1.DDR.G0.D4.N  
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168 □ IL1.DDR.G0.L.B  
169 □ IL1.DDR.G0.S.N  
170 GND

171 GND  
172 □ IL1.DDR.G1.D0.P  
173 □ IL1.DDR.G1.D0.N  
174 GND  
175 □ IL1.VOREF.L.B  
176 □ IL1.VOREF.L.B  
177 GND  
178 □ IL1.VOREF.L.B  
179 □ IL1.VOREF.L.B  
180 GND

181 GND  
182 □ IL1.VOREF.L.B  
183 □ IL1.VOREF.L.B  
184 GND  
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187 □ IL1.VOREF.L.B  
188 □ IL1.VOREF.L.B  
189 □ IL1.VOREF.L.B  
190 GND

191 GND  
192 □ IL1.VOREF.L.B  
193 GND  
194 GND  
195 □ IL1.VOREF.L.B  
196 GND  
197 □ IL1.VOREF.L.B  
198 □ IL1.VOREF.L.B  
199 □ IL1.VOREF.L.B  
200 GND

J2E

201 GND  
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204 GND  
205 □ IL1.DDR.G0.D1.P  
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208 □ IL1.DDR.G0.D2.P  
209 □ IL1.DDR.G0.D2.N  
210 GND

211 GND  
212 □ IL1.DDR.G0.D3.P  
213 □ IL1.DDR.G0.D3.N  
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219 □ IL1.DDR.G0.S.N  
220 GND

221 GND  
222 □ IL1.DDR.G1.D0.P  
223 □ IL1.DDR.G1.D0.N  
224 GND  
225 □ IL1.DDR.G1.D1.P  
226 □ IL1.DDR.G1.D1.N  
227 GND  
228 □ IL1.DDR.G1.D2.P  
229 □ IL1.DDR.G1.D2.N  
230 GND

231 GND  
232 □ IL1.DDR.G1.D3.P  
233 □ IL1.DDR.G1.D3.N  
234 GND  
235 □ IL1.DDR.G1.D4.P  
236 GND  
237 □ IL1.DDR.G1.S.P  
238 □ IL1.DDR.G1.S.N  
239 GND  
240 GND

241 GND  
242 □ IL1.DDR.G2.D0.P  
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246 GND  
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J2F

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270 GND

271 GND  
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290 GND

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293 □ IL1.SDR.G13.D2.N  
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295 □ IL1.SDR.G13.D3.P  
296 GND  
297 □ IL1.SDR.G13.D4.P  
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300 GND

J2G

301 GND  
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310 GND

311 GND  
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320 GND

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324 GND  
325 □ IL1.SDR.G3.D4.P  
326 □ IL1.SDR.G3.D4.N  
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328 □ IL1.SDR.G3.S.P  
329 □ IL1.SDR.G3.S.N  
330 GND

331 GND  
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333 □ IL1.SDR.G13.C.N  
334 GND  
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337 GND  
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343 □ IL1.SDR.G13.D2.N  
344 GND  
345 □ IL1.SDR.G13.D3.P  
346 □ IL1.SDR.G13.D3.N  
347 GND  
348 □ IL1.SDR.G13.D4.P  
349 □ IL1.SDR.G13.D4.N  
350 GND

J2H

351 GND  
352 GND  
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397 GND  
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400 GND

Referenzinput Referenz-Voltages



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IL0.DDR.VTT  
VTTREF.L.B

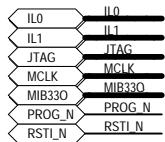
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IL0.VIOB  
IL1.VIOA  
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VIOREF.L.B



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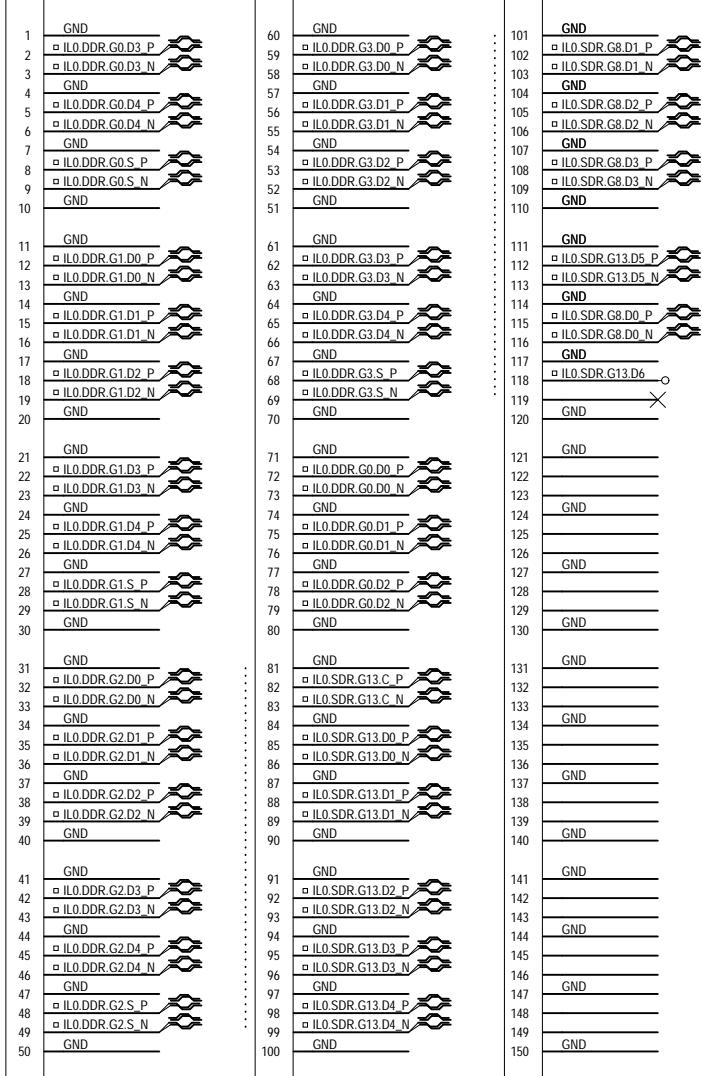
## Copper Suicide - Left Bottom

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision 1	Sheet 31 of 43	Date 12/31/2016



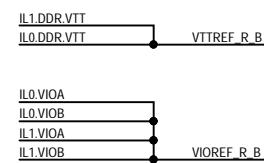
V48BB  
V48BB

J1A  
SEAF-40-06-S-10-2-A-K-TR



Referenz-Eingang Referenz-Voltages

GND  
GND

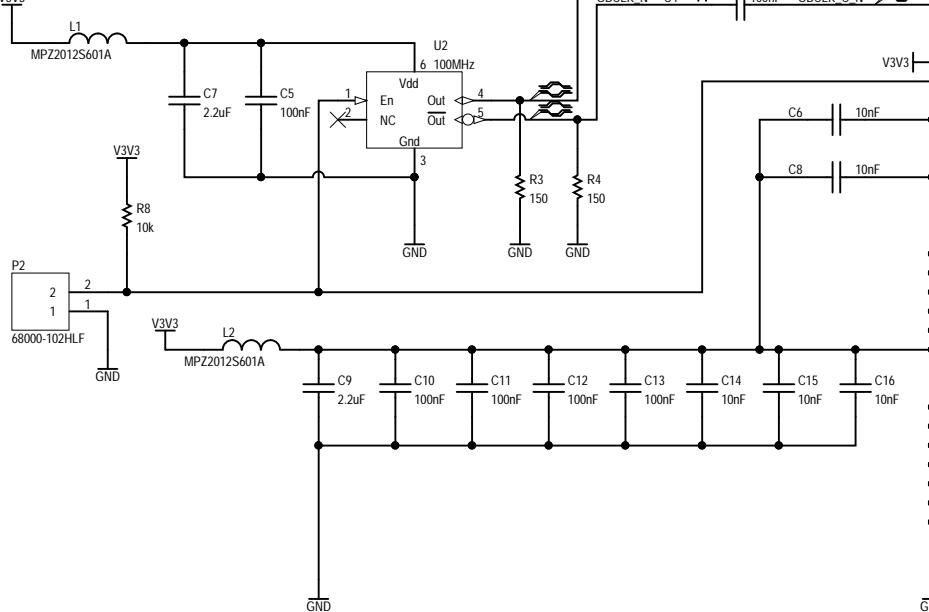


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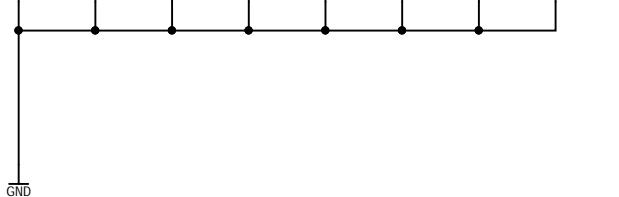
## Title Copper Suicide - Right Bottom

Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 32 of 43	Date 12/31/2016

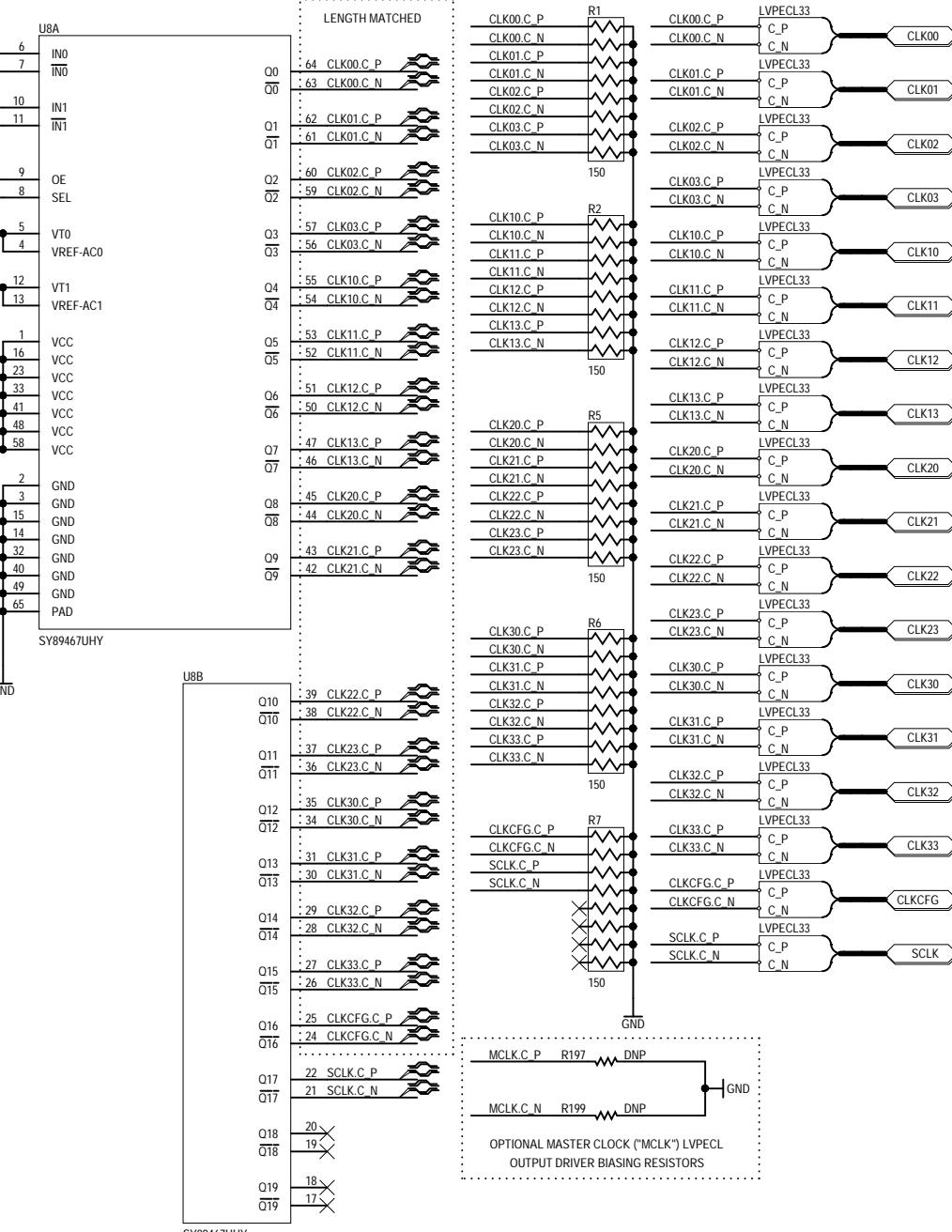
A



B



C



D

REVIEW COMPLETE: JDB 10/7/2016



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## Copper Suicide - Clock Fanout

Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 33 of 43	Date 12/31/2016

A

A

B

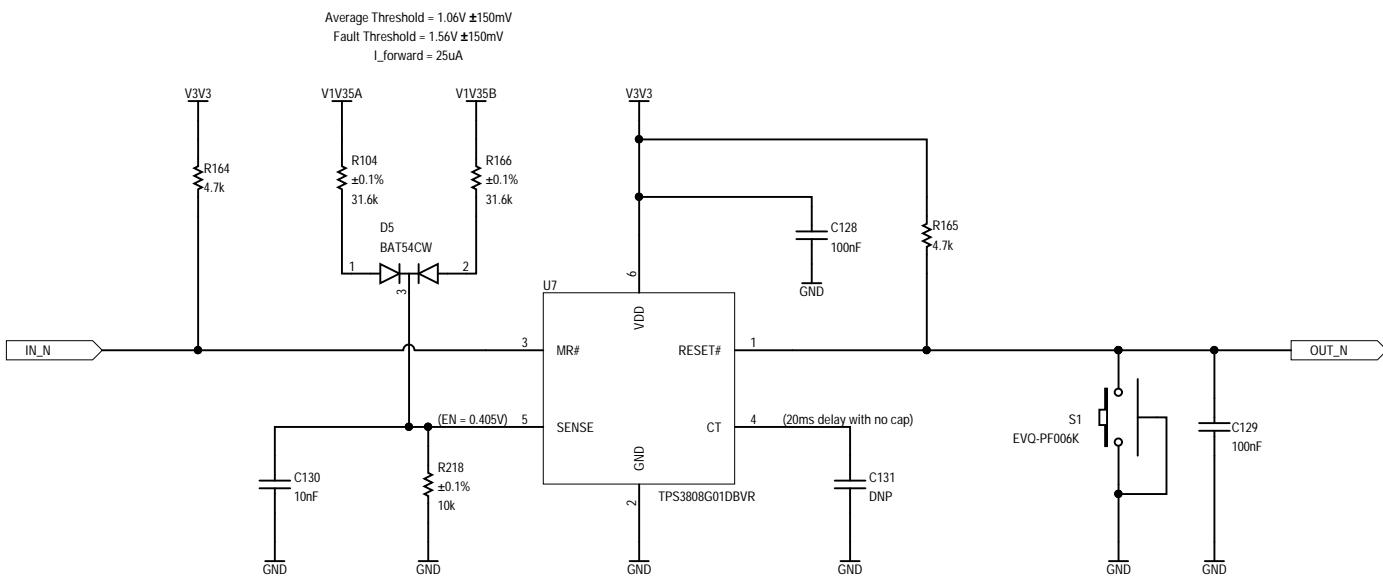
B

C

C

D

D



A

B

C

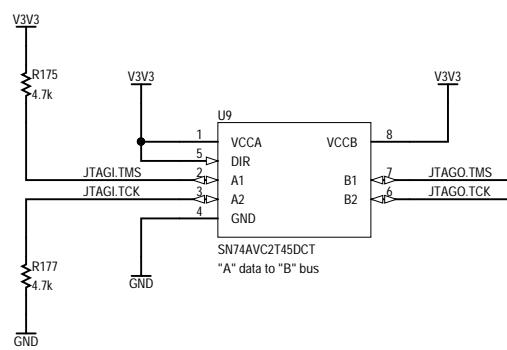
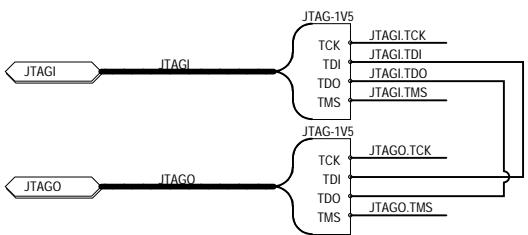
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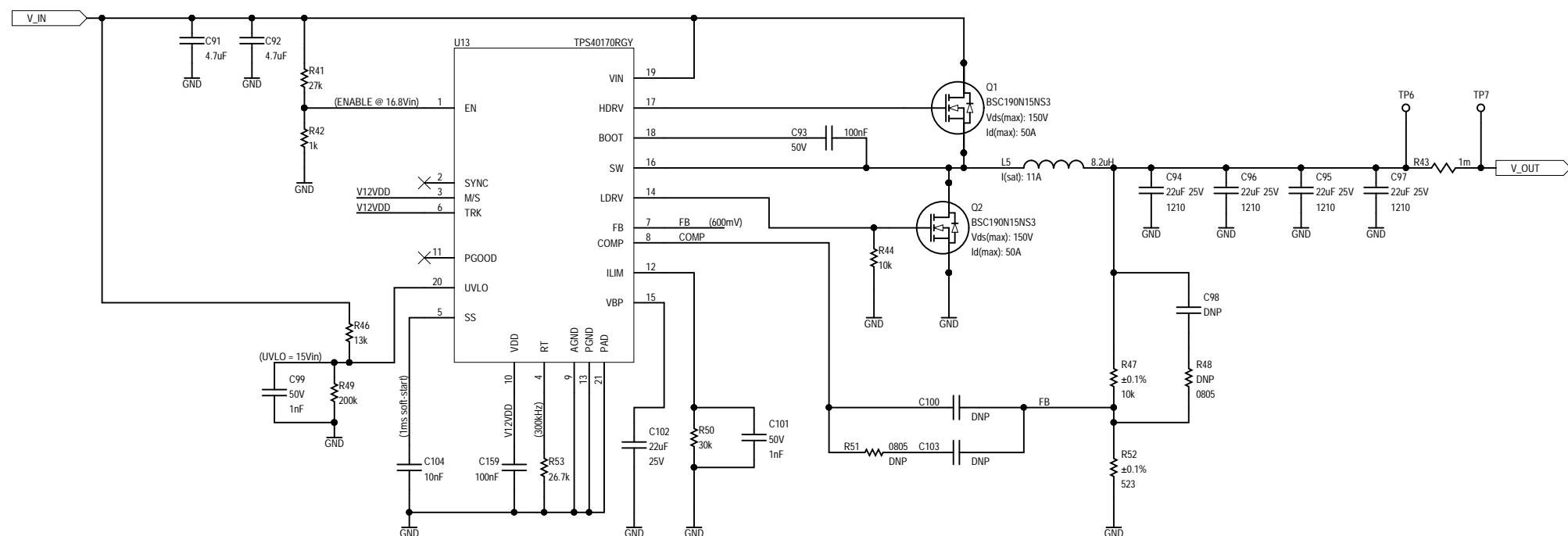
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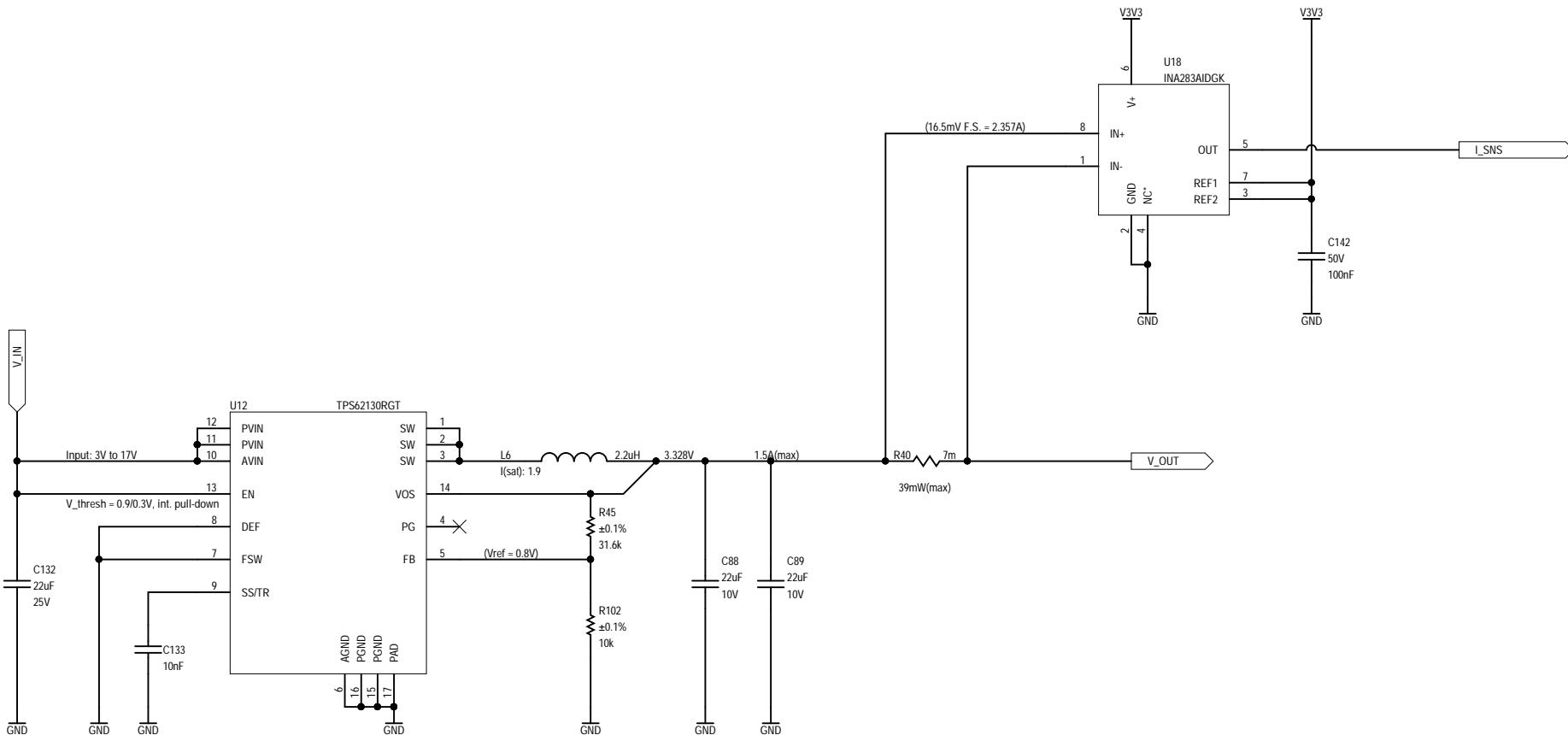
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C

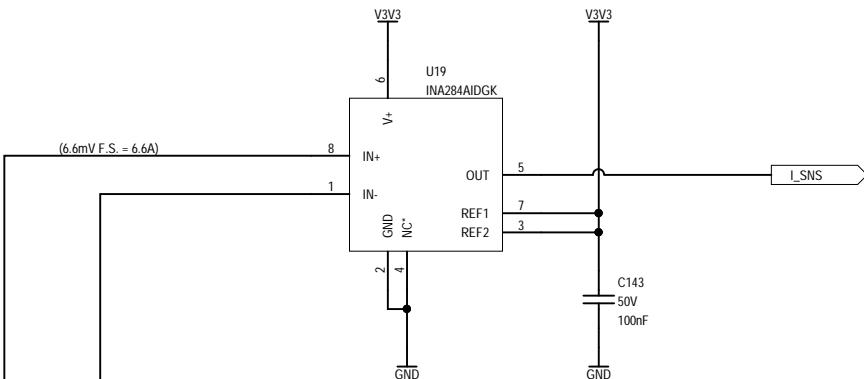
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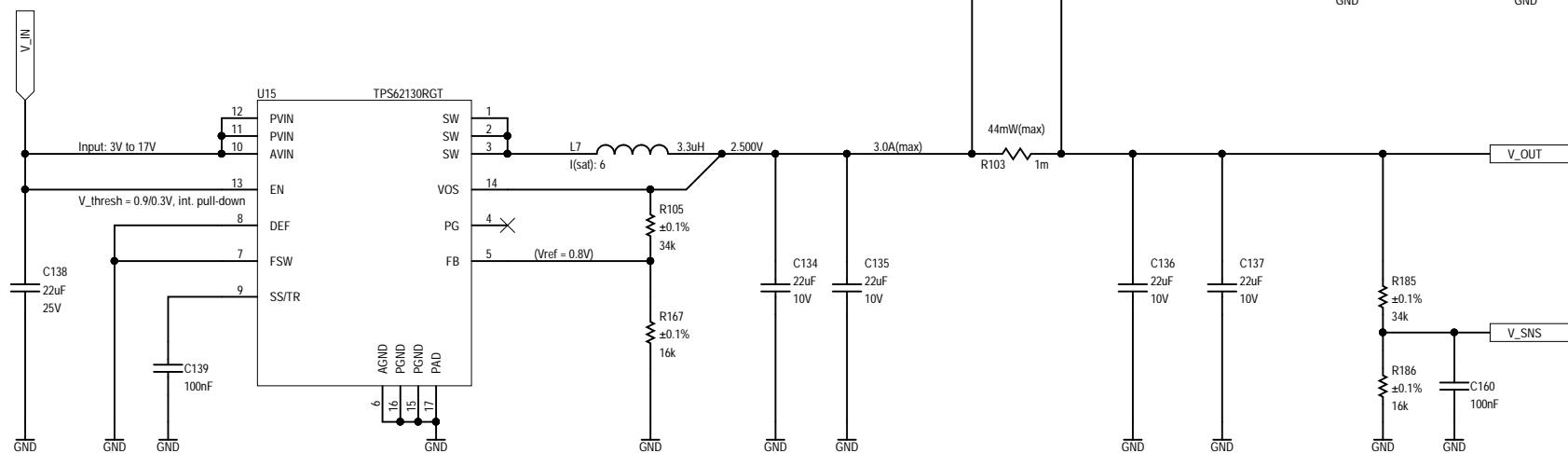




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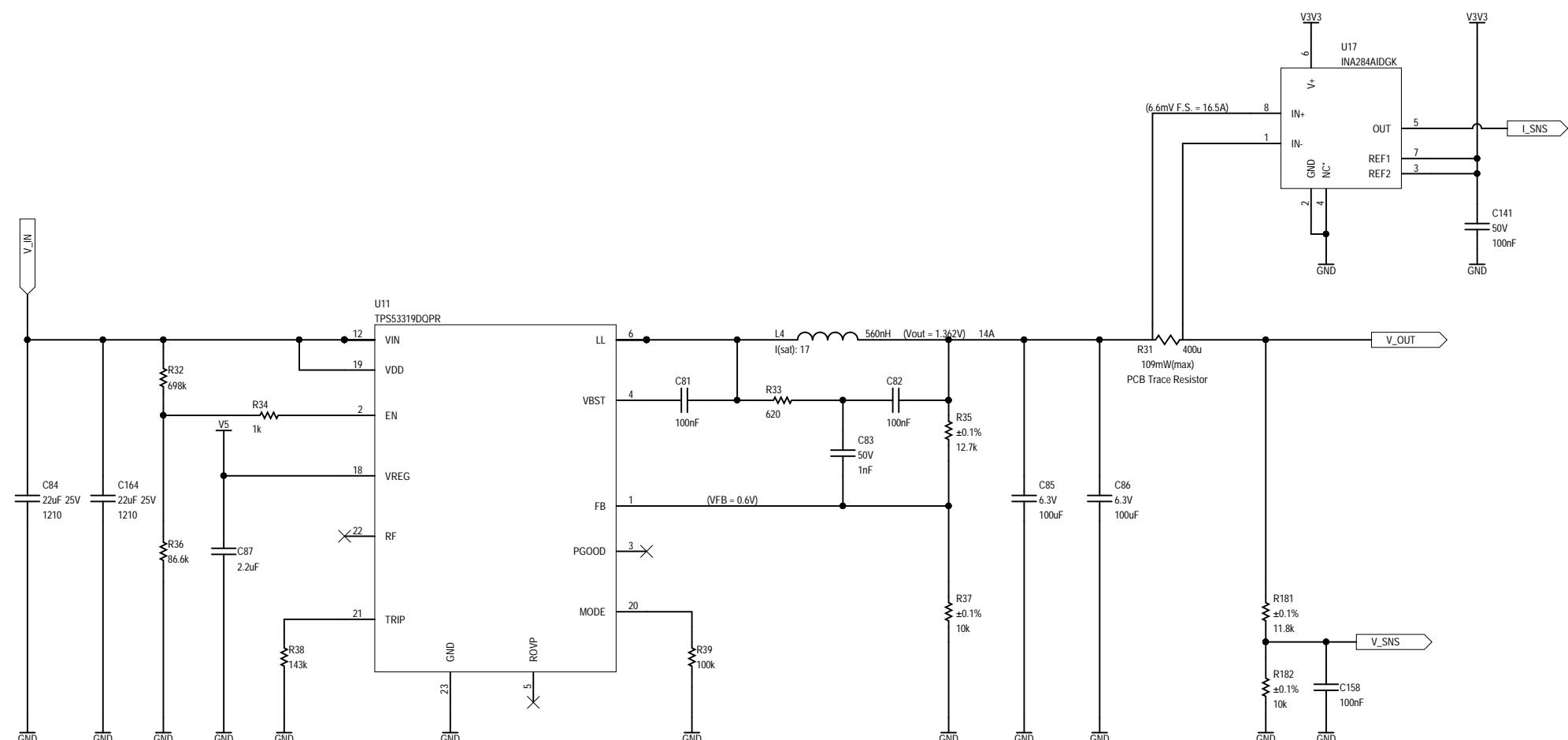


B

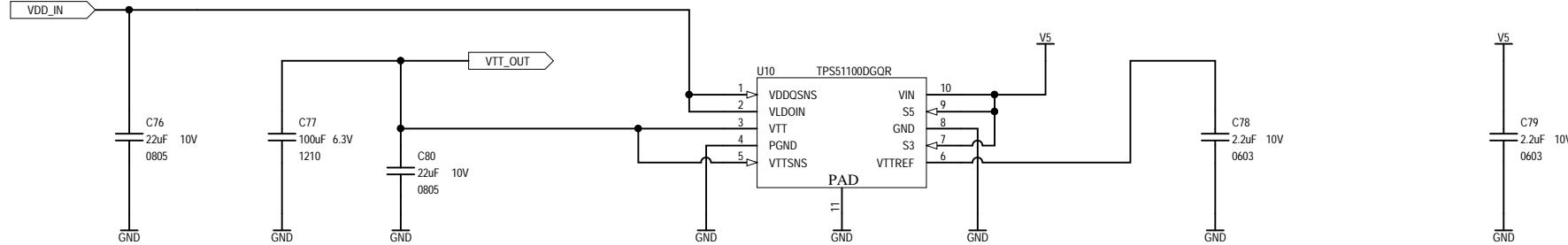


C

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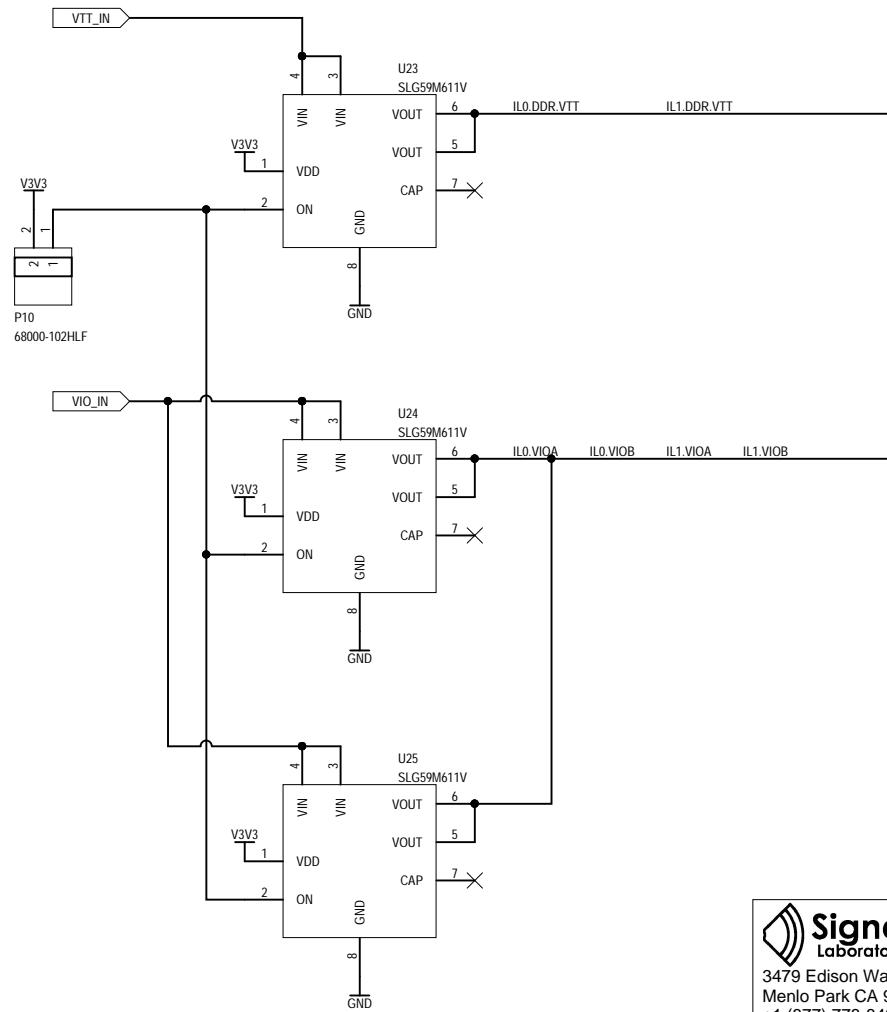
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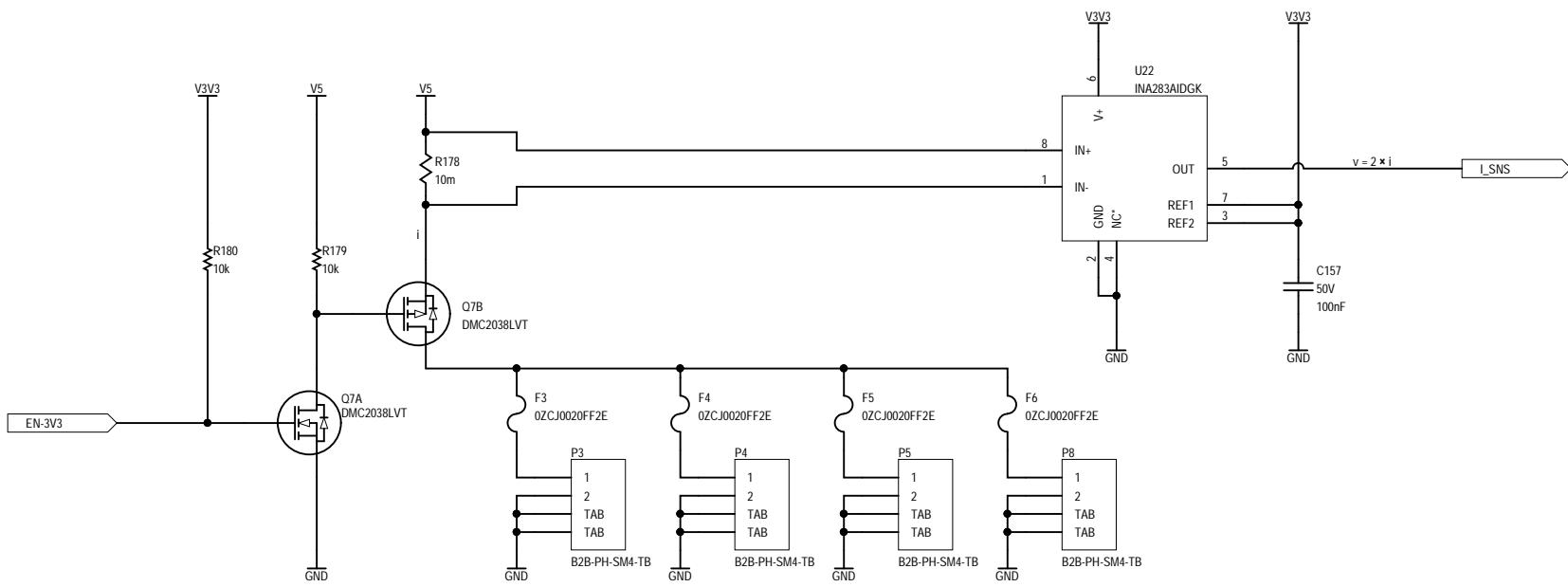


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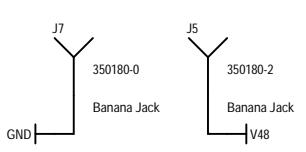
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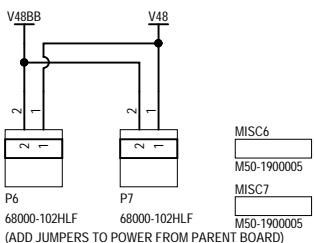
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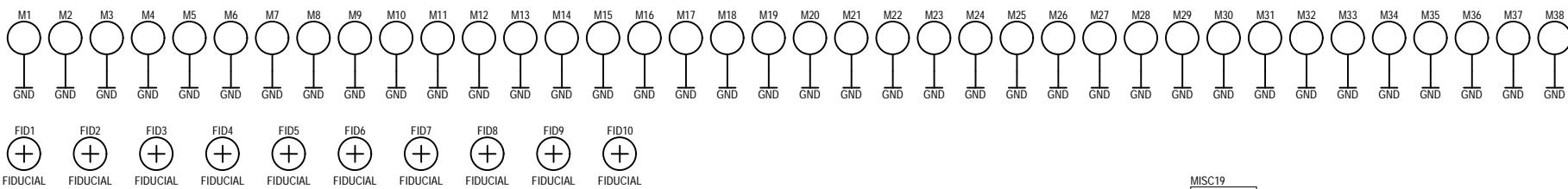
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