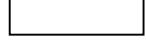


MAIN  
main.SchDoc



MECH  
mechanical.SchDoc



NOTE: DO ECPS DESIGN CHECKLIST!  
NOTE: ANALYZE JTAG PULL-UPS/DOWNS  
NOTE: ANALYZE DDR3 TERMINATION

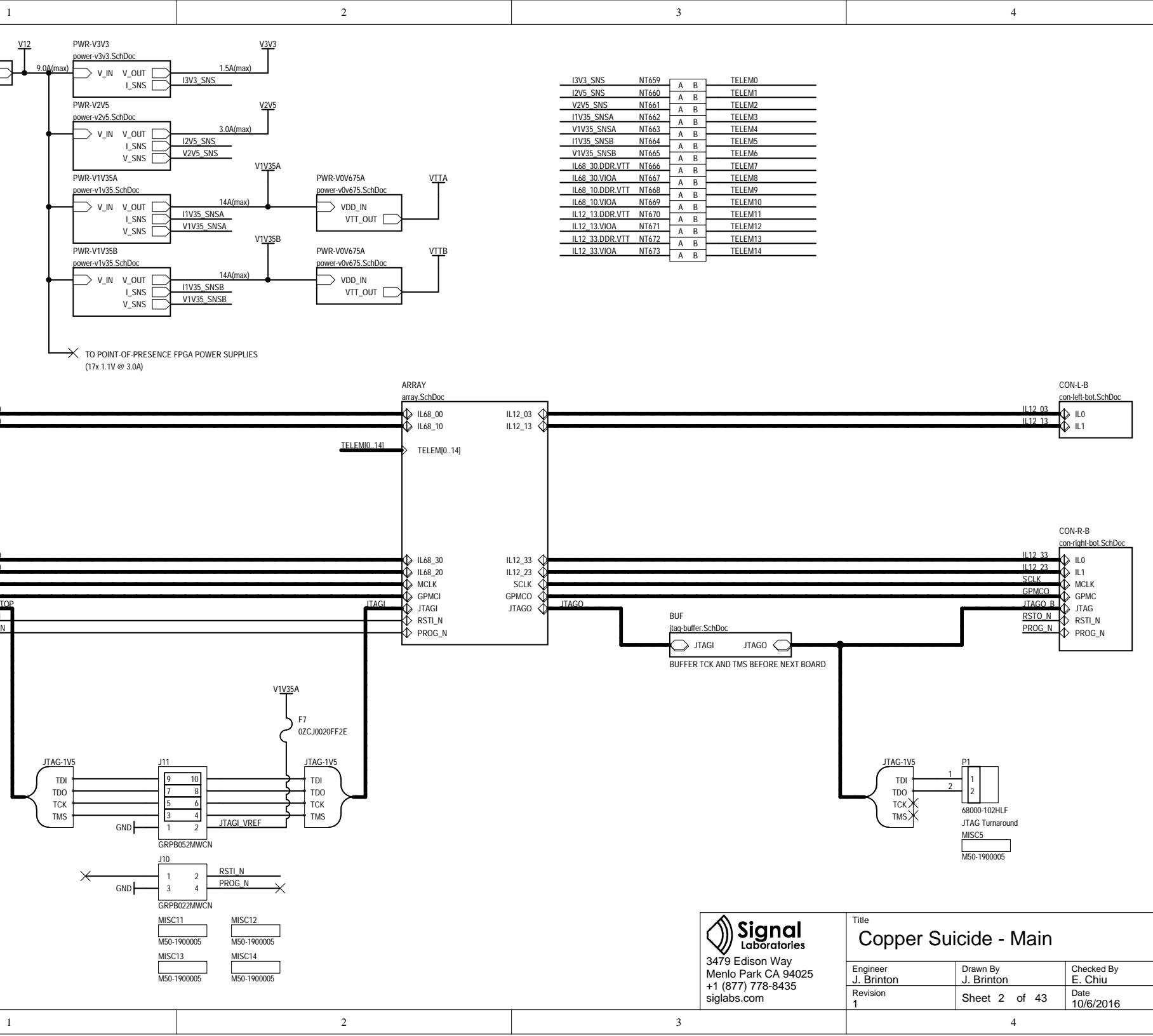
A  
A  
Todo:

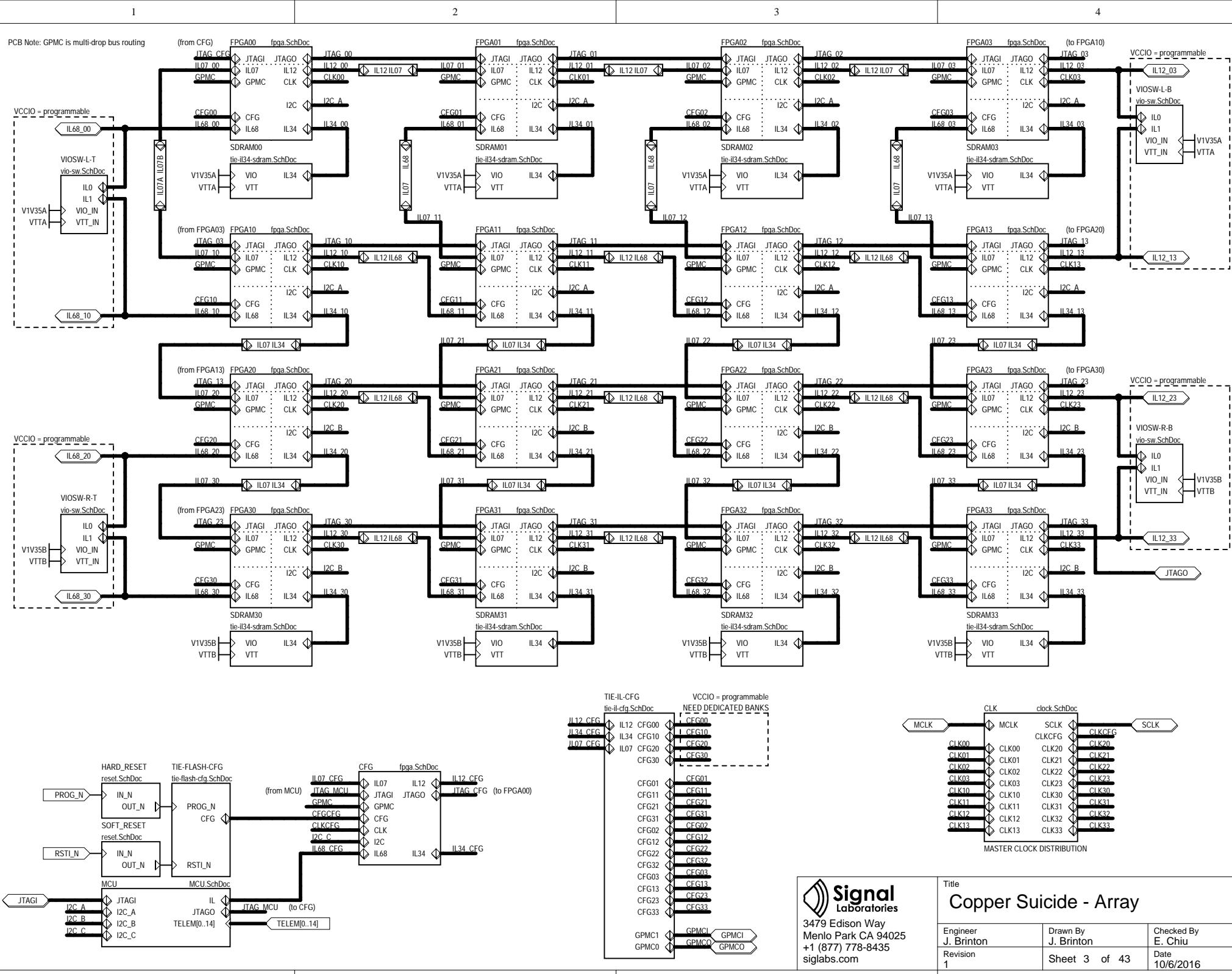
Done- \*\* pins need to get mapped to connectors  
 Done- \*\* pins need to get mapped between fpgas (see map.SchDoc)  
 Done- \*\* need soft reset buffer  
 Done- \*\* need high-speed clock buffer  
 Done- \*\* would like to use right angle "programming jumpers (J7)" to access JTAG when boards are stacked.  
 Done- \*\* would like to add some LEDs  
 \* component placement  
 \*\* can hopefully use some tricks to copy routing across FPGAs (rooms don't work on "sub parts spread across multiple child sheets in hierarchical design")  
 \* routing  
 \* review (especially of configuration and programming)  
 Done- 5V supply has caps from low side gate to drain. This has to be a mistake  
 Done- Swapping groups for DDR data lines (only within DQS group)  
 Done- Check power to unused SERDES  
 Done- Add global (non-GPMC) bus between all array FPGAs  
 Done- Mclk source needs to be pinned out on connector J3  
 Done- V48 needs to be pinned out on J3  
 Done- Add 3.3V power supply (linear reg)  
 Done- DDR3 chip termination R packs are 39k??  
 Done- Add reset button  
 Done- Change 2.5V switcher inductor to 3A  
 Done- Add jumper on 48V in  
 Done- Add power input barrel jack  
 Done- Add current sense resistors on supply rail PS outputs  
 Done- Add local JTAG connector to access entire board JTAG chain  
 Done- Review for single board operation

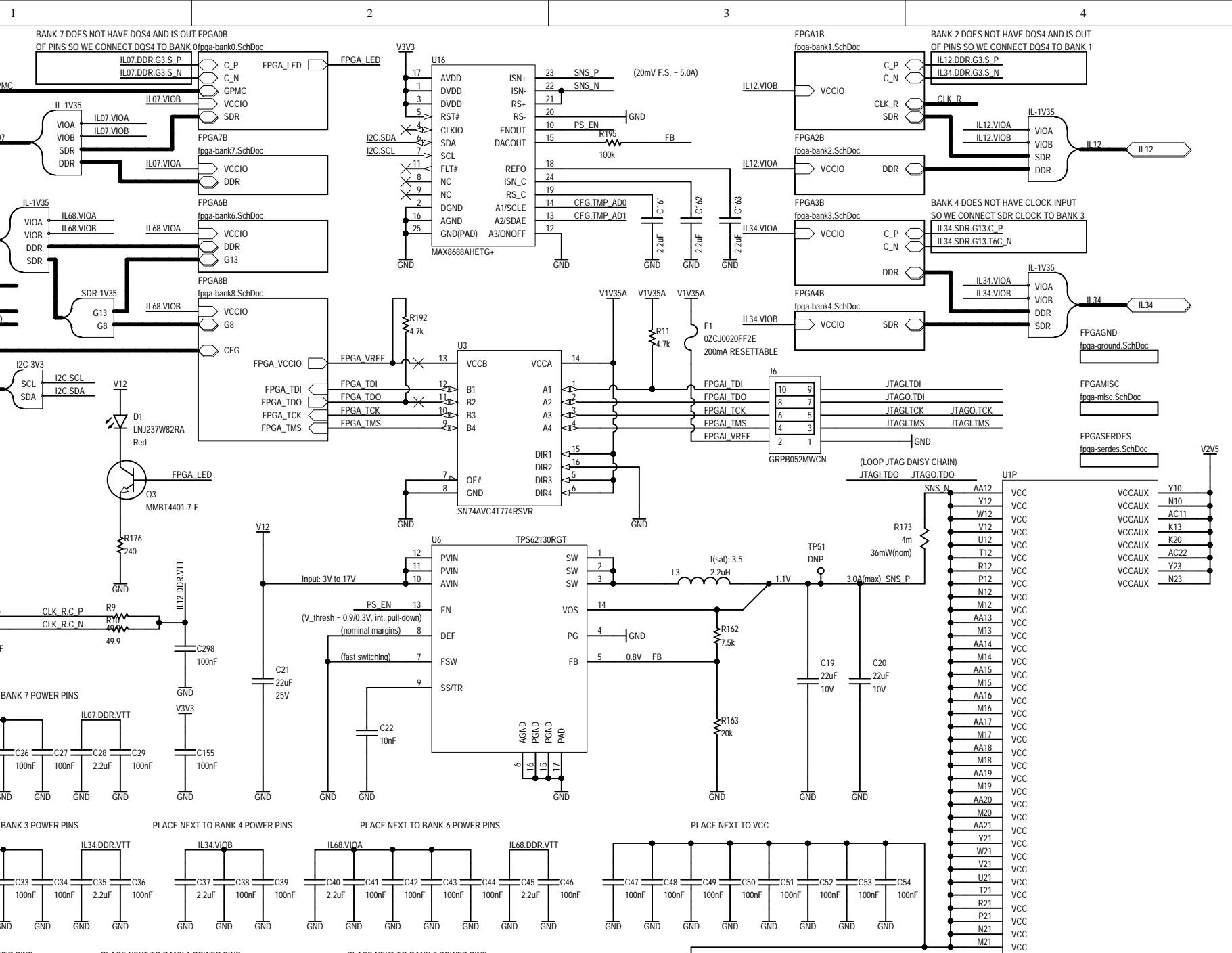
B  
B  
Done:  
DDR3 checked

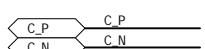
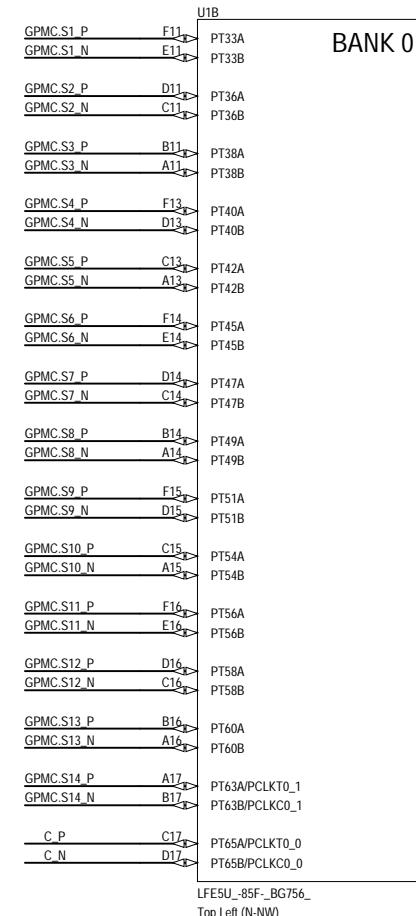
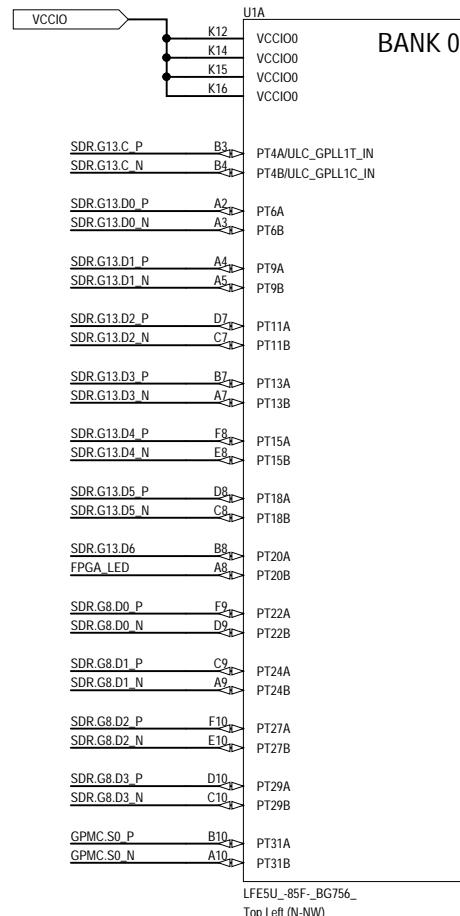
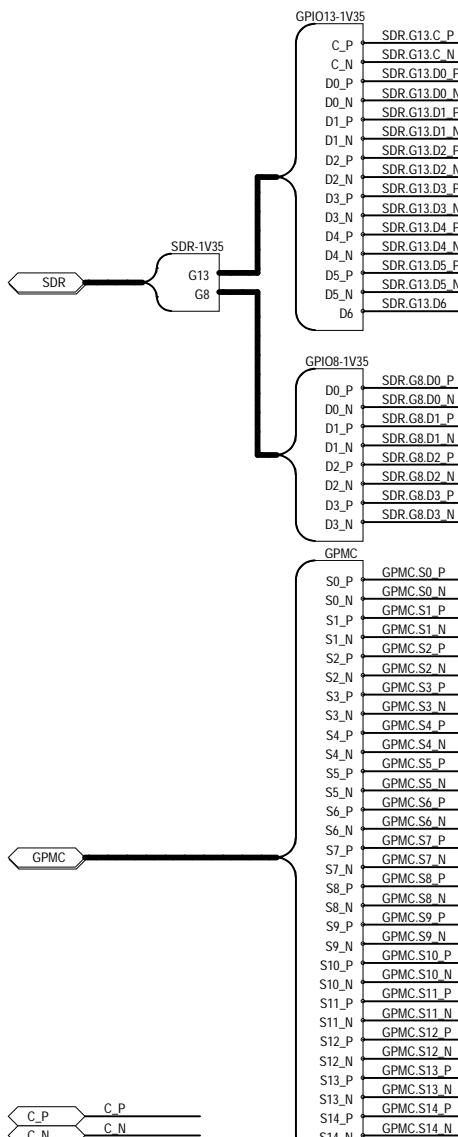


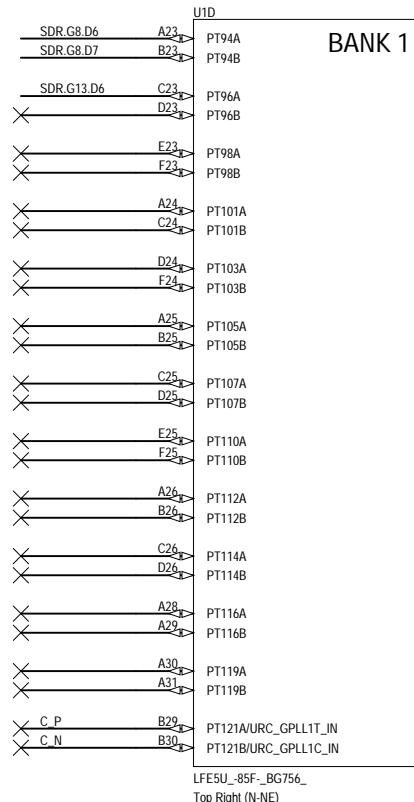
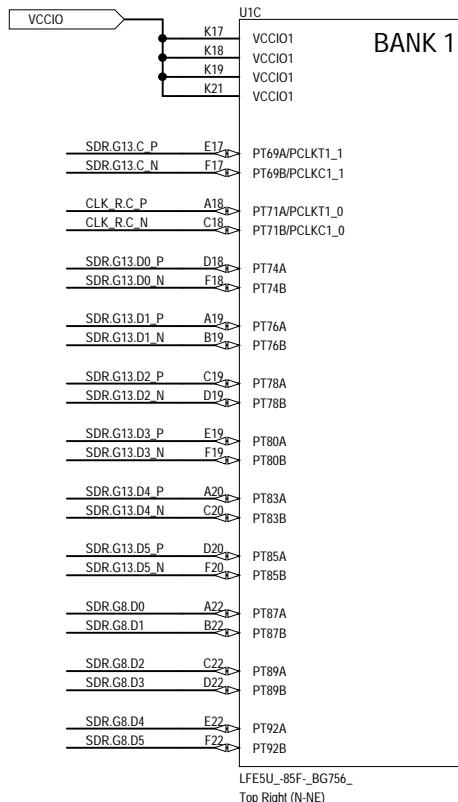
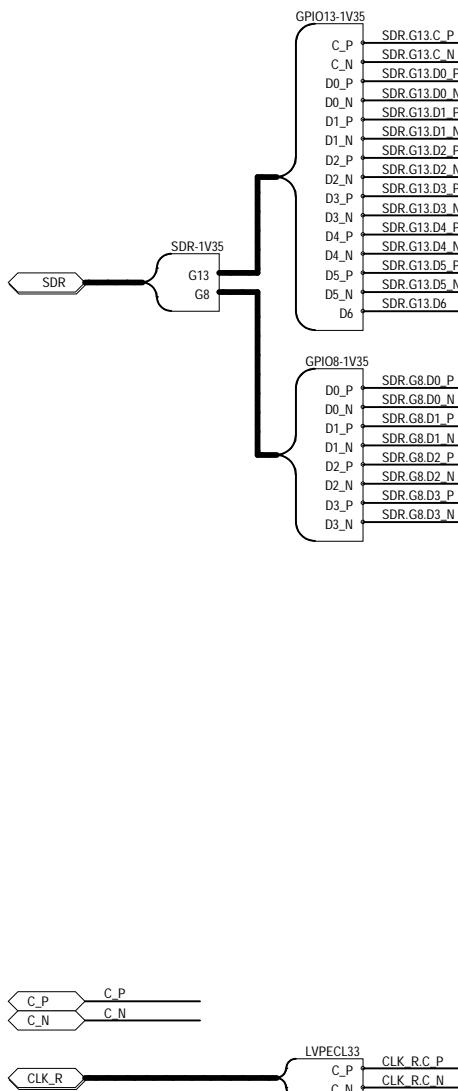
Title		
<b>Copper Suicide - Top</b>		
Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision	Sheet 1 of 43	Date
1		10/6/2016

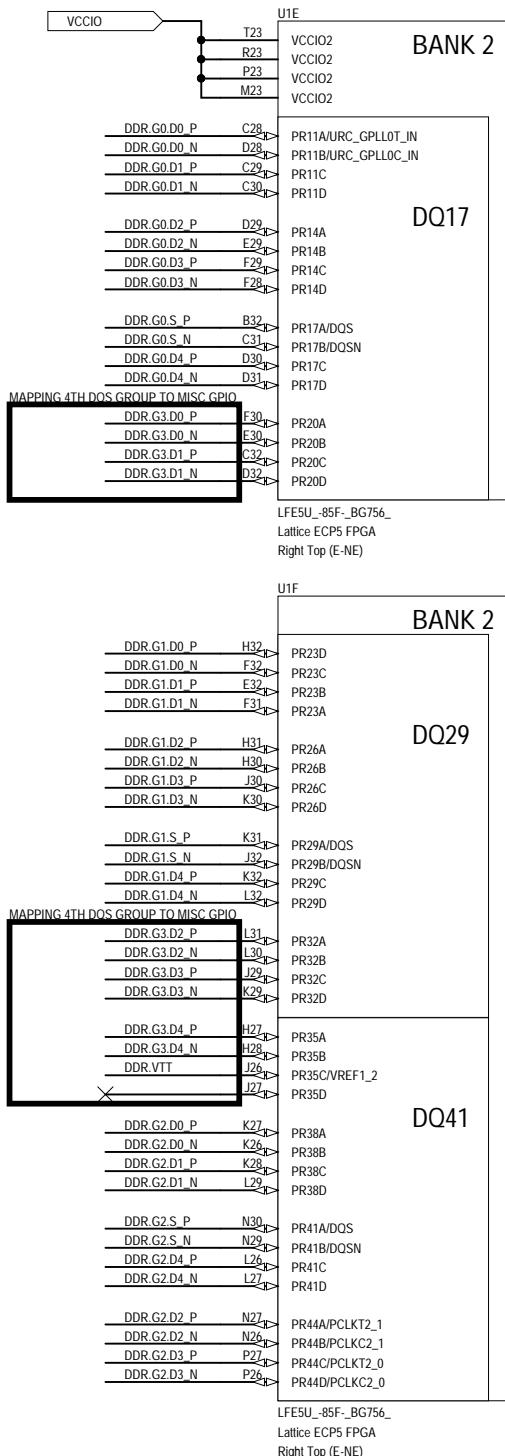
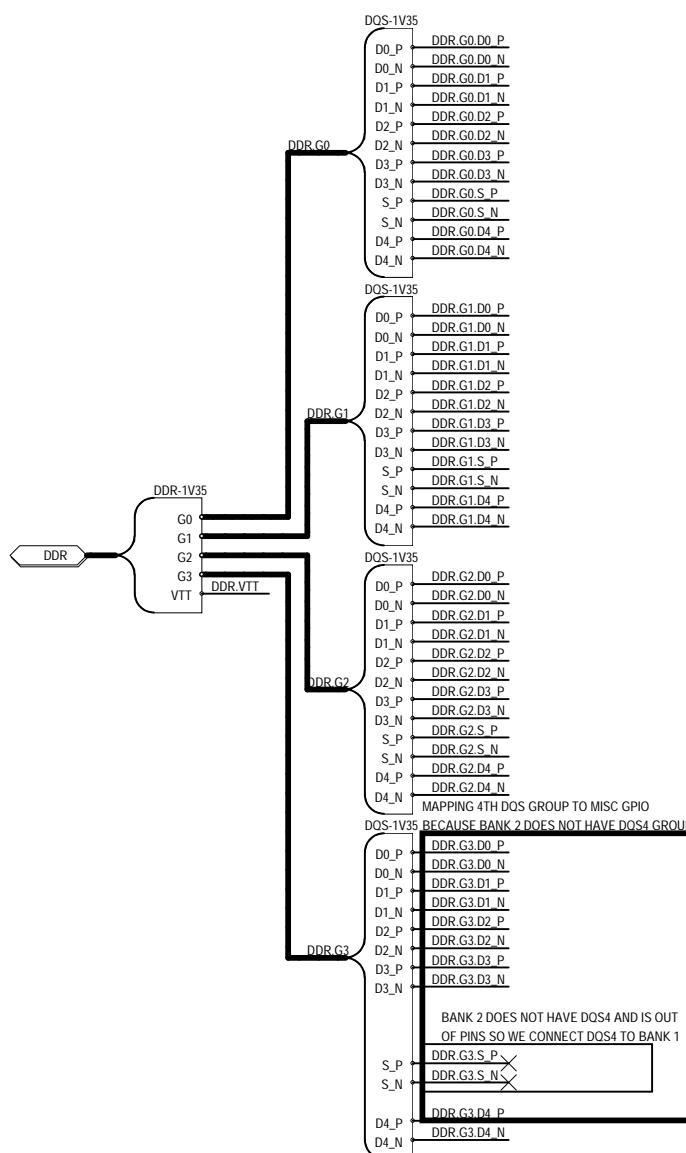


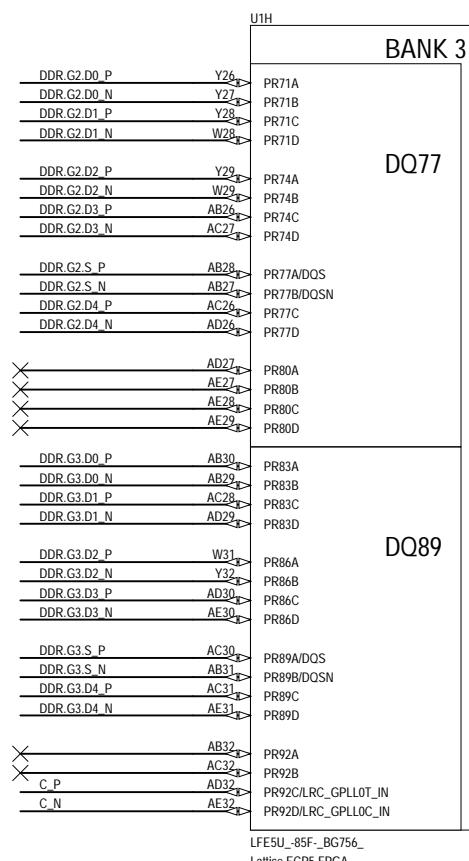
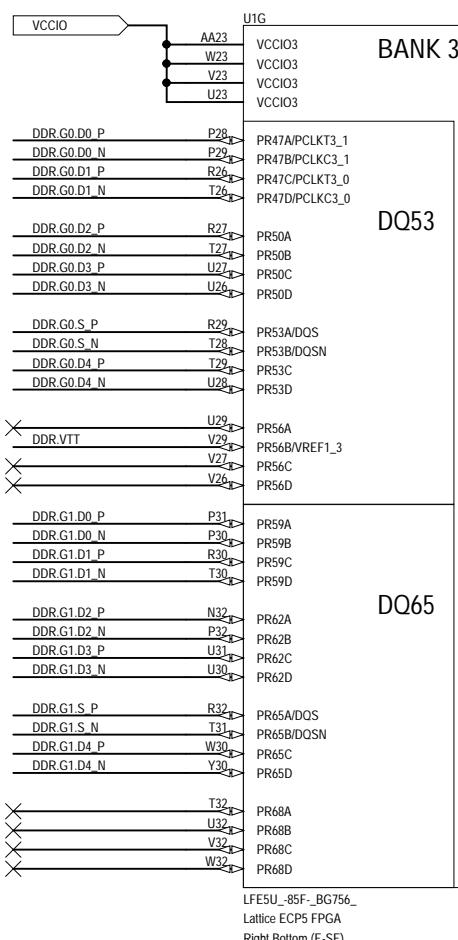
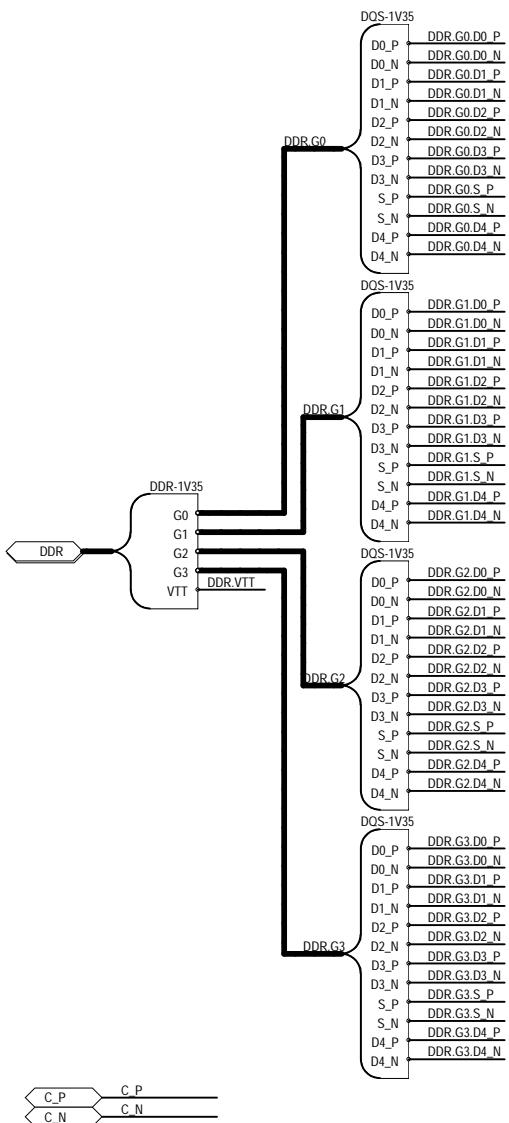






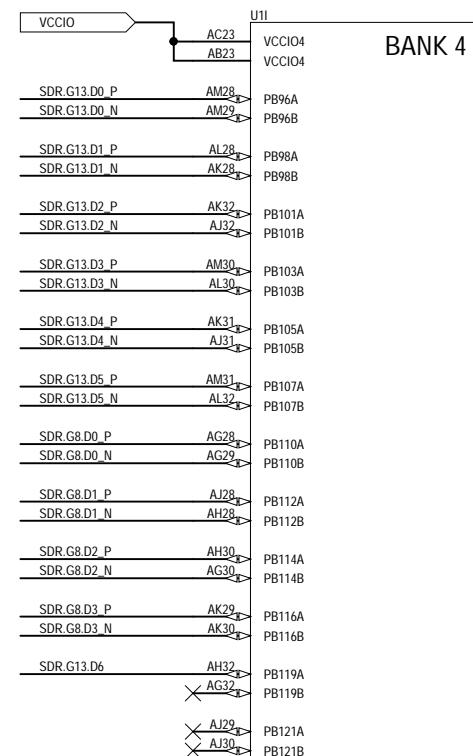
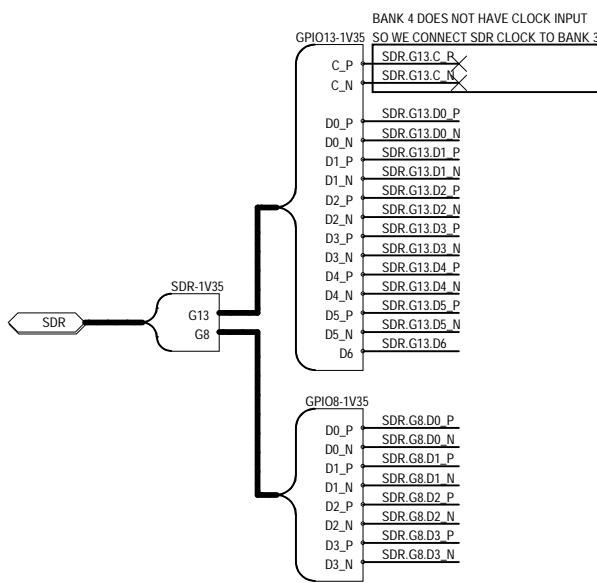


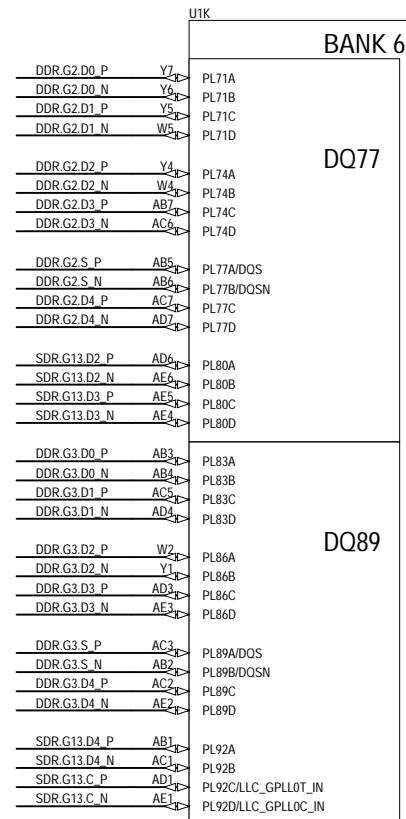
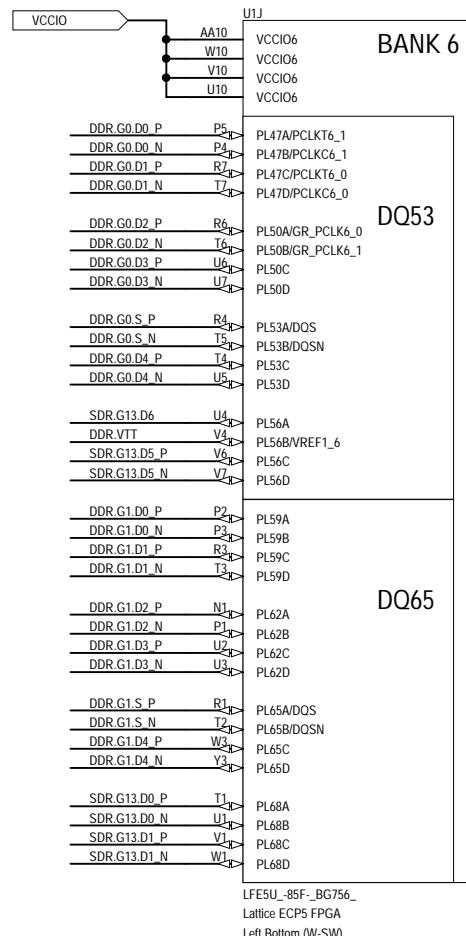
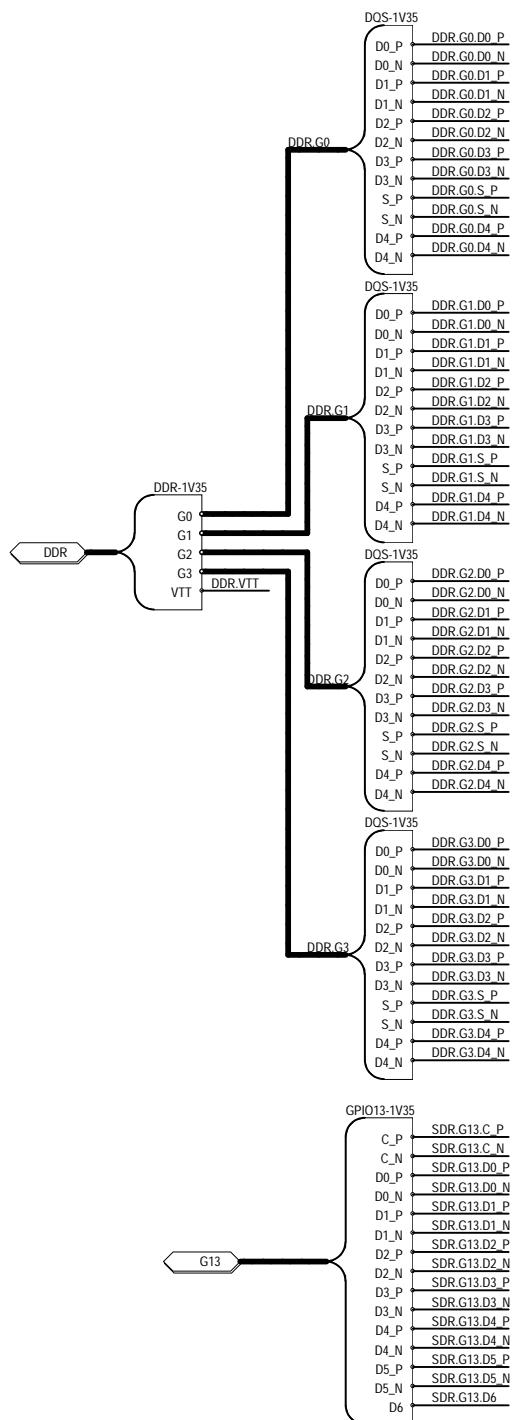


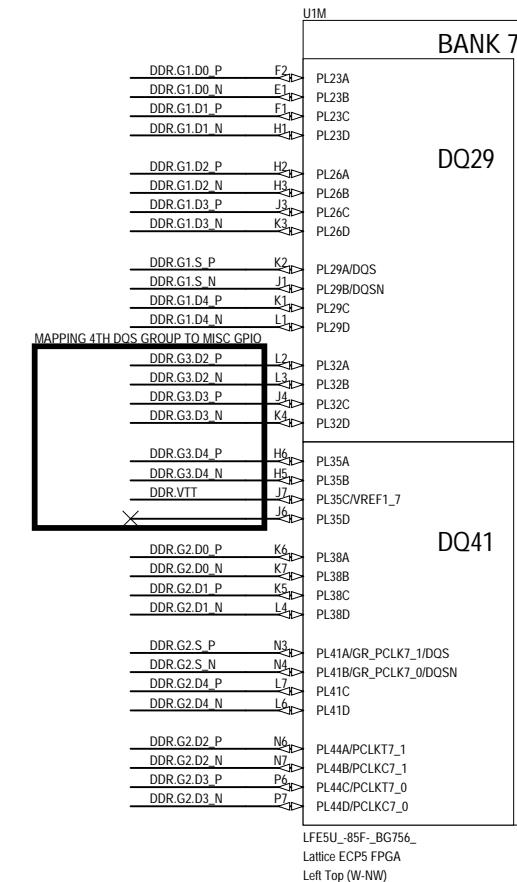
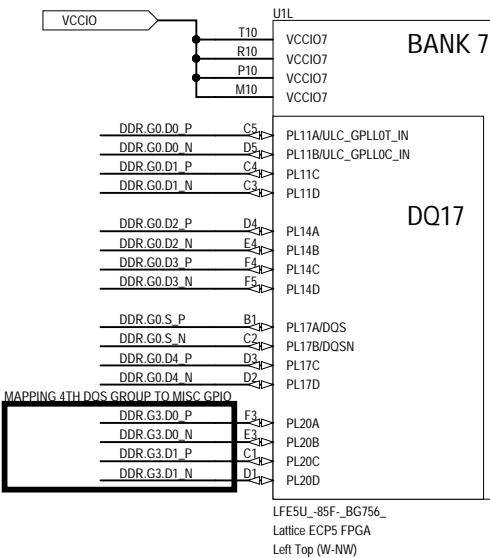
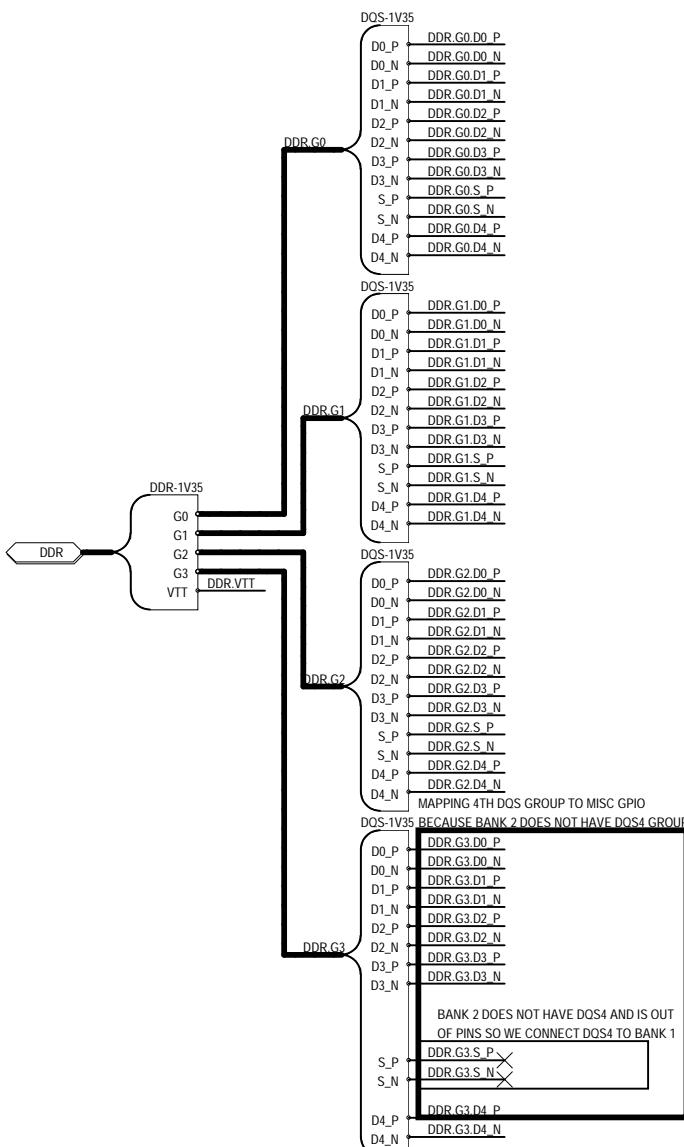


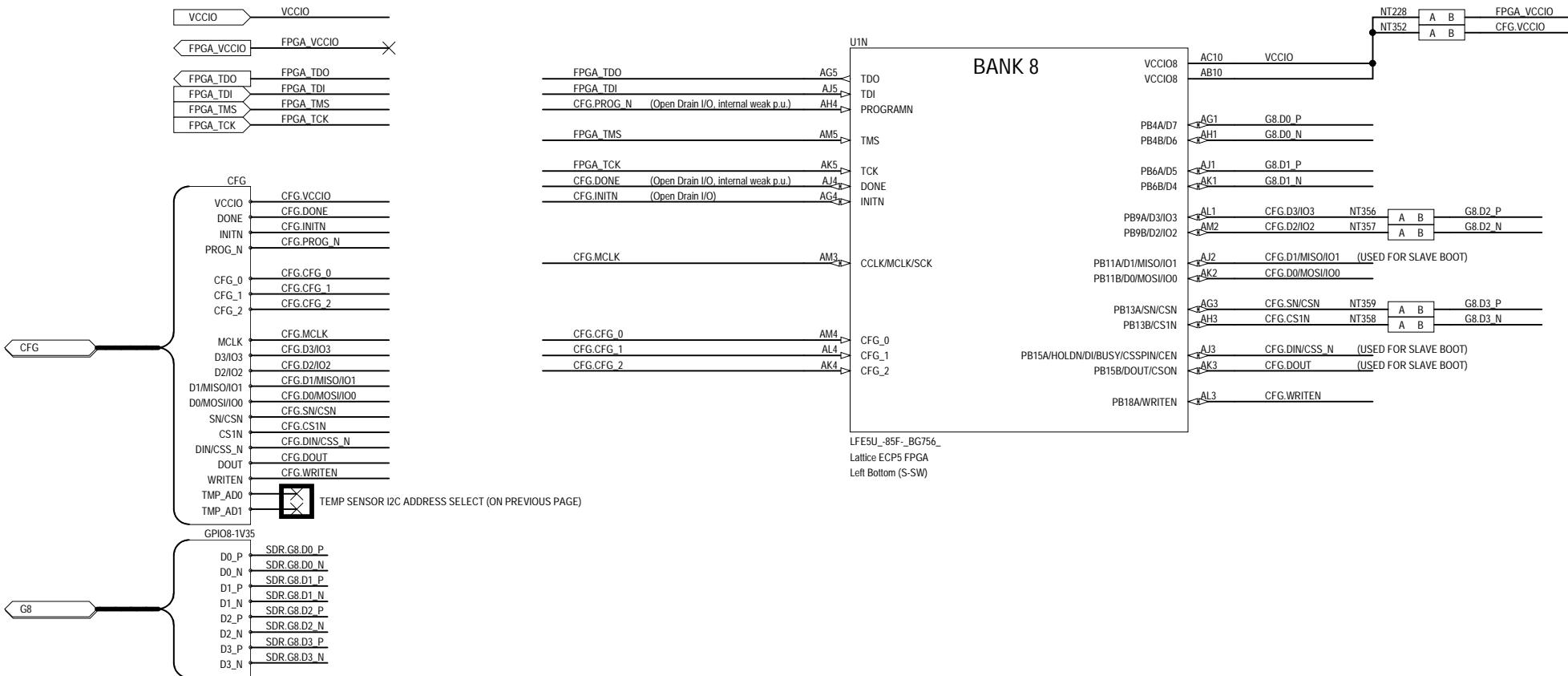
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Title			
Copper Suicide - FPGA - Bank 3			
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu	
Revision 1	Sheet 8 of 43	Date 10/6/2016	









A

B

C

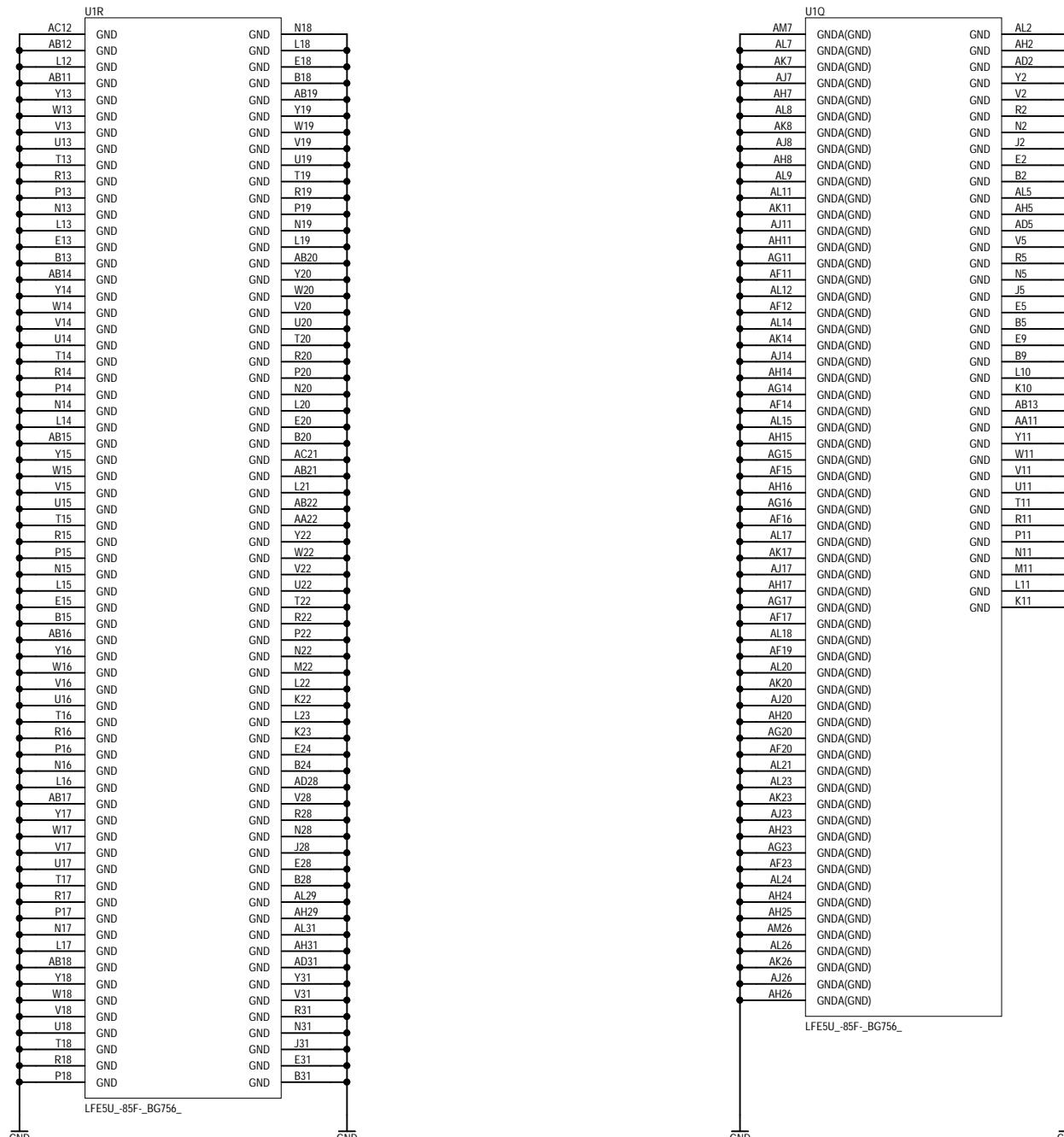
D

A

B

C

D



Copper Suicide - FPGA - Ground		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 13 of 43	Date 10/6/2016

A

A

B

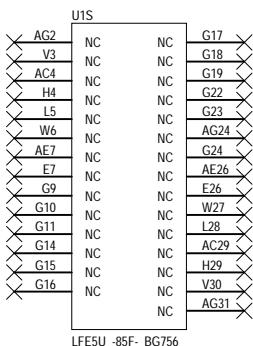
B

C

C

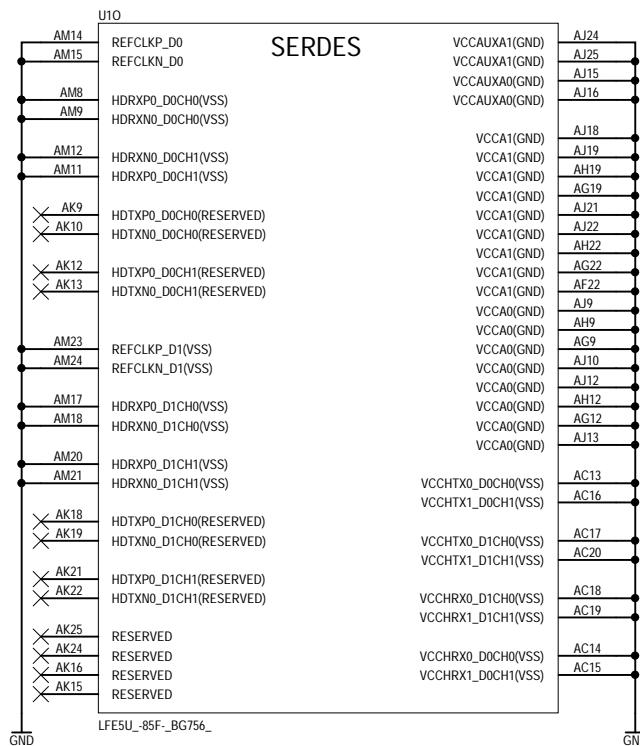
D

D



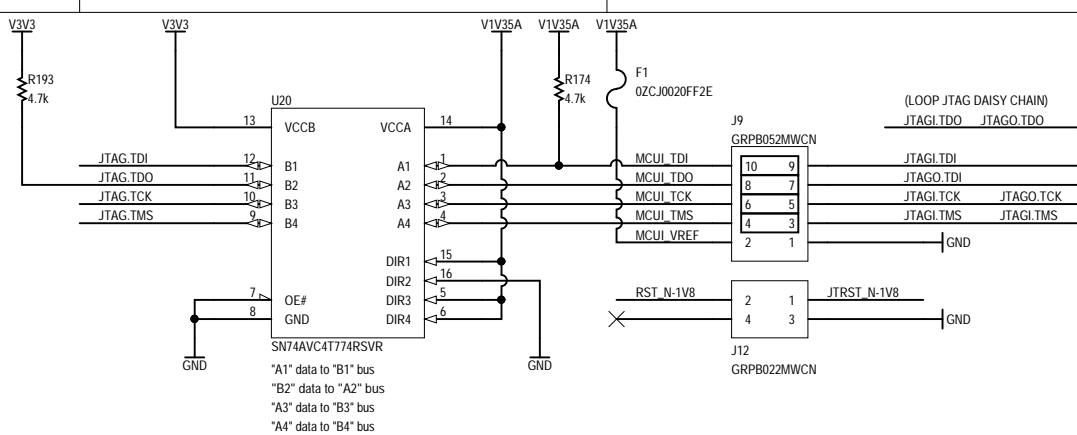
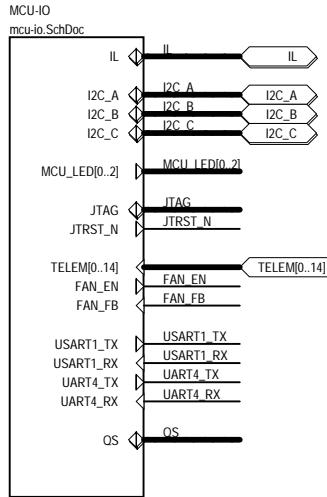
Title  
**Copper Suicide - FPGA - Misc**

Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 14 of 43	Date 10/6/2016



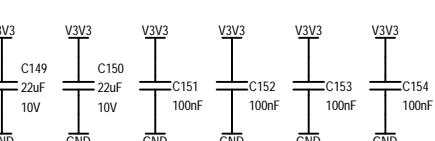
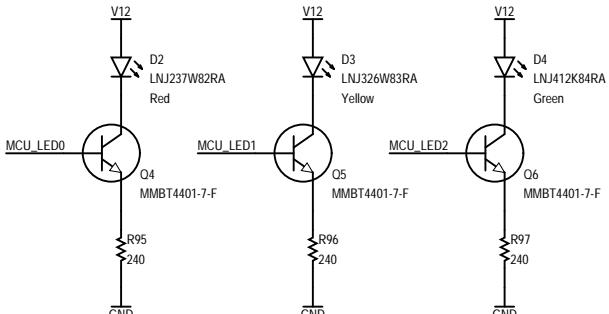
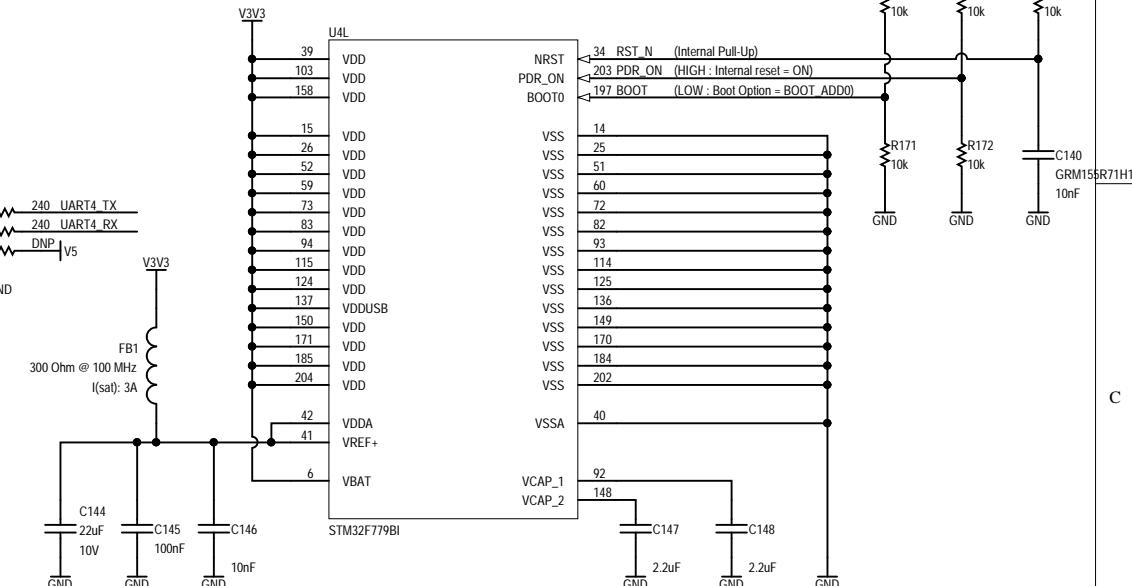
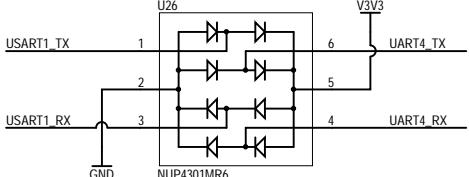
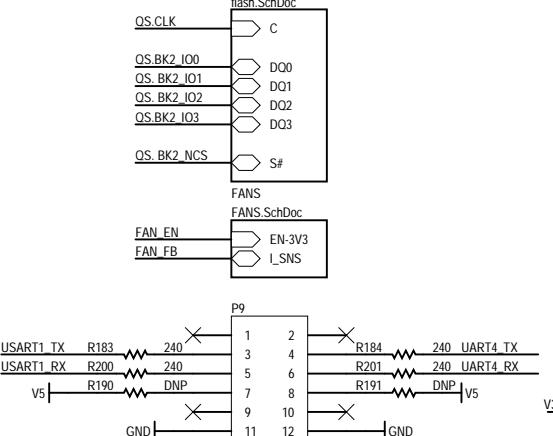
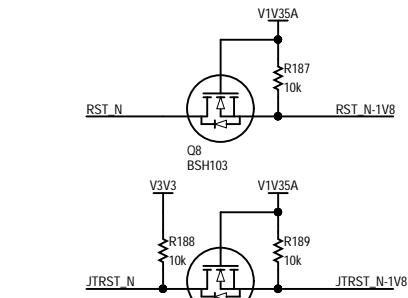
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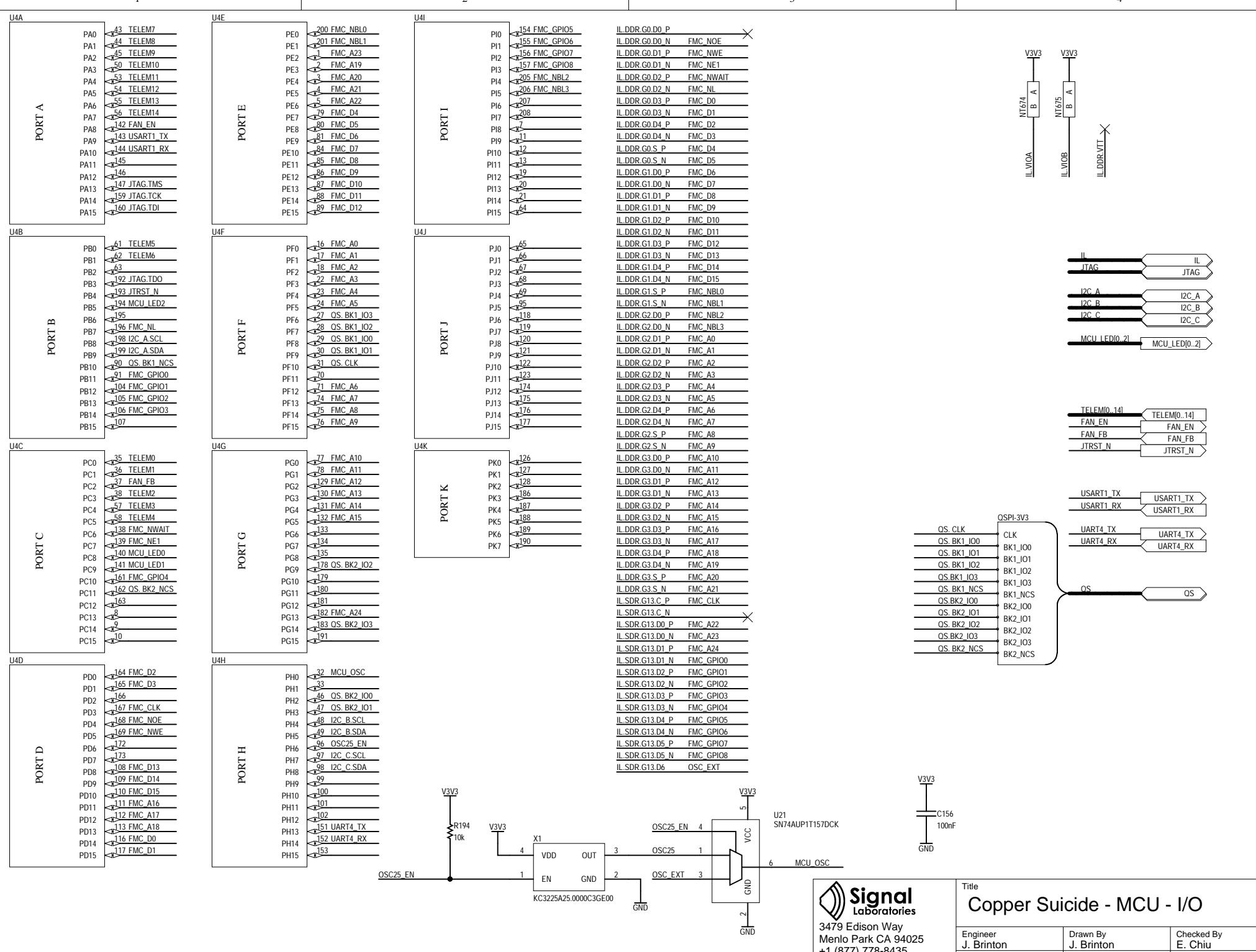
Title	Copper Suicide - FPGA - SERDES		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu	
Revision 1	Sheet 15 of 43	Date 10/6/2016	

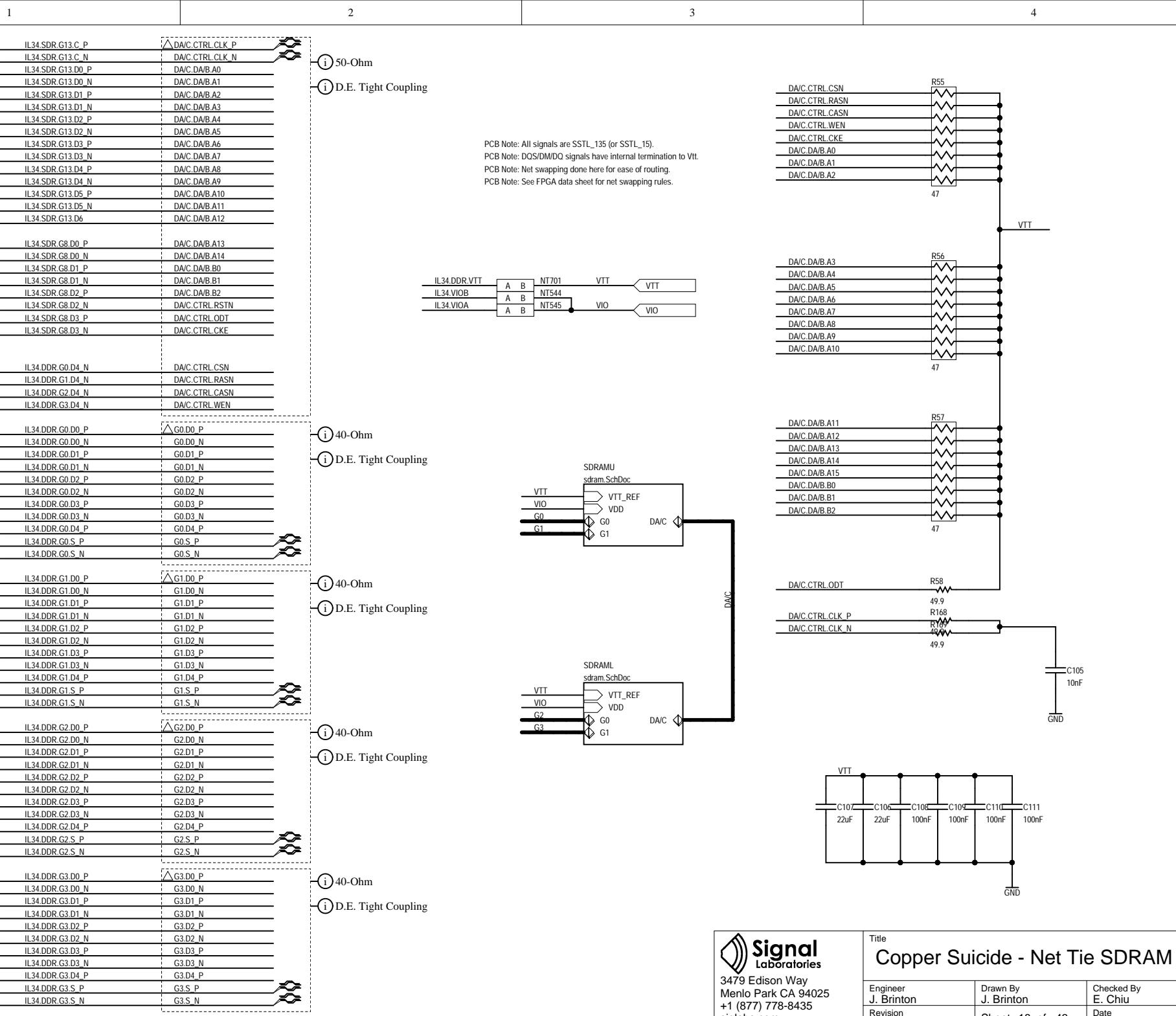


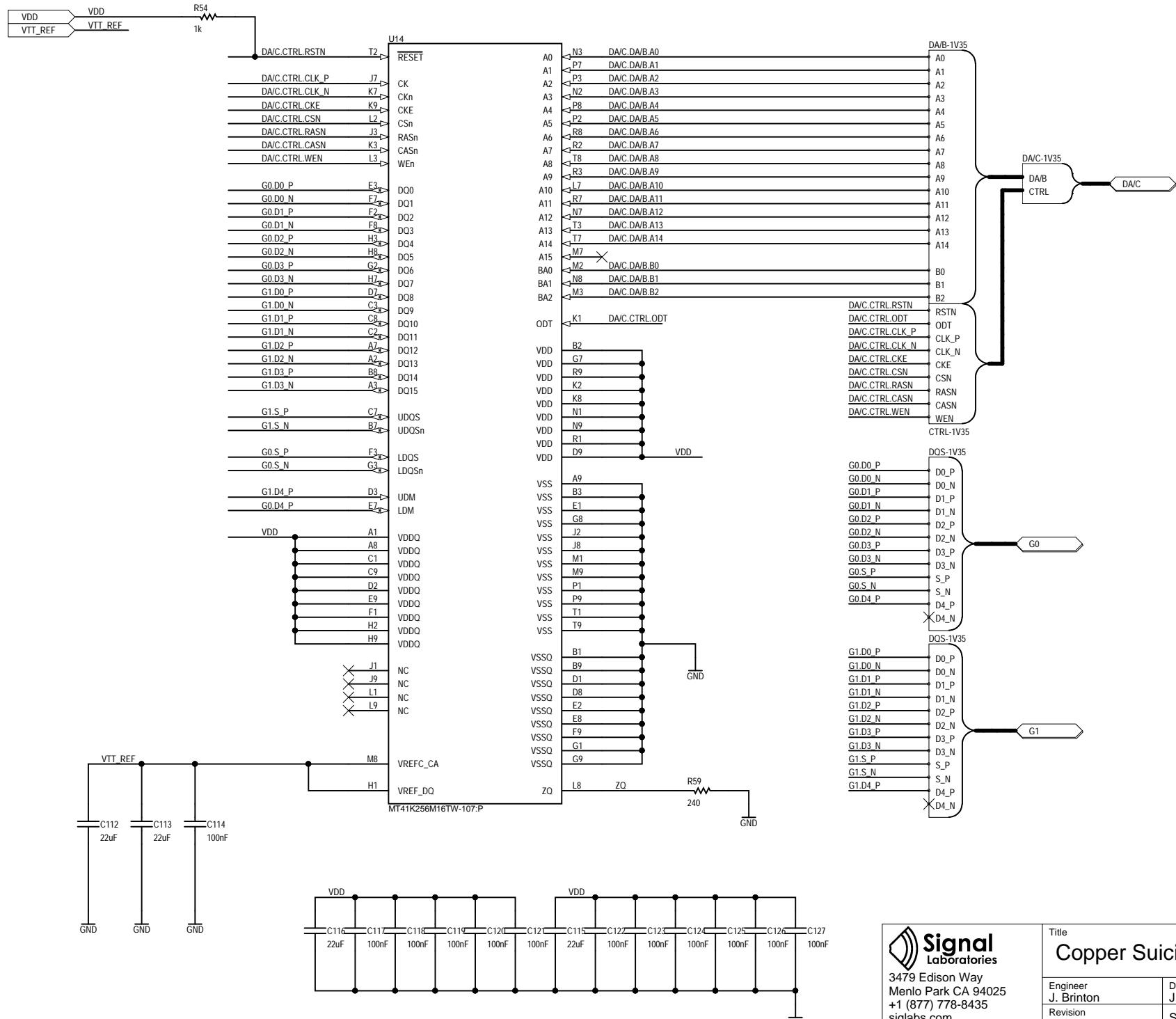
(LOOP JTAG DAISY CHAIN)

JTAGI.TDI — JTAGO.TDI  
JTAGO.TDI — JTAGO.TDO  
JTAGO.TCK — JTAGO.TCK  
JTAGI.TMS — JTAGI.TMS









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# Title

# Copper Suicide - SDRAM

Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 19 of 43	Date 10/6/2016

VCCIO = programmable, NEEDS DEDICATED BANK

IL12.SDR.G13.C_P	NT2	A B	CFG10.MCLK
IL12.SDR.G13.C_N	NT3	A B	CFG10.DONE
IL12.SDR.G13.D_P	NT4	A B	CFG10.INITN
IL12.SDR.G13.D_N	NT5	A B	CFG10.PROG_N
IL12.SDR.G13.D1_P	NT6	A B	CFG10.DIN/CSS_N
IL12.SDR.G13.D1_N	NT7	A B	CFG10.DOUT
IL12.SDR.G13.D2_P	NT8	A B	CFG10.D1/MISO/I01
IL12.SDR.G13.D2_N	NT9	A B	CFG10.D0/MOSI/I00
IL12.SDR.G13.D3_P	NT10	A B	CFG10.WRITEN
IL12.SDR.G13.D3_N	NT11	A B	
IL12.SDR.G13.D4_P	NT12	A B	CFG00.MCLK
IL12.SDR.G13.D4_N	NT13	A B	CFG00.DONE
IL12.SDR.G13.D5_P	NT14	A B	CFG00.INITN
IL12.SDR.G13.D5_N	NT15	A B	CFG00.PROG_N
IL12.SDR.G13.D6	NT16	A B	CFG00.DIN/CSS_N
IL12.SDR.G8.D0_P	NT17	A B	CFG00.DOUT
IL12.SDR.G8.D0_N	NT18	A B	CFG00.D1/MISO/I01
IL12.SDR.G8.D1_P	NT19	A B	CFG00.D0/MOSI/I00
IL12.SDR.G8.D1_N	NT20	A B	CFG00.WRITEN
IL12.SDR.G8.D2_P	NT21	A B	
IL12.SDR.G8.D2_N	NT22	A B	
IL12.SDR.G8.D3_P	NT23	A B	
IL12.SDR.G8.D3_N	NT24	A B	
IL12.DDR.G3.S_P	NT71	A B	
IL12.DDR.G3.S_N	NT212	A B	
IL12.VIOB	NT232	A B	CFG00.VCCIO

VCCIO = programmable, NEEDS DEDICATED BANK

IL07.SDR.G13.C_P	NT355	A B	CFG20.MCLK
IL07.SDR.G13.C_N	NT360	A B	CFG20.DONE
IL07.SDR.G13.D1_P	NT361	A B	CFG20.INITN
IL07.SDR.G13.D1_N	NT362	A B	CFG20.PROG_N
IL07.SDR.G13.D2_P	NT363	A B	CFG20.DIN/CSS_N
IL07.SDR.G13.D2_N	NT364	A B	CFG20.DOUT
IL07.SDR.G13.D3_P	NT365	A B	CFG20.D1/MISO/I01
IL07.SDR.G13.D3_N	NT366	A B	CFG20.D0/MOSI/I00
IL07.SDR.G13.D4_P	NT367	A B	CFG20.WRITEN
IL07.SDR.G13.D4_N	NT368	A B	
IL07.SDR.G13.D5_P	NT369	A B	CFG30.MCLK
IL07.SDR.G13.D5_N	NT370	A B	CFG30.DONE
IL07.SDR.G13.D6	NT371	A B	CFG30.INITN
IL07.SDR.G8.D0_P	NT372	A B	CFG30.PROG_N
IL07.SDR.G8.D0_N	NT373	A B	CFG30.DIN/CSS_N
IL07.SDR.G8.D1_P	NT374	A B	CFG30.DOUT
IL07.SDR.G8.D1_N	NT375	A B	CFG30.D1/MISO/I01
IL07.SDR.G8.D2_P	NT376	A B	CFG30.D0/MOSI/I00
IL07.SDR.G8.D2_N	NT377	A B	CFG30.WRITEN
IL07.SDR.G8.D3_P	NT378	A B	
IL07.SDR.G8.D3_N	NT379	A B	
IL07.DDR.G3.S_P	NT426	A B	
IL07.DDR.G3.S_N	NT213	A B	
IL07.VIOB	NT233	A B	CFG20.VCCIO

IL34.SDR.G13.C_P	NT218	A B	GPMC0.S0_P
IL34.SDR.G13.C_N	NT219	A B	GPMC0.S0_N
IL34.SDR.G13.D0_P	NT220	A B	GPMC0.S1_P
IL34.SDR.G13.D0_N	NT221	A B	GPMC0.S1_N
IL34.SDR.G13.D1_P	NT222	A B	GPMC0.S2_P
IL34.SDR.G13.D1_N	NT223	A B	GPMC0.S2_N
IL34.SDR.G13.D2_P	NT224	A B	GPMC0.S3_P
IL34.SDR.G13.D2_N	NT225	A B	GPMC0.S3_N
IL34.SDR.G13.D3_P	NT226	A B	GPMC0.S4_P
IL34.SDR.G13.D3_N	NT227	A B	GPMC0.S4_N
IL34.SDR.G13.D4_P	NT229	A B	GPMC0.S5_P
IL34.SDR.G13.D4_N	NT230	A B	GPMC0.S5_N
IL34.SDR.G13.D5_P	NT231	A B	GPMC0.S6_P
IL34.SDR.G13.D5_N	NT236	A B	GPMC0.S6_N
IL34.SDR.G13.D6	NT237	A B	CFG22.D0/MOSI/I00
IL34.SDR.G8.D0_P	NT242	A B	GPMC0.S7_P
IL34.SDR.G8.D0_N	NT243	A B	GPMC0.S7_N
IL34.SDR.G8.D1_P	NT248	A B	GPMC0.S8_P
IL34.SDR.G8.D1_N	NT249	A B	GPMC0.S8_N
IL34.SDR.G8.D2_P	NT254	A B	GPMC0.S9_P
IL34.SDR.G8.D2_N	NT255	A B	GPMC0.S9_N
IL34.SDR.G8.D3_P	NT260	A B	GPMC0.S10_P
IL34.SDR.G8.D3_N	NT262	A B	GPMC0.S10_N
IL34.DDR.G3.S_P	NT541	A B	GPMC0.S11_P
IL34.DDR.G3.S_N	NT542	A B	GPMC0.S11_N
IL34.VIOB	NT264	A B	V1V35A

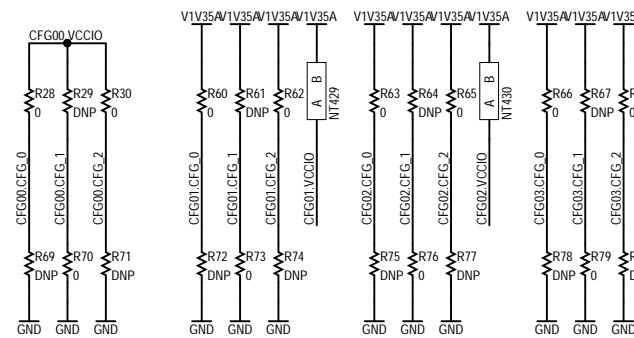
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IL34.DDR.G0.D0_N	NT263	A B	GPMC1.S0_N
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IL34.DDR.G0.D1_N	NT266	A B	GPMC1.S1_N
IL34.DDR.G0.D2_P	NT267	A B	GPMC1.S2_P
IL34.DDR.G0.D2_N	NT268	A B	GPMC1.S2_N
IL34.DDR.G0.D3_P	NT269	A B	GPMC1.S3_P
IL34.DDR.G0.D3_N	NT270	A B	GPMC1.S3_N
IL34.DDR.G0.D4_P	NT271	A B	GPMC1.S4_P
IL34.DDR.G0.D4_N	NT272	A B	GPMC1.S4_N
IL34.DDR.G0.S_P	NT273	A B	GPMC1.S5_P
IL34.DDR.G0.S_N	NT274	A B	GPMC1.S5_N
IL34.DDR.G1.D0_P	NT275	A B	GPMC1.S6_P
IL34.DDR.G1.D0_N	NT276	A B	GPMC1.S6_N
IL34.DDR.G1.D1_P	NT277	A B	GPMC1.S7_P
IL34.DDR.G1.D1_N	NT278	A B	GPMC1.S7_N
IL34.DDR.G1.D2_P	NT279	A B	GPMC1.S8_P
IL34.DDR.G1.D2_N	NT280	A B	GPMC1.S8_N
IL34.DDR.G1.D3_P	NT281	A B	GPMC1.S9_P
IL34.DDR.G1.D3_N	NT514	A B	GPMC1.S9_N
IL34.DDR.G1.D4_P	NT515	A B	GPMC1.S10_P
IL34.DDR.G1.D4_N	NT516	A B	GPMC1.S10_N
IL34.DDR.G1.L_S_P	NT517	A B	GPMC1.S11_P
IL34.DDR.G1.S_N	NT518	A B	GPMC1.S11_N
IL34.DDR.G2.D0_P	NT519	A B	GPMC1.S12_P
IL34.DDR.G2.D0_N	NT520	A B	GPMC1.S12_N
IL34.DDR.G2.D1_P	NT521	A B	GPMC1.S13_P
IL34.DDR.G2.D1_N	NT522	A B	GPMC1.S13_N
IL34.DDR.G2.D2_P	NT523	A B	GPMC1.S14_P
IL34.DDR.G2.D2_N	NT524	A B	GPMC1.S14_N
IL34.DDR.G2.D3_P	NT525	A B	CFG22.D0/MOSI/I00
IL34.DDR.G2.D3_N	NT526	A B	CFG32.WRITEN
IL34.DDR.G2.D4_P	NT527	A B	CFG03.D0/MOSI/I00
IL34.DDR.G2.D4_N	NT528	A B	CFG03.WRITEN
IL34.DDR.G2.S_P	NT529	A B	CFG13.D0MOSI/I00
IL34.DDR.G2.S_N	NT530	A B	CFG13.WRITEN
IL34.DDR.G3.D0_P	NT531	A B	CFG23.D0/MOSI/I00
IL34.DDR.G3.D0_N	NT532	A B	CFG23.WRITEN
IL34.DDR.G3.D1_P	NT533	A B	CFG33.D0MOSI/I00
IL34.DDR.G3.D1_N	NT534	A B	CFG33.WRITEN
IL34.DDR.G3.D2_P	NT535	A B	GPMC0.S12_P
IL34.DDR.G3.D2_N	NT536	A B	GPMC0.S12_N
IL34.DDR.G3.D3_P	NT537	A B	GPMC0.S13_P
IL34.DDR.G3.D3_N	NT538	A B	GPMC0.S13_N
IL34.DDR.G3.D4_P	NT539	A B	GPMC0.S14_P
IL34.DDR.G3.D4_N	NT540	A B	GPMC0.S14_N
IL34.DDR.VTT	NT622	A B	CFG22.WRITEN

(D1/MISO/I01 IS USED FOR SOFT RESET)  
PIN SWAPPING TO REDUCE ROUTING COMPLEXITY

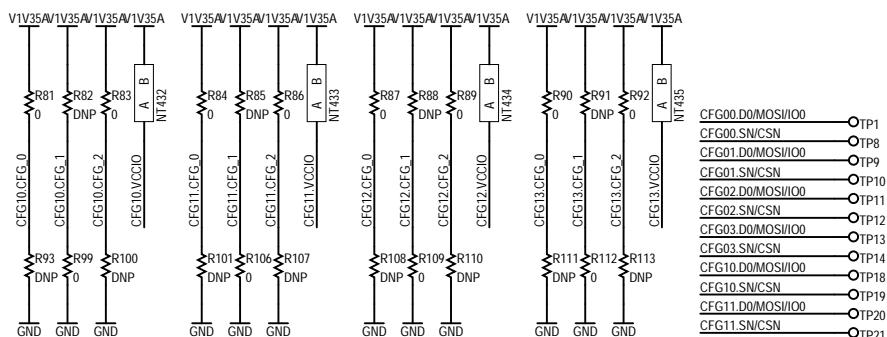


Title	Copper Suicide - Net Tie CFG		
Engineer	J. Brinton	Drawn By	E. Chiu
Revision	1	Sheet	20 of 43

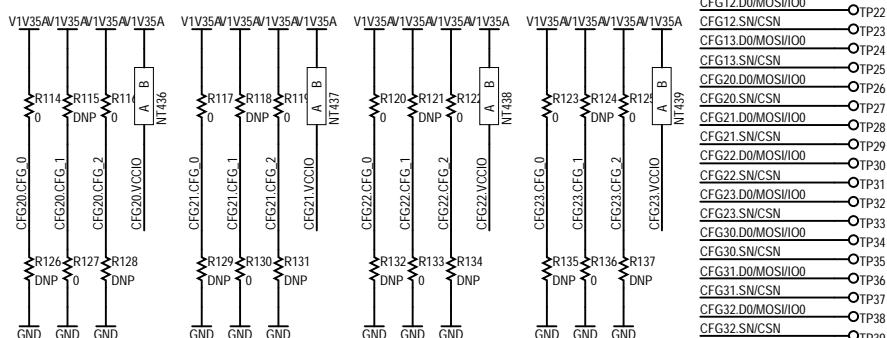
A



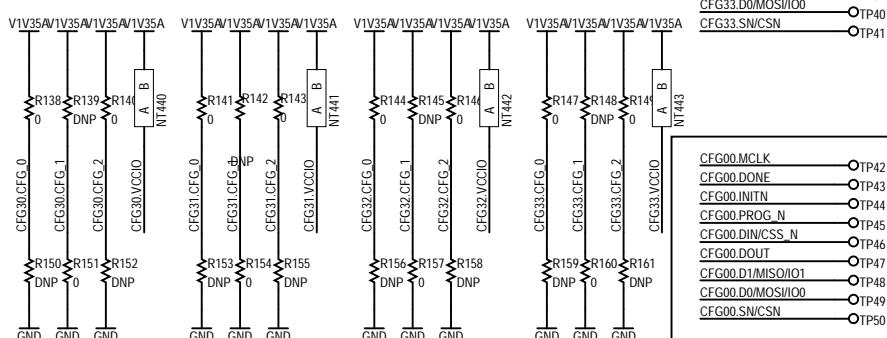
B



C



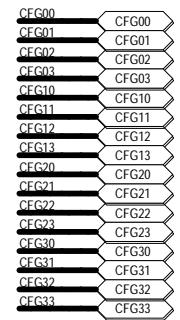
D



CFG[2:0] = 0b101 (Slave Serial Boot)

PCB NOTE: PLACE NEXT TO FPGA #00

CFG00.MCLK	TP42
CFG00.DONE	TP43
CFG00.INITN	TP44
CFG00.PROG_N	TP45
CFG00.DIN/CSS_N	TP46
CFG00.D1/MISO/I01	TP47
CFG00.D0/MOSI/I00	TP48
CFG00.SN/CSN	TP49



## TEMP SENSOR I2C ADDRESS SELECT - I2C BUS A

CFG00.TMP_A00 NT635	A B	GND	0b00 : 7'addr = 0x48
CFG01.TMP_A00 NT637	A B	X	0b0x : 7'addr = 0x49
CFG02.TMP_A00 NT638	A B	V3V3	0b01 : 7'addr = 0x4A
CFG03.TMP_A00 NT640	A B	GND	0b10 : 7'addr = 0x4B
CFG10.TMP_A00 NT642	A B	X	0b1x : 7'addr = 0x4C
CFG11.TMP_A00 NT643	A B	V3V3	0b11 : 7'addr = 0x4D
CFG12.TMP_A00 NT645	A B	GND	0bx0 : 7'addr = 0x4E
CFG13.TMP_A00 NT646	A B	V3V3	0bx1 : 7'addr = 0x4F

## TEMP SENSOR I2C ADDRESS SELECT - I2C BUS B

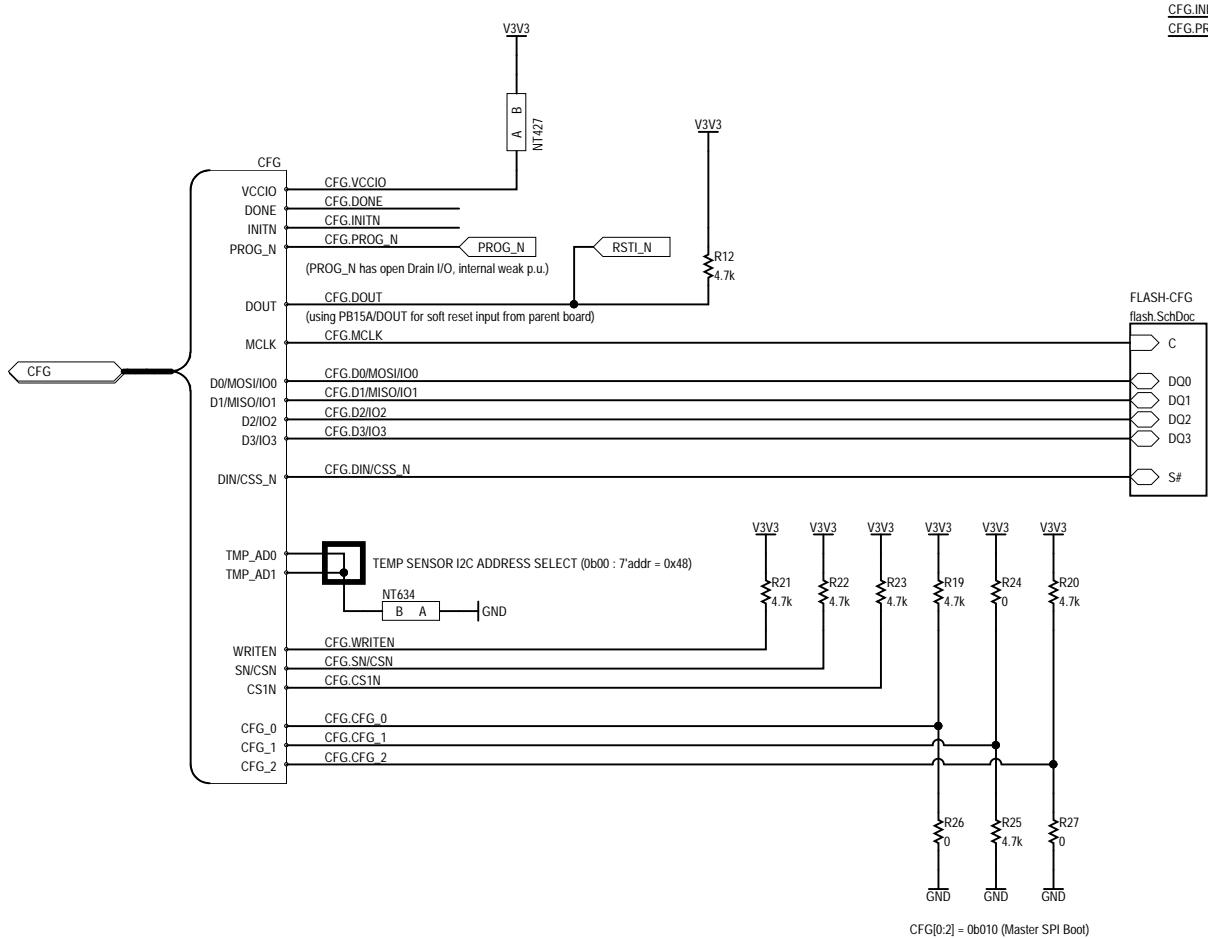
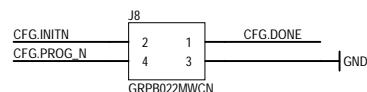
CFG20.TMP_A00 NT647	A B	GND	0b00 : 7'addr = 0x48
CFG20.TMP_A01 NT648	A B	X	0b0x : 7'addr = 0x49
CFG21.TMP_A00 NT649	A B	GND	0b01 : 7'addr = 0x4A
CFG22.TMP_A00 NT650	A B	V3V3	0b10 : 7'addr = 0x4B
CFG22.TMP_A01 NT651	A B	GND	0b11 : 7'addr = 0x4C
CFG23.TMP_A00 NT652	A B	GND	0b1x : 7'addr = 0x4D
CFG23.TMP_A01 NT653	A B	V3V3	0bx0 : 7'addr = 0x4E
CFG30.TMP_A00 NT654	A B	X	0bx1 : 7'addr = 0x4F
CFG31.TMP_A00 NT655	A B	V3V3	0b11 : 7'addr = 0x4D
CFG32.TMP_A00 NT657	A B	GND	0bx0 : 7'addr = 0x4E
CFG33.TMP_A00 NT658	A B	V3V3	0bx1 : 7'addr = 0x4F



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Title <b>Copper Suicide - Config Options</b>		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 21 of 43	Date 10/6/2016

PCB NOTE: Place head next to JTAG per programming header



A

B

C

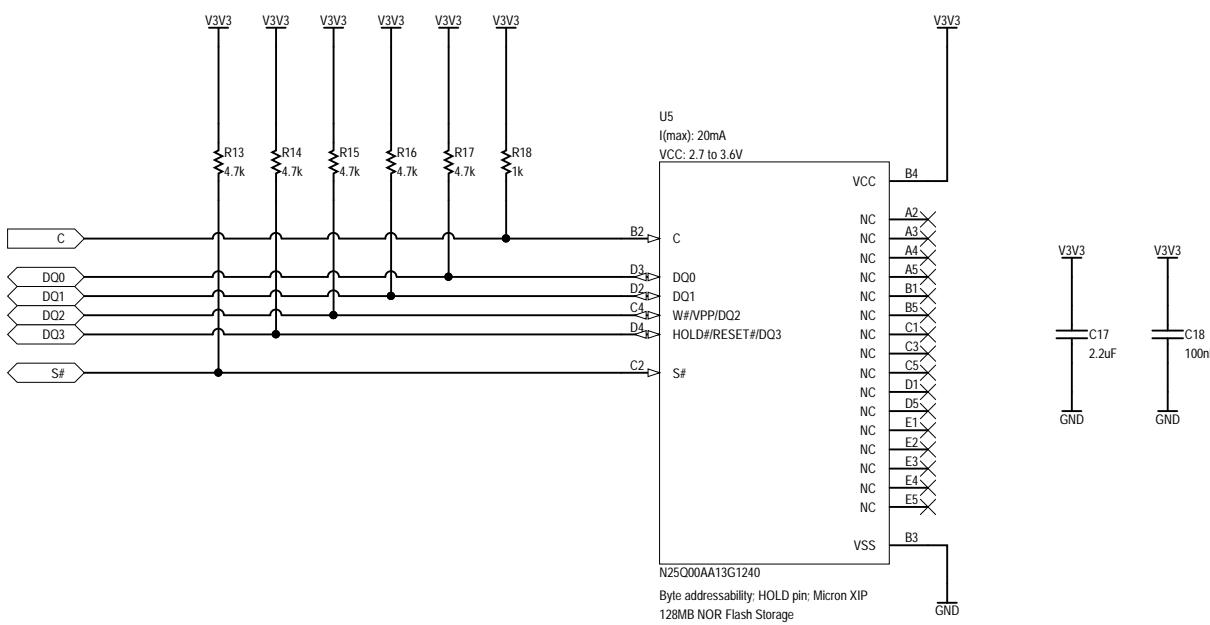
D

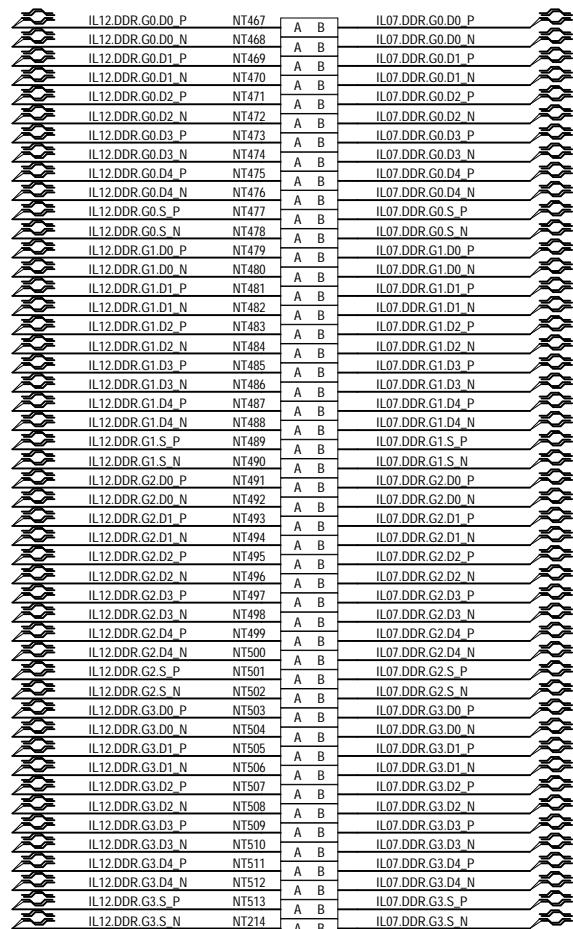
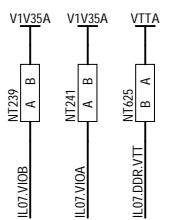
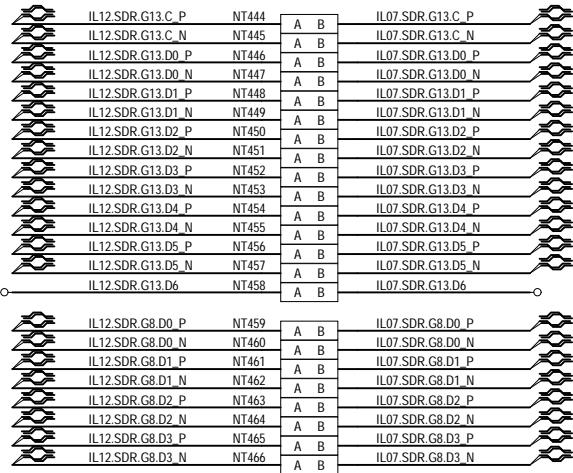
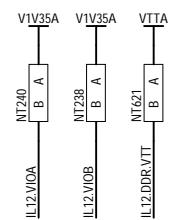
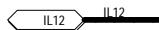
A

B

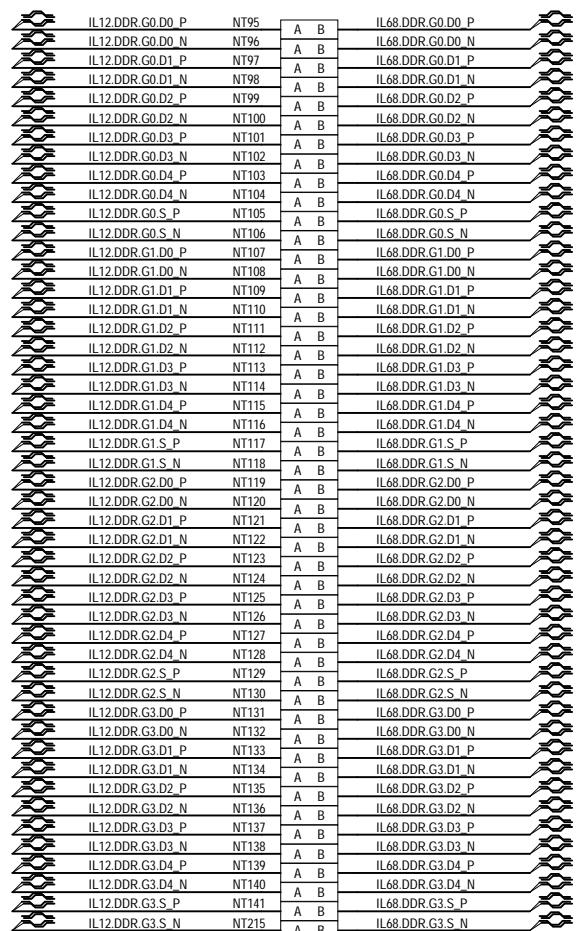
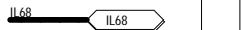
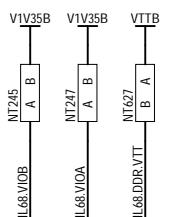
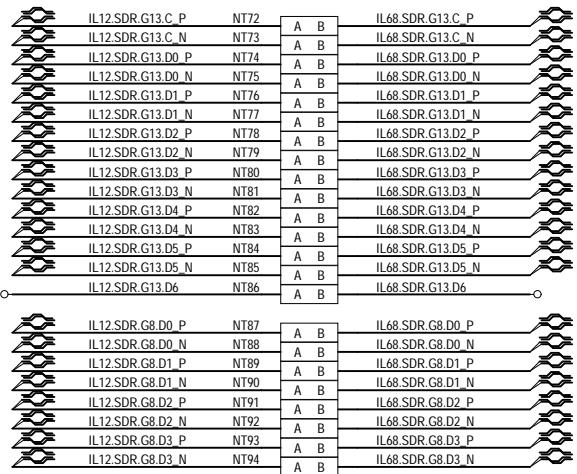
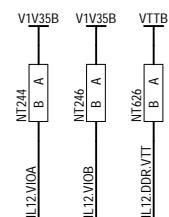
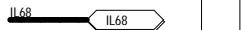
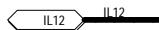
C

D

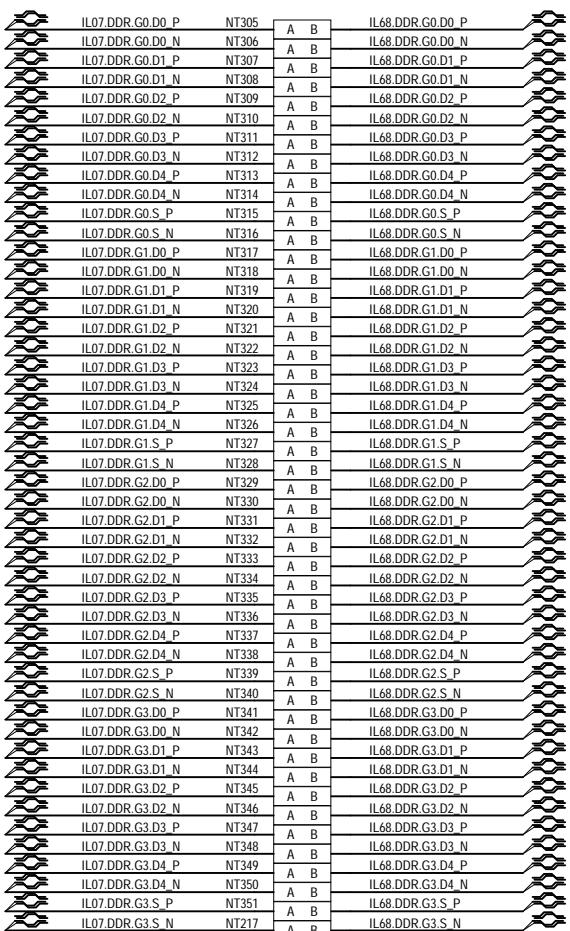
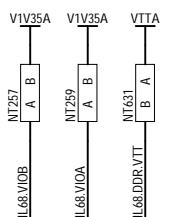
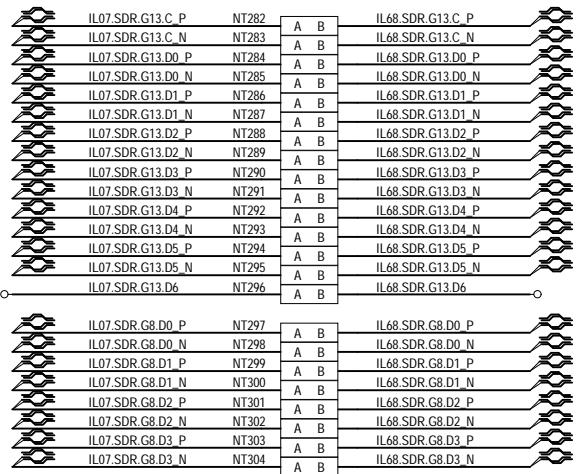
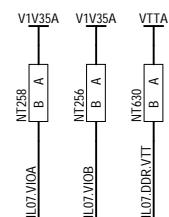
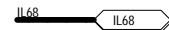
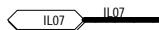




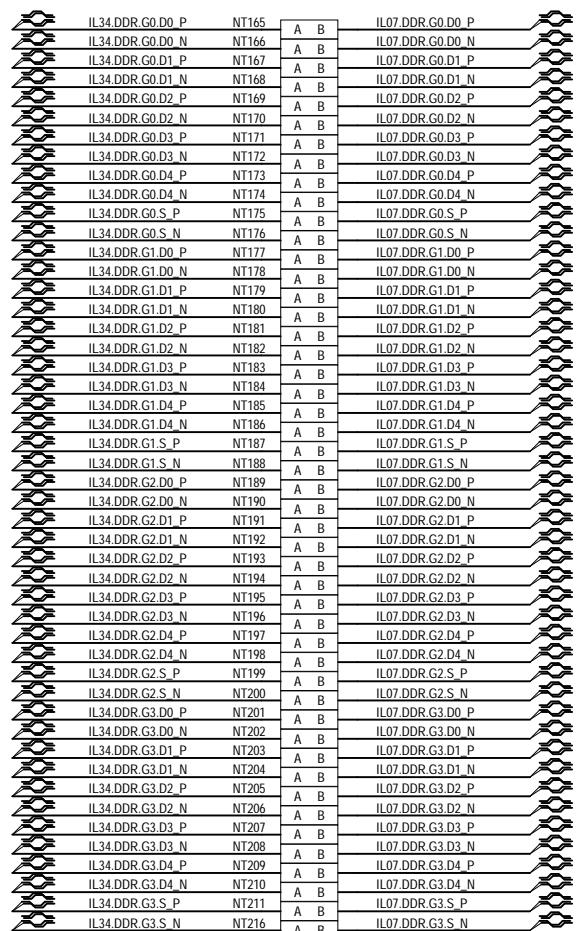
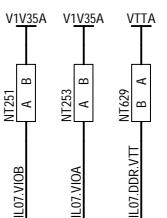
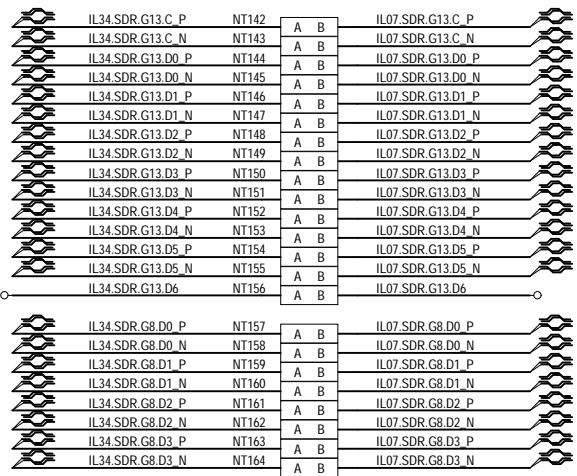
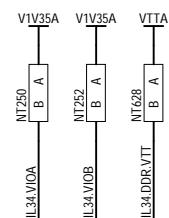
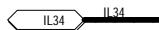
PIN SWAPPING TO REDUCE ROUTING COMPLEXITY



PIN SWAPPING TO REDUCE ROUTING COMPLEXITY

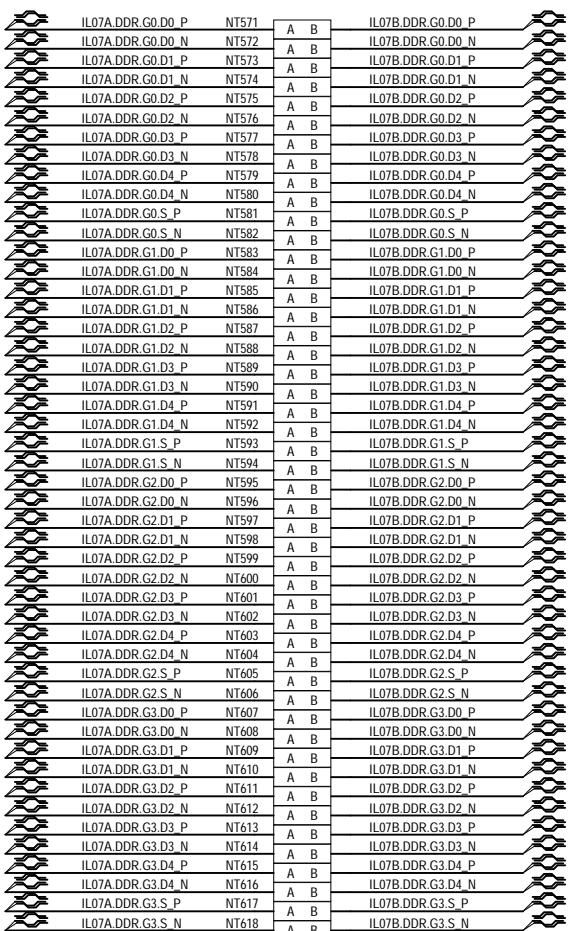
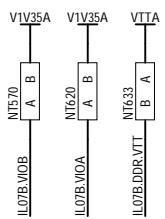
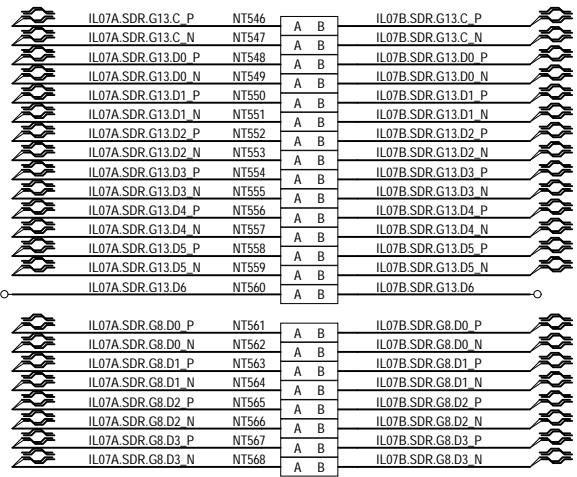
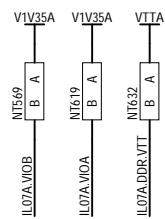
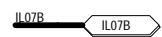
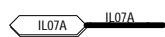


PIN SWAPPING TO REDUCE ROUTING COMPLEXITY



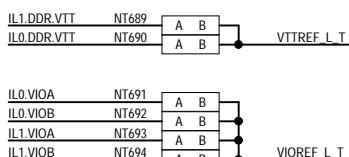
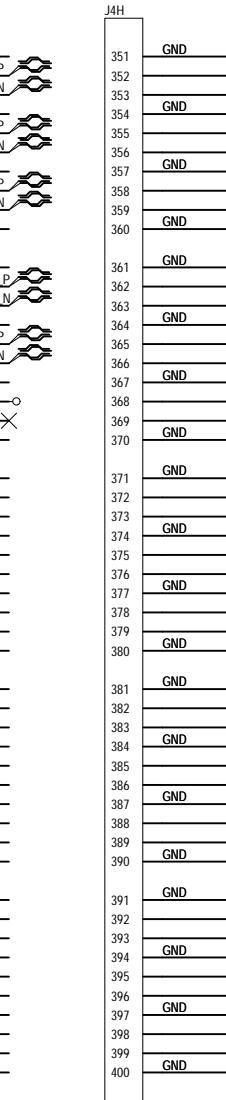
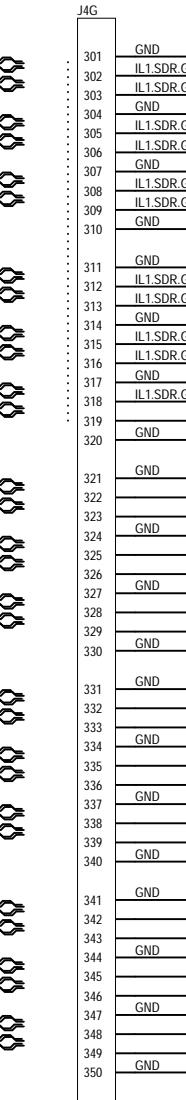
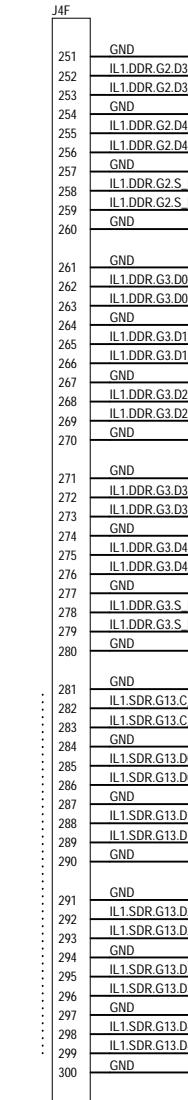
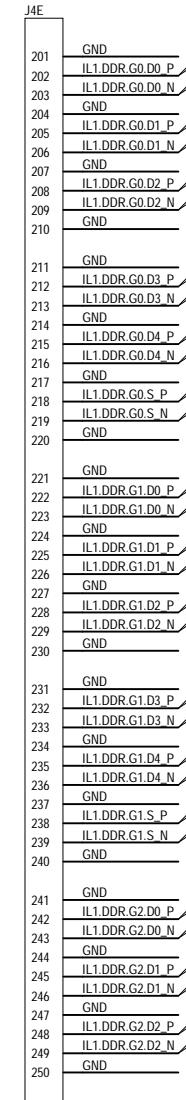
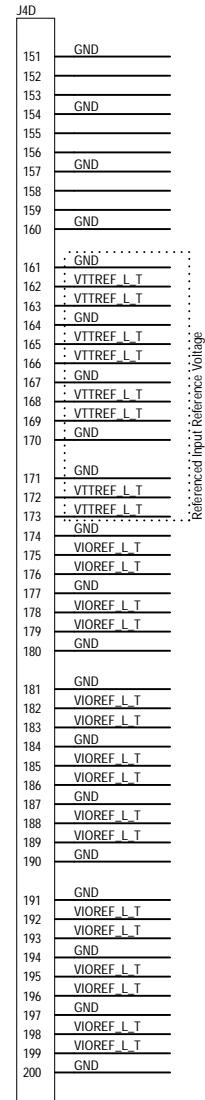
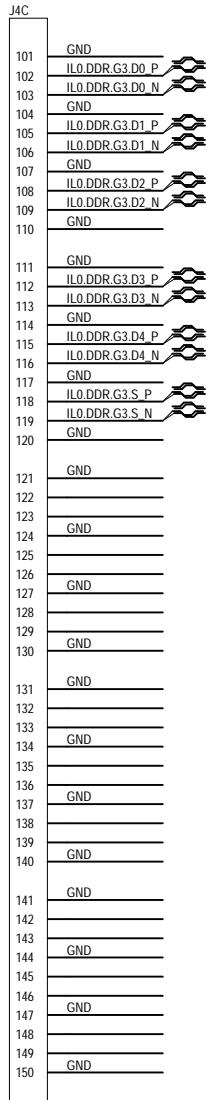
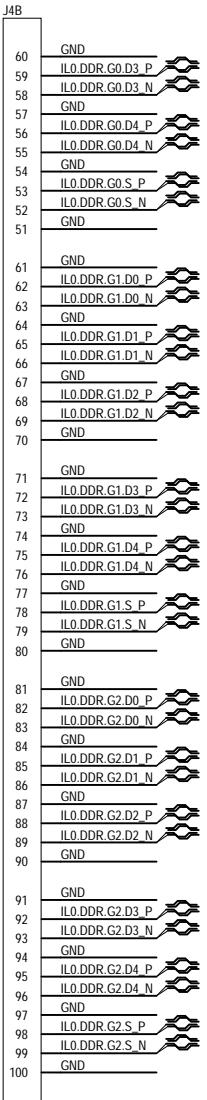
PIN SWAPPING TO REDUCE ROUTING COMPLEXITY

Title		
Copper Suicide - Net Tie 34:07		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 27 of 43	Date 10/6/2016



PIN SWAPPING TO REDUCE ROUTING COMPLEXITY

Copper Suicide - Net Tie 07:07		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 28 of 43	Date 10/6/2016



GND  
GND

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3479 Edison Way  
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siglabs.com

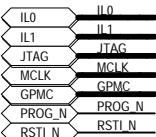
Title: Copper Suicide - Left Top  
Engineer: J. Brinton Drawn By: J. Brinton Checked By: E. Chiu  
Revision: 1 Sheet: 29 of 43 Date: 10/6/2016

1

2

3

4



V48BB  
V48BB

J3A  
SEAM-40-11.0-S-10-2-A-K-TR

1	GND
2	IL0.DDR.G0.D3.P
3	IL0.DDR.G0.D3.N
4	GND
5	IL0.DDR.G0.D4.P
6	IL0.DDR.G0.D4.N
7	GND
8	IL0.DDR.G0.S.P
9	IL0.DDR.G0.S.N
10	GND
11	GND
12	IL0.DDR.G1.D0.P
13	IL0.DDR.G1.D0.N
14	GND
15	IL0.DDR.G1.D1.P
16	IL0.DDR.G1.D1.N
17	GND
18	IL0.DDR.G1.D2.P
19	IL0.DDR.G1.D2.N
20	GND
21	GND
22	IL0.DDR.G1.D3.P
23	IL0.DDR.G1.D3.N
24	GND
25	IL0.DDR.G1.D4.P
26	IL0.DDR.G1.D4.N
27	GND
28	IL0.DDR.G1.S.P
29	IL0.DDR.G1.S.N
30	GND
31	GND
32	IL0.DDR.G2.D0.P
33	IL0.DDR.G2.D0.N
34	GND
35	IL0.DDR.G2.D1.P
36	IL0.DDR.G2.D1.N
37	GND
38	IL0.DDR.G2.D2.P
39	IL0.DDR.G2.D2.N
40	GND
41	GND
42	IL0.DDR.G2.D3.P
43	IL0.DDR.G2.D3.N
44	GND
45	IL0.DDR.G2.D4.P
46	IL0.DDR.G2.D4.N
47	GND
48	IL0.DDR.G2.S.P
49	IL0.DDR.G2.S.N
50	GND

J3B

60	GND
59	IL0.DDR.G3.D0.P
58	IL0.DDR.G3.D0.N
57	GND
56	IL0.DDR.G3.D1.P
55	IL0.DDR.G3.D1.N
54	GND
53	IL0.DDR.G3.D2.P
52	IL0.DDR.G3.D2.N
51	GND
61	GND
62	IL0.DDR.G3.D3.P
63	IL0.DDR.G3.D3.N
64	GND
65	IL0.DDR.G3.D4.P
66	IL0.DDR.G3.D4.N
67	GND
68	IL0.DDR.G3.S.P
69	IL0.DDR.G3.S.N
70	GND
71	GND
72	IL0.DDR.G0.D0.P
73	IL0.DDR.G0.D0.N
74	GND
75	IL0.DDR.G0.D1.P
76	IL0.DDR.G0.D1.N
77	GND
78	IL0.DDR.G0.D2.P
79	IL0.DDR.G0.D2.N
80	GND
81	GND
82	IL0.SDR.G13.C.P
83	IL0.SDR.G13.C.N
84	GND
85	IL0.SDR.G13.D0.P
86	GND
87	IL0.SDR.G13.D1.P
88	IL0.SDR.G13.D1.N
89	GND
90	GND
91	GND
92	IL0.SDR.G13.D2.P
93	IL0.SDR.G13.D2.N
94	GND
95	IL0.SDR.G13.D3.P
96	IL0.SDR.G13.D3.N
97	GND
98	IL0.SDR.G13.D4.P
99	IL0.SDR.G13.D4.N
100	GND

J3C

101	IL0.SDR.G8.D1.P
102	IL0.SDR.G8.D1.N
103	GND
104	IL0.SDR.G8.D2.P
105	IL0.SDR.G8.D2.N
106	GND
107	IL0.SDR.G8.D3.P
108	IL0.SDR.G8.D3.N
109	GND
110	GND
111	GND
112	IL0.SDR.G13.D5.P
113	IL0.SDR.G13.D5.N
114	GND
115	IL0.SDR.G8.D0.P
116	IL0.SDR.G8.D0.N
117	GND
118	IL0.SDR.G13.D6
119	GND
120	GND
121	GND
122	GND
123	GND
124	GND
125	GND
126	GND
127	GND
128	GND
129	GND
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131	GND
132	GND
133	GND
134	GND
135	GND
136	GND
137	GND
138	GND
139	GND
140	GND
141	GND
142	GND
143	GND
144	GND
145	GND
146	GND
147	GND
148	GND
149	GND
150	GND

J3D

151	GPMC.S12.P
152	GPMC.S12.N
153	GND
154	GND
155	GPMC.S13.P
156	GPMC.S13.N
157	GND
158	GPMC.S14.P
159	GPMC.S14.N
160	GND
201	GND
202	GPMC.S9.P
203	GPMC.S9.N
204	GND
205	GPMC.S10.P
206	GPMC.S10.N
207	GND
208	GPMC.S11.P
209	GPMC.S11.N
210	GND
211	GND
212	JTAG.TDI
213	JTAG.TMS
214	GND
215	JTAG.TCK
216	JTAG.TDO
217	GND
218	MCLK.C.P
219	MCLK.C.N
220	GND
221	GND
222	PROG.N
223	RSTI.N
224	V48BB
225	V48BB
226	V48BB
227	GND
228	V48BB
229	V48BB
230	GND
231	GND
232	V48BB
233	V48BB
234	GND
235	V48BB
236	GND
237	V48BB
238	V48BB
239	GND
240	GND
241	V48BB
242	V48BB
243	GND
244	V48BB
245	V48BB
246	GND
247	V48BB
248	V48BB
249	V48BB
250	GND

J3E

251	GPMC.S9.P
252	GPMC.S9.N
253	GND
254	GND
255	GPMC.S1.P
256	GPMC.S1.N
257	GND
258	GPMC.S2.P
259	GPMC.S2.N
260	GND
261	GND
262	GPMC.S3.P
263	GPMC.S3.N
264	GND
265	GPMC.S4.P
266	GPMC.S4.N
267	GND
268	GPMC.S5.P
269	GPMC.S5.N
270	GND
271	GND
272	GPMC.S6.P
273	GPMC.S6.N
274	GND
275	GPMC.S7.P
276	GPMC.S7.N
277	GND
278	GPMC.S8.P
279	GPMC.S8.N
280	GND
281	GND
282	IL0.SDR.G13.C.P
283	IL0.SDR.G13.C.N
284	GND
285	IL0.SDR.G13.D0.P
286	GND
287	IL0.SDR.G13.D1.P
288	IL0.SDR.G13.D1.N
289	GND
290	GND
291	GND
292	IL0.SDR.G13.D2.P
293	IL0.SDR.G13.D2.N
294	GND
295	IL0.SDR.G13.D3.P
296	IL0.SDR.G13.D3.N
297	GND
298	IL0.SDR.G13.D4.P
299	IL0.SDR.G13.D4.N
300	GND

J3F

301	GND
302	IL0.SDR.G13.D5.P
303	IL0.SDR.G13.D5.N
304	GND
305	IL0.SDR.G13.D6
306	GND
307	IL0.SDR.G8.D0.P
308	IL0.SDR.G8.D0.N
309	GND
310	GND
311	GND
312	IL0.SDR.G8.D1.P
313	IL0.SDR.G8.D1.N
314	GND
315	IL0.SDR.G8.D2.P
316	IL0.SDR.G8.D2.N
317	GND
318	IL0.SDR.G8.D3.P
319	IL0.SDR.G8.D3.N
320	GND
321	GND
322	IL1.DDR.G0.D0.P
323	IL1.DDR.G0.D0.N
324	GND
325	IL1.DDR.G0.D1.P
326	IL1.DDR.G0.D1.N
327	GND
328	IL1.DDR.G0.D2.P
329	IL1.DDR.G0.D2.N
330	GND
331	GND
332	IL1.DDR.G3.D0.P
333	IL1.DDR.G3.D0.N
334	GND
335	IL1.DDR.G3.D1.P
336	IL1.DDR.G3.D1.N
337	GND
338	IL1.DDR.G3.D2.P
339	IL1.DDR.G3.D2.N
340	GND
341	GND
342	IL1.DDR.G1.D0.P
343	IL1.DDR.G1.D0.N
344	GND
345	IL1.DDR.G1.D1.P
346	IL1.DDR.G1.D1.N
347	GND
348	IL1.DDR.G1.D2.P
349	IL1.DDR.G1.D2.N
350	GND

J3G

351	IL1.DDR.G1.D3.P
352	IL1.DDR.G1.D3.N
353	GND
354	IL1.DDR.G1.D4.P
355	IL1.DDR.G1.D4.N
356	GND
357	IL1.DDR.G1.L.S.P
358	IL1.DDR.G1.L.S.N
359	GND
360	GND
361	GND
362	IL1.DDR.G2.D0.P
363	IL1.DDR.G2.D0.N
364	GND
365	IL1.DDR.G2.D1.P
366	IL1.DDR.G2.D1.N
367	GND
368	IL1.DDR.G2.D2.P
369	IL1.DDR.G2.D2.N
370	GND
371	GND
372	IL1.DDR.G2.D3.P
373	IL1.DDR.G2.D3.N
374	GND
375	IL1.DDR.G2.D4.P
376	IL1.DDR.G2.D4.N
377	GND
378	IL1.DDR.G2.S.P
379	IL1.DDR.G2.S.N
380	GND
381	GND
382	IL1.DDR.G3.D0.P
383	IL1.DDR.G3.D0.N
384	GND
385	IL1.DDR.G3.D1.P
386	IL1.DDR.G3.D1.N
387	GND
388	IL1.DDR.G3.D2.P
389	IL1.DDR.G3.D2.N
390	GND
391	GND
392	IL1.DDR.G3.D3.P
393	IL1.DDR.G3.D3.N
394	GND
395	IL1.DDR.G3.D4.P
396	IL1.DDR.G3.D4.N
397	GND
398	IL1.DDR.G3.S.P
399	IL1.DDR.G3.S.N
400	GND

J3H

351	IL1.DDR.G1.D3.P
352	IL1.DDR.G1.D3.N
353	GND
354	IL1.DDR.G1.D4.P
355	IL1.DDR.G1.D4.N
356	GND
357	IL1.DDR.G1.L.S.P
358	IL1.DDR.G1.L.S.N
359	GND
360	GND
361	GND
362	IL1.DDR.G2.D0.P
363	IL1.DDR.G2.D0.N
364	GND
365	IL1.DDR.G2.D1.P
366	IL1.DDR.G2.D1.N
367	GND
368	IL1.DDR.G2.D2.P
369	IL1.DDR.G2.D2.N
370	GND
371	GND
372	IL1.DDR.G2.D3.P
373	IL1.DDR.G2.D3.N
374	GND
375	IL1.DDR.G2.D4.P
376	IL1.DDR.G2.D4.N
377	GND
378	IL1.DDR.G2.S.P
379	IL1.DDR.G2.S.N
380	GND
381	GND
382	IL1.DDR.G3.D0.P
383	IL1.DDR.G3.D0.N
384	GND
385	IL1.DDR.G3.D1.P
386	IL1.DDR.G3.D1.N
387	GND
388	IL1.DDR.G3.D2.P
389	IL1.DDR.G3.D2.N
390	GND
391	GND
392	IL1.DDR.G3.D3.P
393	IL1.DDR.G3.D3.N
394	GND
395	IL1.DDR.G3.D4.P
396	IL1.DDR.G3.D4.N
397	GND
398	IL1.DDR.G3.S.P
399	IL1.DDR.G3.S.N
400	GND

A

A

C

C

D



IL1.DDR.VTT NT677  
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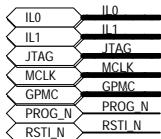
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IL1.VIOA NT681  
IL1.VIOB NT682 A B A B VIREF\_L\_B

GND  
GND



## Copper Suicide - Left Bottom

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	E. Chiu
Revision 1	Sheet 31 of 43	Date 10/6/2016

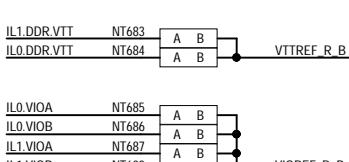


V48BB  
V48BB

A  
J1A  
SEAF-40-06-S-10-2-A-K-TR

1	GND	60	GND	101	GND	151	GND	201	GND	251	GND	301	GND	351	GND
2	IL0.DDR.G0.D3.P	59	IL0.DDR.G3.D0.P	102	IL0.SDR.G8.D1.P	152	GPMC.S12.P	202	GPMC.S9.P	252	GPMC.S0.P	302	IL0.SDR.G13.D5.P	352	IL1.DDR.G1.D3.P
3	IL0.DDR.G0.D3.N	58	IL0.DDR.G3.D0.N	103	IL0.SDR.G8.D1.N	153	GPMC.S12.N	203	GPMC.S9.N	253	GPMC.S0.N	303	IL0.SDR.G13.D5.N	353	IL1.DDR.G1.D3.N
4	GND	57	IL0.DDR.G3.D1.P	104	IL0.SDR.G8.D2.P	154	GND	204	GPMC.S10.P	254	GPMC.S1.P	304	IL0.SDR.G13.D6	354	GND
5	IL0.DDR.G0.D4.P	56	IL0.DDR.G3.D1.N	105	IL0.SDR.G8.D2.N	155	GND	205	GPMC.S10.N	255	GPMC.S1.N	305	GND	355	IL1.DDR.G1.D4.P
6	IL0.DDR.G0.D4.N	55	GND	106	IL0.SDR.G8.D3.P	156	GND	206	GPMC.S11.P	256	GPMC.S2.P	306	GND	356	IL1.DDR.G1.D4.N
7	GND	54	IL0.DDR.G3.D2.P	107	IL0.SDR.G8.D3.N	157	GND	207	GPMC.S11.N	257	GPMC.S2.N	307	GND	357	GND
8	IL0.DDR.G0.S.P	53	IL0.DDR.G3.D2.N	108	IL0.SDR.G8.D3.N	158	GPMC.S14.P	208	GPMC.S11.P	258	GPMC.S2.N	308	IL0.SDR.G8.D0.N	358	IL1.DDR.G1.S.P
9	IL0.DDR.G0.S.N	52	GND	109	GND	159	GPMC.S14.N	209	GPMC.S11.N	259	GND	309	GND	359	IL1.DDR.G1.S.N
10	GND	51	GND	110	GND	160	GND	210	GND	260	GND	310	GND	360	GND
11	GND	61	GND	111	GND	161	GND	211	GND	261	GND	311	GND	361	GND
12	IL0.DDR.G1.D0.P	62	IL0.DDR.G3.D3.P	112	IL0.SDR.G13.D5.P	162	: VITREF.R.B	212	JTAG.TDI	262	GPMC.S3.P	312	IL0.SDR.G8.D1.P	362	IL1.DDR.G2.D0.P
13	IL0.DDR.G1.D0.N	63	IL0.DDR.G3.D3.N	113	IL0.SDR.G13.D5.N	163	: VITREF.R.B	213	JTAG.TMS	263	GPMC.S3.N	313	IL0.SDR.G8.D1.N	363	IL1.DDR.G2.D0.N
14	GND	64	GND	114	GND	164	: GND	214	JTAG.TCK	264	GND	314	GND	364	GND
15	IL0.DDR.G1.D1.P	65	IL0.DDR.G3.D4.P	115	IL0.SDR.G8.D0.P	165	: VITREF.R.B	215	JTAG.TDO	265	GPMC.S4.P	315	IL0.SDR.G8.D2.P	365	IL1.DDR.G2.D1.P
16	IL0.DDR.G1.D1.N	66	IL0.DDR.G3.D4.N	116	IL0.SDR.G8.D0.N	166	: GND	216	GND	266	GPMC.S4.N	316	IL0.SDR.G8.D2.N	366	IL1.DDR.G2.D1.N
17	GND	67	GND	117	IL0.SDR.G13.D6	167	: VITREF.R.B	217	MCLK.C.P	267	GND	317	GND	367	GND
18	IL0.DDR.G1.D2.P	68	IL0.DDR.G3.S.P	118	IL0.SDR.G13.D6	168	: VITREF.R.B	218	MCLK.C.N	268	GPMC.S5.P	318	IL0.SDR.G8.D3.P	368	IL1.DDR.G2.D2.P
19	IL0.DDR.G1.D2.N	69	IL0.DDR.G3.S.N	119	GND	169	: GND	219	GND	269	GPMC.S5.N	319	IL0.SDR.G8.D3.N	369	IL1.DDR.G2.D2.N
20	GND	70	GND	120	GND	170	: Reference Input Reference Voltage	220	GND	270	GND	320	GND	370	GND
21	GND	71	GND	121	GND	171	: VITREF.R.B	221	PROG.N	271	GND	321	GND	371	GND
22	IL0.DDR.G1.D3.P	72	IL0.DDR.G0.D0.P	122	GND	172	: VITREF.R.B	222	RSTI.N	272	GPMC.S6.P	322	IL1.DDR.G0.D0.P	372	IL1.DDR.G2.D3.P
23	IL0.DDR.G1.D3.N	73	IL0.DDR.G0.D0.N	123	GND	173	: VITREF.R.B	223	GND	273	GPMC.S6.N	323	IL1.DDR.G0.D0.N	373	IL1.DDR.G2.D3.N
24	GND	74	GND	124	GND	174	GND	224	V48BB	274	GND	324	GND	374	GND
25	IL0.DDR.G1.D4.P	75	IL0.DDR.G0.D1.P	125	GND	175	: VIREF.R.B	225	V48BB	275	GPMC.S7.P	325	IL1.DDR.G0.D1.P	375	IL1.DDR.G2.D4.P
26	IL0.DDR.G1.D4.N	76	IL0.DDR.G0.D1.N	126	GND	176	: VIREF.R.B	226	V48BB	276	GPMC.S7.N	326	IL1.DDR.G0.D1.N	376	IL1.DDR.G2.D4.N
27	GND	77	GND	127	GND	177	GND	227	GND	277	GND	327	GND	377	GND
28	IL0.DDR.G1.S.P	78	IL0.DDR.G0.D2.P	128	GND	178	: VIREF.R.B	228	V48BB	278	GPMC.S8.P	328	IL1.DDR.G0.D2.P	378	IL1.DDR.G2.S.P
29	IL0.DDR.G1.S.N	79	IL0.DDR.G0.D2.N	129	GND	179	: VIREF.R.B	229	V48BB	279	GPMC.S8.N	329	IL1.DDR.G0.D2.N	379	IL1.DDR.G2.S.N
30	GND	80	GND	130	GND	180	GND	230	GND	280	GND	330	GND	380	GND
31	GND	81	GND	131	GND	181	GND	231	GND	281	IL0.SDR.G13.C.P	331	GND	381	GND
32	IL0.DDR.G2.D0.P	82	IL0.SDR.G13.C.N	132	GND	182	: VIREF.R.B	232	V48BB	282	IL0.SDR.G13.C.N	332	IL1.DDR.G3.D0.P	382	IL1.DDR.G3.D0.N
33	IL0.DDR.G2.D0.N	83	IL0.SDR.G13.C.N	133	GND	183	: VIREF.R.B	233	GND	283	GND	333	GND	383	GND
34	GND	84	GND	134	GND	184	GND	234	V48BB	284	GND	334	GND	384	GND
35	IL0.DDR.G2.D1.P	85	IL0.SDR.G13.D0.P	135	GND	185	: VIREF.R.B	235	V48BB	285	IL0.SDR.G13.D0.P	335	IL1.DDR.G0.D4.P	385	IL1.DDR.G3.D1.P
36	IL0.DDR.G2.D1.N	86	IL0.SDR.G13.D0.N	136	GND	186	: VIREF.R.B	236	GND	286	IL0.SDR.G13.D0.N	336	IL1.DDR.G0.D4.N	386	IL1.DDR.G3.D1.N
37	GND	87	GND	137	GND	187	GND	237	V48BB	287	IL0.SDR.G13.D1.P	337	GND	387	GND
38	IL0.DDR.G2.D2.P	88	IL0.SDR.G13.D1.P	138	GND	188	: VIREF.R.B	238	V48BB	288	IL0.SDR.G13.D1.N	338	IL1.DDR.G0.S.P	388	IL1.DDR.G3.D2.P
39	IL0.DDR.G2.D2.N	89	IL0.SDR.G13.D1.N	139	GND	189	: VIREF.R.B	239	GND	289	GND	339	IL1.DDR.G0.S.N	389	IL1.DDR.G3.D2.N
40	GND	90	GND	140	GND	190	GND	240	GND	290	GND	340	GND	390	GND
41	GND	91	GND	141	GND	191	GND	241	V48BB	291	IL0.SDR.G13.D2.P	341	GND	391	GND
42	IL0.DDR.G2.D3.P	92	IL0.SDR.G13.D2.P	142	GND	192	: VIREF.R.B	242	V48BB	292	IL0.SDR.G13.D2.N	342	IL1.DDR.G1.D0.P	392	IL1.DDR.G3.D3.P
43	IL0.DDR.G2.D3.N	93	IL0.SDR.G13.D2.N	143	GND	193	: VIREF.R.B	243	GND	293	GND	343	GND	393	GND
44	GND	94	GND	144	GND	194	GND	244	V48BB	294	IL0.SDR.G13.D3.P	344	GND	394	GND
45	IL0.DDR.G2.D4.P	95	IL0.SDR.G13.D3.P	145	GND	195	: VIREF.R.B	245	V48BB	295	IL0.SDR.G13.D3.N	345	IL1.DDR.G1.D1.P	395	IL1.DDR.G3.D4.P
46	IL0.DDR.G2.D4.N	96	IL0.SDR.G13.D3.N	146	GND	196	: VIREF.R.B	246	GND	296	GND	346	IL1.DDR.G1.D1.N	396	IL1.DDR.G3.D4.N
47	GND	97	GND	147	GND	197	: VIREF.R.B	247	V48BB	297	IL0.SDR.G13.D4.P	347	GND	397	IL1.DDR.G3.S.P
48	IL0.DDR.G2.S.P	98	IL0.SDR.G13.D4.P	148	GND	198	: VIREF.R.B	248	V48BB	298	IL0.SDR.G13.D4.N	348	IL1.DDR.G1.D2.N	398	IL1.DDR.G3.S.N
49	IL0.DDR.G2.S.N	99	IL0.SDR.G13.D4.N	149	GND	199	GND	249	GND	299	GND	349	GND	399	GND
50	GND	100	GND	150	GND	200	GND	250	GND	300	GND	350	GND	400	GND

GND  
GND



Title

## Copper Suicide - Right Bottom

Engineer  
J. Brinton

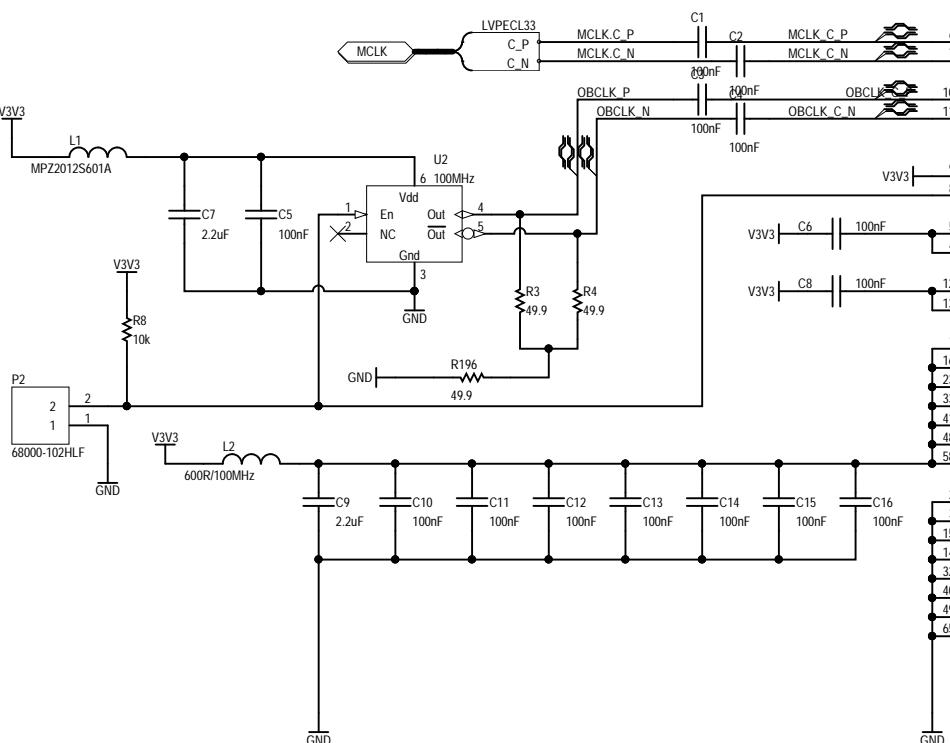
Drawn By  
E. Chiu

Checked By  
Date  
10/6/2016

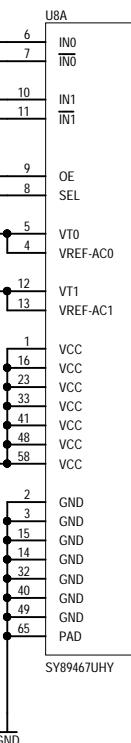
Revision  
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Sheet 32 of 43

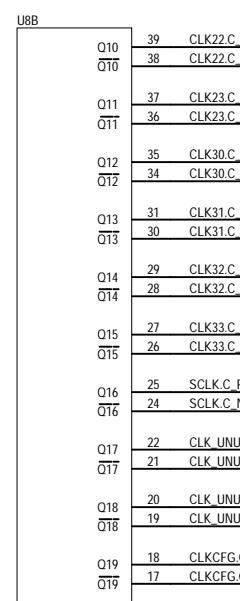
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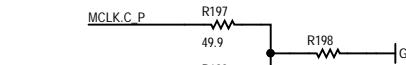
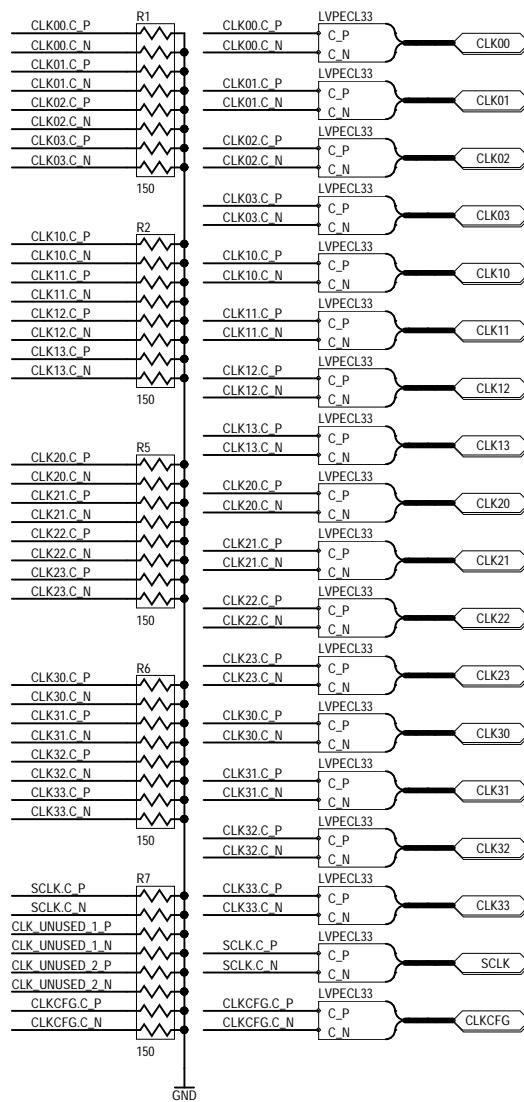
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C



SY89467UHY



A

A

B

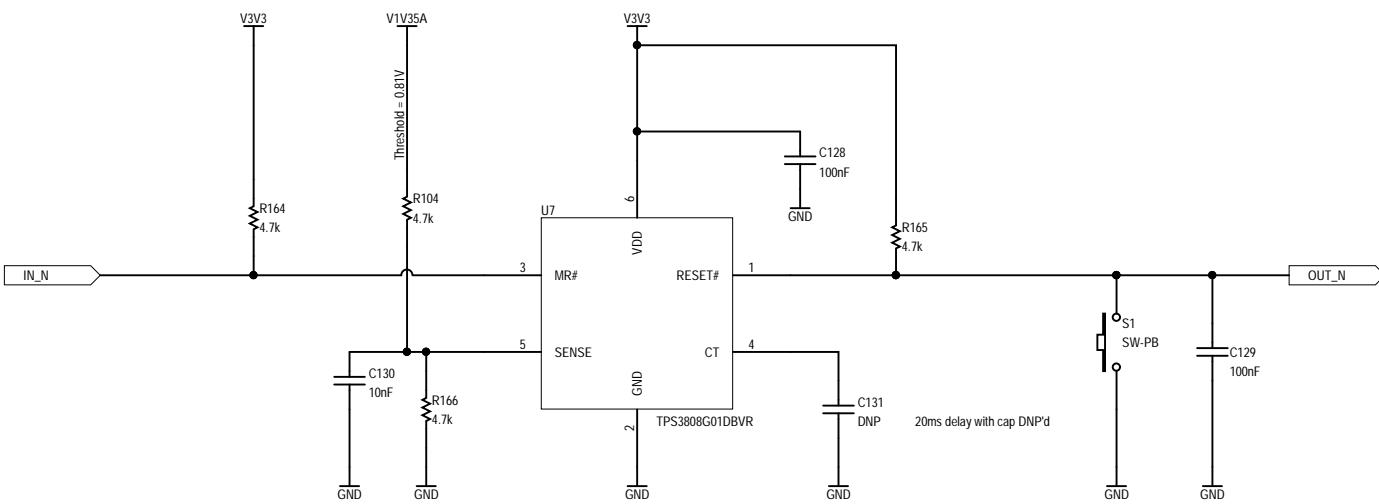
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C

C

D

D



A

B

C

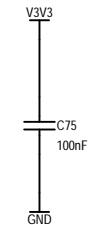
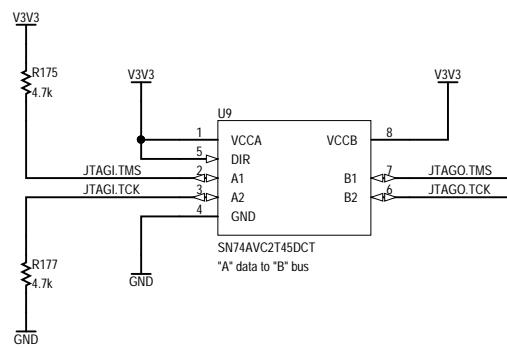
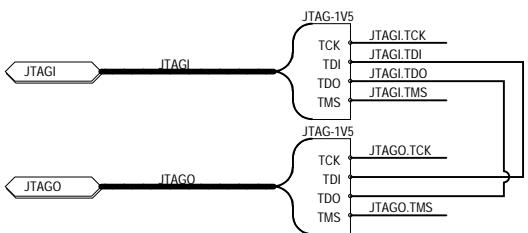
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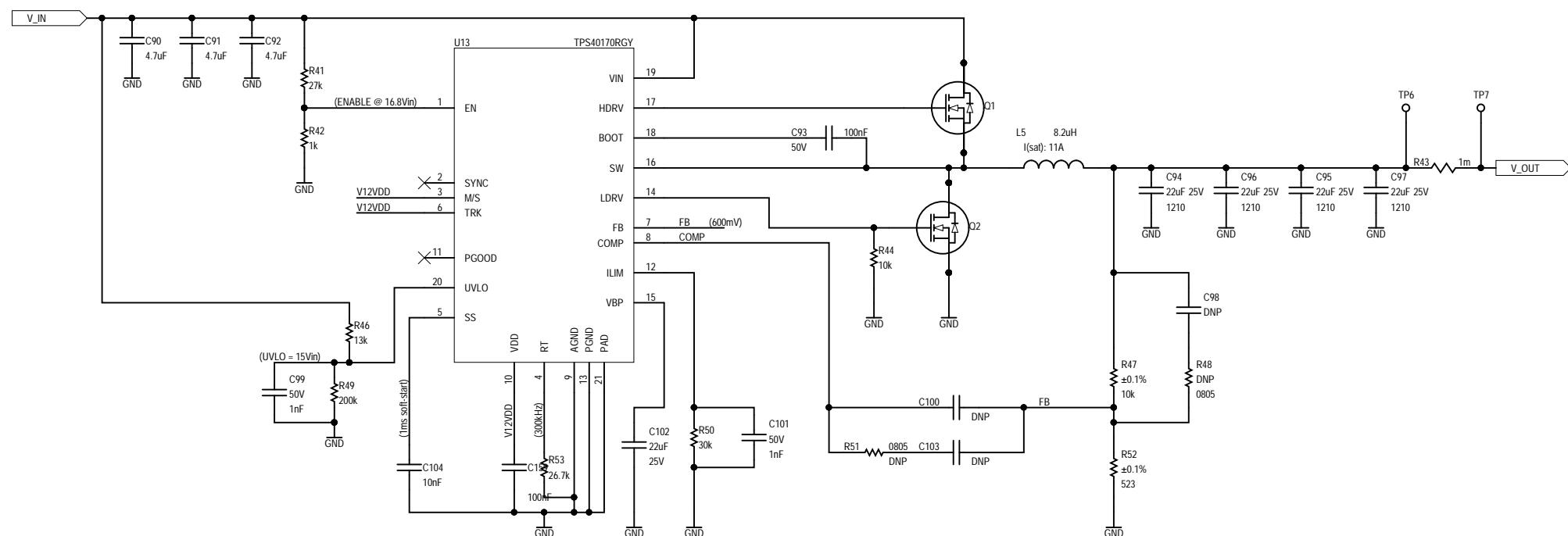
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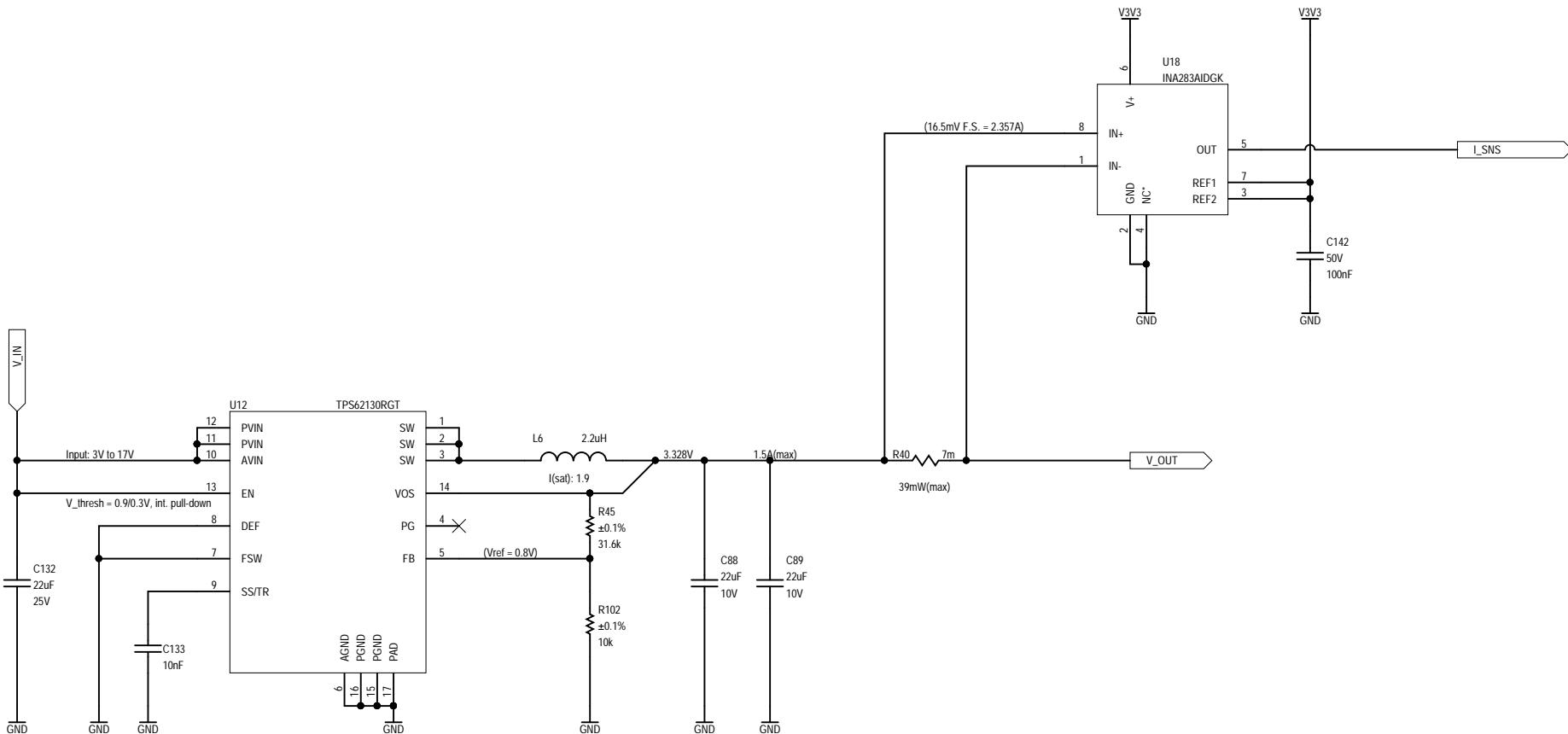
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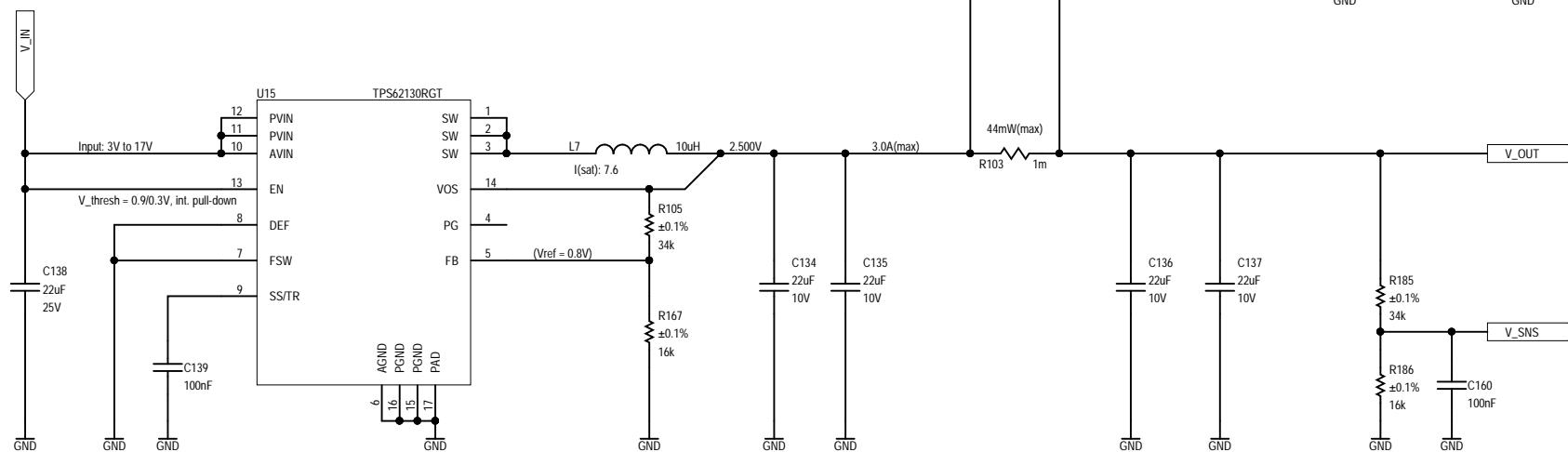
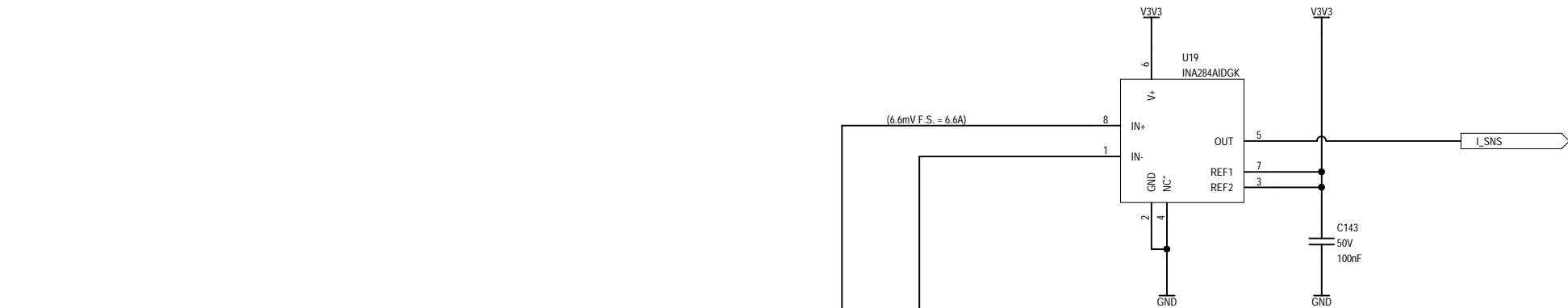
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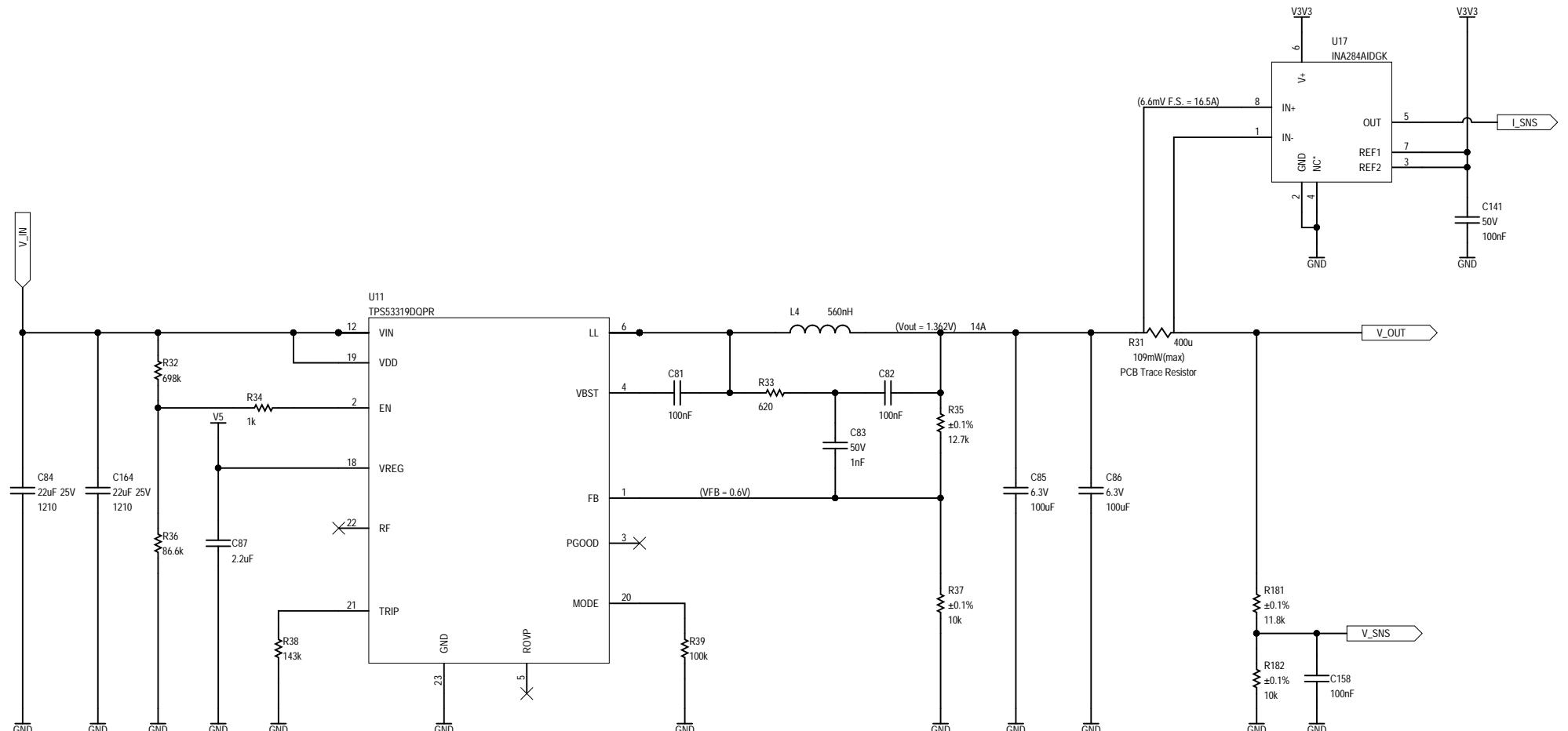






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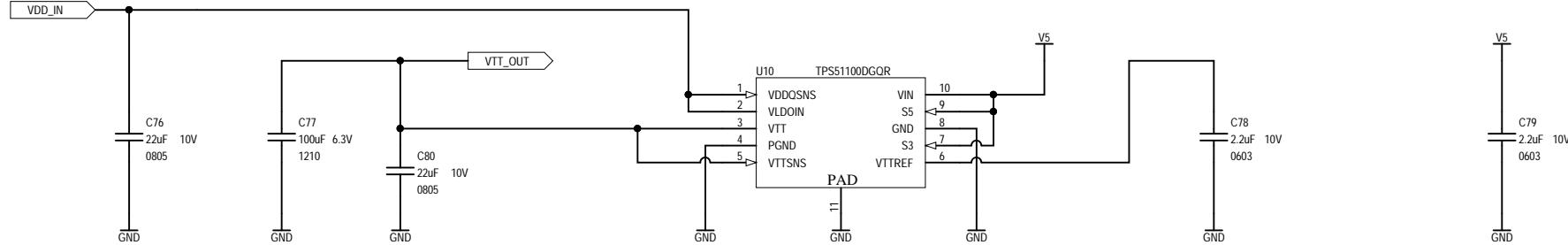
<b>Copper Suicide - Power 2.5V</b>		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 38 of 43	Date 10/6/2016



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Title	Copper Suicide - Power 1.35V		
Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu	
Revision 1	Sheet 39 of 43	Date 10/6/2016	

A



B

C

D

A

B

C

D

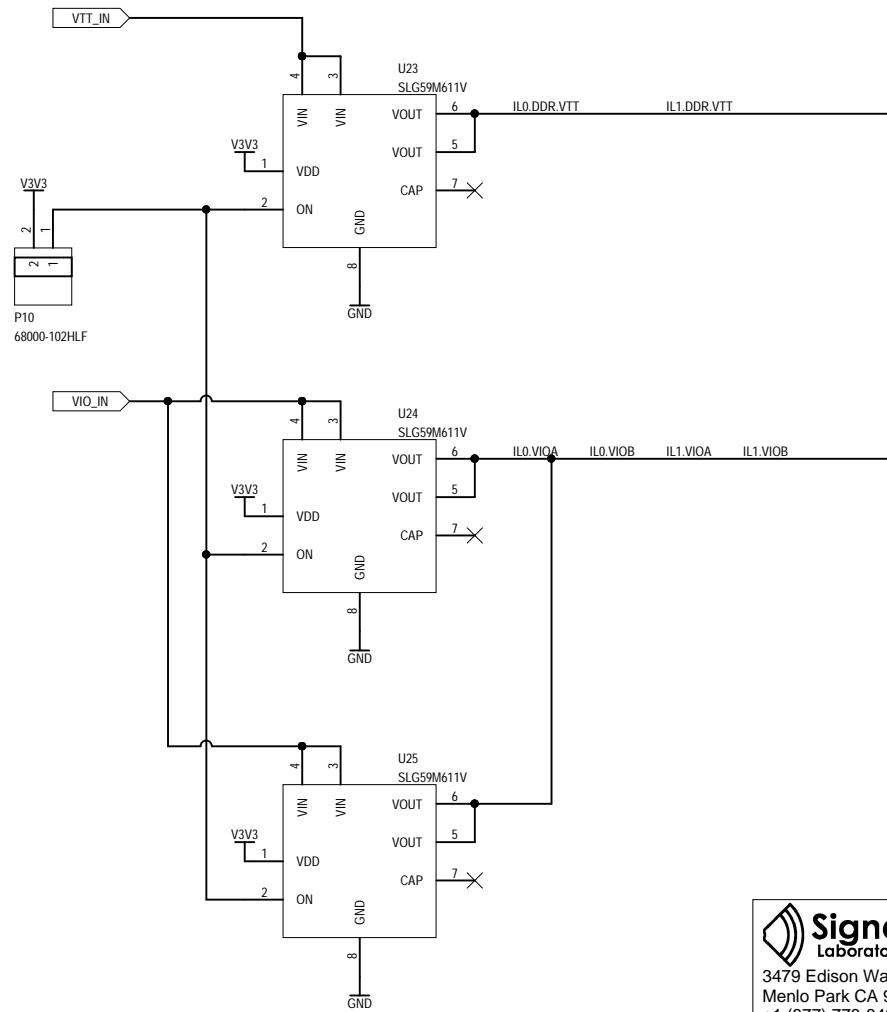
A

A



B

B



C

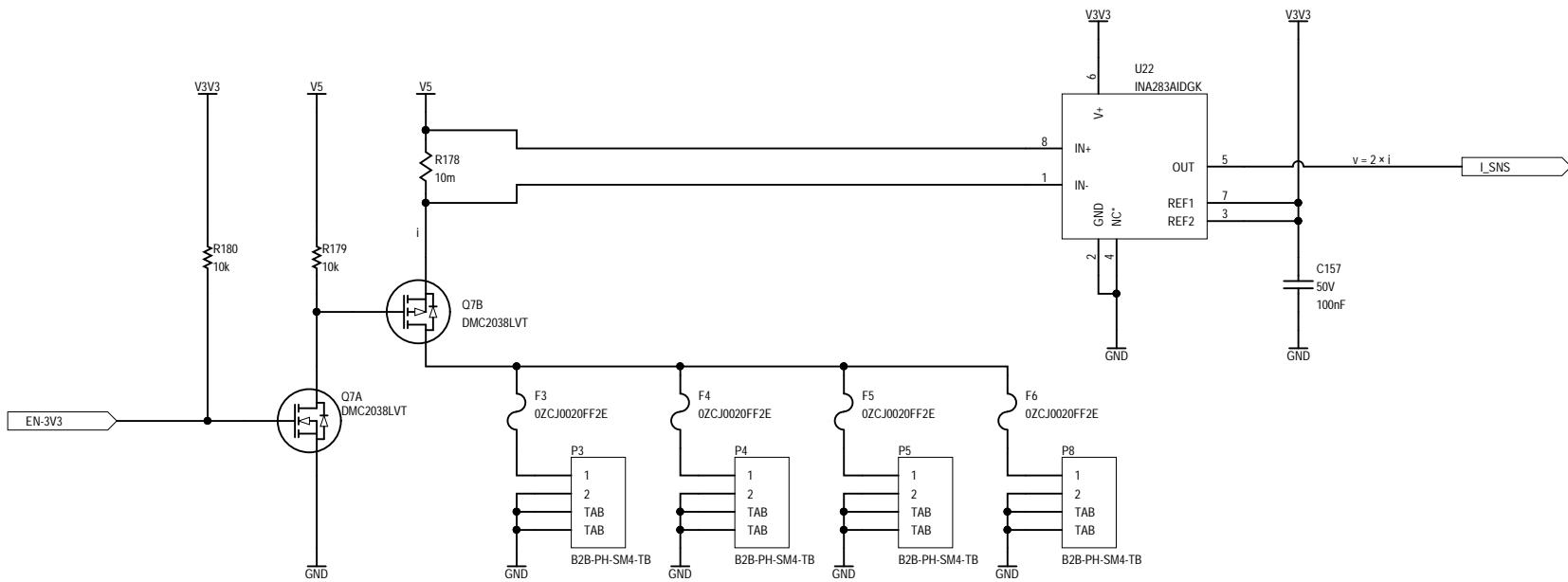
C

MISC10  
M50-1900005

D

D

A



B

C

D

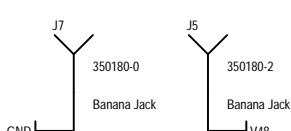
A

B

C

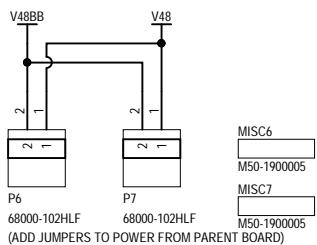
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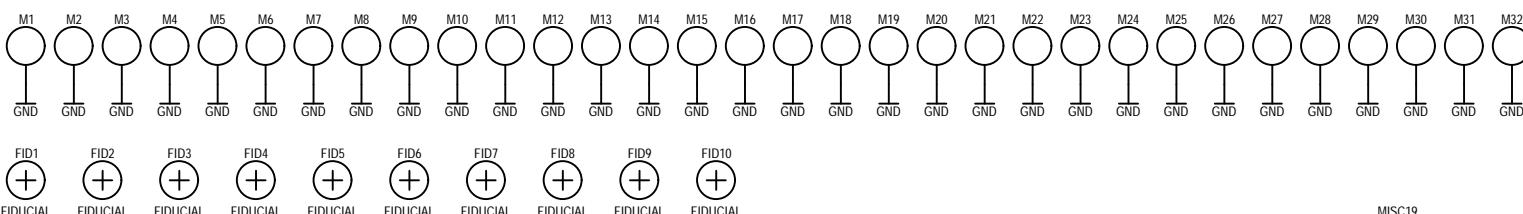
MISC18  
Pomona  
2269-0

B



(ADD JUMPERS TO POWER FROM PARENT BOARD)

C



MISC19

D



## Title

# Copper Suicide - Mechanical

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Engineer J. Brinton	Drawn By J. Brinton	Checked By E. Chiu
Revision 1	Sheet 43 of 43	Date 10/6/2016