October 18, 2002

ERRATA
TO
JEDEC STANDARD

JESD8-9B, - ADDENDUM No. 9B to JESD8 - STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2)

REASON FOR ERRATA: Days after publication of this standard in May 2002, it was brought to the attention of the sponsor that there were errors in Table 4. After further investigation by the sponsor it was noted that during the transfer of numbers from the worksheet to FrameMaker a couple of typo's had been introduced. These typo's had gone unnoticed through the complete ballot process. The sponsor presented the corrected numbers to the committee at it's September 2002 meeting and Table 4 as corrected was approved.

HARD COPY: All recipients of this errata are asked to replace page 7 with the corrected page included in this errata.

ELECTRONIC: If you have downloaded the file prior to date of errata please reprint page 7. The sheet has been corrected in the downloadable file on the JEDEC website as of October 18, 2002.

The standard in question can be downloaded at no charge from the JEDEC web site at www.jedec.org.

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JEDEC STANDARD

Stub Series Terminated Logic for 2.5 V (SSTL_2)

JESD8-9B

(Revision of JESD8-9A)

MAY 2002

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2)

A 2.5 V Supply Voltage Based Interface Standard for Digital Integrated Circuits

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STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2)
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Foreword

The folowing changes are included in this revision: Reduction of V_{IH}/V_{IL} (AC) from 350 mV to 310 mV and of V_{IL}/V_{IH} (DC) from 180 mV to 150 mV (single ended applications); increase of driver current from 15.4 mA (7.6 mA) to 16.2 mA (8.1 mA); reduction of V_{IH}/V_{IL} (AC) from 700 mV to 620 mV and of V_{IH}/V_{IL} (DC) from 360 mV to 300 mV (differential applications.); recalculation of Table 4.

STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2)
A 2.5 V Supply Voltage Based Interface Standard for Digital Integrated Circuits

(From JEDEC Board Ballots JCB-97-80 and JCB-98-80 (section 5), and JCB-01-87, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_2 logic switching range, nominally 0 V to 2.5 V. The standard may be applied to ICs operating with separate V_{DD} and V_{DDQ} supply voltages. In many cases V_{DD} and V_{DDQ} will have the same voltage level. The V_{DD} value is not specified in this standard other than that V_{DDQ} value may not exceed that of V_{DD}.

1.1 Standard structure

The standard is defined in three clauses:

The first clause defines pertinent supply voltage requirements common to all compliant ICs.

The second clause defines the minimum dc and ac input parametric requirements and ac test conditions for inputs on compliant devices.

The third clause specifies the minimum required output characteristics of, and ac test conditions for, compliant outputs targeted for various application environments. The output specifications are divided into two classes, Class I and Class II, which are distinguished by drive requirements and application.

A given IC need not be equipped with both classes of output drivers, but each must support at least one to claim SSTL_2 output compliance.

The full input reference level (V_{REF}) range specified is required on each IC in order to allow any SSTL_2 IC to receive signals from any SSTL_2 output driver.

1.2 Rationale and assumptions

This standard has been developed particularly with the objective of providing a relatively simple upgrade path from MOS push-pull interface designs. The standard is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs. External resistors provide this isolation and also reduce the on-chip power dissipation of the drivers. Busses may be terminated by resistors to an external termination voltage.

1 Scope (cont'd)

1.2 Rationale and assumptions (cont'd)

Actual selection of the resistor values is a system design decision and beyond the scope of this standard. However in order to provide a basis, the driver characteristics will be derived in terms of a typical 50 Ω environment.

While driver characteristics are derived from a 50 Ω environment, this standard will work for other impedance levels. The system designer will be able to vary impedance levels, termination resistors and supply voltage and be able to calculate the effect on system voltage margins. This is accomplished precisely because drivers and receivers are specified independently of each other. The standard defines a reference voltage V_{REF} which is used at the receivers as well as a voltage V_{TT} to which termination resistors are connected. In typical applications V_{TT} tracks as a ratio of V_{DDQ}. In turn V_{REF} will be given the value of V_{TT}. In some standards this ratio equals 0.5.

2 Supply voltage and logic input levels

The standard defines both ac and dc input signal values. Making this distinction is important for the design of high gain, differential, receivers that are required. The ac values are chosen to indicate the levels at which the receiver must meet its timing specifications. The dc values are chosen such that the final logic state is unambiguously defined, that is once the receiver input has crossed this value, the receiver will change to and maintain the new logic state. The reason for this approach is that many input wave-forms will include a certain amount of "ringing". The system designer can be sure that the device will switch state a certain amount of time after the input has crossed ac threshold and not switch back as long as the input stays beyond the dc threshold. The relationship of the different levels is shown in figure 1. An example of ringing is illustrated in the dotted wave-form.

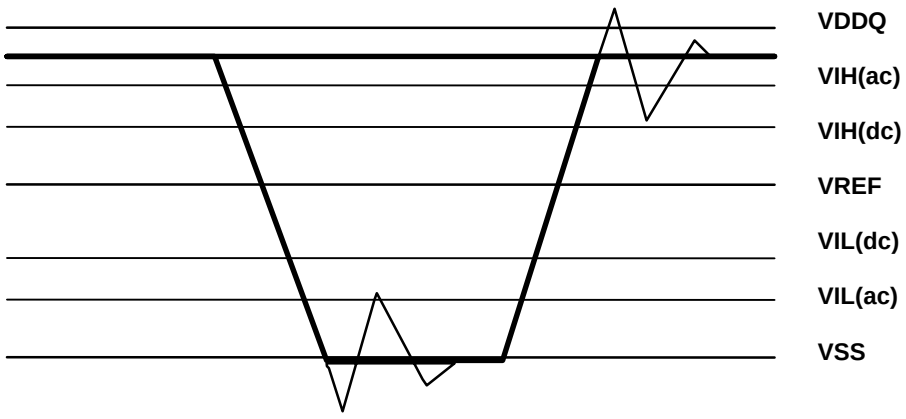

Figure 1 — SSTL_2 input voltage levels

2 Supply voltage and logic input levels (cont'd)

2.1 Supply voltage levels

Table 1 — Supply voltage levels

Symbol	Parameter	Min.	Nom	Max.	Units	Notes
V_{DD}	Device supply voltage	V_{DDQ}		n/a	V	1
V_{DDQ}	Output supply voltage	2.3	2.5	2.7	V	1
$V_{REF(DC)}$	Input reference voltage	1.13	1.25	1.38	V	2, 3
V_{TT}	Termination voltage	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	4

NOTE 1 There is no specific device V_{DD} supply voltage requirement for SSTL_2 compliance. However under all conditions V_{DDQ} must be less than or equal to V_{DD}.

NOTE 2 The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be (0.49-0.51) x V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.

NOTE 3 Peak to peak ac noise on V_{REF} may not exceed +/-2% of $V_{REF(DC)}$.

NOTE 4 V_{TT} of transmitting device must track V_{REF} of receiving device.

2.2 Input parametric

Table 2a — Input dc logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IH(dc)}$	dc input logic high	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1
$V_{IL(dc)}$	dc input logic low	- 0.3	V_{REF} - 0.15	V	1

NOTE 1 Within this standard, it is the relationship of the V_{DDQ} of the driving device and the V_{REF} of the receiving device that determines noise margins. However, in the case of $V_{IH(Max.)}$ (i.e. input overdrive) it is the V_{DD} of the receiving device that is referenced. In the case where a device is implemented that supports SSTL_2 inputs but has no SSTL_2 outputs (e.g., a translator), and therefore no V_{DDQ} supply voltage connection, inputs must tolerate input overdrive to 3.0 V (High corner V_{DDQ} + 300 mV).

2 Supply voltage and logic input levels (cont'd)

2.2 Input parametric (cont'd)

Table 2b — Input ac logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IH(ac)}$	ac input logic high	V_{REF} + 0.31		V	
$V_{IL(ac)}$	ac input logic low		V_{REF} - 0.31	V	

2.3 AC test conditions

The ac input test conditions are specified to be able to obtain reliable, reproducible test results in an automated test environment, where a relatively high noise environment makes it difficult to create clean signals with limited swing. The tester may therefore supply signals with a 1.5 V peak to peak swing to drive the receiving device. Note however, that all timing specifications are still set relative to the ac input level. This is illustrated in figure 2.

Table 3 — AC input test conditions

Symbol	Condition	Value	Units	Notes
V_{REF}	Input reference voltage	0.5 x V_{DDQ}	V	1,4
$V_{SWINGmax}$	Input signal maximum peak to peak swing	1.5	V	1,2
SLEW	Input signal minimum slew rate	1.0	V/ns	3

NOTE 1 In all cases, input wave-form timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test. Table 1 identifies the V_{REF} range supported in SSTL_2.

NOTE 2 Compliant devices must still meet the $V_{IH(ac)}$ and $V_{IL(ac)}$ specifications under actual use conditions.

NOTE 3 The 1V/ns input signal minimum slew rate is to be maintained in the VILmax (ac) to VIHmin (ac) range of the input signal swing, consistent with the ac logic specification of table 2b. See also figure 2.

NOTE 4 AC test conditions may be measured under nominal voltage conditions as long as the supplier can demonstrate by analysis that the device will meet its timing specifications under all supported voltage conditions.

2 Supply voltage and logic input levels (cont'd)

2.3 AC test conditions (cont'd)

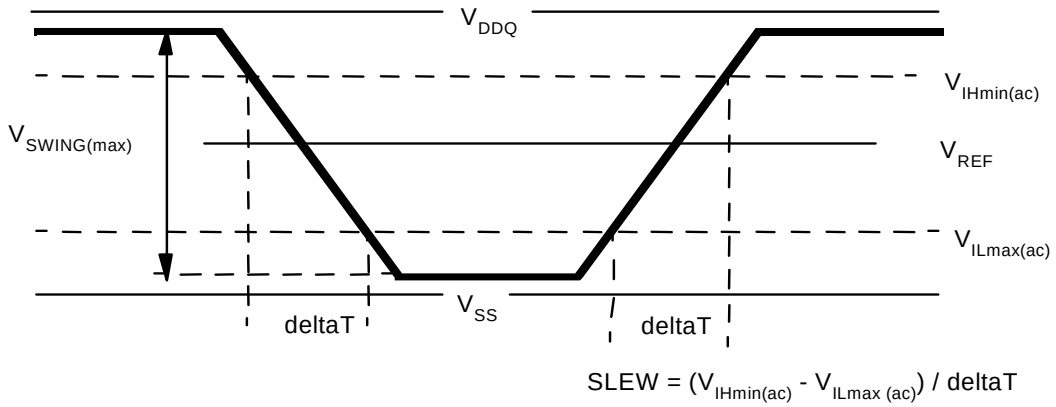

Figure 2 — AC input test signal wave form

3 SSTL_2 output buffers

3.1 Overview

This specification sets minimum requirements for output buffers in such a way that when they are applied within the range of power supply voltages specified in SSTL_2 and are used in conjunction with SSTL_2 input receivers then the input receiver specifications can be met or exceeded. The specifications are quite different from traditional specifications, where minimum values for V_{OH} and maximum values for V_{OL} are set that apply to the entire supply range. In SSTL_2, the input voltage provided to the receiver depends on the driver as well as on the termination voltage and termination resistors. Figure 3 shows the typical dc environment that the output buffer is presented with.

3 SSTL_2 output buffers (cont'd)

3.1 Overview (cont'd)

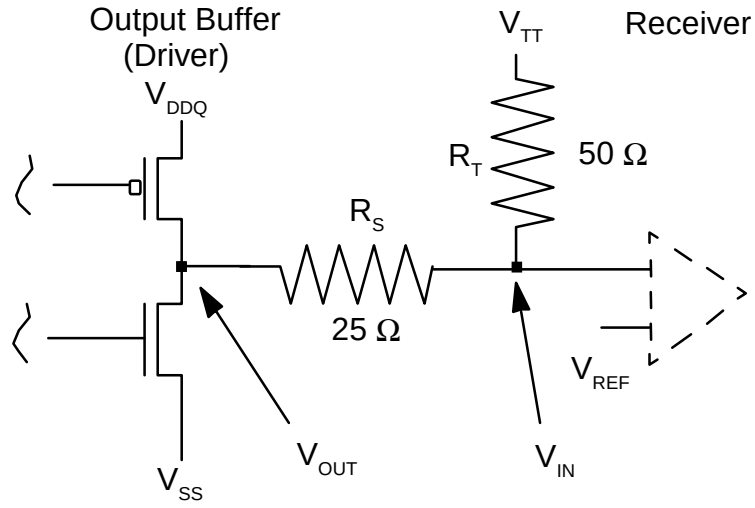

Figure 3 — Typical output buffer (driver) environment

Of particular interest here are the values V_{OUT} and V_{IN}. These values depend not only on the current drive capabilities of the buffer, but also on the values of V_{DDQ} and V_{TT} (V_{REF} is equal to V_{TT}). The important condition is that V_{IN} be at least 405 mV above or below V_{TT} as a result of V_{OUT} attaining its maximum low or it's minimum high value. As will be seen later, the two cases of interest for SSTL_2 are where the series resistor R_S equals 25 Ω and the termination resistor R_T equals 50 Ω (for Class I) or 25 Ω (for Class II). V_{TT} is specified as being equal to 0.5 x V_{DDQ}.

In order to meet the 405 mV minimum requirement for V_{IN}, a minimum of 8.1 mA must be developed across R_T if R_T equals 50 Ω (Class I) or 16.2 mA in case R_T equals 25 Ω (Class II). The driver specification now must guarantee that these values of V_{IN} are obtained in the worst case conditions specified by this standard.

3 SSTL_2 Output buffers (cont'd)

3.1 Overview (cont'd)

Table 4 — Spread sheet showing how the limits of SSTL_2 circuit voltages depending on V_{DDQ}. (For reference only)

Condition	**Units**	**Class I**	**Class I**	**Class I**	**Class II**	**Class II**	**Class II**	**Class II nominal**
V_{DDQ}	V	**2.3**	**2.5**	**2.7**	**2.3**	**2.5**	**2.7**	**2.5**
$V_{REF(MIN)} = V_{DDQ}$ * **0.49**	V	1.13	1.23	1.32	1.13	1.23	1.32	1.25
$V_{REF(MAX)} = V_{DDQ}$ * **0.51**	V	1.17	1.28	1.38	1.17	1.28	1.38	1.25
$V_{TT(MIN)} = V_{REF(MIN)}$ - **40 mV**	V	1.09	1.19	1.28	1.09	1.19	1.28	1.25
$V_{TT(MAX)} = V_{REF(MAX)}$ + **40 mV**	V	1.21	1.32	1.42	1.21	1.32	1.42	1.25
R_S	Ω	**25**	**25**	**25**	**25**	**25**	**25**	**25**
R_T	Ω	**50**	**50**	**50**	**25**	**25**	**25**	**25**
Output High Drive								
Minimum Output Current	mA	**-8.1**	**-8.1**	**-8.1**	**-16.2**	**-16.2**	**-16.2**	**-16.2**
$V_{TT\ (WC)} = V_{REF(MAX)}$ - **40 mV**	V	1.13	1.24	1.34	1.13	1.24	1.34	1.25
Minimum Voltage at V_{IN}	V	1.54	1.64	1.74	1.54	1.64	1.74	1.66
Minimum Voltage at V_{OUT}	V	1.74	1.84	1.94	1.94	2.05	2.15	2.06
Maximum On Resistance	Ω	69.1	81.2	93.3	22.0	28.1	34.1	27.2
$\Delta V_{IN(MIN)} = V_{IN} - V_{REF}$	mV	365	365	365	365	365	365	405
Output Low Drive								
Minimum Output Current	mA	**8.1**	**8.1**	**8.1**	**16.2**	**16.2**	**16.2**	**16.2**
$V_{TT\ (WC)} = V_{REF(MIN)}$ + **40 mV**	V	1.17	1.27	1.36	1.17	1.27	1.36	1.25
Maximum Voltage at V_{IN}	V	0.76	0.86	0.96	0.76	0.86	0.96	0.85
Maximum Voltage at V_{OUT}	V	0.56	0.66	0.76	0.36	0.46	0.55	0.44
Maximum On Resistance	Ω	69.1	81.2	93.3	22.0	28.1	34.1	27.2
$\Delta V_{IN(MIN)} = V_{IN} - V_{REF}$	mV	-365	-365	-365	-365	-365	-365	-405

NOTE 1 Bold numbers resemble the (exact) system assumptions; the other numbers are calculated exactly and then rounded.

NOTE 2 Table 4 does not take into account 2% $V_{REF\ (AC)}$ noise (+/- 25 mV nominal) which will further reduce the effective $\Delta V_{IN(MIN)}$ at the receiver.

3 SSTL_2 Output buffers (cont'd)

3.1 Overview (cont'd)

NOTE 3 From an analysis of figure 3 with fixed driver current for output low voltage, $V_{IN}=V_{TT}$ - I x R_T; $V_{OUT}=V_{TT}$ - I x (R_T+R_S); On Resistance = V_{TT} / I - (R_T+R_S).

NOTE 4 The most stringent requirements will result where V_{DDQ} = 2.3 V, since for that case the output driver transistors must have the lowest "on" resistance. If the driver outputs are sized for this condition, then for all other V_{DDQ} voltage applications, the resulting input signal will be larger than the minimum 365 mV.

NOTE 5 The worst case (WC) assumption for V_{TT} (e.g. $V_{TT(WC)}$ = V_{REF} + 40 mV for driving low) results from the fact that for V_{TT} = $V_{TT(MIN)}$ the input at the receiver is already biased towards the low state and less current will be required to develop 345 mV ΔV_{IN}. If the driver maintains a resistance lower than the Maximum On Resistance, more than the 345 mV will be presented to the receiver.

3.2 SSTL_2 Class I output buffers

3.2.1 Push-pull output buffer for symmetrically single parallel terminated loads with series resistor. (V_{TT} = 0.5 x V_{DDQ})

Table 5a — Output dc current drives

Symbol	Parameter	Min.	Max.	Units	Notes
$I_{OH(dc)}$	Output minimum source dc current	-8.1		mA	1,3,4
$I_{OL(dc)}$	Output minimum sink dc current	8.1		mA	2,3,4

NOTE 1 V_{DDQ} = 2.3 V; V_{OUT} = 1.74 V; V_{TT} = 1.13 V.

NOTE 2 V_{DDQ} = 2.3 V; V_{OUT} = 0.56 V; V_{TT} = 1.17 V

NOTE 3 The dc value of V_{REF} applied to the receiving device is expected to be set to V_{TT}.

NOTE 4 The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions 1, 2. They are used to test device current drive capability which ultimately delivers acceptable noise margin for an SSTL_2 receiver. Under these conditions V_{OH} is 1.74 V and V_{OL} is 0.56 V. Under other conditions for V_{DDQ} and V_{TT} the typical output levels are discussed in 3.1.

3.2 SSTL_2 Class I output buffers (cont'd)

3.2.1 Push-pull output buffer for symmetrically single parallel terminated loads with series resistor. (V_{TT} = 0.5 x V_{DDQ}) (cont'd)

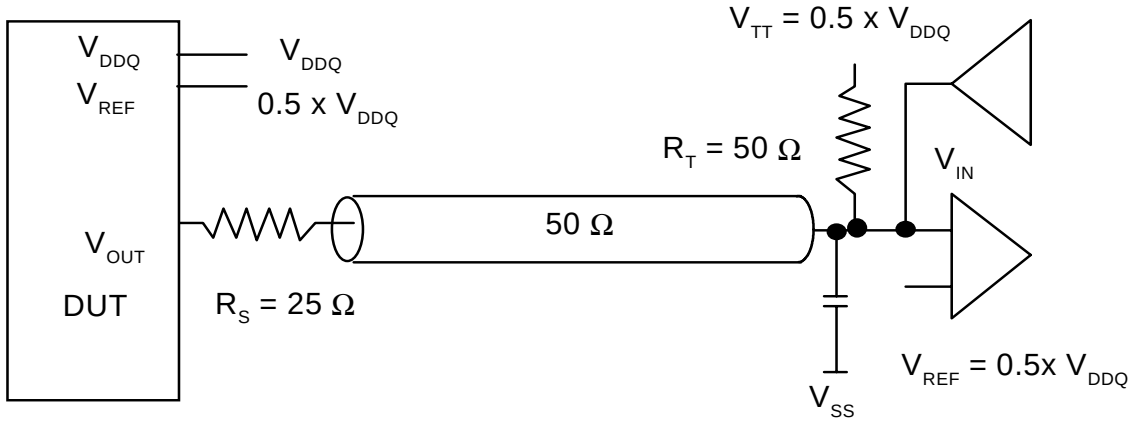

Figure 4 — Example of SSTL_2, Class I, symmetrically single parallel terminated output load, and series resistor

3.2.2 SSTL_2 Class I output ac test conditions

This testing regimen is used to verify SSTL_2 Class I type output buffers (push-pull output buffers designed for symmetrically single parallel terminated loads with series resistor).

This clause is added to set the conditions under which the driver ac specifications can be tested. The test circuit is assumed to be similar to the circuit shown in figure 4. AC test conditions may be measured under nominal voltage conditions as long as the supplier can demonstrate by analysis, that the device will meet its timing specifications under all supported voltage conditions. Table 5a assumes that +/- 405 mV must be developed across the 50 Ω termination resistor at V_{IN}. With a series resistor of 25 Ω this translates into a minimum requirement of 608 mV swing relative to V_{TT} , at the output of the device.

Table 5b — AC test conditions

Symbol	Condition	Value	Units	Notes
V_{OH}	Minimum required output pull-up under ac test load	V_{TT} + 0.608	V	
VOL	Maximum required output pull-down under ac test load	V_{TT} - 0.608	V	
V_{OTR}	Output timing measurement reference level	0.5 x V_{DDQ}	V	1

NOTE 1 The V_{DDQ} of the device under test is referenced.

3.3 SSTL_2 Class II output buffers

3.3.1 Push-pull output buffer for symmetrically double parallel terminated loads with series resistor (V_{TT} = 0.5 x V_{DDQ})

Table 6 — Output dc current drive

Symbol	Parameter	Min.	Max.	Units	Notes
$I_{OH(dc)}$	Output minimum source dc current	-16.2		mA	1,3,4
$I_{OL(dc)}$	Output minimum sink dc current	16.2		mA	2,3,4

NOTE 1 V_{DDQ} = 2.3 V; V_{OUT} = 1.94 V; V_{TT} = 1.13 V.

NOTE 2 V_{DDQ} = 2.3 V; V_{OUT} = 0.36 V; V_{TT} = 1.17 V.

NOTE 3 The dc value of V_{REF} applied to the receiving device is expected to be set to V_{TT}

NOTE 4 The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions 1, 2. They are used to test device current drive capability which ultimately delivers acceptable noise margin for an SSTL_2 receiver. Under these conditions V_{OH} is 1.94 V and VOL is 0.37 V. Under other conditions for V_{DDQ} and V_{TT} the typical output levels are discussed in 3.1.

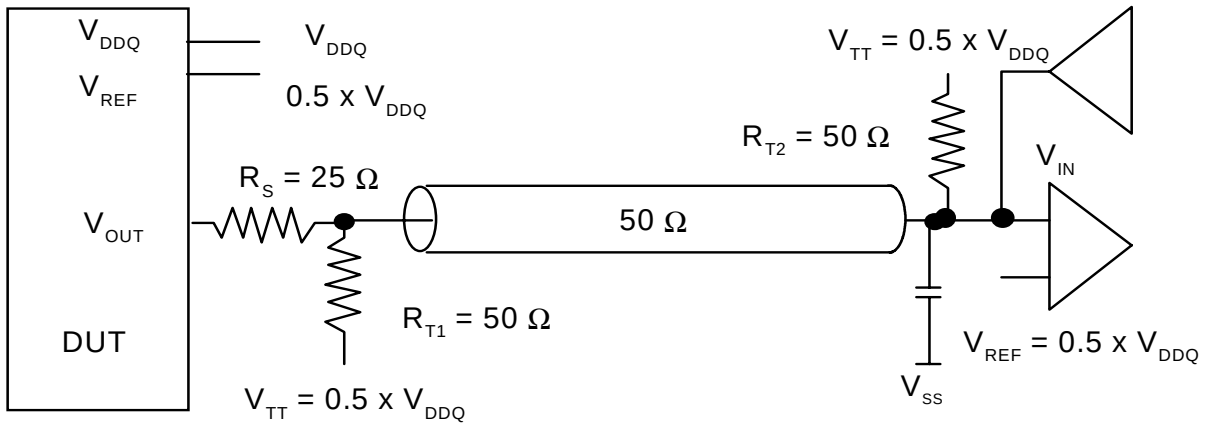

Figure 5 — Example of SSTL_2, Class II, symmetrically double parallel terminated output load with series resistor

3.3 SSTL_2 Class II output buffers (cont'd)

3.3.2 SSTL_2 Class II output ac test conditions

This testing regimen is used to verify SSTL_2 Class II type output buffers (push-pull output buffers designed for symmetrically double parallel terminated loads with series resistor).

This clause is added to set the conditions under which the driver ac specifications can be tested. The test circuit is assumed to be similar to the circuit shown in figure 5. AC test conditions may be measured under nominal voltage conditions as long as the supplier can demonstrate by analysis, that the device will meet its timing specifications under all supported voltage conditions. Table 7 assumes that +/- 405 mV must be developed across the effectively 25 Ω termination resistor at V_{IN} . With a series resistor of 25 Ω this translates into a minimum requirement of 810 mV swing relative to V_{TT}, at the output of the device.

Table 7 — AC test conditions

Symbol	Condition	Value	Units	Notes
V_{OH}	Minimum required output pull-up under ac test load	V_{TT} + 0.81	V	
V_{OL}	Maximum required output pull-down under ac test load	V_{TT} - 0.81	V	
V_{OTR}	Output timing measurement reference level	0.5 x V_{DDQ}	V	1

NOTE 1 The V_{DDQ} of the device under test is referenced.

4 Other application (for reference only)

The specifications for Class I and II were based on an environment comprising both series and parallel terminating resistors. In this non binding section we will show some derived applications. Clearly it is not the intention to show all possible variations in this standard.

4.1 Push-pull output buffer for unterminated loads

In many applications where interconnections are short, there is no need for any termination at all. An example of this is shown in figure 6. This application can be served by a Class I or Class II type buffer and an SSTL_2 type receiver

4 Other application (for reference only) (cont'd)

4.1 Push-pull output buffer for unterminated loads (cont'd)

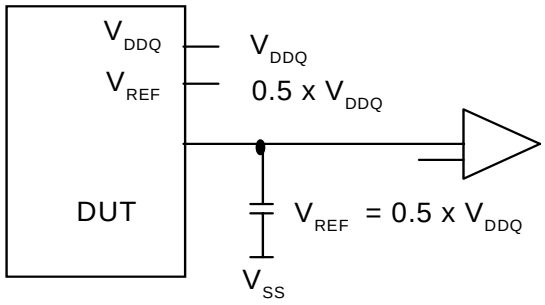

Figure 6 — Example of SSTL_2 unterminated output load

4.2 Push-pull output buffer for symmetrically single parallel terminated loads (V_{TT} = 0.5 x V_{DDQ})

Sometimes the system application requires longer transmission lines that will only be terminated at one end. An example of this may be address drivers on a memory board. This application can also be served with a Class I or Class II type buffer and an SSTL_2 receiver. An example is shown in figure 7.

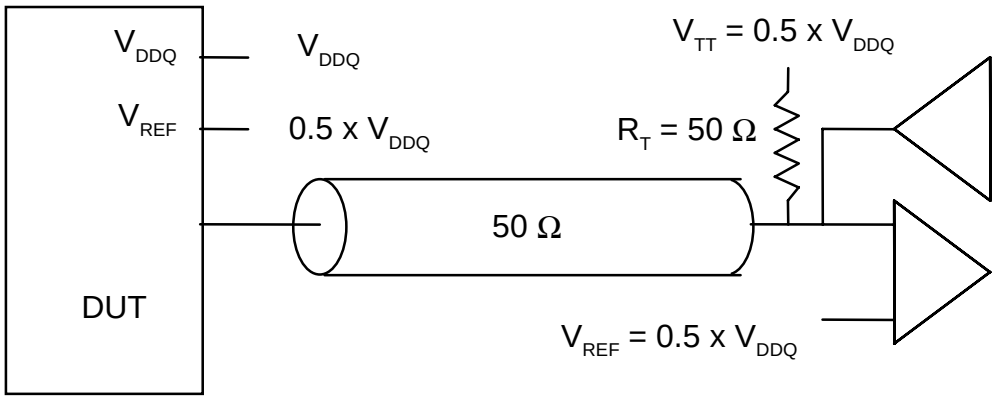

Figure 7 — Example of SSTL_2, Class I or Class II, buffer with symmetrically single parallel terminated output loads.

4 Other application (For reference only) (cont'd)

4.3 Push-pull output buffer for externally source series terminated loads

In other applications the system designer may wish to terminate at the signal source rather than at the end of the transmission line. One advantage of this approach is that there is no need for a V_{TT} power supply. This application may again be served with a Class I or Class II type buffer and SSTL_2 receiver. An example is shown in figure 8. In this example a Class II type buffer might be preferred since it comes closer, in conjunction with the series resistor, to match the characteristic impedance of the transmission line.

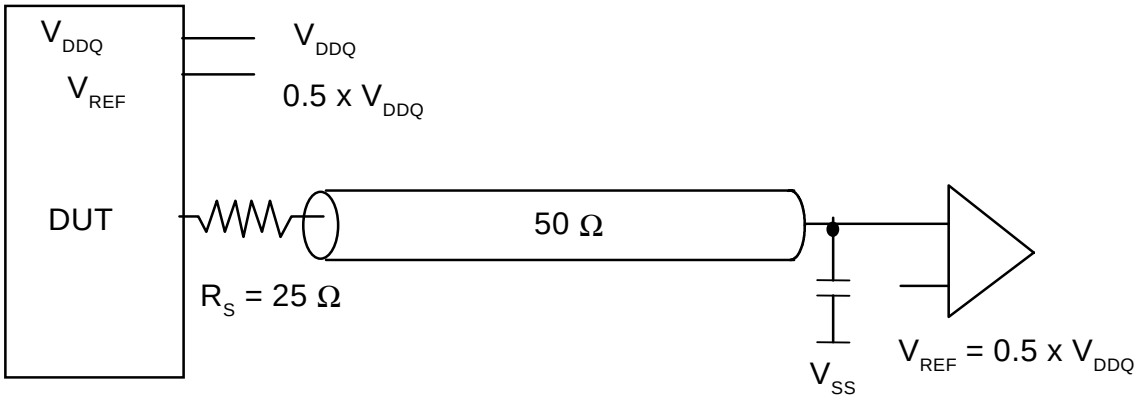

Figure 8 — Example of SSTL_2, Class I or Class II, Externally Source Series terminated output load

4.4 Push-pull output buffer for symmetrically double parallel terminated loads (V_{TT} = 0.5 x V_{DDQ})

Finally, the system designer may require a bus system which must be terminated at both sides. However, the drivers are connected directly onto the bus so there are no stubs present. In that case, the designer may decide to eliminate the series resistors entirely. This application can be implemented using a Class I or Class II driver and SSTL_2 receiver. However a Class II buffer would dissipate more power due to its larger current drive and thus might require special cooling.

4 Other application (Reference only) (cont'd)

4.4 Push-pull output buffer for symmetrically double parallel terminated loads (V_{TT} = 0.5 x V_{DDQ}) (cont'd)

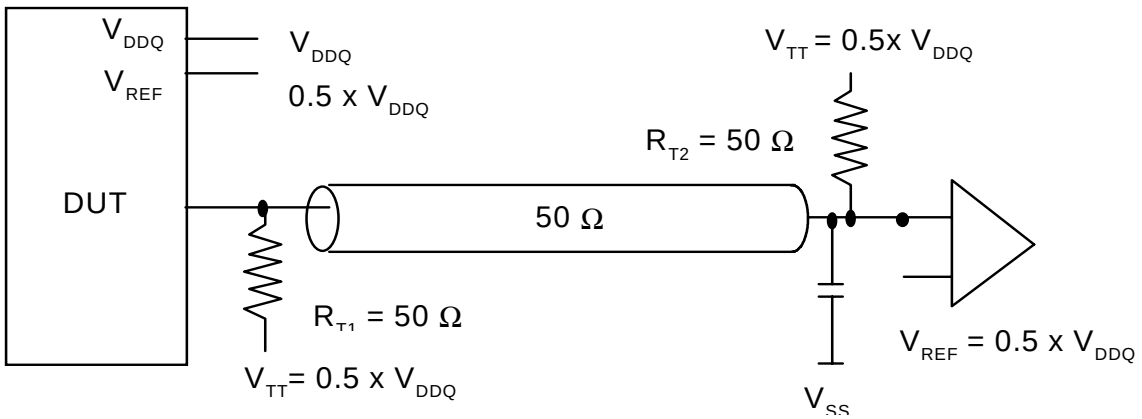

Figure 9 — Example of SSTL_2, Class I, buffer with symmetrically double parallel terminated output load

5 Differential signals

5.1 Overview

The following specifications were added to JESD8-9 as a result of the desire to accommodate differential signals in SSTL_2 based systems. This is particularly relevant to DDR DRAM clock signals, but the specification is intended to cover all differential signals in the SSTL_2 category.

5.2 Differential input parameters

Table 8a — Differential input dc logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{IN(dc)}$	DC input signal voltage	-0.30	V_{DDQ} + 0.30	V	1
$V_{Swing(dc)}$	DC differential input voltage	0.30	V_{DDQ} + 0.6	V	2

NOTE 1 $V_{IN(dc)}$ specifies the allowable dc excursion of each differential input.

NOTE 2 VSwing(dc) specifies the input differential voltage $|V_{TR}-V_{CP}|$ required for switching, where V_{TR} is the "true" input level and V_{CP} is the "complementary" input level.

5 Differential signals (cont'd)

5.2 Differential input parameters (cont'd)

Table 8b — Differential input ac logic levels

Symbol	Parameter	Min.	Max.	Units	Notes
$V_{Swing(ac)}$	AC differential input voltage	0.62	V_{DDQ} + 0.6	V	1
$V_{x(ac)}$	AC differential cross point voltage	0.5 x V_{DDQ} -200 mV	0.5 x V_{DDQ} +200 mV	V	2

NOTE 1 $V_{Swing(ac)}$ specifies the input differential voltage $|V_{TR}-V_{CP}|$ required for switching, where V_{TR} is the "true" input signal and V_{CP} is the "complementary" input signal.

NOTE 2 The typical value of $V_{x(ac)}$ is expected to be about 0.5 x V_{DDQ} of the transmitting device and $V_{x(ac)}$ is expected to track variations in V_{DDQ}. $V_{x(ac)}$ indicates the voltage at which differential input signals must be crossing.

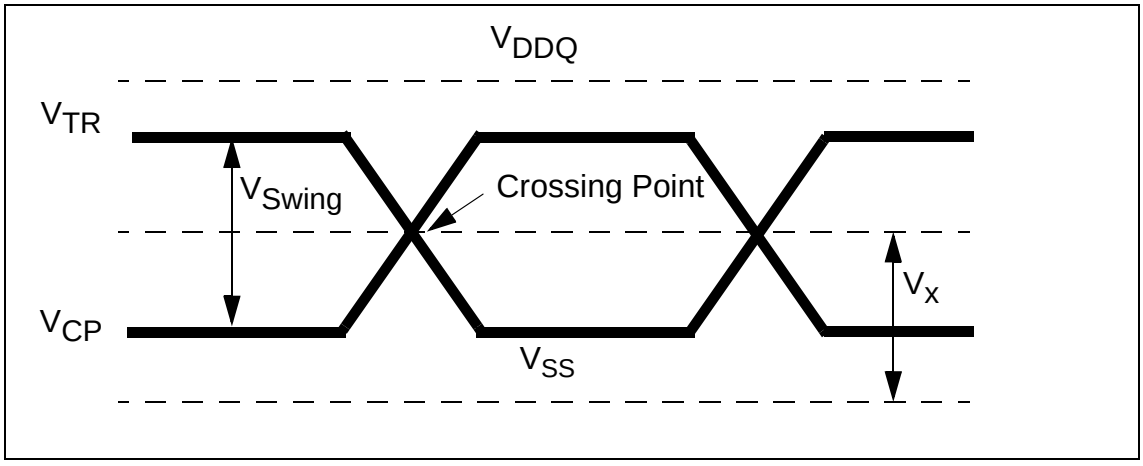

Figure 10 — SSTL_2 differential input levels

5.3 AC test conditions

The differential ac test condition are specified to be able to obtain reliable, reproducible test results in an automated test environment, where a relatively high noise enviroment makes it difficult to create clean signals with limited swing. The tester may therefore supply signals with a 1.5 V peak-to-peak swing to drive the receiving device. Note however, that all timing specifications are still set relative to the differential ac input level. This is illustrated in figure 2.

5 Differential signals (cont'd)

5.3 AC test conditions (cont'd)

Table 9 — Differential input ac test conditions

Symbol	Parameter	Min.	Max.	Units	Notes
V_r	Input timing measurement reference level	Vx (cross point)		V	1
V_{Swing}	Input signal peak to peak swing voltage	-------	1.5	V	2
SLEW	Input signal slew rate	1.0	------	V/ns	3
t_{CKD}	Clock duty cycle	45	55	%	4

NOTE 1 In all cases, input waveform timing is referenced to two input signals (V_{TR} and V_{CP}) crossing point level (Vx) applied to the device under test, where V_{TR} is "true" input signal and V_{CP} is the "complementary" input signal. Table 8b identifies the $V_{x(ac)}$ range supported in SSTL_2 differential input.

NOTE 2 A 1.5 V input pulse level is specified to allow consistent, repeatable test results in an automatic test equipment (ATE) enviroment. Compliant devices must meet the $V_{Swing(ac)}$ specification under actual use conditions. See table 8b.

NOTE 3 The 1 V/ns input signal minimum slew rate is to be maintained the $V_{ILmax(ac)}$ to $V_{IHmin(ac)}$ range of the input signal swing, consistent with table 2b and figure 2.

NOTE 4 For periodic clock inputs, the duty cycle(t_{CKD}) is defined to the t_{CH} (or t_{CL}) divided by t_{CK} time when "true" input signal and "complementary" input signal are crossing each other. See figure 11. This can be expressed by equation-1 or equation-2.

$$t_{CKD} = t_{CH} / t_{CK} \quad (1)$$

$$t_{CKD} = t_{CL} / t_{CK} \quad (2)$$

5 Differential signals (cont'd)

5.3 AC test conditions (cont'd)

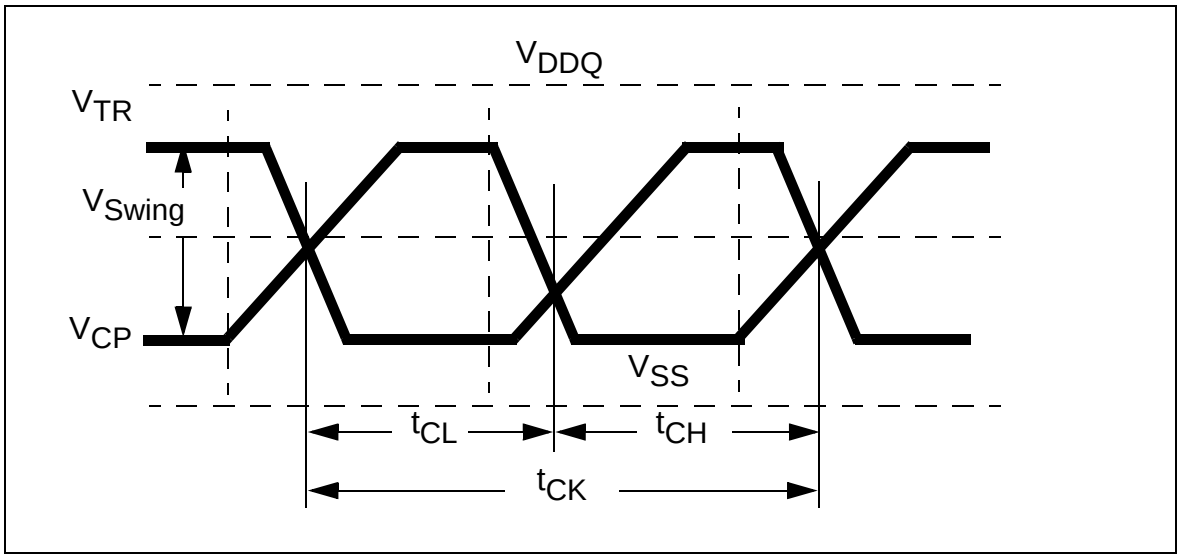

Figure 11 — Differential ac input test signal wave form

5.4 Example of SSTL_2 Class I differential signals

For reference only example, figure 12 show the differential clocks are independently terminated by a 50 Ω resistor. The value of $I_{OH(dc)}$ and $I_{OL(dc)}$ has to be abide by Class I specification.

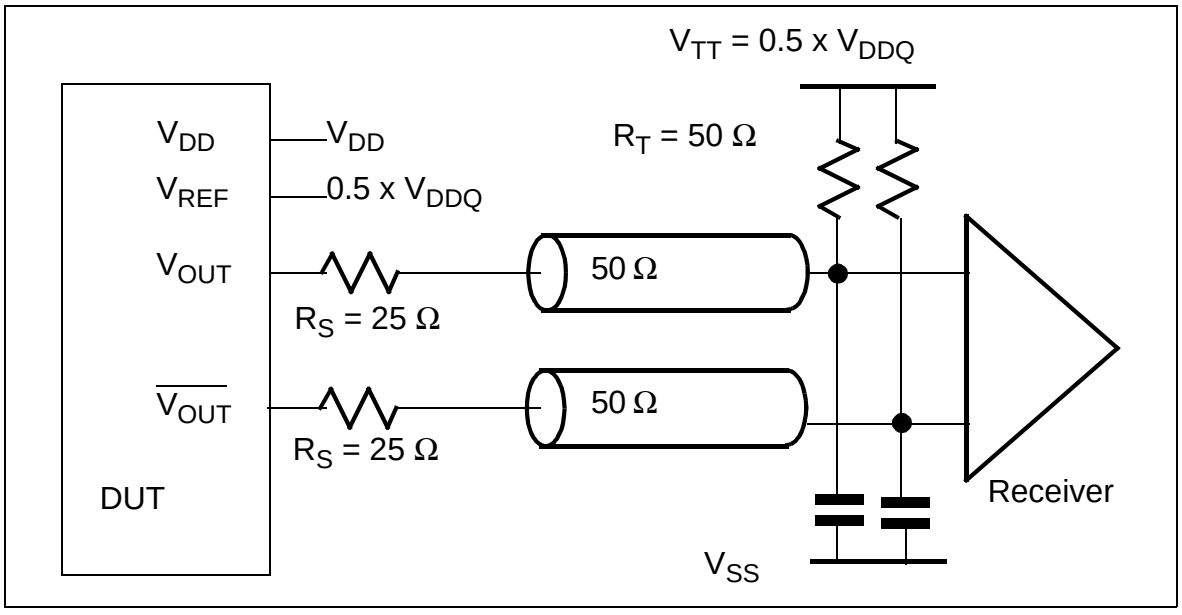

Figure 12 — Example of SSTL_2 class I, differential signal using single load, and series resistor.

5 Differential signals (cont'd)

5.4.1 Example of SSTL_2 Class I differential clock signals (Reference only)

For reference only example, figure 13a shows the differential clocks are directly terminated by a 100 Ω resistor. The value of $I_{OH(dc)}$, $I_{OL(dc)}$ and table 2 parameters has to be abide by Class I specification.

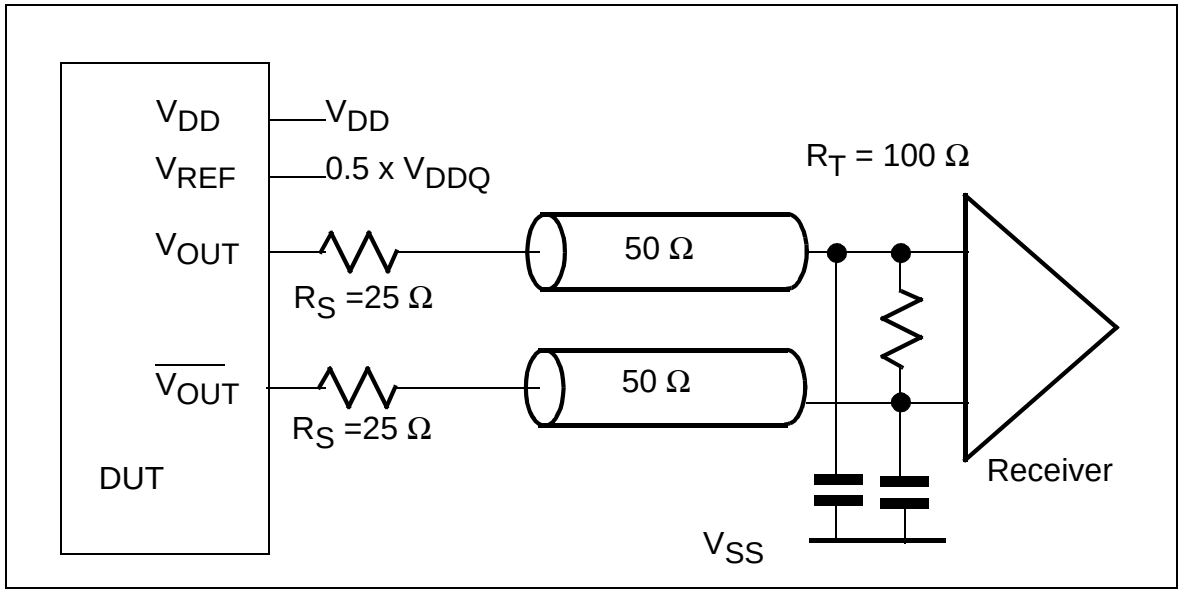

Figure 13a — Example of SSTL_2 Class I differential signal using direct termination resister, and series resistor. (Reference only)

Table 10 — V_{iso} specifications (Reference only)

Symbol	Parameter	Min.	Max.	Units	Notes
V_{iso}	Input clock signal offset voltage	0.5 x V_{DDQ}		V	1
ΔV_{iso}	Viso variation	------	+200	mV	1

NOTE 1 For reference only, the value of Viso is expected to be $(|V_{TR}+V_{CP}|)/2$ in case of each clock directly terminated by a 100 Ω resistor, where V_{TR} is the "true" input signal voltage and VCP is the "complementary" input signal voltage respectively. See figure 13b.

5 Differential signals (cont'd)

5.4.1 Example of SSTL_2 Class I differential clock signals (Reference only) (cont'd)

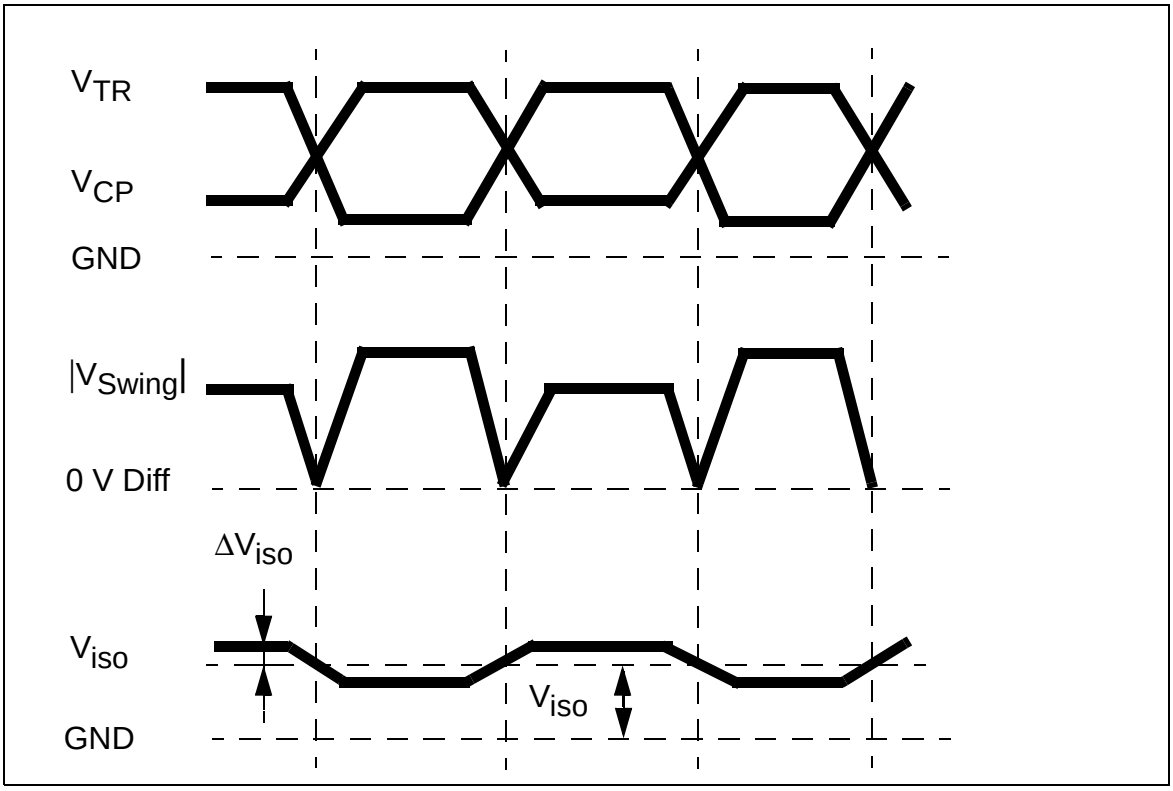

Figure 13b — Input clock signal offset voltage (Reference only)


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