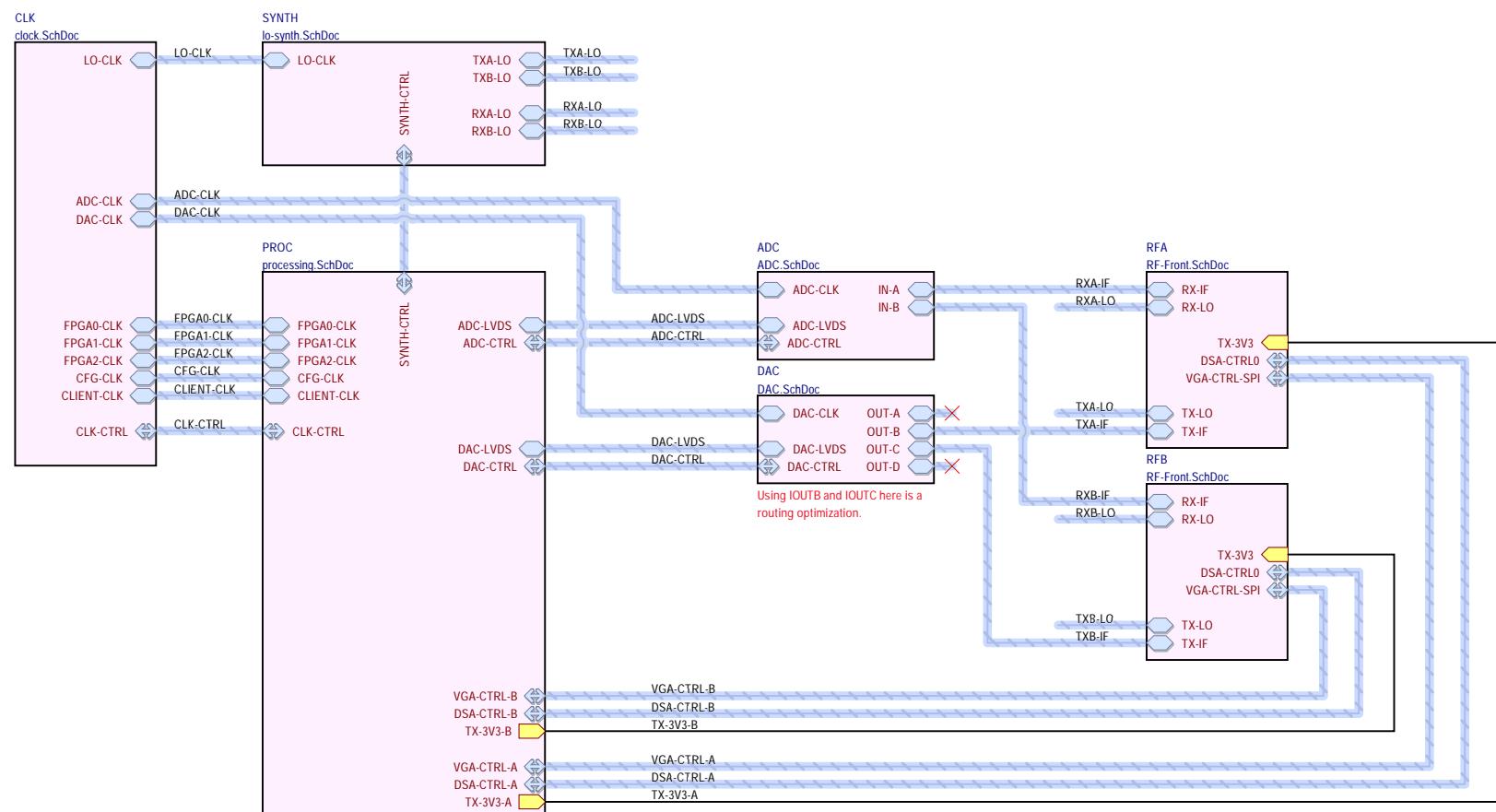


A



B

A

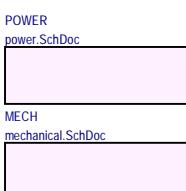
B

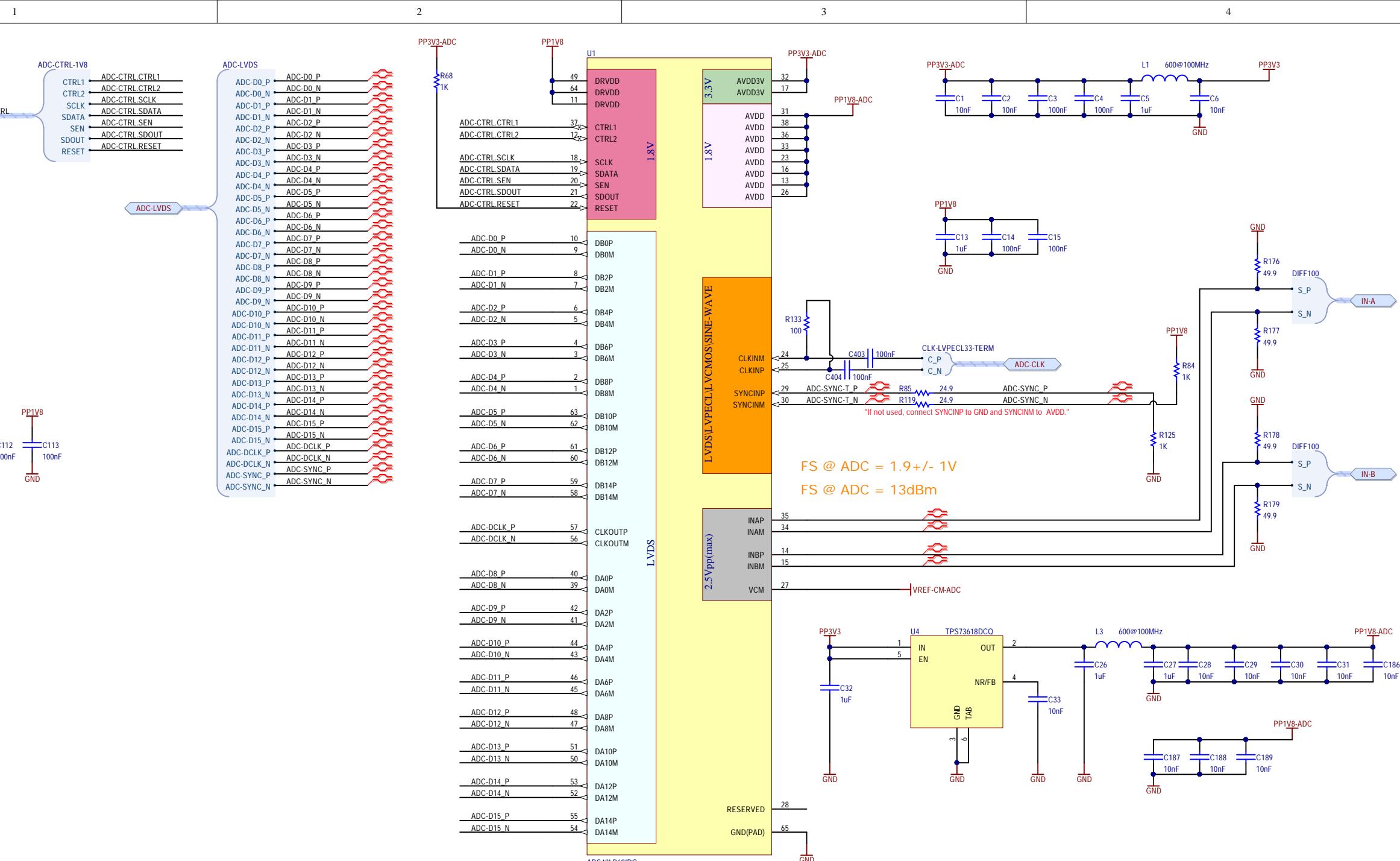
C

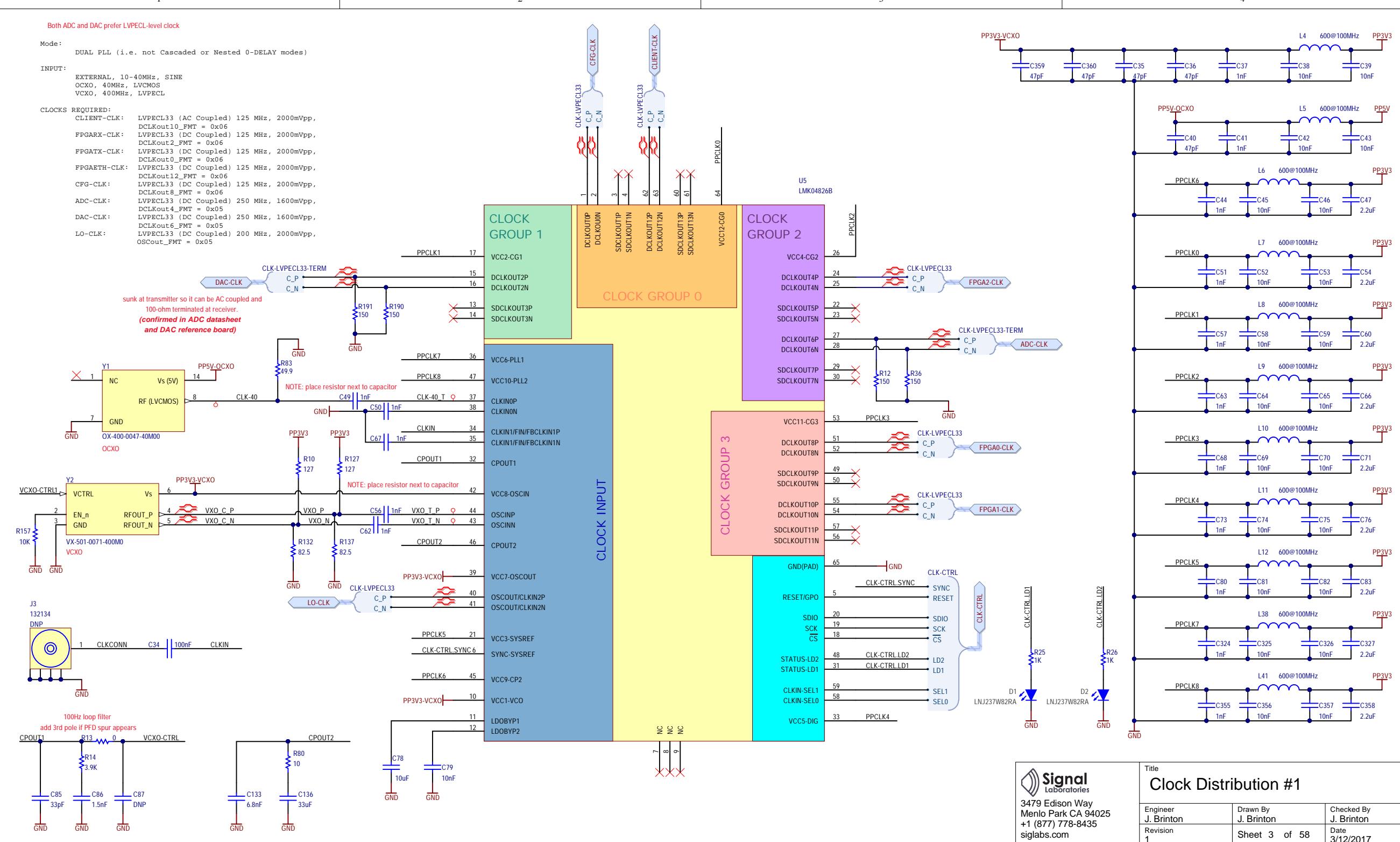
C

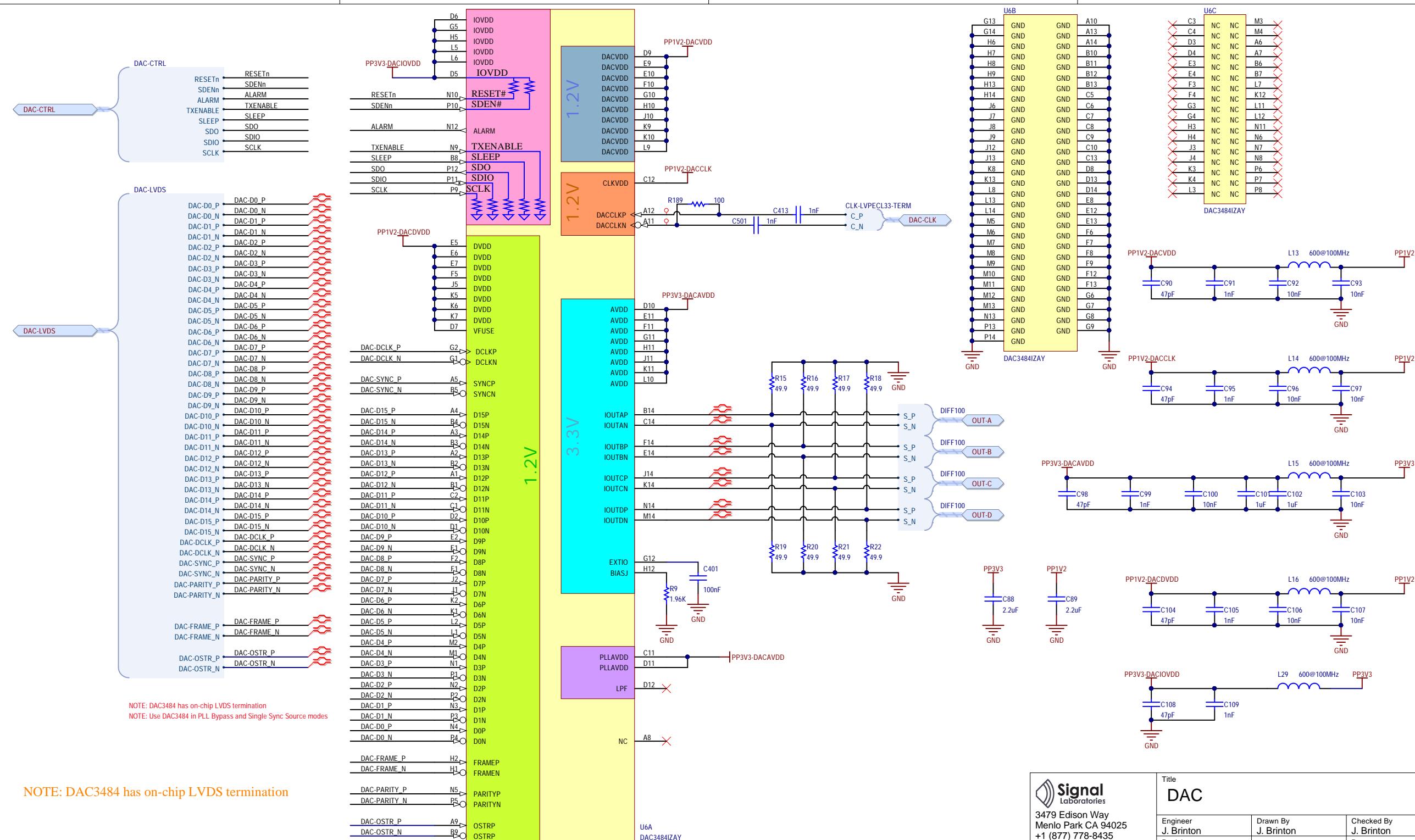
D

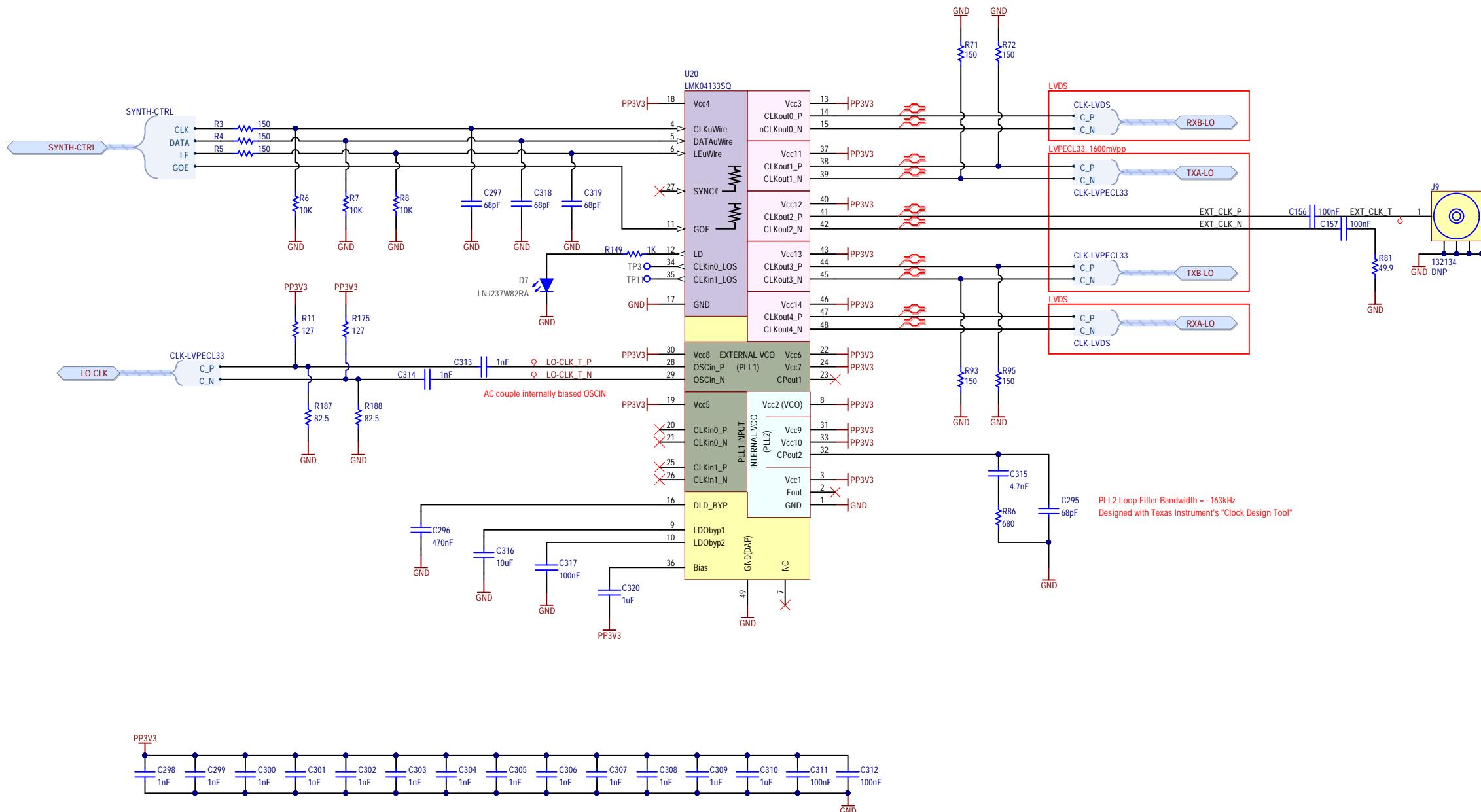
D



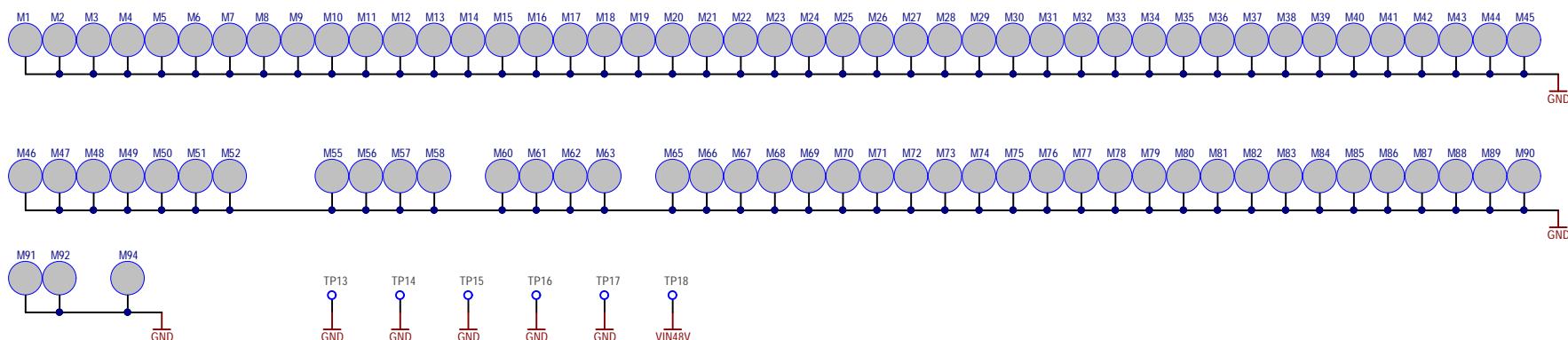








A



B

C

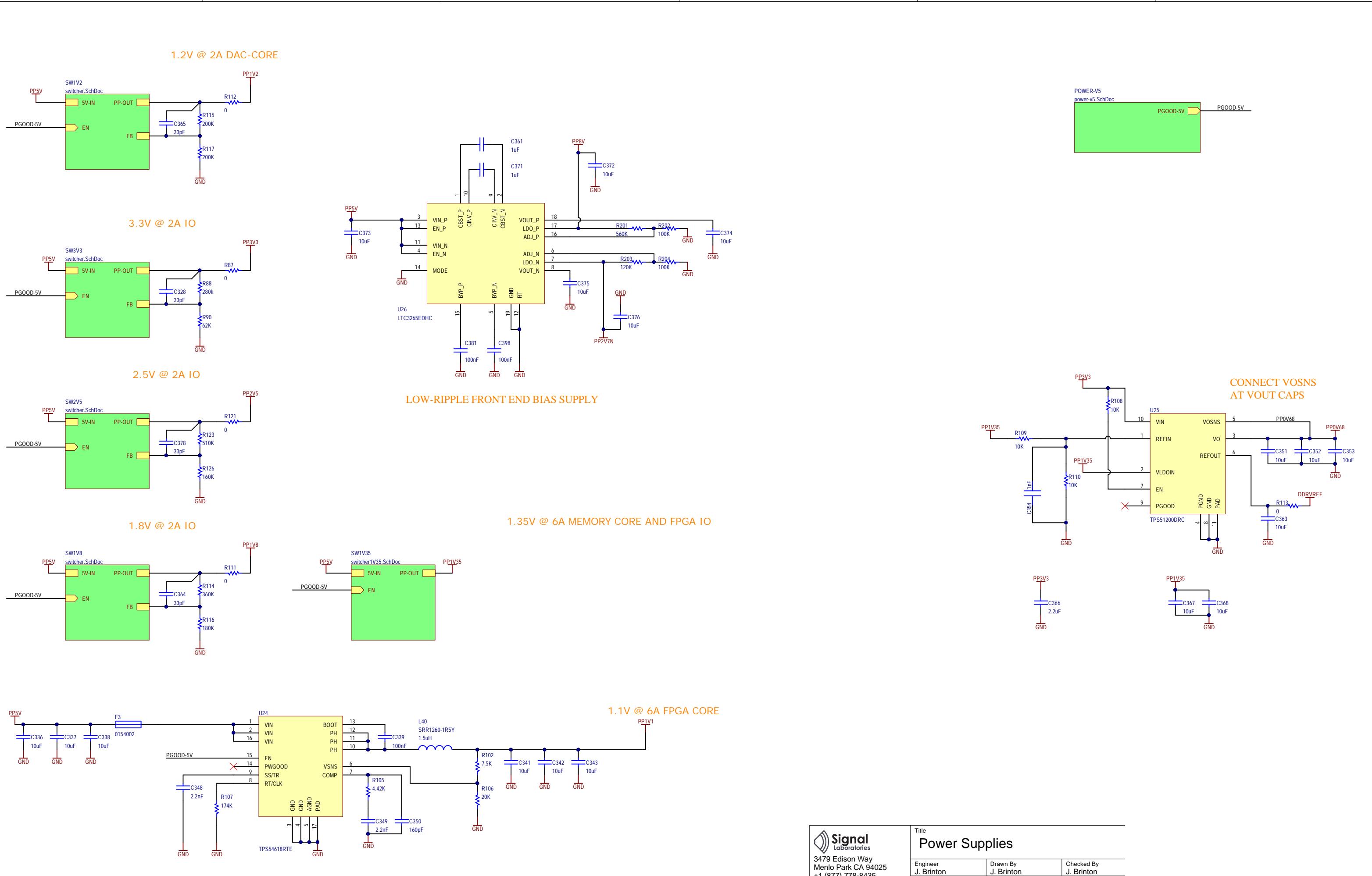
D

A

B

C

D



A

A

B

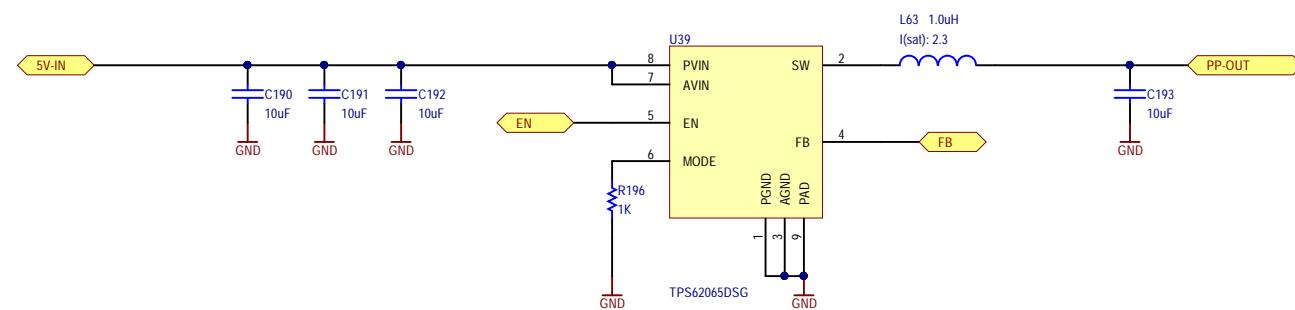
B

C

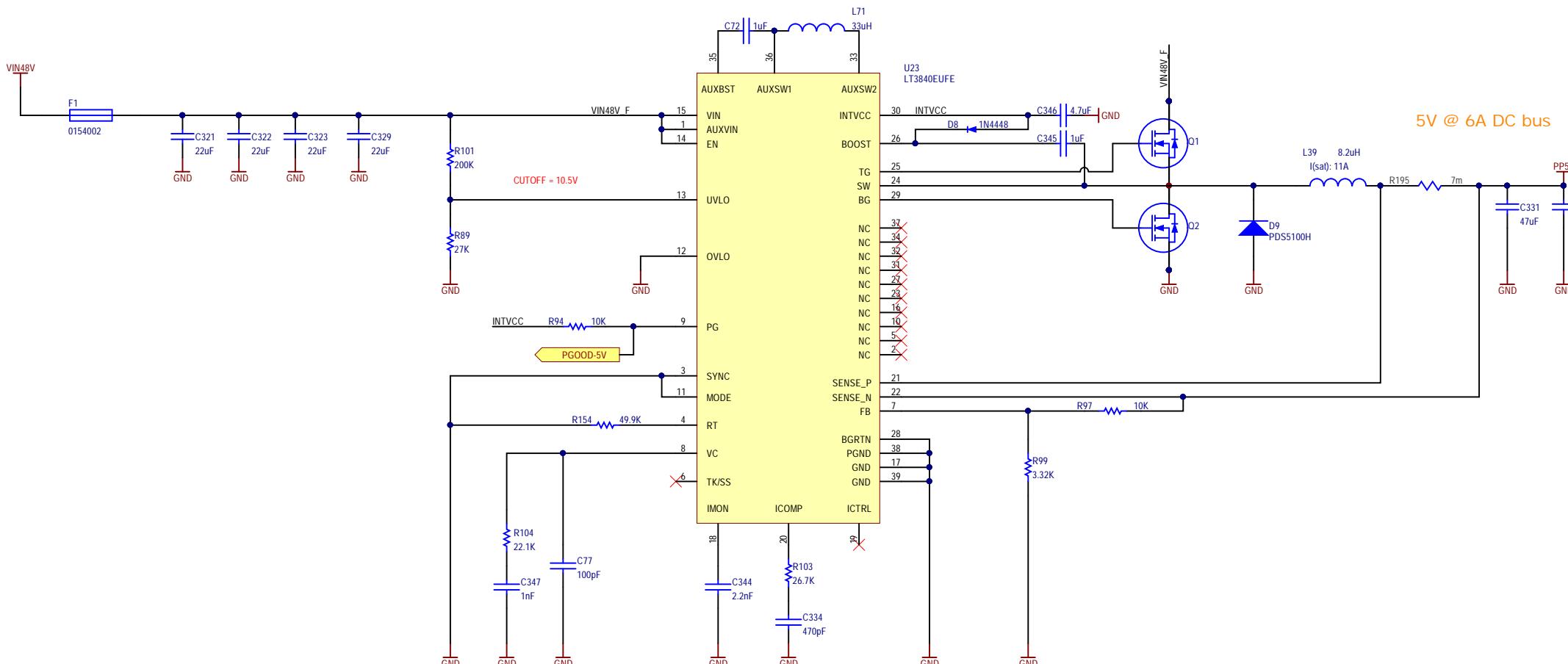
C

D

D



A



B

C

D

A

B

C

D

A

A

B

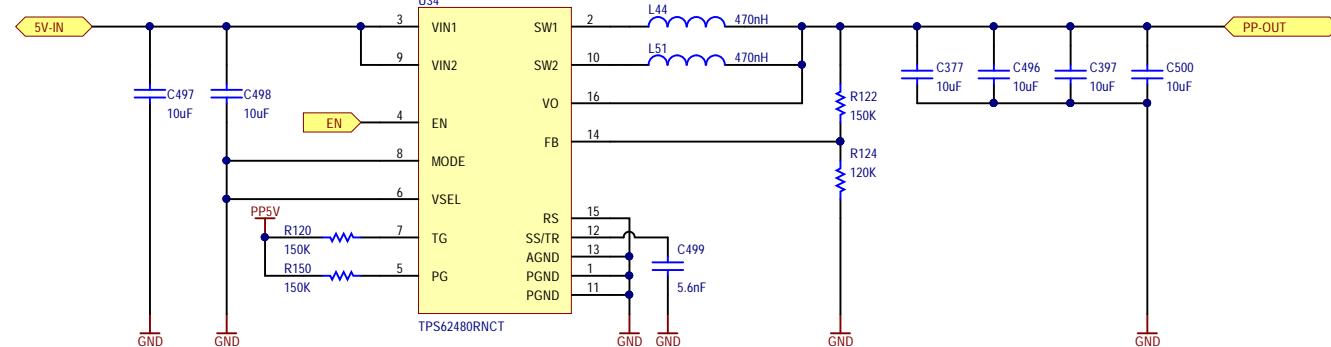
B

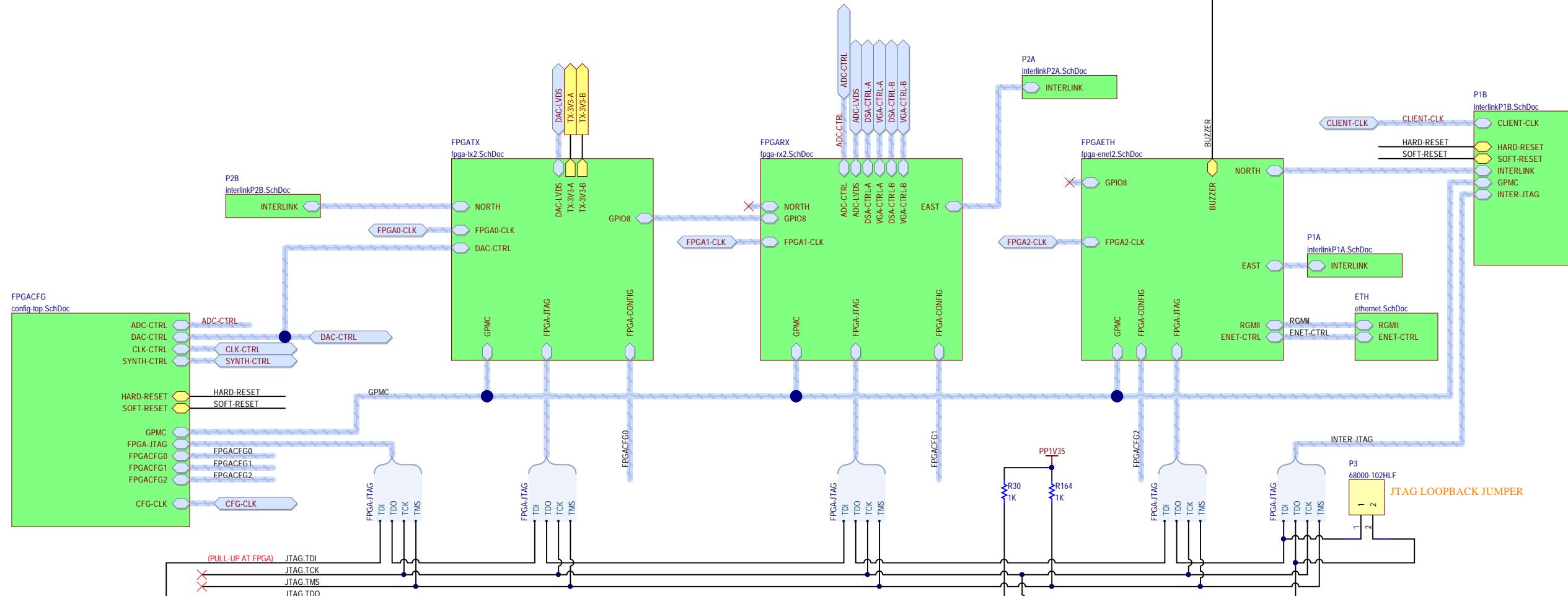
C

C

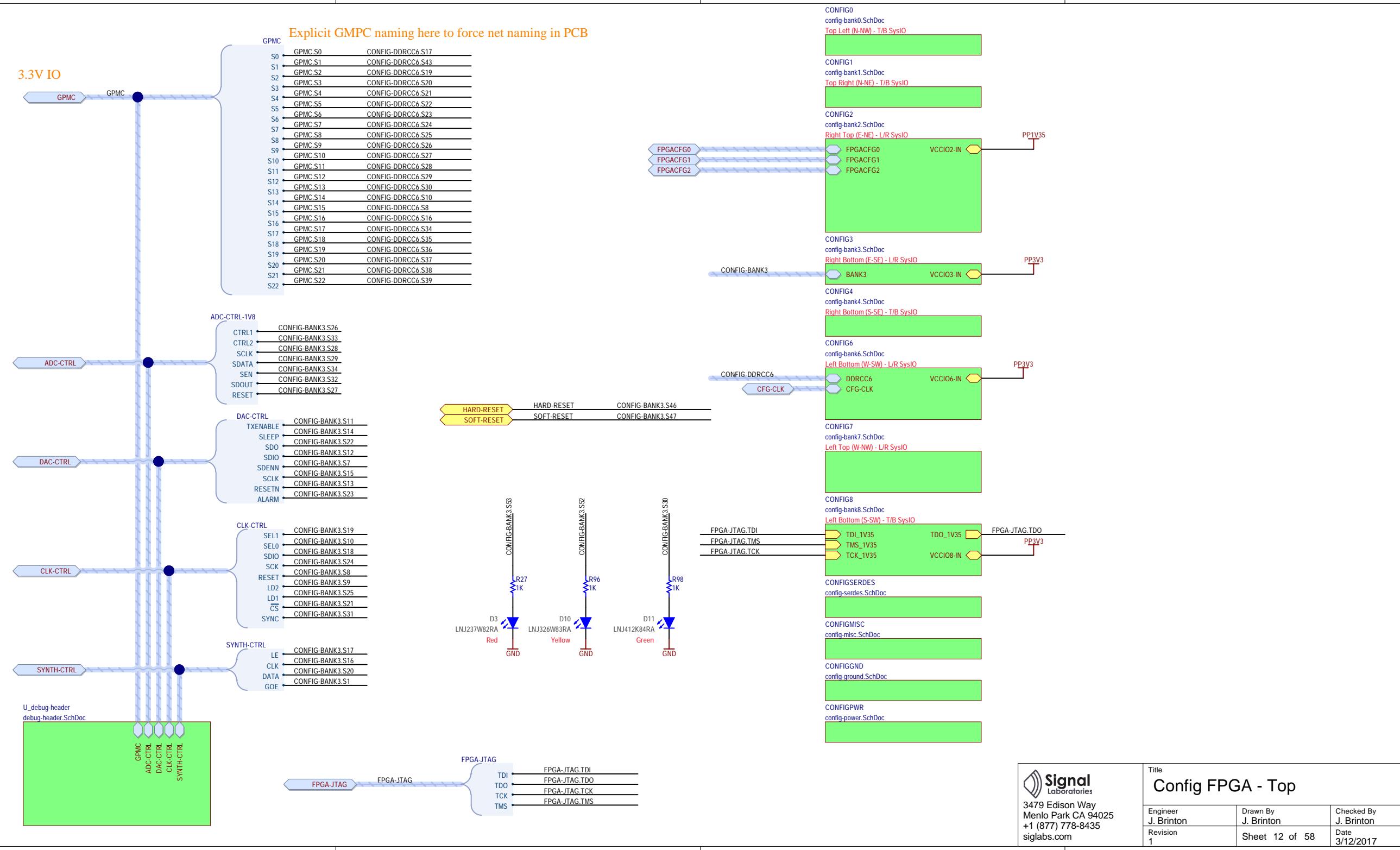
D

D





CONFIGURATION IS SLAVE SERIAL MODE (SCM)
EITHER CONFIG FPGA AS MASTER-OF-ALL
OR DAISY CHAIN SCM THRU CONFIG FPGA TO FLASH MEMORY
SEE ECP5 sysCONFIG DOCUMENTATION



A

B

C

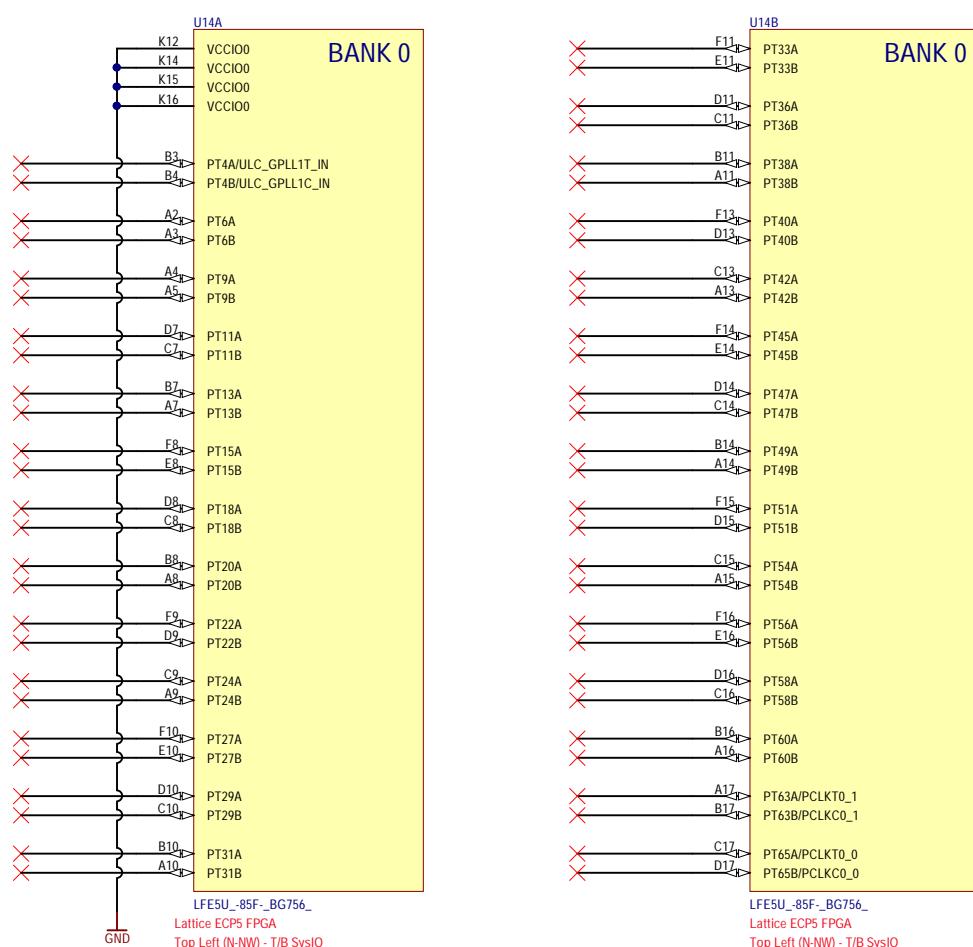
D

A

B

C

D



A

B

C

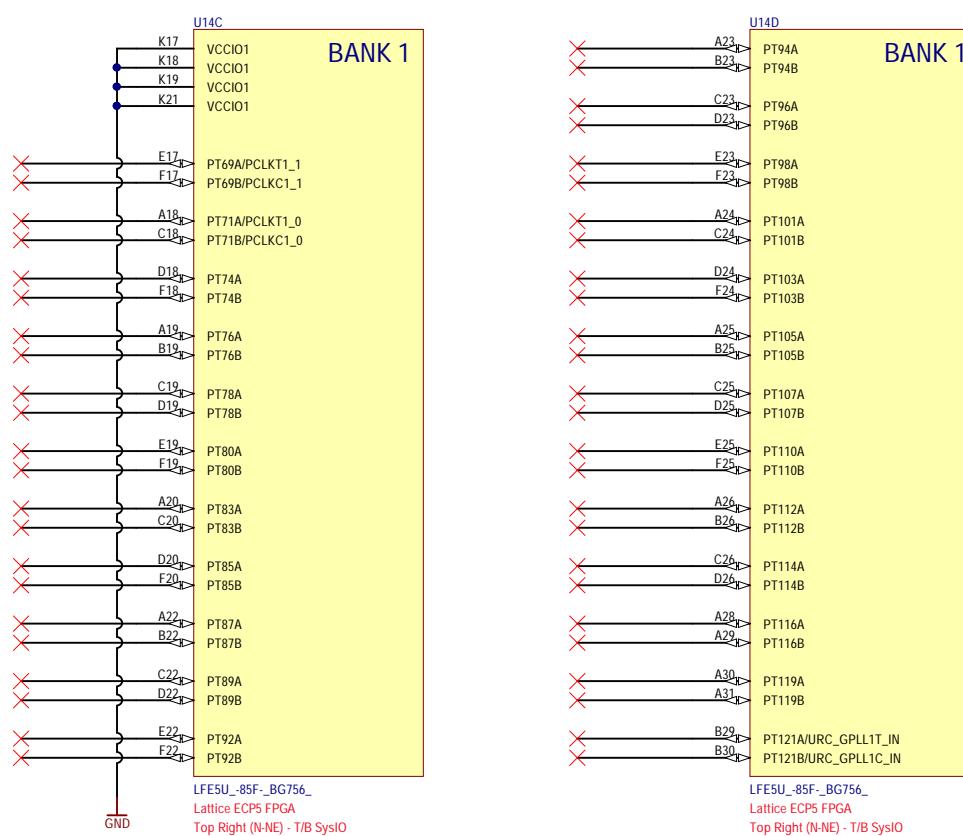
D

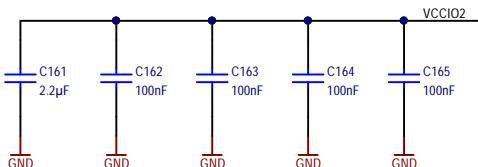
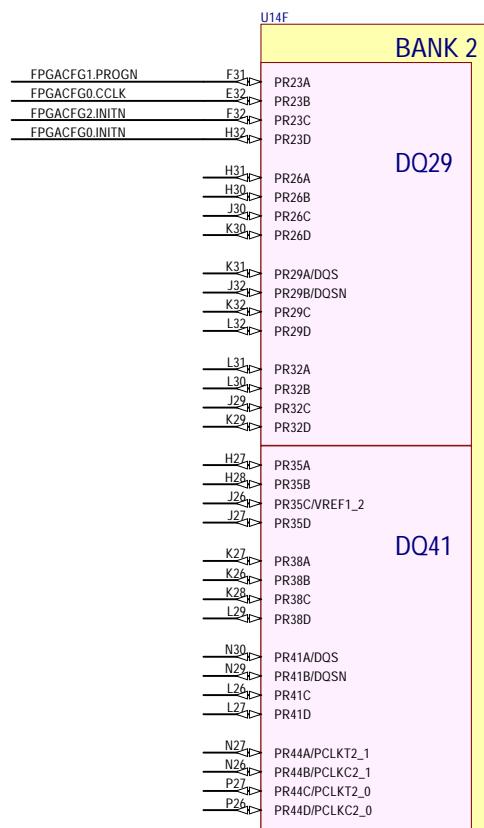
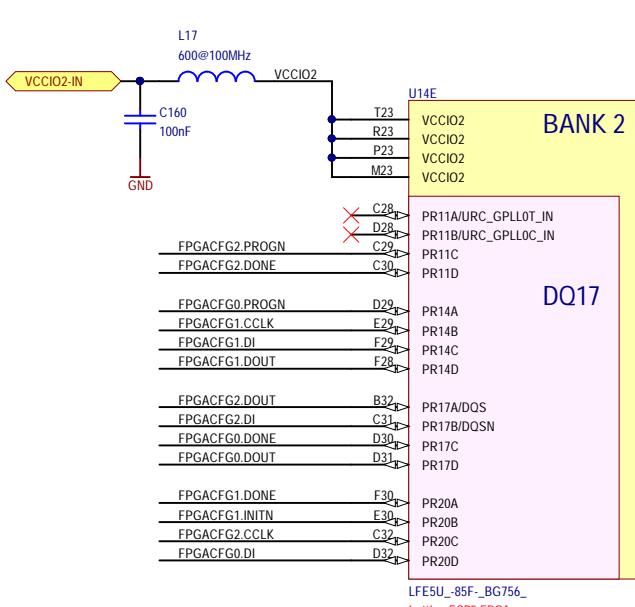
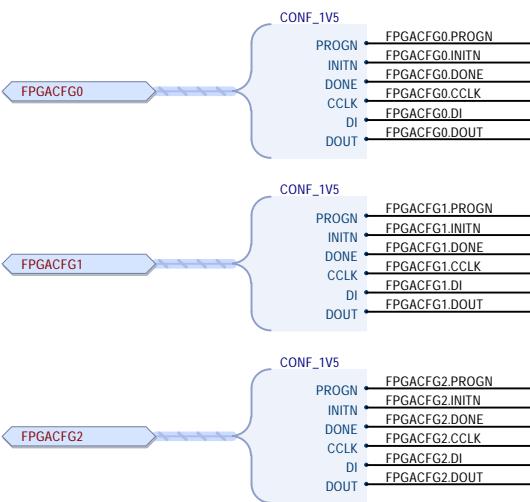
A

B

C

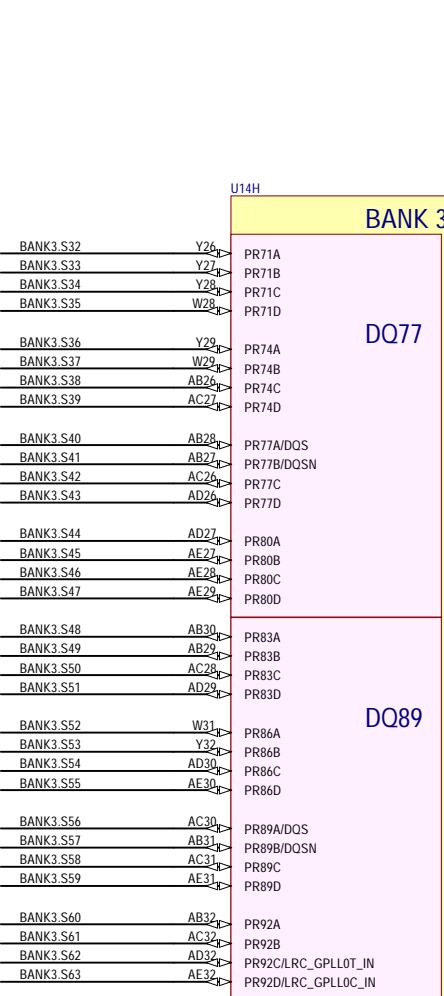
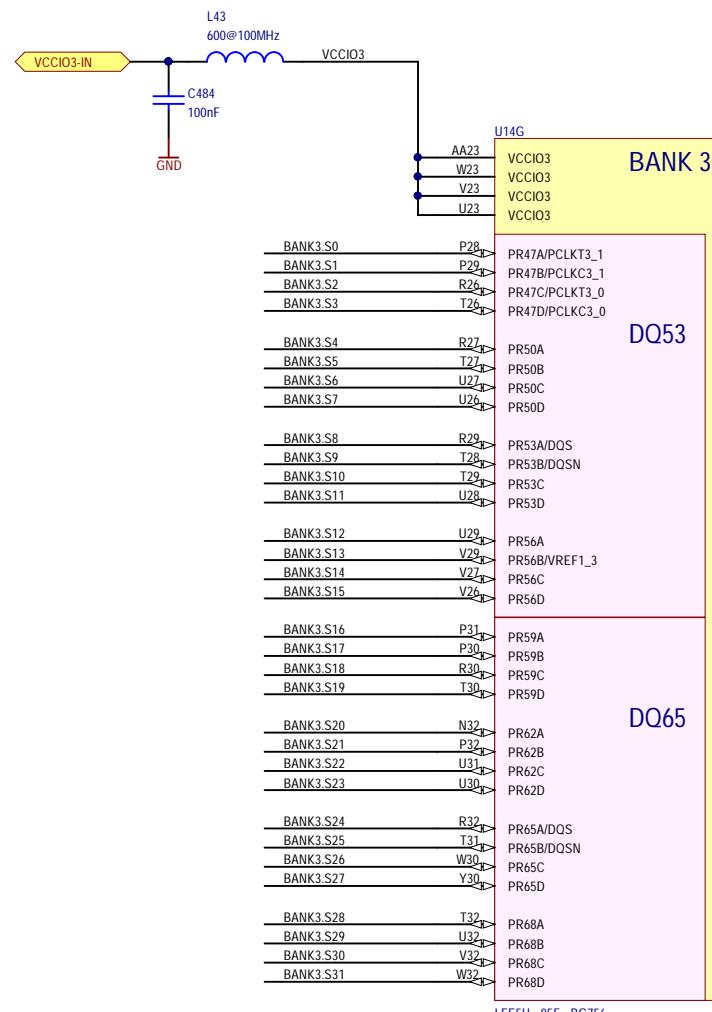
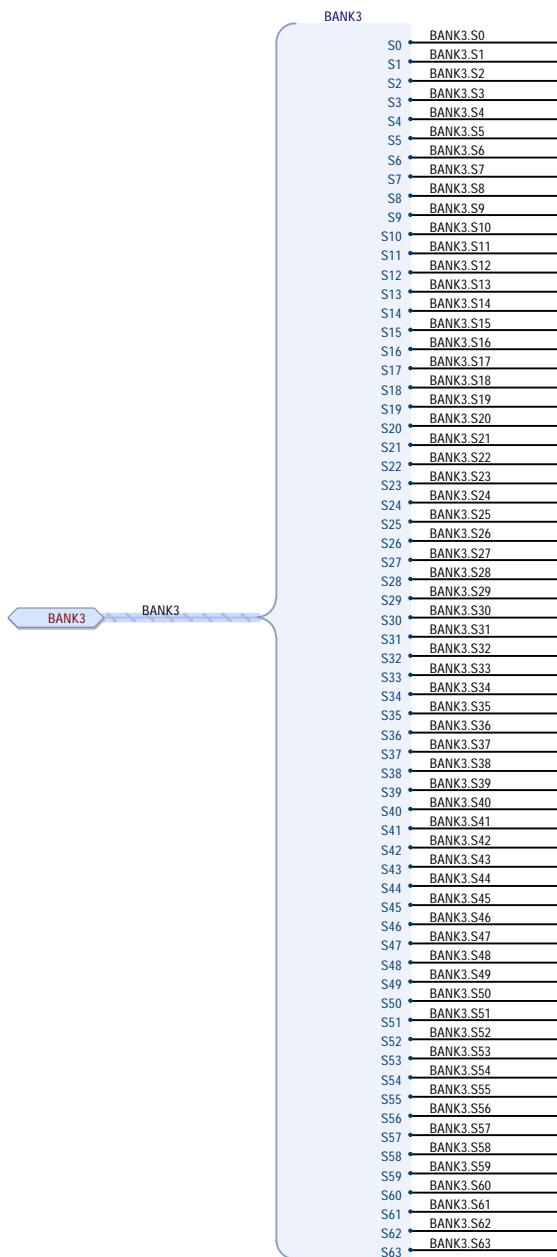
D





Config FPGA - Bank 2

3479 Edison Way Menlo Park CA 94025 +1 (877) 778-8435 siglabs.com	Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
	Revision 1	Sheet 15 of 58	Date 3/12/2017



A

A

B

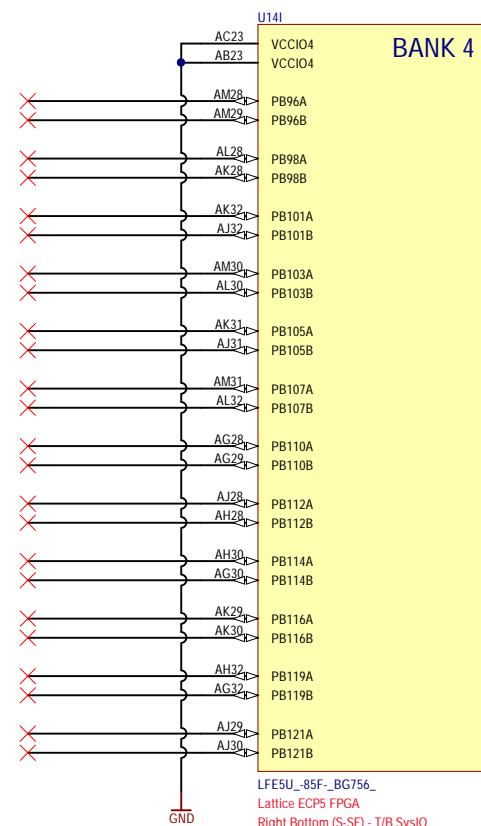
B

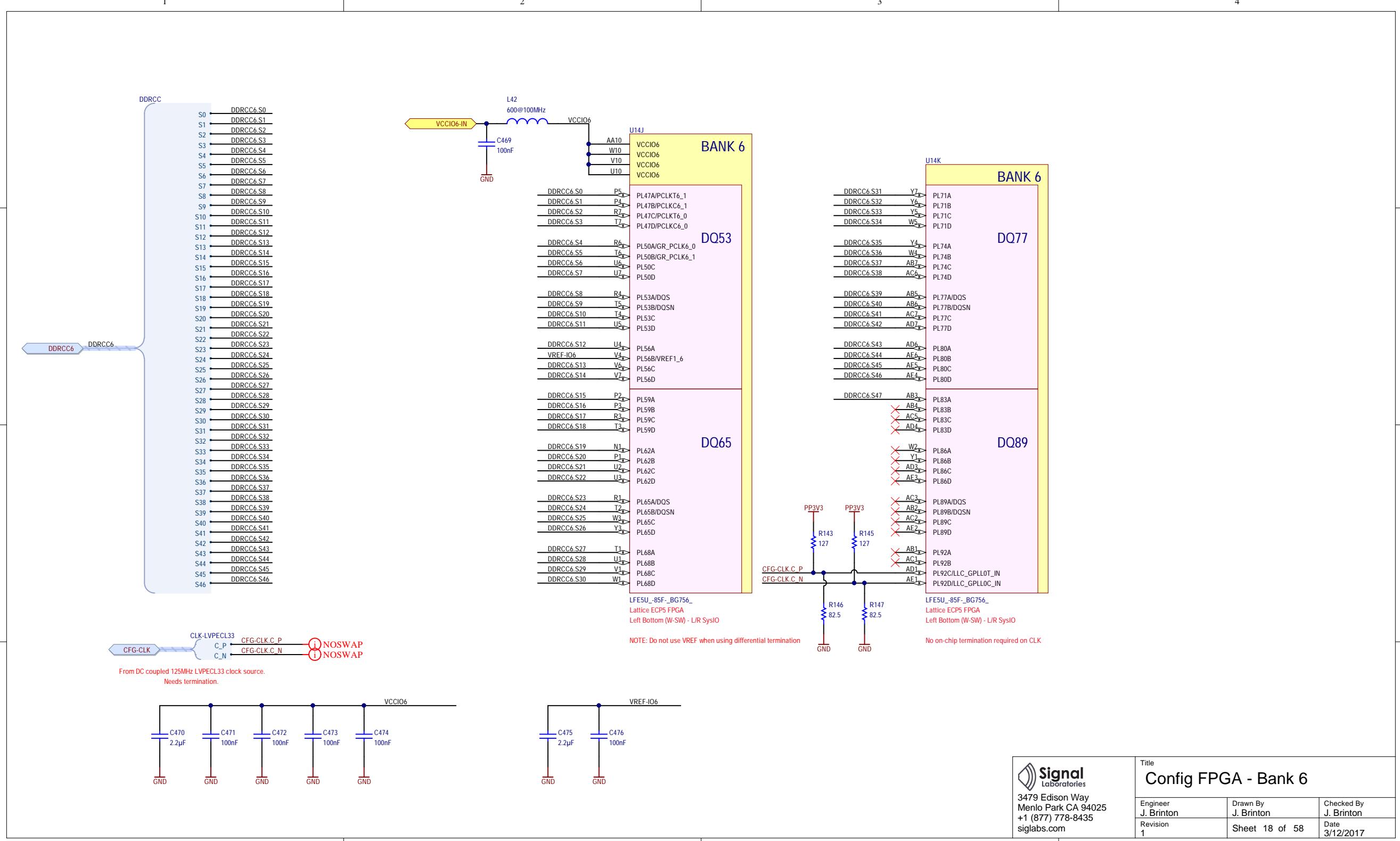
C

C

D

D





A

B

C

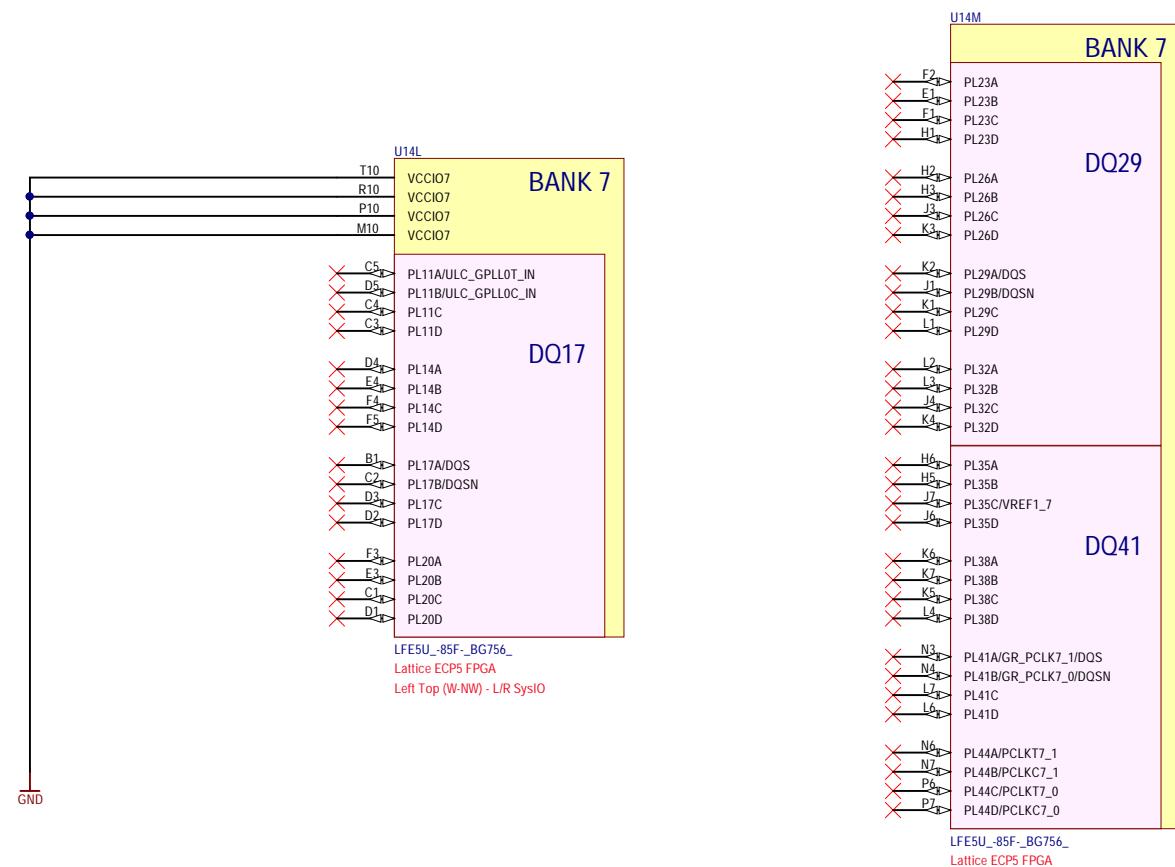
D

A

B

C

D

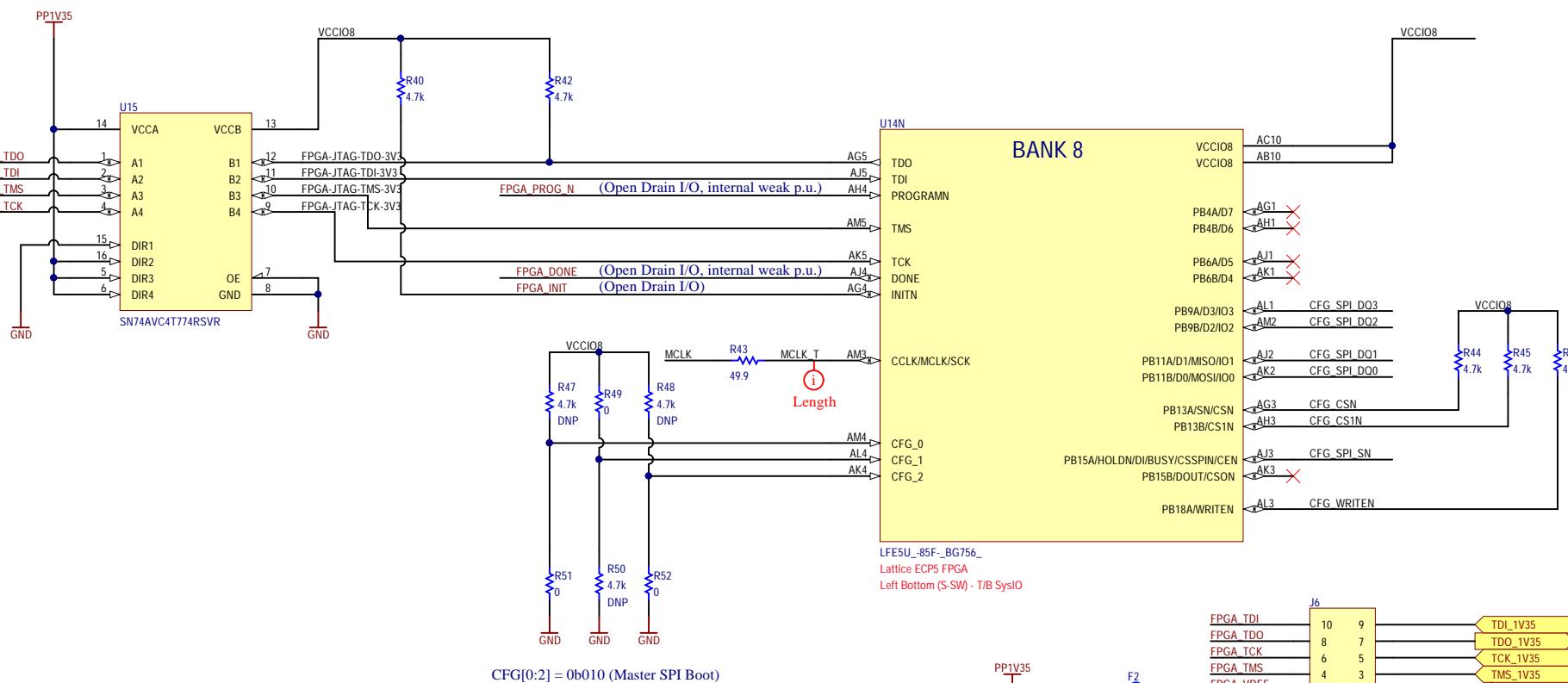


3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siglabs.com

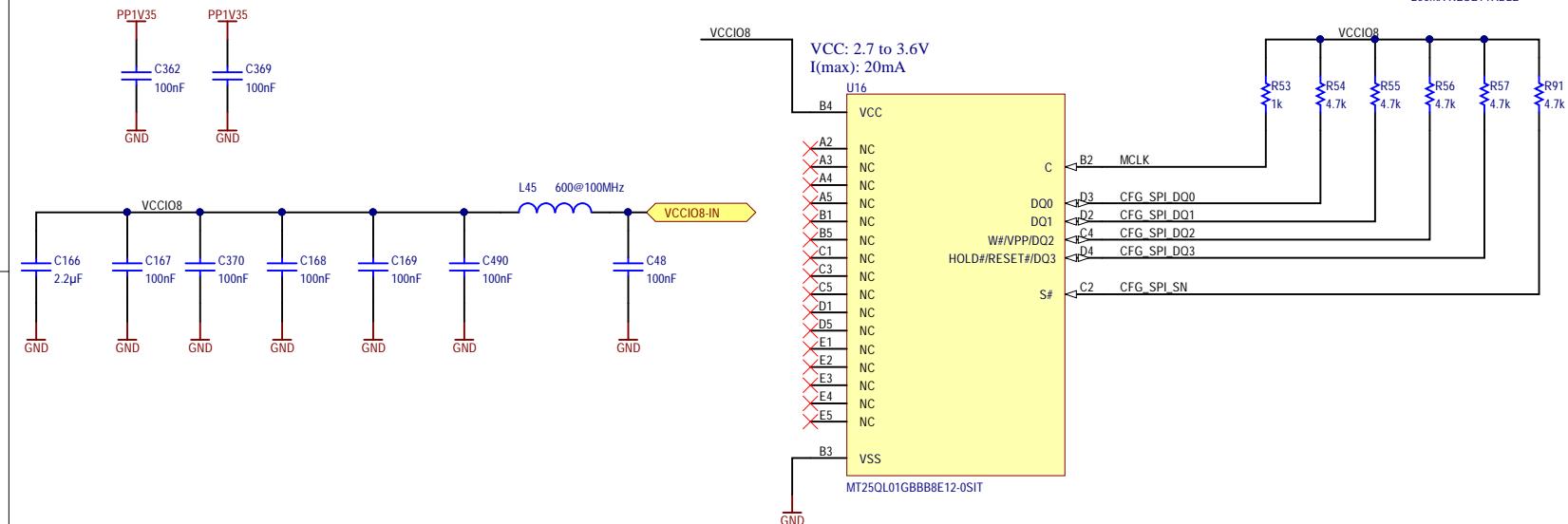
Title
Config FPGA - Bank 7

Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 1	Sheet 19 of 58	Date 3/12/2017

A



C



D

A

B

C

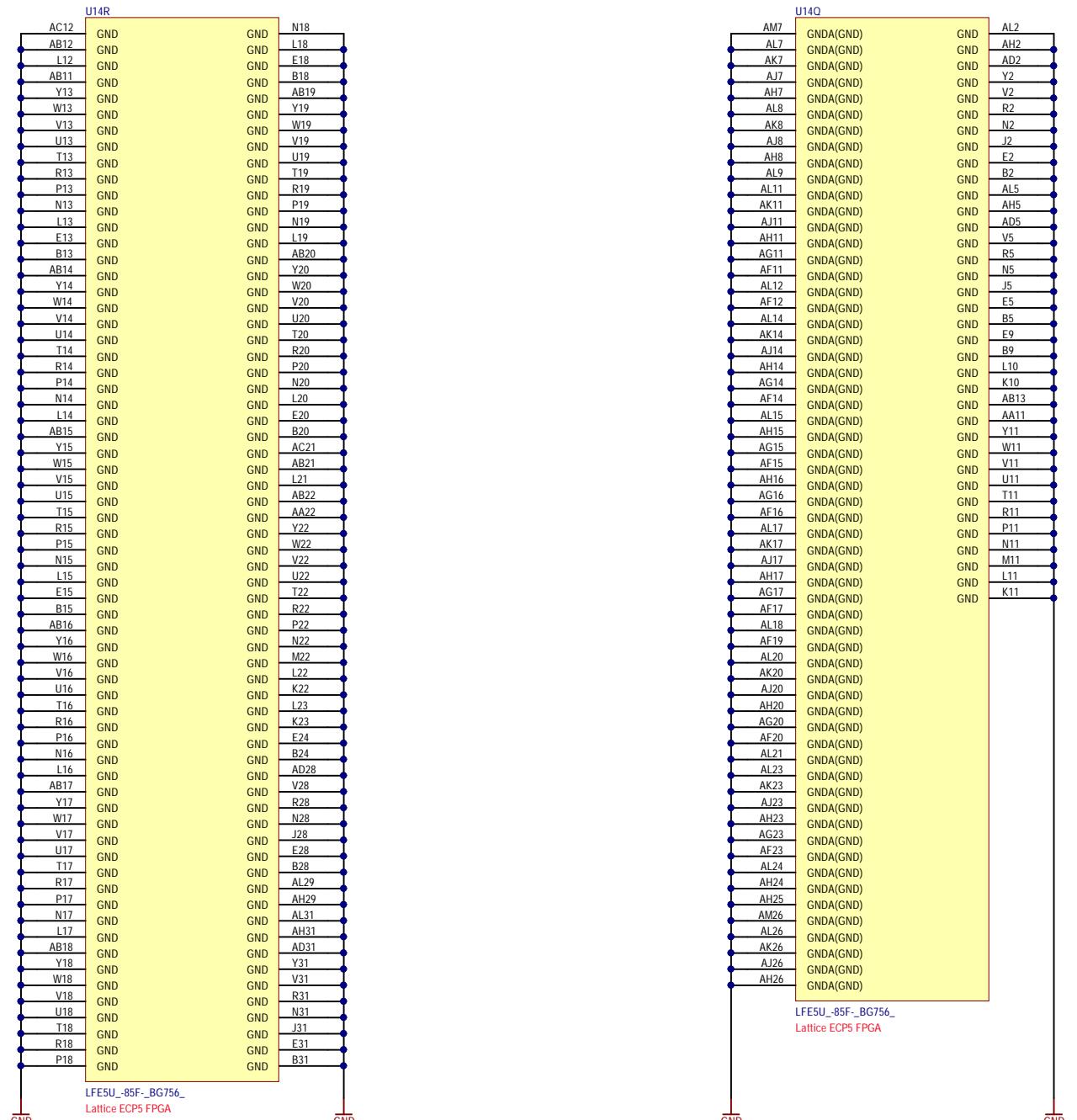
D

A

B

C

D



A

A

B

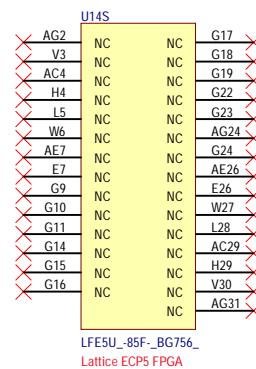
B

C

C

D

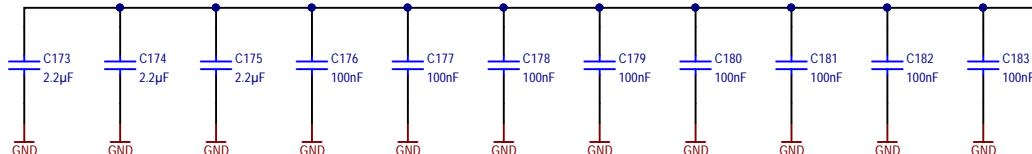
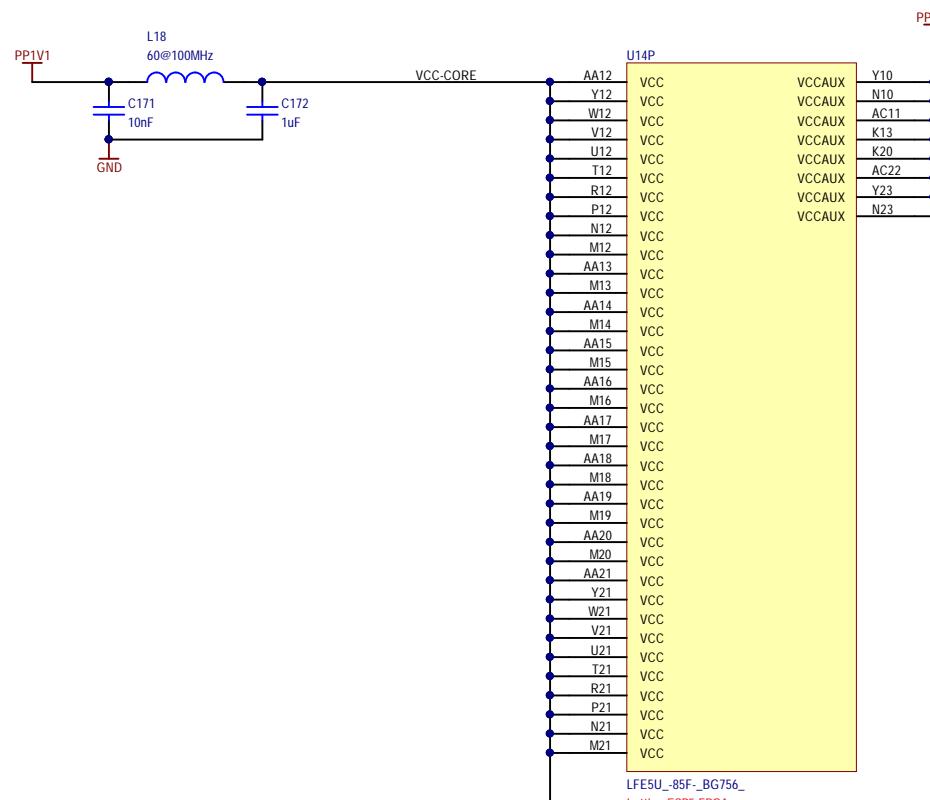
D



3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siglabs.com

Title
Config FPGA - Misc

Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 1	Sheet 22 of 58	Date 3/12/2017



Title

Config FPGA - Power

3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siglabs.com

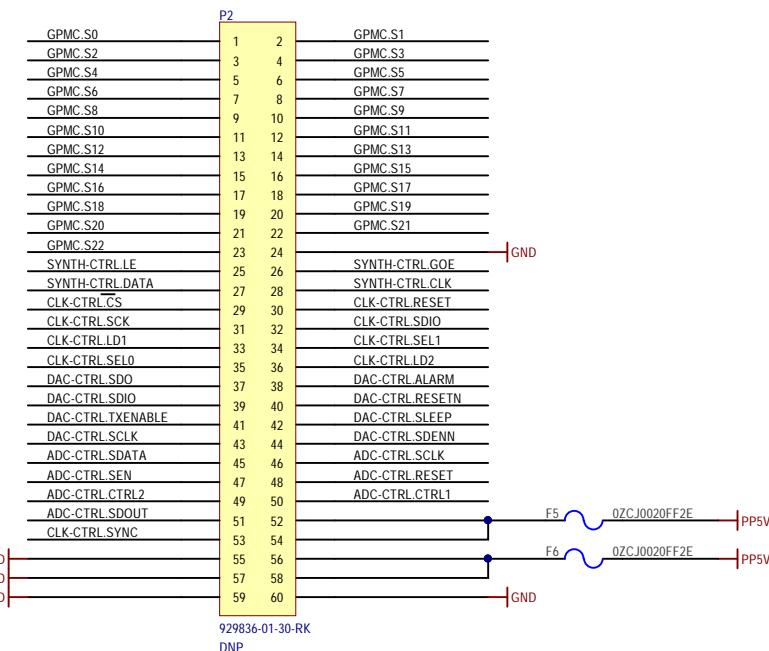
Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 1	Sheet 23 of 58	Date 3/12/2017



3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siqlabs.com

Title	Config FPGA - Serdes		
Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton	
Revision 1	Sheet 24 of 58	Date 3/12/2017	

A

3.3V IO

B

A

B

C

C

D

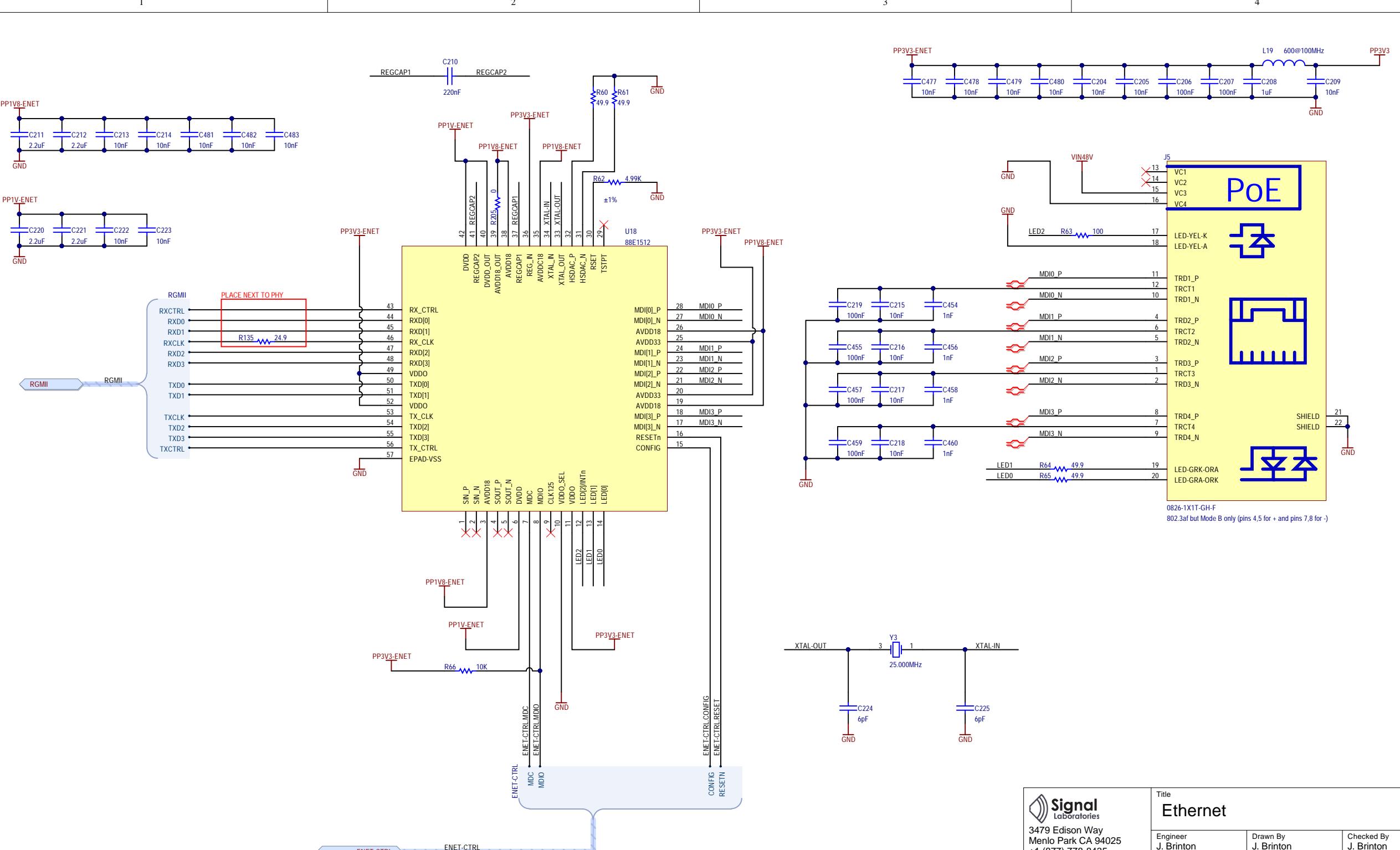
D

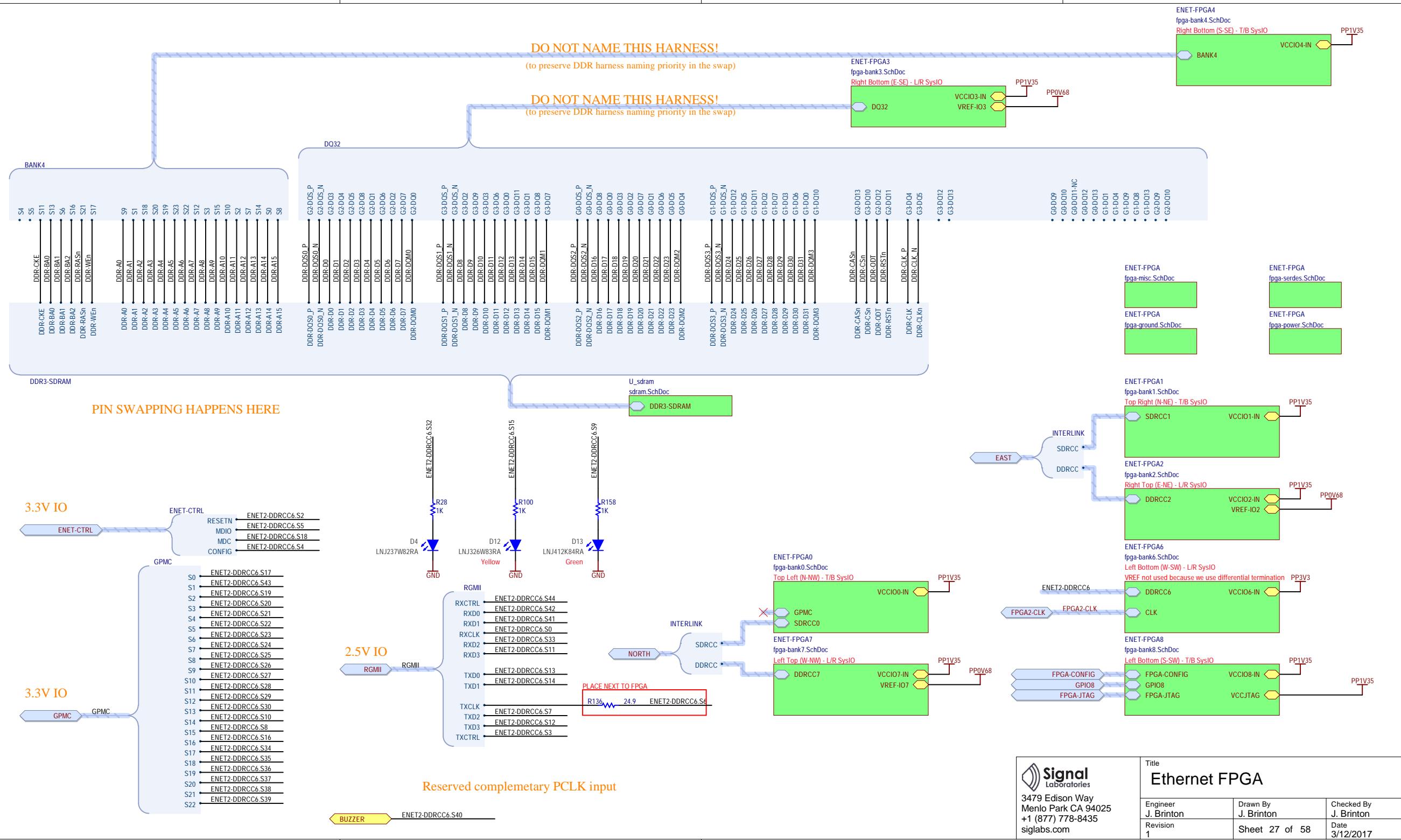


3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siglabs.com

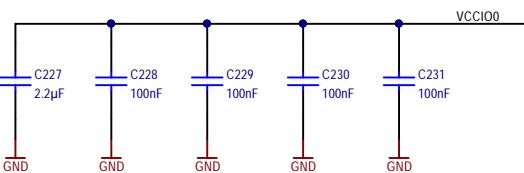
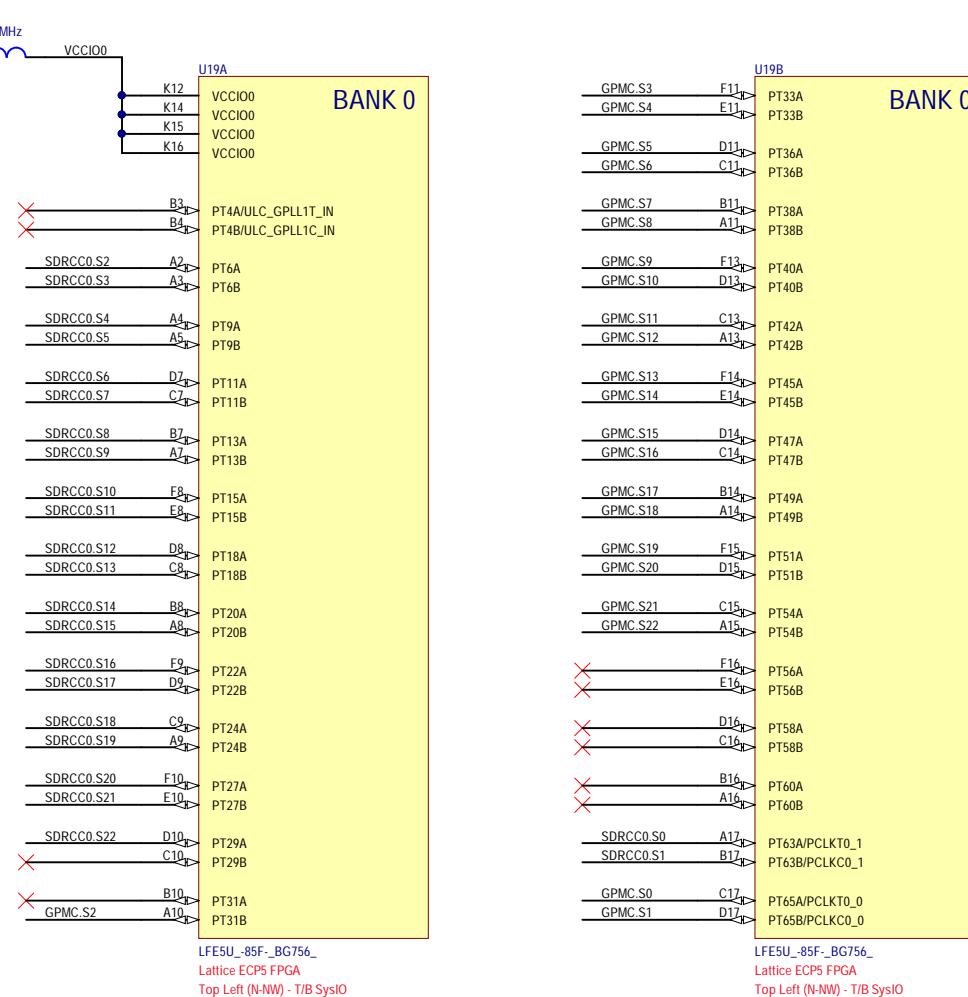
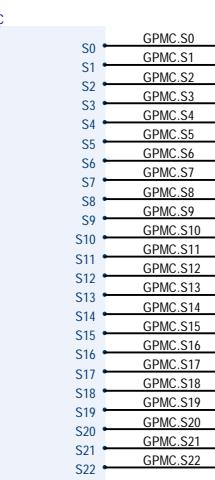
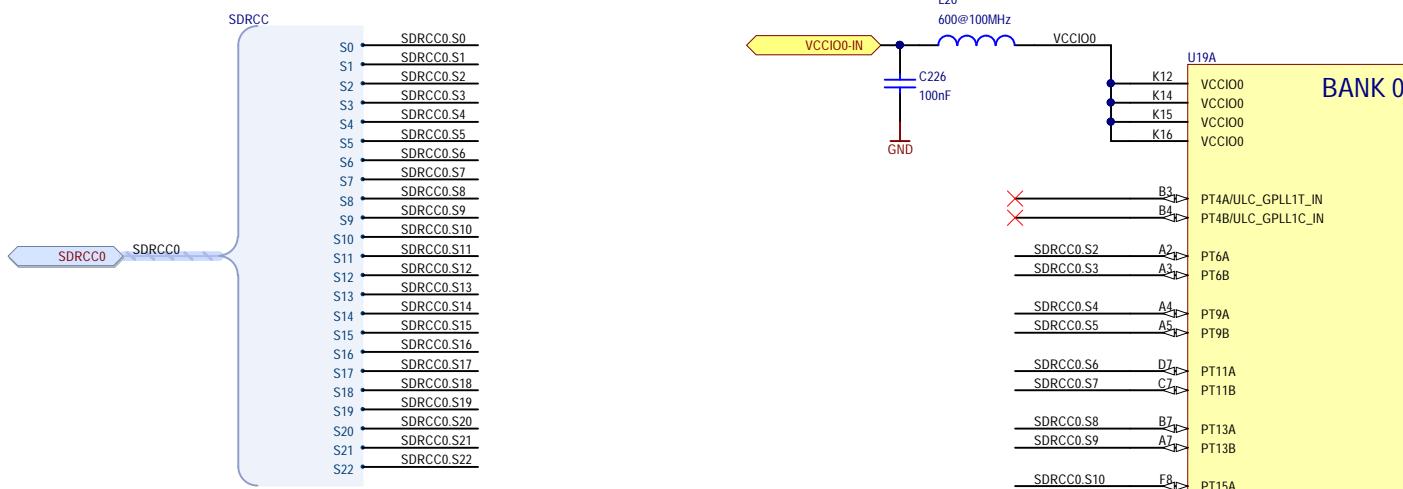
Title
Debug Header

Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 1	Sheet 25 of 58	Date 3/12/2017

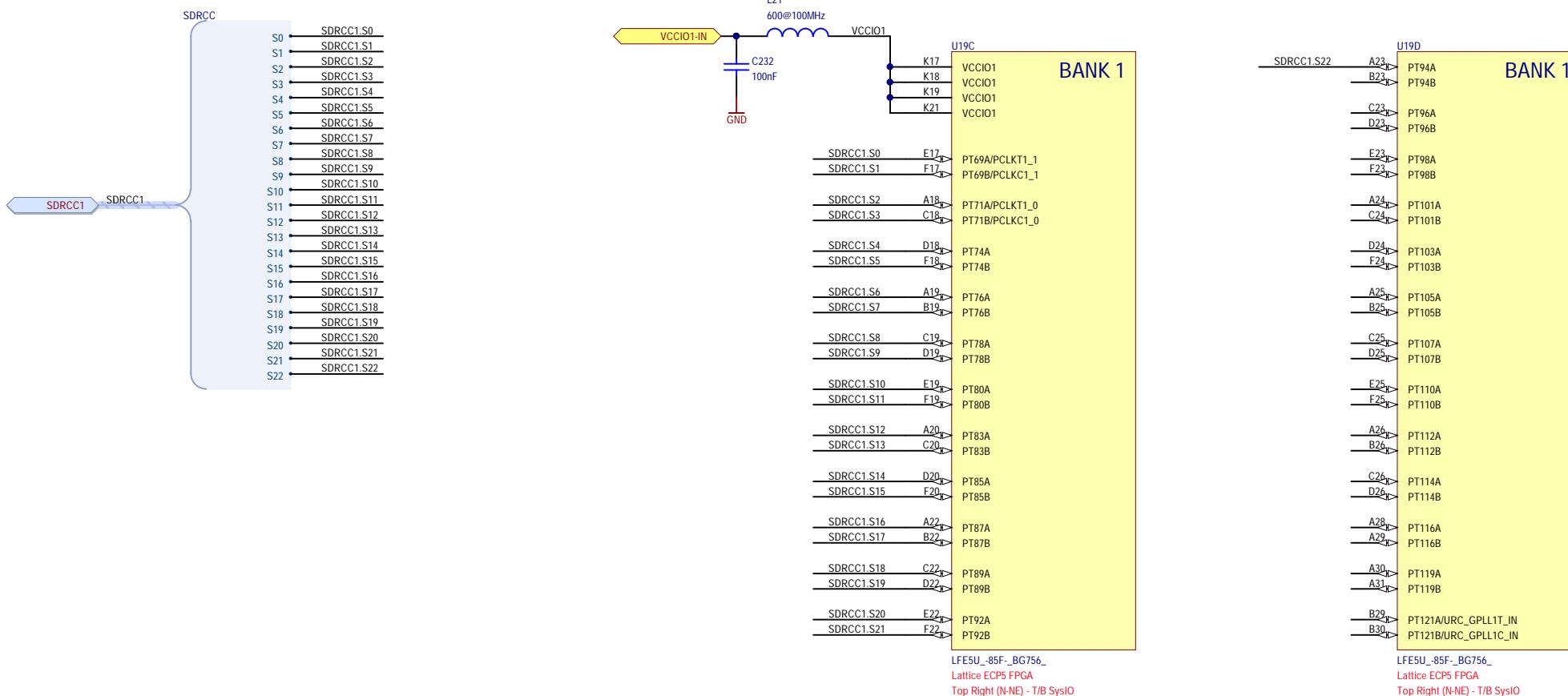




A



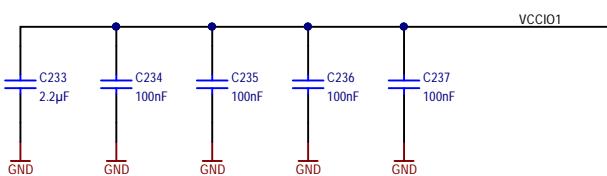
A



B

C

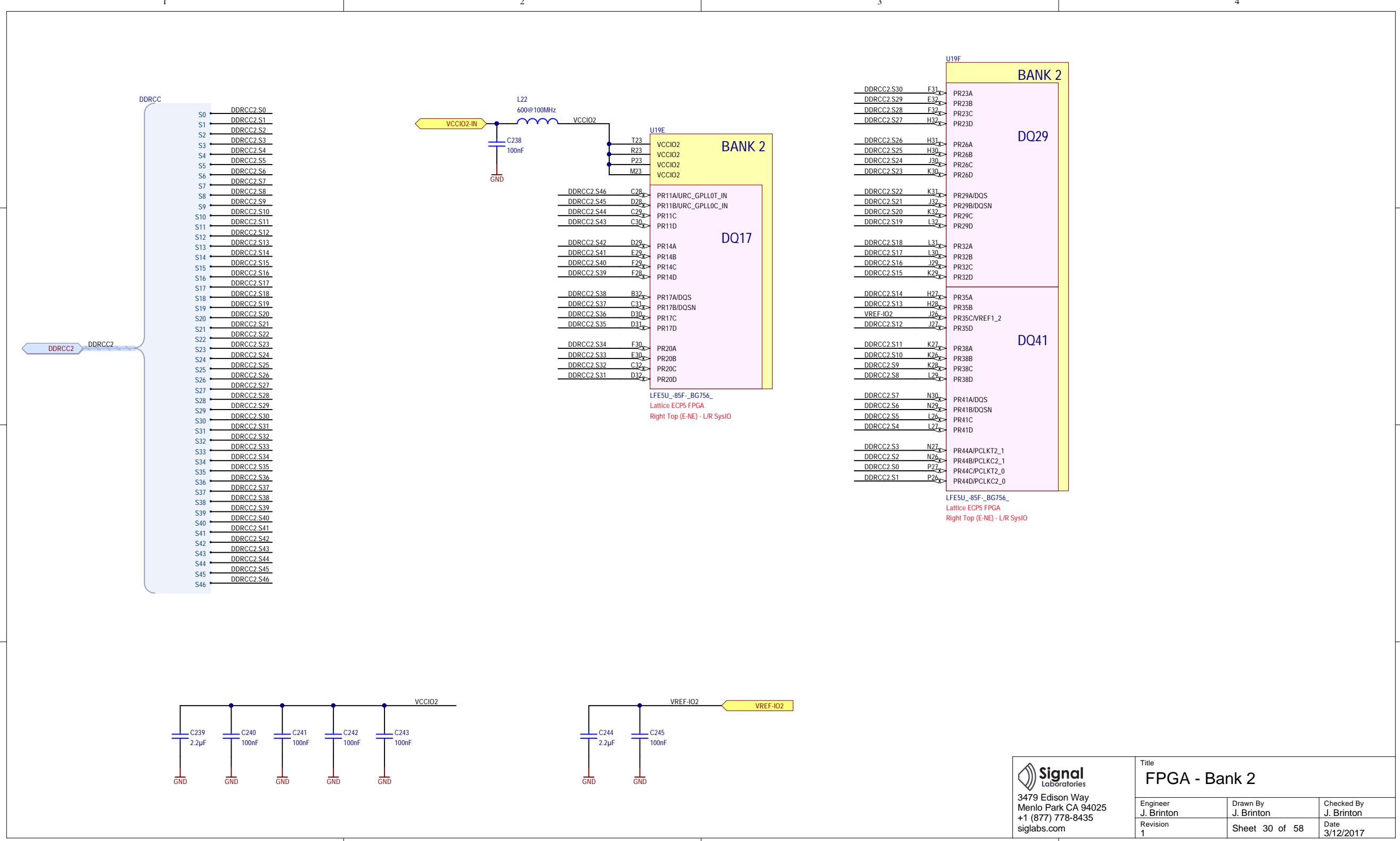
D



Title

FPGA - Bank 1

Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 1	Sheet 29 of 58	Date 3/12/2017



DQ32

- G0-DQS_P DO32.G0-DQS_P
- G0-DQS_N DO32.G0-DQS_N
- G0-D00 DO32.G0-D00
- G0-D01 DO32.G0-D01
- G0-D02 DO32.G0-D02
- G0-D03 DO32.G0-D03
- G0-D04 DO32.G0-D04
- G0-D05 DO32.G0-D05
- G0-D06 DO32.G0-D06
- G0-D07 DO32.G0-D07
- G0-D08 DO32.G0-D08
- G0-D09 DO32.G0-D09
- G0-D10 DO32.G0-D10
- G0-D11-NC DO32.G0-D11-NC
- G0-D12 DO32.G0-D12
- G0-D13 DO32.G0-D13

G1-DQS_P DO32.G1-DQS_P

G1-DQS_N DO32.G1-DQS_N

G1-D00 DO32.G1-D00

G1-D01 DO32.G1-D01

G1-D02 DO32.G1-D02

G1-D03 DO32.G1-D03

G1-D04 DO32.G1-D04

G1-D05 DO32.G1-D05

G1-D06 DO32.G1-D06

G1-D07 DO32.G1-D07

G1-D08 DO32.G1-D08

G1-D09 DO32.G1-D09

G1-D10 DO32.G1-D10

G1-D11 DO32.G1-D11

G1-D12 DO32.G1-D12

G1-D13 DO32.G1-D13

G2-DQS_P DO32.G2-DQS_P

G2-DQS_N DO32.G2-DQS_N

G2-D00 DO32.G2-D00

G2-D01 DO32.G2-D01

G2-D02 DO32.G2-D02

G2-D03 DO32.G2-D03

G2-D04 DO32.G2-D04

G2-D05 DO32.G2-D05

G2-D06 DO32.G2-D06

G2-D07 DO32.G2-D07

G2-D08 DO32.G2-D08

G2-D09 DO32.G2-D09

G2-D10 DO32.G2-D10

G2-D11 DO32.G2-D11

G2-D12 DO32.G2-D12

G2-D13 DO32.G2-D13

G3-DQS_P DO32.G3-DQS_P

G3-DQS_N DO32.G3-DQS_N

G3-D00 DO32.G3-D00

G3-D01 DO32.G3-D01

G3-D02 DO32.G3-D02

G3-D03 DO32.G3-D03

G3-D04 DO32.G3-D04

G3-D05 DO32.G3-D05

G3-D06 DO32.G3-D06

G3-D07 DO32.G3-D07

G3-D08 DO32.G3-D08

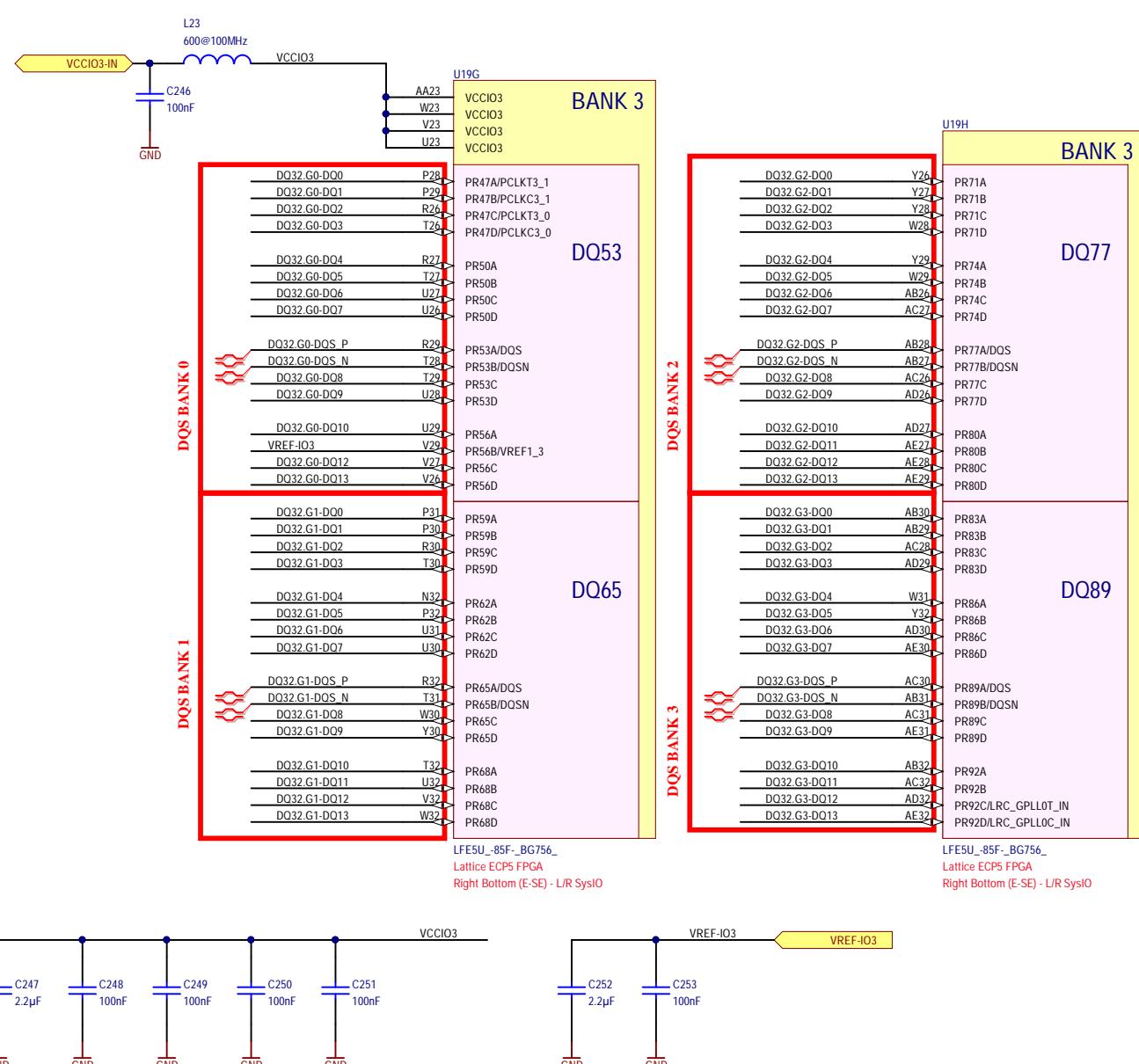
G3-D09 DO32.G3-D09

G3-D10 DO32.G3-D10

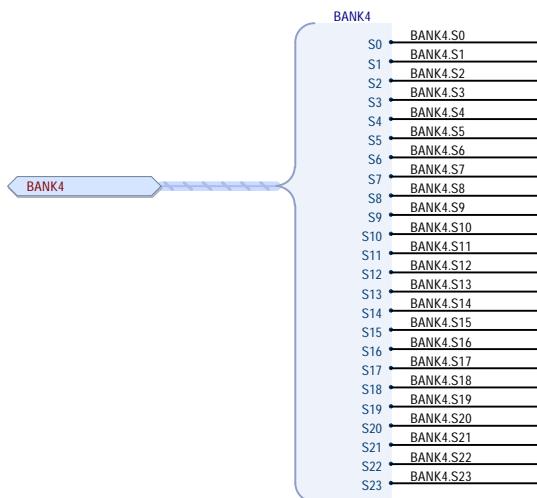
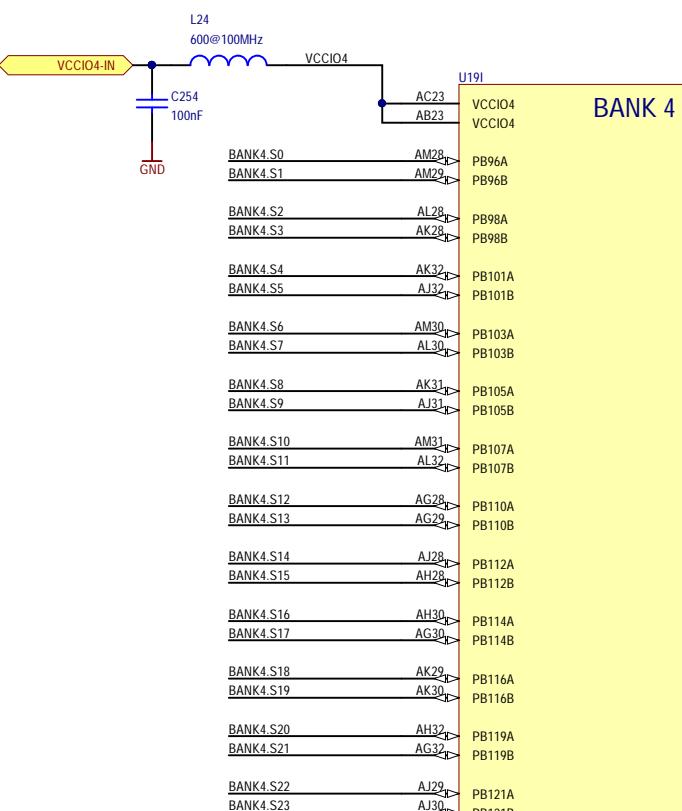
G3-D11 DO32.G3-D11

G3-D12 DO32.G3-D12

G3-D13 DO32.G3-D13



A



B

C

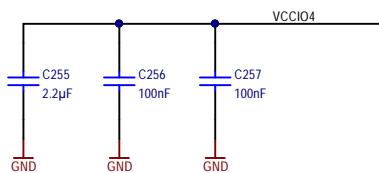
D

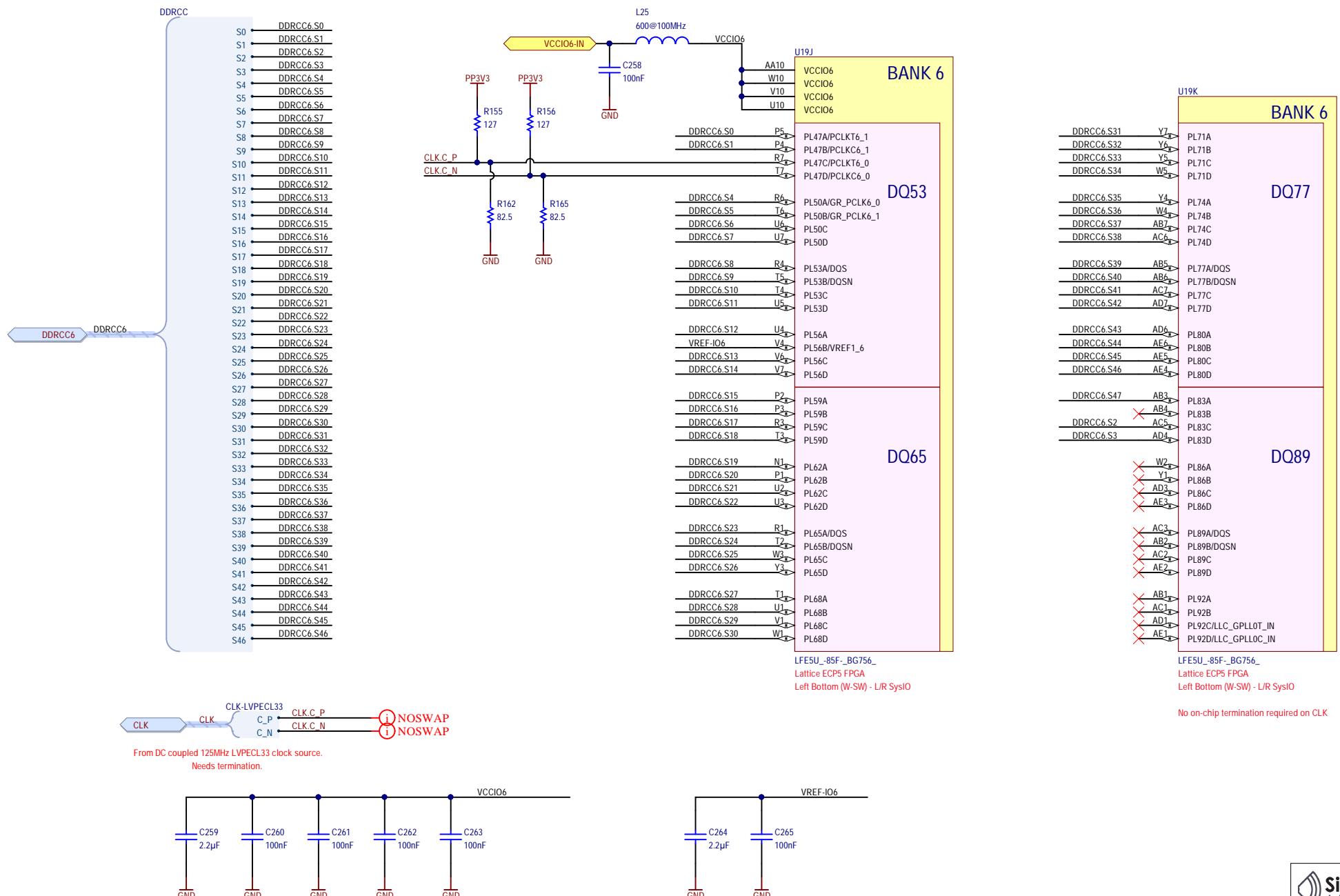
A

B

C

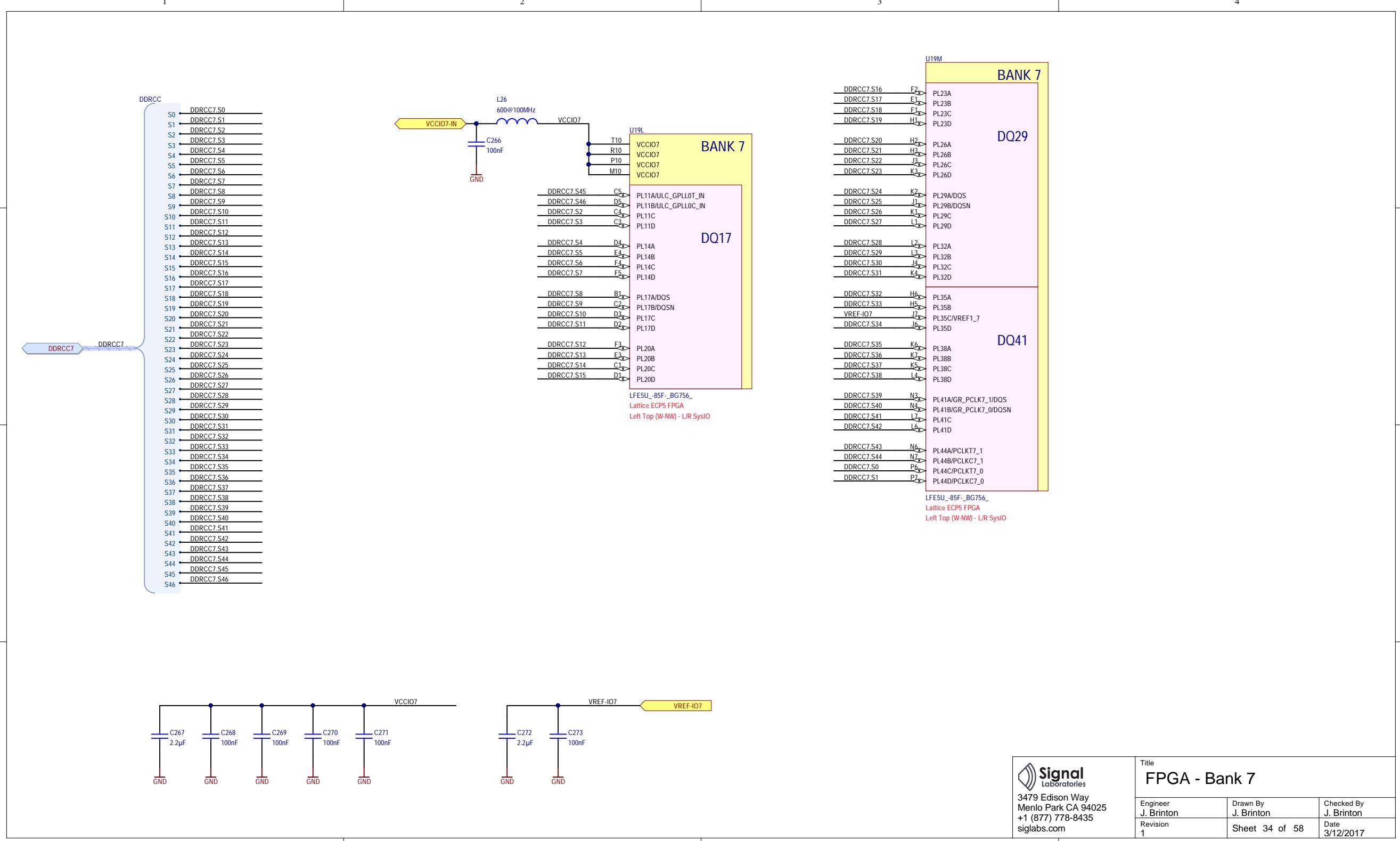
D

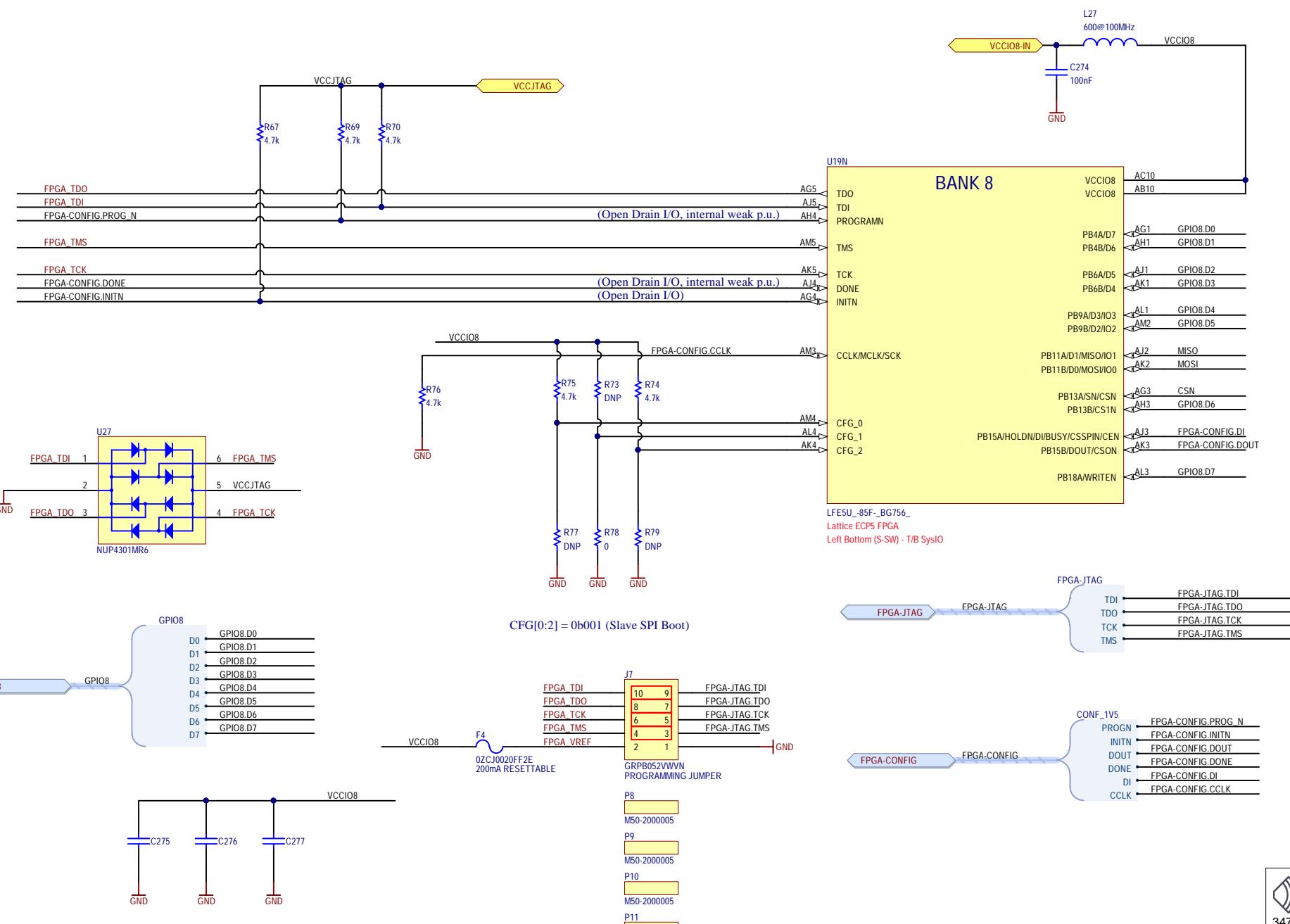




Title

5	Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
	Revision 1	Sheet 33 of 58	Date 3/12/2017





FPGA - Bank 8

5	Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
	Revision 1	Sheet 35 of 58	Date 3/12/2017

A

B

C

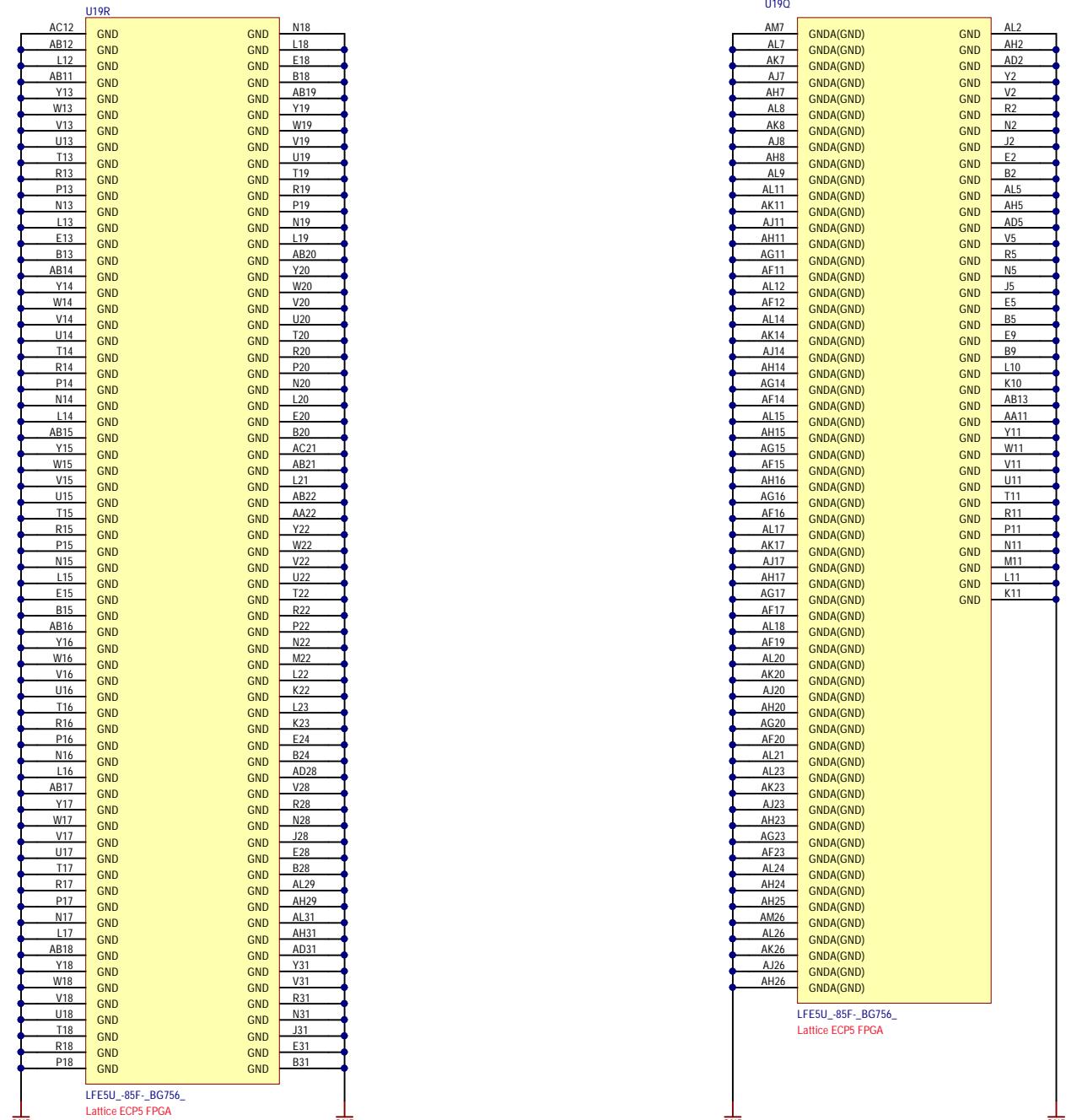
D

A

B

C

D



3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siglabs.com

Title FPGA - Ground

Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 1	Sheet 36 of 58	Date 3/12/2017

A

A

B

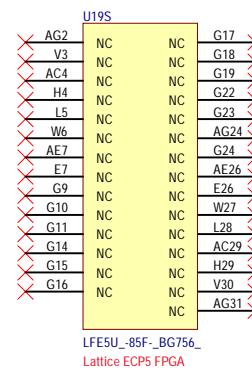
B

C

C

D

D



3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siglabs.com

Title		
FPGA - Misc		
Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	J. Brinton
Revision	Sheet 37 of 58	Date 3/12/2017

A

A

B

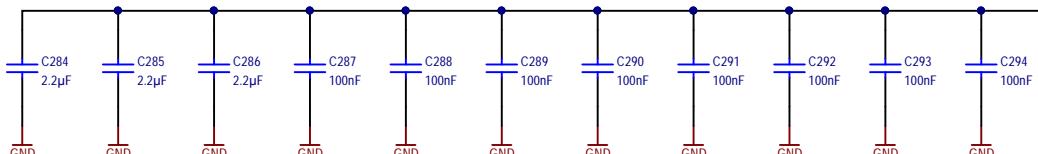
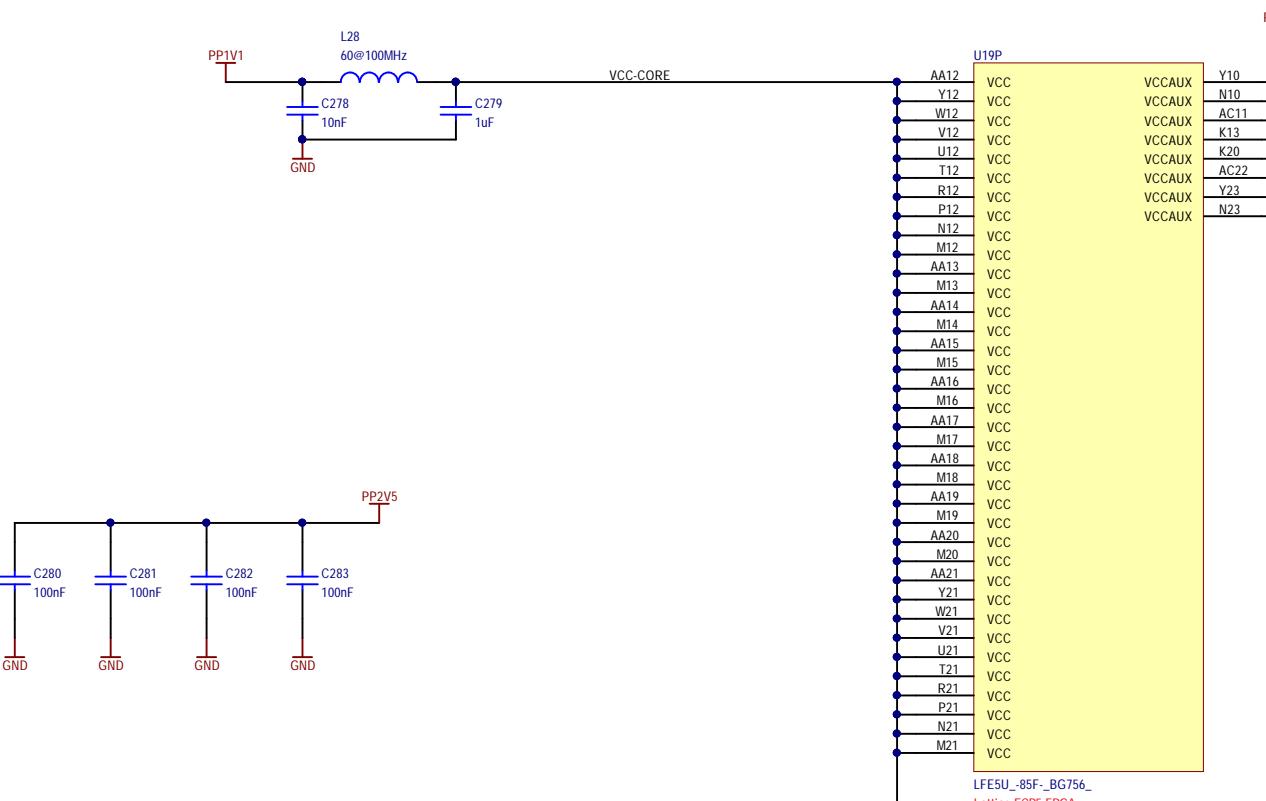
B

C

C

D

D



A

A

B

B

C

C

D

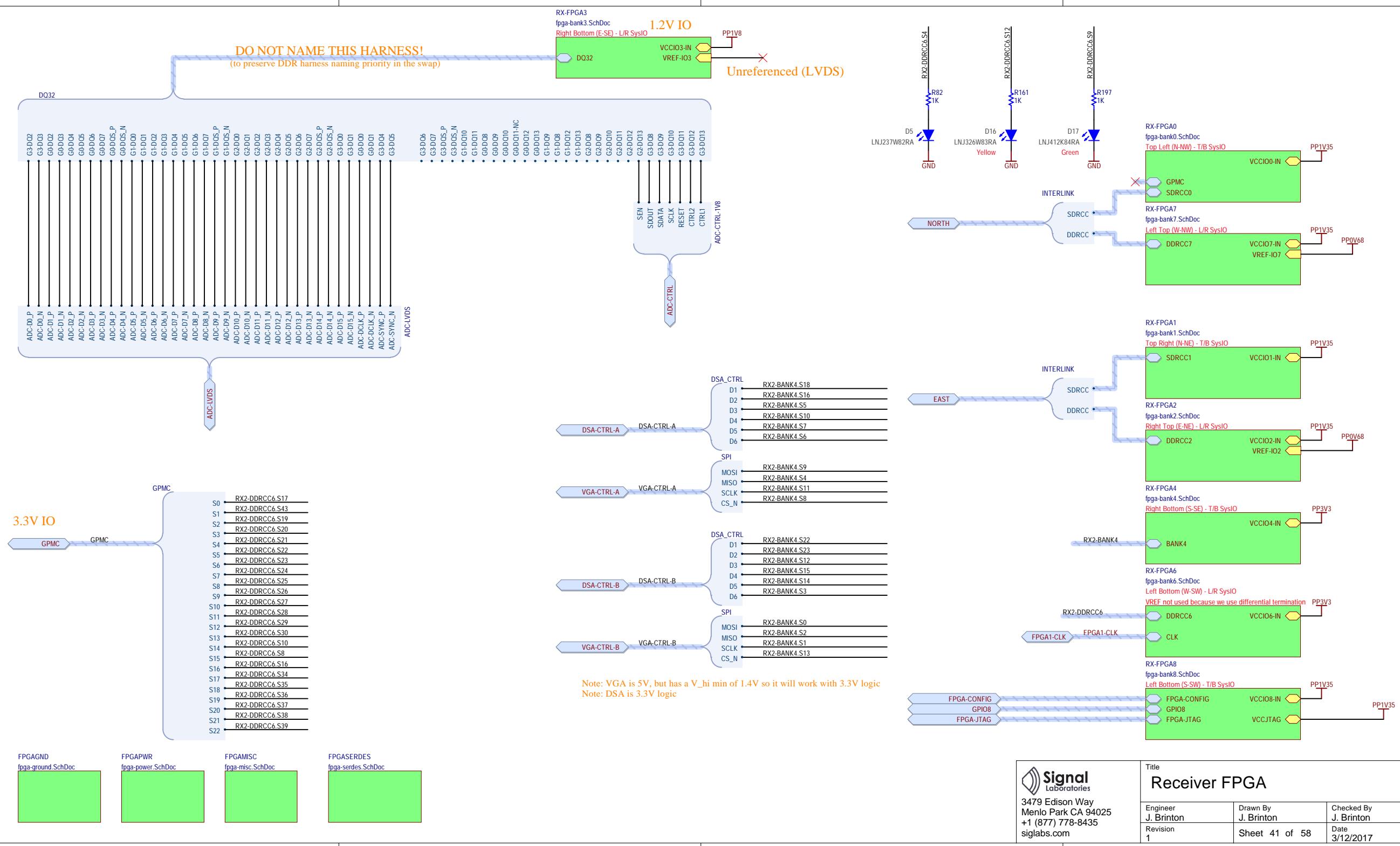
D

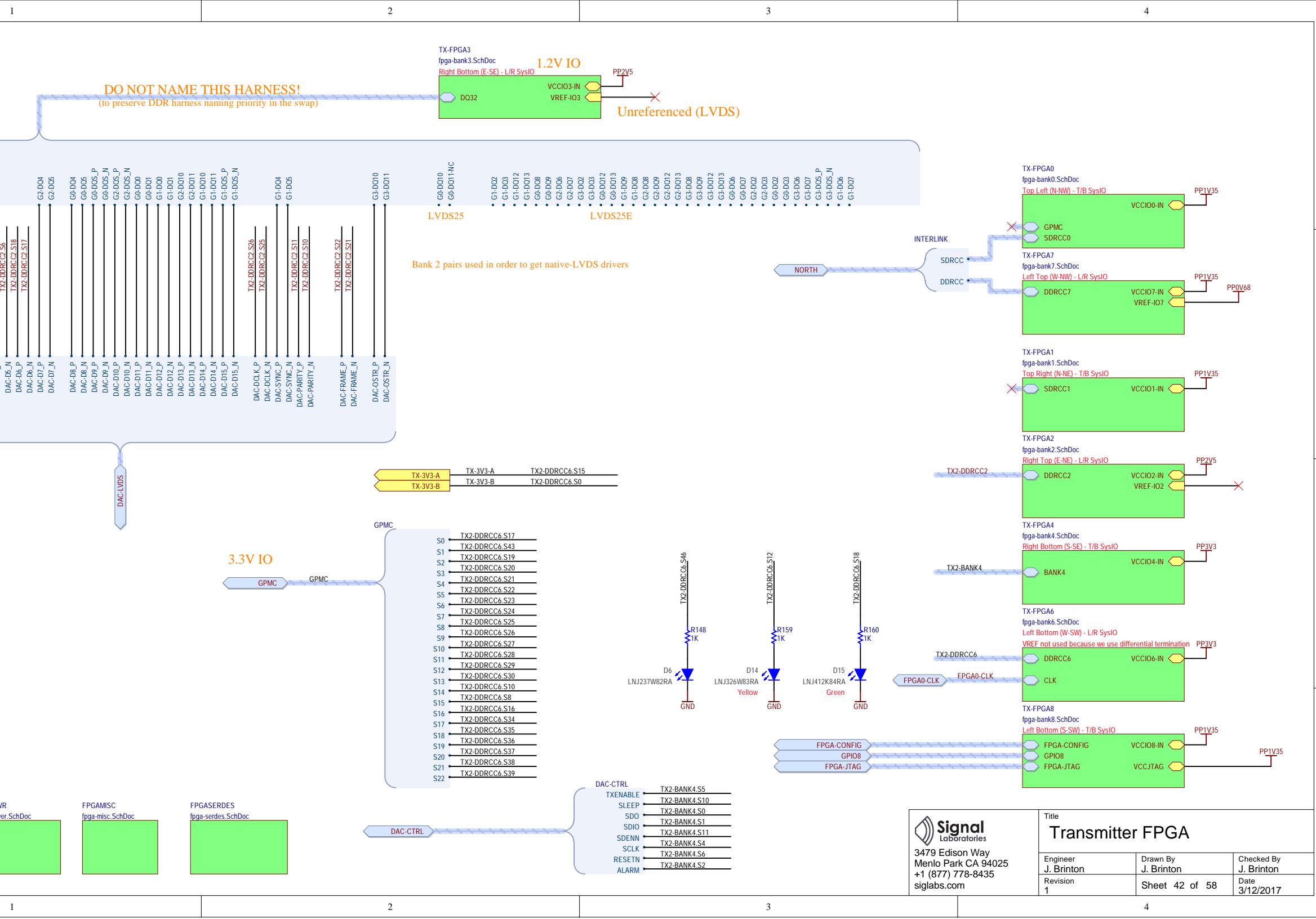


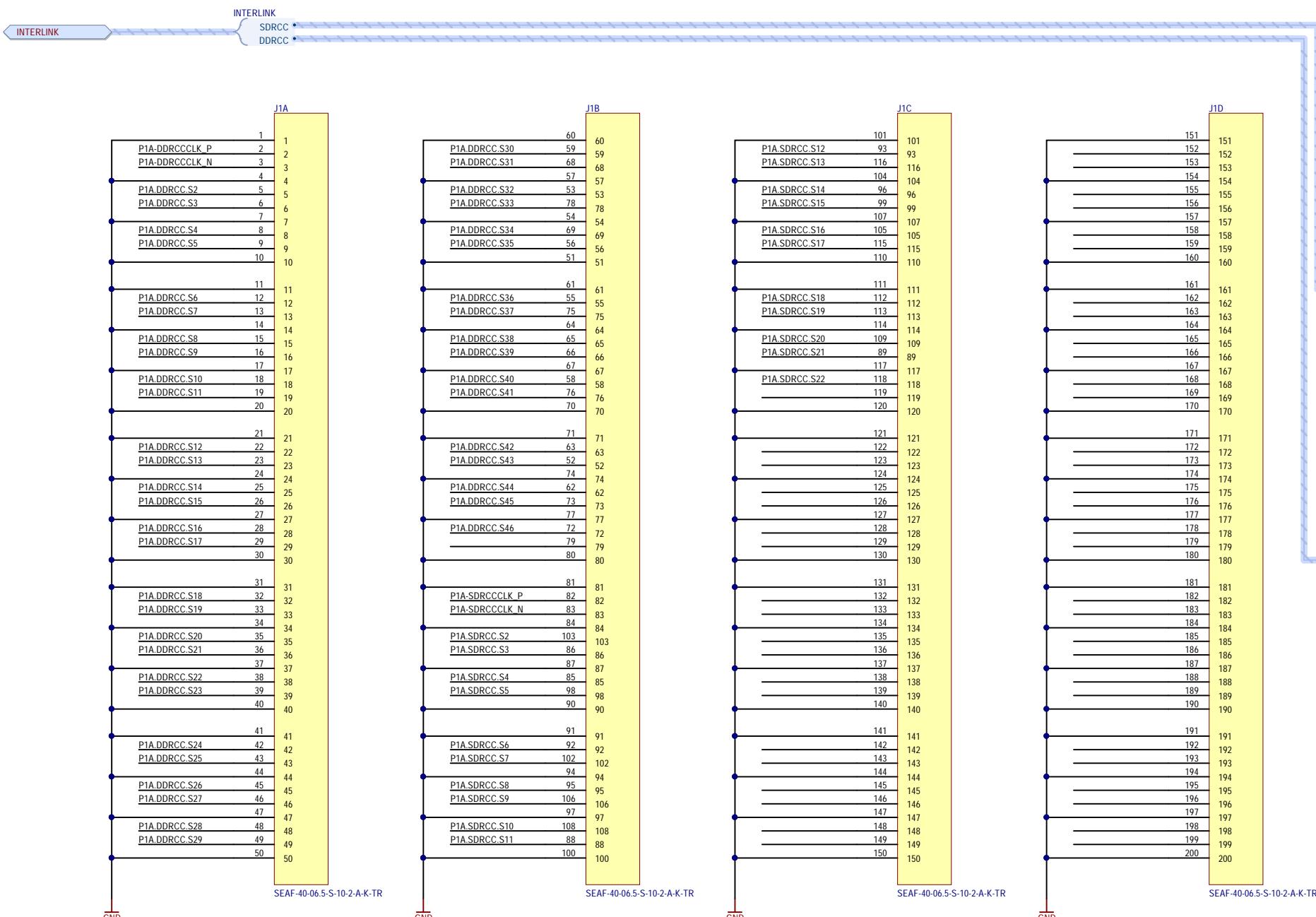
3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siglabs.com

Title
FPGA - Serdes

Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 1	Sheet 39 of 58	Date 3/12/2017







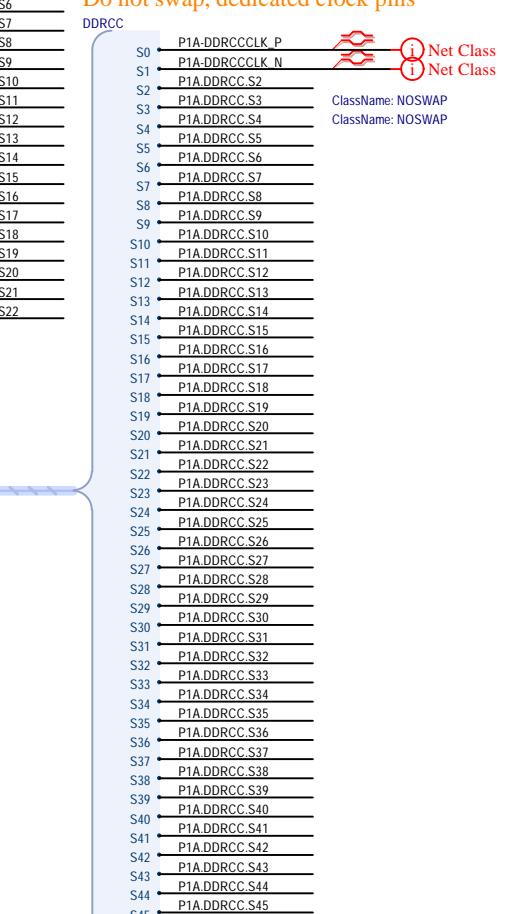
3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siglabs.com

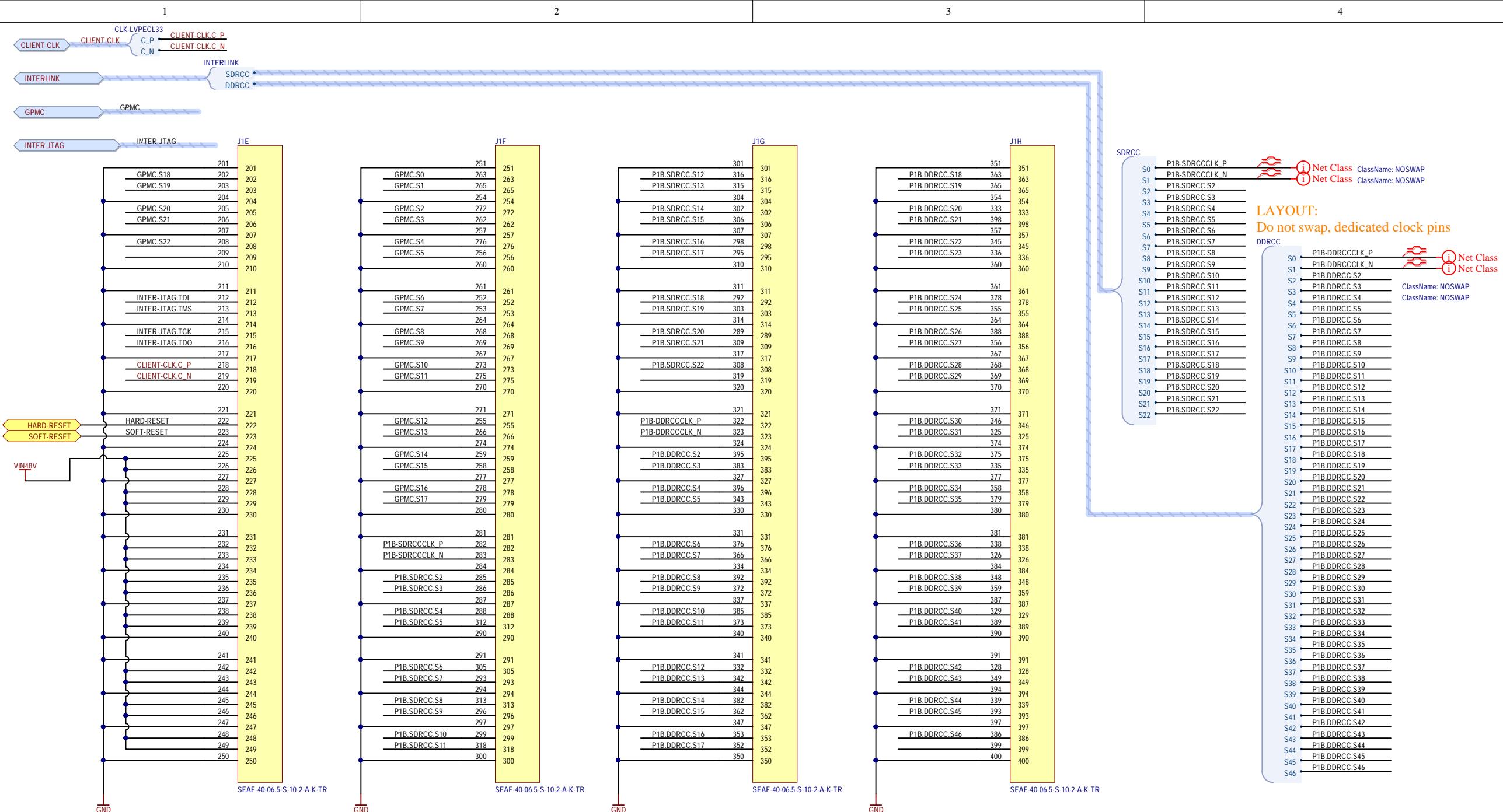
Board-to-Board P1A

Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	J. Brinton

Revision 1 Sheet 43 of 58 Date 3/12/2017

LAYOUT:
Do not swap, dedicated clock pins

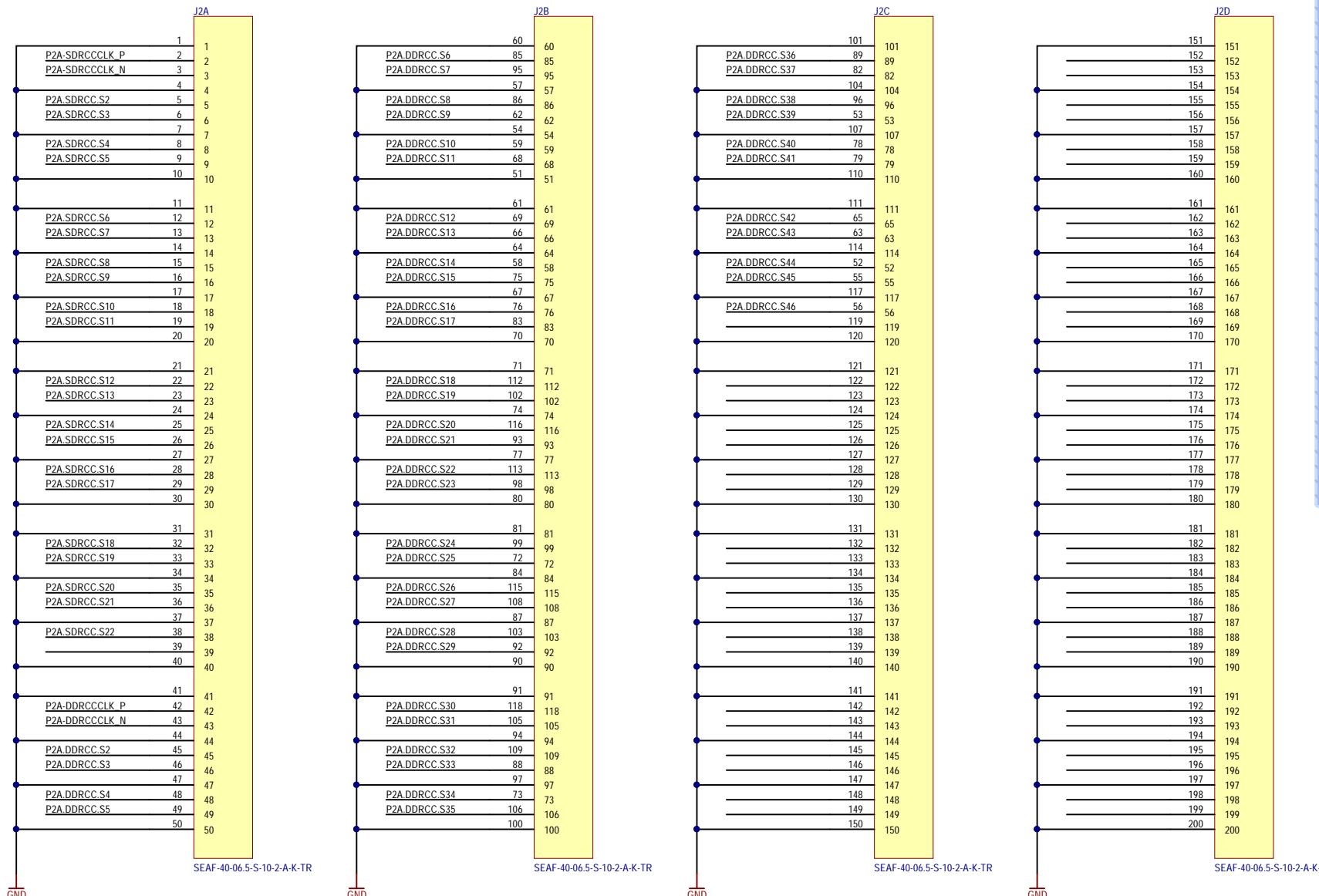




 Laboratorios
3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siglabs.com

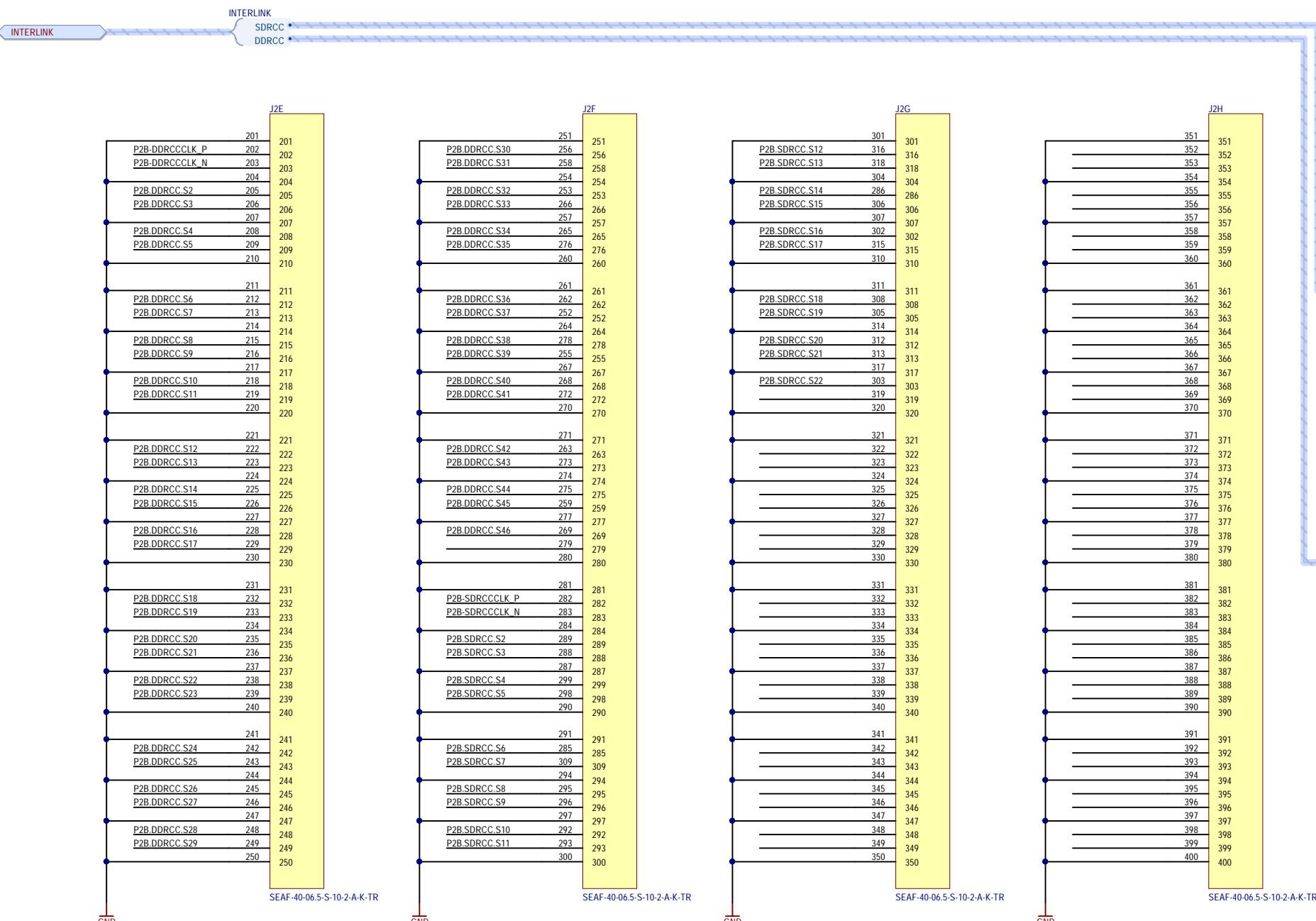
Title	Board-to-Board P1B		
Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton	
Revision 1	Sheet 44 of 58	Date 3/12/2017	

INTERLINK
SDRCC •
DDRCC •



LAYOUT:
Do not swap, dedicated clock pins

SDRCC	P2A-SDRCCCLK_P	Net Class	ClassName: NOSWAP
S0	P2A-SDRCCCLK_N	Net Class	ClassName: NOSWAP
S1	P2A_SDRCC_S2		
S2	P2A_SDRCC_S3		
S3	P2A_SDRCC_S4		
S4	P2A_SDRCC_S5		
S5	P2A_SDRCC_S6		
S6	P2A_SDRCC_S7		
S7	P2A_SDRCC_S8		
S8	P2A_SDRCC_S9		
S9	P2A_SDRCC_S10		
S10	P2A_SDRCC_S11		
S11	P2A_SDRCC_S12		
S12	P2A_SDRCC_S13		
S13	P2A_SDRCC_S14		
S14	P2A_SDRCC_S15		
S15	P2A_SDRCC_S16		
S16	P2A_SDRCC_S17		
S17	P2A_SDRCC_S18		
S18	P2A_SDRCC_S19		
S19	P2A_SDRCC_S20		
S20	P2A_SDRCC_S21		
S21	P2A_SDRCC_S22		
S22	P2A_SDRCC_S23		
S23	P2A_SDRCC_S24		
S24	P2A_SDRCC_S25		
S25	P2A_SDRCC_S26		
S26	P2A_SDRCC_S27		
S27	P2A_SDRCC_S28		
S28	P2A_SDRCC_S29		
S29	P2A_SDRCC_S30		
S30	P2A_SDRCC_S31		
S31	P2A_SDRCC_S32		
S32	P2A_SDRCC_S33		
S33	P2A_SDRCC_S34		
S34	P2A_SDRCC_S35		
S35	P2A_SDRCC_S36		
S36	P2A_SDRCC_S37		
S37	P2A_SDRCC_S38		
S38	P2A_SDRCC_S39		
S39	P2A_SDRCC_S40		
S40	P2A_SDRCC_S41		
S41	P2A_SDRCC_S42		
S42	P2A_SDRCC_S43		
S43	P2A_SDRCC_S44		
S44	P2A_SDRCC_S45		
S45	P2A_SDRCC_S46		
S46	P2A_SDRCC_S47		



SDRCC

S0 P2B-SDRCCCLK_P
S1 P2B-SDRCCCLK_N
S2 P2B-SDRCC_S2
S3 P2B-SDRCC_S3
S4 P2B-SDRCC_S4
S5 P2B-SDRCC_S5
S6 P2B-SDRCC_S6
S7 P2B-SDRCC_S7
S8 P2B-SDRCC_S8
S9 P2B-SDRCC_S9
S10 P2B-SDRCC_S10
S11 P2B-SDRCC_S11
S12 P2B-SDRCC_S12
S13 P2B-SDRCC_S13
S14 P2B-SDRCC_S14
S15 P2B-SDRCC_S15
S16 P2B-SDRCC_S16
S17 P2B-SDRCC_S17
S18 P2B-SDRCC_S18
S19 P2B-SDRCC_S19
S20 P2B-SDRCC_S20
S21 P2B-SDRCC_S21
S22 P2B-SDRCC_S22

LAYOUT:
Do not swap, dedicated clock pins

DDRCC

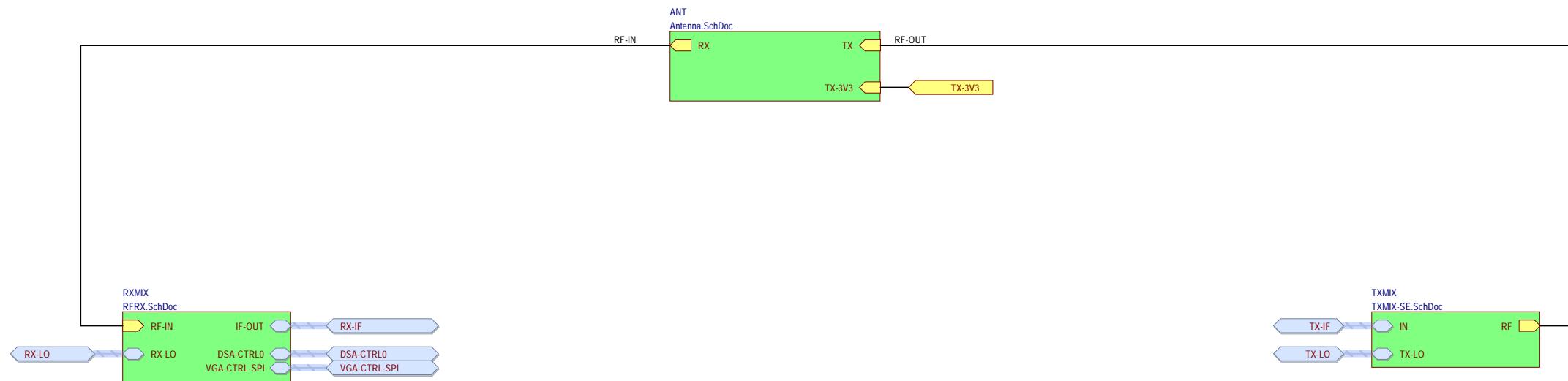
S0 P2B-DDRCCCLK_P
S1 P2B-DDRCCCLK_N
S2 P2B-DDRCC_S2
S3 P2B-DDRCC_S3
S4 P2B-DDRCC_S4
S5 P2B-DDRCC_S5
S6 P2B-DDRCC_S6
S7 P2B-DDRCC_S7
S8 P2B-DDRCC_S8
S9 P2B-DDRCC_S9
S10 P2B-DDRCC_S10
S11 P2B-DDRCC_S11
S12 P2B-DDRCC_S12
S13 P2B-DDRCC_S13
S14 P2B-DDRCC_S14
S15 P2B-DDRCC_S15
S16 P2B-DDRCC_S16
S17 P2B-DDRCC_S17
S18 P2B-DDRCC_S18
S19 P2B-DDRCC_S19
S20 P2B-DDRCC_S20
S21 P2B-DDRCC_S21
S22 P2B-DDRCC_S22



3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siglabs.com

Title
Board-to-Board P2B

Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 1	Sheet 46 of 58	Date 3/12/2017



50-ohm Grounded Coplanar Waveguide

TOP and BOTTOM LAYERS ONLY

Er (FR408 or RT4xxx) = 3.6
 Dielectric Thickness = 0.10mm [3.9mil]
 Copper Thickness (1oz outer) = 0.036mm [1.4mil]
 Trace Width = 0.21mm [11.8mil]
 Coplanar gap = 0.11mm [4.3mil]

100-ohm Differential Pair

EXTERNAL

Er (FR408 or RT4xxx) = 3.6
 Dielectric Thickness = 0.10mm [3.9mil]
 Copper Thickness (1 oz) = 0.036mm [1.4mil]
 Trace Width = 0.076mm [3mil]
 Differential gap = 0.127mm [5mil]

INTERNAL

Er (FR408 or RT4xxx) = 3.6
 Dielectric Thickness = 0.10mm [3.9mil]
 Copper Thickness (1/2oz) = 0.018mm [0.7mil]
 Trace Width = 0.076mm [3mil]
 Differential gap = 0.08mm [3.1mil]

50-ohm single-ended microstrip (everything else)

EXTERNAL

Er (FR408 or RT4xxx) = 3.6
 Dielectric Thickness = 0.10mm [3.9mil]
 Copper Thickness (1oz outer) = 0.036mm [1.4mil]
 Trace Width = 0.17mm [6.7mil]

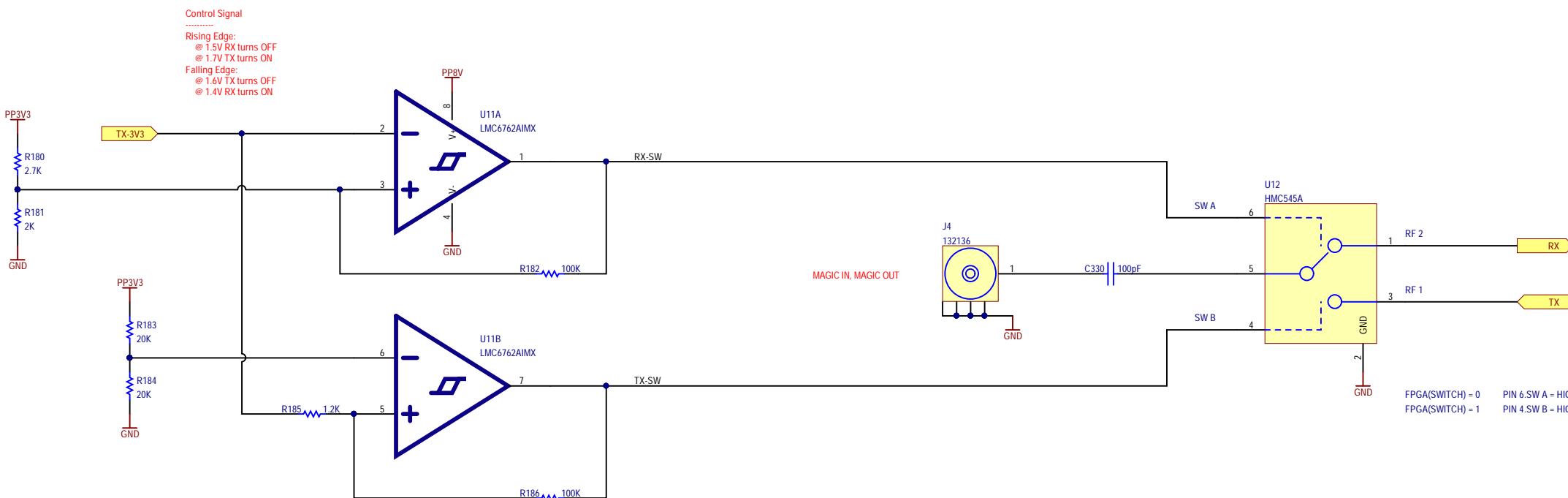
INTERNAL

Er (FR408 or RT4xxx) = 3.6
 Dielectric Thickness = 0.10mm [3.9 mil]
 Copper Thickness (1/2oz) = 0.018mm [0.7mil]
 Trace Width = 0.14mm [5.5mil]



Title		
RF Front End		
Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	J. Brinton
Revision 1	Sheet 47 of 58	Date 3/12/2017

A



B

C

D

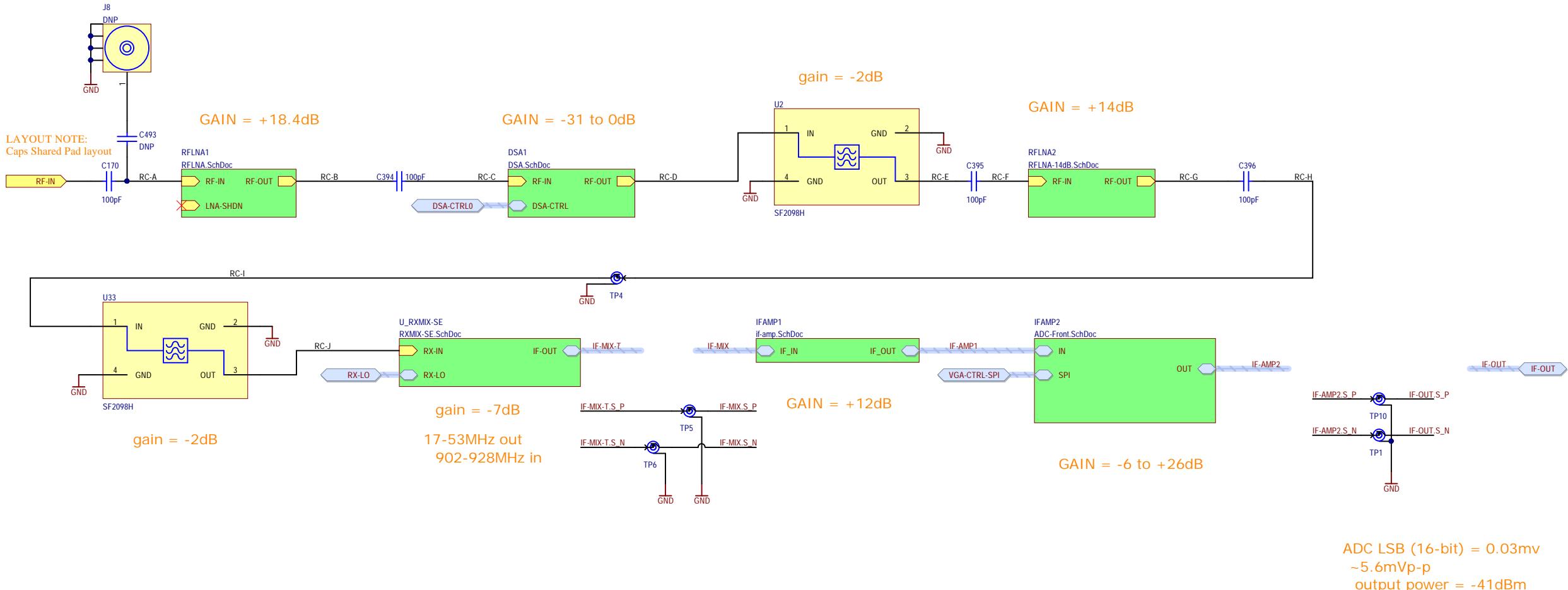
A

B

C

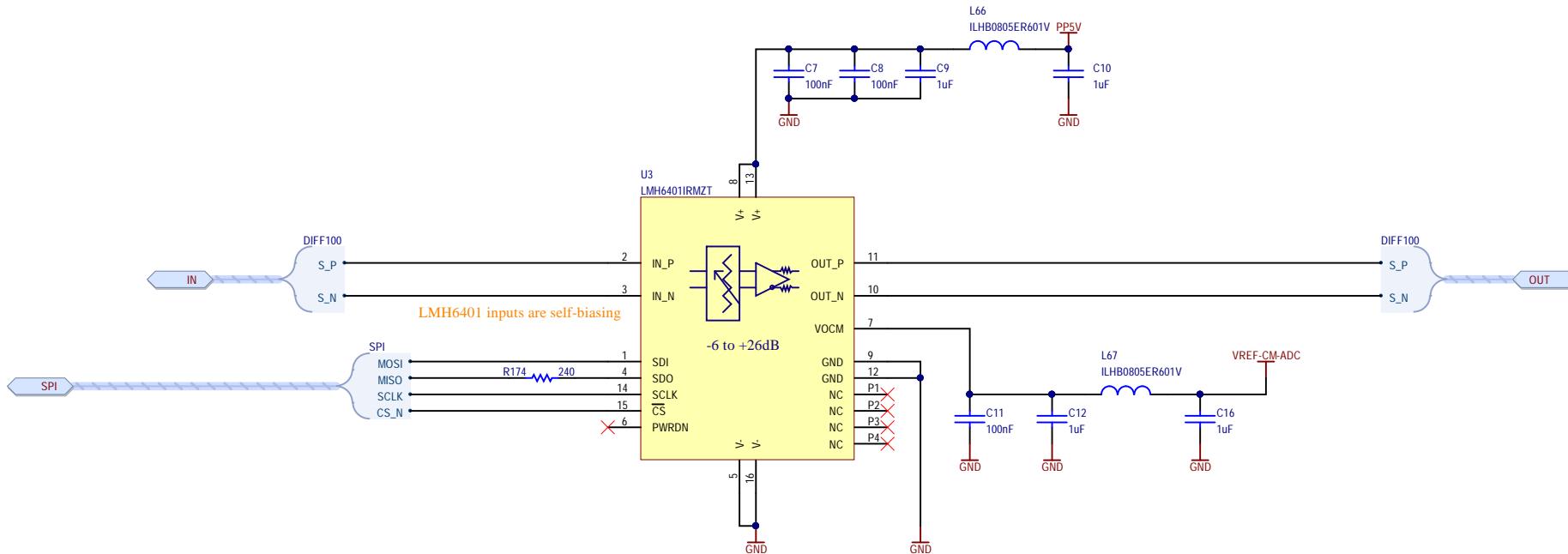
D

noise floor power @ 26MHz BW = -100dBm
loudest received signal - 16dBm



A

A



A

B

C

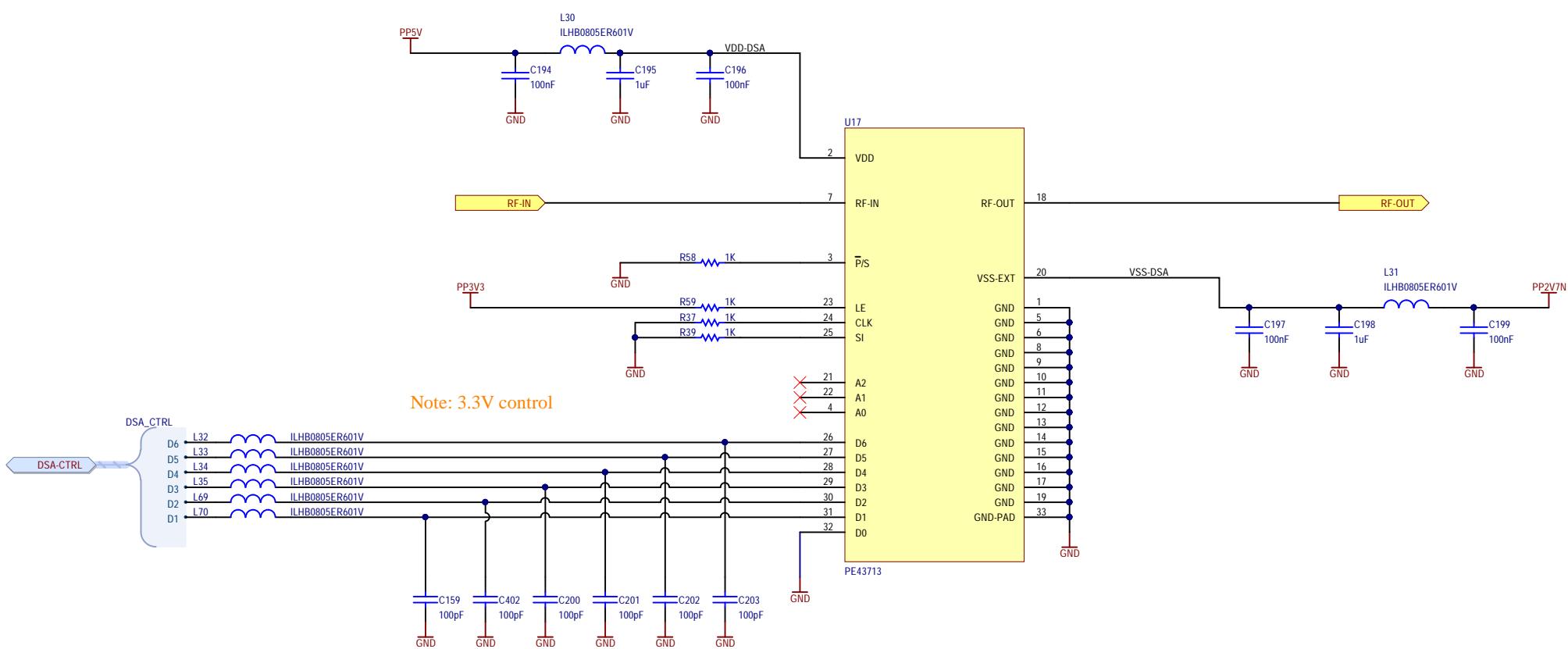
D

A

B

C

D



3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siglabs.com

Title		
DSA		
Engineer	Drawn By	Checked By
J. Brinton	J. Brinton	J. Brinton
Revision 1	Sheet 51 of 58	Date 3/12/2017

A

A

B

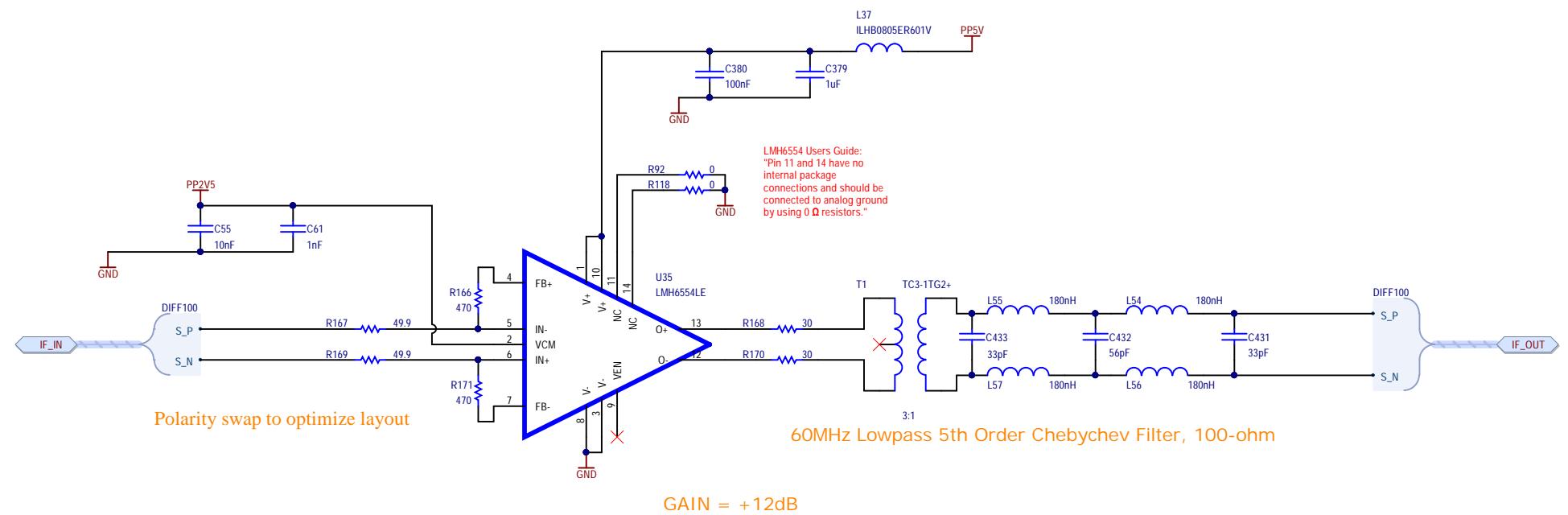
B

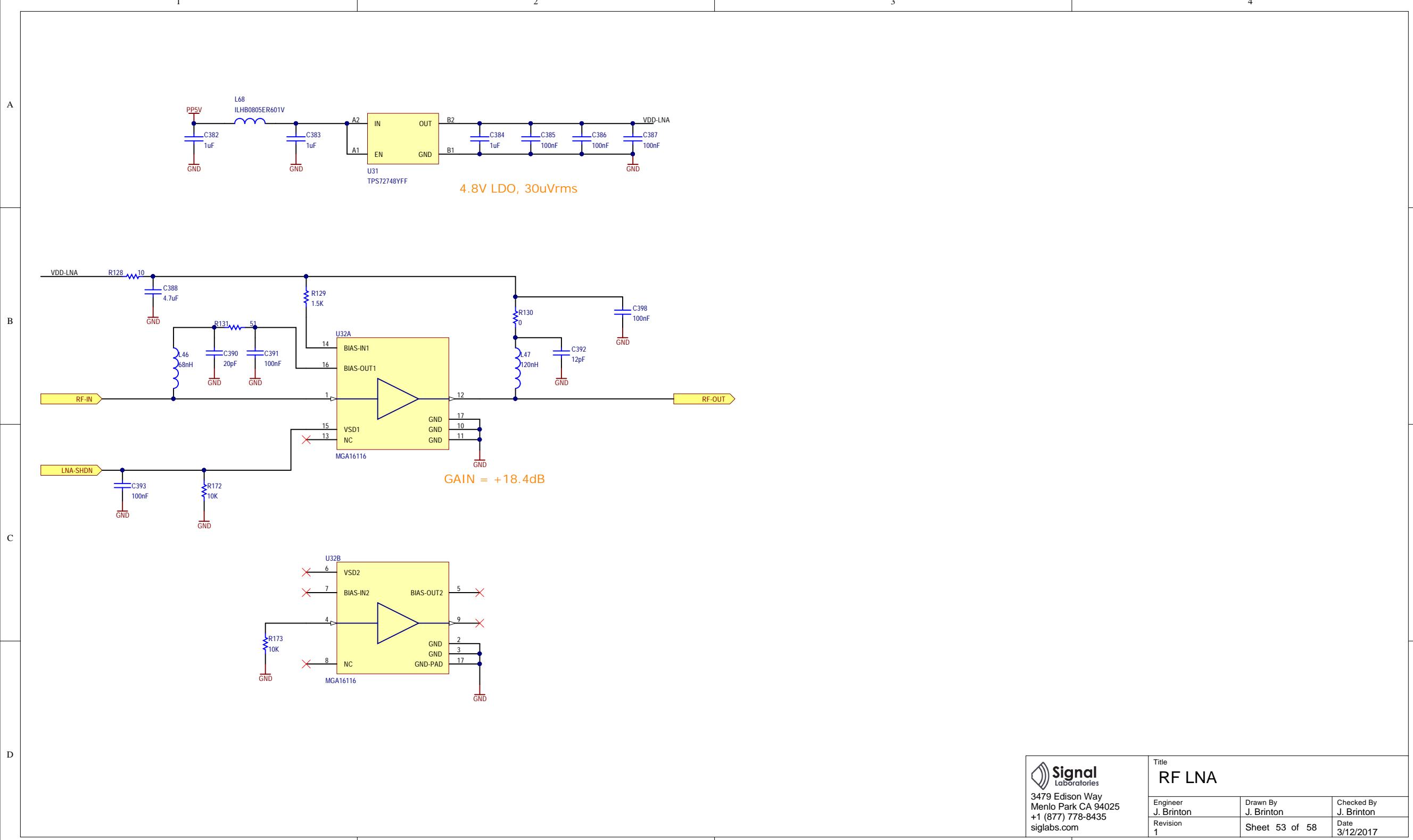
C

C

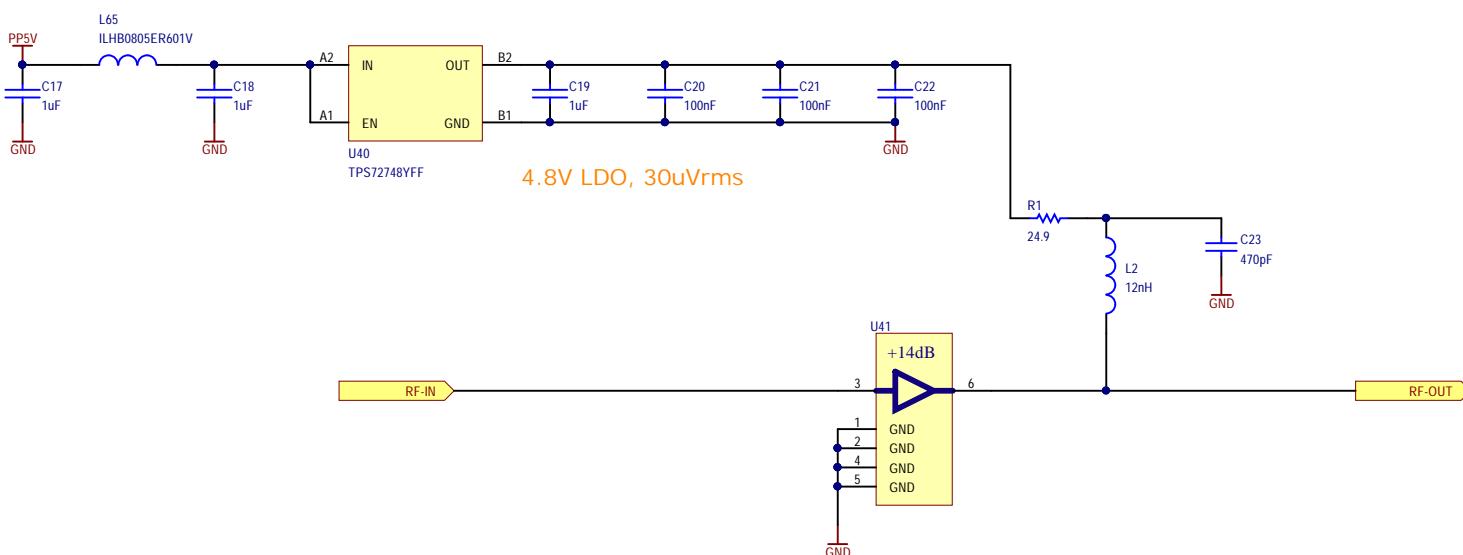
D

D





A



B

C

D

A

B

C

D

target LO = 0dBm
actual = -3 to -2dBm

LVDS Differential-ended:

$$V_{diff_{pp}} = 0.8V,$$

$$V_{diff} = 0.5 \times V_{pp} = 0.4V,$$

$$RMS \approx 0.9,$$

$$P = \frac{(RMS \times V_{diff})^2}{R},$$

$$P = \frac{(0.9 \times 0.4V)^2}{100} = 1.3mW = 1dBm.$$

LVDS Single-ended:

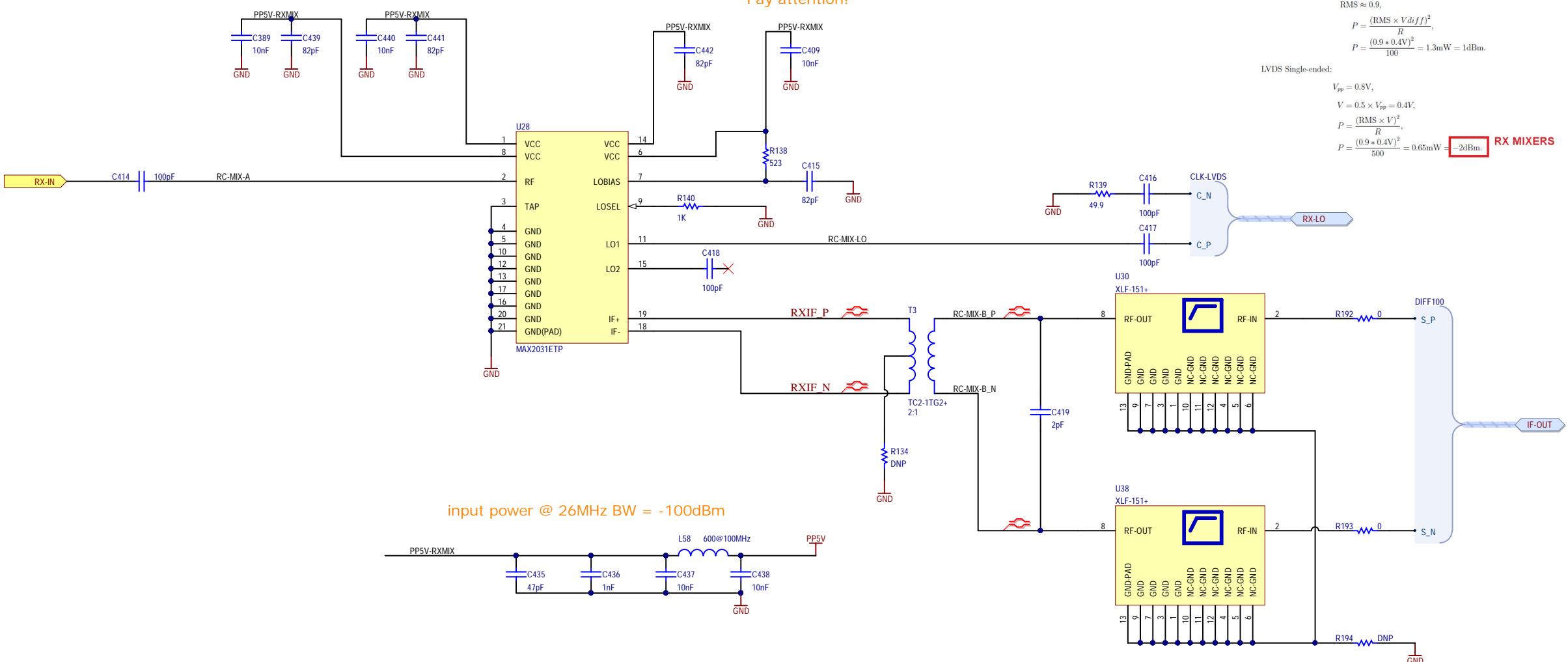
$$V_{pp} = 0.8V,$$

$$V = 0.5 \times V_{pp} = 0.4V,$$

$$P = \frac{(RMS \times V)^2}{R},$$

$$P = \frac{(0.9 \times 0.4V)^2}{500} = 0.65mW = -2dBm.$$

RX MIXERS



target LO = 0dBm, actual = 3-4dBm

LVPECL33 Differential-ended:

$$V_{diff,pp} = 1.6V,$$

$$V_{diff} = 0.5 \times V_{pp} = 0.8V,$$

RMS ≈ 0.9 ,

$$P = \frac{(RMS \times V_{diff})^2}{R},$$

$$P = \frac{(0.9 \times 0.8V)^2}{100} = 5mW = 7dBm.$$

LVPECL33 Single-ended:

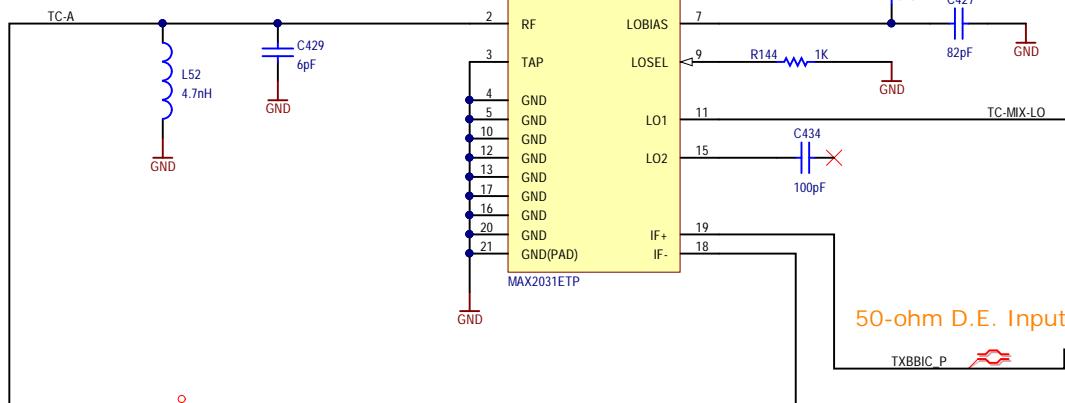
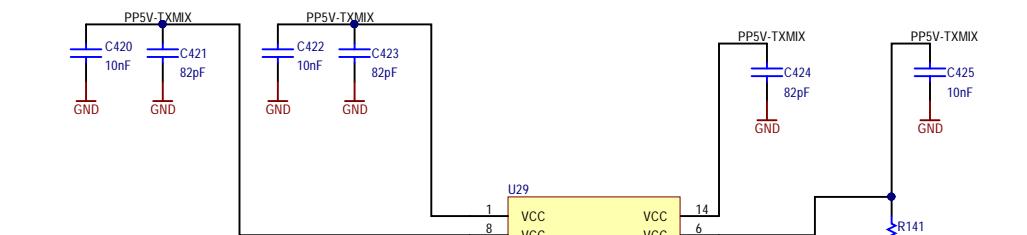
$$V_{pp} = 0.8V,$$

$$V = 0.5 \times V_{pp} = 0.4V,$$

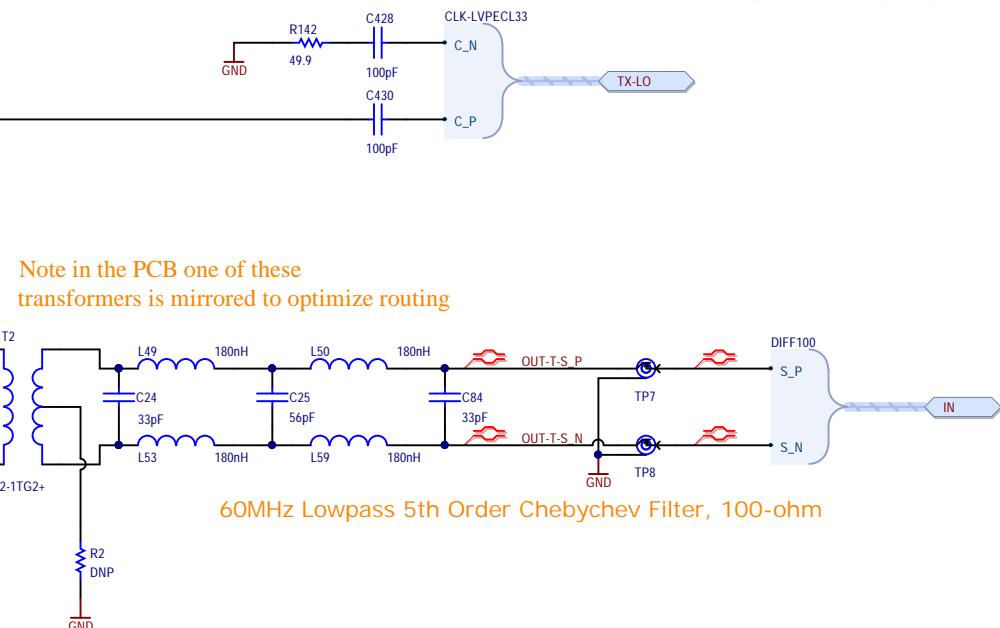
$$P = \frac{(RMS \times V)^2}{R},$$

$$P = \frac{(0.9 \times 0.4V)^2}{500} = 2.5mW = 4dBm. \quad \text{TX MIXERS}$$

LAYOUT NOTE:
Different VCC pins have different decoupling
Pay attention!



Note in the PCB one of these
transformers is mirrored to optimize routing



A

A

B

B

C

C

D

D

1

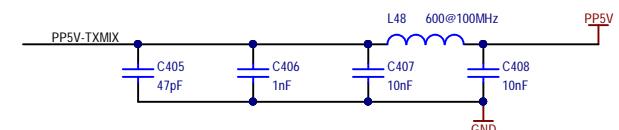
2

3

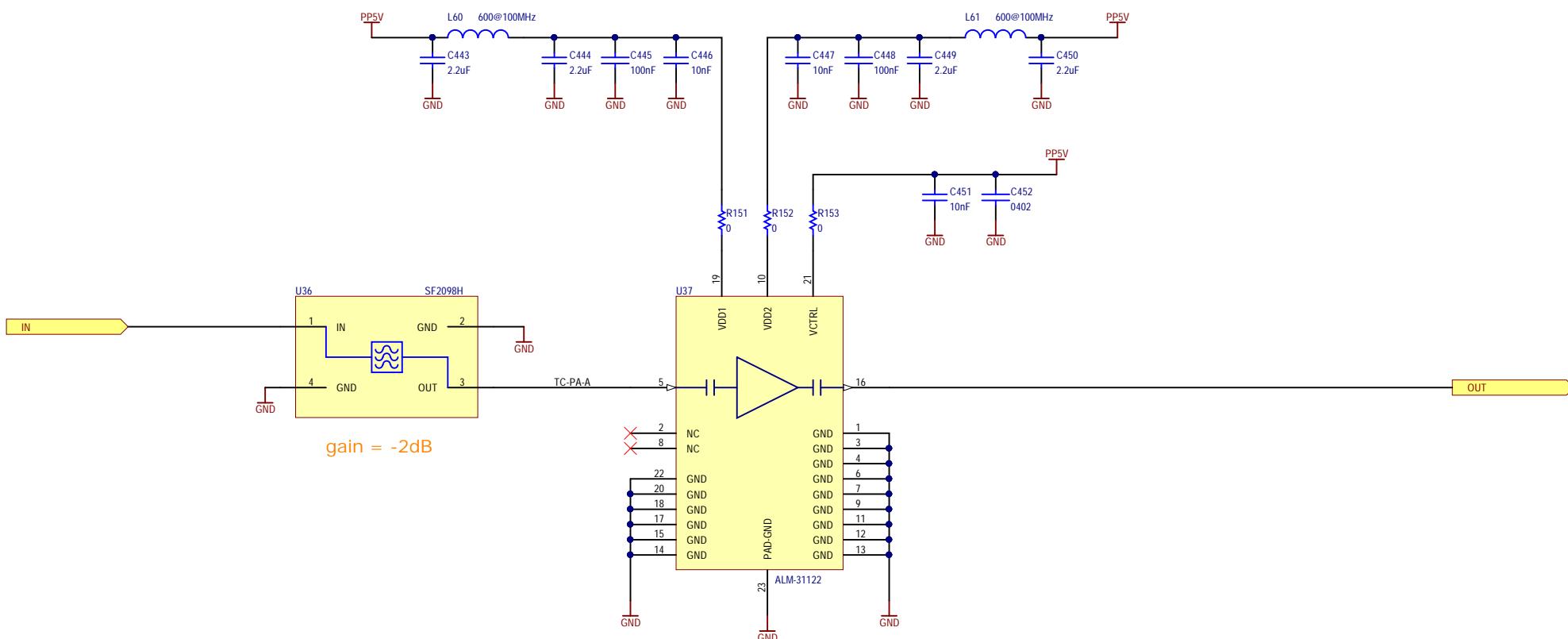
4

GAIN = 13.5dB

GAIN = +20dB



input power @ 26MHz BW = -100dBm



3479 Edison Way
Menlo Park CA 94025
+1 (877) 778-8435
siglabs.com

<p>Title Transmitter PA #1</p>		
Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 1	Sheet 57 of 58	Date 3/12/2017

A

A

B

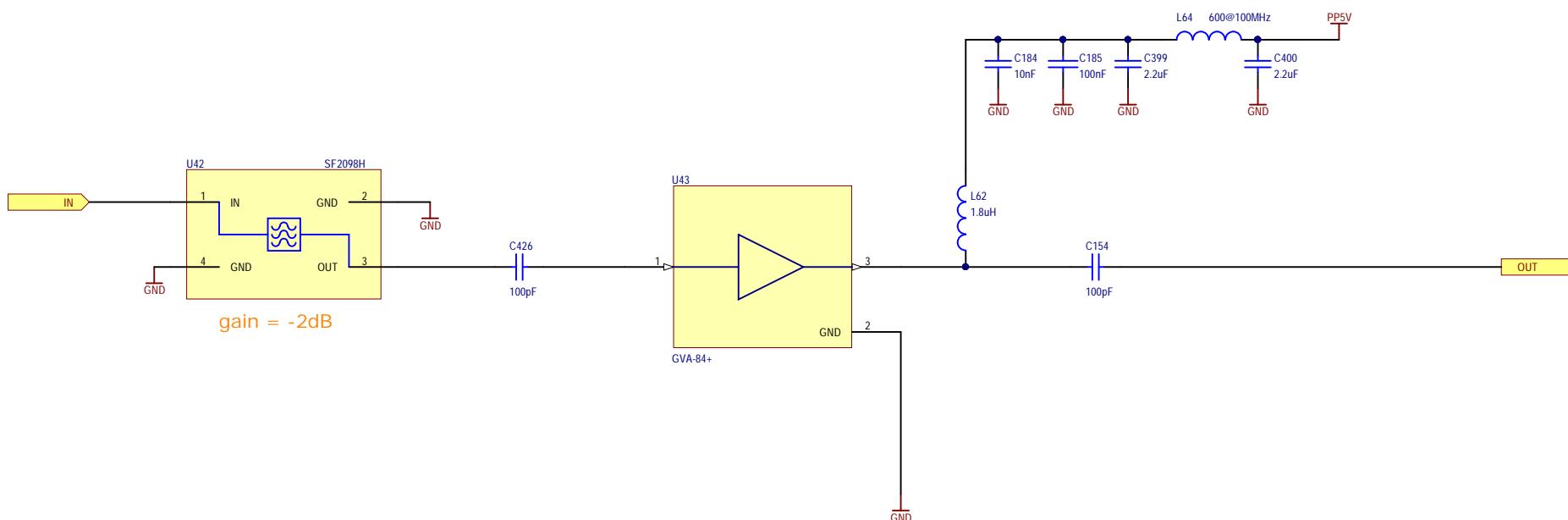
B

C

C

D

D



Engineer J. Brinton	Drawn By J. Brinton	Checked By J. Brinton
Revision 1	Sheet 58 of 58	Date 3/12/2017