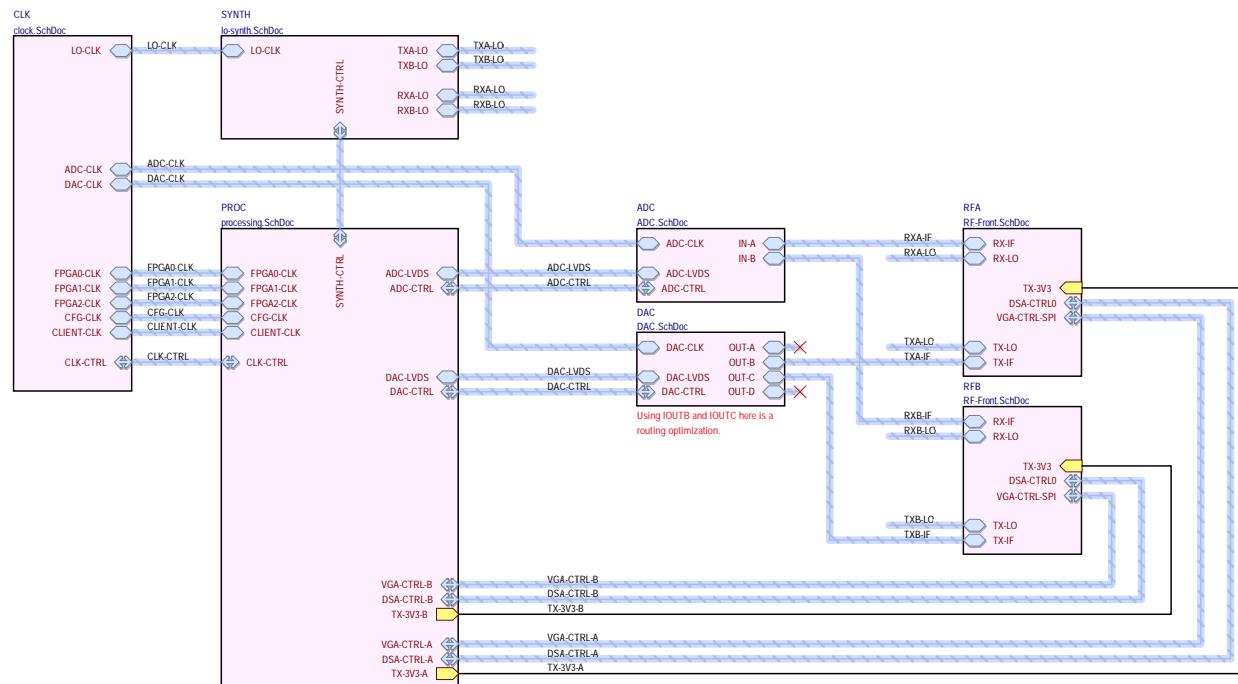


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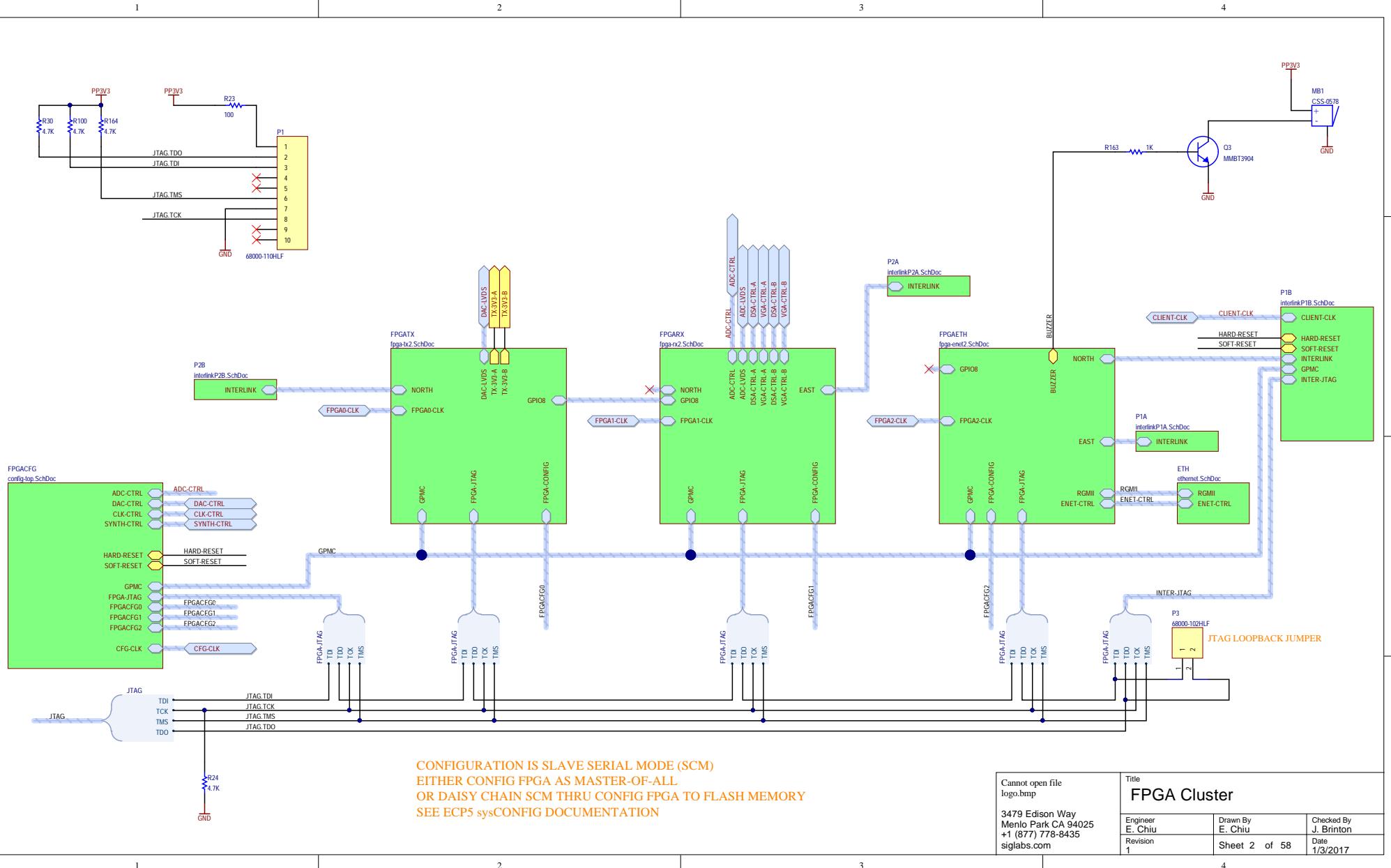
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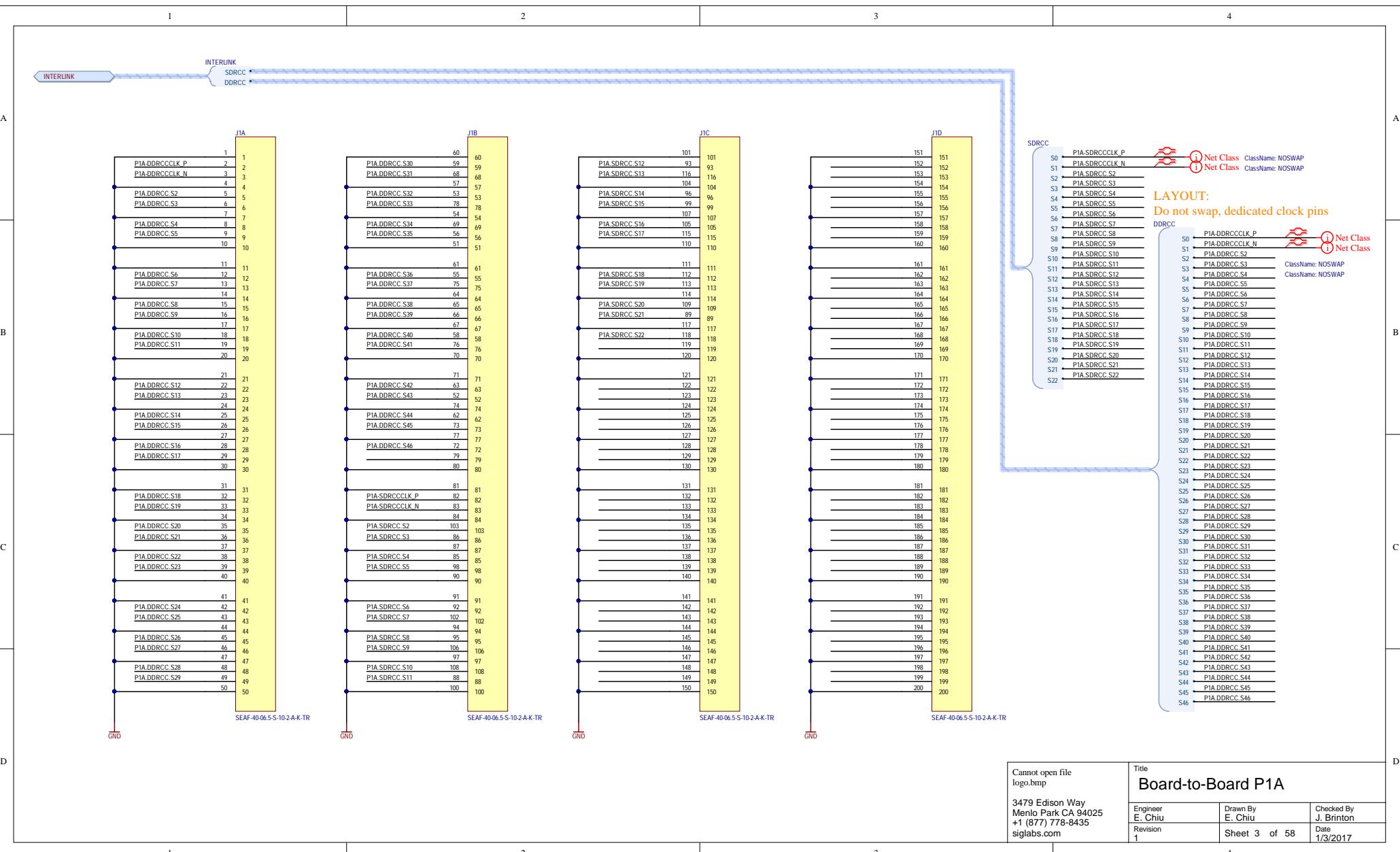
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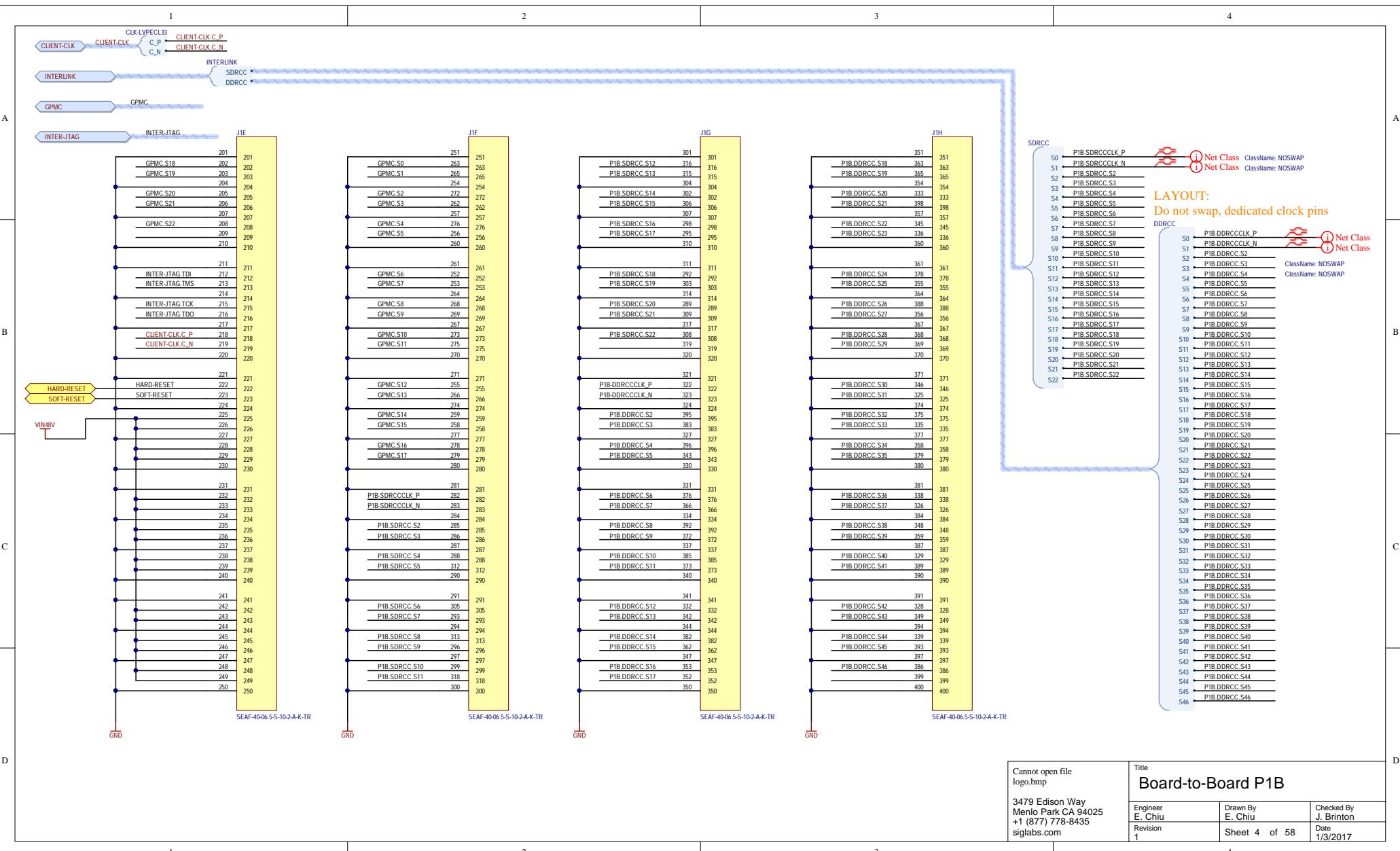
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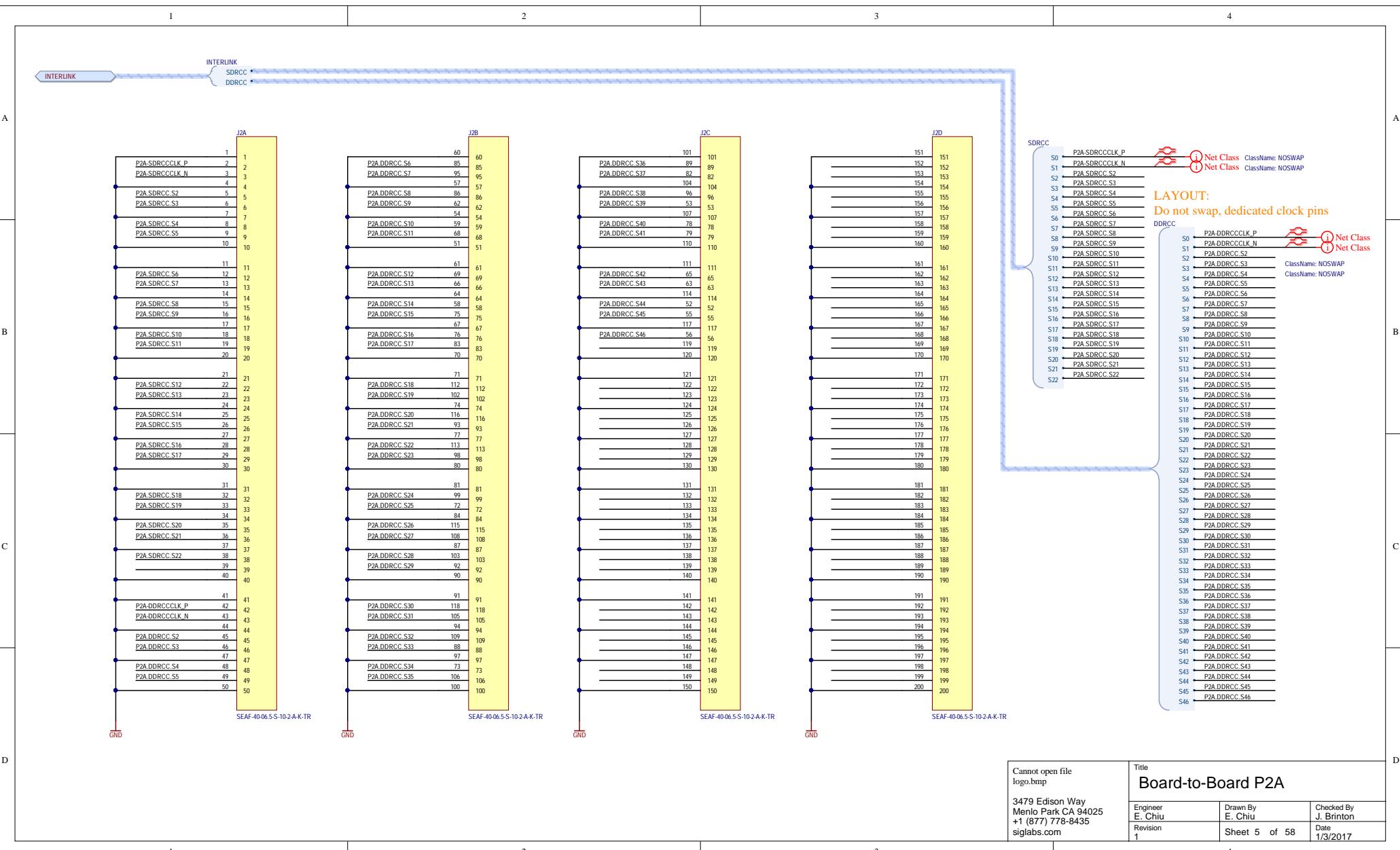
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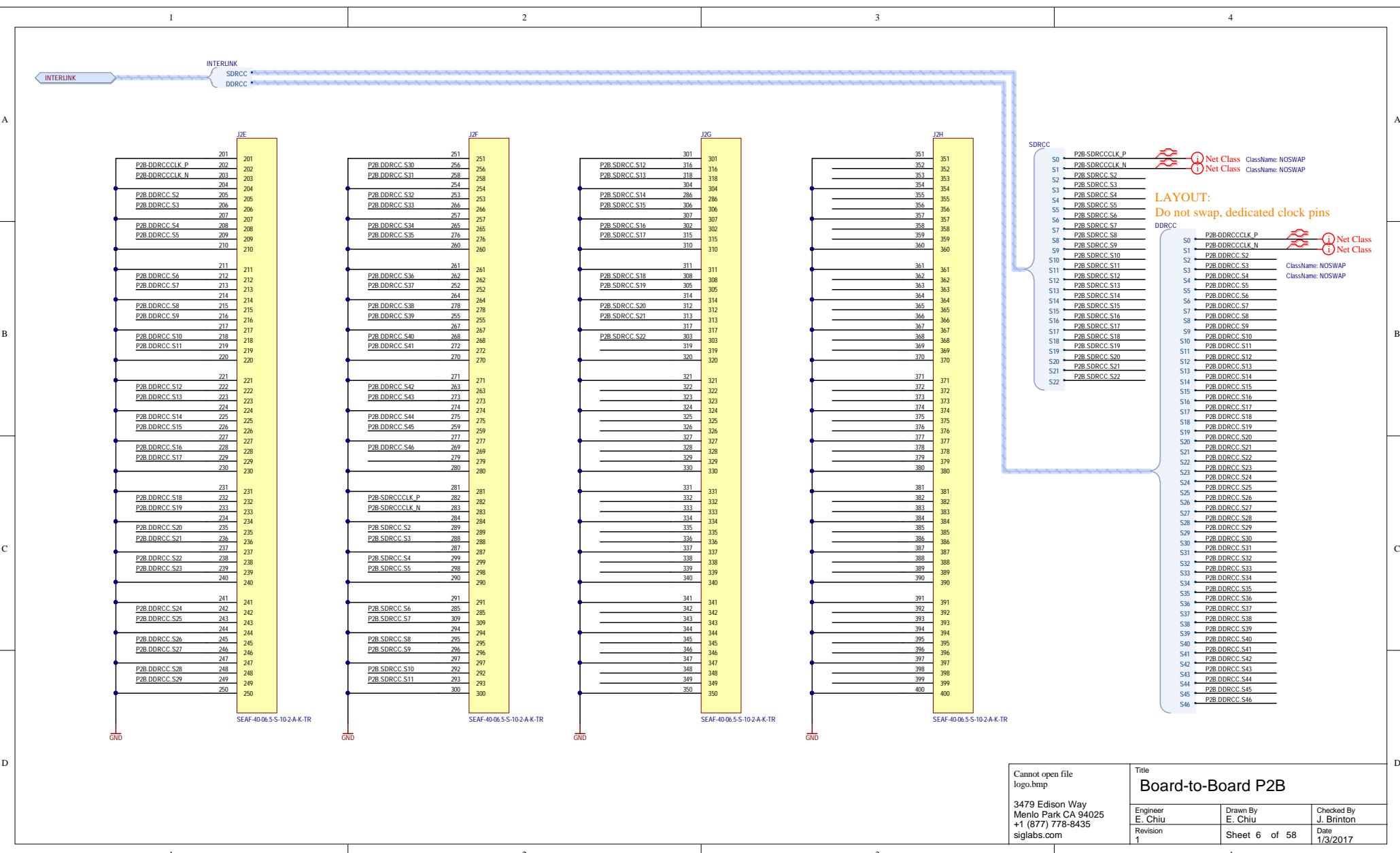
Engineer	Drawn By	Checked By
E. Chiu	E. Chiu	J. Brinton
Revision 1	Sheet 1 of 58	Date 1/3/2017

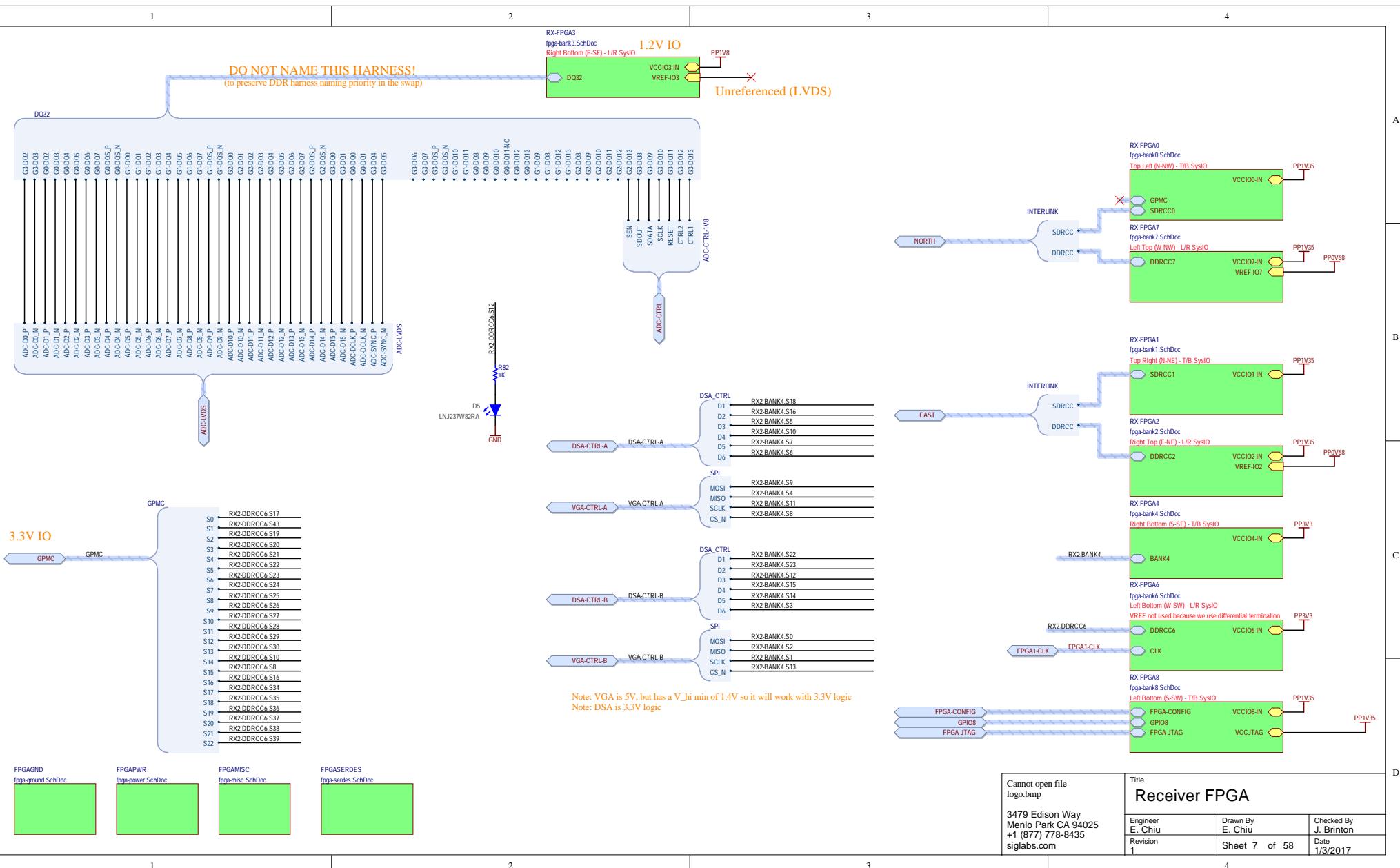


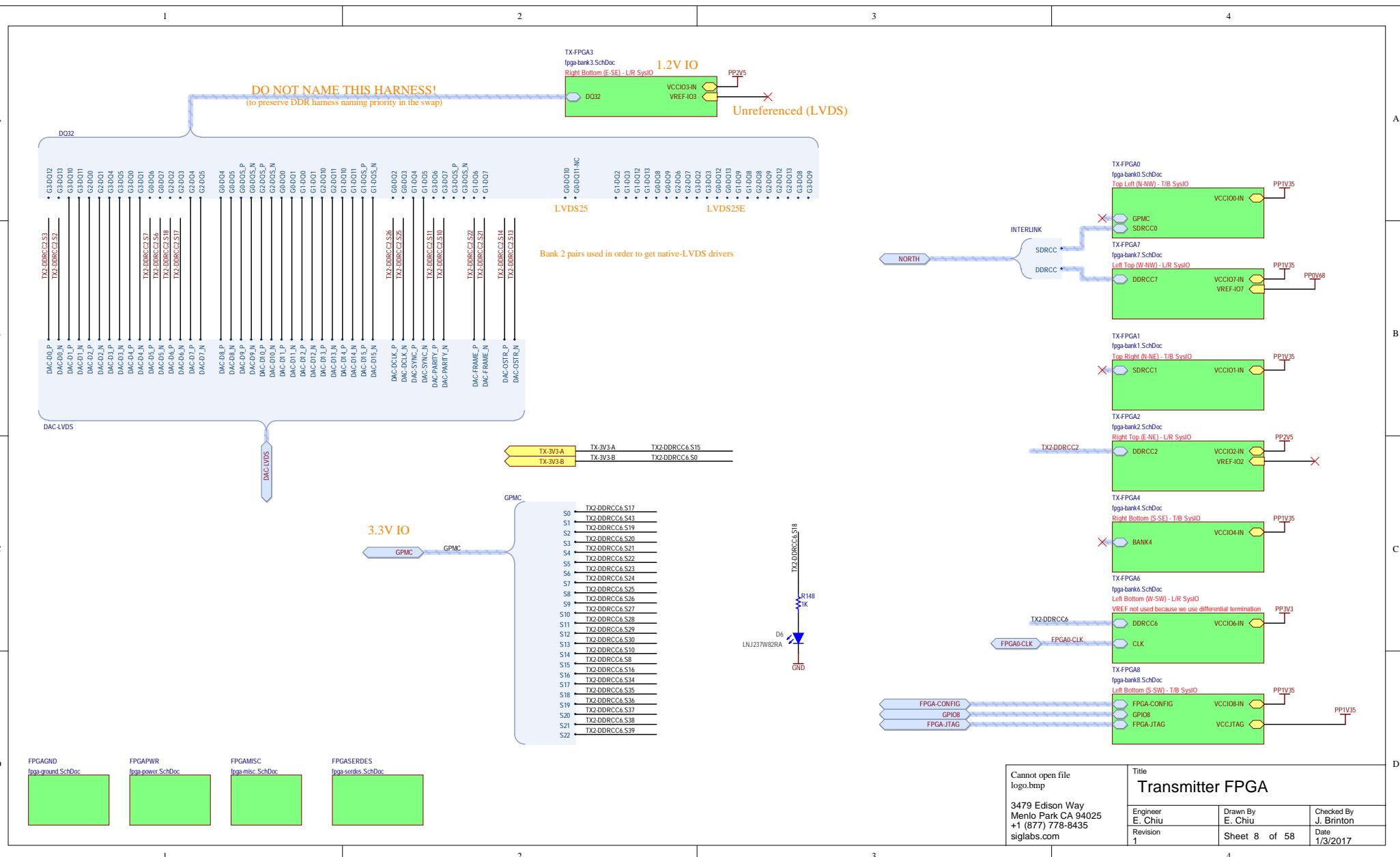


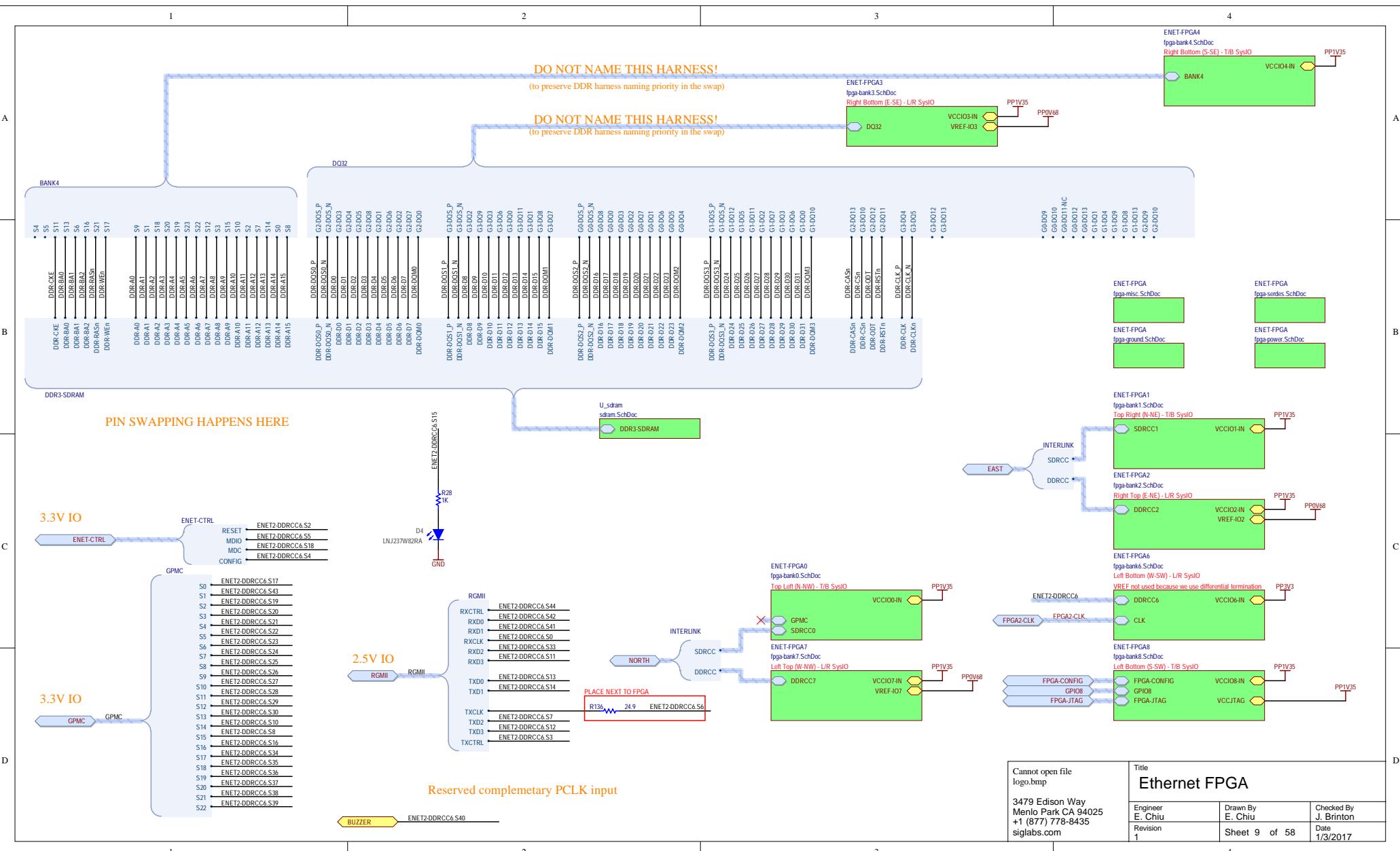




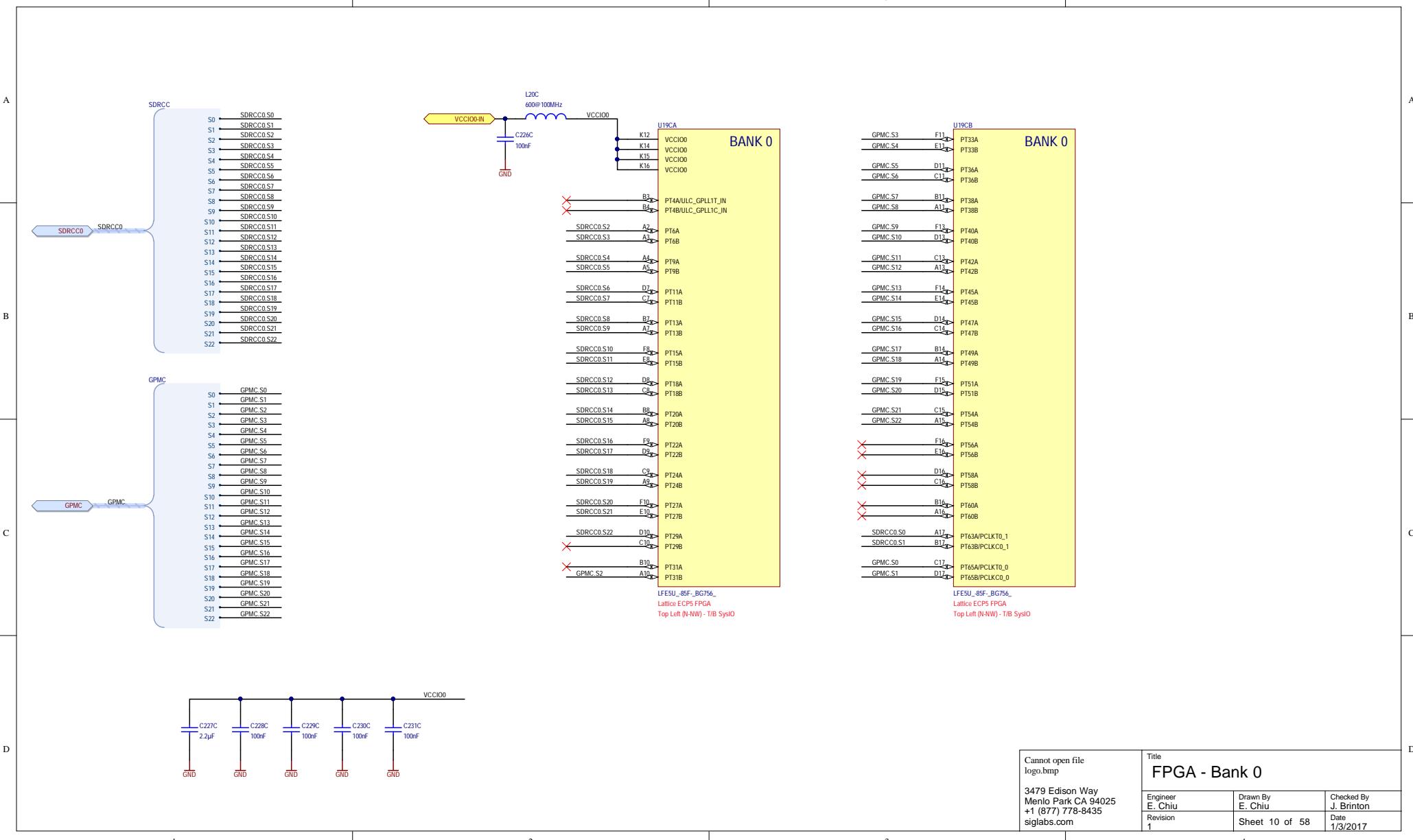






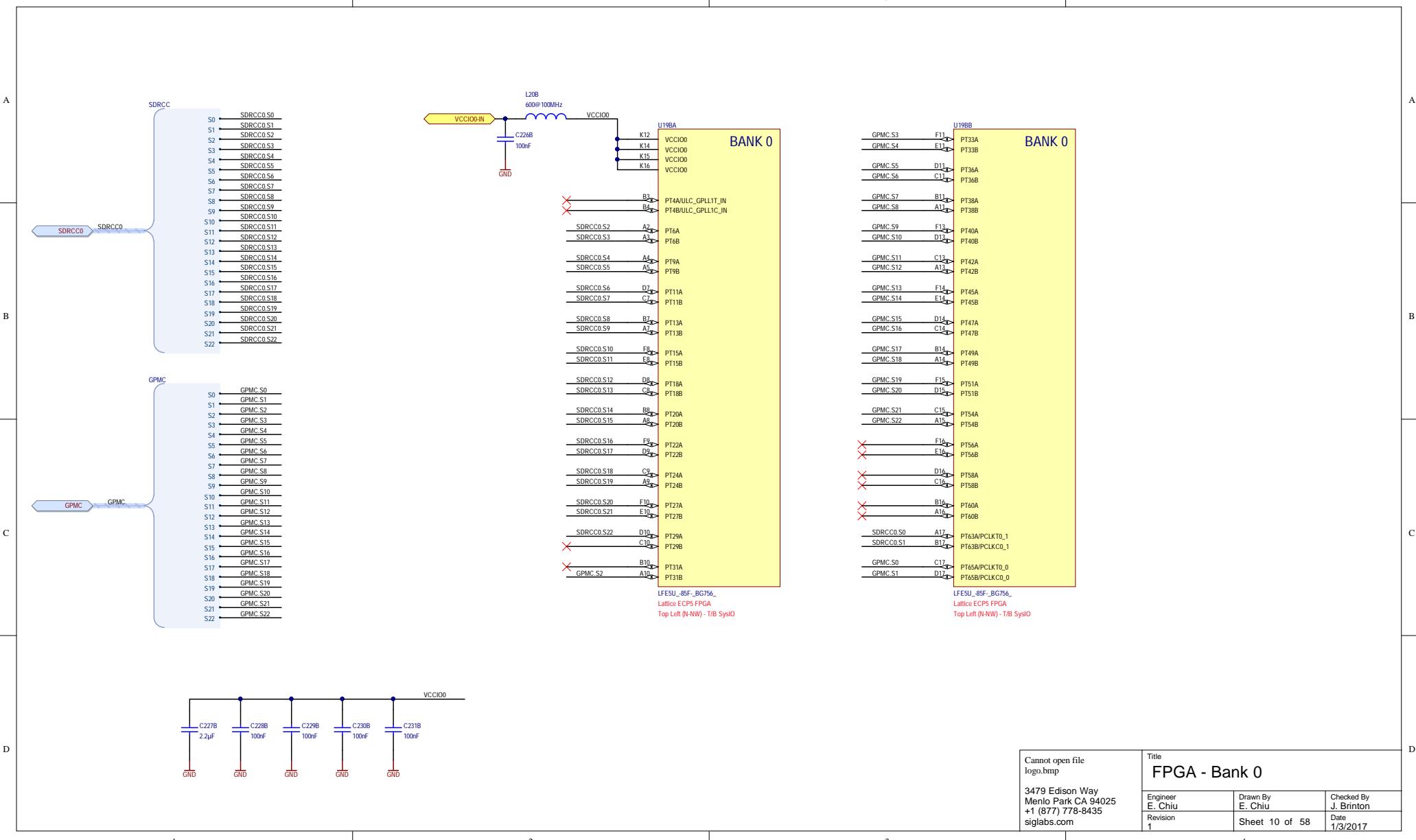


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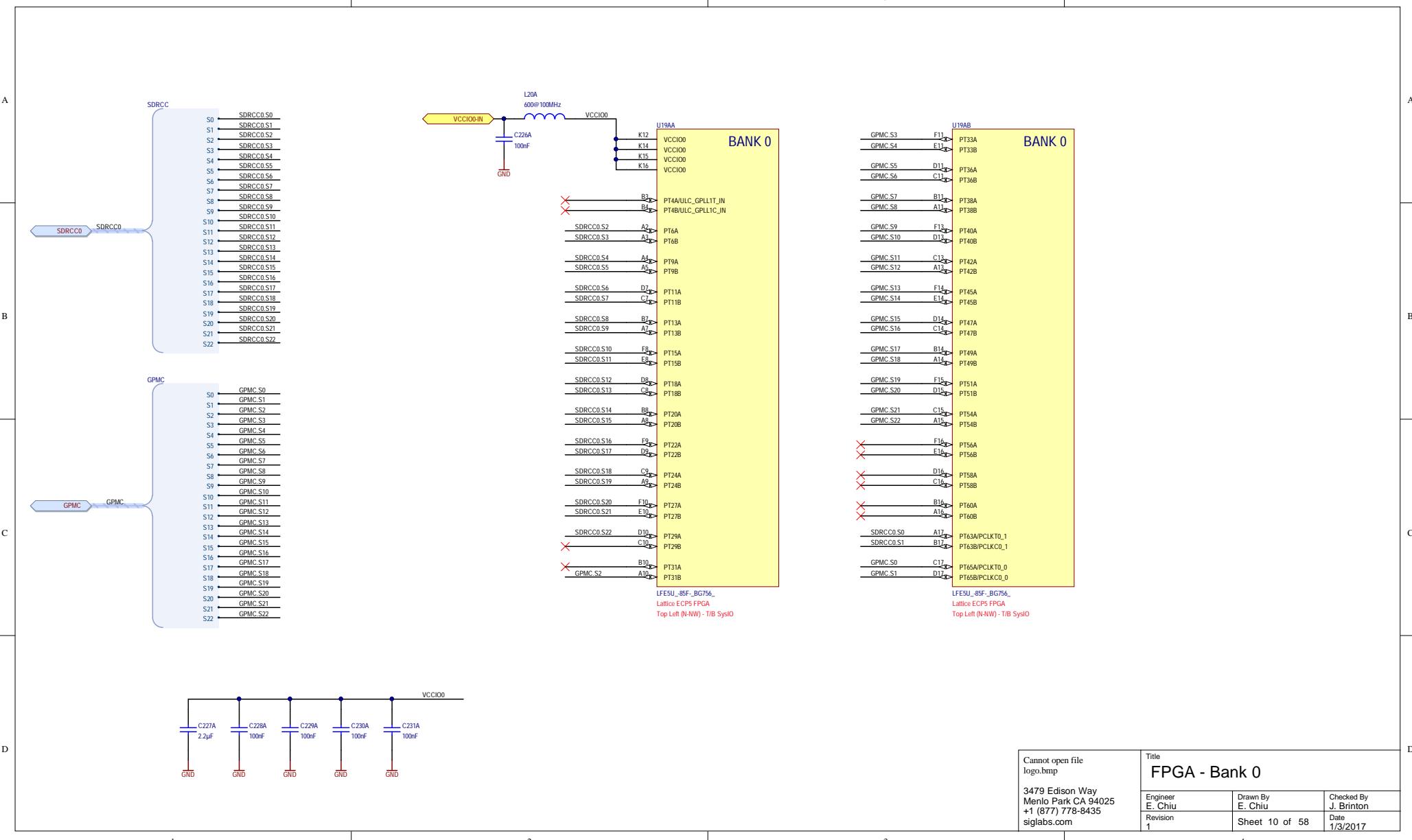
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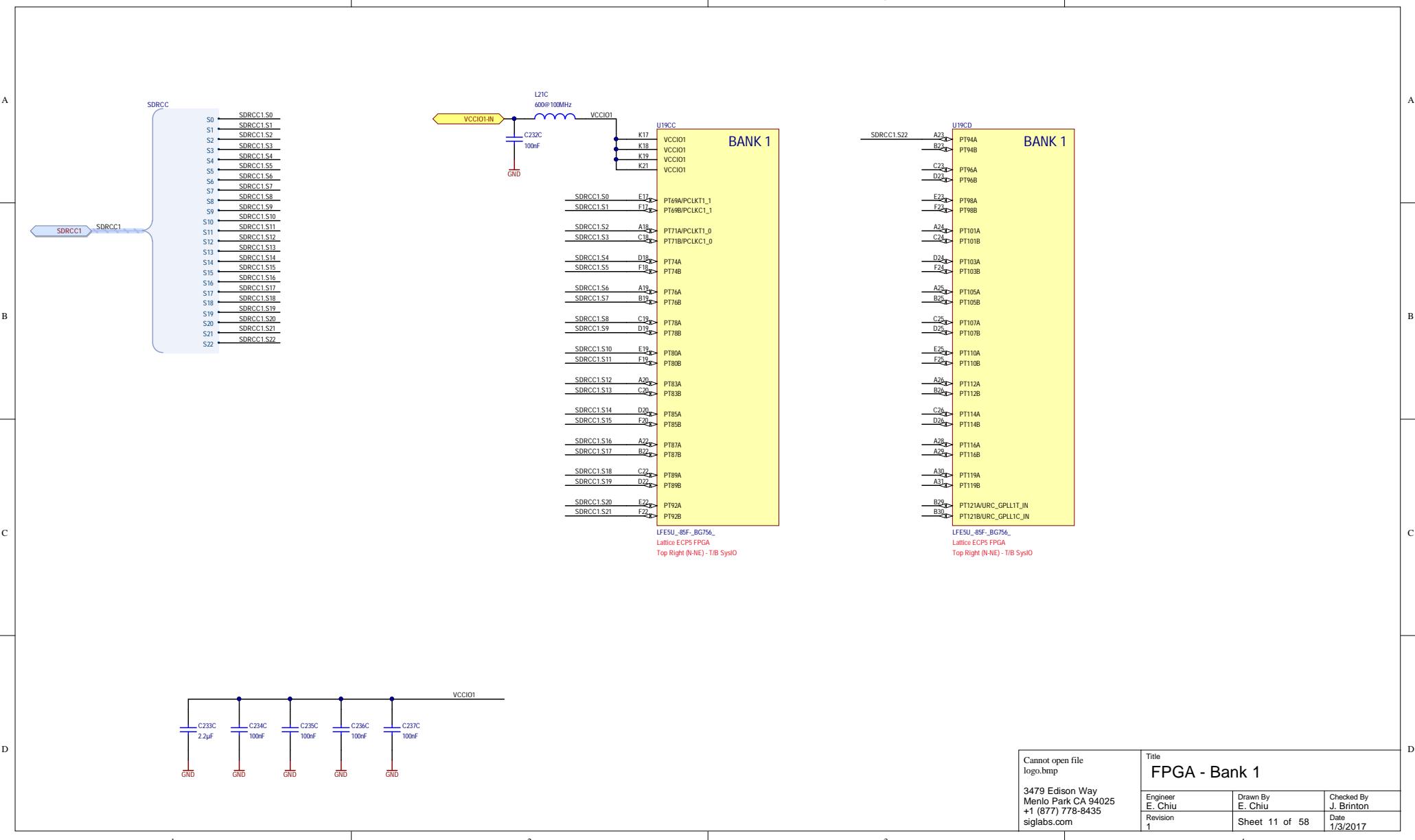


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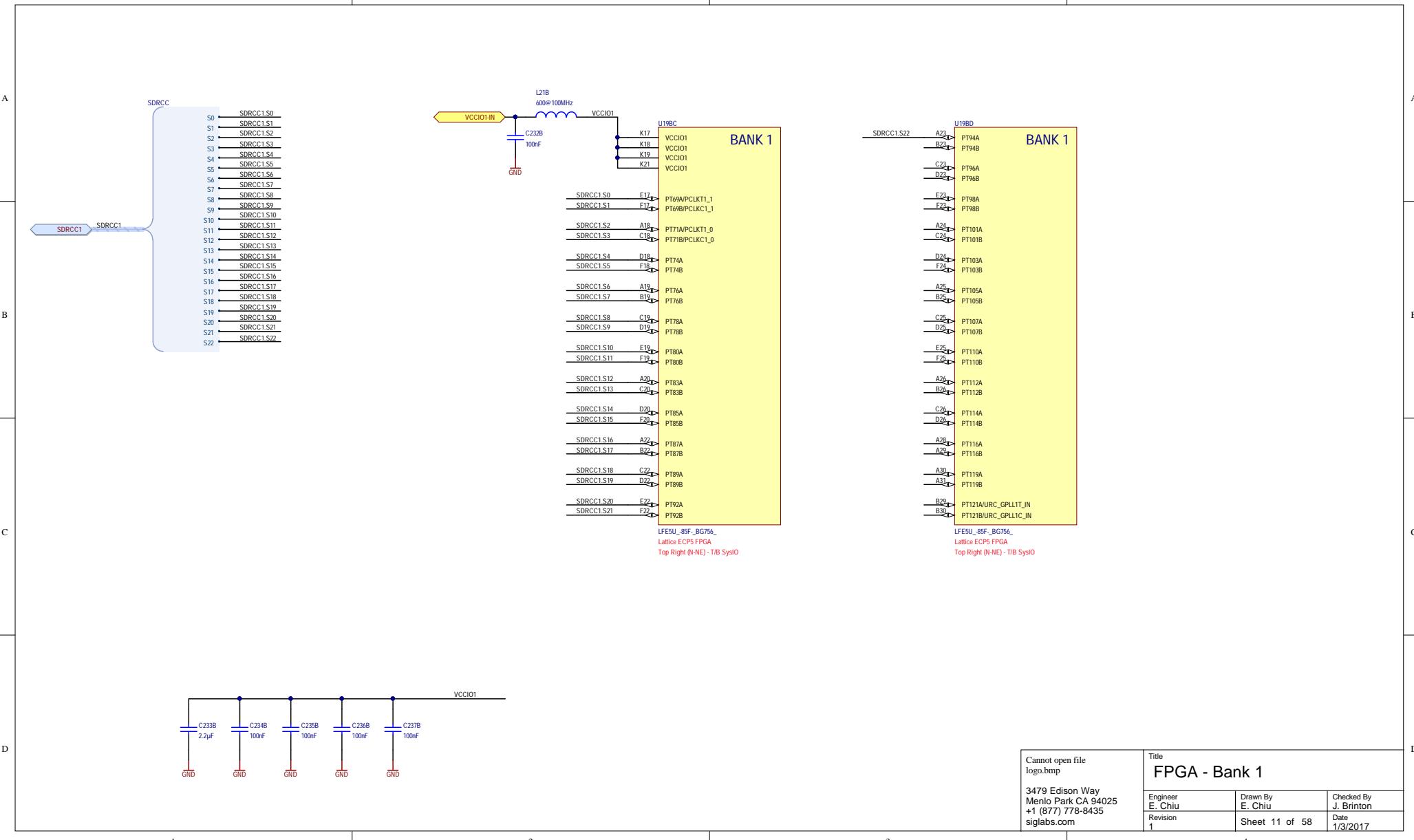


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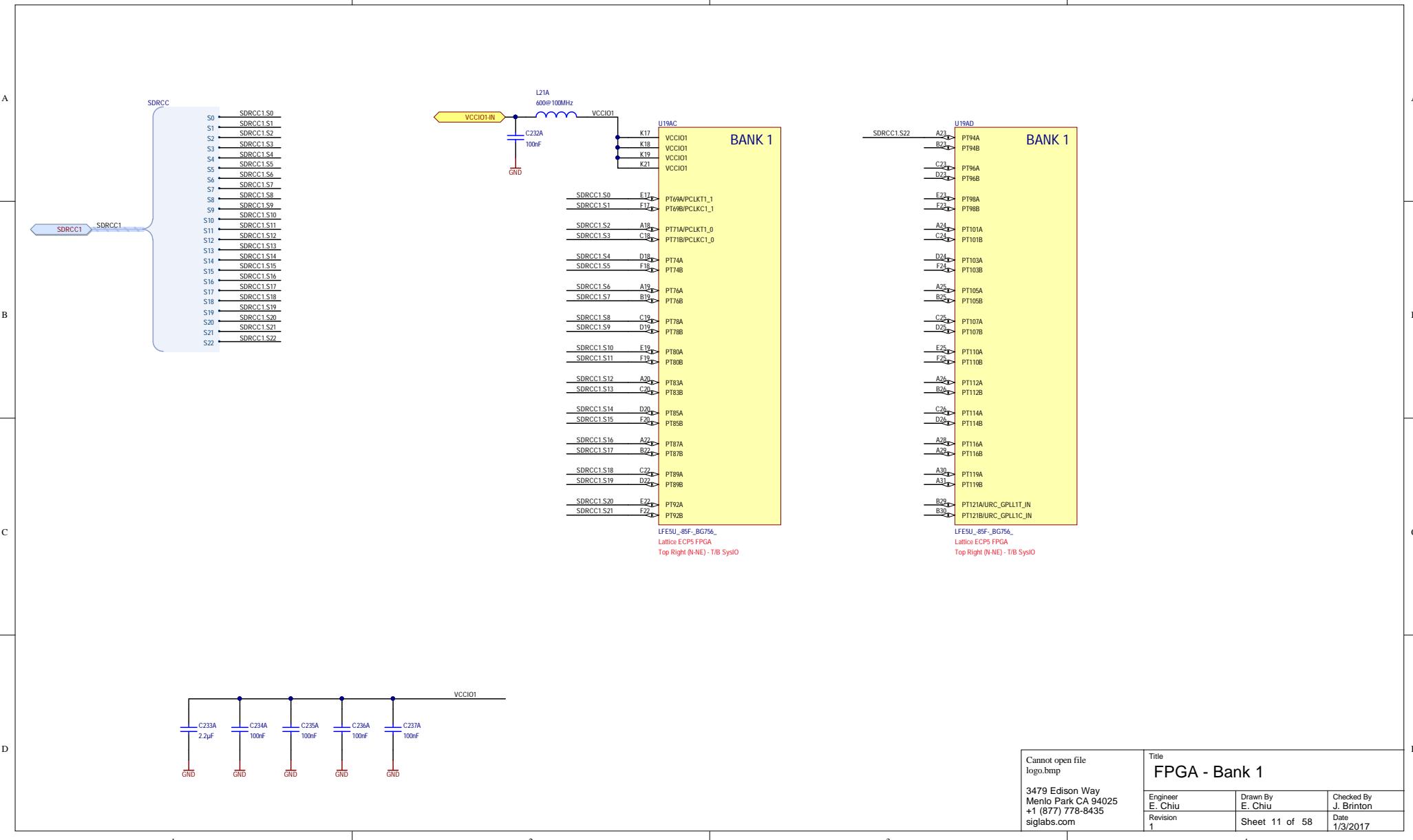
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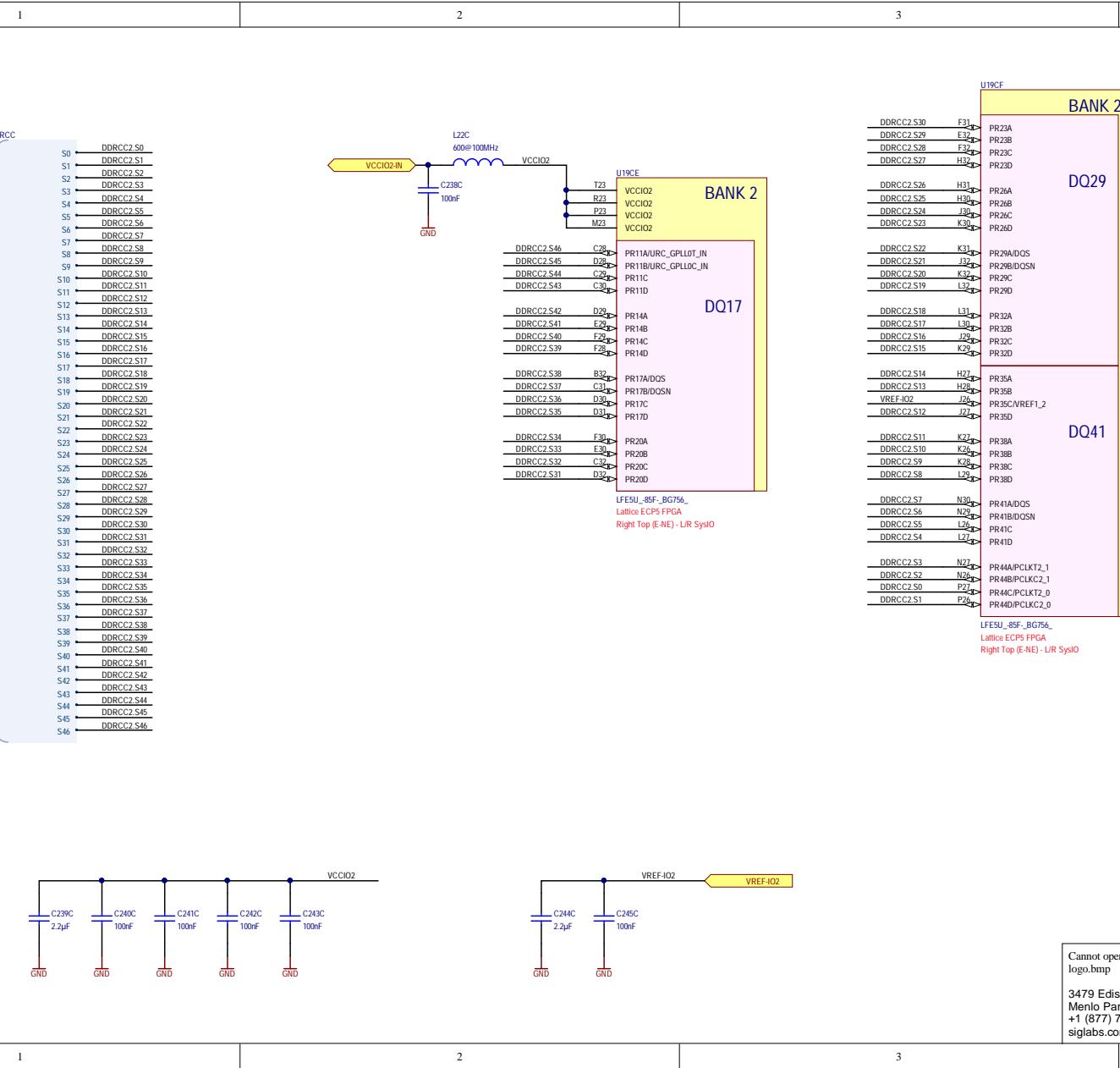


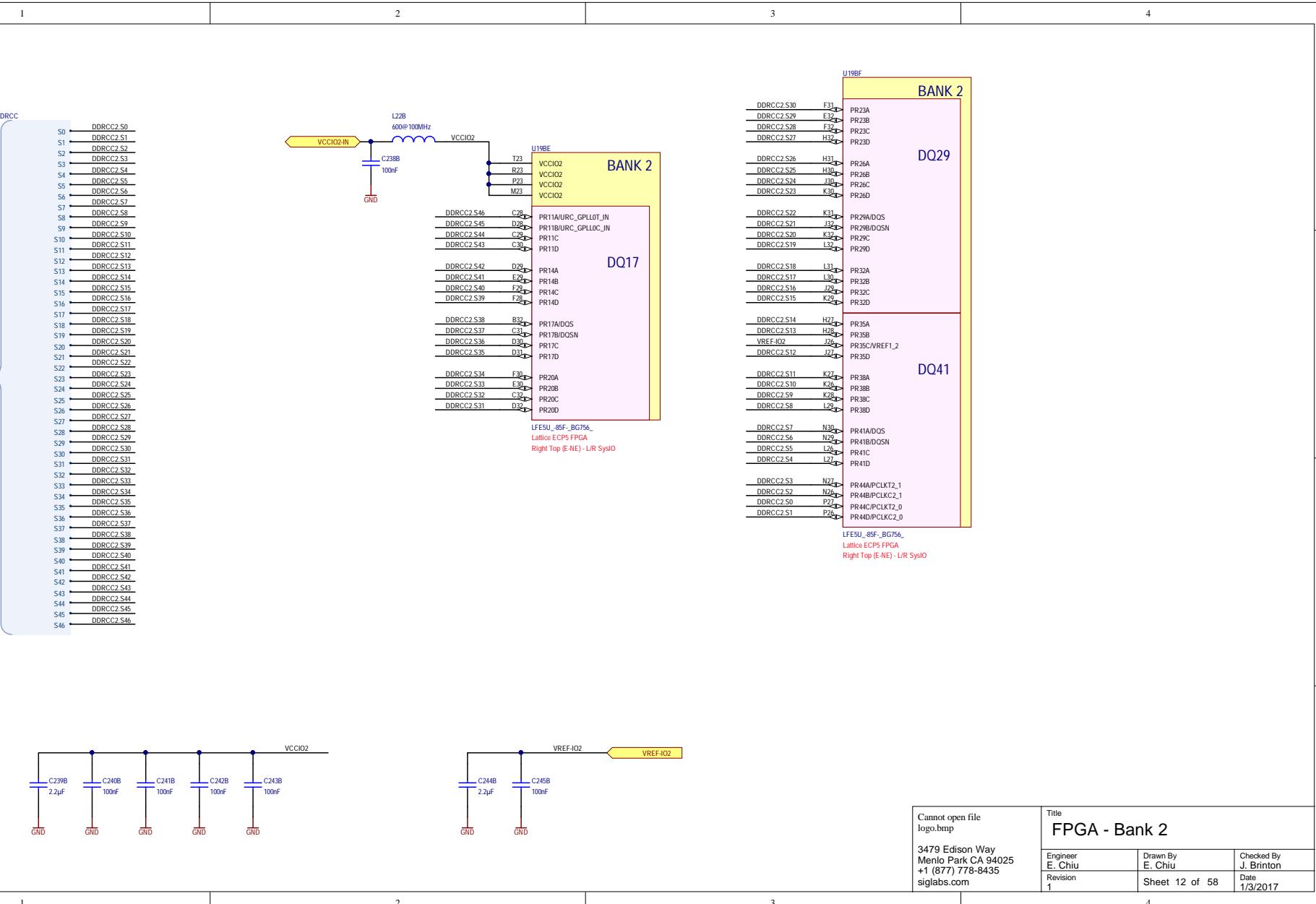
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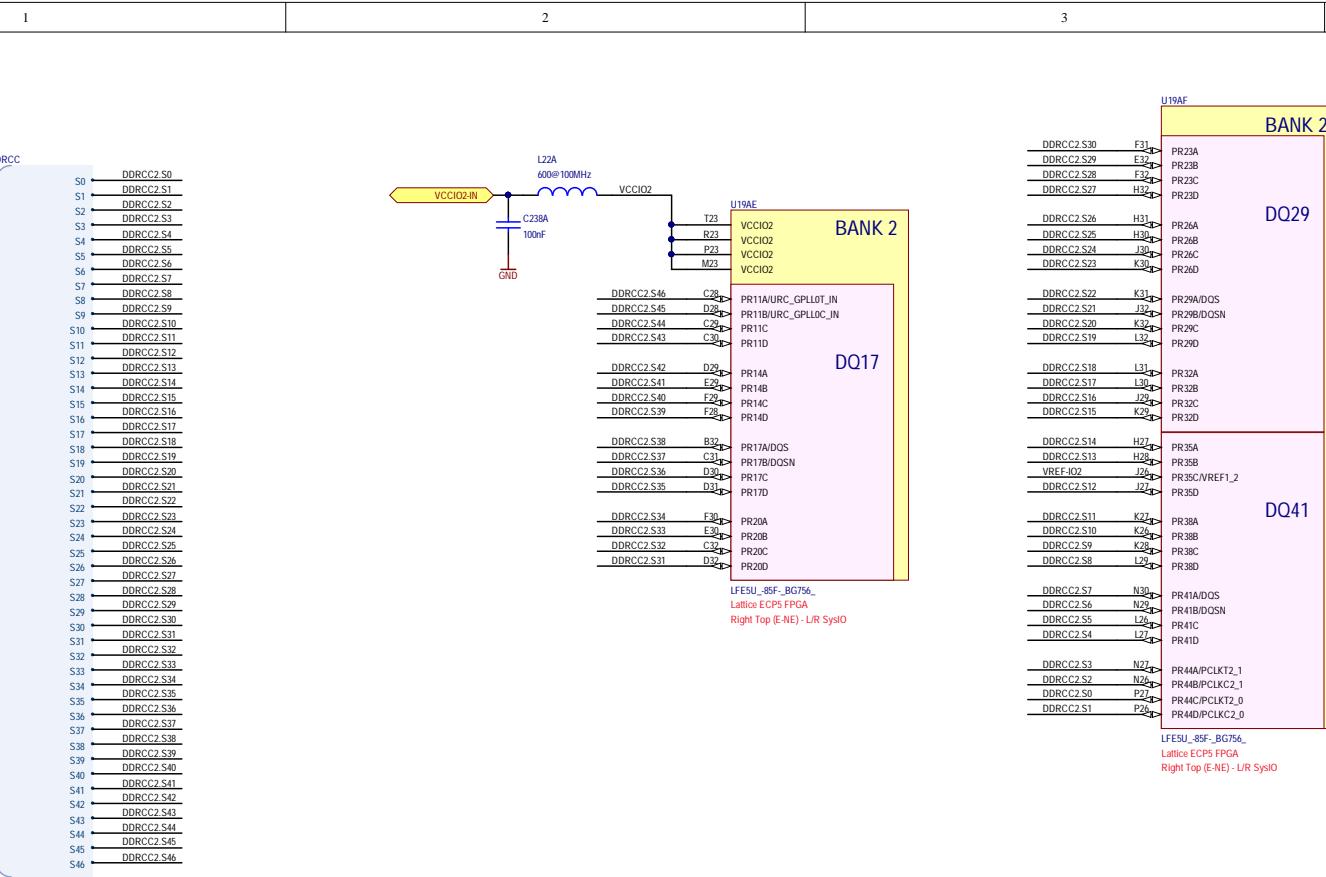
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Title
FPGA - Bank 2

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Engineer

E. Chiu

Drawn By

E. Chiu

Checked By

J. Brinton

Revision

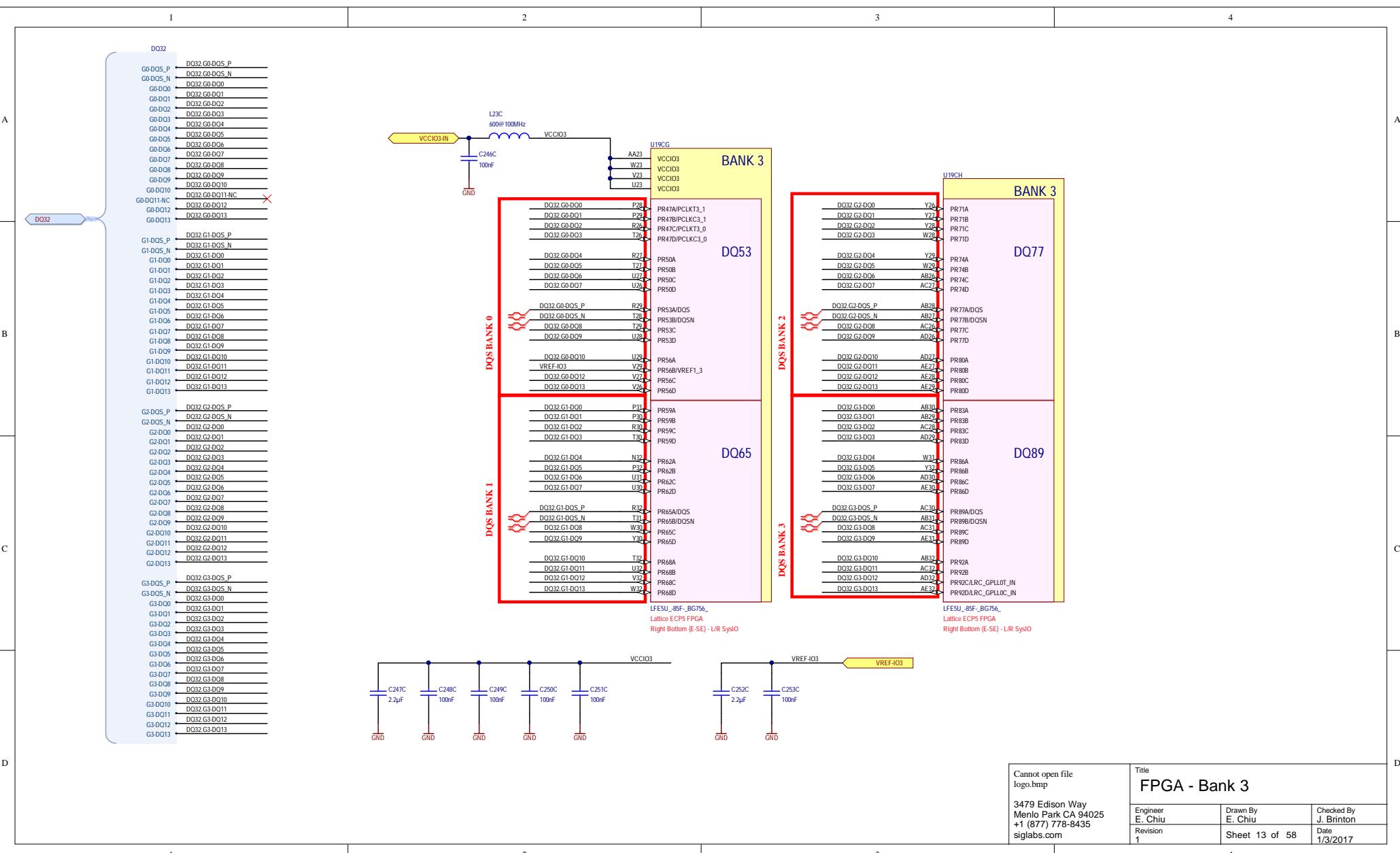
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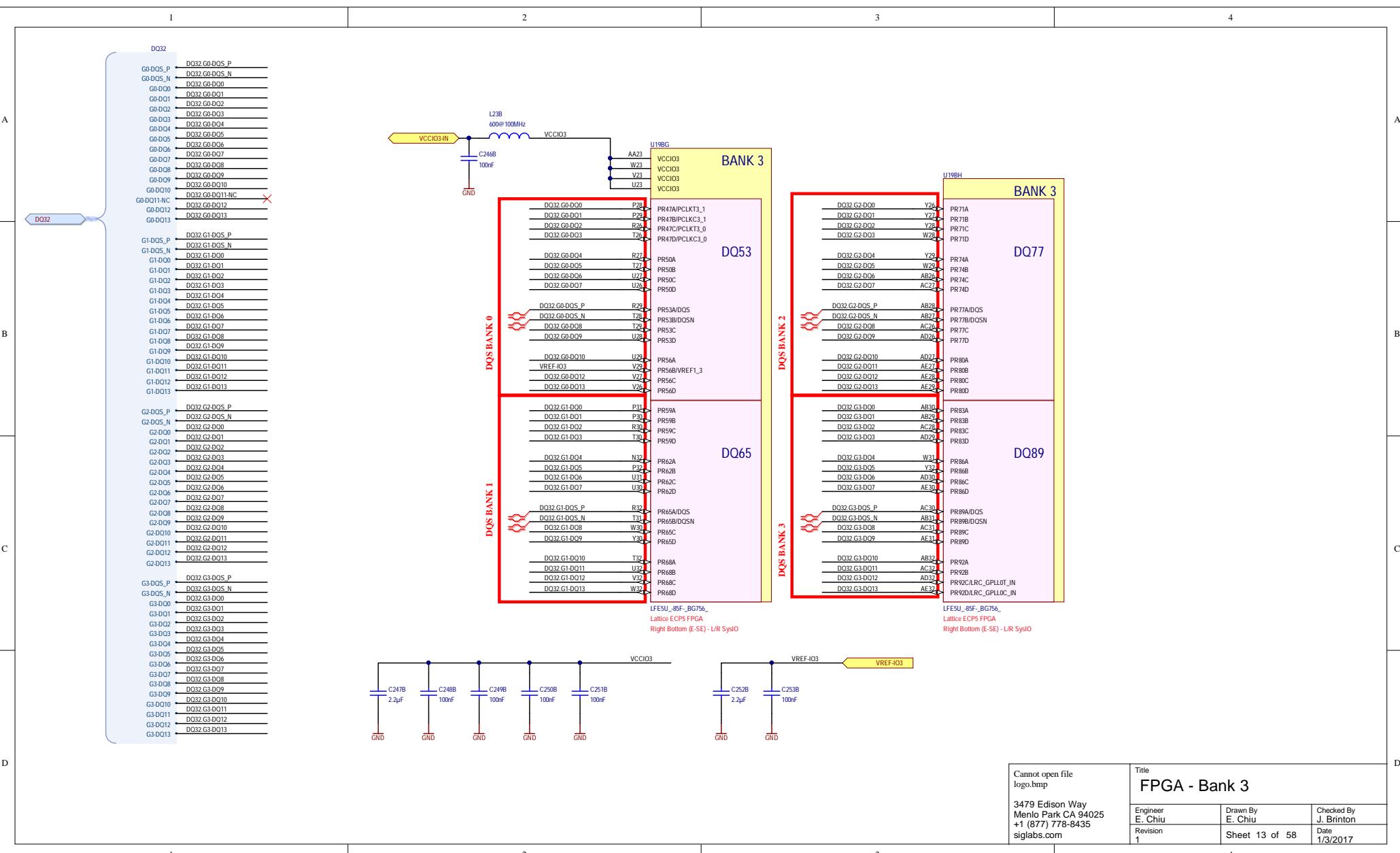
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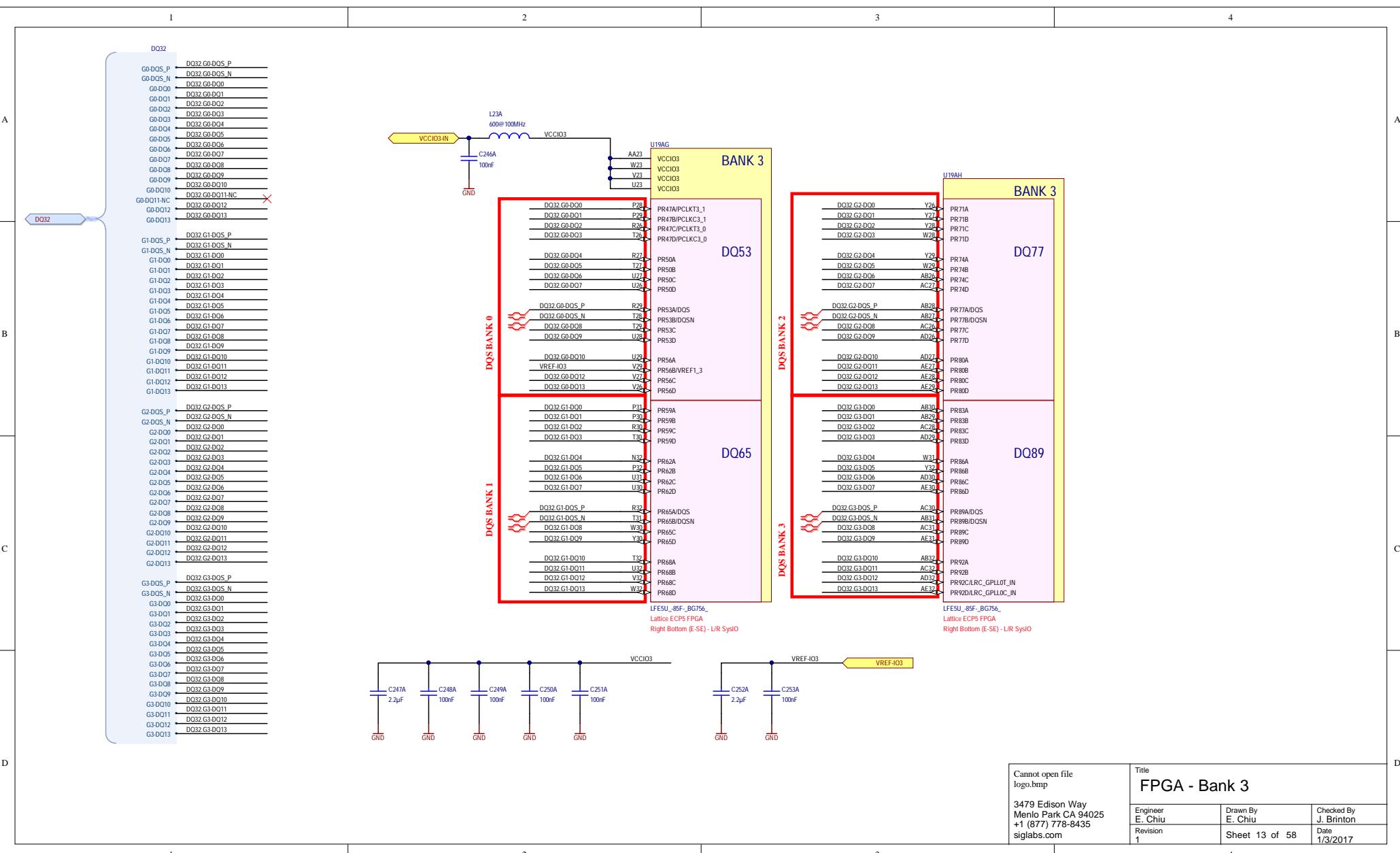
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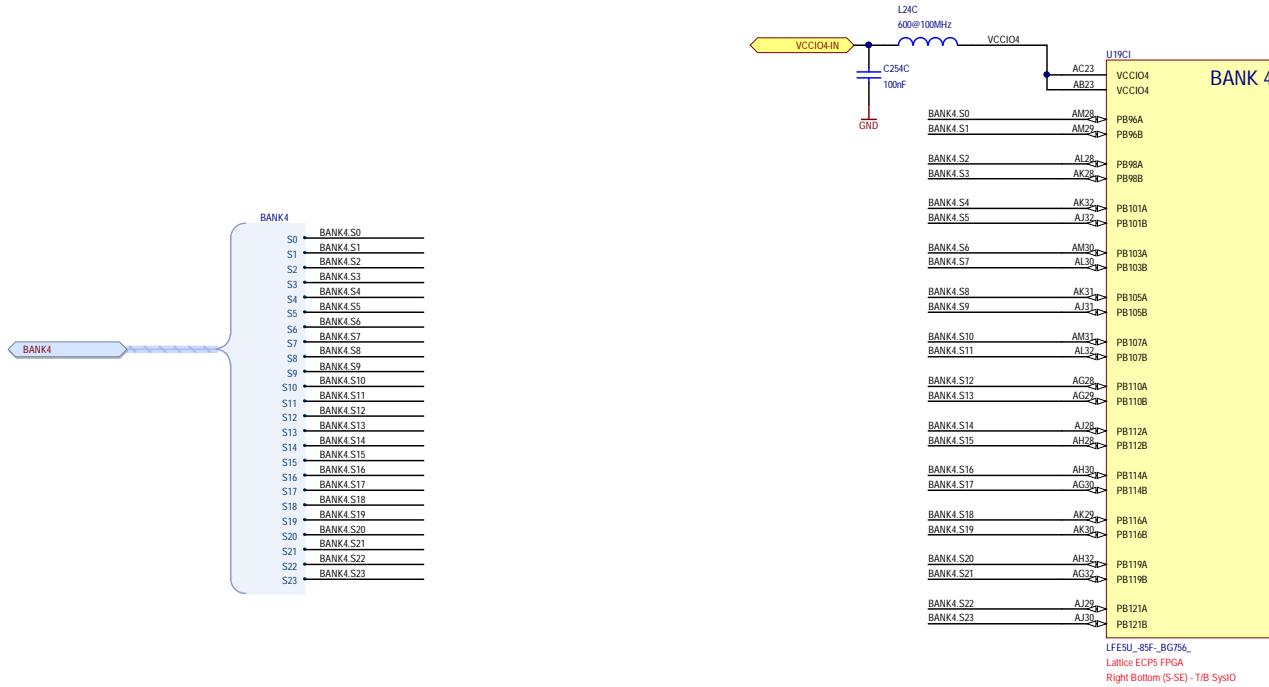
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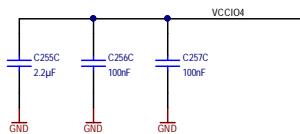
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FPGA - Bank 4

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Engineer	Drawn By	Checked By
E. Chiu	E. Chiu	J. Brinton
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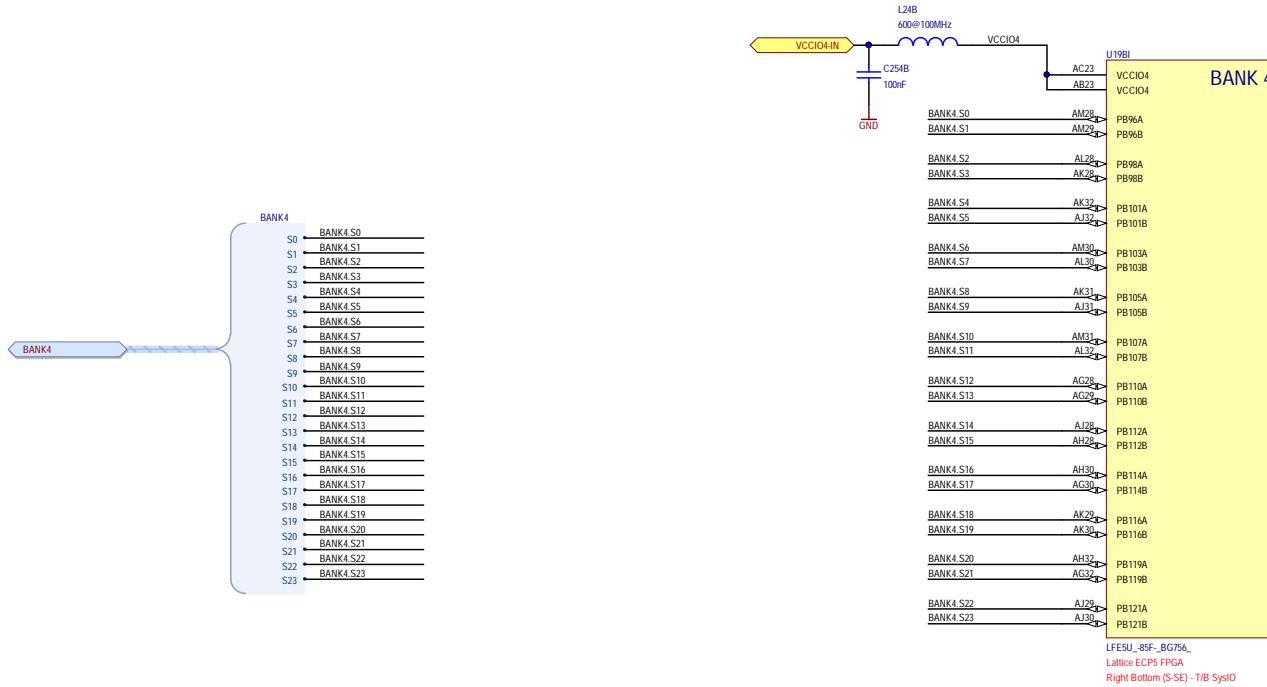
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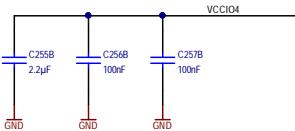
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FPGA - Bank 4

Engineer	Drawn By	Checked By
E. Chiu	E. Chiu	J. Brinton
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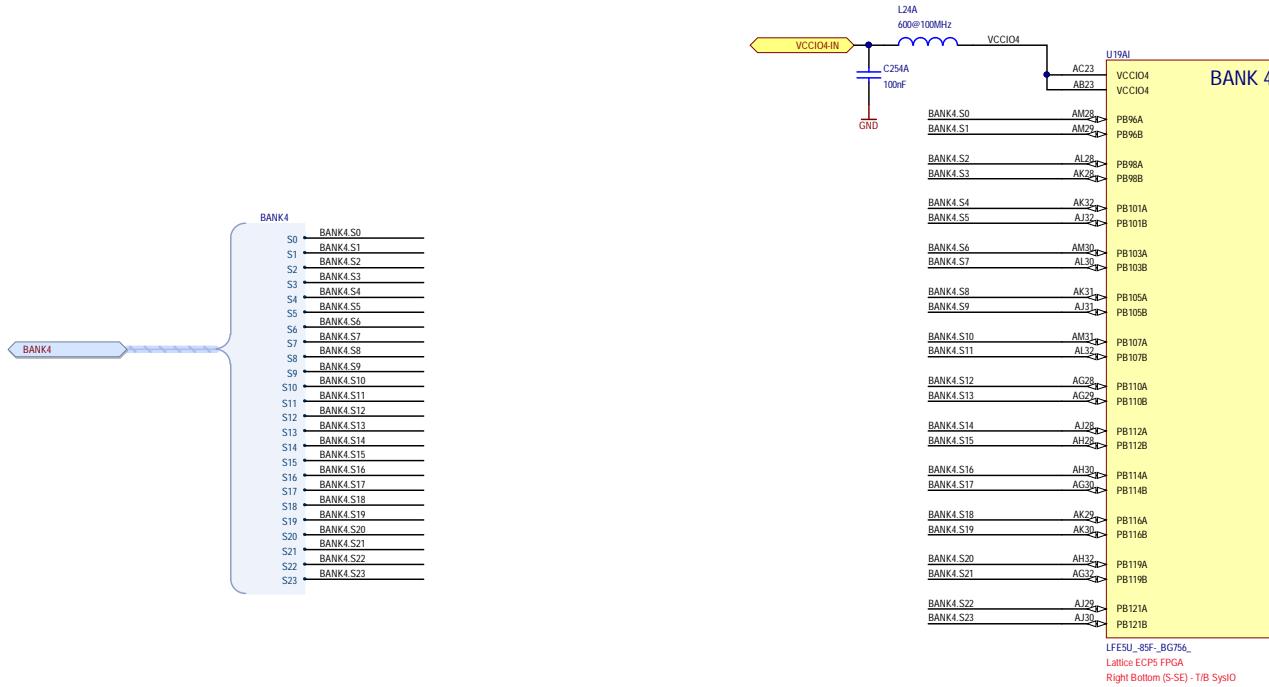
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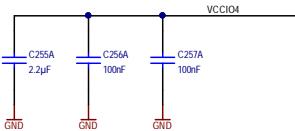


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FPGA - Bank 4

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Engineer	Drawn By	Checked By
E. Chiu	E. Chiu	J. Brinton
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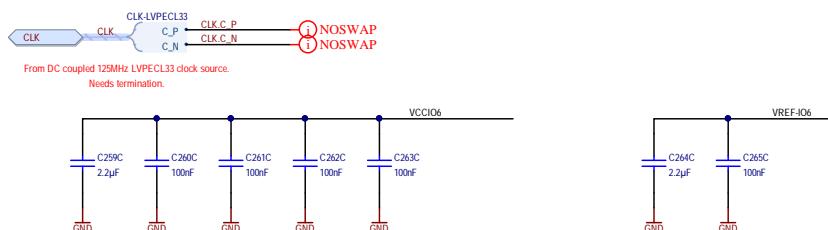
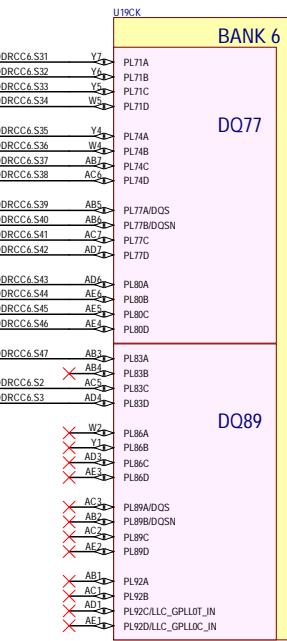
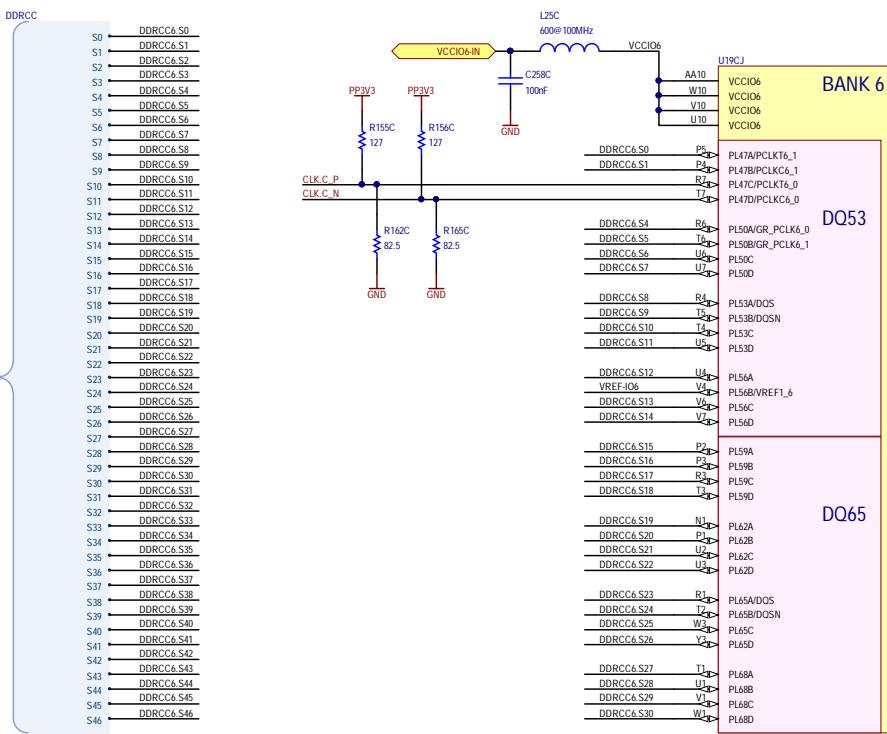
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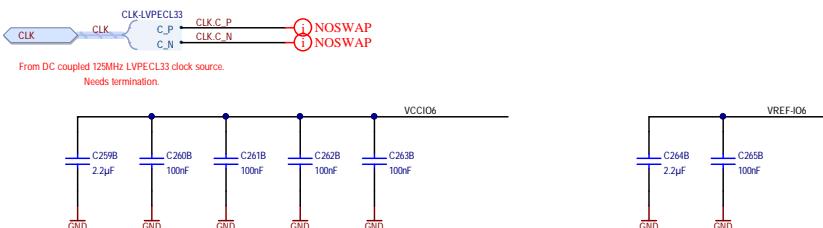
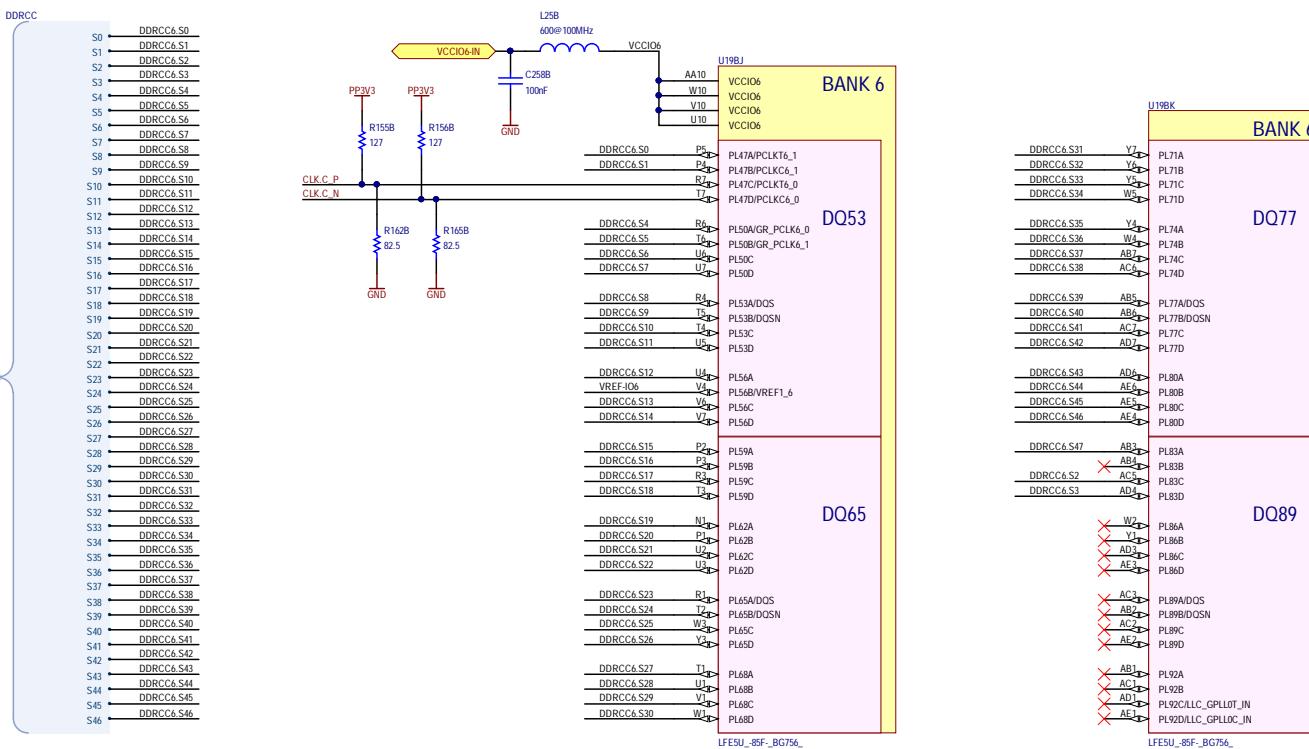
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Engineer E. Chiu	Drawn By E. Chiu	Checked By J. Brinton	Date 1/3/2017
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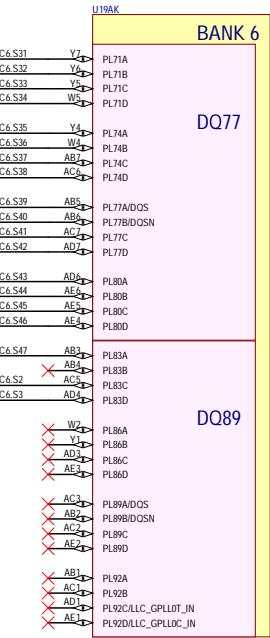
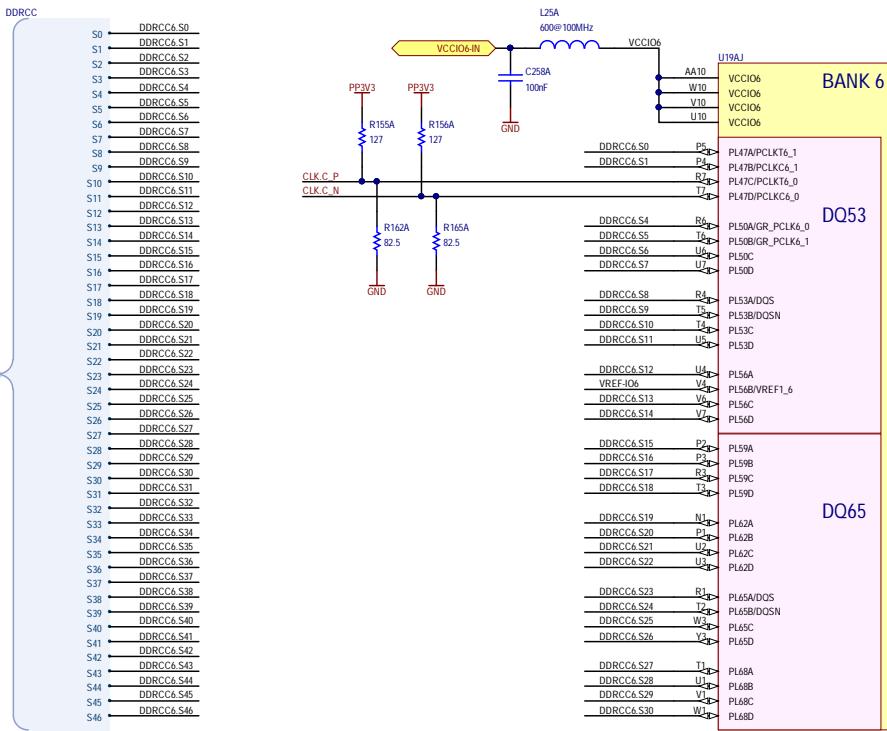
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3479 Edison Way Menlo Park CA 94025 +1 (877) 778-8435 siglabs.com	Engineer E. Chiu	Drawn By E. Chiu
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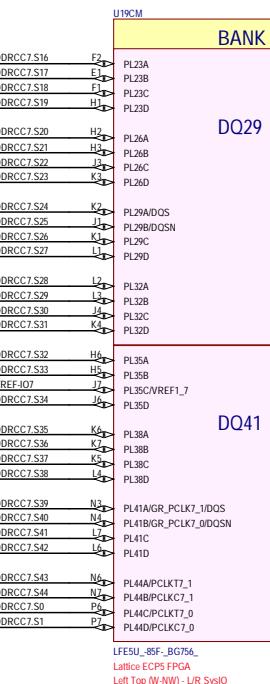
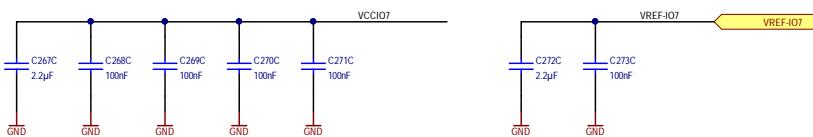
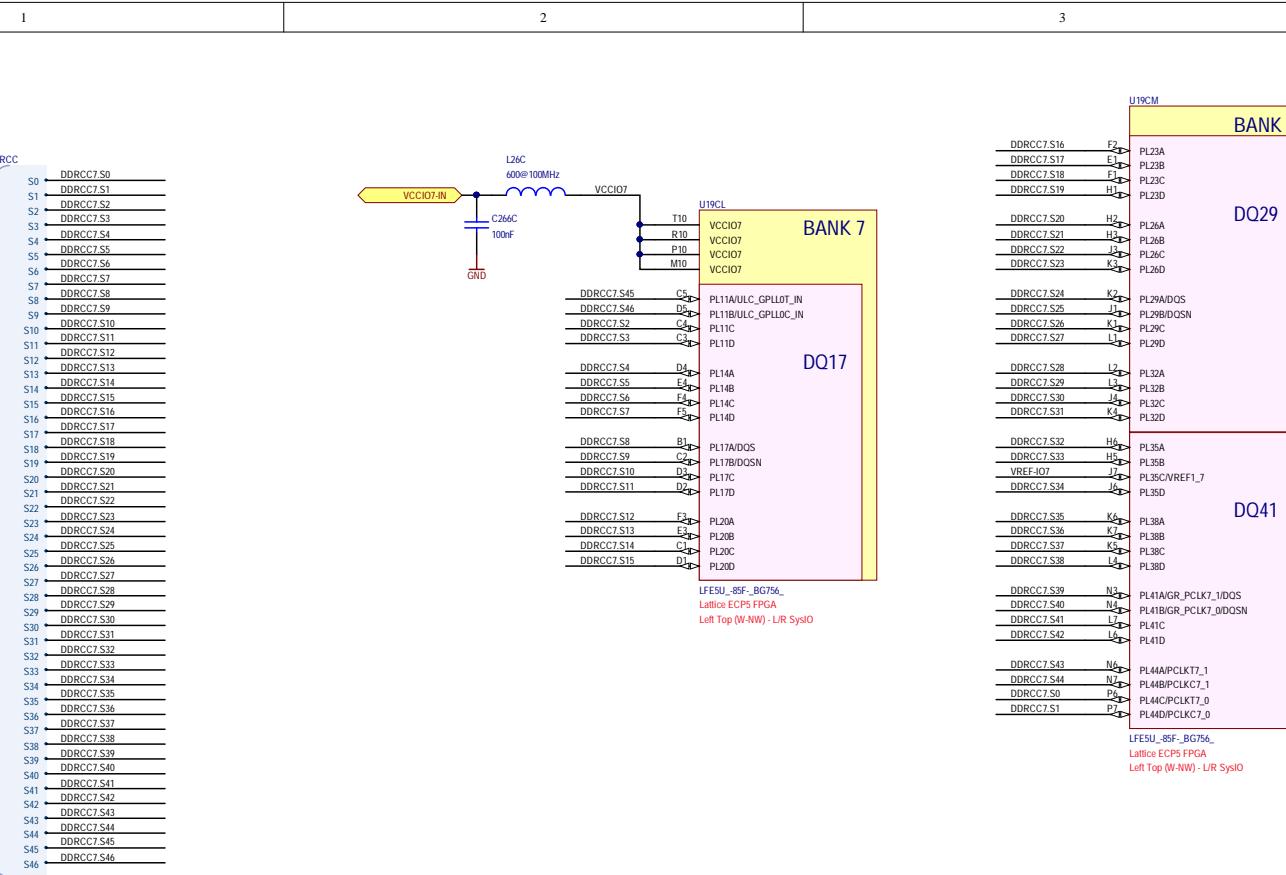
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Cannot open file logo.bmp		Title FPGA - Bank 6		
Engineer E. Chiu	Drawn By E. Chiu	Checked By		Date 1/3/2017
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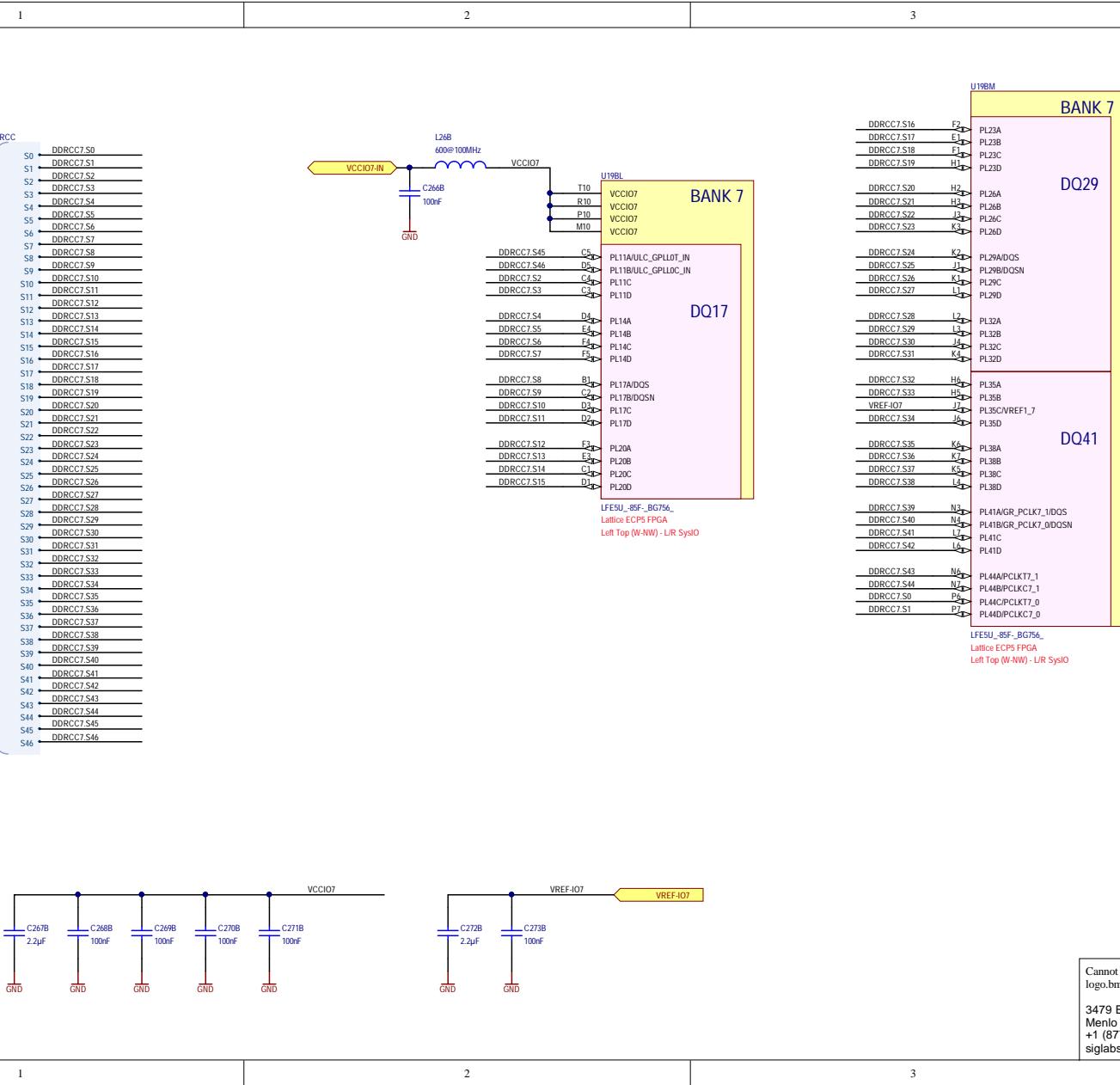
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FPGA - Bank 7

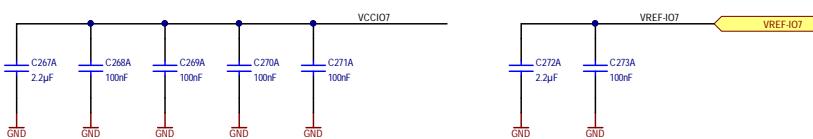
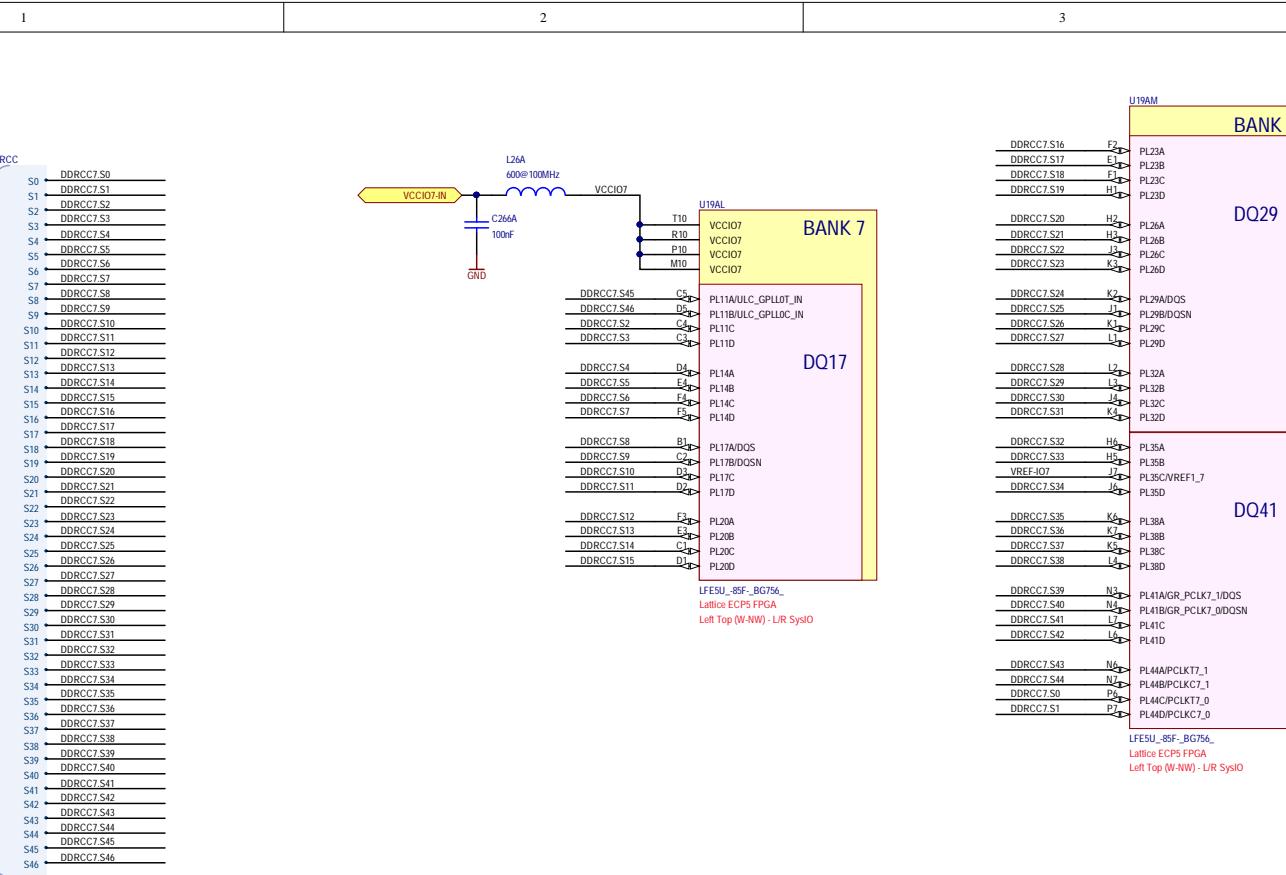
Engineer	Drawn By	Checked By
E. Chiu	E. Chiu	J. Brinton

Revision
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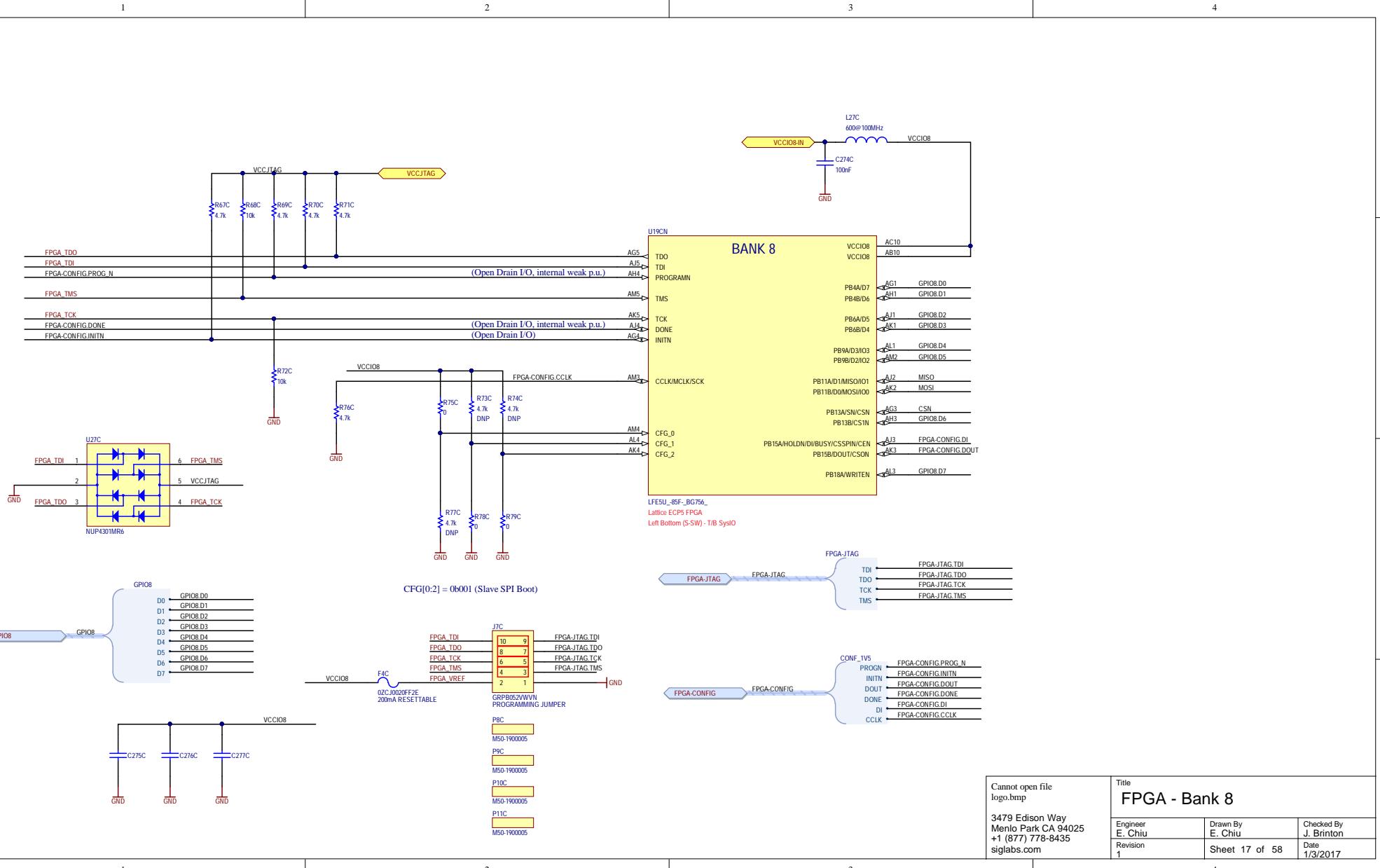
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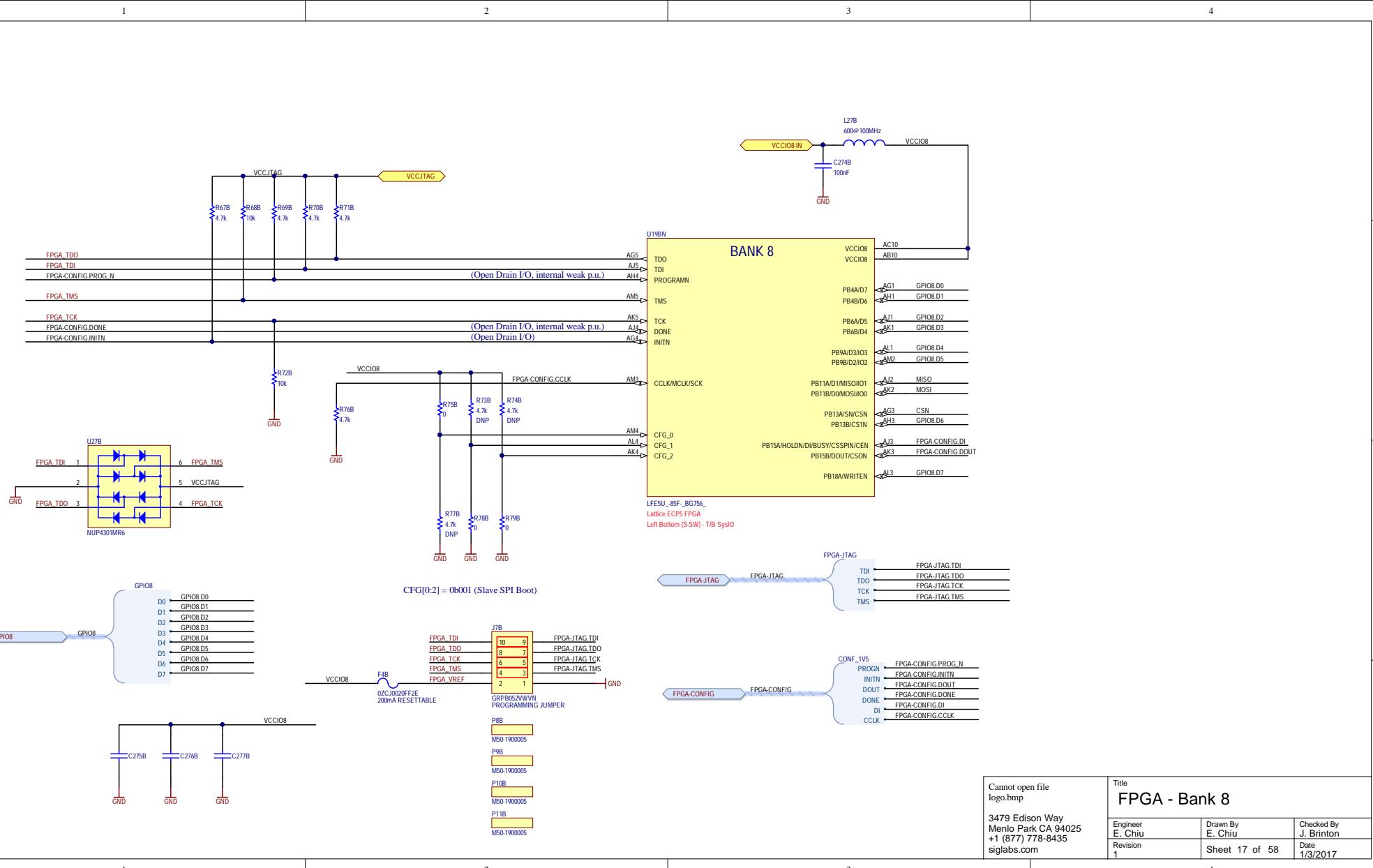
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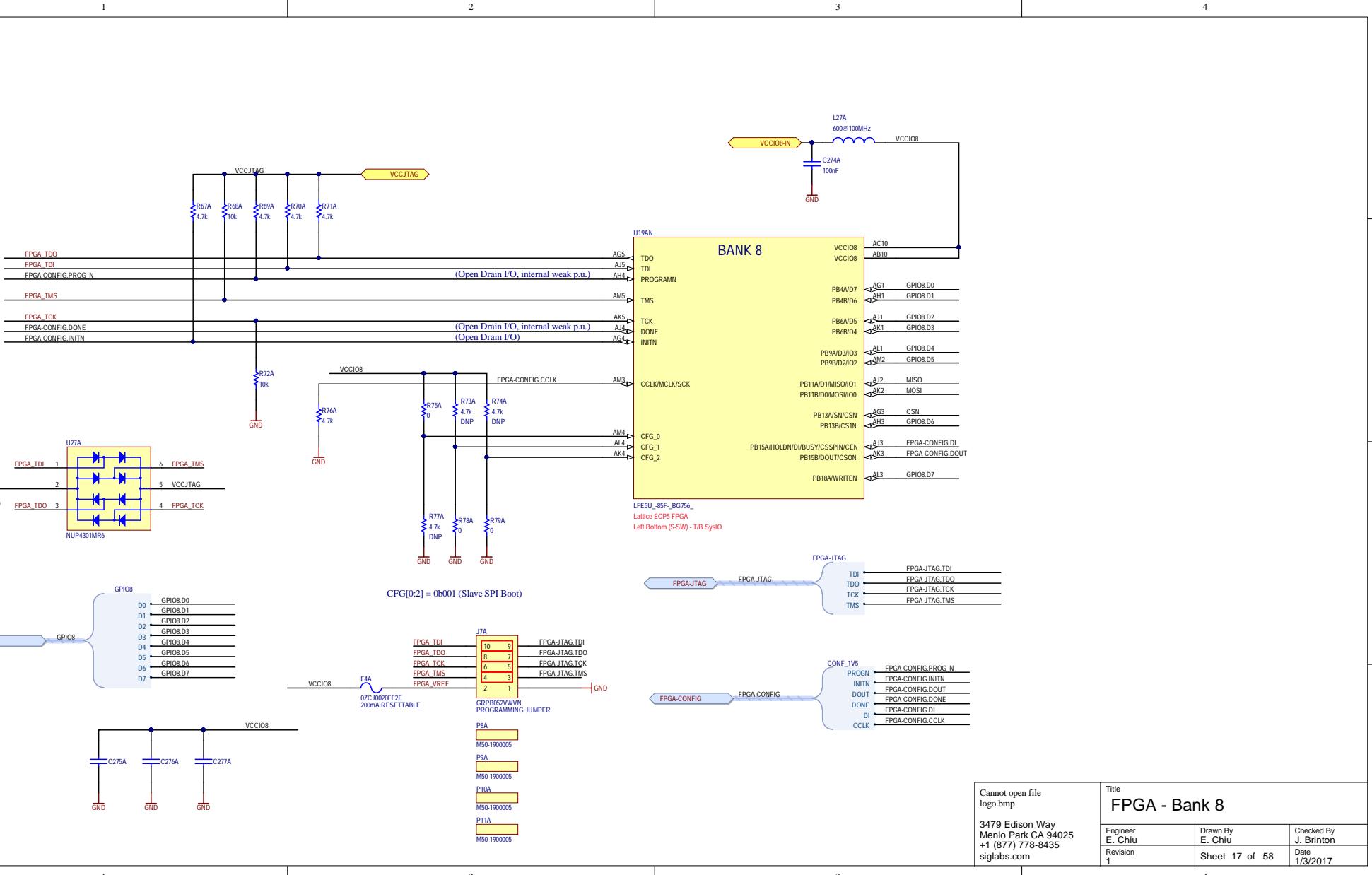




Title		
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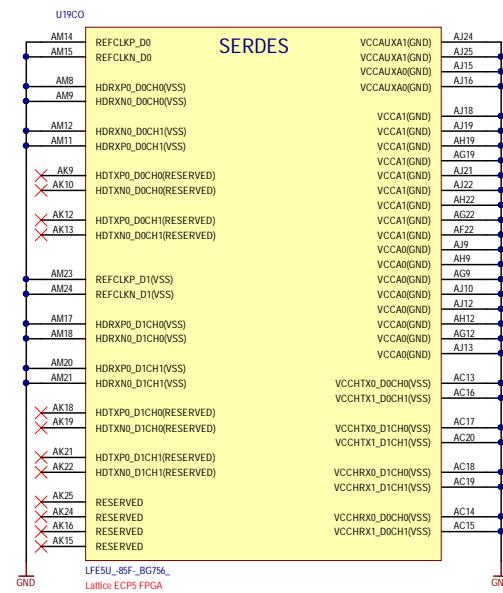
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FPGA - Serdes

Engineer E. Chiu	Drawn By E. Chiu	Checked By J. Brinton
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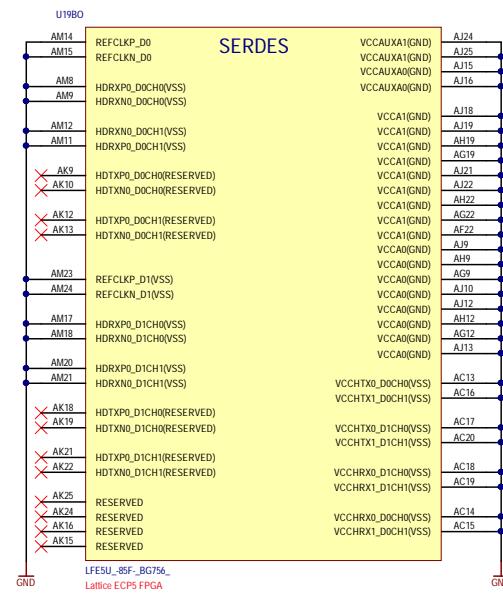
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FPGA - Serdes

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Engineer	Drawn By	Checked By
E. Chiu	E. Chiu	J. Brinton
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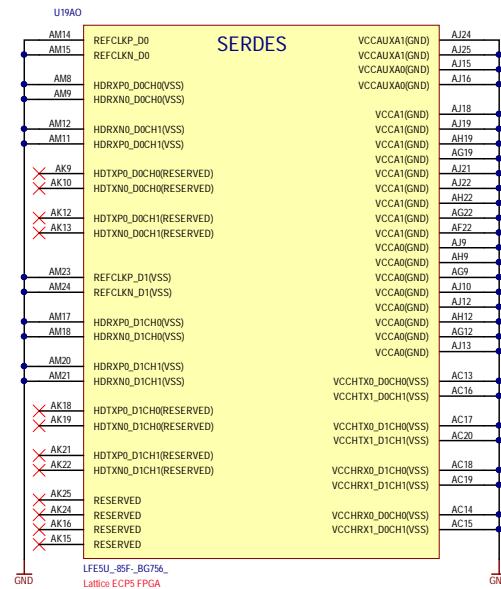
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Title
FPGA - Serdes

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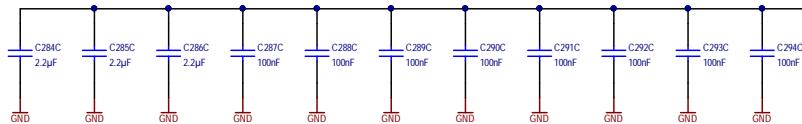
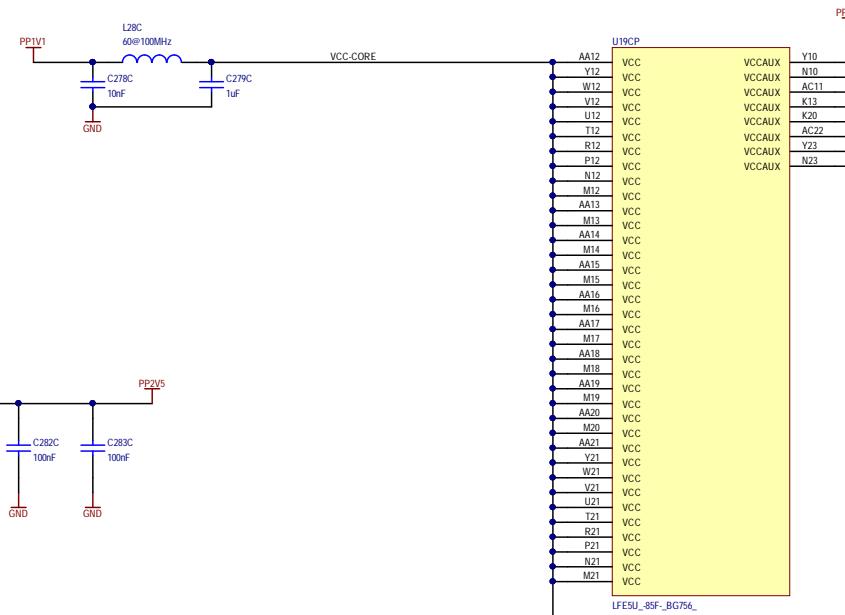
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FPGA - Power

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Engineer
E. Chiu

Drawn By
E. Chiu

Checked By
J. Brinton

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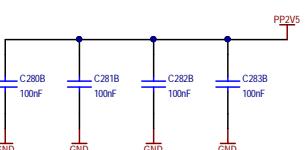
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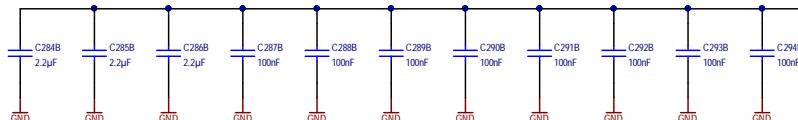


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Lattice ECP5 FPGA



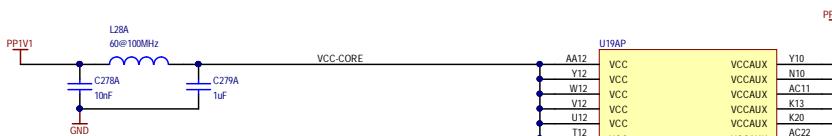
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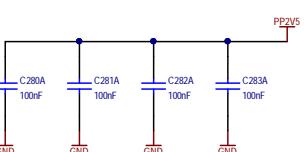
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Engineer E. Chiu	Drawn By E. Chiu	Checked By J. Brinton
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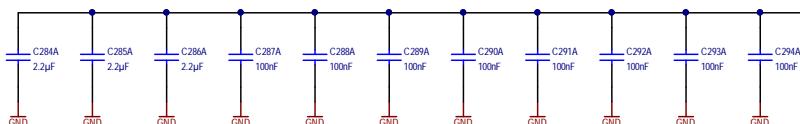
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Lattice ECP5 FPGA

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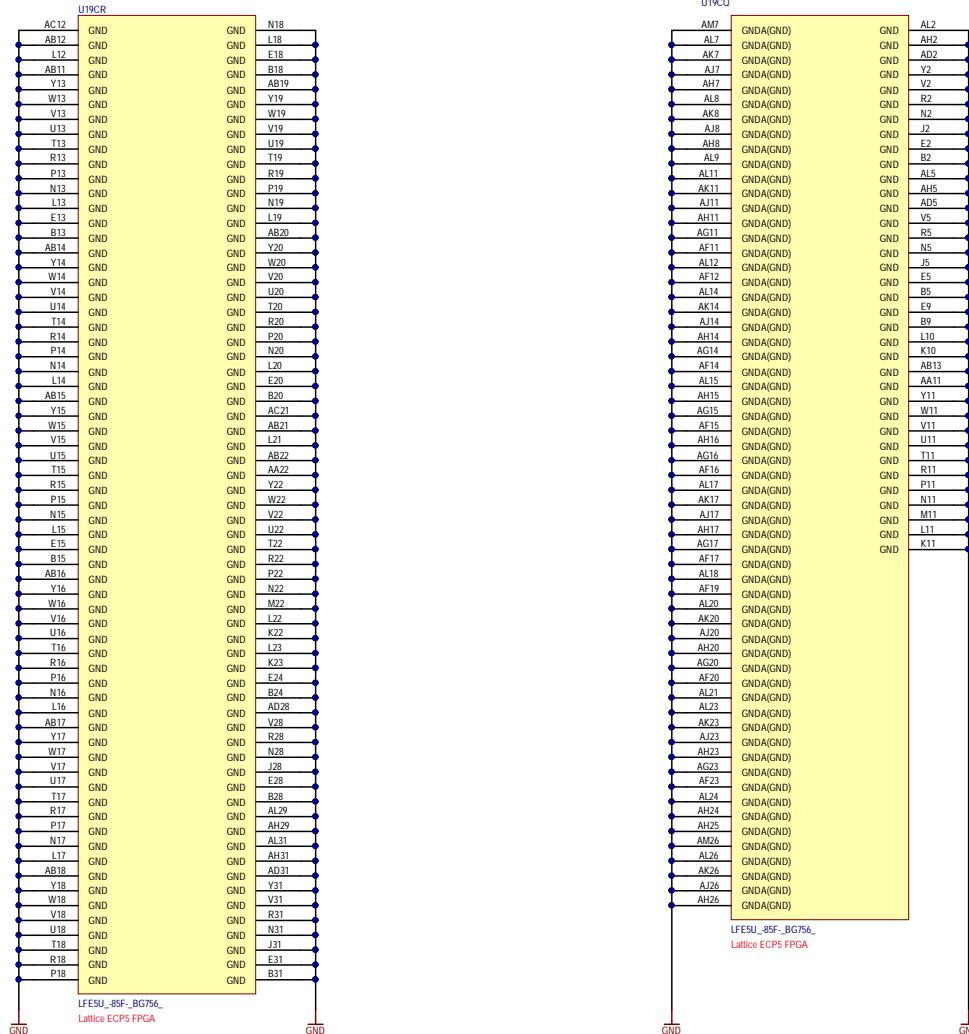
Engineer E. Chiu	Drawn By E. Chiu	Checked By J. Brinton
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FPGA - Ground

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Engineer	Drawn By	Checked By
E. Chiu	E. Chiu	
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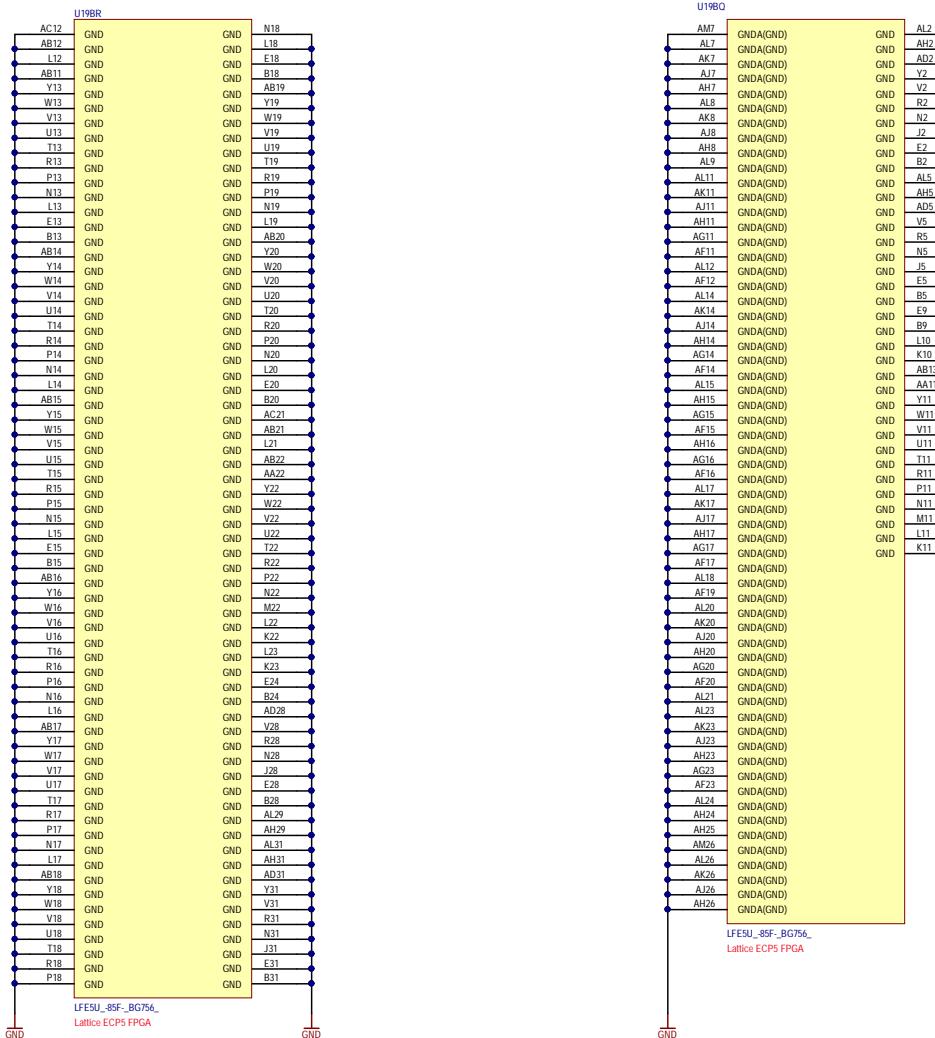
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Title
FPGA - Ground
3479 Edison Way
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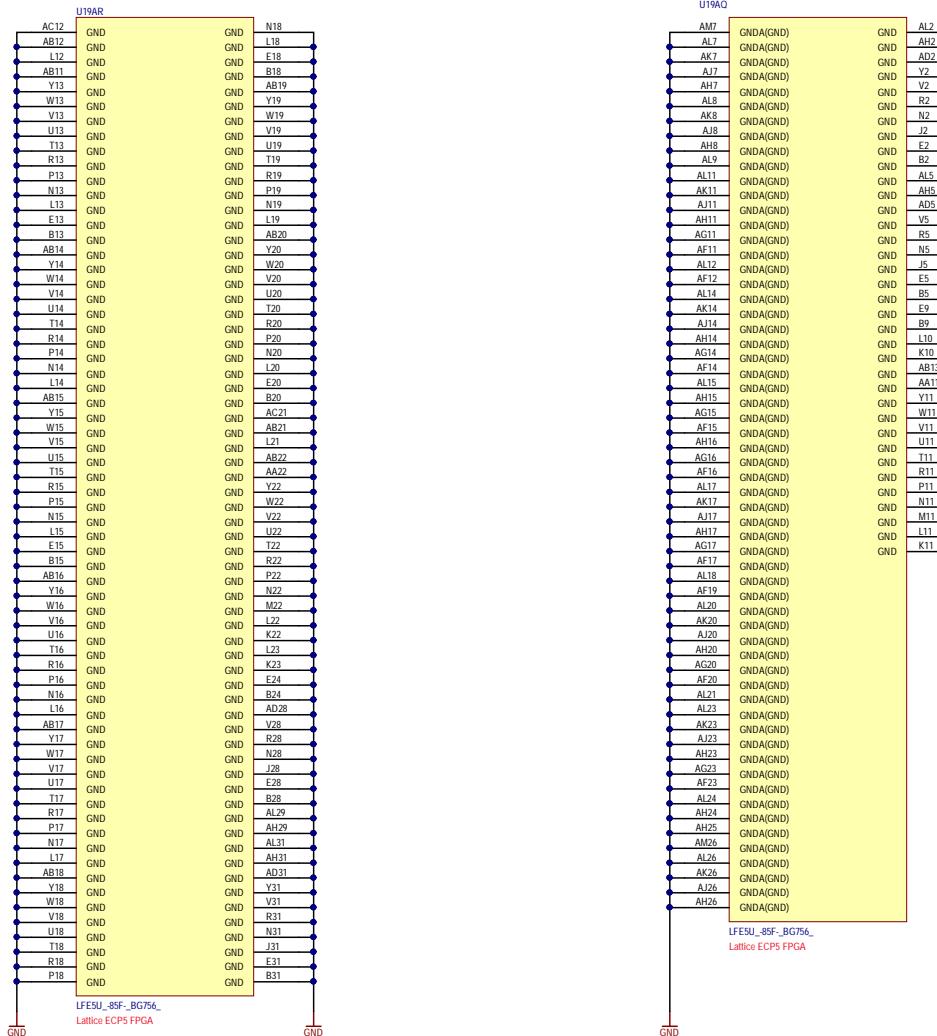
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siglabs.comEngineer
E. Chiu
Revision
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Drawn By
E. Chiu
Checked By
Date
1/3/2017

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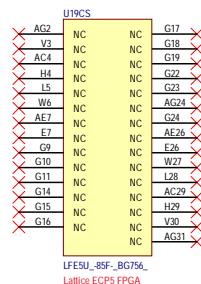
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Title
FPGA - Misc

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E. Chiu	E. Chiu	J. Brinton
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E. Chiu	E. Chiu	J. Brinton
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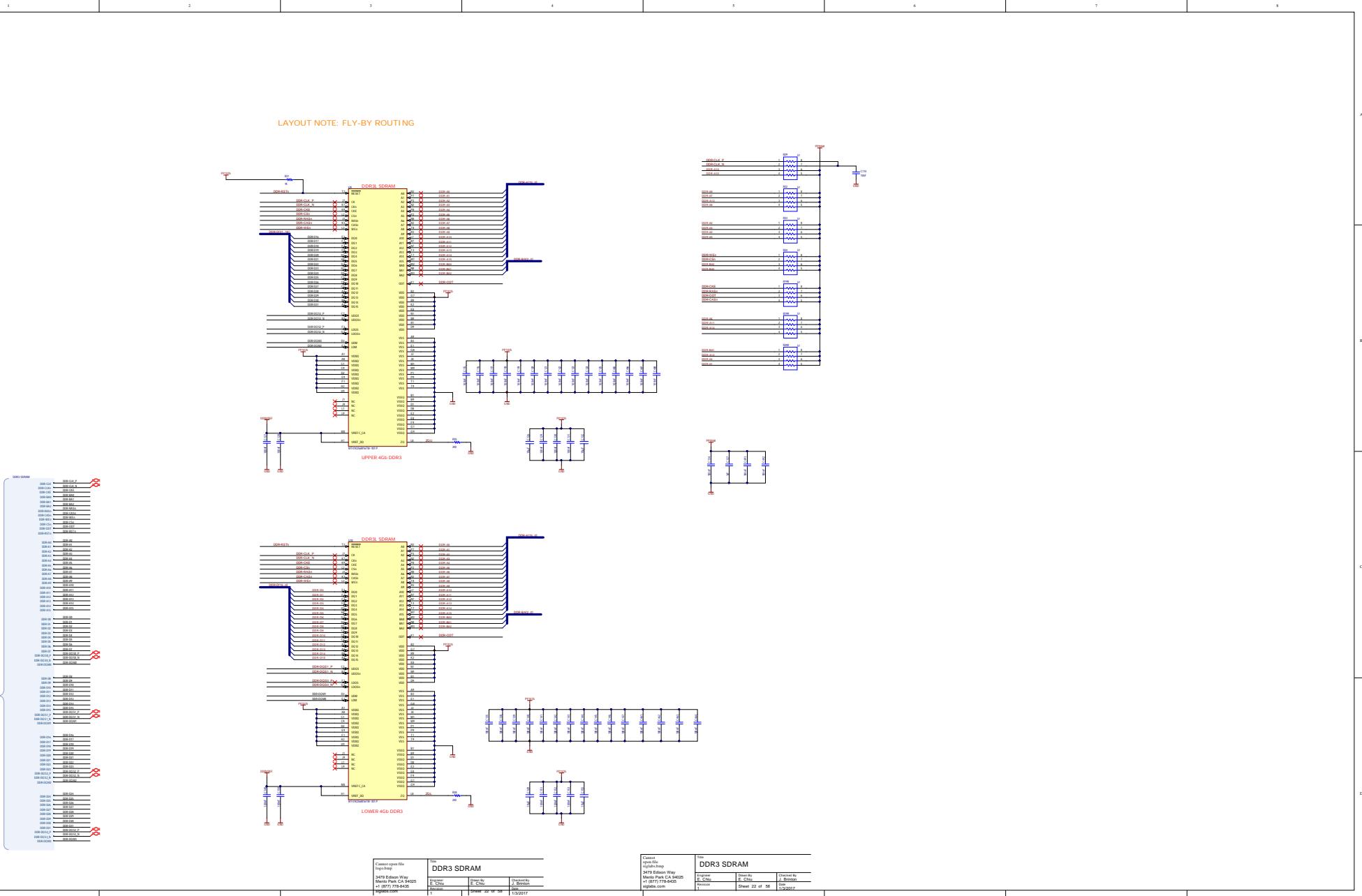
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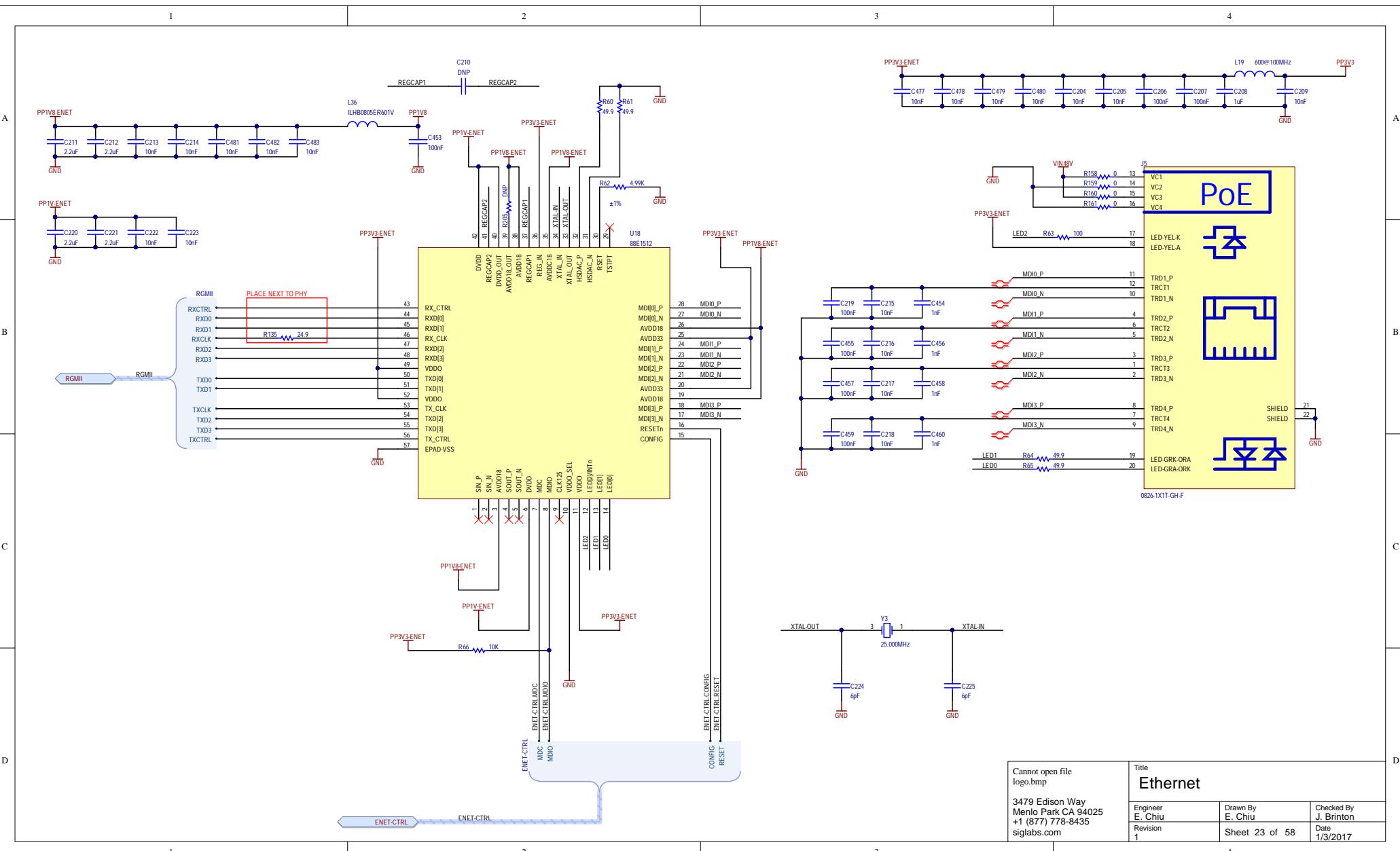
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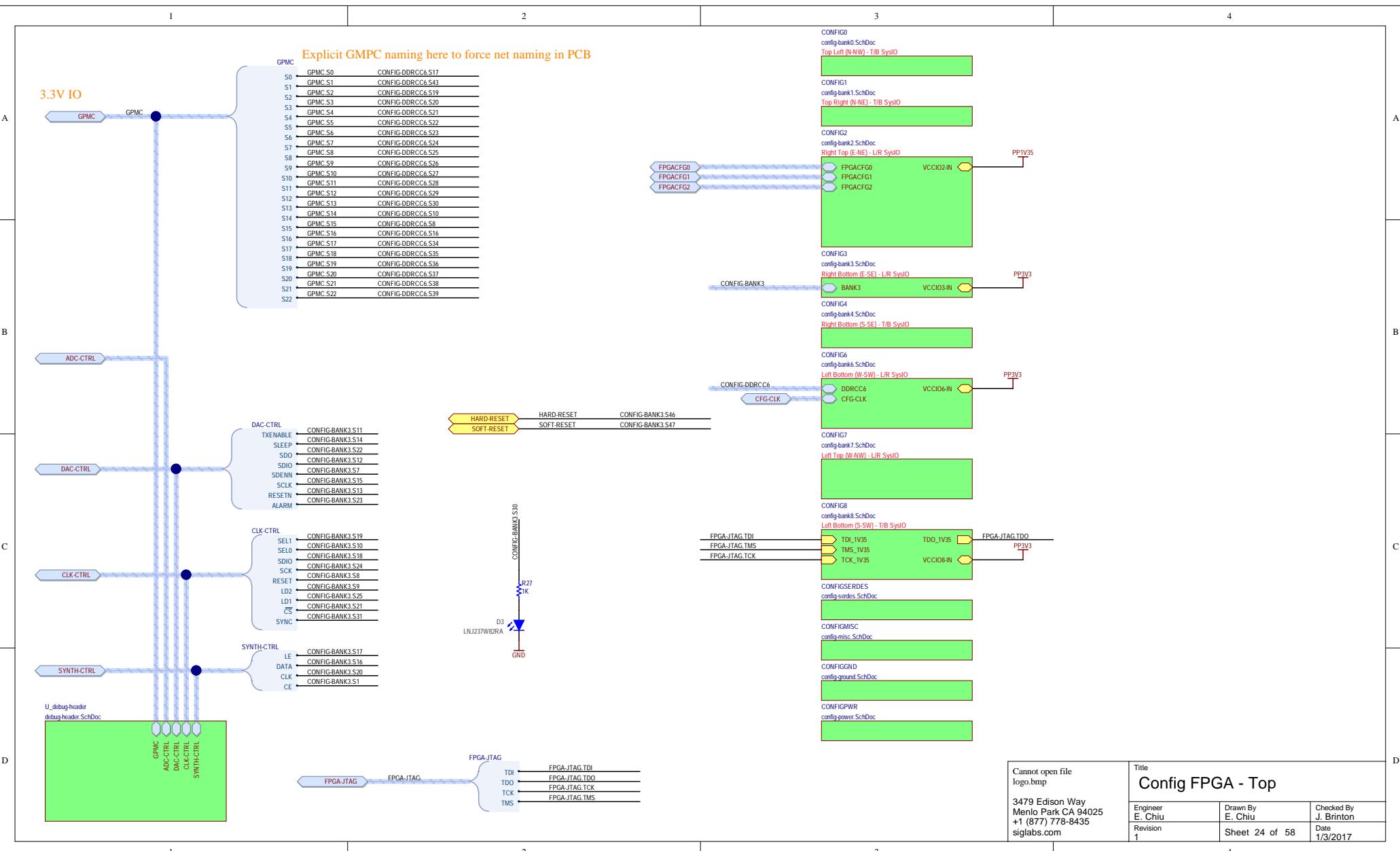
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E. Chiu	E. Chiu	J. Brinton
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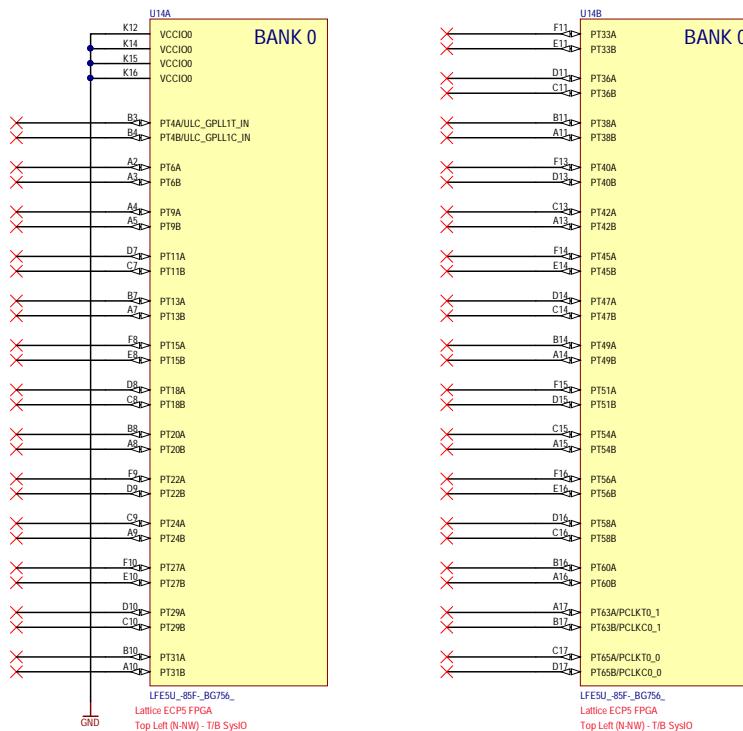
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Config FPGA - Bank 0		
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3479 Edison Way Menlo Park CA 94025 +1 (877) 778-8435 siglabs.com	Engineer E. Chiu	Drawn By E. Chiu
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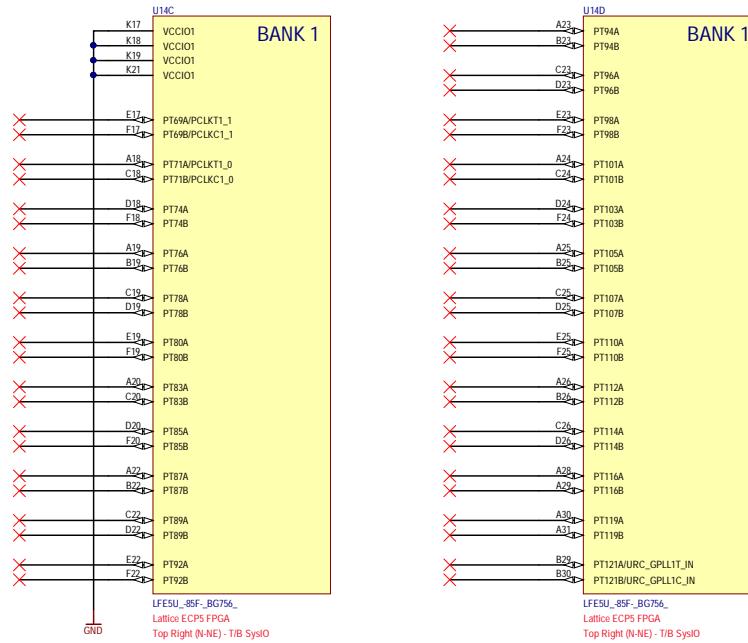
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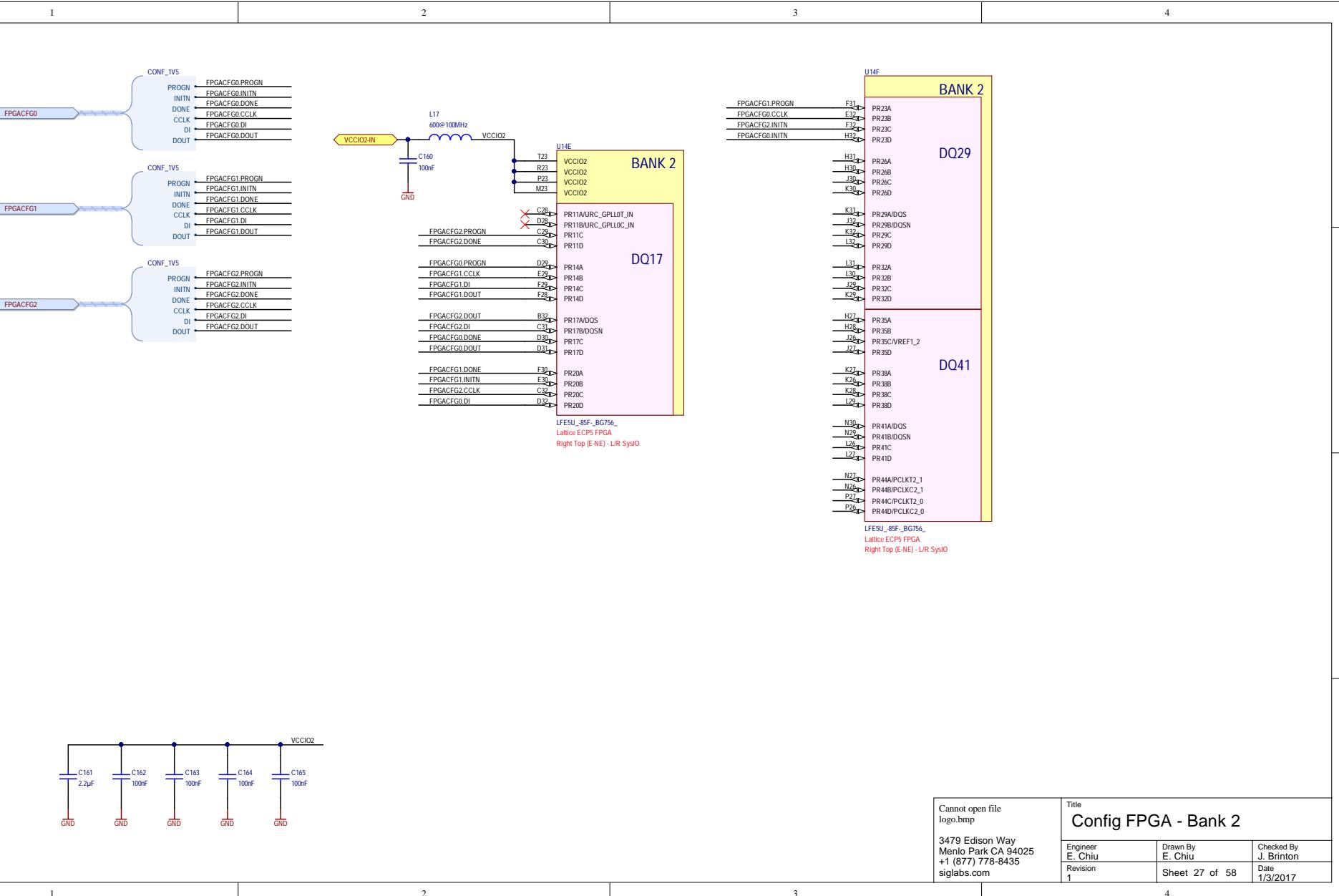
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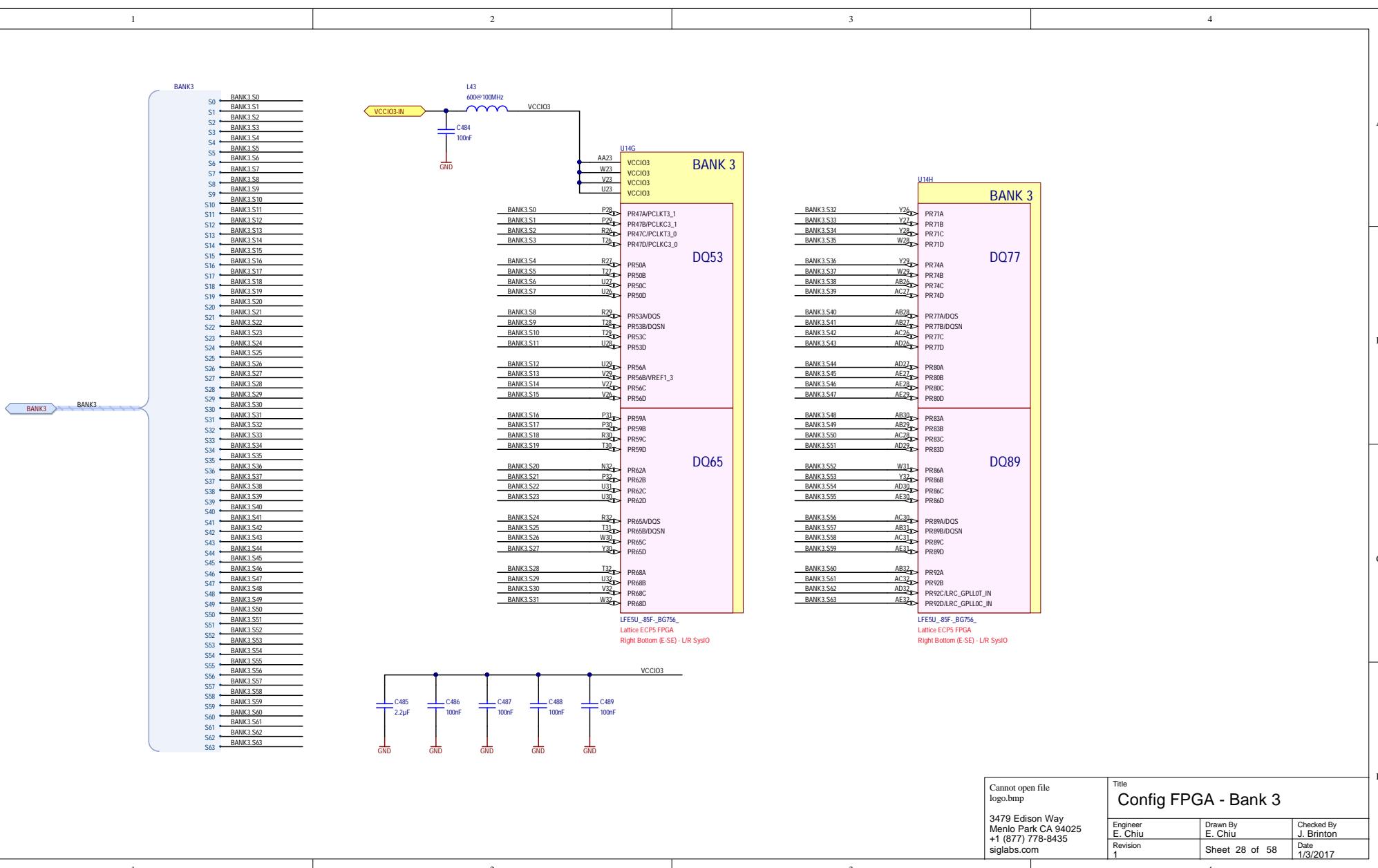
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Title
Config FPGA - Bank 1

Engineer E. Chiu	Drawn By E. Chiu	Checked By J. Brinton
Revision 1	Sheet 26 of 58	Date 1/3/2017





A

B

C

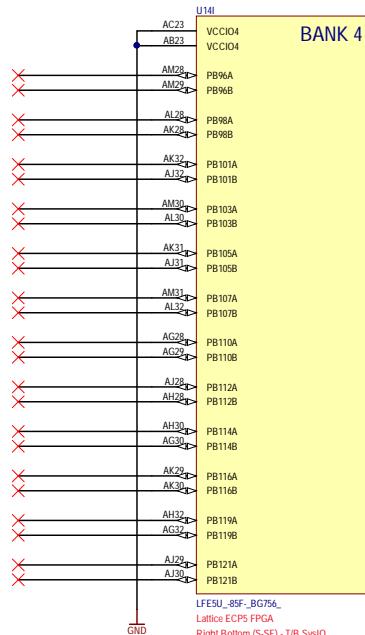
D

A

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Config FPGA - Bank 4

Engineer	Drawn By	Checked By
E. Chiu	E. Chiu	J. Brinton

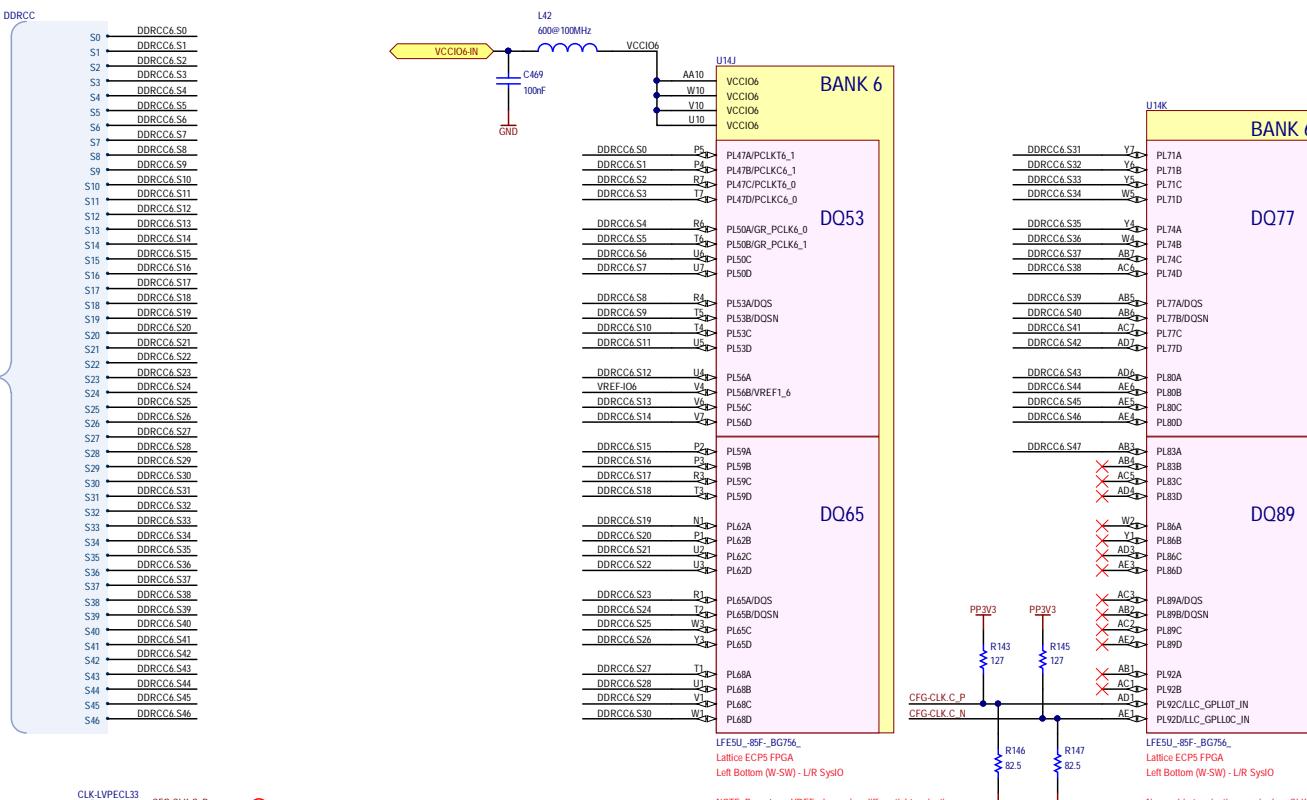
Revision

1

Sheet 29 of 58

Date 1/3/2017

1 2 3 4



Title Config FPGA - Bank 6		
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3479 Edison Way Menlo Park CA 94025 +1 (877) 778-8435 siglabs.com	Drawn By E. Chiu	Checked By J. Brinton
Revision 1	Sheet 30 of 58	Date 1/3/2017

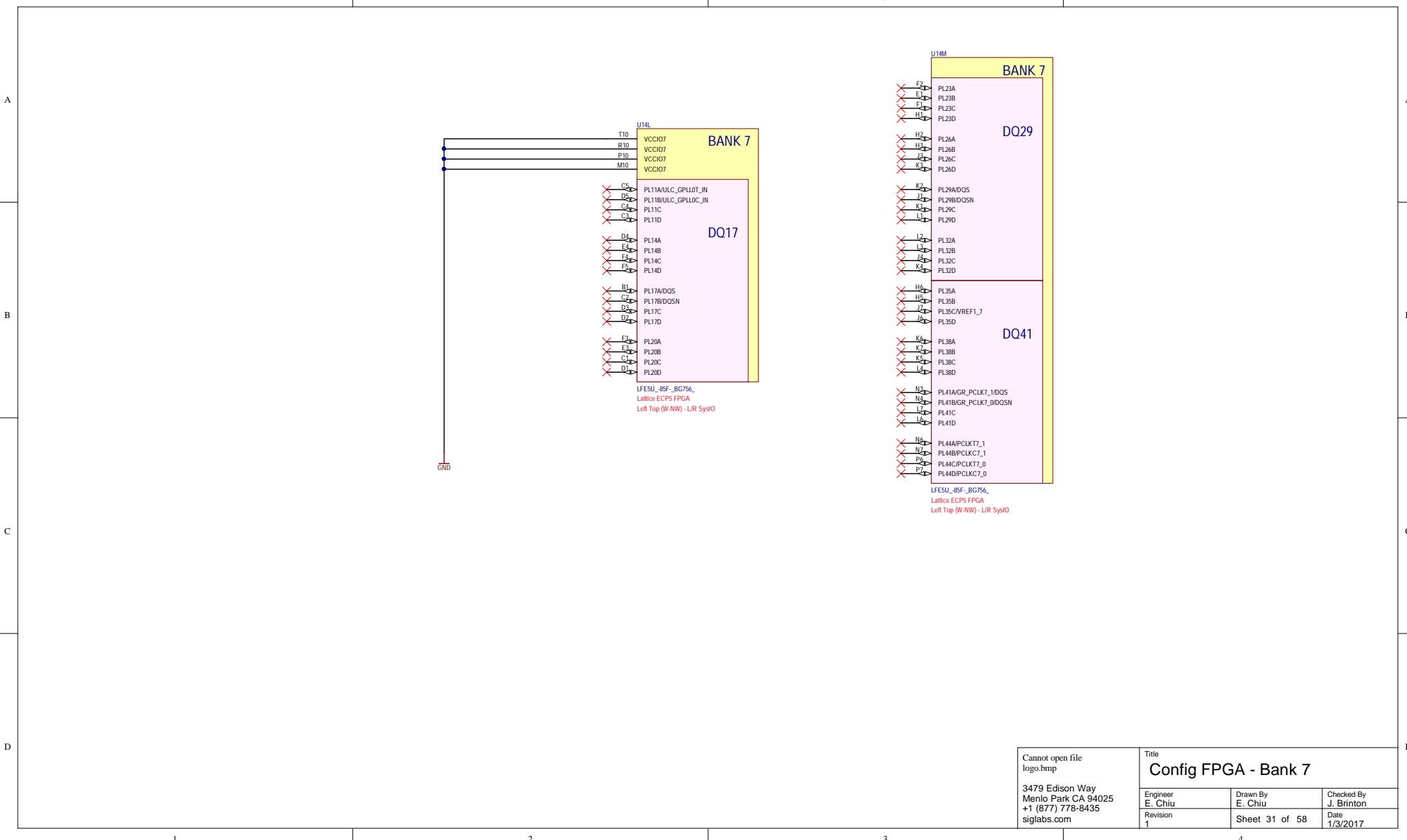
1 2 3 4

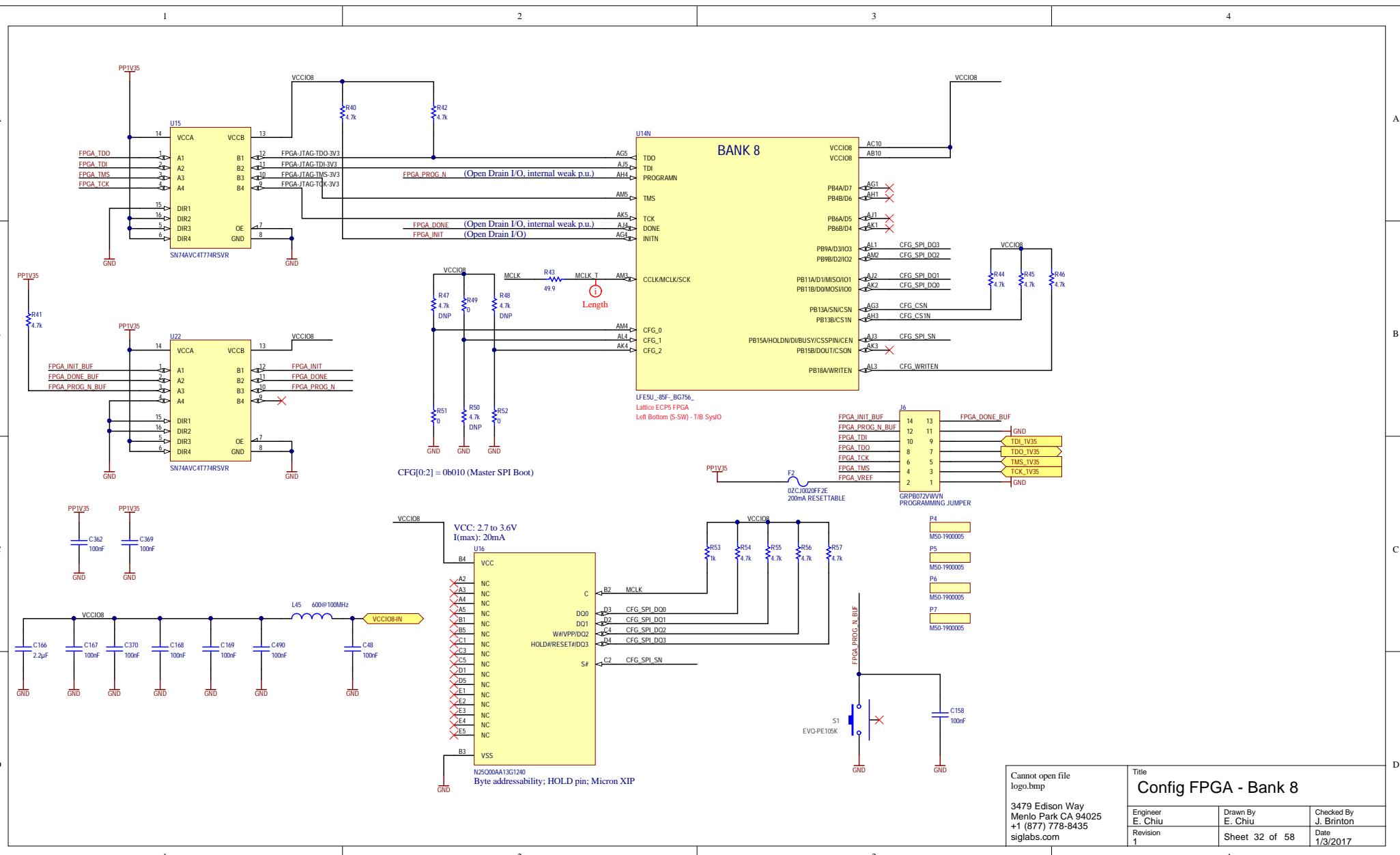
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A

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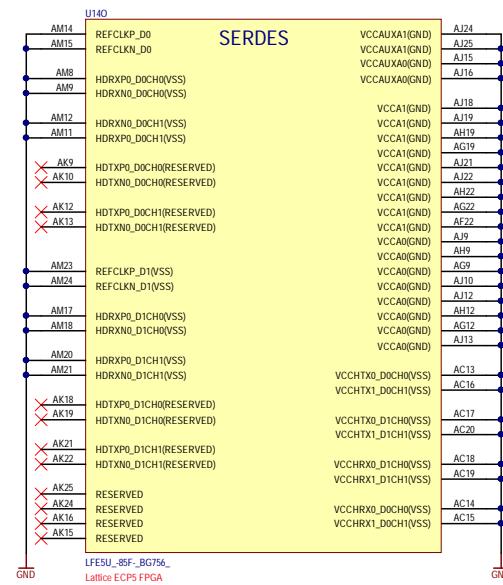
B

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C

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D

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Config FPGA - Serdes

Engineer	Drawn By	Checked By
E. Chiu	E. Chiu	J. Brinton

A

B

C

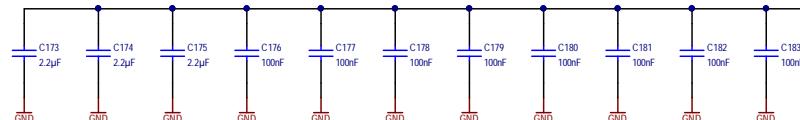
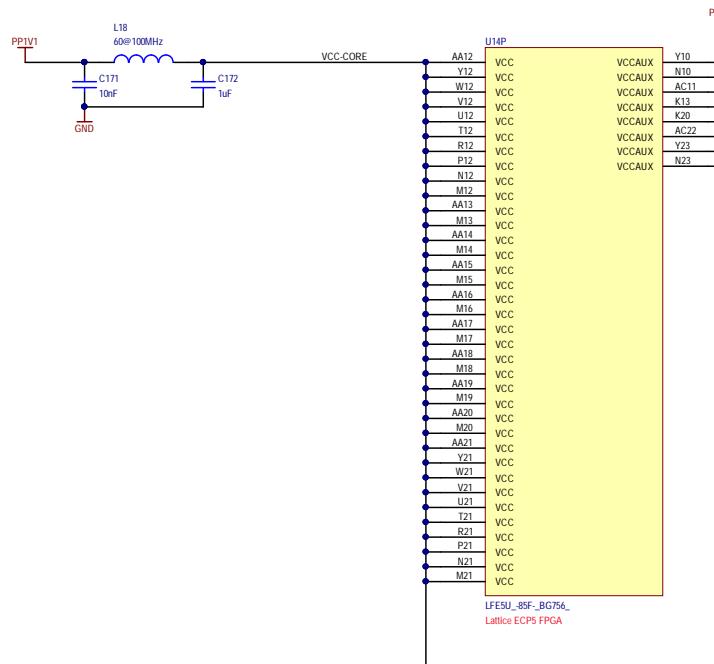
D

A

B

C

D



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Config FPGA - Power

Engineer E. Chiu	Drawn By E. Chiu	Checked By J. Brinton
Revision 1	Sheet 34 of 58	Date 1/3/2017

A

B

C

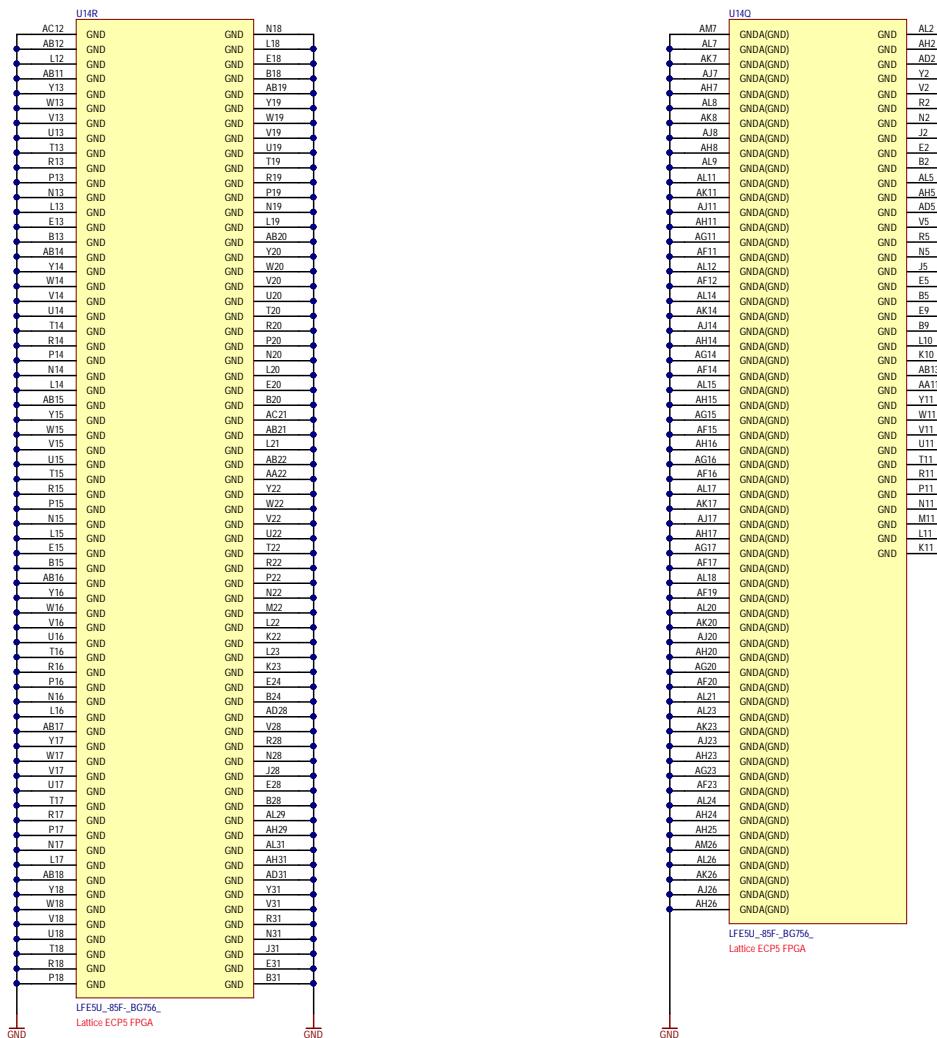
D

A

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Title
Config FPGA - Ground

Engineer E. Chiu	Drawn By E. Chiu	Checked By J. Brinton
Revision 1	Sheet 35 of 58	Date 1/3/2017

A

A

B

B

C

C

D

D

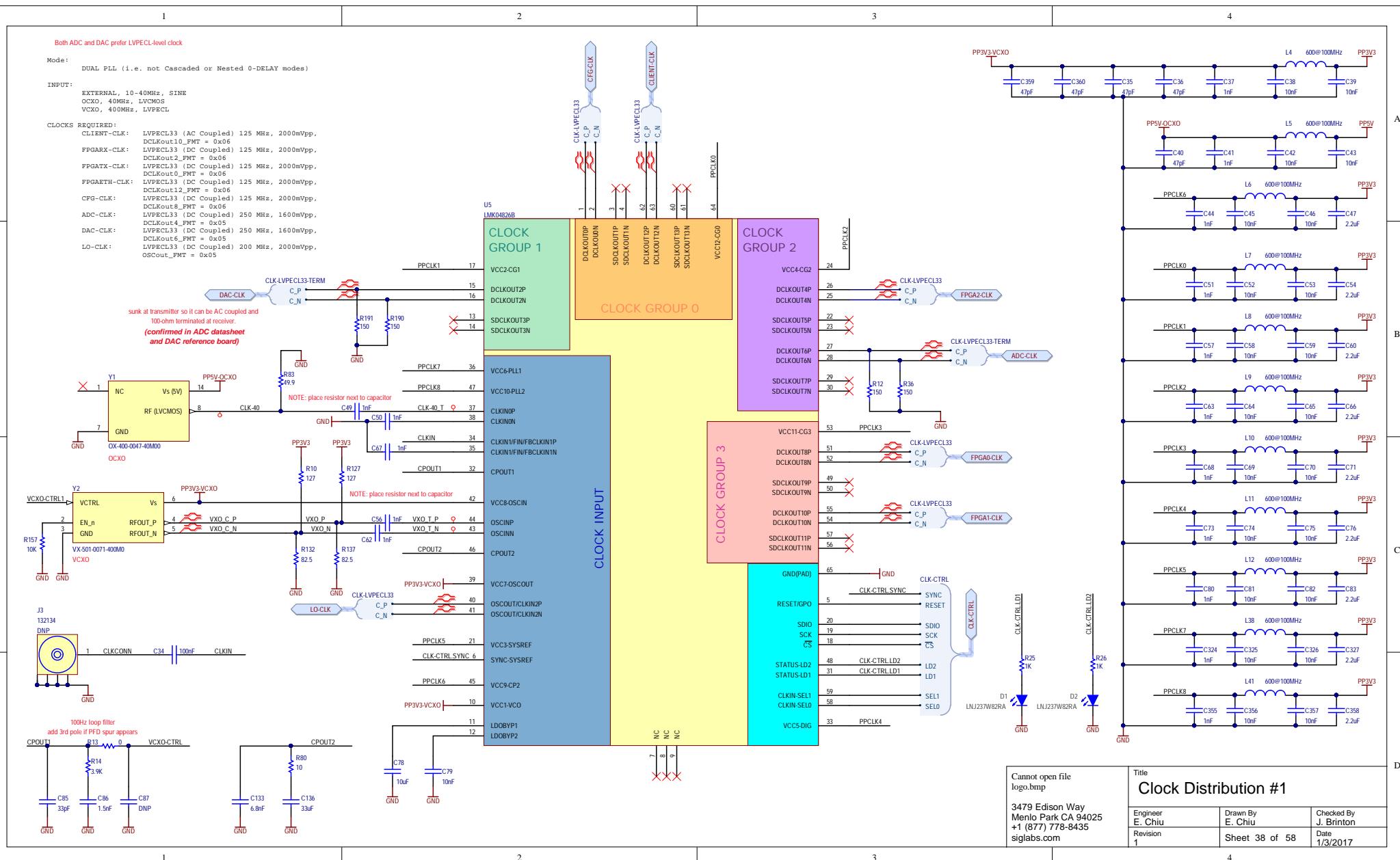


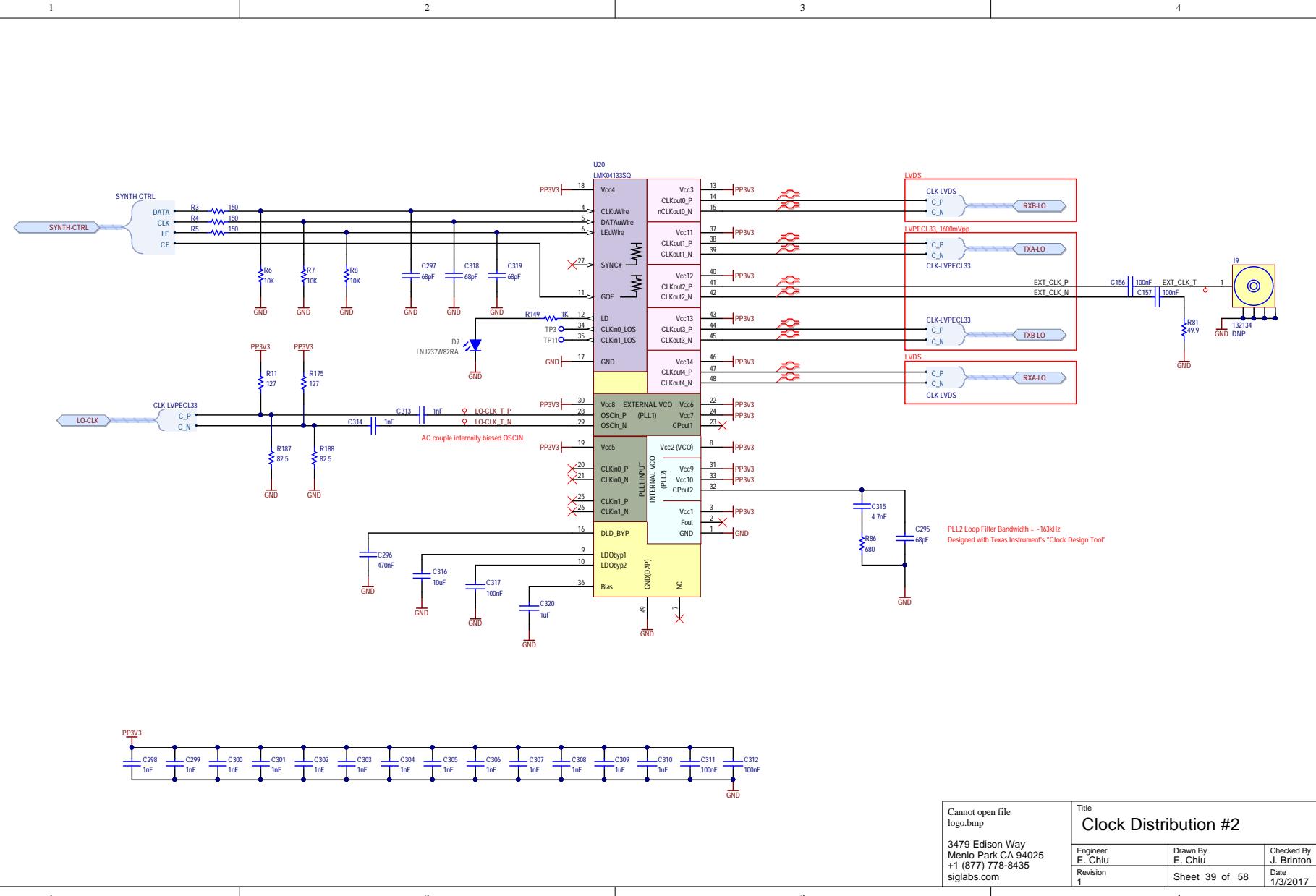
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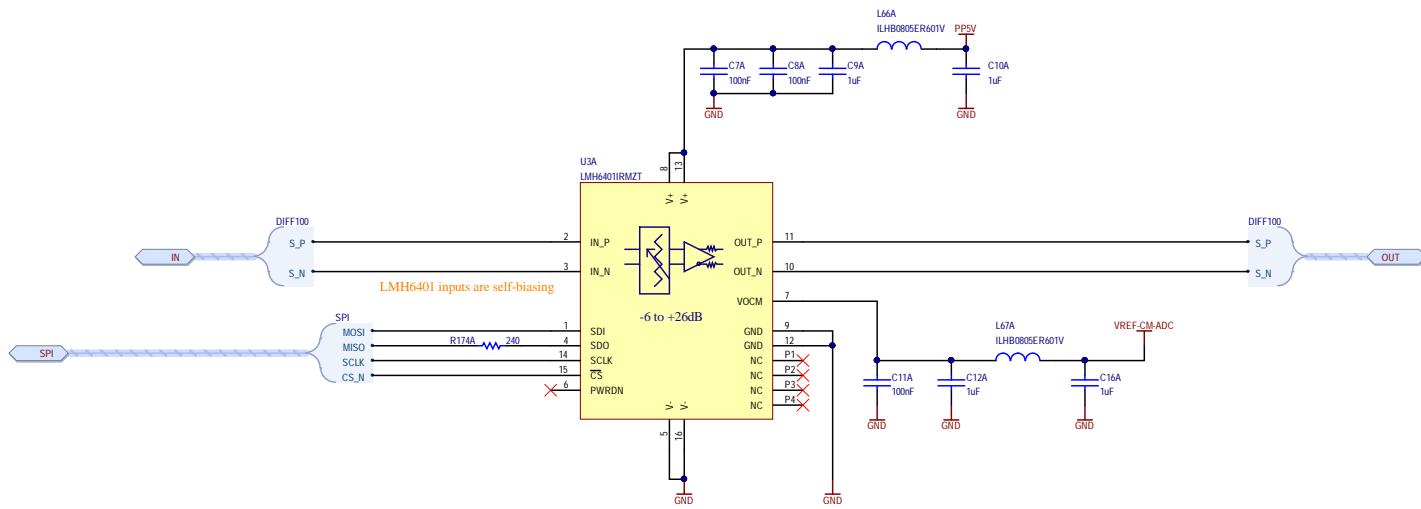
Title
Config FPGA - Misc

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Engineer	Drawn By	Checked By
E. Chiu	E. Chiu	J. Brinton
Revision 1	Sheet 36 of 58	Date 1/3/2017





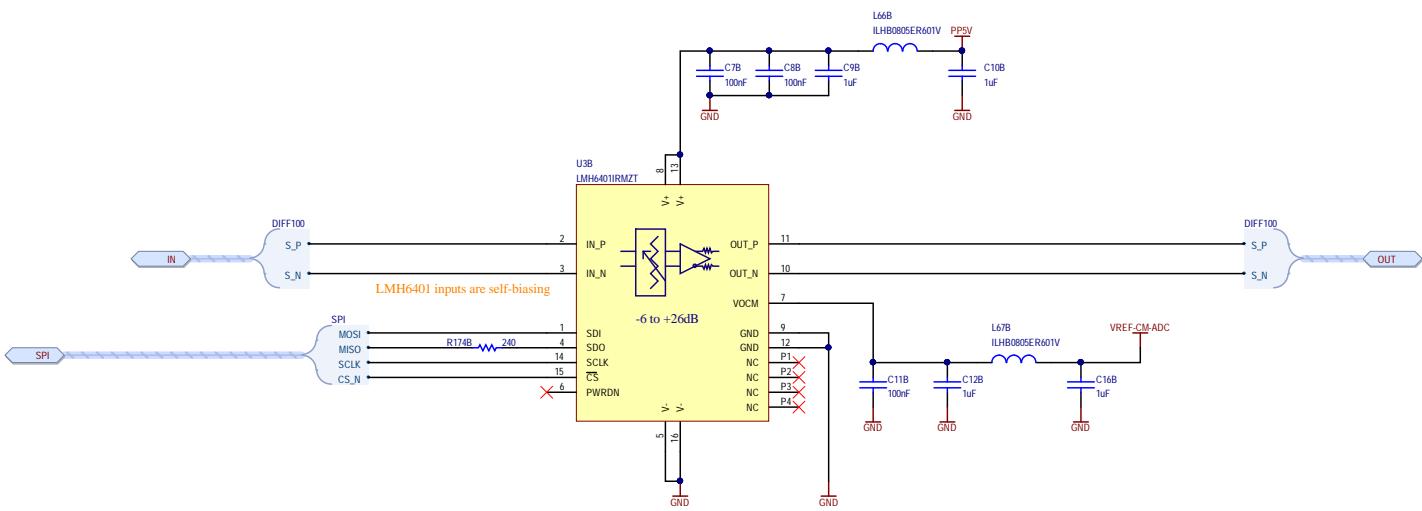


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Title
ADC Frontend

Engineer E. Chiu	Drawn By E. Chiu	Checked By J. Brinton
Revision 1	Sheet 40 of 58	Date 1/3/2017



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ADC Frontend

Engineer
E. Chiu

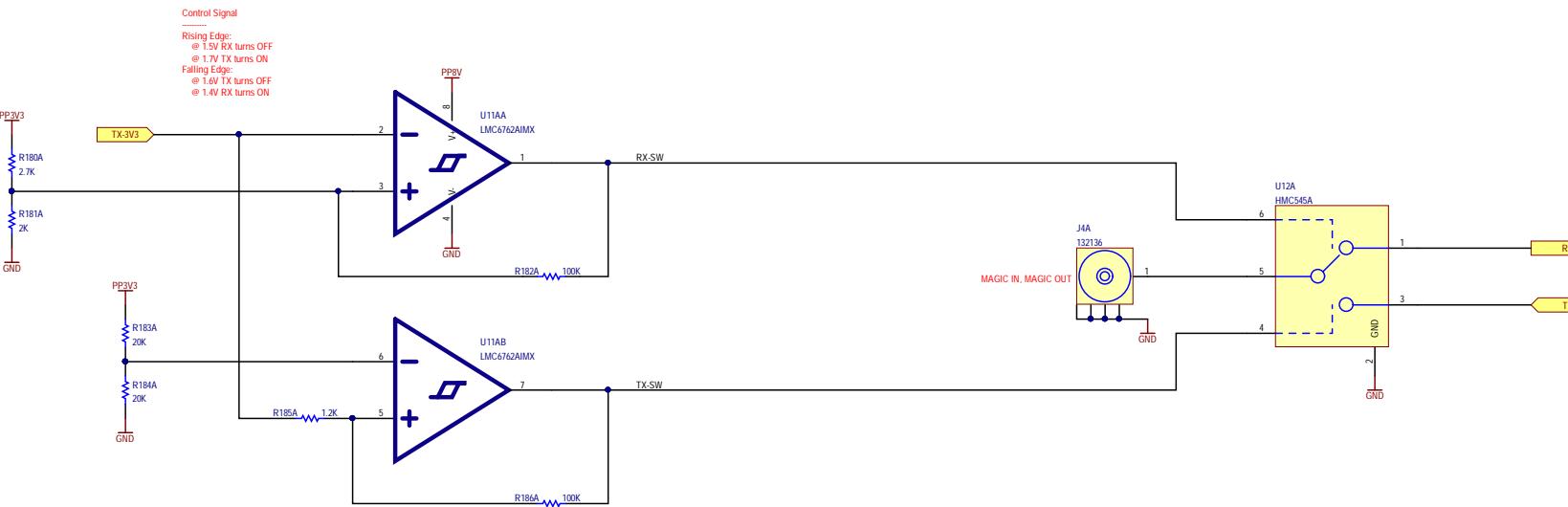
Drawn By
E. Chiu

Checked By
J. Brinton

Revision
1

Sheet 40 of 58

Date
1/3/2017



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Title
Antenna Switch

Engineer

E. Chiu

Drawn By

E. Chiu

Checked By

J. Brinton

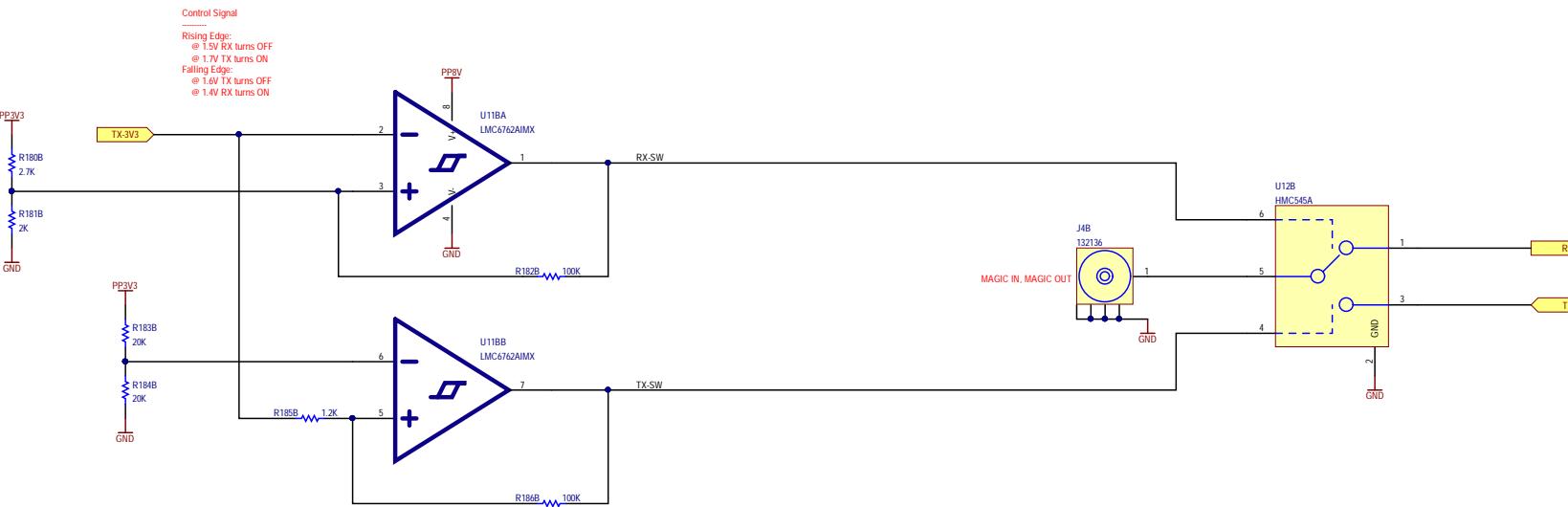
Revision

1

Sheet 41 of 58

Date

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Title
Antenna Switch

Engineer

E. Chiu

Drawn By

E. Chiu

Checked By

J. Brinton

Revision

1

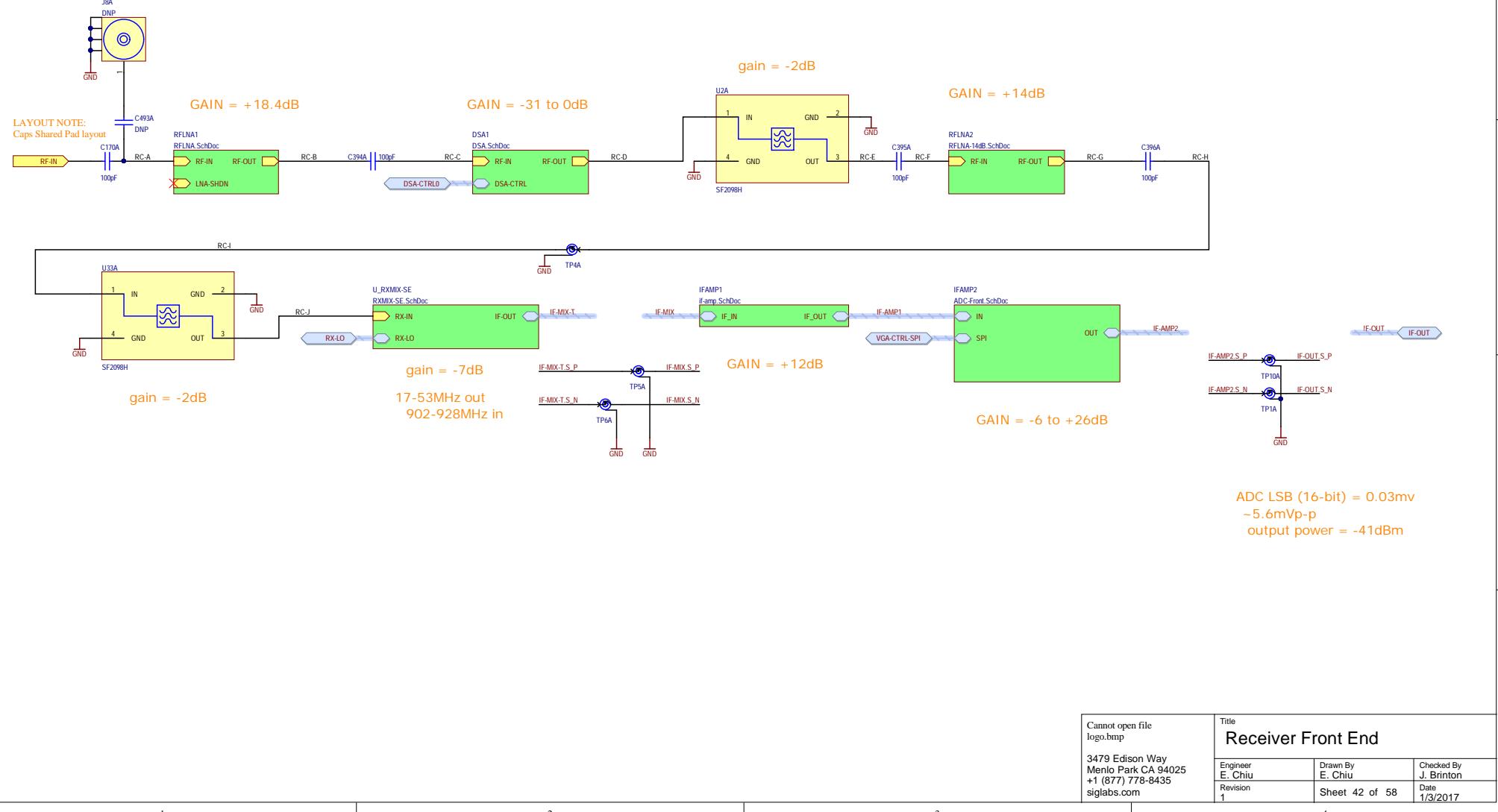
Sheet 41 of 58

Date

1/3/2017

1 2 3 4

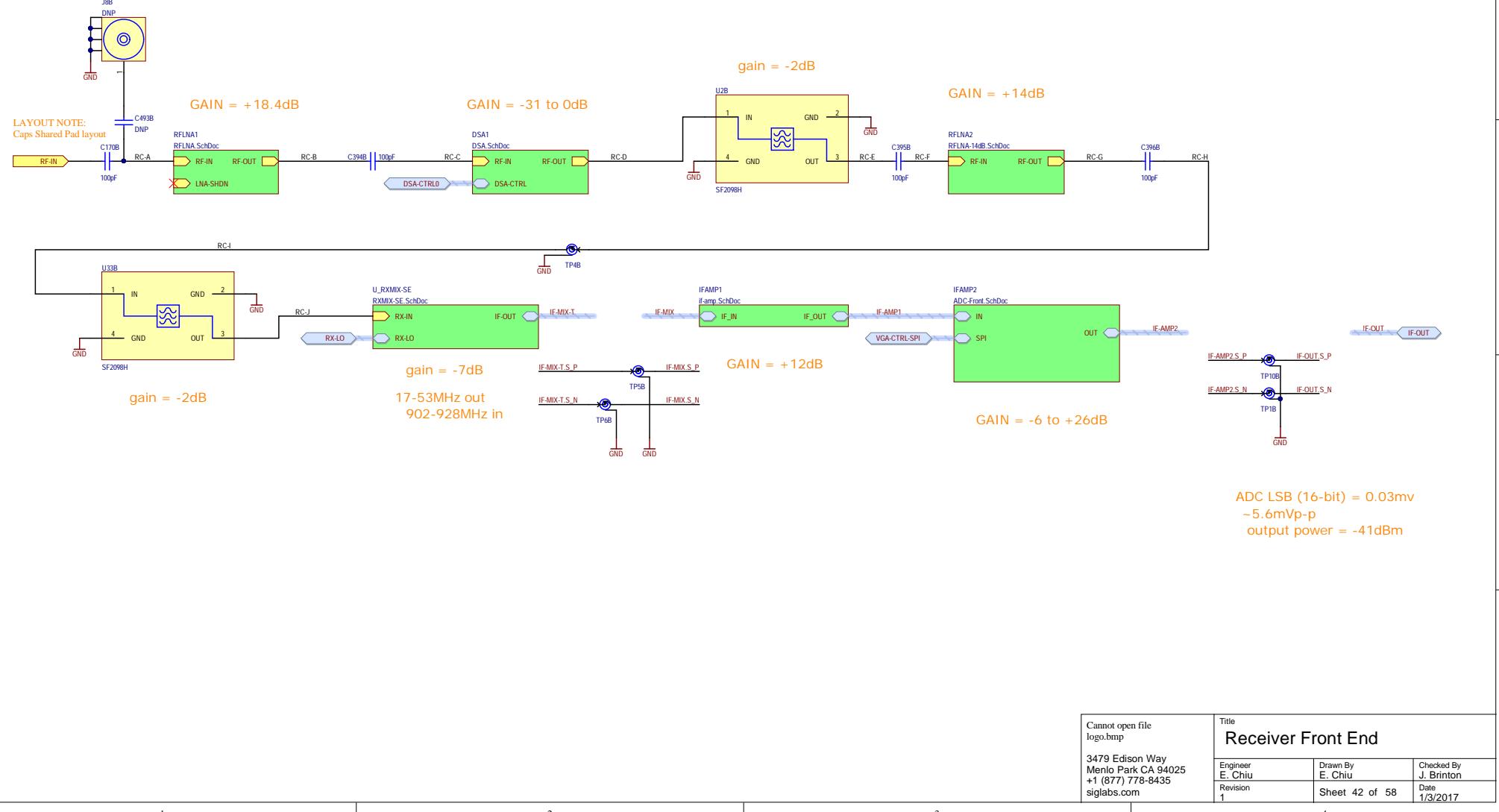
noise floor power @ 26MHz BW = -100dBm
loudest received signal - 16dBm



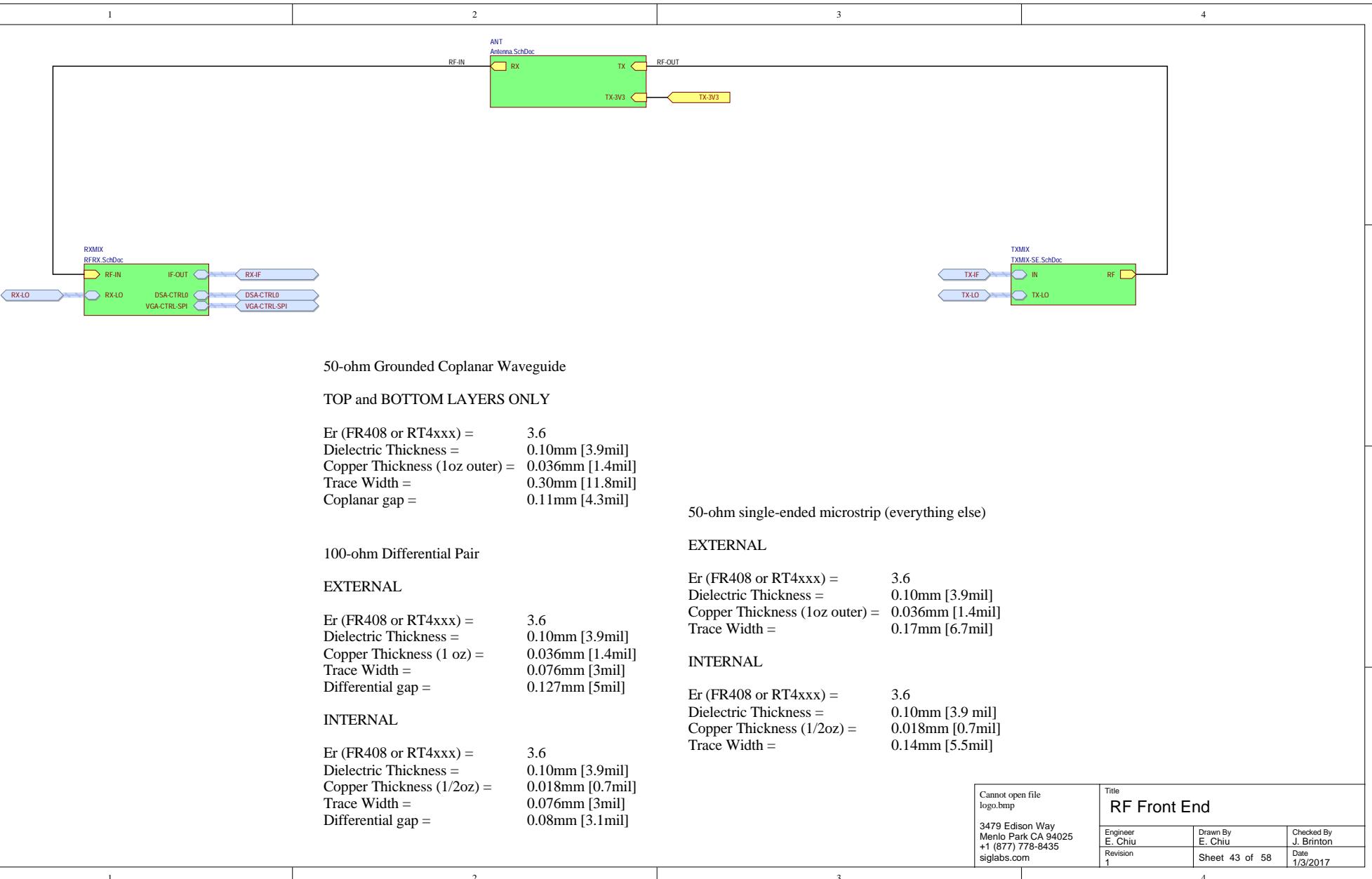
1 2 3 4

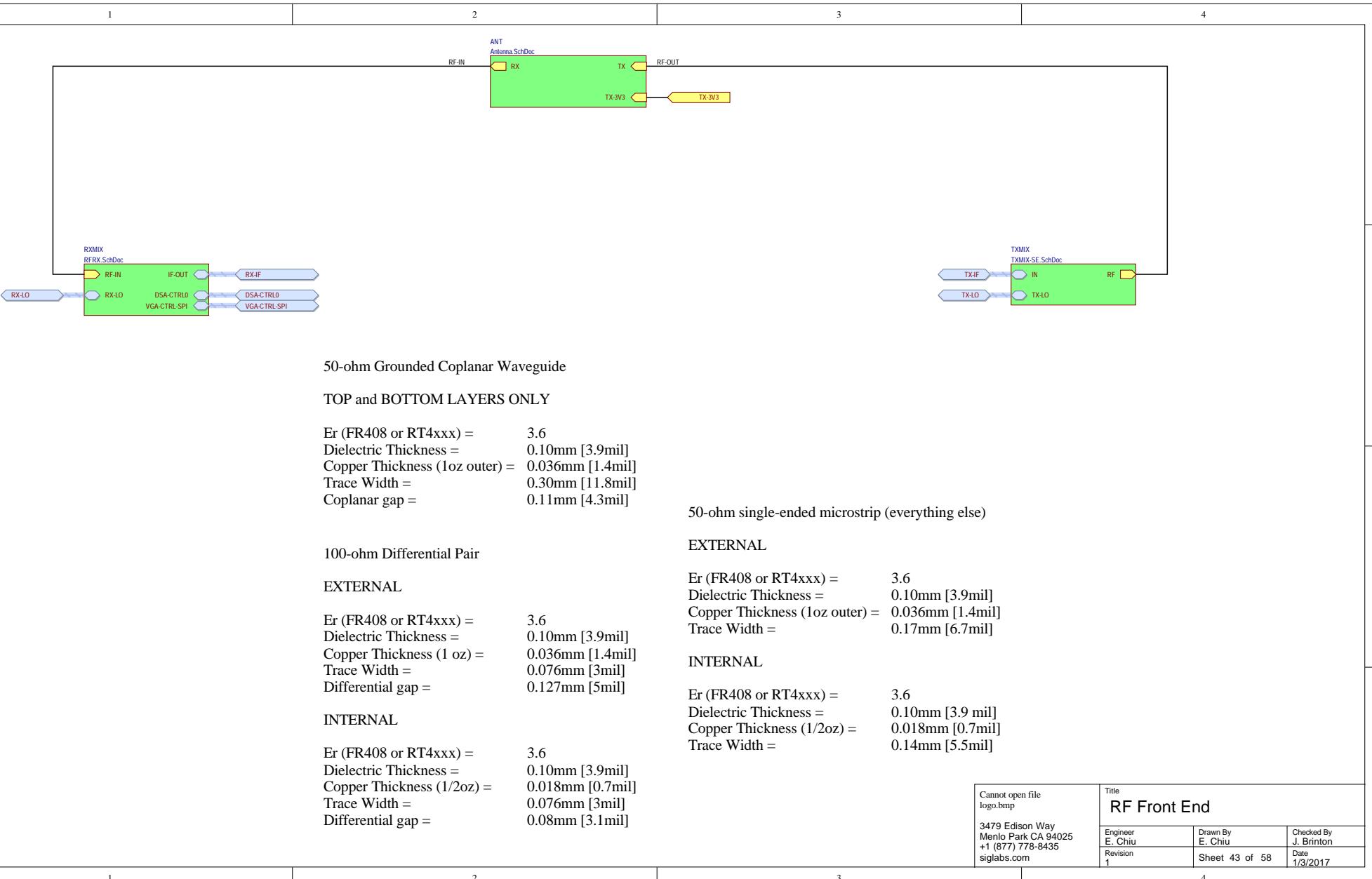
1 2 3 4

noise floor power @ 26MHz BW = -100dBm
loudest received signal - 16dBm

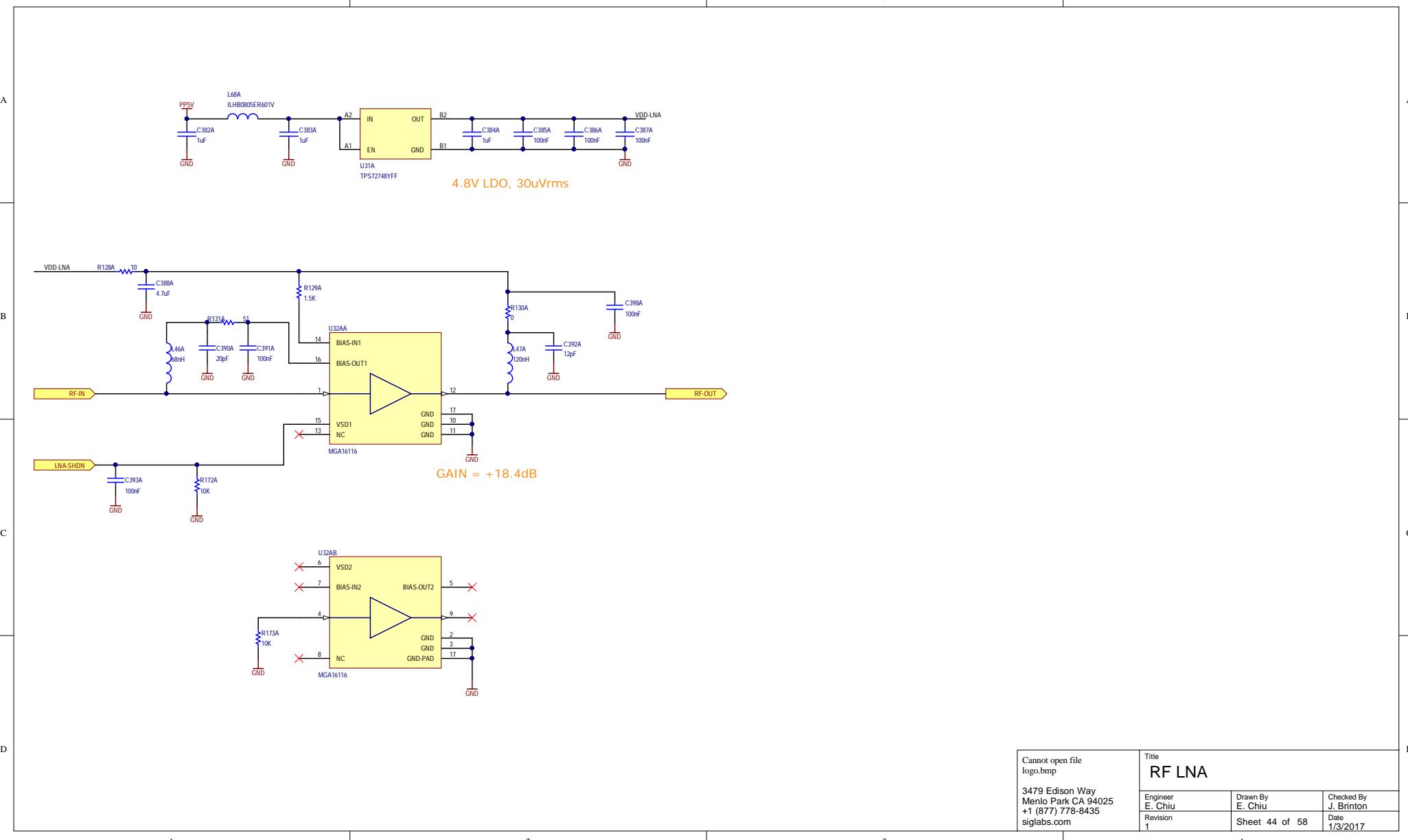


1 2 3 4



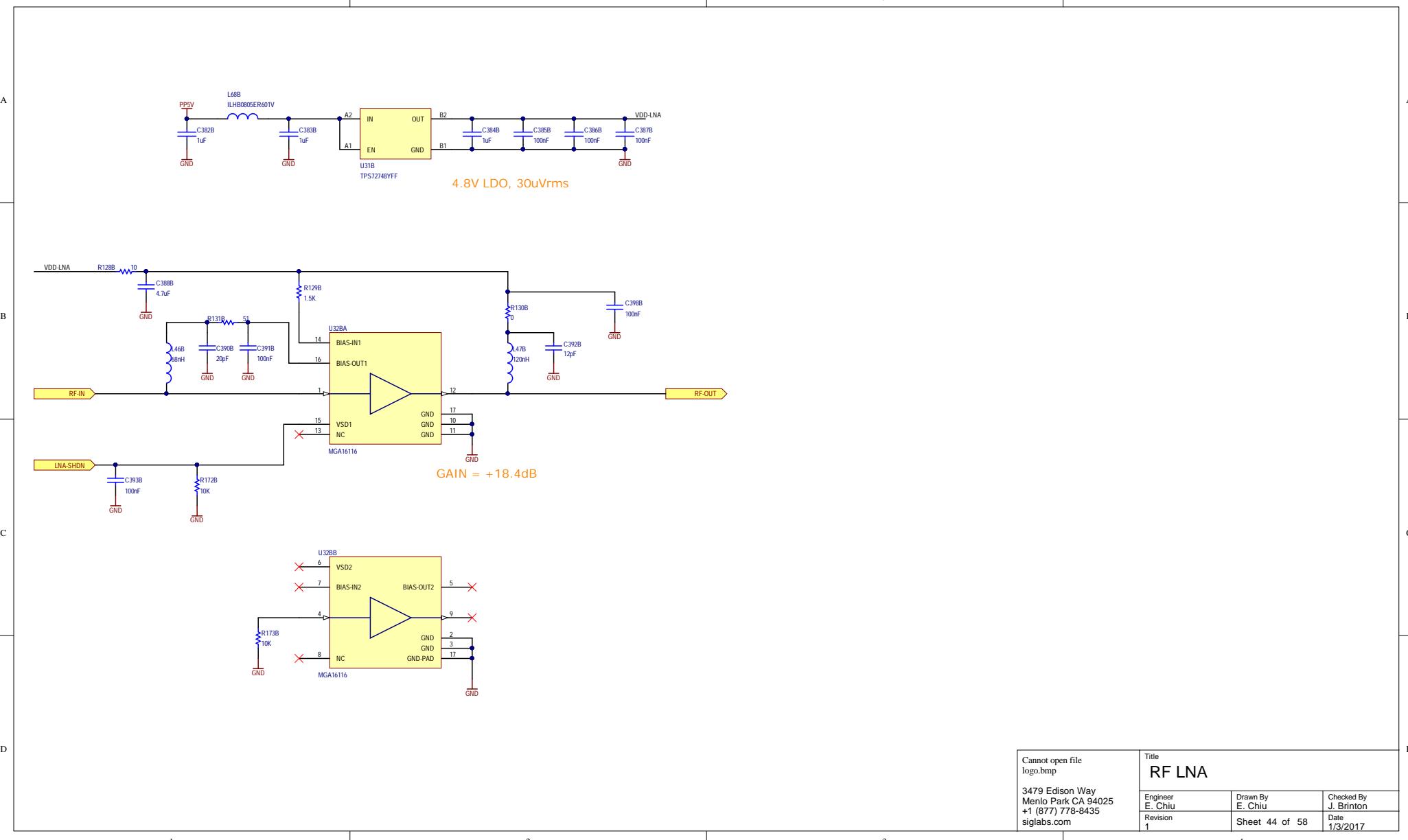


1 2 3 4

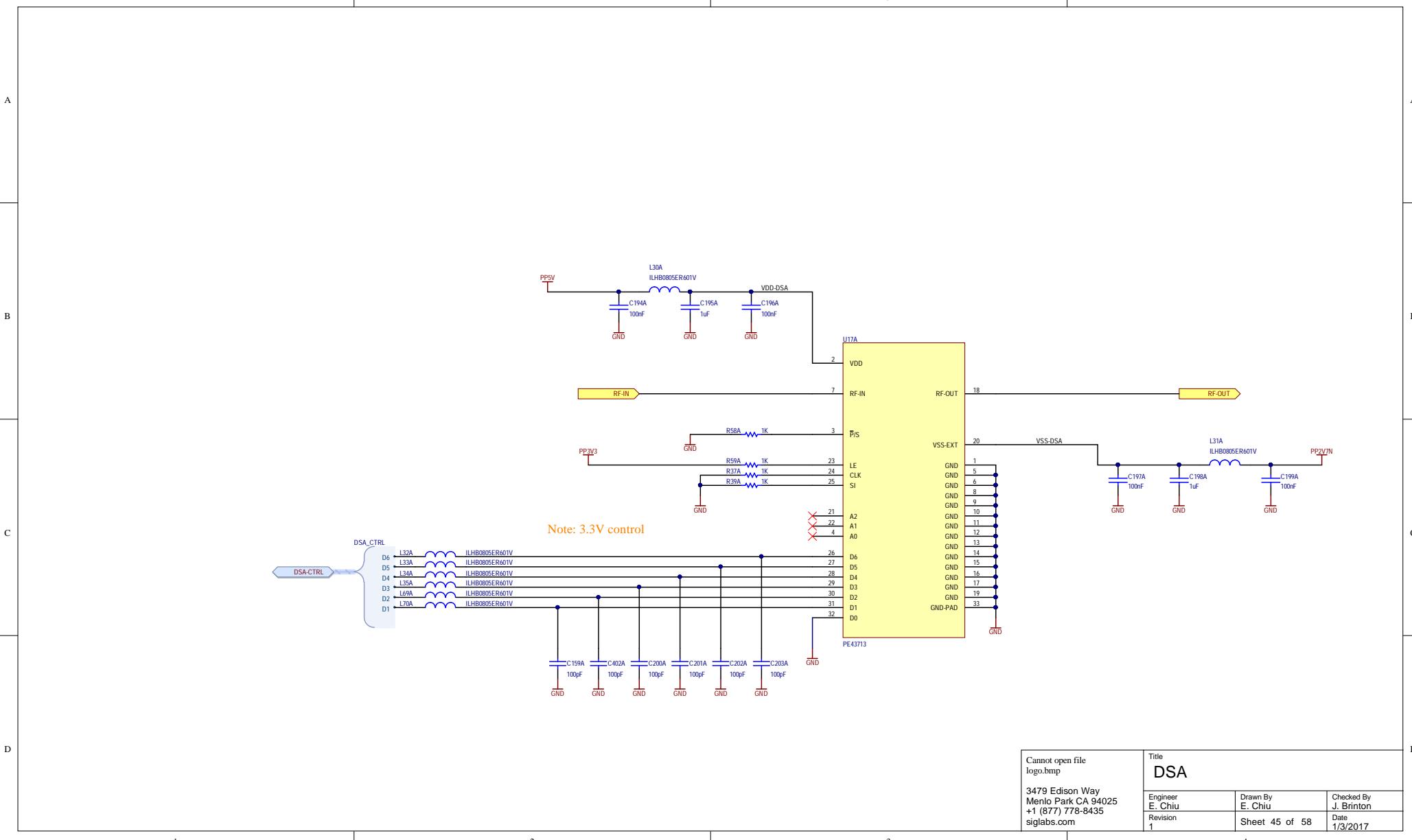


1 2 3 4

1 2 3 4



1 2 3 4



A

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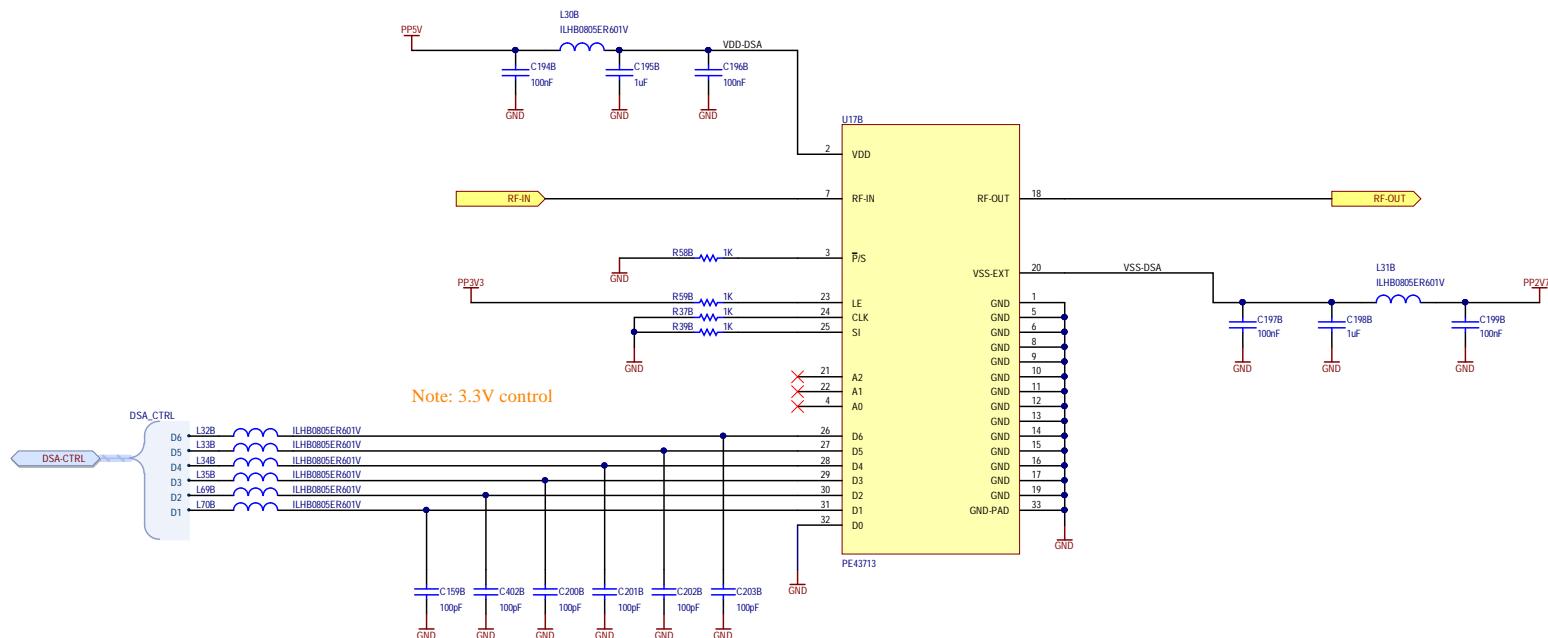
C

D

B

C

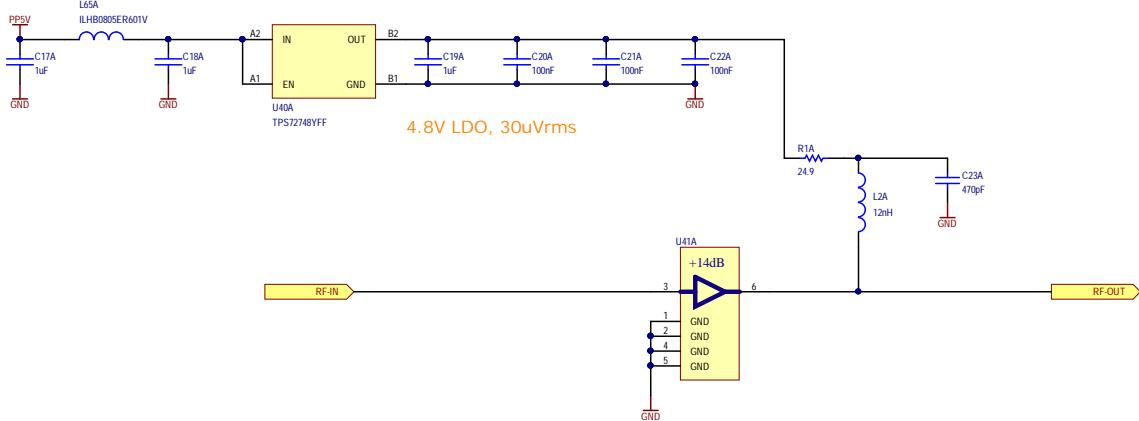
D



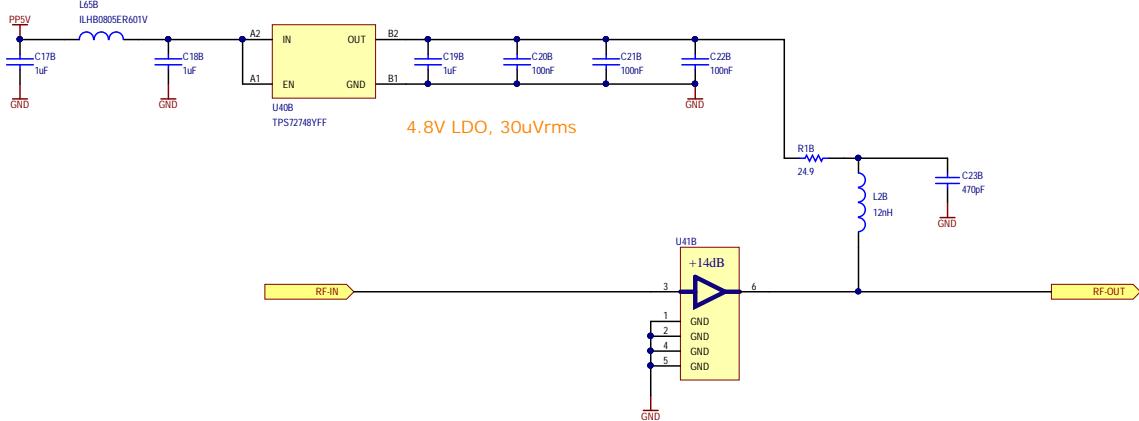
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Cannot open file logo.bmp	Title 14dB LNA	
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Revision 1	Sheet 46 of 58	Checked By J. Brinton
	Date 1/3/2017	



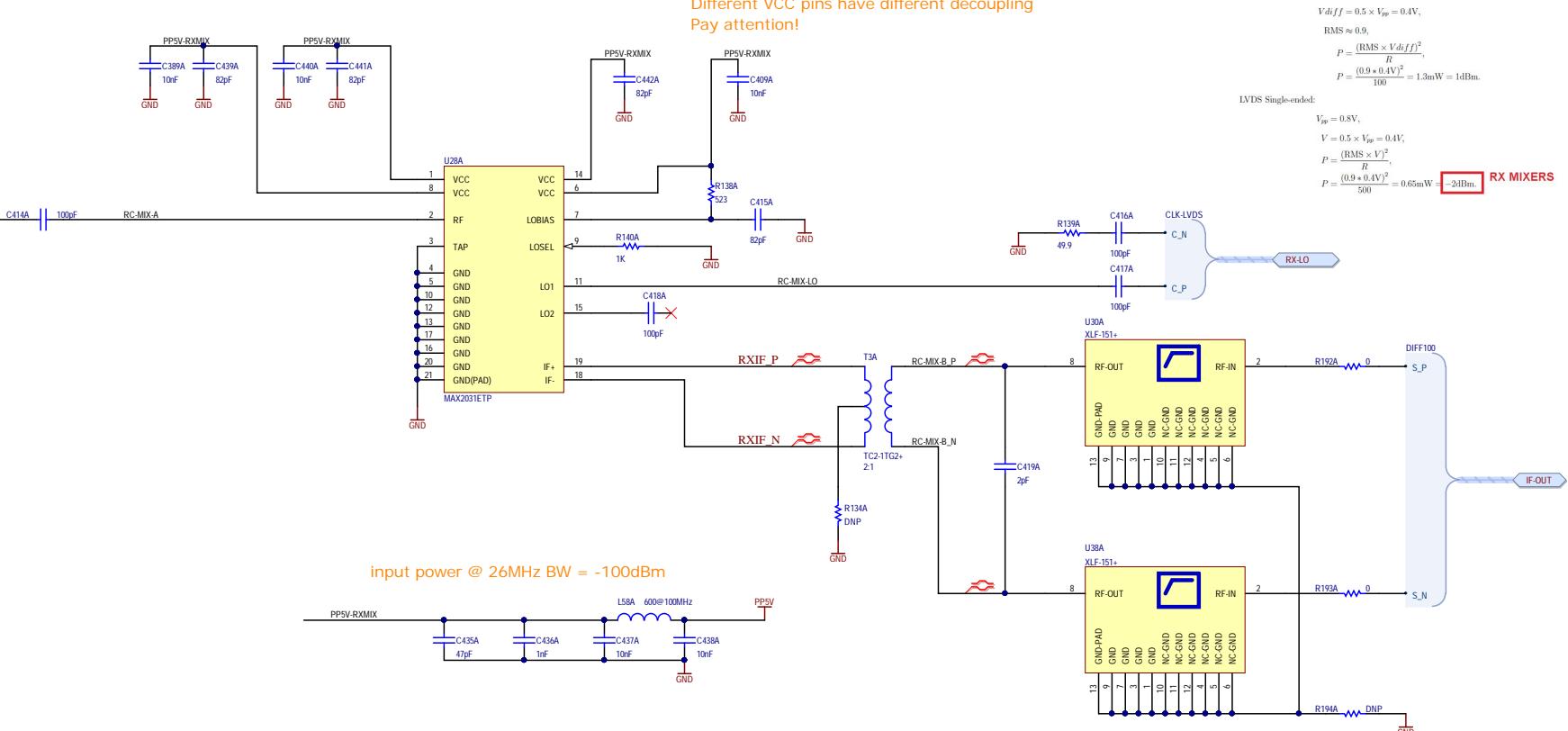
Cannot open file logo.bmp	Title 14dB LNA	
3479 Edison Way Menlo Park CA 94025 +1 (877) 778-8435 siglabs.com	Engineer E. Chiu	Drawn By E. Chiu
Revision 1	Sheet 46 of 58	Checked By J. Brinton Date 1/3/2017

1

2

3

4



input power @ 26MHz BW = -100dBm

1

2

3

4

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Title
Receiver Mixer

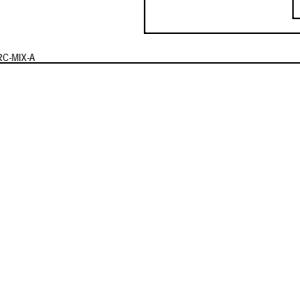
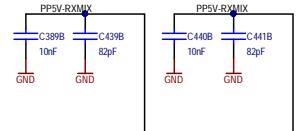
Engineer E. Chiu	Drawn By E. Chiu	Checked By J. Brinton
Revision 1	Sheet 47 of 58	Date 1/3/2017

1

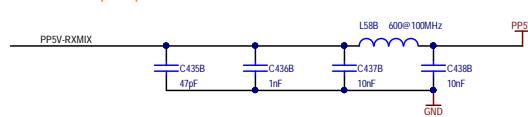
2

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4



input power @ 26MHz BW = -100dBm



LAYOUT NOTE:
Different VCC pins have different decoupling
Pay attention!

target LO = 0dBm
actual = -3 to -2dBm

LVDS Differential-ended:

$$V_{diff} = 0.8V,$$

$$V_{diff} = 0.5 \times V_{pp} = 0.4V,$$

RMS ≈ 0.9 ,

$$P = \frac{(RMS \times V_{diff})^2}{R},$$

$$P = \frac{(0.9 \times 0.4V)^2}{100} = 1.3mW = 1dBm.$$

LVDS Single-ended:

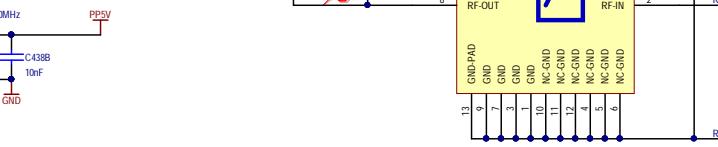
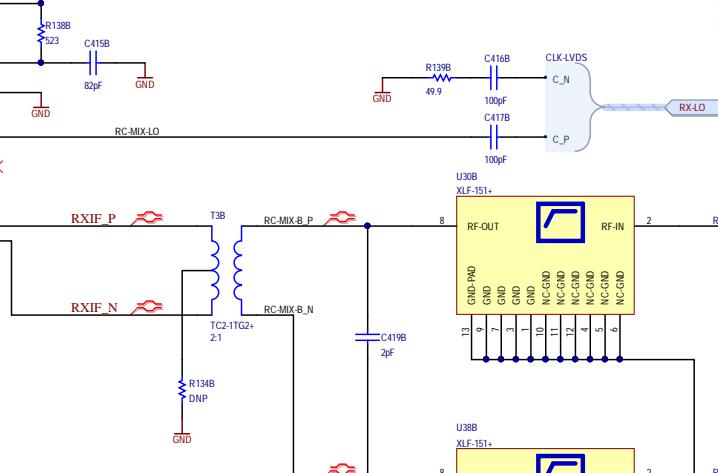
$$V_{pp} = 0.8V,$$

$$V = 0.5 \times V_{pp} = 0.4V,$$

P = $\frac{(RMS \times V)^2}{R}$,

$$P = \frac{(0.9 \times 0.4V)^2}{500} = 0.65mW = -2dBm.$$

RX MIXERS



DIFF100 S_P

IF-OUT

S_N

IF-OUT

S_N

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Title
Receiver Mixer

Engineer

E. Chiu

Drawn By

E. Chiu

Checked By

J. Brinton

Revision

1

Date

1/3/2017

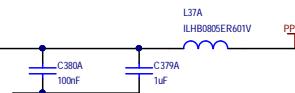
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2

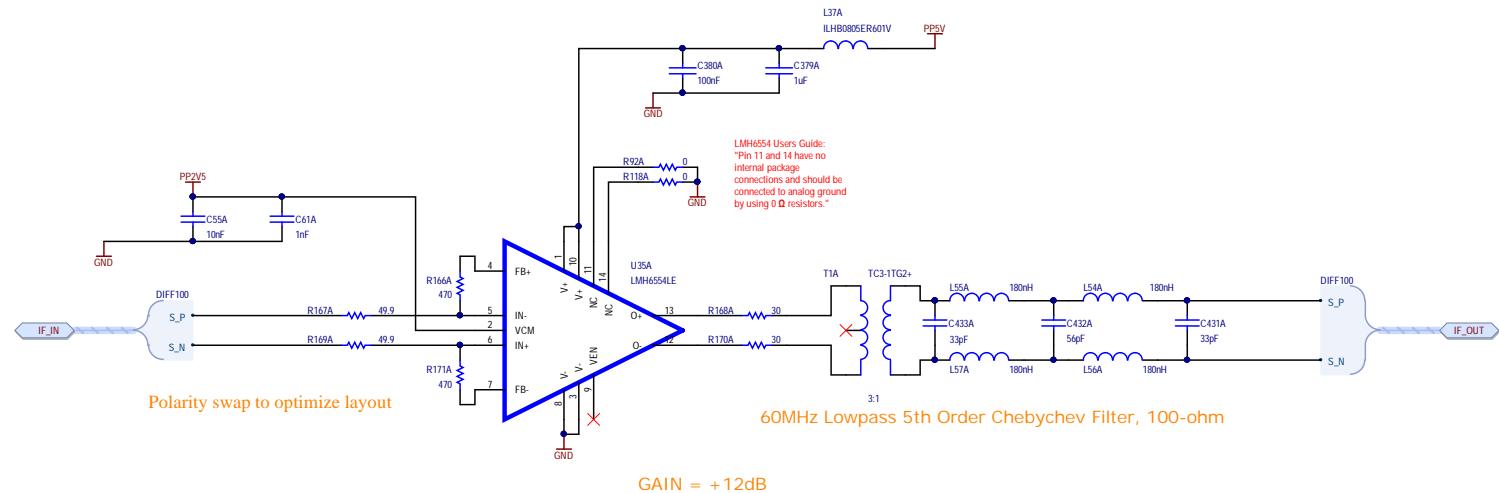
3

4

A



LMH6554 Users Guide:
"Pin 11 and 14 have no
internal package
connections and should be
connected to analog ground
by using 0 Ω resistors."



B

A

B

C

D

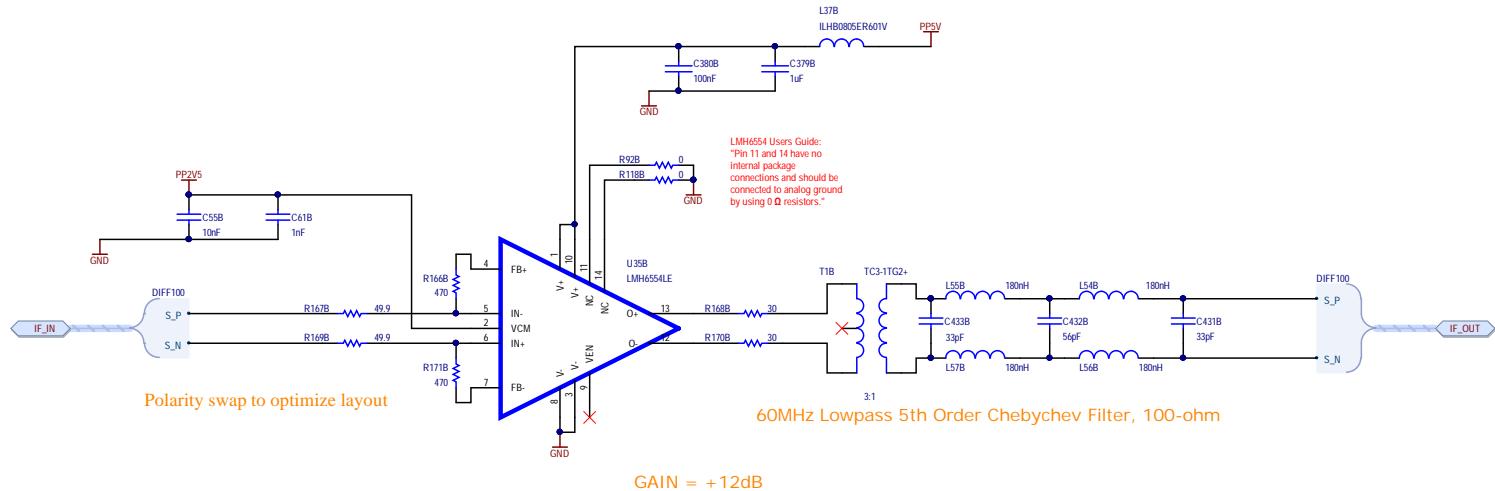
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Title IF Amplifier

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Engineer E. Chiu	Drawn By E. Chiu	Checked By J. Brinton
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A



B

A

B

C

D

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Title
IF Amplifier

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Engineer
E. Chiu

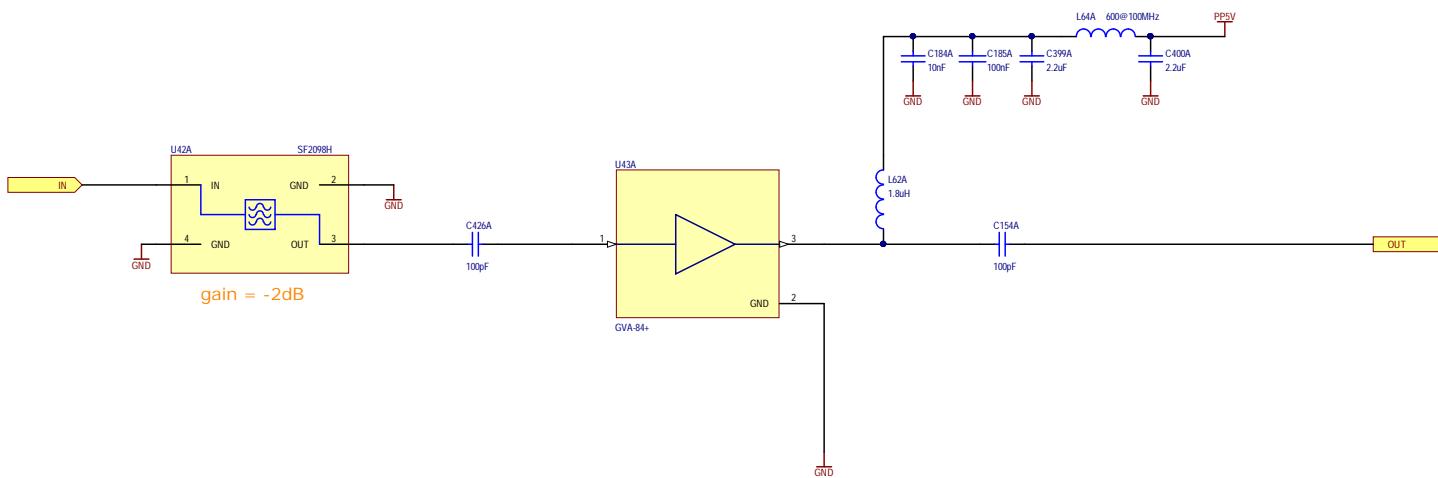
Drawn By
E. Chiu

Checked By
J. Brinton

Revision
1

Sheet 48 of 58

Date
1/3/2017

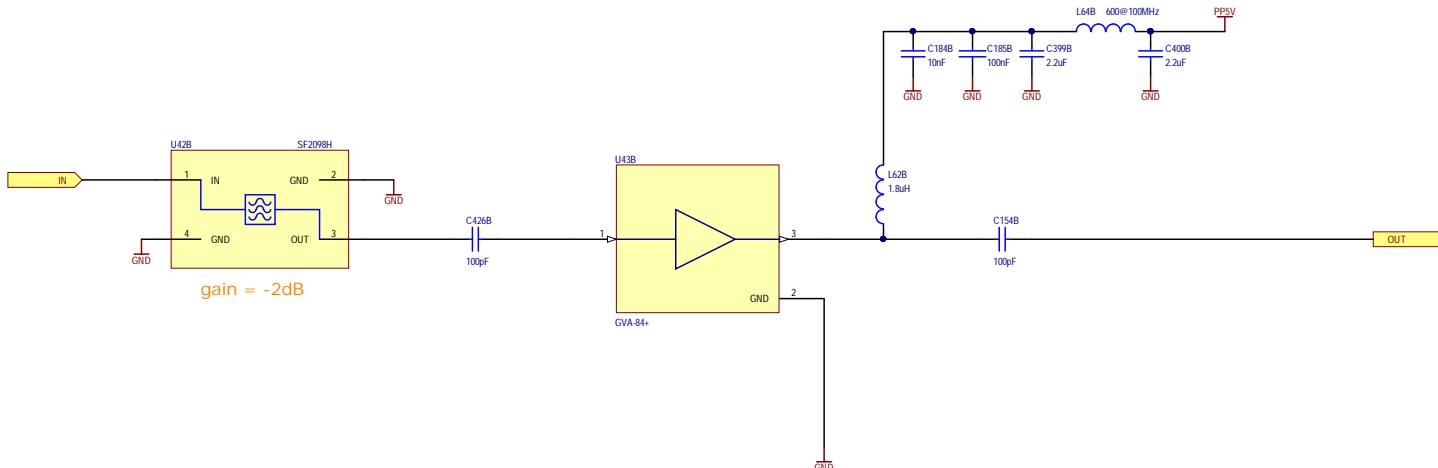


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Title
Transmitter PA #2

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Title Transmitter PA #2

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Engineer

E. Chiu

Drawn By

E. Chiu

Checked By
J. Brinton

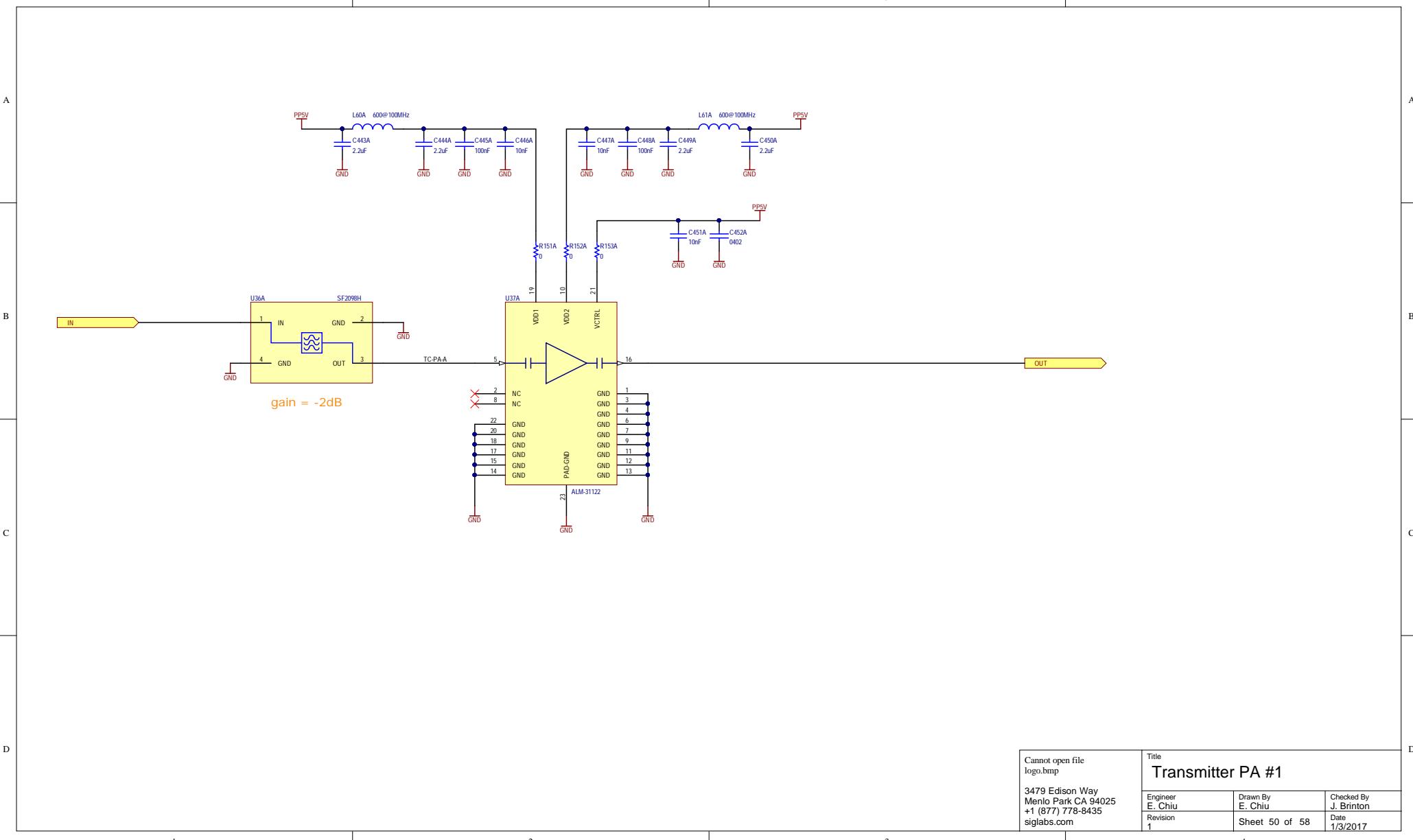
Revision

1

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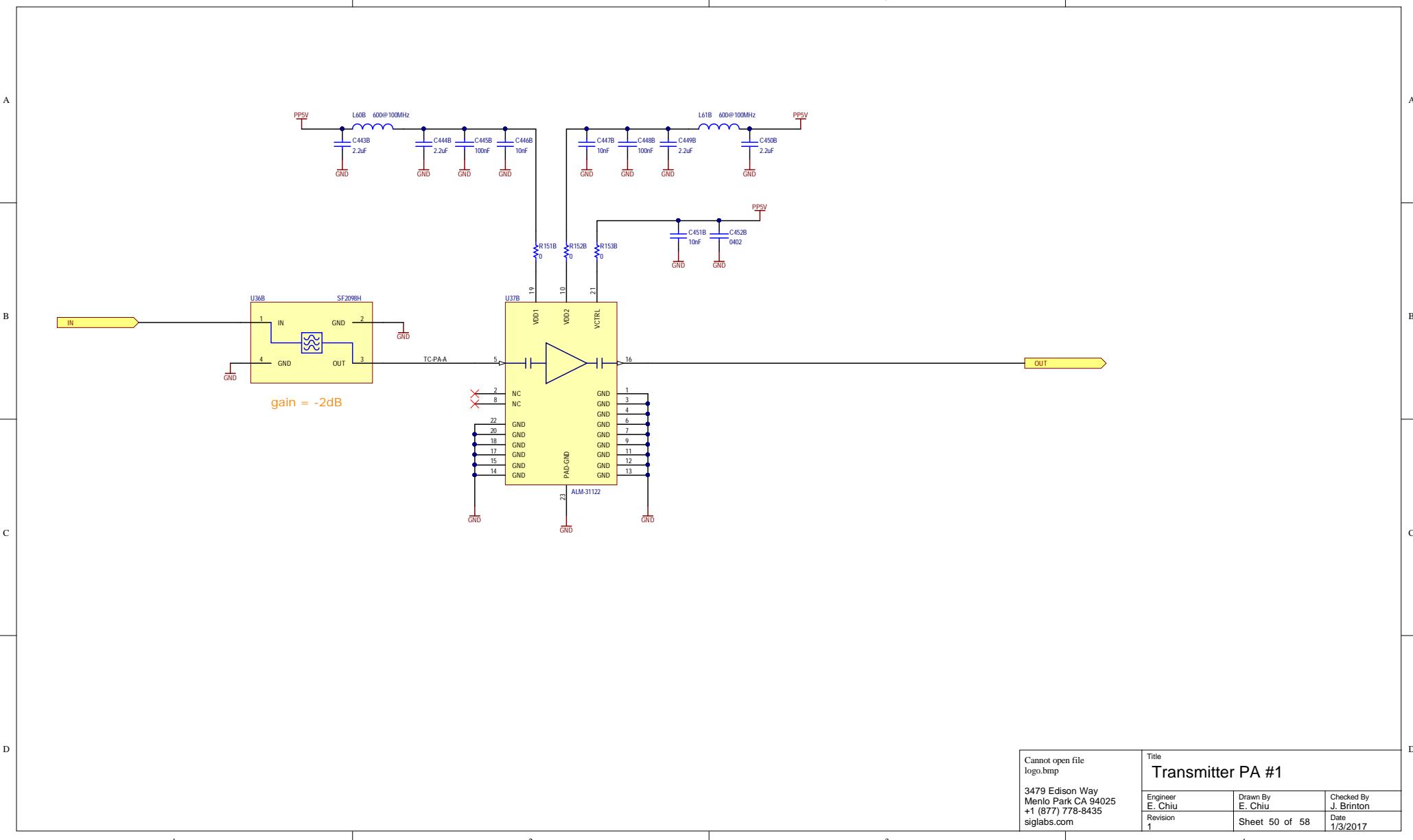
Date
1/3/2017

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1 2 3 4

1 2 3 4



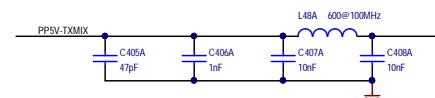
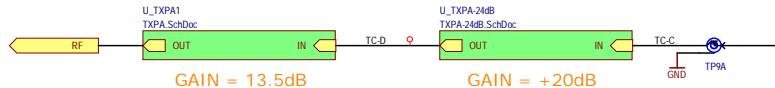
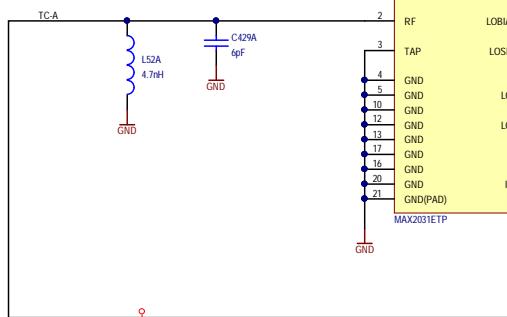
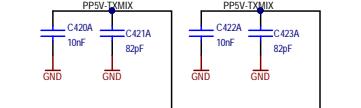
1 2 3 4

1

2

3

4



input power @ 26MHz BW = -100dBm

LAYOUT NOTE:
Different VCC pins have different decoupling
Pay attention!

target LO = 0dBm, actual = 3-4dBm

LVPECL33 Differential-ended:

$$V_{diff,pp} = 1.6V,$$

$$V_{diff} = 0.5 \times V_{pp} = 0.8V,$$

RMS ≈ 0.9,

$$P = (\text{RMS} \times V_{diff})^2 / R,$$

$$P = \frac{(0.9 \times 0.8V)^2}{100} = 5mW = 7dBm.$$

LVPECL33 Single-ended:

$$V_{pp} = 0.8V,$$

$$V = 0.5 \times V_{pp} = 0.4V,$$

P = $\frac{(\text{RMS} \times V)^2}{R}$,

$$P = \frac{(0.9 \times 0.4V)^2}{500} = 2.5mW = 4dBm.$$

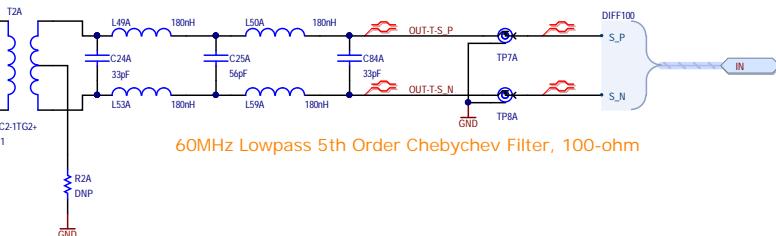
TX MIXERS



Note in the PCB one of these
transformers is mirrored to optimize routing



60MHz Lowpass 5th Order Chebychev Filter, 100-ohm



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Title
Transmitter Mixer

Engineer
E. Chiu

Drawn By
E. Chiu

Checked By
J. Brinton

Revision
1

Date
1/3/2017

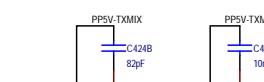
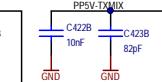
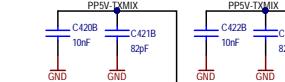
1

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1 2 3 4



target LO = 0dBm, actual = 3-4dBm

LVPECL33 Differential-ended:

$$V_{diff,pp} = 1.6V,$$

$$V_{diff} = 0.5 \times V_{pp} = 0.8V,$$

RMS ≈ 0.9,

$$P = (\text{RMS} \times V_{diff})^2 / R,$$

$$P = \frac{(0.9 \times 0.8V)^2}{100} = 5mW = 7dBm.$$

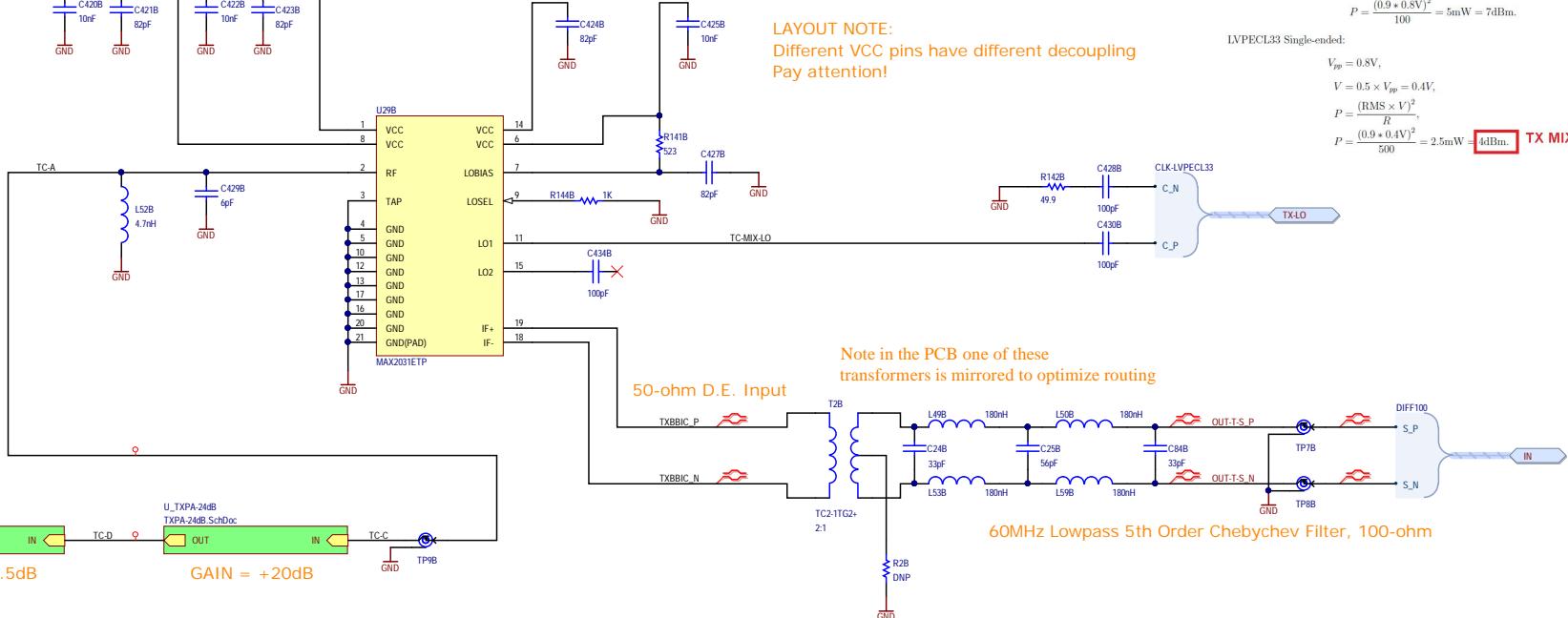
LVPECL33 Single-ended:

$$V_{pp} = 0.8V,$$

$$V = 0.5 \times V_{pp} = 0.4V,$$

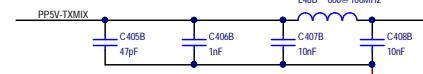
$$P = \frac{(\text{RMS} \times V)^2}{R},$$

$$P = \frac{(0.9 \times 0.4V)^2}{500} = 2.5mW = 4dBm. \quad \text{TX MIXERS}$$



GAIN = 13.5dB

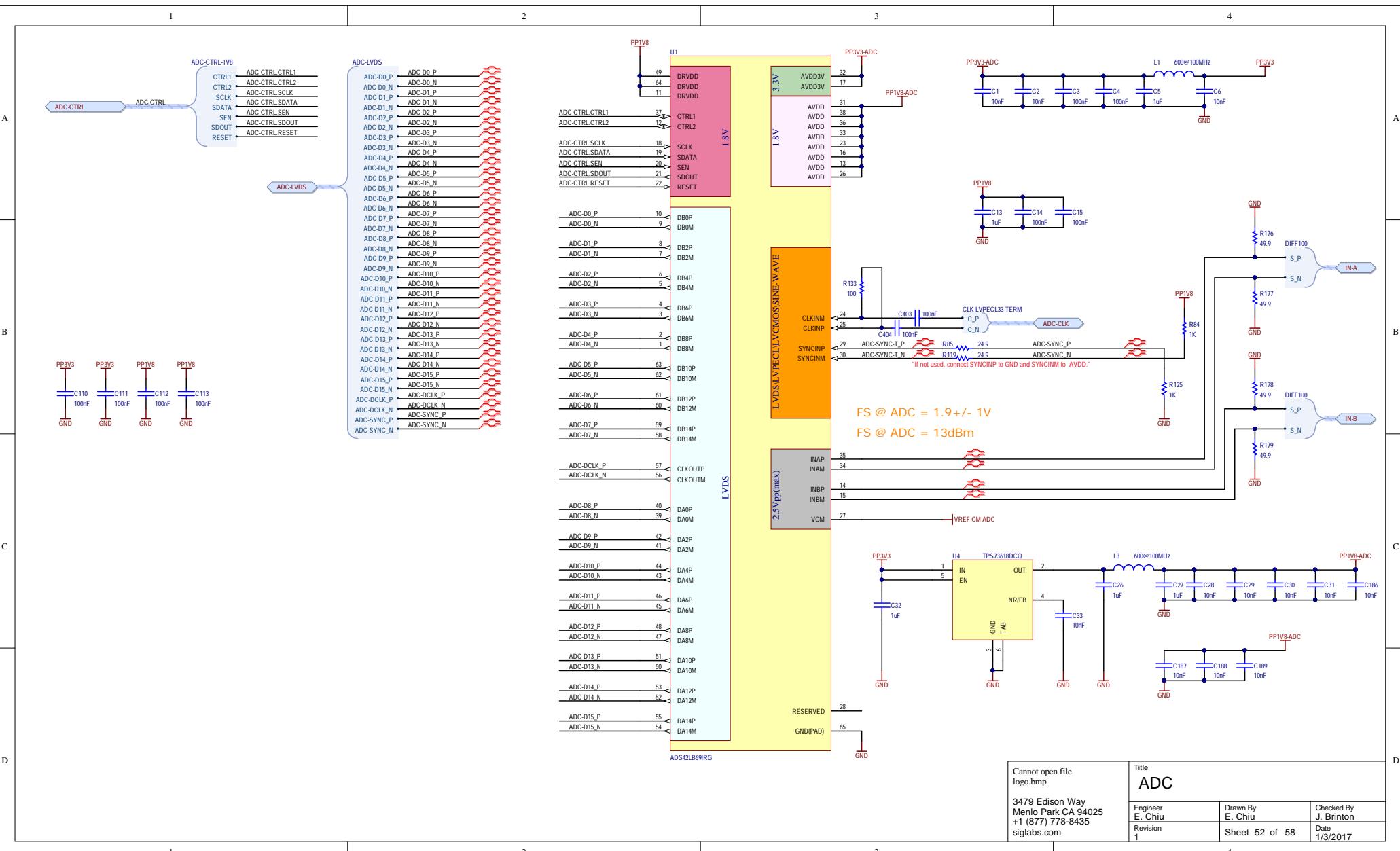
GAIN = +20dB

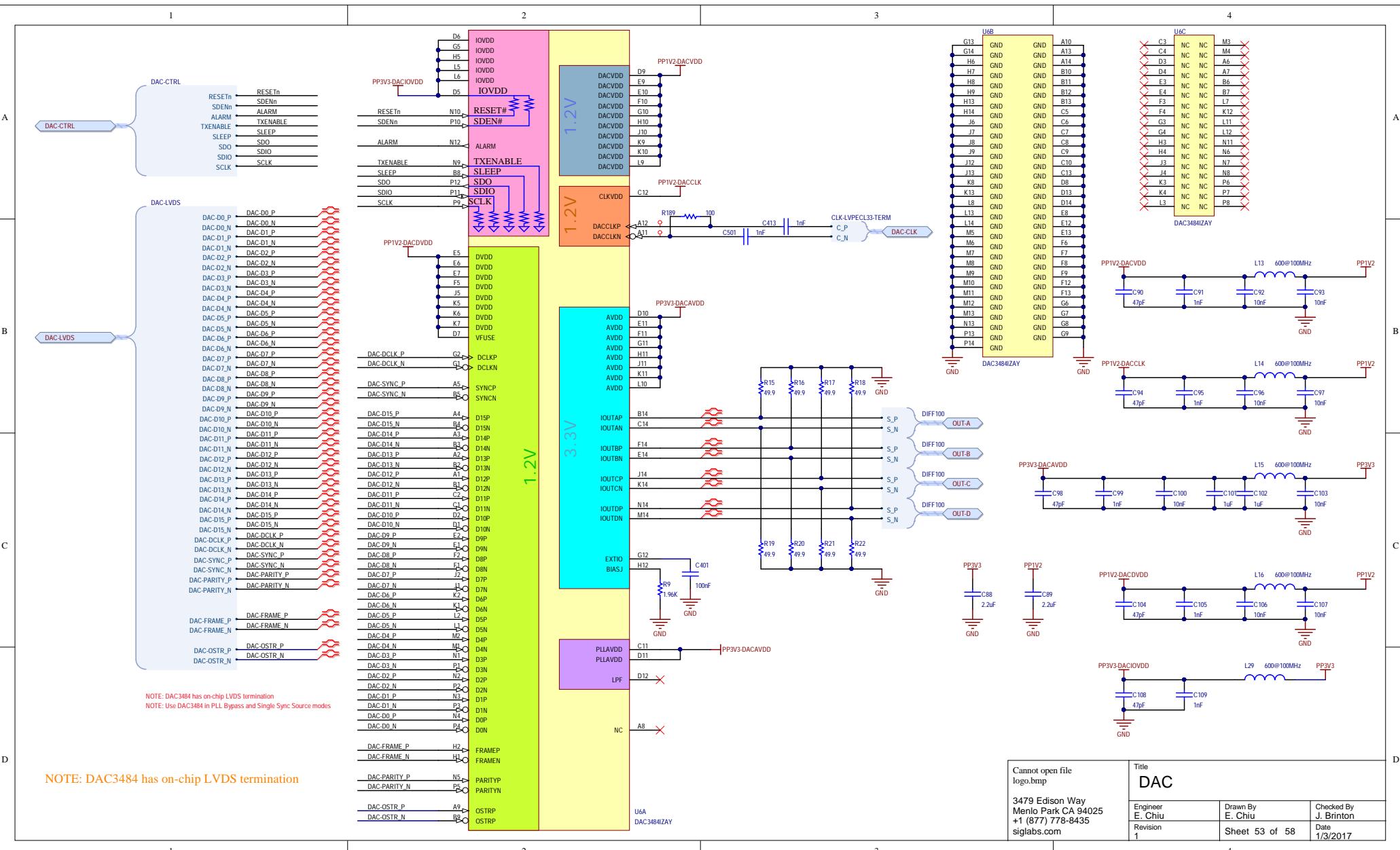


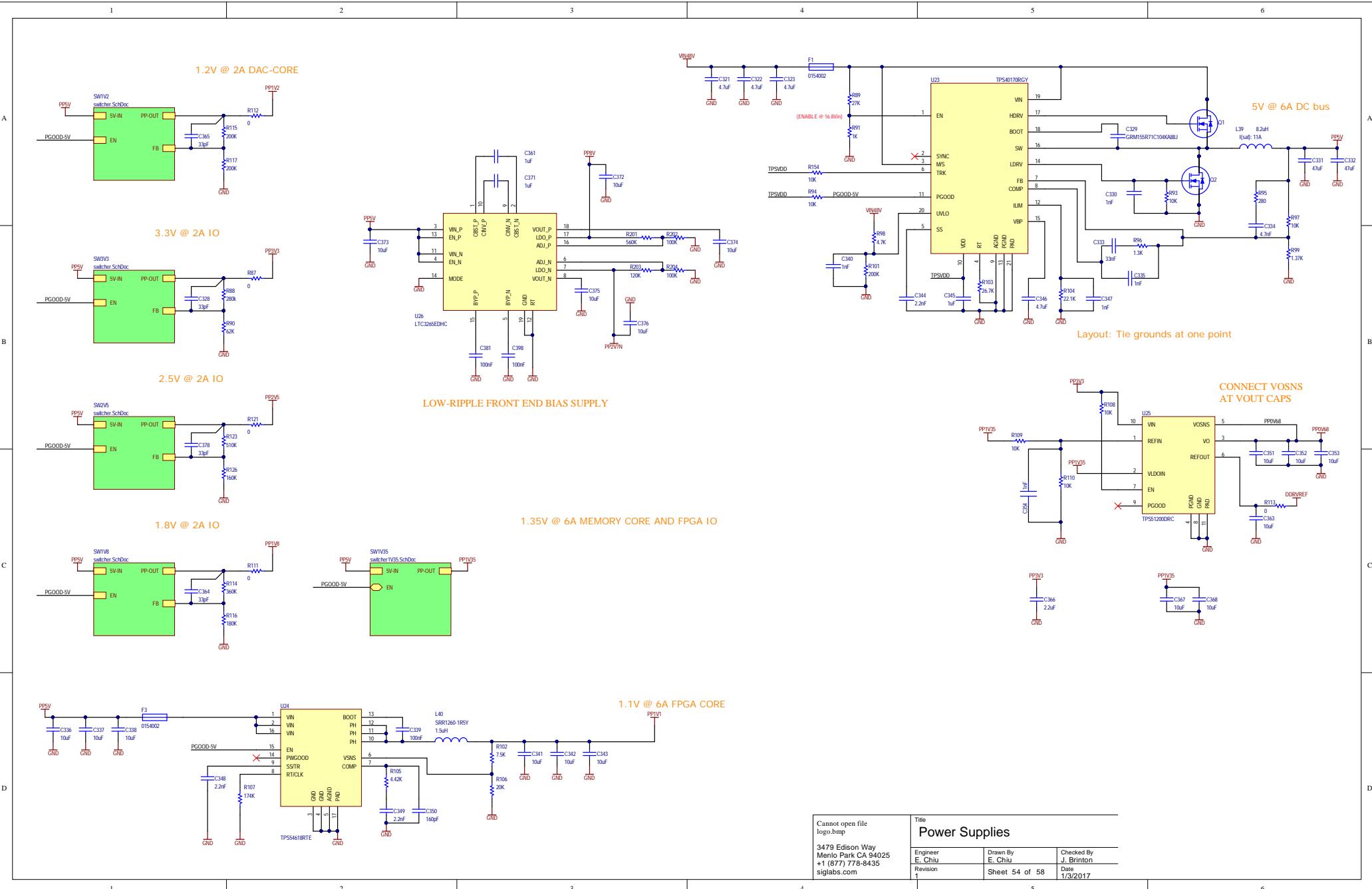
input power @ 26MHz BW = -100dBm

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Transmitter Mixer3479 Edison Way
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Revision 1 Sheet 51 of 58 Date 1/3/2017

1 2 3 4







A

B

C

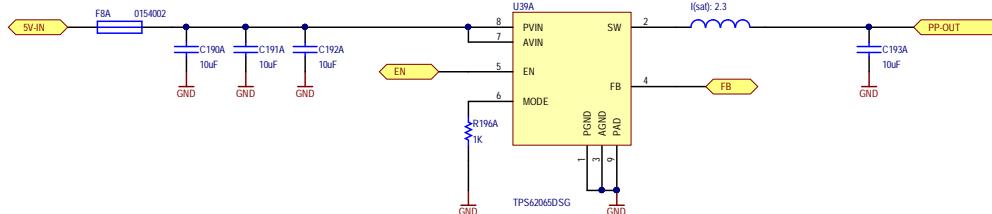
D

A

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Title
Switching Power Supply

Engineer E. Chiu	Drawn By E. Chiu	Checked By J. Brinton
Revision 1	Sheet 55 of 58	Date 1/3/2017

A

B

C

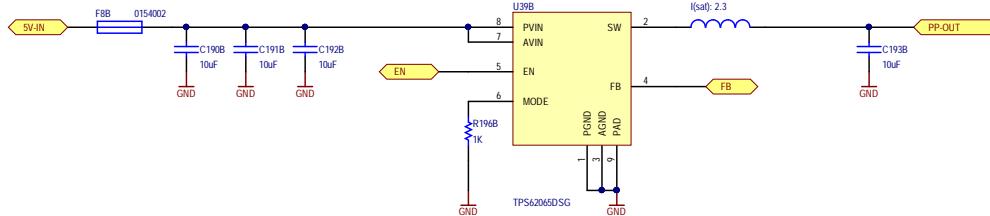
D

A

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Title
Switching Power Supply

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A

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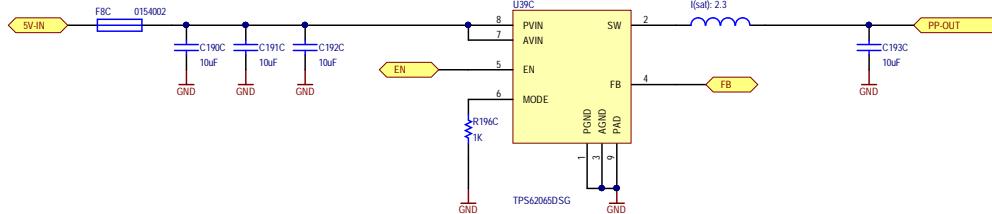
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Title
Switching Power Supply

Engineer E. Chiu	Drawn By E. Chiu	Checked By J. Brinton
Revision 1	Sheet 55 of 58	
	Date 1/3/2017	

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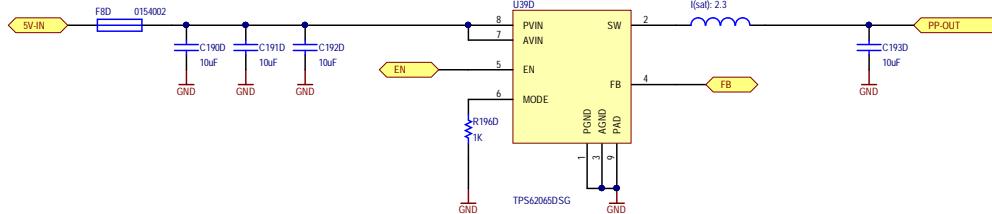
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Title
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Engineer E. Chiu	Drawn By E. Chiu	Checked By J. Brinton
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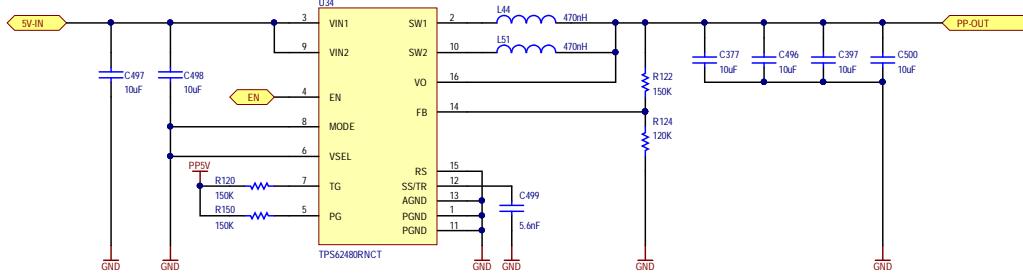
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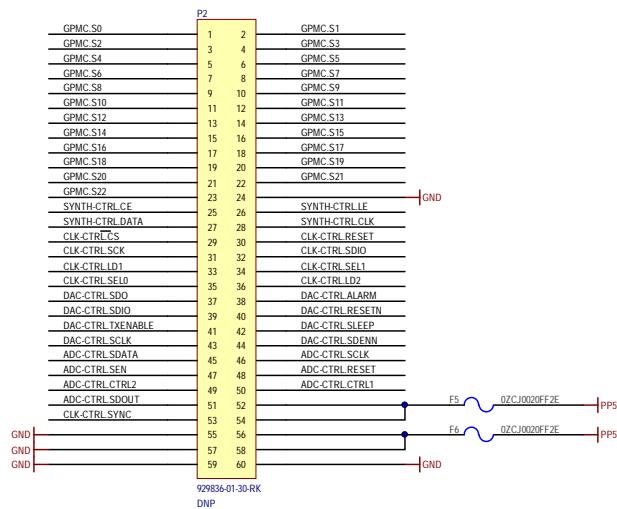
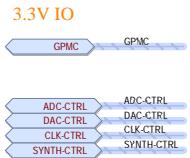
1.35V Supply

Engineer
E. Chiu
Revision
1

Drawn By
E. Chiu
Sheet 56 of 58

Checked By
J. Brinton
Date
1/3/2017

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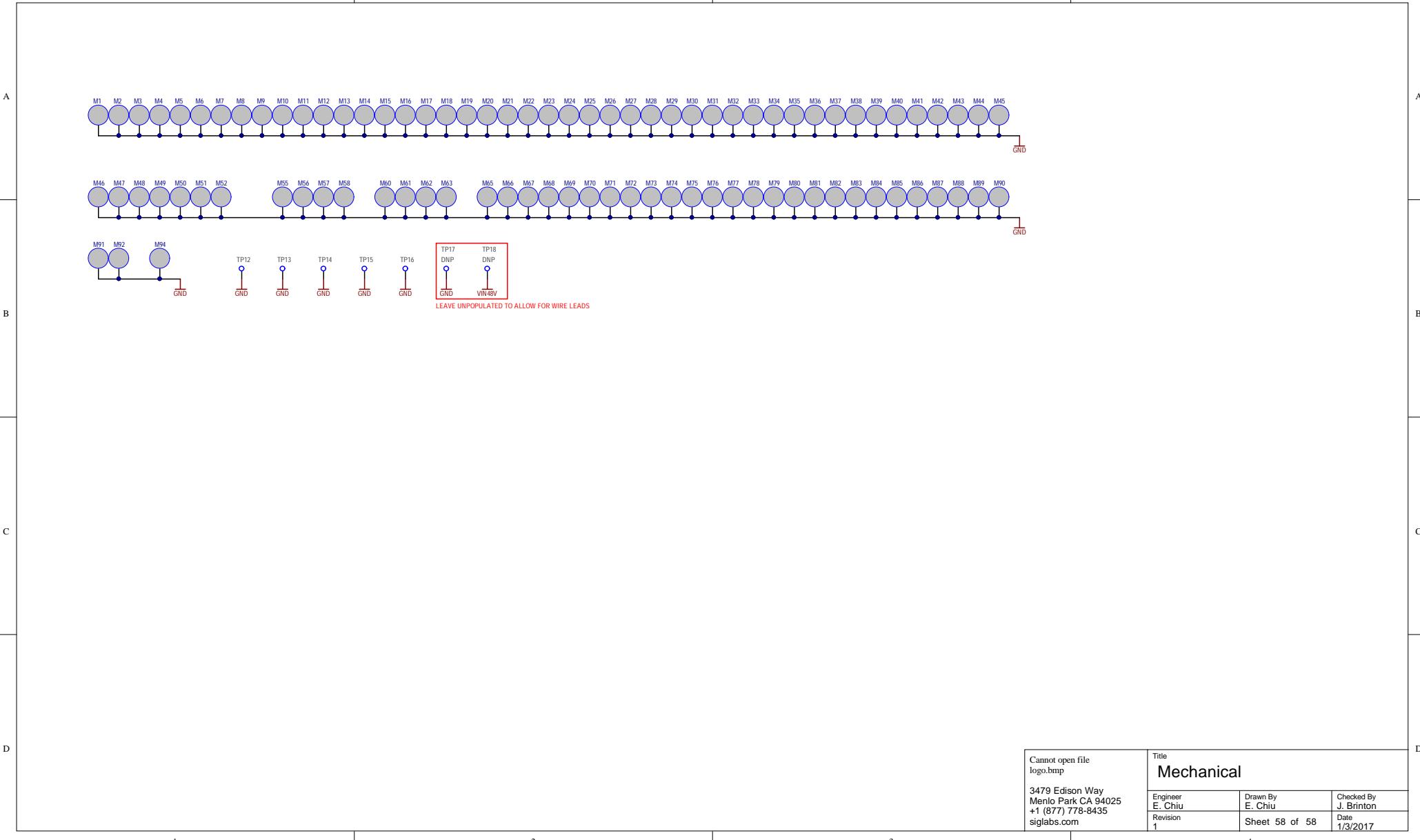
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Engineer	Drawn By	Checked By
E. Chiu	E. Chiu	J. Brinton
Revision 1	Sheet 57 of 58	Date 1/3/2017

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