Texas Instruments

PROFILE: Hardware

Name of the Role: Digital Design Engineer/ EDA

Expected GPA requirement: > 7

Eligible departments: CSE, EEE, ECE, ICE

The process involved: OT, 2 Technical Interviews, and 1 HR Interview.

Test Details:

- Step 1 – OT (2-4 hrs approx.): 3 Sections – Aptitude, Analog, Digital,

Basic C (for EDA). NEGATIVE MARKING may be present.

- Analog: Analog circuits, RLC circuits and signal processing, Diode Capacitor Resistor circuits with different voltage and currents sources, OPAMP circuits, bjt and amplifier (control system concept), semiconductor device understanding, transistors like BJTs, JFETs, e-MOSFETs and d-MOSFETs.
- Digital: Basics of digital, combinational and sequential circuits, FSMs, counters, STA, FIFO, digital circuit designing, VLSI, Verilog or Vhdl, flipflops, TTL, RTL logics, Muxes, decoders.
- Aptitude: General Aptitude, quantitative aptitude, data interpretation and Einstein Puzzle, placement and routing, area analysis.

- Software: Operator precedence, bitwise operators, left shift and right shift, implementation of division by a power of 2 using right shift operator, unions, bit fields, sizes of different data types, pointers, strings, arrays, etc. This section also includes some microprocessor concepts 8085 and 8086 processor (interrupts, addressing, various addressing modes, data and address lines in memory chips and their related concepts, etc.)

- Step 2 – Interviews:
- Technical Interview (Analog and Digital):

Fundamentals of Digital and Analog

The interviewer tends to start with a simple concept and then gets on to the deeper details based on our answers.

Topics generally asked are RC circuits, OpAmps, Understanding of Transistors, MOSFETs and their circuits. Digital Electronics and basics of VLSI.

Software interview (EDA): Implementation of division using shift operators (Pro's and Con's), basic concepts like OOPs, polymorphism, checking your familiarity with different Operating Systems & versions of C and C++ .

I was taught a new concept called forking and was immediately asked questions regarding the concept just learnt – interpretation of the program.

- HR Interview:

Resume based questions about extracurricular activities.

Preparation: CPCs
- RS Agarwal, Arun Sharma for Aptitude
- C programming by Schaum's Series, and learncpp.com

- Circuit Theory by Ramakalyan Sir, Hayt and Kemmerly and Alexander and Sadiku for general circuit theory and the book of Electronic Devices and Circuit Theory by Robert Boylestad, microelectronics for analog circuits
- Digital Electronics by Morris Mano, Floyd and Jain

JOB DETAILS:

A typical day in this role:
A significant amount of work is done in the afternoon from 11 to 4. You get to work on everything from specs to designing and then converting into Verilog code, getting requirements from other companies, working on those requirements, and making radar chips (Radar group of TI). Verifications of the design, bug fixing, and then passing on to the physical design team. Meetings to discuss about the work (WFH) also happen during this time.

Expectation vs Reality:
I didn't have any prerequisite expectations for the team I will be working with; I thought verification was the central part, but chip designing is equally challenging cause the requirements you get are very high level. The transformation process from spec to design in Verilog takes a lot of effort.
I expected to get a format on what needs to be done, but in reality, you have to do that by making many assumptions and designing on paper. A lot of collaborations with other teams is also required.

Your Growth in 1-2 years:
For New college graduates (NCGs), TI has a program worldwide called Make an Impact, where you go through different training programs where they train you on how to increase your performance in a day and cope with things. It trains you to tackle issues that arise due to WFH and gives the basic training required

for an NCG. Many such programs like digital boot camps were conducted where you get to learn about the digital designs needed in industries and also get to work on projects. The learning curve is very steep in the initial six months. Also, training is provided to understand the working of special teams. Portals are available where you can take up courses for free.

Projects and tasks are given:
Spec to Verilog code (designing of chips), documentation of the designed chips, and the requirements coming from other teams, design and bug fixes.

Work culture, Employee benefits etc. and few points about the company:
Work culture is very good, flexible, lot of opportunities to learn. TI specifically catered to a lot of problems you face as a WFH NCG. No monitoring at the micro-level is done in a day. TI focuses more on the output produced. You have a lot of autonomy as an employee. Deadlines are abstract, probably weekly or once every two weeks. Everybody in the team sits around in a cubicle together while working, with no particular office space, and this makes you feel like you are a part of something and there is no hierarchy.
Insurance of the dependents is covered. 20 causal + 12 sick leaves, TI gives importance to employee's mental health.
 A pay increase happens every year.

Any advice from your side:
Concentrate on one profile, analog or digital and solve previous year interview questions. The interviewers ask questions that test your in-depth knowledge of the subject. You have to write down the

approach you have used and your thought process behind it. You can expect them to ask questions from ALL corners of the problem.
If you are stuck up, they will usually give you hints, and if you make any mistakes, they will ask you to find them out and explain what mistakes you have made. It might panic you, but that is how it goes. Just be confident and keep trying to answer their questions. They ask questions from all aspects of the fundamentals which you have studied, so focus on that.

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