

EFR32BG24L Wireless SoC Family Data Sheet



EFR32BG24L Wireless SoCs are ideal for wireless connectivity using Bluetooth Low Energy and Bluetooth mesh.

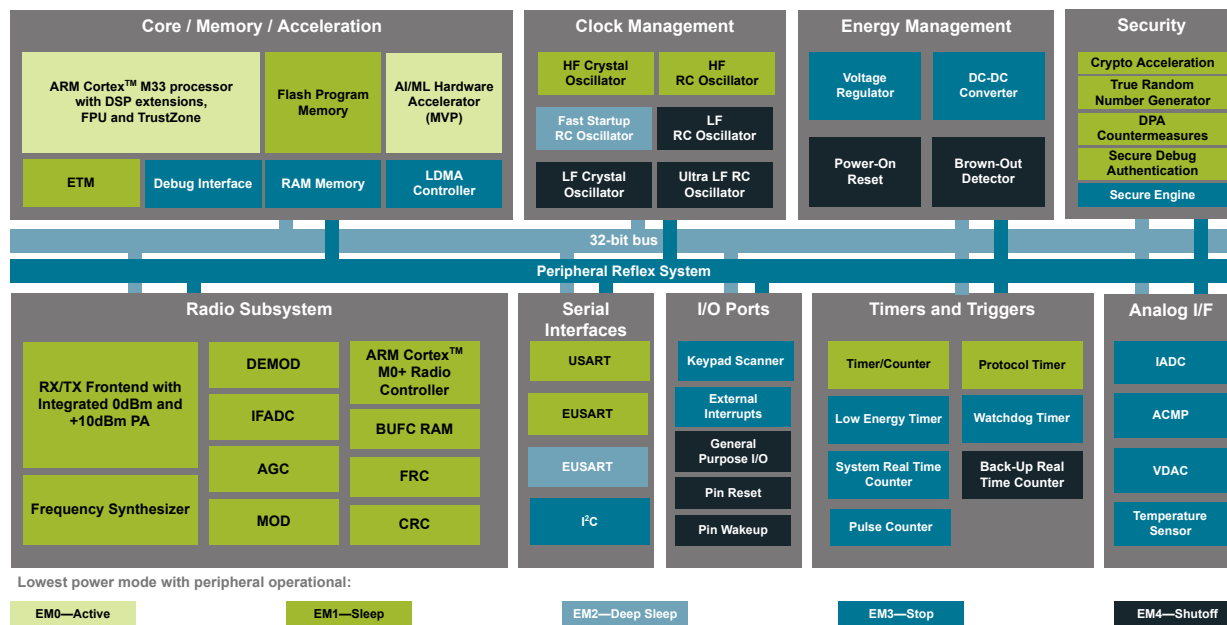
With key features like high-performance 2.4 GHz RF, low current consumption, an AI/ML hardware accelerator, and Secure Vault, IoT device makers can create smart, robust, and energy-efficient products that are secure from remote and local cyber-attacks. A Cortex®-M33 running up to 78 MHz and up to 768 kB of flash and 96 kB of RAM provides resources for demanding applications while leaving room for future growth.

Target applications include:

- Smart Home - Gateways and hubs, sensors, switches, door locks, smart plugs
- Lighting - LED bulbs, luminaires
- Portable Medical Devices - Blood glucose meters, pulse oximeters
- AI/ML - Predictive maintenance, anomaly detection

KEY FEATURES

- 32-bit ARM® Cortex®-M33 core with 78 MHz maximum operating frequency
- Up to 768 kB of flash and 96 kB of RAM
- High-performance radio with up to +10 dBm output power
- Energy efficient design with low active and sleep currents
- Secure Vault™
- AI/ML Hardware Accelerator
- Channel sounding



1. Feature List

The EFR32BG24L highlighted features are listed below.

- **Low Power Wireless System-on-Chip**
 - High-performance 32-bit 78 MHz ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
 - 768 kB flash program memory
 - 96 kB RAM data memory
 - 2.4 GHz radio operation
 - Matrix Vector Processor for AI/ML acceleration
- **Radio Performance**
 - -105.7 dBm sensitivity @ 125 kbps GFSK
 - -97.6 dBm sensitivity @ 1 Mbps GFSK
 - -94.8 dBm sensitivity @ 2 Mbps GFSK
 - TX power up to 10 dBm
- **Low System Energy Consumption**
 - 4.4 mA RX current (1 Mbps GFSK)
 - 5 mA TX current @ 0 dBm output power
 - 19.1 mA TX current @ 10 dBm output power
 - 33.4 μ A/MHz in Active Mode (EM0) at 39.0 MHz
 - 1.3 μ A EM2 DeepSleep current (16 kB RAM retention and RTC running from LFRCO)
- **Supported Modulation Format**
 - 2 (G)FSK with fully configurable shaping
 - OQPSK DSSS
 - (G)MSK
- **Protocol Support**
 - Bluetooth Low Energy
 - Bluetooth Mesh
 - Proprietary 2.4 GHz
 - Direction finding using Angle-of-Arrival (AoA) and Angle-of-Departure (AoD)
 - Channel sounding
 - 40 MHz crystal required
 - Maximum TX power for Channel Sounding is 10 dBm for all part numbers
- **Secure Vault**
 - Hardware Cryptographic Acceleration for AES128/192/256, SHA-1, SHA-2/256, ECDSA+ECDH(P-192, P-256), Ed25519 and Curve25519, J-PAKE
 - True Random Number Generator (TRNG)
 - ARM® TrustZone®
 - Secure Boot (Root of Trust Secure Loader)
 - Secure Debug Unlock
 - DPA Countermeasures
- **Wide Selection of MCU Peripherals**
 - Analog to Digital Converter (IADC)
 - 12-bit @ 1 Msps
 - 16-bit @ 76.9 kbps
 - 2 \times Analog Comparator (ACMP)
 - 2 \times Digital to Analog Converter (VDAC)
 - Up to 26 General Purpose I/O pins with output state retention and asynchronous interrupts
 - 8 Channel DMA Controller (LDMA)
 - 16 Asynchronous Channel, 4 Synchronous Channel Peripheral Reflex System (PRS)
 - 3 \times 16-bit Timer/Counter with 3 Compare/Capture/PWM channels (TIMER2/3/4)
 - 2 \times 32-bit Timer/Counter with 3 Compare/Capture/PWM channels (TIMER0/1)
 - 2 \times 32-bit Real Time Counter (SYSRTC/BURTC)
 - 24-bit Low Energy Timer for waveform generation (LETIMER)
 - 16-bit Pulse Counter with asynchronous operation (PCNT)
 - 2 \times Watchdog Timer (WDOG)
 - 1 \times Universal Synchronous/Asynchronous Receiver/Transmitter (USART), supporting UART/SPI/SmartCard (ISO 7816)/IrDA/I²S
 - 2 \times Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART) supporting UART/SPI/DALI/IrDA
 - 2 \times I²C interface with SMBus support
 - Low-Frequency RC Oscillator with precision mode to replace 32 kHz sleep crystal (LFRCO)
 - Keypad scanner supporting up to 6x8 matrix (KEYSCAN)
 - Die temperature sensor with ± 1.5 °C accuracy after single-point calibration
- **Wide Operating Range**
 - 1.71 to 3.8 V single power supply
 - -40 to 125 °C
- **Packages**
 - **QFN40** 5 \times 5 \times 0.85 mm

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Max TX Power	Flash (KB)	RAM (KB)	Secure Vault	IADC High-Speed / High-Accuracy	Matrix Vector Processor	GPIO	Package / Pin-out
EFR32BG24L210F768IM40-B	10 dBm	768	96	Mid	No	Yes	26	QFN40 / Standard
EFR32BG24L010F768IM40-B	10 dBm	768	96	Mid	No	No	26	QFN40 / Standard

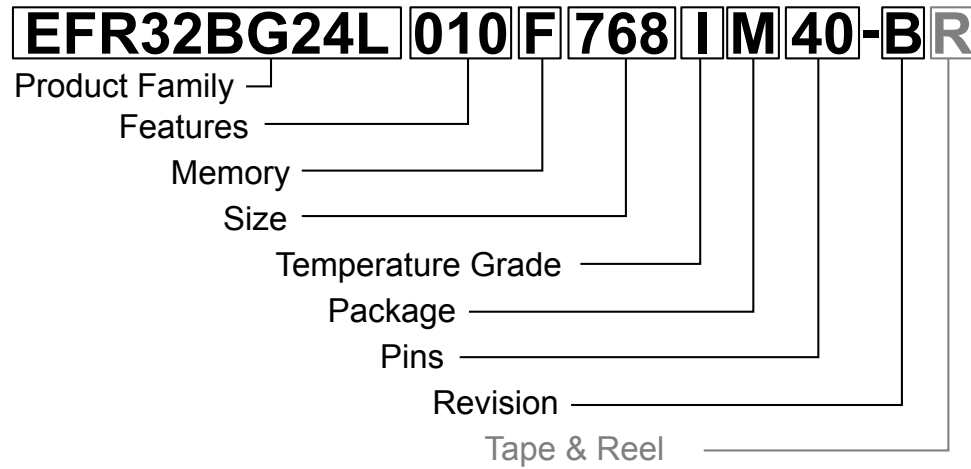


Figure 2.1. Ordering Code Key

Field	Options
Product Family	<ul style="list-style-type: none"> • EFR32BG24L: Blue Gecko 24L Family
Features [f1][f2][f3]	<ul style="list-style-type: none"> • f1 <ul style="list-style-type: none"> • 0: Base Configuration • 2: Matrix Vector Processor (MVP) Available • f2 <ul style="list-style-type: none"> • 1: 10 dBm PA Transmit Power • f3 <ul style="list-style-type: none"> • 0: No feature enabled
Memory	<ul style="list-style-type: none"> • F: Flash
Size	<ul style="list-style-type: none"> • Memory Size in kBytes
Temperature Grade	<ul style="list-style-type: none"> • I: -40 to +125 °C
Package	<ul style="list-style-type: none"> • M: QFN
Pins	<ul style="list-style-type: none"> • Number of Package Pins
Revision	<ul style="list-style-type: none"> • B: Revision B
Tape & Reel	<ul style="list-style-type: none"> • R: Tape & Reel (optional)

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3. System Overview

3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a high-performance radio transceiver. The devices are well suited for secure connected IoT multiprotocol devices requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32xG24 Reference Manual.

A block diagram of the EFR32BG24L family is shown in [Figure 3.1 Detailed EFR32BG24L Block Diagram on page 9](#). The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult [2. Ordering Information](#).

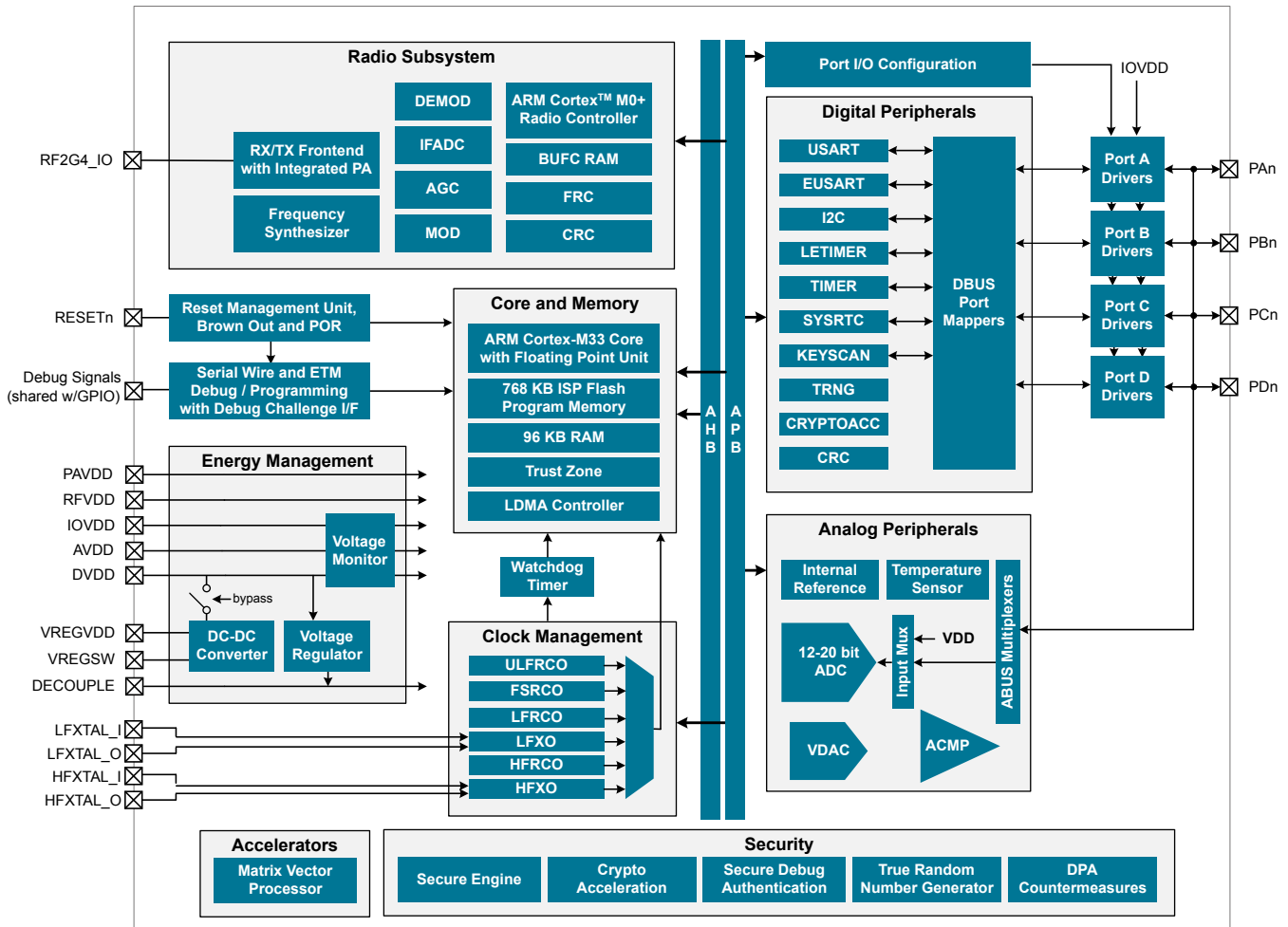


Figure 3.1. Detailed EFR32BG24L Block Diagram

3.2 Radio

The EFR32BG24L Wireless SoC features a highly configurable radio transceiver supporting Bluetooth Low Energy, Bluetooth Mesh, and Proprietary 2.4 GHz wireless protocols.

3.2.1 Antenna Interface

The 2.4 GHz antenna interface consists of a single-ended pin (RF2G4_IO). The external components for the antenna interface in typical applications are shown in the RF Matching Networks section.

3.2.2 Fractional-N Frequency Synthesizer

The EFR32BG24L contains a high-performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency for the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance, frequency resolution better than 100 Hz, and low energy consumption. The synthesizer's fast frequency settling allows for very short receiver and transmitter wake up times to reduce system energy consumption.

3.2.3 Receiver Architecture

The EFR32BG24L uses a low-IF receiver architecture, which consists of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer. The I/Q signals are further filtered and amplified before being sampled by the IF Analog-to-Digital Converter (IFADC).

The IF frequency is configurable from 150 to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The 2.4 GHz radio is calibrated at production to improve image rejection performance.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, level-based proximity detection, and RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

3.2.4 Transmitter Architecture

The EFR32BG24L uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32BG24L. These algorithms are typically defined by regulatory standards to improve interoperability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.2.5 Packet and State Trace

The EFR32BG24L Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data, and state information
- Data observability on a single-pin UART data output or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data, and state / meta information in a single serial data stream

3.2.6 Data Buffering

The EFR32BG24L features an advanced Radio Buffer Controller (BUFC) capable of handling up to four buffers of adjustable size from 64 to 4096 bytes. Each buffer can be used for RX, TX, or for both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.7 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32BG24L. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter, and frequency synthesizer
- Detailed frame transmission timing with optional LBT or CSMA-CA

3.2.8 RF Signal Identifier

When an IoT radio is placed next to a high duty-cycle co-located Wi-Fi radio transmission, IoT radios are blocked from receiving weak signals. The RF Signal Identifier feature available on EFR32BG24L devices enables the IoT radio to detect partial 802.15.4 or BLE/BT Mesh packets. When a partial packet is detected, the IoT radio can communicate this information to the corresponding Wi-Fi device (through serial interface or GPIO asserts), which can consequently halt transmission while the IoT radio waits for a packet retry to be received. This helps provide a higher success rate of receiving packets from other devices on the network, when co-located with an interfering Wi-Fi radio.

3.3 General Purpose Input/Output (GPIO)

EFR32BG24L has up to 26 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by low-energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have wake functionality down to EM4. These pins are listed in the Alternate Function Table with the function GPIO.EM4WU.

3.4 Keypad Scanner (KEYSCAN)

A low-energy keypad scanner (KEYSCAN) is included, which can scan up to a 6 x 8 matrix of keyboard switches. The KEYSCAN peripheral contains logic for debounce and settling time, allowing it to scan through the switch matrix autonomously in EM0 and EM1, and interrupt the processor when a key press is detected. A wake-on-keypress feature is also supported, allowing for the detection of any key press down to EM3.

3.5 Clocking

3.5.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32BG24L. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.5.2 Internal and External Oscillators

The EFR32BG24L supports two crystal oscillators and fully integrates four RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. The HFXO provides excellent RF clocking performance using a 39.0 MHz crystal. The HFXO can also support an external clock source such as a TCXO for applications that require an extremely accurate clock frequency over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system when crystal accuracy is not required. The HFRCO employs fast start-up at minimal energy consumption combined with a wide frequency range, from 1 MHz to 78 MHz.
- An integrated fast start-up RC oscillator (FSRCO) that runs at a fixed 20 MHz
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation without an external crystal. Precision mode enables periodic recalibration against the 39.0 MHz HFXO crystal to improve accuracy to +/- 500 ppm, suitable for BLE sleep interval timing.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 Counters/Timers and PWM

3.6.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs, and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 16-bit or 32-bit counter with up to 3 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers. In addition, some timers offer dead-time insertion.

See [3.14 Configuration Summary](#) for information on the feature set of each timer.

3.6.2 Low Energy Timer (LETIMER)

The unique LETIMER is a 24-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Peripheral Reflex System (PRS), and can be configured to start counting on compare matches from other peripherals such as the Real Time Clock.

3.6.3 System Real Time Clock with Capture (SYSRTC)

The System Real Time Clock (SYSRTC) is a 32-bit counter providing timekeeping down to EM3. The SYSRTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user defined intervals.

3.6.4 Back-Up Real Time Counter (BURTC)

The Back-Up Real Time Counter (BURTC) is a 32-bit counter providing timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

3.6.5 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the Peripheral Reflex System (PRS).

3.7 Communications and Other Digital Peripherals

3.7.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire, and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I²S

3.7.2 Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)

The Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter supports full duplex asynchronous UART communication with hardware flow control, RS-485, and IrDA support. The EUSART also supports high-speed SPI. In EM0 and EM1, the EUSART provides a high-speed, buffered communication interface.

When routed to GPIO ports A or B, the EUSART0 may also be used in a low-energy mode and operate in EM2. A 32.768 kHz clock source allows full duplex UART communication up to 9600 baud. EUSART0 can also act as a SPI secondary device in EM2 and EM3, and wake the system when data is received from an external bus controller.

3.7.3 Inter-Integrated Circuit Interface (I²C)

The I²C module provides an interface between the MCU and a serial I²C bus. It is capable of acting as a main or secondary interface and supports multi-drop buses. Standard-mode, fast-mode, and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Bus arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of addresses is provided in active and low energy modes. Not all instances of I²C are available in all energy modes.

3.7.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality, such as simple logic operations (AND, OR, NOT), can be applied by the PRS to the signals. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

3.8 Secure Vault Features

A dedicated hardware secure engine containing its own CPU enables the Secure Vault functions. It isolates cryptographic functions and data from the host Cortex-M33 core, and provides several additional security features. The EFR32BG24L family includes devices with Secure Vault Mid capabilities, which are summarized in the table below.

Table 3.1. Secure Vault Features

Feature	Secure Vault Mid
True Random Number Generator (TRNG)	Yes
Secure Boot with Root of Trust and Secure Loader (RTSL)	Yes
Secure Debug with Lock/Unlock	Yes
DPA Countermeasures	Yes
Symmetric Encryption	<ul style="list-style-type: none"> AES 128 / 192 / 256 bit ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC
Public Key Encryption - ECDSA / ECDH / EdDSA	<ul style="list-style-type: none"> p192 and p256 Curve25519 (ECDH)¹ Ed25519 (EdDSA)¹
Key Derivation	<ul style="list-style-type: none"> ECJ-PAKE p192 and p256
Hashes	<ul style="list-style-type: none"> SHA-1 SHA-2/256
Note: 1. These curves are supported in devices running SE v2.1.7 and higher	

3.8.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over The Air updates.

For more information about this feature, see [AN1218: Series 2 Secure Boot with RTSL](#).

3.8.2 Cryptographic Accelerator

The Cryptographic Accelerator in Secure Engine is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, Elliptic Curve Cryptography (ECC) to support public key operations and hashes.

Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CCM (Counter with CBC-MAC)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the National Institute of Standards and Technology (NIST) recommended curves including P-192 and P-256 for Elliptic Curve Diffie-Hellman (ECDH) key derivation and Elliptic Curve Digital Signature Algorithm (ECDSA) sign and verify operations.

Secure Engine also supports Elliptic Curve variant of Password Authenticated Key Exchange by Juggling (ECJ-PAKE).

Supported hashes include SHA-1, SHA2/224, and SHA-2/256.

This implementation provides a fast and energy-efficient solution to state of the art cryptographic needs.

Note: AES_ECB, AES_CBC, AES_CBCMAC, and SHA-1 are provided for legacy compatibility and are not recommended for cryptographic purposes without thoroughly understanding their potential security weaknesses.

3.8.3 True Random Number Generator

The TRNG module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31, as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.8.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

Secure Vault also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

For more information about this feature, see [AN1190: Series 2 Secure Debug](#).

3.8.5 DPA Countermeasures

The AES and ECC accelerators have Differential Power Analysis (DPA) countermeasures support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

3.9 Analog

3.9.1 Analog to Digital Converter (IADC)

The IADC is a hybrid architecture combining techniques from both SAR and Delta-Sigma style converters. It has a resolution of 12 bits at 1 Msps and 16 bits at up to 76.9 kbps. Hardware oversampling reduces system-level noise over multiple front-end samples. The IADC includes integrated voltage reference options. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.9.2 Analog Comparator (ACMP)

The ACMP is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.9.3 Digital to Analog Converter (VDAC)

The VDAC can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.10 Power

The EFR32BG24L has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. An optional integrated DC-DC buck regulator further reduces the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFR32BG24L device family includes support for internal supply voltage scaling, as well as two different power domains groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

3.10.1 Energy Management Unit (EMU)

The EMU manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to implement system-wide voltage scaling and turn off the power to unused RAM blocks to optimize the energy consumption in the target application. The DC-DC regulator operation is tightly integrated with the EMU.

3.10.2 Voltage Scaling

The EFR32BG24L supports supply voltage scaling for the LDO powering DECOUPLE, with independent selections for EM0 / EM1 and EM2 / EM3. Voltage scaling helps to optimize the energy efficiency of the system by operating at lower voltages when possible. The EM0 / EM1 voltage scaling level defaults to VSCALE2, which allows the core to operate in active mode at full speed. The intermediate level, VSCALE1, allows operation in EM0 and EM1 at up to 40 MHz. The lowest level, VSCALE0, can be used to conserve power further in EM2 and EM3. The EMU will automatically switch the target voltage scaling level when transitioning between energy modes.

3.10.3 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents, providing high efficiency in energy modes EM0, EM1, EM2, and EM3. RF noise mitigation allows operation of the DC-DC converter without significantly degrading sensitivity of radio components. An on-chip supply-monitor signals when the supply voltage is low to allow bypass of the regulator via programmable software interrupt. It employs soft switching at boot and DCDC regulating-to-bypass transitions to limit the max supply slew-rate and mitigate inrush current.

3.10.4 Power Domains

Peripherals may exist on one of several independent power domains which are powered down to minimize supply current when not in use. Power domains are managed automatically by the EMU.

The lowest-energy power domain is the "high-voltage" power domain (PDHV), which supports extremely low-energy infrastructure and peripherals. Circuits powered from PDHV are always on and available in all energy modes down to EM4.

The next power domain is the low power domain (PD0), which is further divided to power subsets of peripherals. All PD0 power domains are shut down in EM4. Circuits powered from PD0 power domains may be available in EM0, EM1, EM2, and EM3.

Low power domain A (PD0A) is the base power domain for EM2 and EM3 and will always remain on in EM0-EM3. It powers the most commonly-used EM2 and EM3-capable peripherals and infrastructure required to operate in EM2 and EM3. Auxiliary PD0 power domains (PD0B, PD0C, PD0D, PD0E) power additional EM2 and EM3-capable peripherals on demand. If any peripherals on one of the auxiliary power domains is enabled, that power domain will be active in EM2 and EM3. Otherwise, the auxiliary PD0 power domains will be shut down to reduce current.

Note: Power domain PD0E is also turned on when peripherals on PD0B, PD0C, or PD0D are used.

The active power domain (PD1) powers the rest of the device circuitry, including the CPU core and EM0 / EM1 peripherals. PD1 is always powered on in EM0 and EM1. PD1 is always shut down in EM2, EM3, and EM4.

Table 3.2 Peripheral Power Subdomains on page 17 shows the peripherals on the PDHV and PD0x domains. Any peripheral not listed is on PD1.

Table 3.2. Peripheral Power Subdomains

Always On in EM2/EM3		Selectively On in EM2/3			
PDHV ¹	PD0A	PD0B ²	PD0C ²	PD0D ²	PD0E
LFRCO (Non-precision Mode)	SYSRTC	LETIMER0	LFRCO (Precision Calibration Mode)	DEBUG	GPIO
LFXO	FSRCO	IADC0	HFRCOEM23	WDOG0/1	KEYSCAN
BURTC		PCNT0	HFXO	EUSART0	PRS
BURAM		ACMP0/1		I2C0	
ULFRCO		VDAC0/1			
Note: 1. Peripherals on PDHV are also available in EM4. 2. If any of PD0B, PD0C, or PD0D are enabled, PD0E will also be automatically enabled.					

3.11 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32BG24L. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.12 Core, Memory, and Accelerators

3.12.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M33 RISC processor achieving 1.50 Dhrystone MIPS/MHz
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 768 KB flash program memory
- Up to 96 KB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.12.2 Memory System Controller (MSC)

The MSC is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M33 and LDMA. In addition to the main flash array where program code is normally written, the MSC also provides an information block where additional information, such as special user information or flash-lock bits, is stored. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.12.3 Linked Direct Memory Access Controller (LDMA)

The LDMA controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.12.4 Matrix Vector Processor (MVP)

The MVP is designed to offload the major computationally intensive floating point operations, particularly matrixed complex floating point multiplications and additions. The MVP supports the acceleration of the key Angle-of-Arrival (AoA) Multiple Signal Classification (MUSIC) algorithm computations, as well as other heavily floating-point computational problems such as Machine Learning (ML) or linear algebra.

3.13 Memory Map

The EFR32BG24L memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

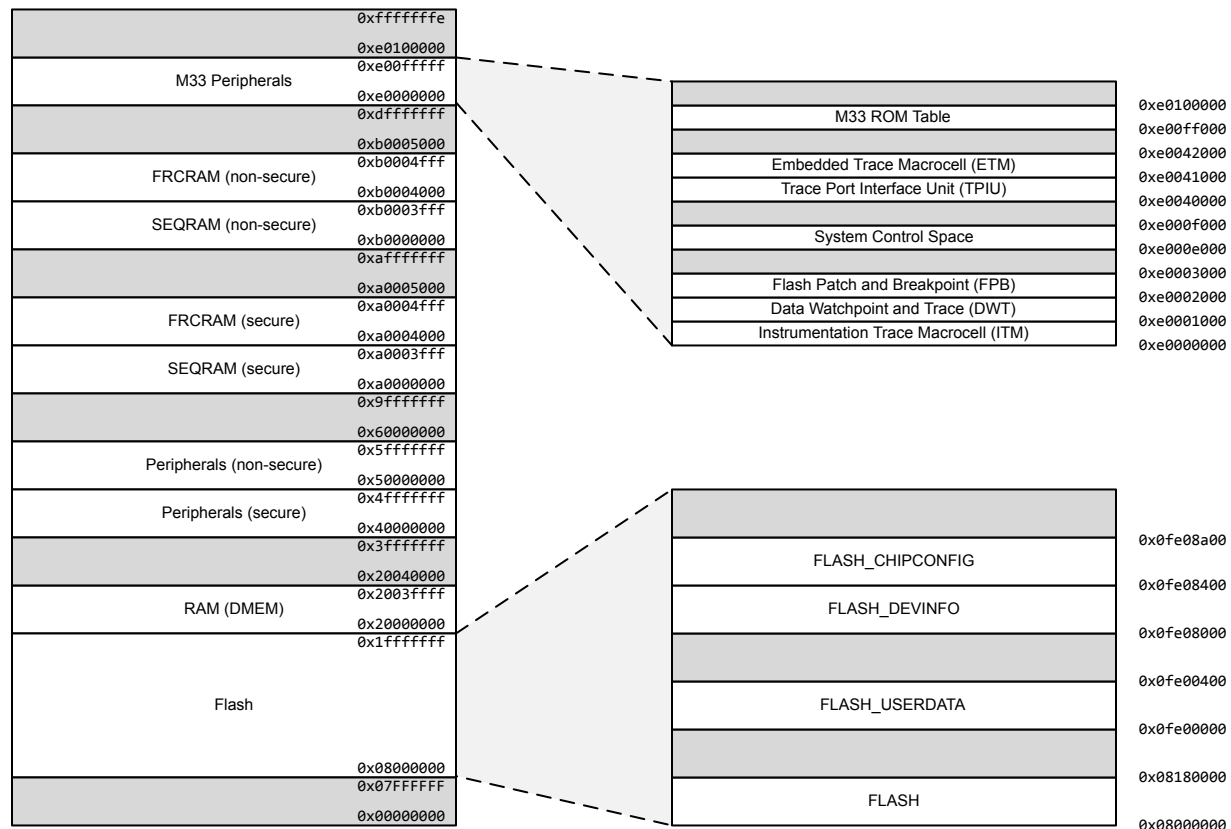


Figure 3.2. EFR32BG24L Memory Map — Core Peripherals and Code Space

3.14 Configuration Summary

The features of the EFR32BG24L are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration. Refer to the Energy Modes table in the Reference Manual EMU Chapter for a more comprehensive list of energy mode support for all device peripherals.

Table 3.3. Configuration Summary

Module	Lowest Energy Mode	Configuration
I2C0	EM1 - Full functionality EM2/3 ¹ - Functionality limited to receive address recognition	
I2C1	EM1 - Full functionality	
LETIMER0	EM2/3 ¹	24-bit, 2-channels
TIMER0	EM1	32-bit, 3-channels, +DTI
TIMER1	EM1	32-bit, 3-channels, +DTI
TIMER2	EM1	16-bit, 3-channels, +DTI
TIMER3	EM1	16-bit, 3-channels, +DTI
TIMER4	EM1	16-bit, 3-channels, +DTI
EUSART0	EM1 - Full high-speed operation, all modes EM2 ¹ - Low-energy UART operation, 9600 Baud EM2/3 ¹ - Low-energy SPI secondary receiver	UART, SPI, IrDA, DALI
EUSART1	EM1	UART, SPI, IrDA, DALI
USART0	EM1	UART, SPI, IrDA, I2S, SmartCard
Note: 1. EM2 and EM3 operation is only supported for digital peripheral I/O on Port A and Port B. All GPIO ports support digital peripheral operation in EM0 and EM1.		

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_A=25\text{ }^{\circ}\text{C}$ and all supplies at 3.0 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Due to on-chip circuitry (e.g., diodes), some EFR32BG24L power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFR32BG24L supply pins are defined below. Exceeding the below constraints can result in damage to the device and/or increased current draw.

- VREGVDD and DVDD
 - In systems using the DCDC converter, DVDD (the buck converter output) should not be driven externally and VREGVDD (the buck converter input) must be greater than DVDD ($VREGVDD \geq DVDD$)
 - In systems not using the DCDC converter, DVDD must be shorted to VREGVDD on the PCB ($VREGVDD = DVDD$)
- AVDD, IOVDD: No dependency with each other or any other supply pin. Additional leakage may occur if DVDD remains unpowered with power applied to these supplies.
- $DVDD \geq DECOUPLE$
- $PAVDD \geq RFVDD$

4.2 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T _{STG}		-50	—	+150	°C
Voltage on any supply pin ¹	V _{DDMAX}		-0.3	—	3.8	V
Junction temperature	T _{JMAX}	-I grade	—	—	+125	°C
Voltage ramp rate on any supply pin	V _{DDRAMP} MAX		—	—	1.0	V / μs
Voltage on HFXO pins	V _{HFXO} PIN		-0.3	—	1.2	V
DC voltage on any GPIO pin	V _{DIG} PIN		-0.3	—	V _{IOVDD} + 0.3	V
DC voltage on RESETn pin ²	V _{RESET} n		-0.3	—	3.8	V
DC voltage on RF pin RF2G4_IO	V _{MAX} 2G4		-0.3	—	1.2	V
Total current into VDD power lines	I _{VDD} MAX	Source	—	—	200	mA
Total current into VSS ground lines	I _{VSS} MAX	Sink	—	—	200	mA
Current per I/O pin	I _{IO} MAX	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	I _{IOALL} MAX	Sink	—	—	200	mA
		Source	—	—	200	mA
Note:						
1. The maximum supply voltage on VREGVDD is limited under certain conditions when using the DC-DC. See the DC-DC specifications for more details.						
2. The RESETn pin has a pull-up device to the DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD.						

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-I temperature grade ¹	-40	—	+125	° C
DVDD supply voltage	V_{DVDD}	EM0/1	1.71	3.0	3.8	V
		EM2/3/4 ²	1.71	3.0	3.8	V
AVDD supply voltage	V_{AVDD}	AVDDBODEN=0 ³	1.71	3.0	3.8	V
IOVDDx operating supply voltage (All IOVDD pins)	V_{IOVDDx}	IOVDDxBODEN=0 ³	1.71	3.0	3.8	V
RFVDD operating supply voltage	V_{RFVDD}		1.71	3.0	V_{PAVDD}	V
VREGVDD operating supply voltage	$V_{VREGVDD}$	DC-DC in regulation ⁴	2.2	3.0	3.8	V
		DC-DC in bypass 60 mA load	1.8	3.0	3.8	V
		DC-DC in bypass 120 mA load	1.8	3.0	3.8	V
		DC-DC not in use. DVDD externally shorted to VREGVDD	1.71	3.0	3.8	V
PAVDD operating supply voltage	V_{PAVDD}		1.71	3.0	3.8	V
DECOUPLE output capacitor ⁵	$C_{DECOUPLE}$	1.0 μ F \pm 10% X8L capacitor used for performance characterization.	1.0	—	2.75	μ F
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	78	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
		VSCALE1, MODE = WS1	—	—	40	MHz
		VSCALE1, MODE = WS0	—	—	20	MHz
PCLK frequency	f_{PCLK}	VSCALE2 or VSCALE1	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	78	MHz
		VSCALE1	—	—	40	MHz
EM01 Group C clock frequency	$f_{EM01GRPCCLK}$	VSCALE2	—	—	78	MHz
		VSCALE1	—	—	40	MHz
Radio HCLK frequency ⁶	f_{RHCLK}	VSCALE2 or VSCALE1	—	39.0	—	MHz
External clock input	f_{CLKIN}	VSCALE2 or VSCALE1, IOVDD \geq 2.7 V	—	—	40	MHz
DPLL reference clock	$f_{DPLLREFCLK}$	VSCALE2 or VSCALE1	—	—	40	MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: <ol style="list-style-type: none">1. The device may operate continuously at the maximum allowable ambient T_A rating as long as the absolute maximum T_{JMAX} is not exceeded. For an application with significant power dissipation, the allowable T_A may be lower than the maximum T_A rating. $T_A = T_{JMAX} - (\theta_{JA} \times \text{PowerDissipation})$. Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_{JMAX} and θ_{JA}.2. The DVDD supply is monitored by the DVDD BOD in EM0/1 and the LE DVDD BOD in EM2/3/4.3. The AVDD and IOVDD enable bits are in the EMU_BOD3SENSE register. These BODs are disabled on reset.4. The maximum supply voltage on VREGVDD is limited under certain conditions when using the DC-DC. See the DC-DC specifications for more details.5. Murata GCM21BL81C105KA58L used for performance characterization. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 0.6 μF.6. The recommended radio crystal frequency for the 2.4 GHz radio is 39 MHz. The minimum and maximum RHCLK frequency in this table represents the design timing limits, which are much wider than the typical crystal tolerance.						

4.4 DC-DC Converter

Test conditions: $L_{DCDC} = 2.2 \mu\text{H}$ (Murata DFE2HCAH2R2MJ0), $C_{DCDC} = 4.7 \mu\text{F}$ (TDK CGA5L3X8R1C475K160AB), $V_{VREGVDD} = 3.0 \text{ V}$, $V_{OUT} = 1.8 \text{ V}$, $IPKVAL$ in EM0/1 modes is set to 150 mA, and in EM2/3 modes is set to 90 mA, unless otherwise indicated.

Table 4.3. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range at VREGVDD pin	$V_{VREGVDD}$	DCDC in regulation, $I_{LOAD} = I_{LOAD\ MAX}^1$, EM0/EM1 mode	2.2	—	3.8	V
		DCDC in regulation, $I_{LOAD} = 5 \text{ mA}$, EM0/EM1 or EM2/EM3 mode	1.8	—	3.8	V
		Bypass Mode, $I_{LOAD} \leq 60 \text{ mA}$	1.8	—	3.8	V
		Bypass Mode, $I_{LOAD} \leq 120 \text{ mA}$	1.9	—	3.8	V
Regulated output voltage	V_{OUT}		—	1.8	—	V
Regulation DC accuracy	ACC_{DC}	$V_{VREGVDD} \geq 2.2 \text{ V}$, Steady state in EM0/EM1 mode or EM2/EM3 mode	-2.5	—	4.0	%
Regulation total accuracy	ACC_{TOT}	All error sources (including DC errors, overshoot, undershoot)	-5	—	7	%
Steady-state output ripple	V_R	$I_{LOAD} = 20 \text{ mA}$ in EM0/EM1 mode	—	12	—	mVpp
DC line regulation	V_{REG}	$I_{LOAD} = I_{LOAD\ MAX}$ in EM0/EM1 mode, $V_{VREGVDD} \geq 2.2 \text{ V}$	—	-2.6	—	mV/V
Efficiency	EFF	Load current between 100 μA and 60 mA in EM0/EM1 mode	—	90	—	%
		Load current between 10 μA and 5 mA in EM2/EM3 mode	—	89	—	%
DC load regulation	I_{REG}	Load current between 100 μA and $I_{LOAD\ MAX}$ in EM0/EM1 mode	—	-0.08	—	mV/mA
Output load current	I_{LOAD}	EM0/EM1 mode, DCDC in regulation, $DCDC_EM01CTRL0.IPKVAL = 9$, Radio not transmitting	—	—	60	mA
		EM0/EM1 mode, DCDC in regulation, Radio in receive mode	—	—	36	mA
		EM0/EM1 mode, DCDC in regulation, Radio transmitting ¹	—	—	120	mA
		EM2/EM3 mode, DCDC in regulation	—	—	5	mA
		Bypass mode, $1.8 \text{ V} \leq V_{VREGVDD} \leq 3.8 \text{ V}$	—	—	60	mA
		Bypass mode, $1.9 \text{ V} \leq V_{VREGVDD} \leq 3.8 \text{ V}$	—	—	120	mA
Nominal output capacitor	C_{DCDC}	$4.7 \mu\text{F} \pm 10\%$ X7R capacitor used for performance characterization ²	—	4.7	10	μF
Nominal inductor	L_{DCDC}	$\pm 20\%$ tolerance	—	2.2	—	μH
Nominal input capacitor	C_{IN}		C_{DCDC}	—	—	μF

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resistance in bypass mode	R _{BYP}	Bypass switch from VREGVDD to DVDD, V _{VREGVDD} = 1.8 V	—	0.45	0.69	Ω
		Powertrain PFET switch from VREGVDD to VREGSW, V _{VREGVDD} = 1.8 V	—	0.6	0.9	Ω
Supply monitor threshold programming range	V _{CMP_RNG}	Programmable in 0.1 V steps	2	—	2.3	V
Supply monitor threshold accuracy	V _{CMP_ACC}	Supply falling edge trip point	-5	—	5	%
Supply monitor threshold hysteresis	V _{CMP_HYST}	Positive hysteresis on the supply rising edge referred to the falling edge trip point	—	4	—	%
Supply monitor response time	t _{CMP_DELAY}	Supply falling edge at -100 mV / μs	—	0.6	—	μs

Note:

1. During radio transmit operations, the RAIL library will place the DCDC into a mode that increases the maximum load current to support higher TX output power supplied from the DCDC converter.
2. Actual capacitor values can be significantly de-rated from their specified nominal value by the rated tolerance, as well as the application's AC voltage, DC bias, and temperature. The minimum capacitance counting all error sources should be no less than 3.6 μF.

4.4.1 DC-DC Maximum Load Current

The system will operate in one of two states in EM0/1, determined by the maximum TX power:

- PFM mode only: Operating state only when TX power is less than 10 dBm
- PFM + PFMX mode: Operating state when TX power is greater than or equal to 10 dBm

4.5 Thermal Characteristics**Table 4.4. Thermal Characteristics**

Package	Board	Parameter	Symbol	Test Condition	Value	Unit
40QFN (5x5 mm)	JEDEC - High Thermal Cond. (2s2p) ¹	Thermal Resistance, Junction to Ambient	Θ _{JA}	Still Air	29.2	°C/W
		Thermal Resistance, Junction to Board	Θ _{JB}		15.2	°C/W
		Thermal Resistance, Junction to Top Center	Ψ _{JT}		0.3	°C/W
		Thermal Resistance, Junction to Board	Ψ _{JB}		11.2	°C/W
	No Board	Thermal Resistance, Junction to Case	Θ _{JC}	Temperature controlled heat sink on top of package, all other sides of package insulated to prevent heat flow.	24.6	°C/W

Note:

1. Based on 4-layer PCB with dimension 3" x 4.5", PCB Thickness of 1.6 mm, per JEDEC. PCB Center Land with 9 Via to top internal plane of PCB.

4.6 Current Consumption

4.6.1 MCU Current Consumption using DC-DC at 3.0 V input

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.0 V. DVDD = RFVDD = PAVDD = 1.8 V from DC-DC. Voltage scaling level = VSCALE1. $T_A = 25\text{ }^{\circ}\text{C}$. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A = 25\text{ }^{\circ}\text{C}$.

Table 4.5. MCU Current Consumption using DC-DC at 3.0 V input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running Prime from flash, VSCALE2	—	33.3	—	$\mu\text{A}/\text{MHz}$
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running while loop from flash, VSCALE2	—	32.8	—	$\mu\text{A}/\text{MHz}$
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	49.1	—	$\mu\text{A}/\text{MHz}$
		39 MHz crystal, CPU running Prime from flash	—	33.9	—	$\mu\text{A}/\text{MHz}$
		39 MHz crystal, CPU running while loop from flash	—	33.4	—	$\mu\text{A}/\text{MHz}$
		39 MHz crystal, CPU running CoreMark loop from flash	—	49.4	—	$\mu\text{A}/\text{MHz}$
		38 MHz HFRCO, CPU running while loop from flash	—	28.1	—	$\mu\text{A}/\text{MHz}$
		26 MHz HFRCO, CPU running while loop from flash	—	31.0	—	$\mu\text{A}/\text{MHz}$
		16 MHz HFRCO, CPU running while loop from flash	—	37.6	—	$\mu\text{A}/\text{MHz}$
		1 MHz HFRCO, CPU running while loop from flash	—	281.8	—	$\mu\text{A}/\text{MHz}$
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, VSCALE2	—	22.6	—	$\mu\text{A}/\text{MHz}$
		39 MHz crystal	—	24.4	—	$\mu\text{A}/\text{MHz}$
		38 MHz HFRCO	—	19.0	—	$\mu\text{A}/\text{MHz}$
		26 MHz HFRCO	—	22.0	—	$\mu\text{A}/\text{MHz}$
		16 MHz HFRCO	—	28.5	—	$\mu\text{A}/\text{MHz}$
		1 MHz HFRCO	—	272.1	—	$\mu\text{A}/\text{MHz}$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I _{EM2_VS}	96 kB RAM and full Radio RAM retention, RTC running from LFXO ¹	—	1.9	—	μA
		96 kB RAM and full Radio RAM retention, RTC running from LFRCO ¹	—	1.9	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFXO ¹	—	1.3	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO ¹	—	1.3	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO in precision mode ¹	—	1.9	—	μA
Current consumption in EM3 mode, VSCALE0	I _{EM3_VS}	96 kB RAM and full Radio RAM retention, RTC running from ULFRCO ¹	—	1.7	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from ULFRCO ¹	—	1.1	—	μA
Change in current consumption if CPU cached unre-tained in EM2 or EM3	I _{EM23_CPUCACHE}		—	-0.06	—	μA
Change in current consumption if EM0/1 peripheral states unretained in EM2 or EM3	I _{EM23_STATERET}		—	-0.01	—	μA
Change in current consumption for retained RAM bank in EM2 or EM3	I _{EM23_RAM}	Per 16 kB RAM bank	—	0.11	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled ²	I _{PD0B_VS}		—	0.93	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0C is enabled ²	I _{PD0C_VS}		—	0.26	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0D is enabled ²	I _{PD0D_VS}		—	1.1	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0E is enabled ²	I _{PD0E_VS}		—	0.09	—	μA
Current consumption in EM4 mode	I _{EM4}	No BURTC, no LF oscillator	—	0.25	—	μA
		BURTC with LFXO	—	0.64	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: <ol style="list-style-type: none"> 1. CPU cache retained, EM0/1 peripheral states retained. 2. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.10.4 Power Domains for a list of the peripherals in each power domain. Note that if the PD0B, PD0C, or PD0D domains are enabled, PD0E will also automatically be enabled. 						

4.6.2 MCU Current Consumption at 3.0 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = 3.0 V. DC-DC not used. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.6. MCU Current Consumption at 3.0 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I _{ACTIVE}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running Prime from flash, VSCALE2	—	47.3	—	μA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running while loop from flash, VSCALE2	—	46.1	—	μA/MHz
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	69.5	—	μA/MHz
		39 MHz crystal, CPU running Prime from flash	—	48.4	—	μA/MHz
		39 MHz crystal, CPU running while loop from flash	—	47.1	—	μA/MHz
		39 MHz crystal, CPU running CoreMark loop from flash	—	69.6	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	39.4	62	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	43.6	—	μA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	52.7	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	392.4	1170	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I _{EM1}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, VSCALE2	—	32.2	—	μA/MHz
		39 MHz crystal	—	34.5	—	μA/MHz
		38 MHz HFRCO	—	26.8	49	μA/MHz
		26 MHz HFRCO	—	30.9	—	μA/MHz
		16 MHz HFRCO	—	40.0	—	μA/MHz
		1 MHz HFRCO	—	380.0	1160	μA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I _{EM2_VS}	96 kB RAM and full Radio RAM retention, RTC running from LFXO ¹	—	2.6	—	μA
		96 kB RAM and full Radio RAM retention, RTC running from LFRCO ¹	—	2.7	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFXO ¹	—	1.8	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO ¹	—	1.9	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO in precision mode ¹	—	2.8	—	μA
Current consumption in EM3 mode, VSCALE0	I _{EM3_VS}	96 kB RAM and full Radio RAM retention, RTC running from ULFRCO ¹	—	2.3	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from ULFRCO ¹	—	1.5	2.5	μA
Change in current consumption if CPU cached unre-tained in EM2 or EM3	I _{EM23_CPUCACHE}		—	-0.07	—	μA
Change in current consumption if EM0/1 peripheral states unretained in EM2 or EM3	I _{EM23_STATERET}		—	-0.01	—	μA
Change in current consumption for retained RAM bank in EM2 or EM3	I _{EM23_RAM}	Per 16 kB RAM bank	—	0.16	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled ²	I _{PD0B_VS}		—	1.4	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0C is enabled ²	I _{PD0C_VS}		—	0.39	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0D is enabled ²	I _{PD0D_VS}		—	1.6	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0E is enabled ²	I _{PD0E_VS}		—	0.11	—	μA
Current consumption in EM4 mode	I _{EM4}	No BURTC, no LF oscillator	—	0.26	0.65	μA
		BURTC with LFXO	—	0.64	—	μA
Current consumption during reset	I _{RST}	Hard pin reset held	—	457	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: <ol style="list-style-type: none">CPU cache retained, EM0/1 peripheral states retained.Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.10.4 Power Domains for a list of the peripherals in each power domain. Note that if the PD0B, PD0C, or PD0D domains are enabled, PD0E will also automatically be enabled.						

4.6.3 MCU Current Consumption at 1.8 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = VREGVDD = 1.8 V. DC-DC not used. Voltage scaling level = VSCALE1. $T_A = 25\text{ }^{\circ}\text{C}$. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A = 25\text{ }^{\circ}\text{C}$.

Table 4.7. MCU Current Consumption at 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running Prime from flash, VSCALE2	—	47.8	—	$\mu\text{A}/\text{MHz}$
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running while loop from flash, VSCALE2	—	46.1	—	$\mu\text{A}/\text{MHz}$
		78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	69.4	—	$\mu\text{A}/\text{MHz}$
		39 MHz crystal, CPU running Prime from flash	—	48.1	—	$\mu\text{A}/\text{MHz}$
		39 MHz crystal, CPU running while loop from flash	—	47.1	—	$\mu\text{A}/\text{MHz}$
		39 MHz crystal, CPU running CoreMark loop from flash	—	69.8	—	$\mu\text{A}/\text{MHz}$
		38 MHz HFRCO, CPU running while loop from flash	—	39.4	—	$\mu\text{A}/\text{MHz}$
		26 MHz HFRCO, CPU running while loop from flash	—	43.5	—	$\mu\text{A}/\text{MHz}$
		16 MHz HFRCO, CPU running while loop from flash	—	52.5	—	$\mu\text{A}/\text{MHz}$
		1 MHz HFRCO, CPU running while loop from flash	—	390.0	—	$\mu\text{A}/\text{MHz}$
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	78 MHz HFRCO w/ DPLL referenced to 39 MHz crystal, VSCALE2	—	32.2	—	$\mu\text{A}/\text{MHz}$
		39 MHz crystal	—	34.5	—	$\mu\text{A}/\text{MHz}$
		38 MHz HFRCO	—	26.7	—	$\mu\text{A}/\text{MHz}$
		26 MHz HFRCO	—	30.8	—	$\mu\text{A}/\text{MHz}$
		16 MHz HFRCO	—	39.8	—	$\mu\text{A}/\text{MHz}$
		1 MHz HFRCO	—	377.3	—	$\mu\text{A}/\text{MHz}$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, VSCALE0	I _{EM2_VS}	96 kB RAM and full Radio RAM retention, RTC running from LFXO ¹	—	2.6	—	μA
		96 kB RAM and full Radio RAM retention, RTC running from LFRCO ¹	—	2.6	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFXO ¹	—	1.8	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO ¹	—	1.8	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO in precision mode ¹	—	2.7	—	μA
Current consumption in EM3 mode, VSCALE0	I _{EM3_VS}	96 kB RAM and full Radio RAM retention, RTC running from ULFRCO ¹	—	2.2	—	μA
		16 kB RAM and full Radio RAM retention, RTC running from ULFRCO ¹	—	1.4	—	μA
Change in current consumption if CPU cached unre-tained in EM2 or EM3	I _{EM23_CPUCACHE}		—	-0.07	—	μA
Change in current consumption if EM0/1 peripheral states unretained in EM2 or EM3	I _{EM23_STATERET}		—	-0.01	—	μA
Change in current consumption for retained RAM bank in EM2 or EM3	I _{EM23_RAM}	Per 16 kB RAM bank	—	0.16	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled ²	I _{PD0B_VS}		—	1.4	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0C is enabled ²	I _{PD0C_VS}		—	0.38	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0D is enabled ²	I _{PD0D_VS}		—	1.6	—	μA
Additional current in EM2 or EM3 when any peripheral in PD0E is enabled ²	I _{PD0E_VS}		—	0.12	—	μA
Current consumption in EM4 mode	I _{EM4}	No BURTC, no LF oscillator	—	0.18	—	μA
		BURTC with LFXO	—	0.53	—	μA
Current consumption during reset	I _{RST}	Hard pin reset held	—	391	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: <ol style="list-style-type: none">CPU cache retained, EM0/1 peripheral states retained.Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.10.4 Power Domains for a list of the peripherals in each power domain. Note that if the PD0B, PD0C, or PD0D domains are enabled, PD0E will also automatically be enabled.						

4.6.4 Radio Current Consumption at 3.0V using DCDC

RF current consumption measured with MCU in EM1, HCLK = 39.0 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VREGVDD = IOVDD = 3.0 V. AVDD = DVDD = RFVDD = PAVDD = 1.8 V powered from DCDC. $T_A = 25\text{ }^{\circ}\text{C}$. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A = 25\text{ }^{\circ}\text{C}$.

Table 4.8. Radio Current Consumption at 3.0V using DCDC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System current consumption in receive mode, active packet reception	I _{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4.6	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	4.9	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	5.2	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4.7	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	5	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	5.2	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4.4	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	4.7	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	4.9	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	5.4	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	5.6	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System current consumption in receive mode, listening for packet	I _{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4.7	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	4.9	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	5.2	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4.7	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	5	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	5.2	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	4.3	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	4.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	4.9	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	5.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	5.4	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	5.7	—	mA
System current consumption in transmit mode	I _{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1	—	5	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 10 dBm output power, VSCALE1	—	19.1	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE2	—	5.2	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 10 dBm output power, VSCALE2	—	19.2	—	mA

4.6.5 Radio Current Consumption at 3.0V

RF current consumption measured with MCU in EM1, HCLK = 39.0 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0 V. DCDC disabled. $T_A = 25\text{ }^{\circ}\text{C}$. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A = 25\text{ }^{\circ}\text{C}$.

Table 4.9. Radio Current Consumption at 3.0V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I _{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.1	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	7.5	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.9	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.2	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	7.6	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6.7	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	7.1	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.4	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.7	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	8.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	8.6	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, listening for packet	I _{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.1	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	7.5	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.9	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.1	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	7.5	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.9	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	7	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.4	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.7	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	8.2	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	8.6	—	mA
Current consumption in transmit mode	I _{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE2	—	8	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 10 dBm output power, VSCALE2	—	28.7	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1	—	7.8	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 10 dBm output power, VSCALE1	—	28.4	—	mA

4.6.6 Radio Current Consumption at 1.8V

RF current consumption measured with MCU in EM1, HCLK = 39.0 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8 V. DCDC disabled. $T_A = 25\text{ }^{\circ}\text{C}$. Minimum and maximum values in this table represent the worst conditions across process variation at $T_A = 25\text{ }^{\circ}\text{C}$.

Table 4.10. Radio Current Consumption at 1.8V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I _{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	7.5	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.9	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.1	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	7.6	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	8	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	7.1	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.4	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.7	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1	—	8.1	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	8.6	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, listening for packet	I _{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.1	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.9	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.1	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.9	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	6.6	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.4	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P (Radio clocks only)	—	7.7	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	8.6	—	mA
Current consumption in transmit mode	I _{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE2	—	7.8	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 10 dBm output power, VSCALE2	—	28.5	—	mA
		f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power, VSCALE1	—	7.5	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 10 dBm output power, VSCALE1	—	28.2	—	mA

4.7 Flash Characteristics

Table 4.11. Flash Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash supply voltage during write or erase	V_{FLASH}		1.71	—	3.8	V
Flash data retention ¹	$\text{RET}_{\text{FLASH}}$		10	—	—	years
Flash erase cycles before failure ¹	EC_{FLASH}		10,000	—	—	cycles
Program Time	t_{PROG}	$T_A = 25\text{ }^{\circ}\text{C}$, one word (32-bits)	41.9	43.4	45.0	μs
		$T_A = 25\text{ }^{\circ}\text{C}$, average per word over 128 words	10.6	10.9	11.3	μs
Page Erase Time ²	t_{PERASE}	$T_A = 25\text{ }^{\circ}\text{C}$	11.6	12.9	14.0	ms
Mass Erase Time ^{3 4}	t_{MERASE}	$T_A = 25\text{ }^{\circ}\text{C}$, 768 kB	62	77	87	ms
Program Current	I_{WRITE}		—	—	2.8	mA
Page Erase Current	I_{PERASE}	Page Erase	—	—	1.9	mA
Mass Erase Current	I_{MERASE}	Mass Erase	—	—	2.0	mA

Note:

- Flash data retention information is published in the Quarterly Quality and Reliability Report.
- Page Erase time is measured from setting the ERASEPAGE bit in the MSC_WRITECMD register until the BUSY bit in the MSC-STATUS register is cleared to 0. Internal set-up and hold times are included.
- Mass Erase is issued by the CPU and erases all of user space.
- Mass Erase time is measured from setting the ERASEMAIN0 bit in the MSC_WRITECMD register until the BUSY bit in the MSC-STATUS register is cleared to 0. Internal set-up and hold times are included.

4.8 Energy Mode Wake-up and Entry Times

Unless otherwise specified, these times are measured using the HFRCO at 19 MHz.

Table 4.12. Energy Mode Wake-up and Entry Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake-up Time from EM1	t_{EM1_WU}	Code execution from flash	—	3	—	HCLKs
		Code execution from RAM	—	1.4	—	μ s
Wake-up Time from EM2	t_{EM2_WU}	Code execution from flash, No Voltage Scaling	—	13.7	—	μ s
		Code execution from RAM, No Voltage Scaling	—	5.1	—	μ s
		Voltage scaling up one level ¹	—	37.7	—	μ s
		Voltage scaling up two levels ²	—	50.7	—	μ s
Wake-up Time from EM3	t_{EM3_WU}	Code execution from flash, No Voltage Scaling	—	13.7	—	μ s
		Code execution from RAM, No Voltage Scaling	—	5.1	—	μ s
		Voltage scaling up one level ¹	—	37.7	—	μ s
		Voltage scaling up two levels ²	—	50.7	—	μ s
Wake-up Time from EM4	t_{EM4_WU}	Code execution from flash	—	21.7	—	ms
Entry time to EM1	t_{EM1_ENT}	Code execution from flash	—	1.5	—	μ s
Entry time to EM2	t_{EM2_ENT}	Code execution from flash	—	6.1	—	μ s
Entry time to EM3	t_{EM3_ENT}	Code execution from flash	—	6.0	—	μ s
Entry time to EM4	t_{EM4_ENT}	Code execution from flash	—	11.2	—	μ s
Voltage scaling time in EM0 ³	t_{SCALE}	Up from VSCALE1 to VSCALE2	—	32	—	μ s
		Down from VSCALE2 to VSCALE1	—	172	—	μ s

Note:

1. Voltage scaling one level is between VSCALE0 and VSCALE1 or between VSCALE1 and VSCALE2.
2. Voltage scaling two levels is between VSCALE0 and VSCALE2.
3. During voltage scaling in EM0, RAM is inaccessible and processor will be halted until complete.

4.9 2.4 GHz RF Transceiver Characteristics

4.9.1 RF Transmitter Characteristics

4.9.1.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^{\circ}\text{C}$, Crystal frequency = 39.0 MHz, RF center frequency = 2.45 GHz.

- For 0 dBm / 10 dBm PA: VREGVDD = IOVDD = AVDD = 3.0 V, DVDD = RFVDD = PAVDD = 1.8 V powered from DCDC

Table 4.13. RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		2400	—	2483.5	MHz
Radio-only current consumption while transmitting ¹	$I_{\text{TX_RADIO}}$	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power	—	3.5	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 10 dBm output power	—	17.6	—	mA
Maximum TX power ²	$POUT_{\text{MAX}}$	10 dBm PA ³	—	10	—	dBm
		0 dBm PA	—	-0.7	—	dBm
Minimum active TX power	$POUT_{\text{MIN}}$	10 dBm PA	—	-29.8	—	dBm
		0 dBm PA	—	-25.2	—	dBm
Output power variation vs supply voltage variation, frequency = 2450 MHz	$POUT_{\text{VAR_V}}$	10 dBm PA output power with PAVDD voltage swept from 1.8 to 3.0 V	—	0.03	—	dB
		0 dBm PA output power with PAVDD voltage swept from 1.8 to 3.0 V	—	0.02	—	dB
Output power variation vs temperature, frequency = 2450 MHz	$POUT_{\text{VAR_T}}$	10 dBm PA at 10 dBm, (-40 to +125 °C)	—	0.2	—	dB
		0 dBm PA at 0 dBm, (-40 to +125 °C)	—	1.23	—	dB
Output power variation vs RF frequency	$POUT_{\text{VAR_F}}$	10 dBm PA, 10 dBm	—	0.11	—	dB
		0 dBm PA, 0 dBm	—	0.16	—	dB
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{\text{HRM_FCC_R}}$	Continuous transmission of CW carrier, $P_{\text{out}} = POUT_{\text{MAX}}$, Test Frequency = 2450 MHz.	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{\text{HRM_FCC_NRR}}$	Continuous transmission of CW carrier. $P_{\text{out}} = POUT_{\text{MAX}}$. Test Frequency = 2450 MHz.	—	-26	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	SPUR _{OOB_FCC_R}	Restricted bands 30-88 MHz, Continuous transmission of CW carrier, P _{out} = POUT _{MAX} , Test Frequency = 2450 MHz	—	-61	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of CW carrier, P _{out} = POUT _{MAX} , Test Frequency = 2450 MHz	—	-58	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of CW carrier, P _{out} = POUT _{MAX} , Test Frequency = 2450 MHz	—	-55	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of CW carrier, P _{out} = POUT _{MAX} , Test Frequency = 2450 MHz	—	-47	—	dBm
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	SPUR _{OOB_FCC_NR}	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission CW carrier, P _{out} = POUT _{MAX} , Test Frequency = 2450 MHz	—	-26	—	dBc
Spurious emissions per ETSI EN300.440	SPUR _{ETSI440}	47-74 MHz, 87.5-108 MHz, 174-230 MHz, 470-862 MHz, P _{out} = 10 dBm, Test Frequency = 2450 MHz	—	-60	—	dBm
		25-1000 MHz, excluding above frequencies. P _{out} = 10 dBm, Test Frequency = 2450 MHz	—	-42	—	dBm
		1G-14G, P _{out} = 10 dBm, Test Frequency = 2450 MHz	—	-36	—	dBm
Spurious emissions out-of-band, per ETSI 300.328	SPUR _{ETSI328}	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P _{out} = 10 dBm, Test Frequency = 2402 and 2480 MHz	—	-26	—	dBm
		47-74 MHz, 87.5-118 MHz, 174-230 MHz, 470-862 MHz, P _{out} = 10 dBm, Test Frequency = 2450 MHz	—	-60	—	dBm
		30-47 MHz, 74-87.5 MHz, 118-174 MHz, 230-470 MHz, 862-1000 MHz, P _{out} = 10 dBm, Test Frequency = 2450 MHz	—	-42	—	dBm
		1G-12.75 GHz, excluding bands listed above, P _{out} = 10 dBm, Test Frequency = 2450 MHz	—	-36	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P _{out} = 10 dBm, Test Frequency = 2402 and 2480 MHz	—	-16	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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Note:

1. Supply current to radio, supplied by DC-DC with 3.0 V, measured at VREGVDD.
2. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this datasheet can be found in the Max TX Power column of the Ordering Information Table.
3. The PA is capable of delivering higher than 10 dBm output power (refer to Output Power plots in [4.27.2 RF Characteristics](#)). However, all transmitter characteristics and recommended application circuits are specified at 10 dBm output. If used with the recommended application circuits above 10 dBm, harmonics may be higher than regulatory limits.

4.9.1.2 RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: $T_A = 25^\circ\text{C}$, Crystal frequency = 39.0 MHz, RF center frequency = 2.45 GHz.

- For 0 dBm / 10 dBm PA: VREGVDD = IOVDD = AVDD = 3.0 V, DVDD = RFVDD = PAVDD = 1.8 V powered from DCDC

Table 4.14. RF Transmitter Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Error vector magnitude per 802.15.4-2011	EVM	Average across frequency, signal is DSSS-OQPSK reference packet, $P_{\text{out}} = 10\text{ dBm}$	—	2.9	—	% rms
		Average across frequency, signal is DSSS-OQPSK reference packet, $P_{\text{out}} = 0\text{ dBm}$	—	2.9	—	% rms
Power spectral density limit	PSD _{LIMIT}	Relative, at carrier $\pm 3.5\text{ MHz}$, $P_{\text{out}} = 10\text{ dBm}$	—	-50.1	—	dBc/100kHz
		Relative, at carrier $\pm 3.5\text{ MHz}$, $P_{\text{out}} = 0\text{ dBm}$	—	-50.7	—	dBc/100kHz
		Absolute, at carrier $\pm 3.5\text{ MHz}$, $P_{\text{out}} = 10\text{ dBm}$	—	-48.7	—	dBm/100kHz
		Absolute, at carrier $\pm 3.5\text{ MHz}$, $P_{\text{out}} = 0\text{ dBm}$	—	-59.2	—	dBm/100kHz
		Per FCC part 15.247, $P_{\text{out}} = 10\text{ dBm}$	—	-9.2	—	dBm/3kHz
		Per FCC part 15.247, $P_{\text{out}} = 0\text{ dBm}$	—	-19.9	—	dBm/3kHz
		ETSI 300.328 $P_{\text{out}} = 10\text{ dBm}$	—	8	—	dBm
		ETSI 300.328 $P_{\text{out}} = 0\text{ dBm}$	—	-2.8	—	dBm
Occupied channel bandwidth per ETSI EN300.328	OCP _{ETSI328}	99% BW at highest and lowest channels in band, $P_{\text{out}} = 10\text{ dBm}$	—	2.2	—	MHz
		99% BW at highest and lowest channels in band, $P_{\text{out}} = 0\text{ dBm}$	—	2.2	—	MHz

4.9.1.3 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^{\circ}\text{C}$, Crystal frequency = 39.0 MHz, RF center frequency = 2.45 GHz.

- For 0 dBm / 10 dBm PA: VREGVDD = IOVDD = AVDD = 3.0 V, DVDD = RFVDD = PAVDD = 1.8 V powered from DCDC

Table 4.15. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	$P_{out} = 10\text{ dBm}$	—	714	—	kHz
		$P_{out} = 0\text{ dBm}$	—	715	—	kHz
Power spectral density limit	PSD _{LIMIT}	$P_{out} = 10\text{ dBm}$, Per FCC part 15.247 at 10 dBm	—	-10.4	—	dBm/3kHz
		$P_{out} = 0\text{ dBm}$, Per FCC part 15.247 at 0 dBm	—	-21.2	—	dBm/3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	9.7	—	dBm
Occupied channel bandwidth per ETSI EN300.328	OCP _{ETSI328}	$P_{out} = 10\text{ dBm}$ 99% BW at highest and lowest channels in band	—	1	—	MHz
		$P_{out} = 0\text{ dBm}$ 99% BW at highest and lowest channels in band	—	1	—	MHz
In-band spurious emissions, with allowed exceptions ¹	SPUR _{INB}	$P_{out} = 10\text{ dBm}$, Inband spurs at $\pm 2\text{ MHz}$	—	-38.8	—	dBm
		$P_{out} = 0\text{ dBm}$, Inband spurs at $\pm 2\text{ MHz}$	—	-49.8	—	dBm
		$P_{out} = 10\text{ dBm}$ Inband spurs at $\pm 3\text{ MHz}$	—	-43.8	—	dBm
		$P_{out} = 0\text{ dBm}$ Inband spurs at $\pm 3\text{ MHz}$	—	-54.6	—	dBm

Note:

- Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.9.1.4 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^{\circ}\text{C}$, Crystal frequency = 39.0 MHz, RF center frequency = 2.45 GHz.

- For 0 dBm / 10 dBm PA: VREGVDD = IOVDD = AVDD = 3.0 V, DVDD = RFVDD = PAVDD = 1.8 V powered from DCDC

Table 4.16. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	$P_{out} = 10\text{ dBm}$	—	1308	—	kHz
		$P_{out} = 0\text{ dBm}$	—	1306	—	kHz
Power spectral density limit	PSD _{LIMIT}	$P_{out} = 10\text{ dBm}$, Per FCC part 15.247 at 10 dBm	—	-8.5	—	dBm/3kHz
		$P_{out} = 0\text{ dBm}$, Per FCC part 15.247 at 0 dBm	—	-19.3	—	dBm/3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	8.7	—	dBm
Occupied channel bandwidth per ETSI EN300.328	OCP _{ETSI328}	$P_{out} = 10\text{ dBm}$ 99% BW at highest and lowest channels in band	—	2.1	—	MHz
		$P_{out} = 0\text{ dBm}$ 99% BW at highest and lowest channels in band	—	2.1	—	MHz
In-band spurious emissions, with allowed exceptions ¹	SPUR _{INB}	$P_{out} = 10\text{ dBm}$, Inband spurs at $\pm 4\text{ MHz}$	—	-43.7	—	dBm
		$P_{out} = 0\text{ dBm}$, Inband spurs at $\pm 4\text{ MHz}$	—	-54.5	—	dBm
		$P_{out} = 10\text{ dBm}$ Inband spurs at $\pm 6\text{ MHz}$	—	-48.8	—	dBm
		$P_{out} = 0\text{ dBm}$ Inband spurs at $\pm 6\text{ MHz}$	—	-59.5	—	dBm

Note:

- Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.9.1.5 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^{\circ}\text{C}$, Crystal frequency = 39.0 MHz, RF center frequency = 2.45 GHz.

- For 0 dBm / 10 dBm PA: VREGVDD = IOVDD = AVDD = 3.0 V, DVDD = RFVDD = PAVDD = 1.8 V powered from DCDC

Table 4.17. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	$P_{out} = 10\text{ dBm}$	—	718	—	kHz
		$P_{out} = 0\text{ dBm}$	—	717	—	kHz
Power spectral density limit	PSD _{LIMIT}	$P_{out} = 10\text{ dBm}$, Per FCC part 15.247 at 10 dBm	—	-10.4	—	dBm/3kHz
		$P_{out} = 0\text{ dBm}$, Per FCC part 15.247 at 0 dBm	—	-21.2	—	dBm/3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	9.7	—	dBm
Occupied channel bandwidth per ETSI EN300.328	OCP _{ETSI328}	$P_{out} = 10\text{ dBm}$ 99% BW at highest and lowest channels in band	—	1	—	MHz
		$P_{out} = 0\text{ dBm}$ 99% BW at highest and lowest channels in band	—	1	—	MHz
In-band spurious emissions, with allowed exceptions ¹	SPUR _{INB}	$P_{out} = 10\text{ dBm}$, Inband spurs at $\pm 2\text{ MHz}$	—	-38.9	—	dBm
		$P_{out} = 0\text{ dBm}$, Inband spurs at $\pm 2\text{ MHz}$	—	-49.8	—	dBm
		$P_{out} = 10\text{ dBm}$ Inband spurs at $\pm 3\text{ MHz}$	—	-43.8	—	dBm
		$P_{out} = 0\text{ dBm}$ Inband spurs at $\pm 3\text{ MHz}$	—	-54.6	—	dBm

Note:

- Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.9.1.6 RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^{\circ}\text{C}$, Crystal frequency = 39.0 MHz, RF center frequency = 2.45 GHz.

- For 0 dBm / 10 dBm PA: VREGVDD = IOVDD = AVDD = 3.0 V, DVDD = RFVDD = PAVDD = 1.8 V powered from DCDC

Table 4.18. RF Transmitter Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit 6 dB bandwidth	TXBW	$P_{out} = 10\text{ dBm}$	—	651	—	kHz
		$P_{out} = 0\text{ dBm}$	—	651	—	kHz
Power spectral density limit	PSD _{LIMIT}	$P_{out} = 10\text{ dBm}$, Per FCC part 15.247 at 10 dBm	—	3.8	—	dBm/3kHz
		$P_{out} = 0\text{ dBm}$, Per FCC part 15.247 at 0 dBm	—	-7	—	dBm/3kHz
		Per ETSI 300.328 at 10 dBm/1 MHz	—	9.7	—	dBm
Occupied channel bandwidth per ETSI EN300.328	OCP _{ETSI328}	$P_{out} = 10\text{ dBm}$ 99% BW at highest and lowest channels in band	—	1	—	MHz
		$P_{out} = 0\text{ dBm}$ 99% BW at highest and lowest channels in band	—	1	—	MHz
In-band spurious emissions, with allowed exceptions ¹	SPUR _{INB}	$P_{out} = 10\text{ dBm}$, Inband spurs at $\pm 2\text{ MHz}$	—	-39	—	dBm
		$P_{out} = 0\text{ dBm}$, Inband spurs at $\pm 2\text{ MHz}$	—	-49.7	—	dBm
		$P_{out} = 10\text{ dBm}$ Inband spurs at $\pm 3\text{ MHz}$	—	-43.7	—	dBm
		$P_{out} = 0\text{ dBm}$ Inband spurs at $\pm 3\text{ MHz}$	—	-54.5	—	dBm

Note:

- Per Bluetooth Core_5.1, Vol.6 Part A, Section 3.2.2, exceptions are allowed in up to three bands of 1 MHz width, centered on a frequency which is an integer multiple of 1 MHz. These exceptions shall have an absolute value of -20 dBm or less.

4.9.2 RF Receiver Characteristics

4.9.2.1 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: $T_A = 25\text{ }^{\circ}\text{C}$, $V_{\text{REGVDD}} = \text{IOVDD} = \text{AVDD} = \text{PAVDD} = 3.0\text{ V}$, $\text{RFVDD} = \text{DVDD} = 1.8\text{ V}$ powered from DCDC. Crystal frequency = 39.0 MHz, RF center frequency = 2.45 GHz.

Table 4.19. RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		2400	—	2483.5	MHz
Radio-only current consumption in receive mode ¹	$I_{\text{RX_RADIO}}$		—	2.8	—	mA
Receive mode maximum spurious emission	SPUR_{RX}	30 MHz to 1 GHz	—	-63	—	dBm
		1 GHz to 12 GHz	—	-53	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$\text{SPUR}_{\text{RX_FCC}}$	216 MHz to 960 MHz, conducted measurement	—	-55	—	dBm
		Above 960 MHz, conducted measurement.	—	-47	—	dBm
2GFSK Sensitivity	$\text{SENS}_{2\text{GFSK}}$	2 Mbps 2GFSK signal ² , 1% PER	—	-92.5	—	dBm
		250 kbps 2GFSK signal ³ , 0.1% BER	—	-102.9	—	dBm

Note:

1. Supply current to radio, supplied by DC-DC with 3.0 V, measured at V_{REGVDD} .
2. Reference signal is 2 Mbps 2GFSK, $\text{BT}=0.5$, $\text{mi}=1.0$, $\Delta f = \pm 1\text{ MHz}$, Channel bandwidth = 2.4 MHz.
3. Reference signal is 250 kbps 2GFSK, $\text{BT}=0.5$, $\text{mi}=1.0$, $\Delta f = \pm 125\text{ kHz}$, Channel bandwidth = 350 kHz.

4.9.2.2 RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: $T_A = 25^\circ\text{C}$, $V_{\text{REGVDD}} = \text{IOVDD} = \text{AVDD} = \text{PAVDD} = 3.0\text{ V}$, $\text{RFVDD} = \text{DVDD} = 1.8\text{ V}$ powered from DCDC. Crystal frequency = 39.0 MHz, RF center frequency = 2.45 GHz.

Table 4.20. RF Receiver Characteristics for 802.15.4 DSSS-OQPSK in the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 1% PER	RX_{SAT}	Signal is reference signal ¹ , packet length is 20 octets	—	10	—	dBm
Sensitivity, 1% PER	SENS	Signal is reference signal, packet length is 20 octets	—	-105.4	—	dBm
Co-channel interferer rejection, 1% PER	CCR	Desired signal 3 dB above sensitivity limit	—	-0.7	—	dB
Adjacent channel rejection, Interferer is reference signal, 1% PER, desired is reference signal at 3 dB above reference sensitivity level ²	ACR_{REF1}	Interferer is reference signal at +1 channel spacing	—	36.8	—	dB
		Interferer is reference signal at -1 channel spacing	—	37.5	—	dB
Alternate channel rejection, interferer is reference signal, 1% PER, desired is reference signal at 3 dB above reference sensitivity level ²	ACR_{REF2}	Interferer is reference signal at +2 channel spacing	—	48.9	—	dB
		Interferer is reference signal at -2 channel spacing	—	49.4	—	dB
Image rejection, 1% PER, desired is reference signal at 3 dB above reference sensitivity level ²	IR	Interferer is CW in image band ³	—	53.5	—	dB
Blocking rejection of all other channels, 1% PER, desired is reference signal at 3 dB above reference sensitivity level ² , interferer is reference signal	BLOCK	Interferer frequency < desired frequency -3 channel spacing	—	55.3	—	dB
		Interferer frequency > desired frequency +3 channel spacing	—	55.1	—	dB
RSSI resolution	RSSI_{RES}	-100 dBm to +5 dBm	—	0.25	—	dB
RSSI accuracy in the linear region as defined by 802.15.4-2020	RSSI_{LIN}		—	+/-6	—	dB

Note:

- Reference signal is defined as O-QPSK DSSS per 802.15.4, Frequency range = 2400-2483.5 MHz, Symbol rate = 62.5 ksym-bols/s.
- Reference sensitivity level is -85 dBm.
- Due to low-IF frequency, there is some overlap of adjacent channel and image channel bands. Adjacent channel CW blocker tests place the Interferer center frequency at the Desired frequency $\pm 5\text{ MHz}$ on the channel raster, whereas the image rejection test places the CW interferer near the image frequency of the Desired signal carrier, regardless of the channel raster.

4.9.2.3 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: $T_A = 25^\circ\text{C}$, $V_{\text{REGVDD}} = \text{IOVDD} = \text{AVDD} = \text{PAVDD} = 3.0\text{ V}$, $\text{RFVDD} = \text{DVDD} = 1.8\text{ V}$ powered from DCDC. Crystal frequency = 39.0 MHz, RF center frequency = 2.45 GHz, Packet length is 255 bytes.

Table 4.21. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal ¹	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload ²	—	-97.6	—	dBm
		Signal is reference signal, 255 byte payload ¹	—	-96	—	dBm
		With non-ideal signals ^{3 1}	—	-95.7	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes) ^{1 4}	—	8.7	—	dB
$N \pm 1$ Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset ^{1 5 4 6}	—	-5.4	—	dB
		Interferer is reference signal at -1 MHz offset ^{1 5 4 6}	—	-5.3	—	dB
$N \pm 2$ Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset ^{1 5 4 6}	—	-40.9	—	dB
		Interferer is reference signal at -2 MHz offset ^{1 5 4 6}	—	-39.7	—	dB
$N \pm 3$ Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset ^{1 5 4 6}	—	-45.5	—	dB
		Interferer is reference signal at -3 MHz offset ^{1 5 4 6}	—	-45.7	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision ^{1 6}	—	-23.3	—	dB
Selectivity to image frequency $\pm 1\text{ MHz}$	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision ^{1 6}	—	-40.9	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision ^{1 6}	—	-5.4	—	dB
Intermodulation performance	IM	$n = 3$ (see note ⁷)	—	-17.3	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1.
4. Desired signal -67 dBm.
5. Desired frequency $2402\text{ MHz} \leq F_c \leq 2480\text{ MHz}$.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4.

4.9.2.4 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: $T_A = 25^\circ\text{C}$, $V_{\text{REGVDD}} = \text{IOVDD} = \text{AVDD} = \text{PAVDD} = 3.0\text{ V}$, $\text{RFVDD} = \text{DVDD} = 1.8\text{ V}$ powered from DCDC. Crystal frequency = 39.0 MHz, RF center frequency = 2.45 GHz, Packet length is 255 bytes.

Table 4.22. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal ¹	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload ²	—	-94.8	—	dBm
		Signal is reference signal, 255 byte payload ¹	—	-93.3	—	dBm
		With non-ideal signals ^{3 1}	—	-93.1	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes) ^{1 4}	—	8.6	—	dB
$N \pm 1$ Adjacent channel selectivity	C/I_1	Interferer is reference signal at +2 MHz offset ^{1 5 4 6}	—	-5.3	—	dB
		Interferer is reference signal at -2 MHz offset ^{1 5 4 6}	—	-5.8	—	dB
$N \pm 2$ Alternate channel selectivity	C/I_2	Interferer is reference signal at +4 MHz offset ^{1 5 4 6}	—	-42.2	—	dB
		Interferer is reference signal at -4 MHz offset ^{1 5 4 6}	—	-44.2	—	dB
$N \pm 3$ Alternate channel selectivity	C/I_3	Interferer is reference signal at +6 MHz offset ^{1 5 4 6}	—	-48.1	—	dB
		Interferer is reference signal at -6 MHz offset ^{1 5 4 6}	—	-50.2	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision ^{1 6}	—	-22.8	—	dB
Selectivity to image frequency $\pm 2\text{ MHz}$	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz with 1 MHz precision ^{1 6}	—	-42.2	—	dB
		Interferer is reference signal at image frequency -2 MHz with 1 MHz precision ^{1 6}	—	-5.3	—	dB
Intermodulation performance	IM	$n = 3$ (see note ⁷)	—	-18.3	—	dBm

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1.
4. Desired signal -67 dBm.
5. Desired frequency $2402\text{ MHz} \leq F_c \leq 2480\text{ MHz}$.
6. With allowed exceptions.
7. As specified in Bluetooth Core specification version 5.1, Vol 6, Part A, Section 4.4.

4.9.2.5 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: $T_A = 25^\circ\text{C}$, $V_{\text{REGVDD}} = \text{IOVDD} = \text{AVDD} = \text{PAVDD} = 3.0\text{ V}$, $\text{RFVDD} = \text{DVDD} = 1.8\text{ V}$ powered from DCDC. Crystal frequency = 39.0 MHz, RF center frequency = 2.45 GHz, Packet length is 255 bytes.

Table 4.23. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal ¹	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload ²	—	-101.4	—	dBm
		Signal is reference signal, 255 byte payload ¹	—	-100.1	—	dBm
		With non-ideal signals ^{3 1}	—	-99.1	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes) ^{1 4}	—	2.7	—	dB
$N \pm 1$ Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset ^{1 5 4 6}	—	-7.1	—	dB
		Interferer is reference signal at -1 MHz offset ^{1 5 4 6}	—	-7.4	—	dB
$N \pm 2$ Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset ^{1 5 4 6}	—	-46.8	—	dB
		Interferer is reference signal at -2 MHz offset ^{1 5 4 6}	—	-49.7	—	dB
$N \pm 3$ Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset ^{1 5 4 6}	—	-49.4	—	dB
		Interferer is reference signal at -3 MHz offset ^{1 5 4 6}	—	-54.5	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision ^{1 6}	—	-49	—	dB
Selectivity to image frequency $\pm 1\text{ MHz}$	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision ^{1 6}	—	-49.4	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision ^{1 6}	—	-46.8	—	dB

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1.
4. Desired signal -72 dBm.
5. Desired frequency $2402\text{ MHz} \leq F_c \leq 2480\text{ MHz}$.
6. With allowed exceptions.

4.9.2.6 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: $T_A = 25^\circ\text{C}$, $V_{\text{REGVDD}} = \text{IOVDD} = \text{AVDD} = \text{PAVDD} = 3.0\text{ V}$, $\text{RFVDD} = \text{DVDD} = 1.8\text{ V}$ powered from DCDC. Crystal frequency = 39.0 MHz, RF center frequency = 2.45 GHz, Packet length is 255 bytes.

Table 4.24. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal ¹	—	10	—	dBm
Sensitivity	SENS	Signal is reference signal, 37 byte payload ²	—	-105.7	—	dBm
		Signal is reference signal, 255 byte payload ¹	—	-105.3	—	dBm
		With non-ideal signals ^{3 1}	—	-104.8	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes) ^{1 4}	—	0.9	—	dB
$N \pm 1$ Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset ^{1 5 4 6}	—	-12.4	—	dB
		Interferer is reference signal at -1 MHz offset ^{1 5 4 6}	—	-12.8	—	dB
$N \pm 2$ Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset ^{1 5 4 6}	—	-52.6	—	dB
		Interferer is reference signal at -2 MHz offset ^{1 5 4 6}	—	-55.5	—	dB
$N \pm 3$ Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset ^{1 5 4 6}	—	-53.8	—	dB
		Interferer is reference signal at -3 MHz offset ^{1 5 4 6}	—	-60	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision ^{1 6}	—	-53	—	dB
Selectivity to image frequency $\pm 1\text{ MHz}$	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision ^{1 6}	—	-53.8	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision ^{1 6}	—	-52.6	—	dB

Note:

1. 0.017% Bit Error Rate.
2. 0.1% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1.
4. Desired signal -79 dBm.
5. Desired frequency $2402\text{ MHz} \leq F_c \leq 2480\text{ MHz}$.
6. With allowed exceptions.

4.10 Oscillators

4.10.1 High Frequency Crystal Oscillator (HFXO)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.0 V. $T_A = 25\text{ }^{\circ}\text{C}$. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.25. High Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	F_{HFXO}	see note ^{1 2}	38.0	39.0	40.0	MHz
Supported crystal maximum equivalent series resistance (ESR)	ESR_{HFXO}	Crystal Frequency = 39.0 MHz	—	—	60	Ω
Supported range of crystal load capacitance ³	$C_{\text{L_HFXO}}$	39.0 MHz, ESR = 40 Ω ⁴	—	10	—	pF
Supply current	I_{HFXO}	39.0 MHz	—	565	—	μA
Startup time ⁵	T_{STARTUP}	39.0 MHz, ESR = 40 Ω , C_{L} = 10 pF	—	188	—	μs
On-chip tuning cap step size ⁶	SS_{HFXO}		—	0.04	—	pF

Note:

1. The BLE radio requires a 38.4 or 39.0 MHz crystal with a tolerance of ± 50 ppm over temperature and aging. Use a crystal with the recommended frequency and tolerance (refer to AN0016.2 for recommended crystals).
2. The radio requires additional software configuration based on crystal frequency. Refer to the Simplicity Studio component "RAIL Utility, Built-in PHYs Across HFXO Frequencies".
3. Total load capacitance as seen by the crystal.
4. RF performance characteristics have been determined using crystals with an ESR of 40 Ω and C_{L} of 10 pF.
5. Startup time does not include time implemented by programmable TIMEOUTSTEADY delay.
6. The tuning step size is the effective step size when incrementing both of the tuning capacitors by one count. The step size for the each of the individual tuning capacitors is twice this value.

4.10.2 Low Frequency Crystal Oscillator (LFXO)

Table 4.26. Low Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	F_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	—	—	80	k Ω
		GAIN = 1 to 3	—	—	100	k Ω
Supported range of crystal load capacitance ¹	C_{L_LFXO}	GAIN = 0	4	—	6	pF
		GAIN = 1	6	—	10	pF
		GAIN = 2 (see note ²)	10	—	12.5	pF
		GAIN = 3 (see note ²)	12.5	—	18	pF
Current consumption	I_{CL12p5}	ESR = 70 k Ω , C_L = 12.5 pF, GAIN ³ = 2, AGC ⁴ = 1	—	294	—	nA
Startup Time	$T_{STARTUP}$	ESR = 70 k Ω , C_L = 7 pF, GAIN ³ = 1, AGC ⁴ = 1	—	52	—	ms
On-chip tuning cap step size	SS_{LFXO}		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting ⁵	C_{LFXO_MIN}	CAPTUNE = 0	—	5.2	—	pF
On-chip tuning capacitor value at maximum setting ⁵	C_{LFXO_MAX}	CAPTUNE = 0x4F	—	26.2	—	pF

Note:

1. Total load capacitance seen by the crystal.
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register.
4. In LFXO_CFG Register.
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

4.10.3 High Frequency RC Oscillator (HFRCO)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.27. High Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	F _{HFRCO_ACC}	For all production calibrated frequencies	-3	—	3	%
Current consumption on all supplies ¹	I _{HFRCO}	F _{HFRCO} = 4 MHz	—	28	—	μA
		F _{HFRCO} = 5 MHz ²	—	29	—	μA
		F _{HFRCO} = 7 MHz	—	59	—	μA
		F _{HFRCO} = 10 MHz ²	—	63	—	μA
		F _{HFRCO} = 13 MHz	—	77	—	μA
		F _{HFRCO} = 16 MHz	—	87	—	μA
		F _{HFRCO} = 19 MHz	—	90	—	μA
		F _{HFRCO} = 20 MHz ²	—	107	—	μA
		F _{HFRCO} = 26 MHz	—	116	—	μA
		F _{HFRCO} = 32 MHz	—	139	—	μA
		F _{HFRCO} = 38 MHz ³	—	170	—	μA
		F _{HFRCO} = 40 MHz ²	—	172	—	μA
		F _{HFRCO} = 48 MHz ³	—	207	—	μA
		F _{HFRCO} = 56 MHz ³	—	228	—	μA
		F _{HFRCO} = 64 MHz ³	—	269	—	μA
		F _{HFRCO} = 80 MHz ³	—	285	—	μA
Clock Out current for HFRCODPLL ⁴	I _{CLKOUT_HFRCODPLL}	FORCEEN bit of HFRCO0_CTRL = 1	—	4.5	—	μA/MHz
Clock Out current for HFRCOEM23 ⁴	I _{CLKOUT_HFRCOEM23}	FORCEEN bit of HFRCOEM23_CTRL = 1	—	2.0	—	μA/MHz
Startup time ⁵	T _{STARTUP}	FREQRANGE = 0 to 7	—	1.2	—	μs
		FREQRANGE = 8 to 15	—	0.6	—	μs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Band frequency limits ⁶	$f_{\text{HFRCO_BAND}}$	FREQRANGE = 0	3.71	—	5.24	MHz
		FREQRANGE = 1	4.39	—	6.26	MHz
		FREQRANGE = 2	5.25	—	7.55	MHz
		FREQRANGE = 3	6.22	—	9.01	MHz
		FREQRANGE = 4	7.88	—	11.6	MHz
		FREQRANGE = 5	9.9	—	14.6	MHz
		FREQRANGE = 6	11.5	—	17.0	MHz
		FREQRANGE = 7	14.1	—	20.9	MHz
		FREQRANGE = 8	16.4	—	24.7	MHz
		FREQRANGE = 9	19.8	—	30.4	MHz
		FREQRANGE = 10	22.7	—	34.9	MHz
		FREQRANGE = 11	28.6	—	44.4	MHz
		FREQRANGE = 12	33.0	—	51.0	MHz
		FREQRANGE = 13	42.2	—	64.6	MHz
		FREQRANGE = 14	48.8	—	74.8	MHz
		FREQRANGE = 15	57.6	—	87.4	MHz

Note:

1. Does not include additional clock tree current. See specifications for additional current when selected as a clock source for a particular clock multiplexer.
2. This frequency is calibrated for the HFRCOEM23 only.
3. This frequency is calibrated for the HFRCODPLL (HFRCO0) only.
4. When the HFRCO is enabled for characterization using the FORCEEN bit, the total current will be the HFRCO core current plus the specified CLKOUT current. When the HFRCO is enabled on demand, the clock current may be different.
5. Hardware delay ensures settling to within $\pm 0.5\%$. Hardware also enforces this delay on a band change.
6. The frequency band limits represent the lowest and highest frequency which each band can achieve over the operating range.

4.10.4 Fast Start-Up RC Oscillator (FSRCO)**Table 4.28. Fast Start-Up RC Oscillator (FSRCO)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FSRCO frequency	F_{FSRCO}		17.2	20	21.2	MHz

4.10.5 Precision Low Frequency RC Oscillator (LFRCO)**Table 4.29. Precision Low Frequency RC Oscillator (LFRCO)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F _{LFRCO}		—	32.768	—	kHz
Frequency accuracy	F _{LFRCO_ACC}	Normal mode	-3	—	3	%
		Precision mode ¹ , across operating temperature range ²	-500	—	500	ppm
Startup time	t _{STARTUP}	Normal mode	—	204	—	μs
		Precision mode ¹	—	11.7	—	ms
Current consumption	I _{LFRCO}	Normal mode	—	189.9	—	nA
		Precision mode ¹ , T = stable at 25 °C ³	—	649.8	—	nA

Note:

1. The LFRCO operates in high-precision mode when CFG_HIGHPRECEN is set to 1. High-precision mode is not available in EM4.
2. Includes ± 40 ppm frequency tolerance of the HFXO crystal.
3. Includes periodic re-calibration against HFXO crystal oscillator.

4.10.6 Ultra Low Frequency RC Oscillator (ULFRCO)**Table 4.30. Ultra Low Frequency RC Oscillator (ULFRCO)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation Frequency	F _{ULFRCO}		0.944	1.0	1.095	kHz

4.11 GPIO Pins (GPIO)

Table 4.31. GPIO Pins (GPIO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, IOVDD = 1.71 V	—	1.9	—	nA
		MODEx = DISABLED, IOVDD = 3.0 V	—	2.5	—	nA
		MODEx = DISABLED, IOVDD = 3.8 V T_A = 125 °C, PB00-PB03, PC06-PC09, PA00	—	—	250	nA
		MODEx = DISABLED, IOVDD = 3.8 V T_A = 125 °C, All Other Pins	—	—	200	nA
Input low voltage ¹	V_{IL}	Any GPIO pin	—	—	0.3 * IOVDD	V
		RESETn	—	—	0.3 * DVDD	V
Input high voltage ¹	V_{IH}	Any GPIO pin	0.7 * IOVDD	—	—	V
		RESETn	0.7 * DVDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05 * IOVDD	—	—	V
		RESETn	0.05 * DVDD	—	—	V
Output high voltage	V_{OH}	Sourcing 20 mA, IOVDD = 3.0 V	0.8 * IOVDD	—	—	V
		Sourcing 8 mA, IOVDD = 1.71 V	0.6 * IOVDD	—	—	V
Output low voltage	V_{OL}	Sinking 20 mA, IOVDD = 3.0 V	—	—	0.2 * IOVDD	V
		Sinking 8 mA, IOVDD = 1.71 V	—	—	0.4 * IOVDD	V
GPIO rise time	T_{GPIO_RISE}	IOVDD = 3.0 V, C_{load} = 50 pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
		IOVDD = 1.71 V, C_{load} = 50 pF, SLEWRATE = 4, 10% to 90%	—	13	—	ns
GPIO fall time	T_{GPIO_FALL}	IOVDD = 3.0 V, C_{load} = 50 pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
		IOVDD = 1.71 V, C_{load} = 50 pF, SLEWRATE = 4, 90% to 10%	—	11.9	—	ns
Pull up/down resistance ²	R_{PULL}	Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0.	35	44	55	kΩ
		RESETn pin. Pull-up to DVDD	35	44	55	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RESETn low time to ensure pin reset	T _{RESET}		100	—	—	ns

Note:

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD.

4.12 Analog to Digital Converter (IADC)

Specified at 1 Msps, ADCCLK = 10 MHz, OSR=2, unless otherwise indicated.

Table 4.32. Analog to Digital Converter (IADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main analog supply	V _{AVDD}	Normal mode	1.71	—	3.8	V
Maximum input range ¹	V _{IN_MAX}	Maximum allowable input voltage	0	—	AVDD	V
Full-scale voltage	V _{FS}	Voltage required for full-scale measurement	—	V _{REF} / Gain	—	V
Input measurement range	V _{IN}	Differential mode - plus and minus inputs	-V _{FS}	—	+V _{FS}	V
		Single ended mode - one input tied to ground	0	—	V _{FS}	V
Input sampling capacitance	C _s	Analog Gain = 1x	—	1.8	—	pF
		Analog Gain = 2x	—	3.6	—	pF
		Analog Gain = 3x	—	5.4	—	pF
		Analog Gain = 4x	—	7.2	—	pF
		Analog Gain = 0.5x	—	0.9	—	pF
ADC clock frequency	f _{ADC_CLK}	Normal mode, Gain = 1x or 0.5x	—	—	10	MHz
		Normal mode, Gain = 2x	—	—	5	MHz
		Normal mode, Gain = 3x or 4x	—	—	2.5	MHz
Input sampling frequency	f _s	Normal mode	—	f _{ADC_CLK} /4	—	MHz
Throughput rate	f _{SAMPLE}	Normal mode, f _{ADC_CLK} = 10 MHz, OSR = 2	—	—	1	Msps
		Normal mode, f _{ADC_CLK} = 10 MHz, OSR = 32	—	—	76.9	ksps
Current from all supplies, Continuous operation	I _{ADC_CONT}	Normal Mode, 1 Msps, OSR = 2, f _{ADC_CLK} = 10 MHz	—	305	385	μA
Current in standby mode. ADC is not functional but can wake up in 1 μs.	I _{STBY}	Normal mode	—	17	—	μA
ADC Startup Time	t _{startup}	From power down state	—	5	—	μs
		From standby state	—	1	—	μs
Normal mode ADC resolution ²	Resolution	OSR = 2	—	12	—	bits
		OSR = 32	—	16	—	bits
Differential nonlinearity	DNL	Normal mode. Differential Input. OSR = 2 (No missing codes)	-1	+/- 0.25	1.5	LSB12
Integral nonlinearity	INL	Normal mode. Differential Input, OSR = 2	-2.5	+/- 0.65	2.5	LSB12

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Effective number of bits ³	ENOB	Normal Mode, Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21V	10.7	11.7	—	bits
		Normal Mode, Differential Input. Gain = 1x, OSR = 32, f_{IN} = 2.5 kHz, Internal VREF = 1.21 V.	—	13.5	—	bits
		Normal Mode, Differential Input. Gain = 1x, OSR = 32, f_{IN} = 2.5 kHz, External VREF = 1.25 V.	—	14.3	—	bits
Signal to Noise + Distortion Ratio Normal Mode ³	SNDR	Differential Input. Gain=1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21V	66	72.3	—	dB
		Differential Input. Gain=2x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21V	—	72.3	—	dB
		Differential Input. Gain=4x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21V	—	68.8	—	dB
		Differential Input. Gain=0.5x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21V	—	72.5	—	dB
		Differential Input. Gain = 1x, OSR = 64, f_{IN} = 1.25 kHz, Internal VREF = 1.21 V	—	83.9	—	dB
Total Harmonic Distortion	THD	Normal mode, Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V	—	-80.8	-70	dB
Spurious-Free Dynamic Range	SFDR	Normal mode, Differential Input. Gain = 1x, OSR = 2, f_{IN} = 10 kHz, Internal VREF = 1.21 V	72	86.5	—	dB
Common Mode Rejection Ratio	CMRR	Normal mode. DC to 100 Hz	—	87.0	—	dB
		Normal mode. AC high frequency.	—	68.6	—	dB
Power Supply Rejection Ratio	PSRR	Normal mode. DC to 100 Hz	—	80.4	—	dB
		Normal mode. AC high frequency, using internal VBGR	—	33.4	—	dB
		Normal mode. AC high frequency, using VREF pad	—	65.2	—	dB
External reference voltage range ¹	V_{EVREF}		1.0	—	AVDD	V
Offset Error, normal mode	OFFSET	GAIN = 1 and 0.5, Differential Input	-3	0.27	3	LSB12
		GAIN = 2, Differential Input	-4	0.27	4	LSB12
		GAIN = 3, Differential Input	-4	0.25	4	LSB12
		GAIN = 4, Differential Input	-4	0.29	4	LSB12

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Gain Error, Normal mode	GE	GAIN = 1 and 0.5, using external VREF, $f_{\text{ADC_CLK}} = 10 \text{ MHz}$	-0.6	-0.155	0.6	%
		GAIN = 2, using external VREF, $f_{\text{ADC_CLK}} = 5 \text{ MHz}$	-0.6	-0.155	0.6	%
		GAIN = 3, using external VREF, $f_{\text{ADC_CLK}} = 2.5 \text{ MHz}$	-0.7	0.186	0.7	%
		GAIN = 4, using external VREF, $f_{\text{ADC_CLK}} = 2.5 \text{ MHz}$	-1.1	0.227	1.1	%
		Internal VREF ⁴ , all GAIN settings	-1.5	0.023	1.5	%
Internal reference voltage	V_{IVREF}		—	1.21	—	V

Note:

1. When inputs are routed to external GPIO pins, the maximum pin voltage is limited to the lower of the IOVDD and AVDD supplies.
2. ADC output resolution depends on the OSR and digital averaging settings. With no digital averaging, ADC output resolution is 12 bits at OSR = 2, 13 bits at OSR = 4, 14 bits at OSR = 8, 15 bits at OSR = 16, 16 bits at OSR = 32 and 17 bits at OSR = 64. Digital averaging has a similar impact on ADC output resolution. See the product reference manual for additional details.
3. The relationship between ENOB and SNDR is specified according to the equation: $\text{ENOB} = (\text{SNDR} - 1.76) / 6.02$.
4. Includes error from internal VREF drift.

4.13 Analog Comparator (ACMP)

Table 4.33. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ACMP Supply current	I_{ACMP}	BIAS = 0 ¹ , HYST = DISABLED (100 °C max)	—	71	—	nA
		BIAS = 1 ¹ , HYST = DISABLED	—	270	—	nA
		BIAS = 2 ¹ , HYST = DISABLED	—	668	—	nA
		BIAS = 3 ¹ , HYST = DISABLED	—	2.5	—	μA
		BIAS = 4, HYST = DISABLED	—	5.4	—	μA
		BIAS = 5, HYST = DISABLED	—	10.6	—	μA
		BIAS = 6, HYST = DISABLED	—	27	—	μA
		BIAS = 7, HYST = DISABLED	—	50	100	μA
ACMP Supply current with Hysteresis ²	I_{ACMP_WHYS}	BIAS = 3 ¹ , HYST = SYM30MV	—	3.4	—	μA
		BIAS = 4, HYST = SYM30MV	—	7.3	—	μA
		BIAS = 5, HYST = SYM30MV	—	15	—	μA
		BIAS = 6, HYST = SYM30MV	—	38	—	μA
		BIAS = 7, HYST = SYM30MV	—	71	—	μA
Current consumption from VREFDIV in continuous mode	$I_{VREFDIV}$	NEGSEL = VREFDIVAVDD	—	3.2	—	μA
		NEGSEL = VREFDIV1V25	—	4.3	—	μA
		NEGSEL = VREFDIV2V5	—	7.1	—	μA
Current consumption from VREFDIV in sample/hold mode	$I_{VREFDIV_SH}$	NEGSEL = VREFDIV2V5LP	—	81	—	nA
		NEGSEL = VREFDIV1V25LP	—	74	—	nA
		NEGSEL = VREFDIVAVDDLP	—	76	—	nA
Current consumption from VSENSEDIV in continuous mode	$I_{VSENSEDIV}$	NEGSEL = VSENSE01DIV4	—	1.7	—	μA
Current consumption from VSENSEDIV in sample/hold mode	$I_{VSENSEDIV_SH}$	NEGSEL = VSENSE01DIV4LP	—	59.1	—	nA
Hysteresis (BIAS = 4) ²	V_{HYST}	HYST = SYM10MV ³	—	18	—	mV
		HYST = SYM20MV ³	—	33	—	mV
		HYST = SYM30MV ³	—	47	—	mV
Reference Voltage	$V_{ACMPREF}$	Internal 1.25 V Reference	1.19	1.25	1.31	V
		Internal 2.5 V Reference	2.34	2.5	2.75	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input offset voltage	V_{OFFSET}	BIAS = 0, $V_{\text{CM}} = 0.15$ to AVDD - 0.15 V	-25	—	25	mV
		BIAS = 3, $V_{\text{CM}} = 0.15$ to AVDD - 0.15 V	-25	—	25	mV
		BIAS = 4, $V_{\text{CM}} = 0.15$ to AVDD - 0.15 V	-25	—	25	mV
		BIAS = 7, $V_{\text{CM}} = 0.15$ to AVDD - 0.15 V	-30	—	30	mV
Input Range	V_{IN}	Input Voltage Range	0	—	AVDD	V
Comparator delay with 100 mV overdrive	T_{DELAY}	BIAS = 0, (100 °C max)	—	10	—	μs
		BIAS = 1	—	2.7	—	μs
		BIAS = 2	—	1.4	—	μs
		BIAS = 3	—	0.58	—	μs
		BIAS = 4	—	224	—	ns
		BIAS = 5	—	133	—	ns
		BIAS = 6	—	80	—	ns
		BIAS = 7	—	63	—	ns
Capacitive Sense Oscillator Resistance ⁴	R_{CSRESSEL}	CSRESSEL = 0	—	15.9	—	kΩ
		CSRESSEL = 1	—	25.3	—	kΩ
		CSRESSEL = 2	—	43.6	—	kΩ
		CSRESSEL = 3	—	61.9	—	kΩ
		CSRESSEL = 4	—	80.2	—	kΩ
		CSRESSEL = 5	—	98.6	—	kΩ
		CSRESSEL = 6	—	117	—	kΩ

Note:

1. When using the 1.25 V or 2.5 V VREF in continuous mode (VREFDIV1V25 or VREFDIV2V5) and BIAS < 4, an additional 1 μA of supply current is required.
2. Hysteresis is not supported for BIAS=0/1/2. Software should set HYST=DISABLED if using BIAS=0/1/2.
3. $V_{\text{CM}} = 1.25$ V
4. Capacitive Sense has been deprecated and is not recommended for use

4.14 Digital to Analog Converter (VDAC)

Table 4.34. Digital to Analog Converter (VDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage	V_{DACOUT}		0	—	VREF	V
Output Current	I_{DACOUT}		-10	—	10	mA
DAC clock frequency	f_{DAC}		—	—	1	MHz
Sample rate	SR_{DAC}	$f_{DAC} = f_{DAC(max)}$	—	—	500	ksps
Resolution	$N_{RESOLUTION}$		—	12	—	bits
Load Capacitance ¹	C_{LOAD}	High Power and Lower Power Modes	—	—	50	pF
		High Capacitance Load Mode	25	—	—	nF
Load Resistance	R_{LOAD}		5	—	—	k Ω
Current consumption, Dynamic, 500 ksps, 1 channel active ²	$I_{DAC_1_500}$	High Power Mode	—	281	—	μ A
		Low Power Mode	—	179	—	μ A
Current consumption, Dynamic, 500 ksps, 2 channels active ²	$I_{DAC_2_500}$	High Power Mode	—	445	—	μ A
		Low Power Mode	—	242	—	μ A
Current consumption, Static, 1 channel active ³	$I_{DAC_1_STAT}$	High Power Mode	—	135	—	μ A
		Low Power Mode	—	31	—	μ A
		High Capacitance Mode	—	43	—	μ A
Current consumption, Static, 2 channels active ³	$I_{DAC_2_STAT}$	High Power Mode	—	262	—	μ A
		Low Power Mode	—	53	—	μ A
		High Capacitance Mode	—	78	—	μ A
Startup time	$t_{DACSTARTUP}$	Enable to 90% full scale output, settling to 10 LSB	—	4.5	4.9	μ s
Settling time	$t_{DACSETTLE}$	High Power Mode, 25% to 75% of full scale, settling to 10 LSB	—	1.1	1.6	μ s
		Low Power Mode, 25% to 75% of full scale, settling to 1%	—	2.7	—	μ s
Output impedance	R_{OUT}	Main Output, High Power Mode	—	2.1	—	Ω
		Main Output, Low Power Mode	—	3.4	—	Ω
Power supply rejection ratio ⁴	PSRR	$V_{out} = 50\%$ full scale, DC output	—	88.6	—	dB
Signal to noise and distortion ratio	$SNDR_{DAC}$	High Power mode, 500 ksps, internal 2.5 V reference, 1 kHz sine wave input, BW limited to 250 kHz	65.8	67.2	—	dB
		High Power mode, 500 ksps, internal 2.5 V reference, 1 kHz sine wave input, BW limited to 22 kHz	68.0	70.6	—	dB
Total Harmonic Distortion	THD	High Power Mode, internal 2.5 V reference, 1 kHz sine wave input	—	-72.5	-68.7	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Integral Non-Linearity	INL _{DAC}	High Power Mode, Across full temperature range	-5	—	5	LSB
Differential Non-Linearity ⁵	DNL _{DAC}	High Power Mode, Across full temperature range	-1	—	1.3	LSB
Offset error ⁶	V _{OFFSET}	High Power mode	-15	—	15	mV
		Low Power Mode	-25	—	25	mV
		High Capacitance Load mode	-35	—	35	mV
Gain error ⁶	V _{GAIN}	1.25 V internal reference	-1.5	—	1.5	%
		2.5 V internal reference	-2	—	2	%
		External Reference	-0.6	—	0.6	%
External Reference Voltage ⁷	V _{EXTREF}		1.1	—	V _{AVDD}	V

Note:

1. Main outputs only.
2. Dynamic current specifications are for VDAC circuitry operating at max clock frequency with the output updated at the specified sampling rate using DMA transfers. Output is a 1 kHz sine wave from 10% to 90% full scale. Specified current does not include current required to drive the external load. Measurement includes all current from AVDD and DVDD supplies.
3. Static current specifications are for VDAC circuitry operating after a one-time update to a static output at 50% full scale, with the VDAC APB clock disabled. Specified current does not include current required to drive the external load. Measurement includes all current from AVDD and DVDD supplies.
4. PSRR calculated as $20 * \log_{10}(\Delta V_{DD} / \Delta V_{OUT})$.
5. Entire range is monotonic and has no missing codes.
6. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
7. External reference voltage on VREFP pin or PA00 when used for VREFP

4.15 Temperature Sensor

Table 4.35. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature sensor range ¹	T _{RANGE}		-40	—	125	°C
Temperature sensor resolution	T _{RESOLUTION}		—	0.25	—	°C
Measurement noise (RMS)	T _{NOISE}	Single measurement	—	0.6	—	°C
		16-sample average (TEMPAVG- NUM = 0)	—	0.17	—	°C
		64-sample average (TEMPAVG- NUM = 1)	—	0.12	—	°C
Temperature offset	T _{OFF}	Mean error of uncorrected output across full temperature range	—	3.2	—	°C
Temperature sensor accuracy ^{2 3}	T _{ACC}	Direct output accuracy after mean error (T _{OFF}) removed	—	+/-3	—	°C
		After linearization in software, no calibration	—	+/-2	—	°C
		After linearization in software, with single-temperature calibration at 25 °C ⁴	—	+/-1.5	—	°C
Measurement interval	t _{MEAS}		—	250	—	ms

Note:

1. The sensor reports absolute die temperature in Kelvin (K). All specifications are in °C to match the units of the specified product temperature range.
2. Error is measured as the deviation of the mean temperature reading from the expected die temperature. Accuracy numbers represent statistical minimum and maximum using ± 4 standard deviations of measured error.
3. The raw output of the temperature sensor is a predictable curve. It can be linearized with a polynomial function for additional accuracy.
4. Assuming calibration accuracy of ± 0.25 °C.

4.16 Brown Out Detectors

4.16.1 DVDD BOD

BOD thresholds on DVDD in EM0 and EM1 only, unless otherwise noted. Typical conditions are at $T_A = 25\text{ }^{\circ}\text{C}$. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.36. DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	$V_{\text{DVDD_BOD}}$	Supply Rising	—	1.67	1.71	V
		Supply Falling	1.62	1.65	—	V
BOD response time	$t_{\text{DVDD_BOD_DELAY}}$	Supply dropping at 100 mV/ μs slew rate ¹	—	0.95	—	μs
BOD hysteresis	$V_{\text{DVDD_BOD_HYS_T}}$		—	25	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.16.2 Low-Energy DVDD BOD

BOD thresholds on DVDD pin for low energy modes EM2 to EM4, unless otherwise noted.

Table 4.37. Low-Energy DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	$V_{\text{DVDD_LE_BOD}}$	Supply Falling	1.5	—	1.71	V
BOD response time	$t_{\text{DVDD_LE_BOD_DELAY}}$	Supply dropping at 2 mV/ μs slew rate ¹	—	50	—	μs
BOD hysteresis	$V_{\text{DVDD_LE_BOD_HYST}}$		—	20	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.16.3 AVDD and IOVDD BODs

BOD thresholds for AVDD BOD and IOVDD BOD. Available in all energy modes.

Table 4.38. AVDD and IOVDD BODs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{BOD}	Supply falling	1.45	—	1.71	V
BOD response time	t_{BOD_DELAY}	Supply dropping at 2 mV/ μ s slew rate ¹	—	50	—	μ s
BOD hysteresis	V_{BOD_HYST}		—	24	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.17 Pulse Counter (PCNT)

Table 4.39. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	1.0	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz
Setup time in asynchronous external clock mode	$t_{SU_S1N_S0N}$	S1N (data) to S0N (clock)	53	—	—	ns
Hold time in asynchronous external clock mode	$t_{HD_S0N_S1N}$	S0N (clock) to S1N (data)	47	—	—	ns

4.18 USART SPI Main Timing

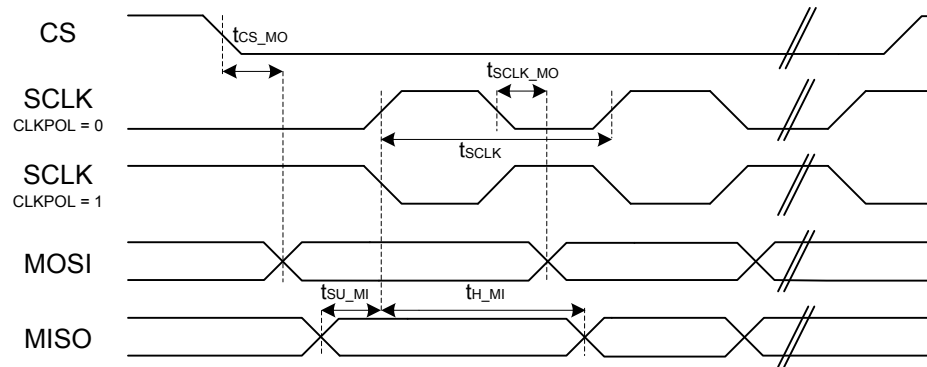


Figure 4.1. SPI Main Timing (SMSDELAY = 0)

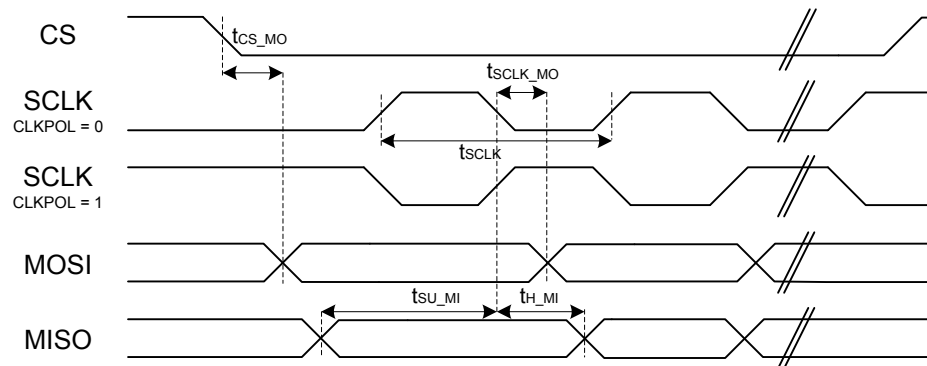


Figure 4.2. SPI Main Timing (SMSDELAY = 1)

4.18.1 USART SPI Main Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.40. USART SPI Main Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t _{SCLK}		2*t _{PCLK}	—	—	ns
CS to MOSI ^{1 2}	t _{CS_MO}		-15	—	15	ns
SCLK to MOSI ^{1 2}	t _{SCLK_MO}		-6	—	13	ns
MISO setup time ^{1 2}	t _{SU_MI}	IOVDD = 1.62 V	40	—	—	ns
		IOVDD = 3.0 V	31	—	—	ns
MISO hold time ^{1 2}	t _{H_MI}		-9	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.18.2 USART SPI Main Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.41. USART SPI Main Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t _{SCLK}		2*t _{PCLK}	—	—	ns
CS to MOSI ^{1 2}	t _{CS_MO}		-26	—	25	ns
SCLK to MOSI ^{1 2}	t _{SCLK_MO}		-7	—	24	ns
MISO setup time ^{1 2}	t _{SU_MI}	IOVDD = 1.62 V	50	—	—	ns
		IOVDD = 3.0 V	42	—	—	ns
MISO hold time ^{1 2}	t _{H_MI}		-9	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.19 USART SPI Secondary Timing

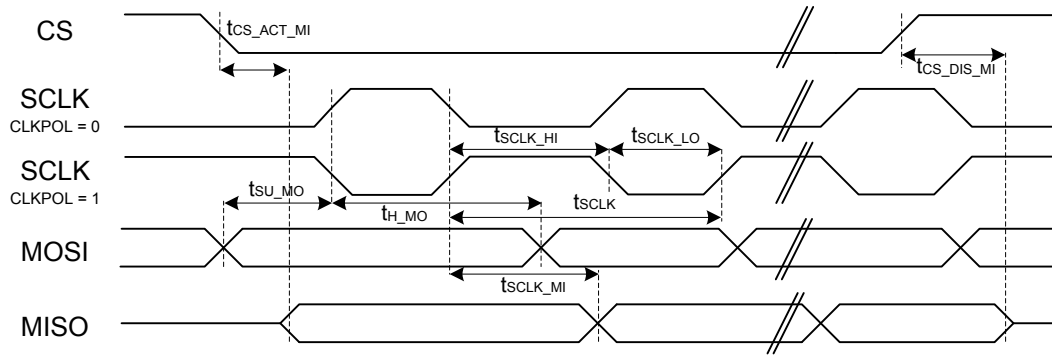


Figure 4.3. SPI Secondary Timing (SSSEARLY = 0)

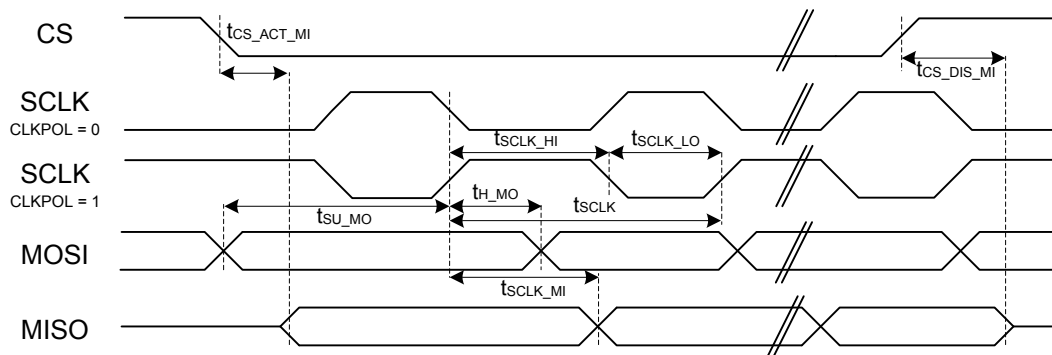


Figure 4.4. SPI Secondary Timing (SSSEARLY = 1)

4.19.1 USART SPI Secondary Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.42. USART SPI Secondary Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t _{SCLK}		6*t _{PCLK}	—	—	ns
SCLK high time ^{1 2 3}	t _{SCLK_HI}		2.5*t _{PCLK}	—	—	ns
SCLK low time ^{1 2 3}	t _{SCLK_LO}		2.5*t _{PCLK}	—	—	ns
CS active to MISO ^{1 2}	t _{CS_ACT_MI}		19	—	67	ns
CS disable to MISO ^{1 2}	t _{CS_DIS_MI}		24	—	89	ns
MOSI setup time ^{1 2}	t _{SU_MO}		12	—	—	ns
MOSI hold time ^{1 2 3}	t _{H_MO}		13	—	—	ns
SCLK to MISO ^{1 2 3}	t _{SCLK_MI}		14 + 1.5*t _{PCLK}	—	24 + 2.5*t _{PCLK}	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).
3. t_{PCLK} is one period of the selected PCLK.

4.19.2 USART SPI Secondary Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.43. USART SPI Secondary Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t _{SCLK}		6*t _{PCLK}	—	—	ns
SCLK high time ^{1 2 3}	t _{SCLK_HI}		2.5*t _{PCLK}	—	—	ns
SCLK low time ^{1 2 3}	t _{SCLK_LO}		2.5*t _{PCLK}	—	—	ns
CS active to MISO ^{1 2}	t _{CS_ACT_MI}		25	—	96	ns
CS disable to MISO ^{1 2}	t _{CS_DIS_MI}		24	—	87	ns
MOSI setup time ^{1 2}	t _{SU_MO}		13	—	—	ns
MOSI hold time ^{1 2 3}	t _{H_MO}		14	—	—	ns
SCLK to MISO ^{1 2 3}	t _{SCLK_MI}		17 + 1.5*t _{PCLK}	—	33 + 2.5*t _{PCLK}	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).
3. t_{PCLK} is one period of the selected PCLK.

4.20 EUSART SPI Main Timing

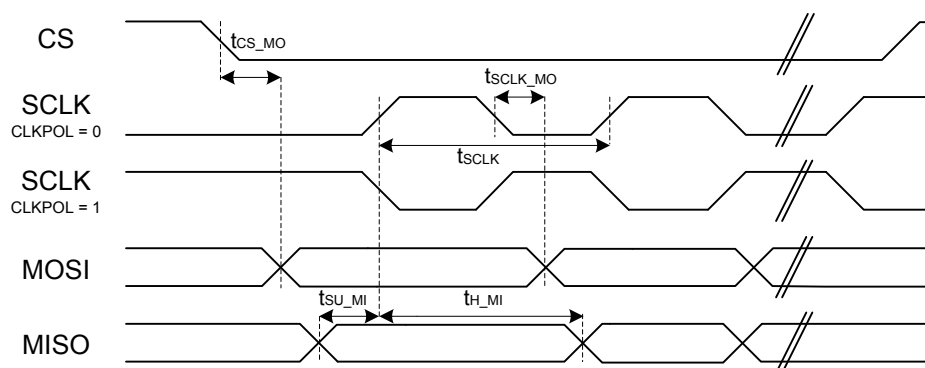


Figure 4.5. SPI Main Timing

4.20.1 EUSART SPI Main Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.44. EUSART SPI Main Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t_{SCLK}		t_{CLK}	—	—	ns
CS to MOSI ^{1 2}	t_{CS_MO}		-10	—	9	ns
SCLK to MOSI ^{1 2}	t_{SCLK_MO}		-3	—	8	ns
MISO setup time ^{1 2}	t_{SU_MI}		6	—	—	ns
MISO hold time ^{1 2}	t_{H_MI}		-21	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 15 pF output loading at 10% and 90% of V_{DD} .
3. t_{CLK} is one period of the selected peripheral clock: EM01GRPCLK for EUSART1/2, EUSART0CLK for EUSART0.

4.20.2 EUSART SPI Main Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.45. EUSART SPI Main Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 2 3}	t _{SCLK}		t _{CLK}	—	—	ns
CS to MOSI ^{1 2}	t _{CS_MO}		-19	—	15	ns
SCLK to MOSI ^{1 2}	t _{SCLK_MO}		-6	—	13	ns
MISO setup time ^{1 2}	t _{SU_MI}		10	—	—	ns
MISO hold time ^{1 2}	t _{H_MI}		-13	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 15 pF output loading at 10% and 90% of V_{DD}.
3. t_{CLK} is one period of the selected peripheral clock: EM01GRPCCLK for EUSART1/2, EUSART0CLK for EUSART0.

4.21 EUSART SPI Secondary Timing

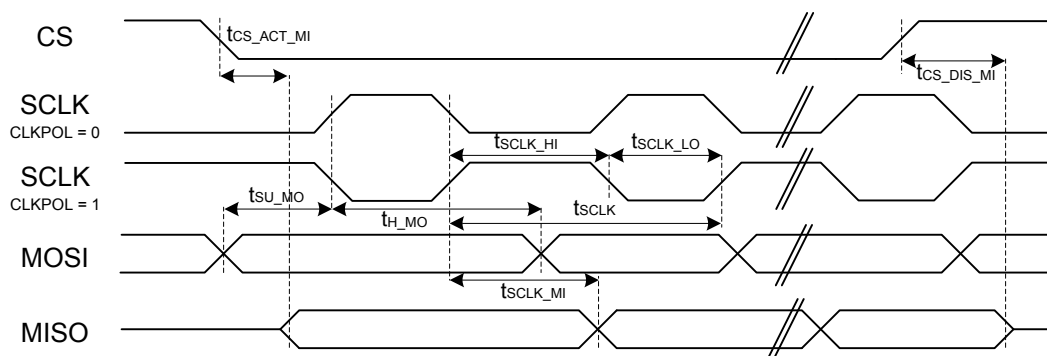


Figure 4.6. SPI Secondary Timing

4.21.1 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE2

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.46. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE2

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time ^{1 2}	$t_{\text{SCLK_HI}}$		50	—	—	ns
SCLK low time ^{1 2}	$t_{\text{SCLK_LO}}$		50	—	—	ns
CS active to MISO ^{1 2}	$t_{\text{CS_ACT_MI}}$		4	—	49	ns
CS disable to MISO ^{1 2}	$t_{\text{CS_DIS_MI}}$		5	—	34	ns
MOSI setup time ^{1 2}	$t_{\text{SU_MO}}$		5	—	—	ns
MOSI hold time ^{1 2}	$t_{\text{H_MO}}$		6	—	—	ns
SCLK to MISO ^{1 2}	$t_{\text{SCLK_MI}}$	IOVDD = 1.8 V	8	—	40	ns
		IOVDD = 3.0 V	8	—	30	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 15 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

4.21.2 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE1

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD) on consecutive pins. All GPIO set to slew rate = 6.

Table 4.47. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time ^{1 2}	t _{SCLK_HI}		50	—	—	ns
SCLK low time ^{1 2}	t _{SCLK_LO}		50	—	—	ns
CS active to MISO ^{1 2}	t _{CS_ACT_MI}		6	—	75	ns
CS disable to MISO ^{1 2}	t _{CS_DIS_MI}		5	—	56	ns
MOSI setup time ^{1 2}	t _{SU_MO}		4	—	—	ns
MOSI hold time ^{1 2}	t _{H_MO}		6	—	—	ns
SCLK to MISO ^{1 2}	t _{SCLK_MI}	IOVDD = 1.8 V	9	—	49	ns
		IOVDD = 3.0 V	9	—	41	ns
Note: 1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0). 2. Measurement done with 15 pF output loading at 10% and 90% of V _{DD} (figure shows 50% of V _{DD}).						

4.21.3 EUSART SPI Secondary Timing, Voltage Scaling = VSCALE0

Timing specifications at VSCALE0 apply to EUSART0 only, routed to DBUSAB on consecutive pins. All GPIO set to slew rate = 6.

Table 4.48. EUSART SPI Secondary Timing, Voltage Scaling = VSCALE0

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK high time ^{1 2}	t _{SCLK_HI}		100	—	—	ns
SCLK low time ^{1 2}	t _{SCLK_LO}		100	—	—	ns
CS active to MISO ^{1 2}	t _{CS_ACT_MI}		8	—	100	ns
CS disable to MISO ^{1 2}	t _{CS_DIS_MI}		7	—	70	ns
MOSI setup time ^{1 2}	t _{SU_MO}		9	—	—	ns
MOSI hold time ^{1 2}	t _{H_MO}		32	—	—	ns
SCLK to MISO ^{1 2}	t _{SCLK_MI}	IOVDD = 1.8 V	11	—	86	ns
		IOVDD = 3.0 V	11	—	78	ns
Note: 1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0). 2. Measurement done with 15 pF output loading at 10% and 90% of V _{DD} (figure shows 50% of V _{DD}).						

4.22 I2C Electrical Specifications

4.22.1 I2C Standard-mode (Sm)

CLHR set to 0 in the I2Cn_CTRL register.

Table 4.49. I2C Standard-mode (Sm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ¹	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	μs
SCL clock high time	t_{HIGH}		4	—	—	μs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	μs
Repeated START condition hold time	t_{HD_STA}		4.0	—	—	μs
STOP condition set-up time	t_{SU_STO}		4.0	—	—	μs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	μs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.22.2 I2C Fast-mode (Fm)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.50. I2C Fast-mode (Fm)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ¹	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	μs
SCL clock high time	t_{HIGH}		0.6	—	—	μs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time	t_{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	μs
Repeated START condition hold time	t_{HD_STA}		0.6	—	—	μs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	μs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	μs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.22.3 I2C Fast-mode Plus (Fm+)

CLHR set to 1 in the I2Cn_CTRL register.

Table 4.51. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ¹	f _{SCL}		0	—	1000	kHz
SCL clock low time	t _{LOW}		0.5	—	—	μs
SCL clock high time	t _{HIGH}		0.26	—	—	μs
SDA set-up time	t _{SU_DAT}		50	—	—	ns
SDA hold time	t _{HD_DAT}		0	—	—	ns
Repeated START condition set-up time	t _{SU_STA}		0.26	—	—	μs
Repeated START condition hold time	t _{HD_STA}		0.26	—	—	μs
STOP condition set-up time	t _{SU_STO}		0.26	—	—	μs
Bus free time between a STOP and START condition	t _{BUF}		0.5	—	—	μs

Note:

1. The maximum SCL clock frequency listed is assuming that an arbitrary clock frequency is available. The maximum attainable SCL clock frequency may be slightly less using the HFXO or HFRCO due to the limited frequencies available. The CLKDIV should be set to a value that keeps the SCL clock frequency below the max value listed.

4.23 Boot Timing

Secure boot impacts the recovery time from all sources of device reset. In addition to the root code authentication process, which cannot be disabled or bypassed, the root code can authenticate a bootloader, and the bootloader can authenticate the application. In projects that include only an application and no bootloader, the root code can authenticate the application directly. The duration of each authentication operation depends on two factors: the computation of the associated image hash, which is proportional to the size of the image, and the verification of the image signature, which is independent of image size.

The duration for the root code to authenticate the bootloader will depend on the SE firmware version as well as on the size of the bootloader.

The duration for the bootloader to authenticate the application can depend on the size of the application.

The configurations below assume that the associated bootloader and application code images do not contain a bootloader certificate or an application certificate. Authenticating a bootloader certificate or an application certificate will extend the boot time by an additional 6 to 7 ms.

The table below provides the durations from the termination of reset until the completion of the secure boot process (start of main() function in the application image) under various conditions.

Conditions:

- SE firmware version 2.1.5
- Gecko Bootloader size 10.2 KB

Timing is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

Table 4.52. Boot Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Boot time	t _{BOOT}	Secure boot application check disabled, no bootloader	—	30.5	—	ms
		Secure boot application check disabled, second stage bootloader check enabled ¹ , 50 KB application size	—	37.7	—	ms
		Secure boot application check enabled, second stage bootloader check enabled ¹ , 50 KB application size	—	48.3	—	ms
		Secure boot application check enabled, second stage bootloader check enabled ¹ , 150 KB application size	—	51.0	—	ms
		Secure boot application check enabled, second stage bootloader check enabled ¹ , 350 KB application size	—	56.4	—	ms

Note:

1. Timing is measured with the specified bootloader size. Actual bootloader size will impact the boot timing slightly, with a similar μs / KB ratio as application size.

4.24 Crypto Operation Timing for SE Manager API

Values in this table represent timing from SE Manager API call to return. The Cortex-M33 HCLK frequency is 39.0 MHz. The timing specifications below are measured at the SE Manager function call API. Each duration in the table contains some portion that is influenced by SE Manager build compilation and Cortex-M33 operating frequency and some portion that is influenced by the Hardware Secure Engine's firmware version and its operating speed (typically 80 MHz). The contributions of the Cortex-M33 properties to the overall specification timing are most pronounced for the shorter operations such as AES and hash when operating on small payloads. The overhead of command processing at the mailbox interface can also dominate the timing for shorter operations.

Conditions:

- SE firmware version 2.1.5
- GSDK version 3.2

Timing is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

Table 4.53. Crypto Operation Timing for SE Manager API

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AES-128 timing	t_{AES128}	AES-128 CCM encryption, PT 1 KB	—	571	—	μs
		AES-128 CCM encryption, PT 32 KB	—	1751	—	μs
		AES-128 CTR encryption, PT 1 KB	—	474	—	μs
		AES-128 CTR encryption, PT 32 KB	—	1043	—	μs
		AES-128 GCM encryption, PT 1 KB	—	522	—	μs
		AES-128 GCM encryption, PT 32 KB	—	1087	—	μs
AES-256 timing	t_{AES256}	AES-256 CCM encryption, PT 1 KB	—	585	—	μs
		AES-256 CCM encryption, PT 32 KB	—	2184	—	μs
		AES-256 CTR encryption, PT 1 KB	—	482	—	μs
		AES-256 CTR encryption, PT 32 KB	—	1255	—	μs
		AES-256 GCM encryption, PT 1 KB	—	529	—	μs
		AES-256 GCM encryption, PT 32 KB	—	1306	—	μs
ECC P-256 timing	$t_{\text{ECC_P256}}$	ECC key generation, P-256	—	5.5	—	ms
		ECC signing, P-256	—	5.9	—	ms
		ECC verification, P-256	—	6.2	—	ms
ECC P-25519 timing ¹	$t_{\text{ECC_P25519}}$	ECC key generation, P-25519	—	4.5	—	ms
		ECC signing, P-25519	—	8.9	—	ms
		ECC verification, P-25519	—	6.3	—	ms
ECDH compute secret timing	t_{ECDH}	ECDH compute secret, P-25519 ¹	—	4.5	—	ms
		ECDH compute secret, P-256	—	5.6	—	ms
ECJPAKE client timing	$t_{\text{ECJPAKE_C}}$	ECJPAKE client write round one	—	21.4	—	ms
		ECJPAKE client read round one	—	11.7	—	ms
		ECJPAKE client write round two	—	15.2	—	ms
		ECJPAKE client read round two	—	6.3	—	ms
		ECJPAKE client derive secret	—	8.8	—	ms

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ECJPAKE server timing	t _{ECJPAKE_S}	ECJPAKE server write round one	—	21.4	—	ms
		ECJPAKE server read round one	—	11.7	—	ms
		ECJPAKE server write round two	—	15.3	—	ms
		ECJPAKE server read round two	—	6.4	—	ms
		ECJPAKE server derive secret	—	8.8	—	ms
SHA-256 timing	t _{SHA256}	SHA-256, PT 1 KB	—	308	—	μs
		SHA-256, PT 32 KB	—	737	—	μs
Note: 1. Option is not available on Secure Vault Mid devices with SE firmware earlier than v2.1.7.						

4.25 Crypto Operation Average Current for SE Manager API

Values in this table represent current consumed by security core during the operation, and represent additions to the current consumed by the Cortex-M33 application CPU due to the Hardware Secure Engine CPU and its associated crypto accelerators. The current measurements below represent the average value of the current for the duration of the crypto operation. Instantaneous peak currents may be higher.

Conditions:

- SE firmware version 2.1.5
- GSDK version 3.2

Current consumption is expected to be similar for subsequent SE firmware versions. Refer to SE firmware release notes for any significant changes.

Table 4.54. Crypto Operation Average Current for SE Manager API

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AES-128 current	I_{AES128}	AES-128 CCM encryption, PT 1 KB	—	0.9	—	mA
		AES-128 CCM encryption, PT 32 KB	—	3.9	—	mA
		AES-128 CTR encryption, PT 1 KB	—	0.8	—	mA
		AES-128 CTR encryption, PT 32 KB	—	3.8	—	mA
		AES-128 GCM encryption, PT 1 KB	—	0.8	—	mA
		AES-128 GCM encryption, PT 32 KB	—	3.8	—	mA
AES-256 current	I_{AES256}	AES-256 CCM encryption, PT 1 KB	—	1.0	—	mA
		AES-256 CCM encryption, PT 32 KB	—	4.0	—	mA
		AES-256 CTR encryption, PT 1 KB	—	0.8	—	mA
		AES-256 CTR encryption, PT 32 KB	—	4.0	—	mA
		AES-256 GCM encryption, PT 1 KB	—	0.8	—	mA
		AES-256 GCM encryption, PT 32 KB	—	3.9	—	mA
ECC P-256 current	I_{ECCP256}	ECC key generation, P-256	—	1.7	—	mA
		ECC signing, P-256	—	1.6	—	mA
		ECC verification, P-256	—	1.7	—	mA
ECC P-25519 current ¹	$I_{\text{ECCP25519}}$	ECC key generation, P-25519	—	1.6	—	mA
		ECC signing, P-25519	—	1.6	—	mA
		ECC verification, P-25519	—	1.6	—	mA
ECDH compute secret current	I_{ECDH}	ECDH compute secret, P-25519 ¹	—	1.5	—	mA
		ECDH compute secret, P-256	—	1.6	—	mA
ECJPAKE client current	$I_{\text{ECJPAKE_C}}$	ECJPAKE client write round one	—	1.7	—	mA
		ECJPAKE client read round one	—	1.7	—	mA
		ECJPAKE client write round two	—	1.7	—	mA
		ECJPAKE client read round two	—	1.7	—	mA
		ECJPAKE client derive secret	—	1.7	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ECJPAKE server current	I _{ECJPAKE_S}	ECJPAKE server write round one	—	1.7	—	mA
		ECJPAKE server read round one	—	1.7	—	mA
		ECJPAKE server write round two	—	1.7	—	mA
		ECJPAKE server read round two	—	1.6	—	mA
		ECJPAKE server derive secret	—	1.7	—	mA
SHA-256 current	I _{SHA256}	SHA-256, PT 1 KB	—	0.7	—	mA
		SHA-256, PT 32 KB	—	2.3	—	mA
Note: 1. Option is not available on Secure Vault Mid devices with SE firmware earlier than v2.1.7.						

4.26 Matrix Vector Processor (MVP)

All measurements are in comparison to EM1 baseline current at given VSCALE and Clock settings. Matrix dimensions are X = 24 x 32, Y = 32 x 24 and Z = 24 x 24.

Table 4.55. Matrix Vector Processor (MVP)

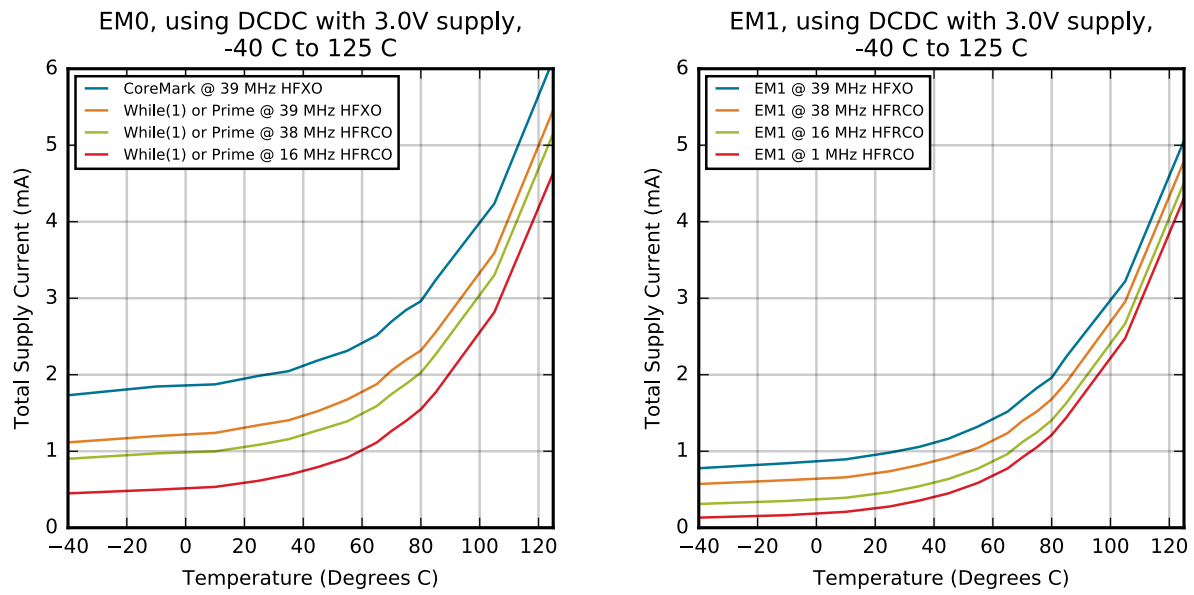
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
MVP Enable Current	I _{EN}	VSCALE1, HFXO @ 39 MHz	—	16.8	—	μA
		VSCALE2, HFRCO w/ DPLL @ 78 MHz	—	41.2	—	μA
Matrix Multiplication Duration using MVP Hardware	T _{MVP_MULTIPLY}	16-bit complex numbers, fully banked memory, VSCALE1, HFXO @ 39 MHz	—	504.0	—	μs
		16-bit complex numbers, fully banked memory, VSCALE2, HFRCO w/ DPLL @ 78 MHz	—	252.0	—	μs
		16-bit complex numbers, interleaved memory, VSCALE1, HFXO @ 39 MHz	—	596.2	—	μs
		16-bit complex numbers, interleaved memory, VSCALE2, HFRCO w/ DPLL @ 78 MHz	—	298.2	—	μs
Matrix Multiplication Duration using Software	T _{SW_MULTIPLY}	16-bit complex numbers, interleaved memory, VSCALE1, HFXO @ 39 MHz	—	41.0	—	ms
		16-bit complex numbers, interleaved memory, VSCALE2, HFRCO w/ DPLL @ 78 MHz	—	20.5	—	ms
		32-bit complex numbers, interleaved memory, VSCALE1, HFXO @ 39 MHz	—	19.7	—	ms
		32-bit complex numbers, interleaved memory, VSCALE2, HFRCO w/ DPLL @ 78 MHz	—	9.9	—	ms
Matrix Multiplication Current using MVP Hardware	I _{MVP_MULTIPLY}	16-bit complex numbers, fully banked memory, VSCALE1, HFXO @ 39 MHz	—	61.3	—	μA/MHz
		16-bit complex numbers, fully banked memory, VSCALE2, HFRCO w/ DPLL @ 78 MHz	—	62.4	—	μA/MHz
		16-bit complex numbers, interleaved memory, VSCALE1, HFXO @ 39 MHz	—	53.2	—	μA/MHz
		16-bit complex numbers, interleaved memory, VSCALE2, HFRCO w/ DPLL @ 78 MHz	—	53.8	—	μA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Matrix Multiplication Current using Software	I _{SW_MULTIPLY}	16-bit complex numbers, interleaved memory, VSCALE1, HFXO @ 39 MHz	—	41.7	—	μA/MHz
		16-bit complex numbers, interleaved memory, VSCALE2, HFRCO w/ DPLL @ 78 MHz	—	44.7	—	μA/MHz
		32-bit complex numbers, interleaved memory, VSCALE1, HFXO @ 39 MHz	—	31.9	—	μA/MHz
		32-bit complex numbers, interleaved memory, VSCALE2, HFRCO w/ DPLL @ 78 MHz	—	33.8	—	μA/MHz

4.27 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.27.1 Supply Current



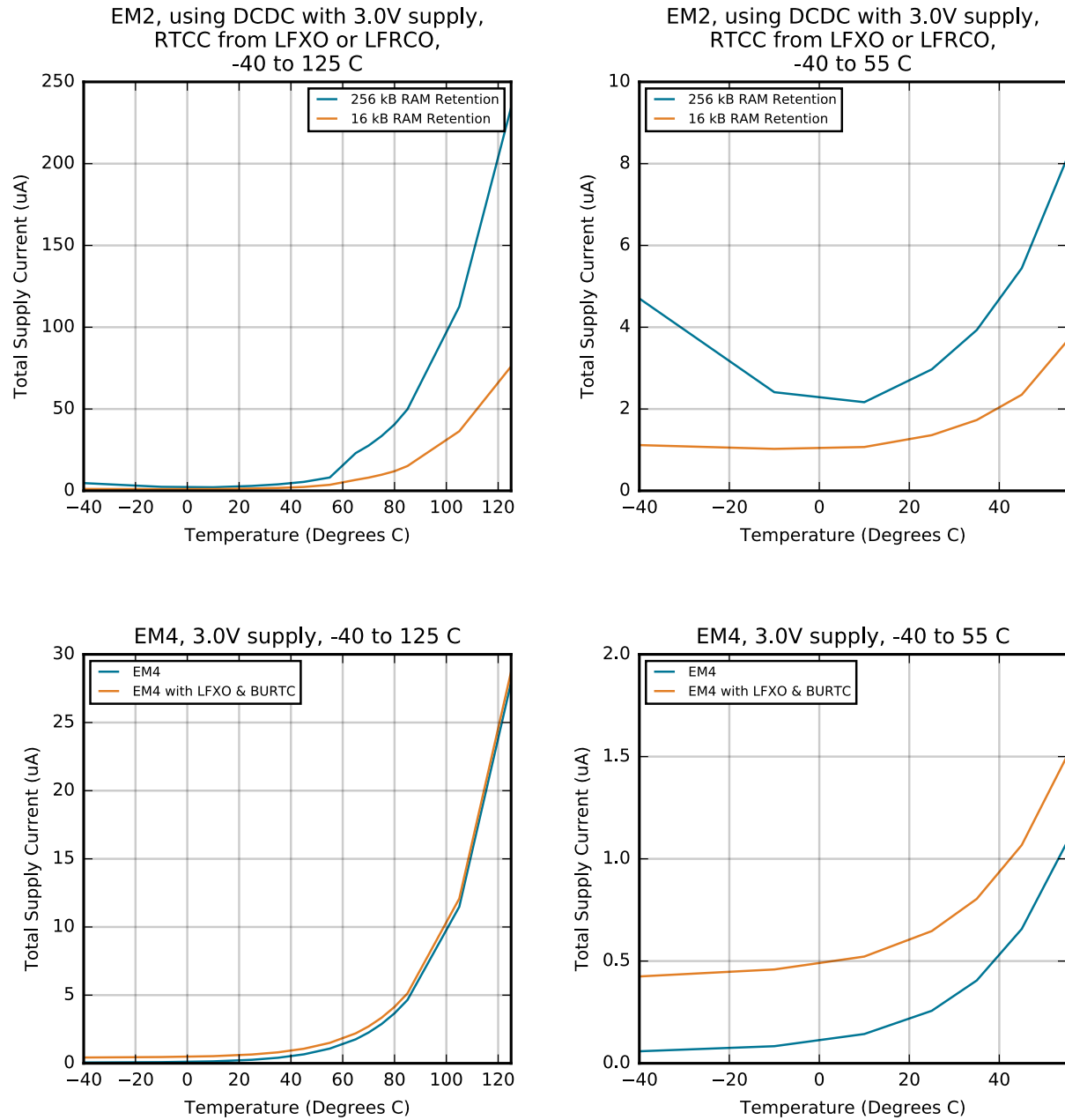


Figure 4.8. EM2 and EM4 Typical Supply Current vs. Temperature

4.27.2 RF Characteristics

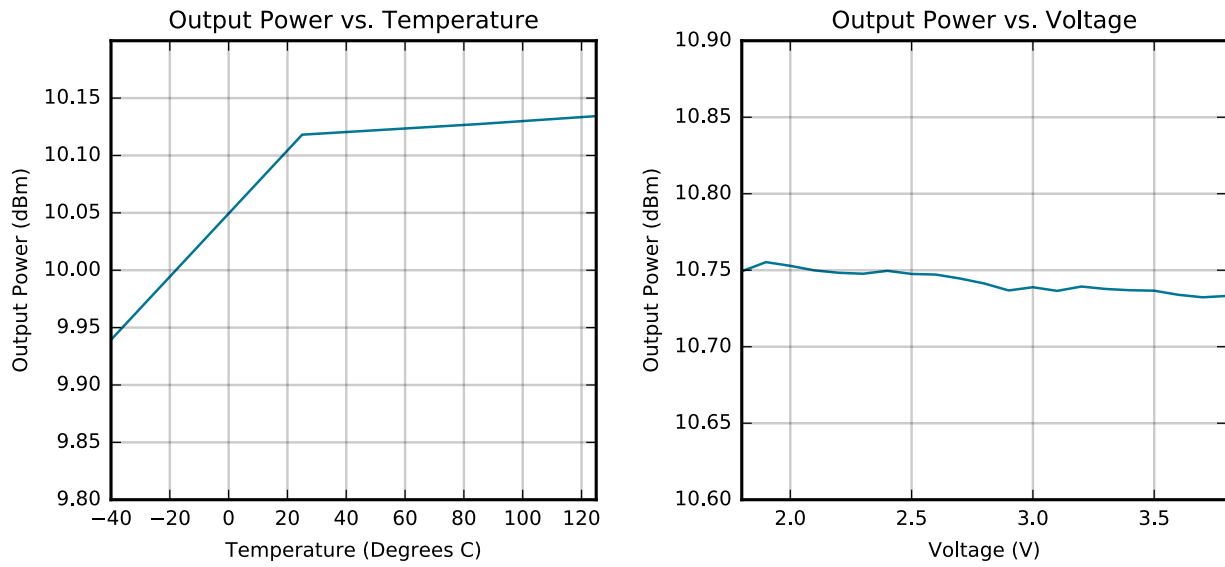


Figure 4.9. 2.4 GHz 10 dBm PA RF Transmitter Output Power (Pout=10 dBm)

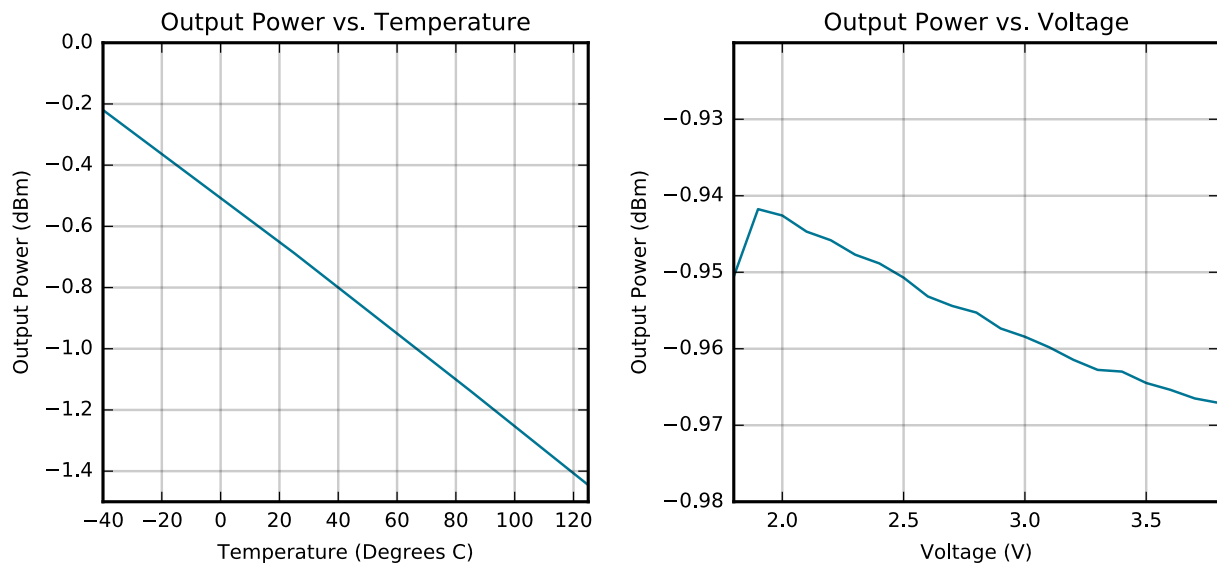


Figure 4.10. 2.4 GHz 0 dBm PA RF Transmitter Output Power (Pout=0 dBm)

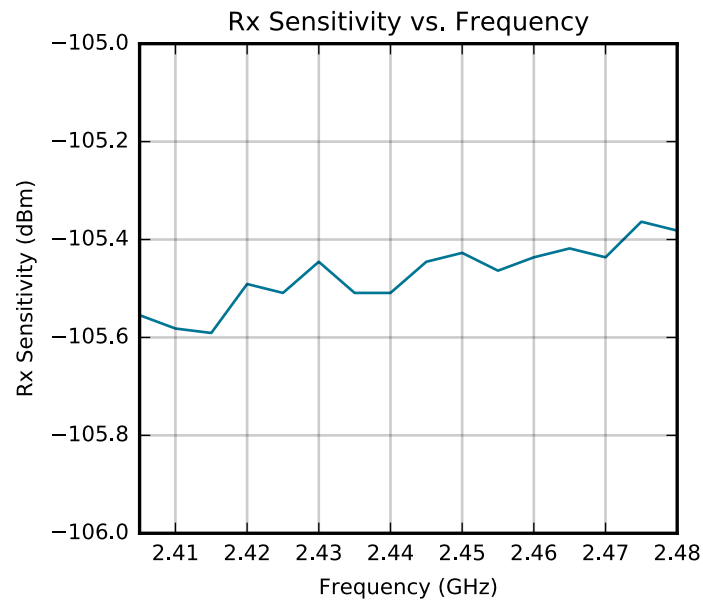


Figure 4.11. 2.4 GHz 802.15.4 RF Receiver Sensitivity

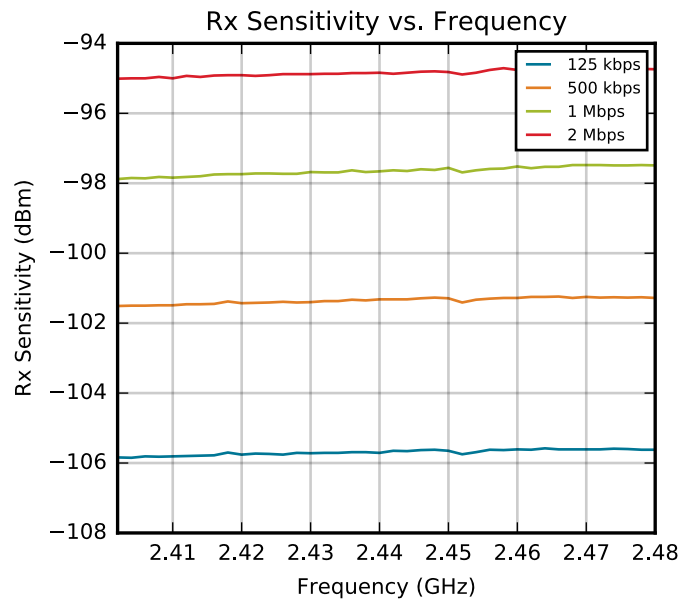


Figure 4.12. 2.4 GHz BLE RF Receiver Sensitivity

4.27.3 DC-DC Converter

Performance characterized with Murata DFE2HCAH2R2MJ0 ($L_{DCDC} = 2.2 \mu\text{H}$) and TDK CGA5L3X8R1C475K160AB ($C_{DCDC} = 4.7 \mu\text{F}$)

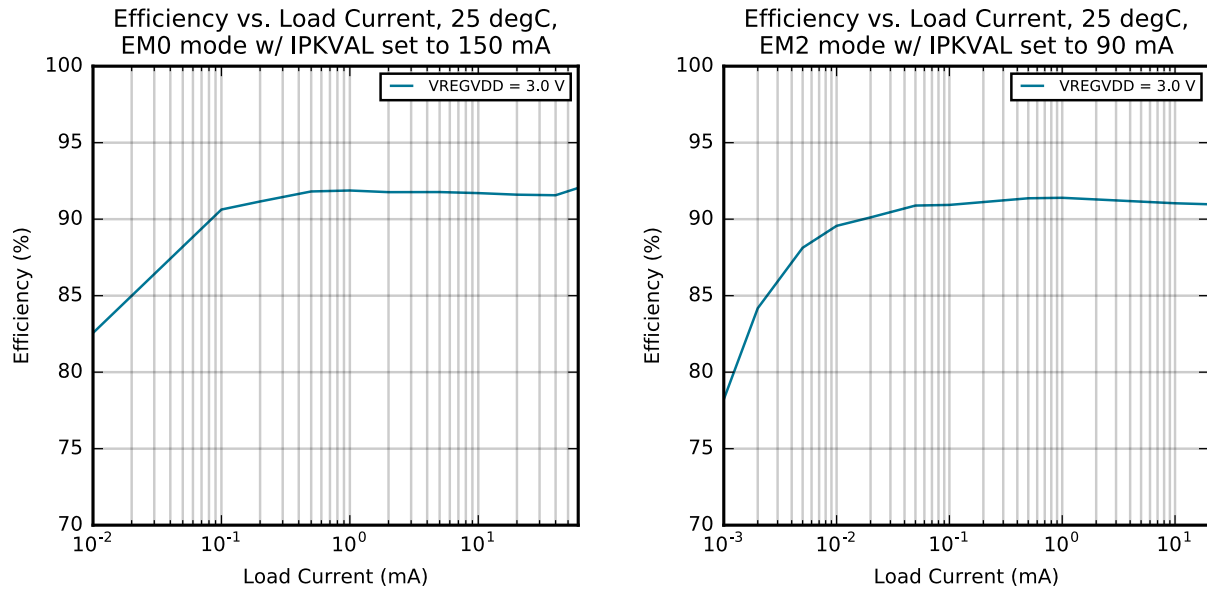


Figure 4.13. DC-DC Efficiency

4.27.4 IADC

Typical performance is shown using 10 MHz ADC clock for fastest sampling speed and adjusting oversampling ratio (OSR).

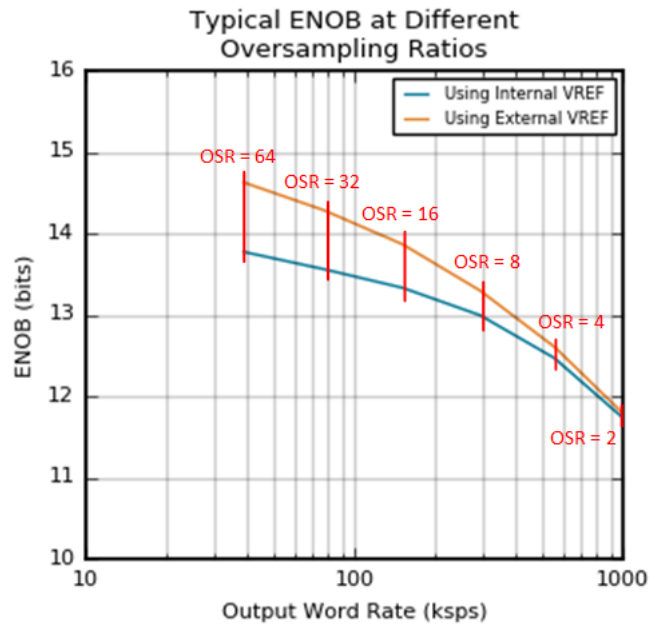


Figure 4.14. Typical ENOB vs. Oversampling Ratio

4.27.5 GPIO

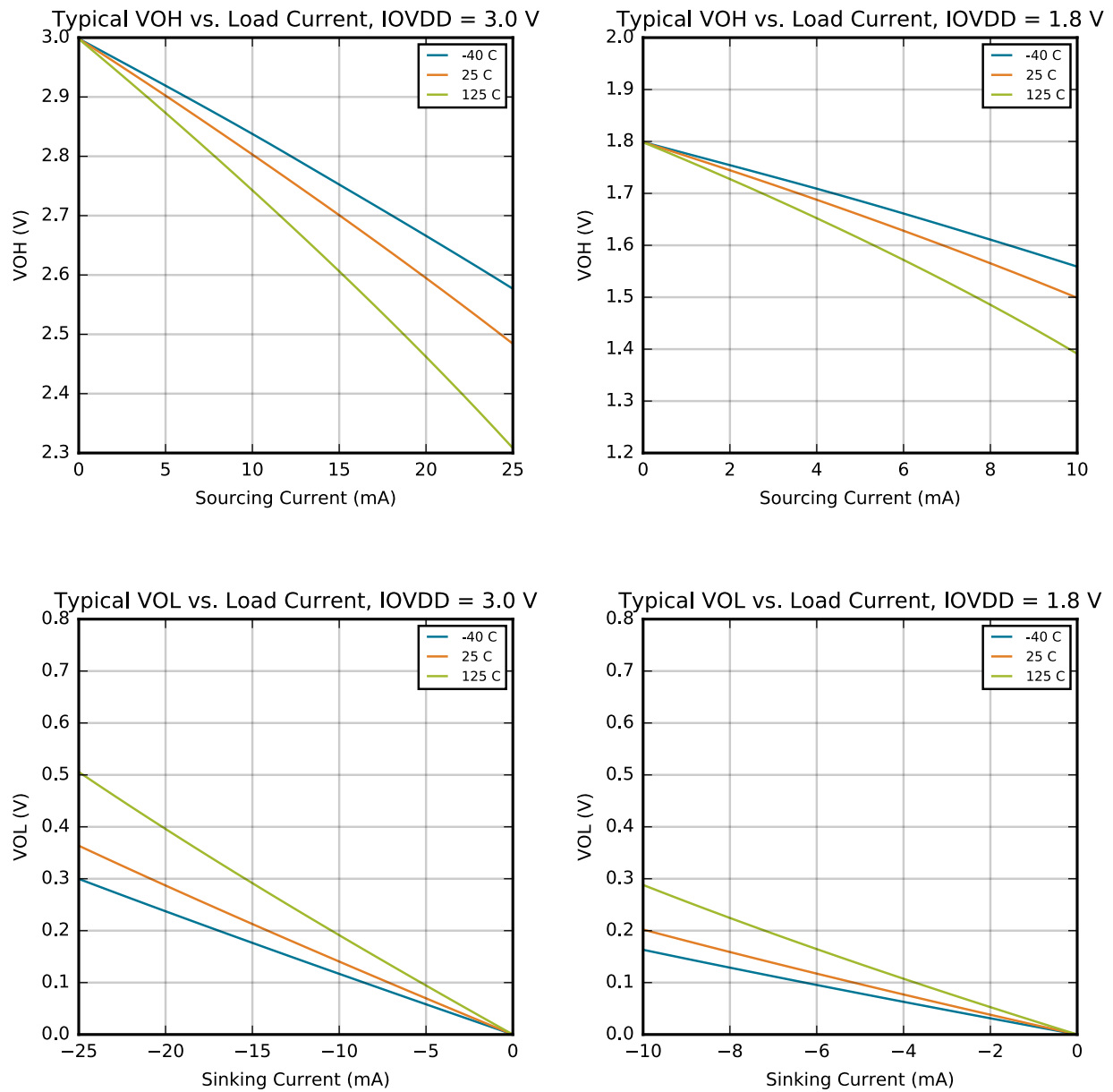


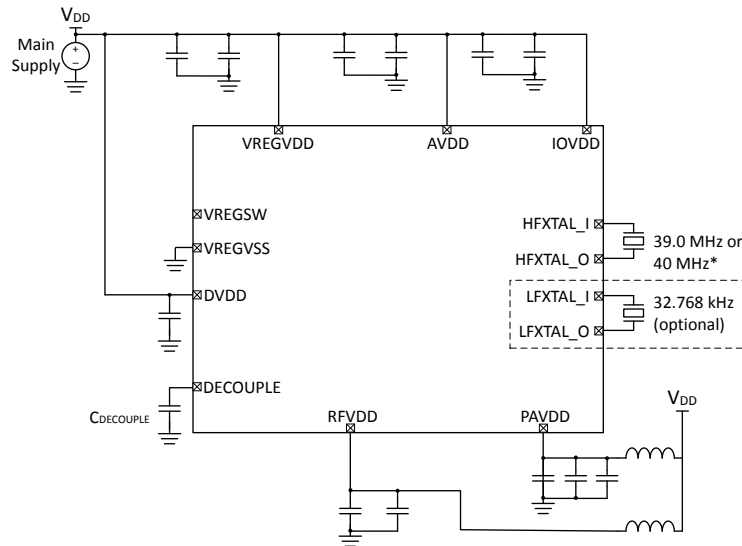
Figure 4.15. VOH and VOL vs. Load Current

5. Typical Connections

5.1 Power

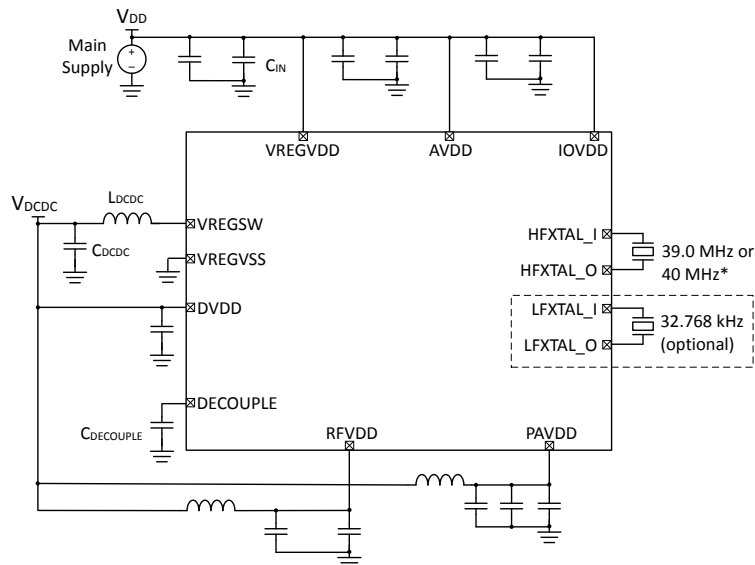
Typical power supply connections are shown in the following figures.

Note: PAVDD, RFVDD, AVDD, and IOVDD supply connections are flexible. They may be connected in other configurations or to external supplies as long as the supply limits described in [4.1 Electrical Characteristics](#) are met.



*40 MHz required for applications using Channel Sounding

Figure 5.1. EFR32BG24L Typical Application Circuit: Direct Supply Configuration without DCDC



*40 MHz required for applications using Channel Sounding

Figure 5.2. EFR32BG24L Typical Application Circuit: DCDC Configuration, PAVDD and RFVDD from DCDC output, AVDD and IOVDD from main supply

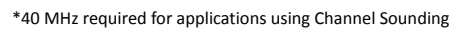


Figure 5.3. EFR32BG24L Typical Application Circuit: DCDC Configuration with PAVDD, RFVDD, AVDD, and IOVDD from DCDC output

5.2 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN0002.2: "EFR32 Wireless Gecko Series 2 Hardware Design Considerations" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 QFN40 / Standard Device Pinout

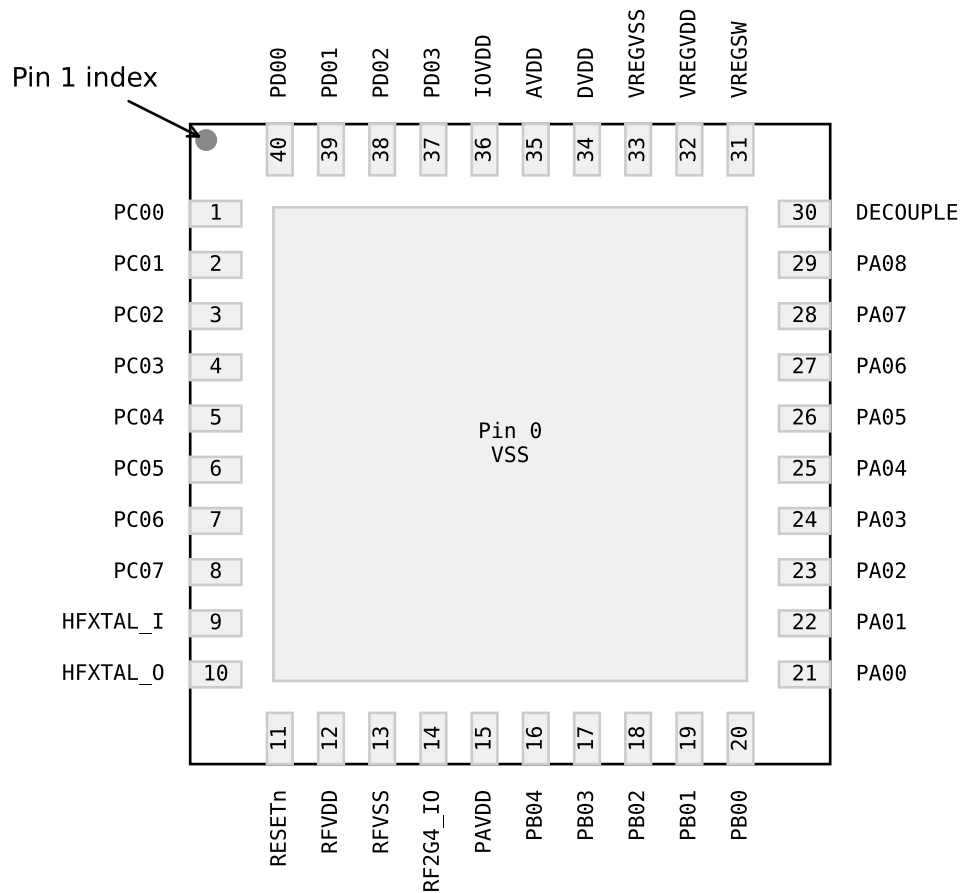


Figure 6.1. QFN40 / Standard Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [6.2 Alternate Function Table](#), [6.3 Analog Peripheral Connectivity](#), and [6.4 Digital Peripheral Connectivity](#).

Table 6.1. QFN40 / Standard Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
PC06	7	GPIO	PC07	8	GPIO
HFX TAL_I	9	High Frequency Crystal Input	HFX TAL_O	10	High Frequency Crystal Output

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	11	Reset Pin. The RESETn pin is internally pulled up to DVDD.	RFVDD	12	Radio power supply
RFVSS	13	Radio Ground	RF2G4_IO	14	2.4 GHz RF input/output
PAVDD	15	Power Amplifier (PA) power supply	PB04	16	GPIO
PB03	17	GPIO	PB02	18	GPIO
PB01	19	GPIO	PB00	20	GPIO
PA00	21	GPIO	PA01	22	GPIO
PA02	23	GPIO	PA03	24	GPIO
PA04	25	GPIO	PA05	26	GPIO
PA06	27	GPIO	PA07	28	GPIO
PA08	29	GPIO	DECOUPLE	30	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
VREGSW	31	DCDC regulator switching node	VREGVDD	32	DCDC regulator input supply
VREGVSS	33	DCDC ground	DVDD	34	Digital power supply
AVDD	35	Analog power supply	IOVDD	36	I/O power supply
PD03	37	GPIO	PD02	38	GPIO
PD01	39	GPIO	PD00	40	GPIO

6.2 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows GPIO pins with support for dedicated functions.

Table 6.2. GPIO Alternate Function Table

GPIO	Alternate Functions
PA00	IADC0.VREFP
PA01	GPIO.SWCLK
PA02	GPIO.SWDIO
PA03	GPIO.SWV
	GPIO.TDO
	GPIO.TRACEDATA0
PA04	GPIO.TDI
	GPIO.TRACECLK
PA05	GPIO.TRACEDATA1
	GPIO.EM4WU0
PA06	GPIO.TRACEDATA2
PA07	GPIO.TRACEDATA3
PB00	VDAC0.CH0_MAIN_OUT
PB01	GPIO.EM4WU3
	VDAC0.CH1_MAIN_OUT
PB02	VDAC1.CH0_MAIN_OUT
PB03	GPIO.EM4WU4
	VDAC1.CH1_MAIN_OUT
PC00	GPIO.EM4WU6
PC01	GPIO.EFP_TX_SDA
PC02	GPIO.EFP_TX_SCL
PC05	GPIO.EFP_INT
	GPIO.EM4WU7
PC07	GPIO.EM4WU8
	GPIO.THMSW_EN
	GPIO.THMSW_HALFSWITCH
PD00	LFXO.LFXTAL_O
PD01	LFXO.LFXTAL_I
	LFXO.LF_EXTCLK
PD02	GPIO.EM4WU9

6.3 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIOs. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used, positive inputs are restricted to the EVEN pins and negative inputs are restricted to the ODD pins. When a single-ended connection is being used, positive input is available on all pins. See the device reference manual for more details on the ABUS and analog peripherals. Note that some functions may not be available on all device variants.

Table 6.3. ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
ACMP0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACMP1	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IADC0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VDAC0	CH0_ABUS_OUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	CH1_ABUS_OUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VDAC1	CH0_ABUS_OUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	CH1_ABUS_OUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.4 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIOs. The table below indicates which peripherals are available on each GPIO port. Note that some functions may not be available on all device variants.

Table 6.4. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
ACMP0.DIGOUT	Available	Available	Available	Available
ACMP1.DIGOUT	Available	Available	Available	Available
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUSART0.CS	Available	Available		
EUSART0.CTS	Available	Available		
EUSART0.RTS	Available	Available		
EUSART0.RX	Available	Available		
EUSART0.SCLK	Available	Available		
EUSART0.TX	Available	Available		
EUSART1.CS	Available	Available	Available	Available
EUSART1.CTS	Available	Available	Available	Available
EUSART1.RTS	Available	Available	Available	Available
EUSART1.RX	Available	Available	Available	Available
EUSART1.SCLK	Available	Available	Available	Available
EUSART1.TX	Available	Available	Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
HFXO0.BUFOUT_REQ_IN_ASYNC	Available	Available		
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available
KEYSCAN.COL_OUT_0	Available	Available	Available	Available
KEYSCAN.COL_OUT_1	Available	Available	Available	Available
KEYSCAN.COL_OUT_2	Available	Available	Available	Available
KEYSCAN.COL_OUT_3	Available	Available	Available	Available
KEYSCAN.COL_OUT_4	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
KEYSCAN.COL_OUT_5	Available	Available	Available	Available
KEYSCAN.COL_OUT_6	Available	Available	Available	Available
KEYSCAN.COL_OUT_7	Available	Available	Available	Available
KEYSCAN.ROW_SENSE_0	Available	Available		
KEYSCAN.ROW_SENSE_1	Available	Available		
KEYSCAN.ROW_SENSE_2	Available	Available		
KEYSCAN.ROW_SENSE_3	Available	Available		
KEYSCAN.ROW_SENSE_4	Available	Available		
KEYSCAN.ROW_SENSE_5	Available	Available		
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PCNT0.S0IN	Available	Available		
PCNT0.S1IN	Available	Available		
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.ASYNCH12	Available	Available		
PRS.ASYNCH13	Available	Available		
PRS.ASYNCH14	Available	Available		
PRS.ASYNCH15	Available	Available		
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
RAC.LNAEN	Available	Available	Available	Available
RAC.PAEN	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available

7. QFN40 Package Specifications

7.1 QFN40 Package Dimensions

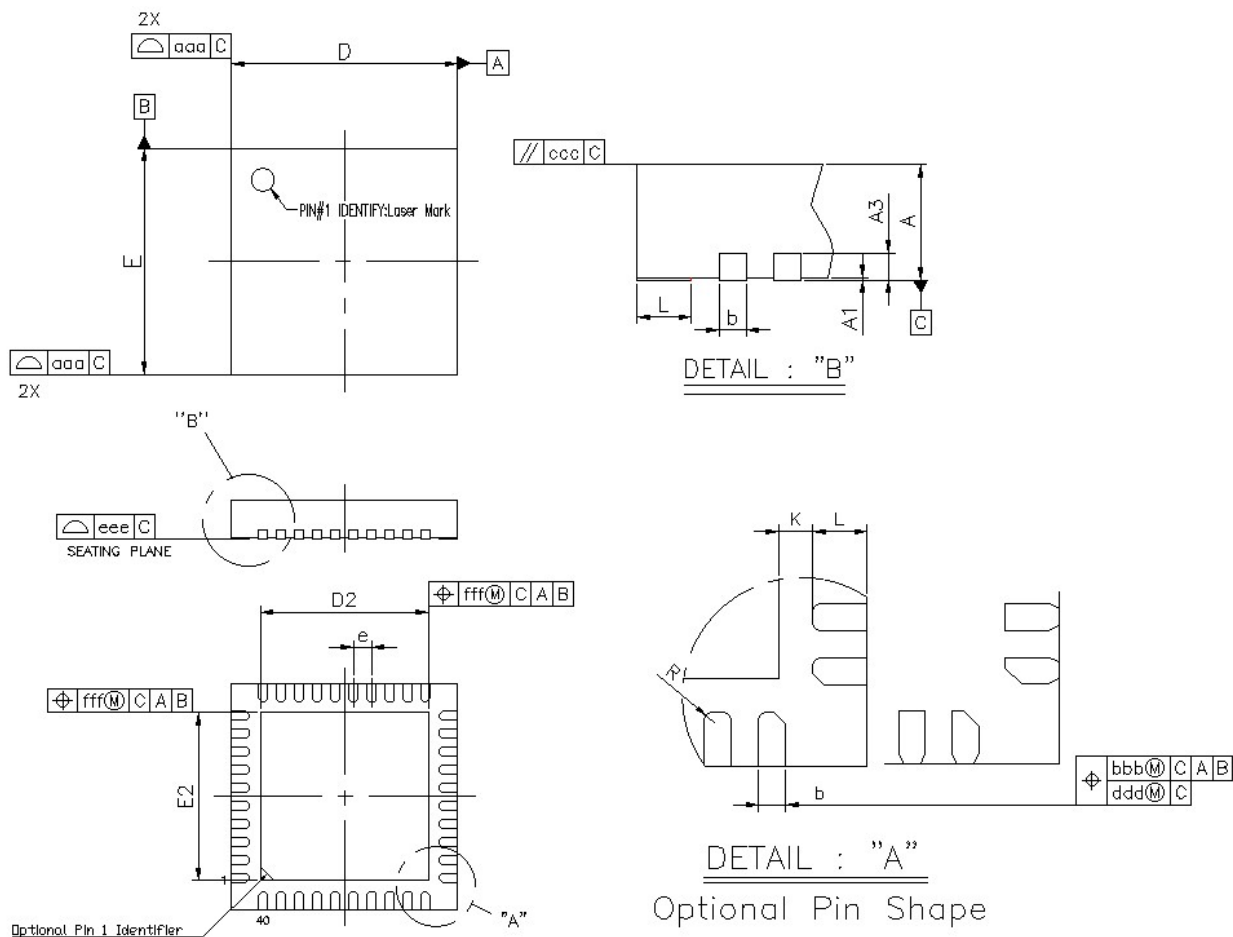


Figure 7.1. QFN40 Package Drawing

Table 7.1. QFN40 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.55	3.70	3.85
E2	3.55	3.70	3.85
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
R	0.075	—	—
aaa	0.10		
bbb	0.07		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. Package external pad (epad) may have pin one chamfer.

7.2 QFN40 PCB Land Pattern

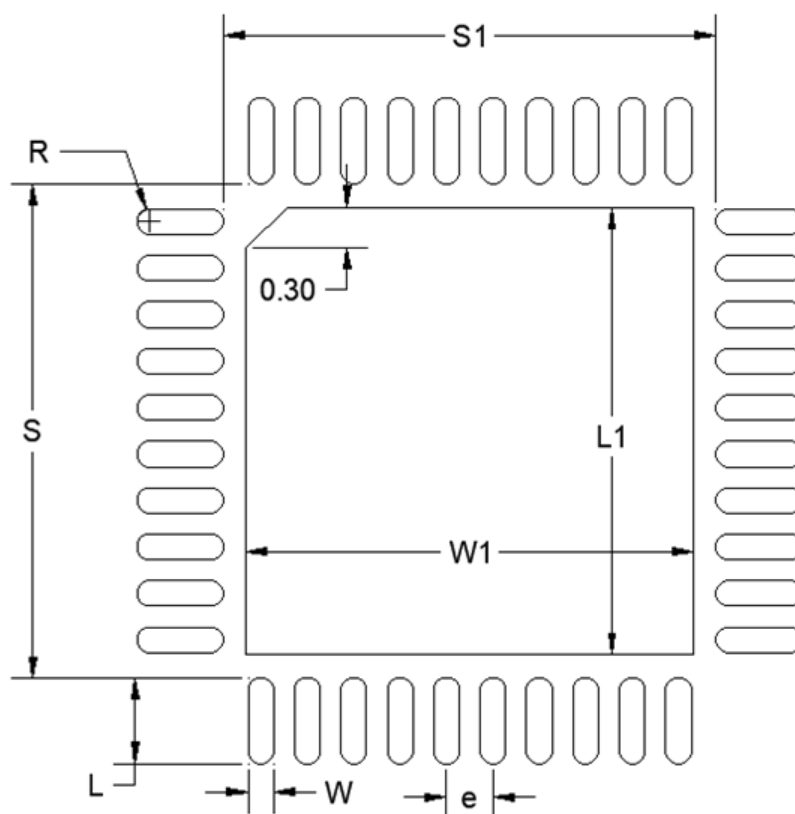


Figure 7.2. QFN40 PCB Land Pattern Drawing

Table 7.2. QFN40 PCB Land Pattern Dimensions

Dimension	Typ
S1	4.25
S	4.25
L1	3.85
W1	3.85
e	0.40
W	0.22
L	0.74
R	0.11

Dimension	Typ
Note: <ol style="list-style-type: none"> 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. This Land Pattern Design is based on the IPC-7351 guidelines. 3. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 4. The stencil thickness should be 0.101 mm (4 mils). 5. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads. 6. A 3x3 array of 0.90 mm square openings on a 1.20 mm pitch can be used for the center ground pad. 7. A No-Clean, Type-3 solder paste is recommended. 8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. 9. Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling. 	

7.3 QFN40 Package Marking

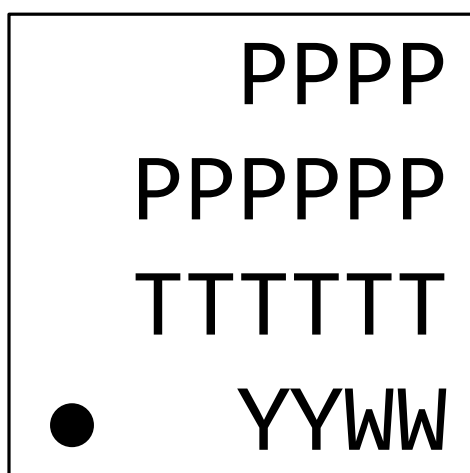


Figure 7.3. QFN40 Package Marking

The package marking consists of:

- Line 1: P P P P – The product family codes (BG24)
- Line 2: P P P P P – The product option codes:
 - 1) Security (L = Secure Vault Mid)
 - 2-4) Product Feature Codes
 - 5) Flash (S = 768k)
 - 6) Temperature grade (I = -40 to 125 °C)
- T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.

8. Revision History

Revision 1.0

April, 2025

- Initial Release

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