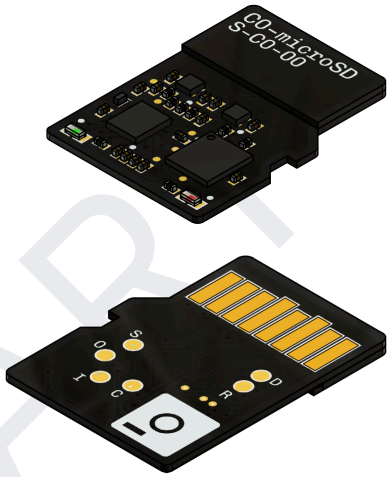
Signaloid C0-microSD Datasheet

Description



The Signaloid C0-microSD is a low-power system-on-module (SoM) that features a Lattice iCE40 FPGA and 128 Mbit of SPI flash memory. It is a hot-swappable module designed to fit and function in a microSD slot as a regular SD block storage device. The C0-microSD's FPGA is connected to both the microSD interface pins as well as to six additional test pads which are used during production for the initial programming of the device. The C0-microSD is shipped pre-configured with two configuration bitstreams: (1) the Signaloid SoC—an FPGA-based RISC-V system-on-chip (SoC) implementing a subset of Signaloid's technology for deterministic arithmetic on probability distributions; (2) a bootloader that allows the standard microSD interface, operating as an SD block device, to load new FPGA bitstreams or programs for the Signaloid SoC, removing the need for any external programmers. Together, these capabilities enable developers to configure the C0-microSD as either a generic FPGA SoM or as an SD-compatible, RISC-V-based accelerator for deterministic arithmetic on probability distributions, accessible from a host computer or embedded system via the 4-wire SD protocol or the SD-over-SPI protocol.

Features

- Lattice ICE40UP5K FPGA
  - 5280 logic cells
  - 120 Kbit dual-port block RAM
  - 1 Mbit (128 KiB) single-port RAM
- Renesas AT25QL128A SPI Flash
  - 128 Mbit (16 MiB) non-volatile memory
- Programmable I/O pins:
  - Two on-board LEDs (one red and one green).
  - Six programmable I/O pins (from the microSD interface)
  - Five additional programmable pins on test pads
- Built-in Signaloid C0 RISC-V processor SoC
- Built-in bootloader, allowing you to load new FPGA bitstreams or RISC-V applications via the SD interface

Table of Contents

1. Functional Block Diagram

The Signaloid C0-microSD is based on the iCE40 FPGA from Lattice Semiconductor. In addition to the iCE40 FPGA, the Signaloid C0-microSD SOM contains 128 Mbit of serial NOR flash for storing bitstreams, firmware, and user data. The device also features two on-board LEDs, one red and one green, connected to the FPGA.

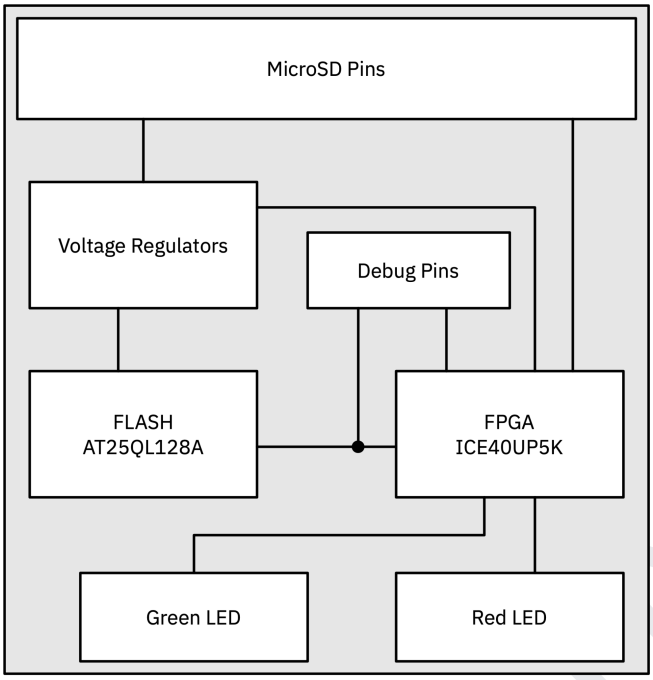


Figure 1. C0-microSD functional diagram.

2. Pinout Diagram

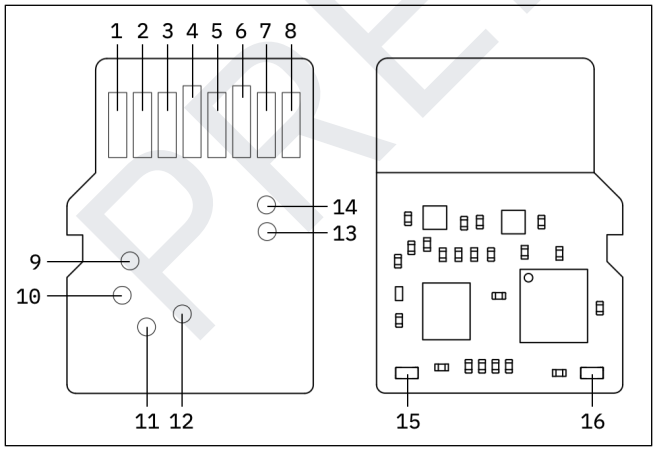


Figure 2. C0-microSD pinout diagram.

The C0-microSD provides six configurable I/O pins by repurposing the microSD pads and five additional I/O pins in the form of test pads.

3. Package Diagram

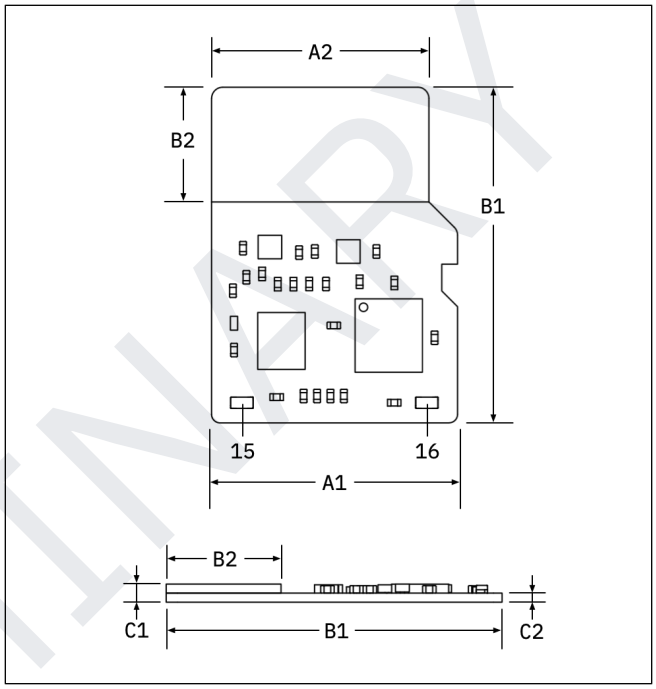


Figure 3. C0-microSD package diagram.

Dimension	Typical	Tolerance	Unit
A1	11	± 0.2	mm
A2	9.7	± 0.2	mm
B1	15	± 0.2	mm
B2	9.9	± 0.2	mm
C1	0.8	± 0.2	mm
C2	0.4	± 0.1	mm

Table 1. C0-microSD dimensions.

4. Modes of Operation

The C0-microSD has three distinct modes of operation (also referred to as active configurations):

- **Bootloader** mode: In this mode, you can flash new custom bitstreams, update the firmware of the C0-microSD, and flash new user data to the non-volatile memory.
- **Signaloid SoC** mode: In this mode, the Signaloid C0 Core is loaded into the device.

- **Custom User Bitstream** mode: In this mode, the latest custom user bitstream is loaded into the device.

5. Pinout Description

Number	Pin Name	FPGA Pin	Standard	Description
1	SD_DAT2	E5	LVCMOS 3.3	GPIO pin connected to the SD bus DAT2
2	SD_DAT3	F5	LVCMOS 3.3	GPIO pin connected to the SD bus DAT3
3	SD_CMD	A4	LVCMOS 3.3	GPIO pin connected to the SD bus CMD
4	VDD	–	–	Supply voltage
5	SD_CLK	B3	LVCMOS 3.3	GPIO pin connected to the SD bus CLK
6	VSS	–	–	Ground voltage
7	SD_DAT0	A1	LVCMOS 3.3	GPIO pin connected to the SD bus DAT0
8	SD_DAT1	A2	LVCMOS 3.3	GPIO pin connected to the SD bus DAT1
9	CONFIG_SCLK	D1	LVCMOS 1.8	Clock pin of SPI configuration port
10	CONFIG_MISO	E1	LVCMOS 1.8	MISO pin of SPI configuration port
11	CONFIG_MOSI	F1	LVCMOS 1.8	MOSI pin of SPI configuration port
12	CONFIG_CSn	C1	LVCMOS 1.8	Chip select of SPI configuration port (active low)
13	COFIG_CRESETn	F3	LVCMOS 1.8	FPGA reset pin (active low)
14	CONFIG_DONE	D3	LVCMOS 1.8	Configuration Done pin
15	GREEN_LED	A5	LVCMOS 3.3 Open Drain	Green status LED
16	RED_LED	B5	LVCMOS 3.3 Open Drain	Red status LED

Table 2. C0-microSD pinout

6. Electrical Specifications

6.1 Nominal Supply Voltage

Supply	Min	Typ	Max	Unit
VDD	3.14	3.3	3.5	V

Table 3. C0-microSD nominal supply voltage.

6.2 I/O Recommended Operating Conditions

Standard	Min	Typ	Max	Unit
LVCMOS 3.3	3.14	3.3	3.46	V
LVCMOS 1.8	1.71	1.8	1.89	V

Table 4. Recommended operating conditions of I/O pins

6.3 Power Consumption

This section presents power consumption measurements of two typical applications of the C0-microSD. All current measurements are taken for a supply voltage of 3.3 V.

6.3.1 Signaloid SoC

In Table 5, we present the power consumption measurements from running the Calculator Demo[1] application on the built-in Signaloid SoC, adding two uniformly distributed double precision floating point numbers: 3.0 ± 0.6 and 5.0 ± 0.6.

Min	Average	Max	Unit
4.96	5.18	7.43	mA

Table 5. Typical power consumption of C0-microSD in Signaloid SoC mode

6.3.2 Blink example circuit

In Table 6, we present the power consumption measurements extracted from configuring the FPGA with a simple blink example[2] in **Custom User Bitstream mode**.

Min	Average	Max	Unit
1.09	1.13	1.17	mA

Table 6. Typical power consumption of blink circuitry on C0-microSD

[1] https://github.com/signaloid/Signaloid-C0-microSD-Demo-Calculator

[2] https://github.com/signaloid/C0-microSD-Hardware/tree/main/rtl-examples/blink

7. Maximum Ratings

7.1 sysI/O Maximum Ratings

Standard	Max	Unit
LVCMOS 3.3	8	mA
LVCMOS 1.8	4	mA

Table 7. I/O pin maximum source current.

7.2 Operating Temperature

Parameter	Min	Max	Unit
Operating temperature	-40	85	°C

Table 8. Operating temperature range.

8. Revision History

Revision 1.0, February 2025

Section	Change Summary
All	Initial release