TFE4152 – Design of integrated circuits 2018

Project description

Digital camera

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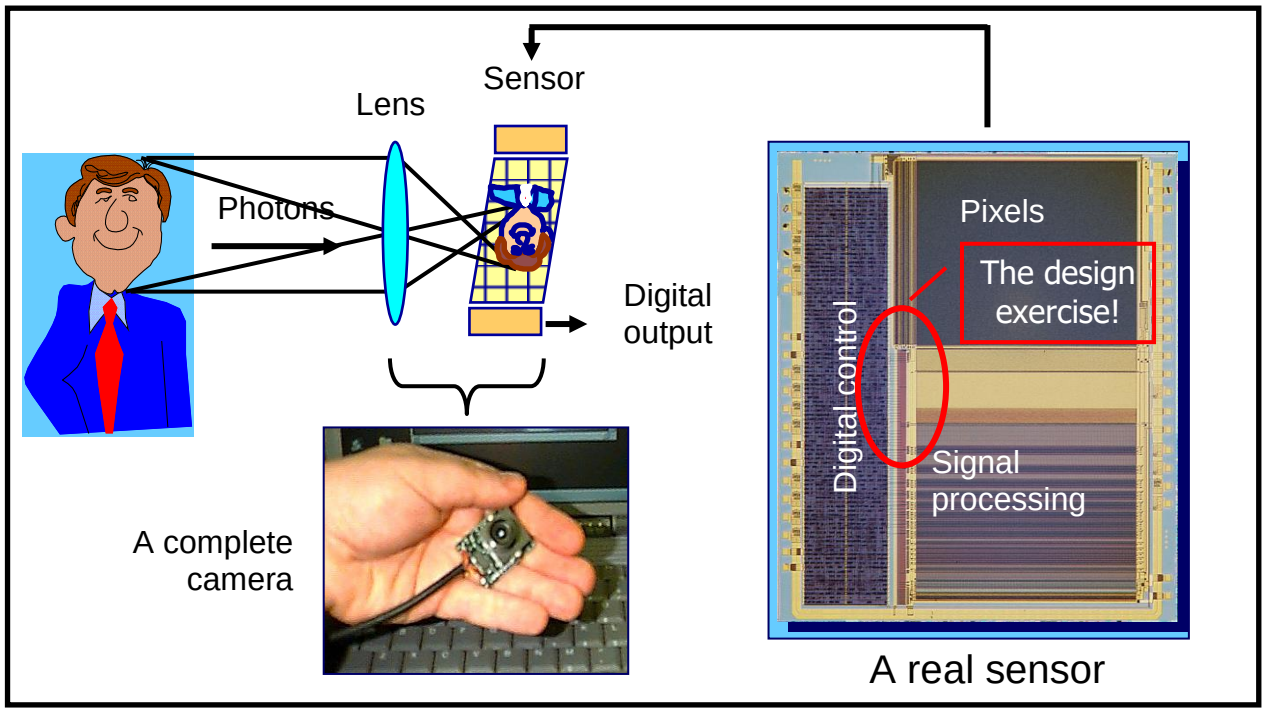
Associate Professor



Read all the words in the assignment before you start your work. Do not assume that you know the rest of the paragraph from the start.

Deadline: Wednesday 21.11.2018 @ 15:00.

Goals and motivation

The assignment is intended to give you experience in the design of analog and digital circuits, and give an insight into some methods used in the industry.

You will use the CAD tools AIM-Spice and Active-HDL, where AIM-Spice is an analog simulator and Active-HDL is a digital HDL simulator. You shall also create test benches and experience how to scale systems. These tools are available on the computers in all student computer rooms. You may also download student versions of the software to your own computer.

Report

After finishing the analog simulations, you may submit a preliminary report as a pdf file. At the end of the digital design and simulations, the complete report shall be submitted electronically as a pdf document. This report shall contain the standard parts of a technical report. An example of a report structure is outlined at the end of this document.

The report deadline is ***Wednesday 21.11.2018 @ 15:00*** and it ***must be uploaded to Blackboard***. An example of a report structure is outlined at the end of this document.

Assistance

There will be assistance available during the exercise hours on Tuesdays from 14:15 to 16:00.

Digital camera

Motivation: Digital applications are becoming more and more common in our daily lives, in many cases replacing analog applications. However, since the world we live in is an analog world, digitalization cannot completely remove the need for analog applications. What we see today is that we are converging toward a mixture of analog and digital systems, and we will take a closer look at digital cameras. Even though it is called a digital camera it contains both analog and digital parts.

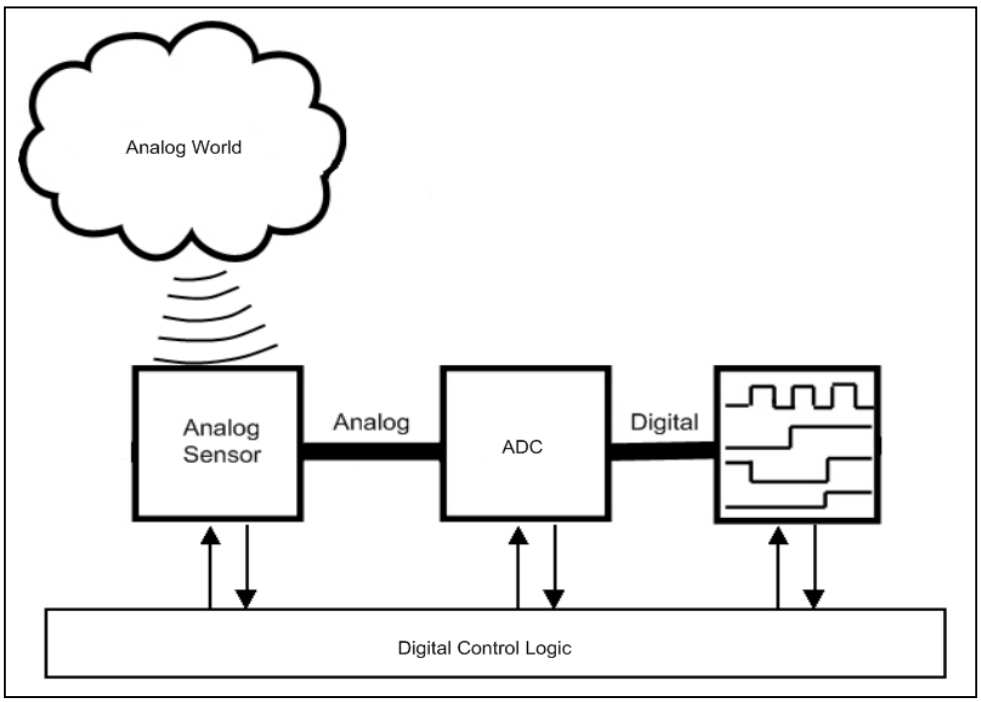


Figure 1 A very simplified view of a digital camera

Figure 1 shows a very simplified view of a digital camera. The light from the analog world is one of the input signals to the camera. This is an analog signal that varies with time and is converted to a digital signal through the use of an Analog to Digital Converter (ADC or A/D). This is done when a trigger signal starts the process of capturing a picture. The converted data is processed to a data format that the digital unit (in this case the camera) can store and comprehend. This is done by a Digital Signal Processor (DSP).

Description of the assignment: Your goal is to design the readout and control circuit for a four pixel digital camera. You need an analog part and a digital control block. These are the blocks *Pixel_electronics* and *RE_Control* in Figure 2. They will be described further.

Figure 2 shows a block diagram of the digital camera you shall design. When the photographer wants to take a picture he will push the button ***Take_a_picture***. The signal from the button is sent to a pulse-shaping module that will generate a pulse that is one clock cycle long. This is not a part of your assignment. If he wants to adjust the exposure time, he can use the buttons ***Increase_time*** or ***Decrease_time***.

Figure 3 shows the analog circuit for one pixel where the input photo detector is represented as a current generator and a pn-diode. The photodiode generates a current that depends on the

light conditions. Bright light will result in a stronger current than if dim light hits the photodiode. This current is visible as a charge in the capacitance, C_S, which depends on the current and the exposure time. Long exposure time combined with a small current can result in the same charge as a short exposure time combined with a strong current. If the pixel is exposed for too long in bright light the charge will become too large. This will result in an excessive voltage over the capacitor, which in turn will give rise to an overexposed picture. The pixel circuit can be expressed as a symbol, as shown in Figure 4.

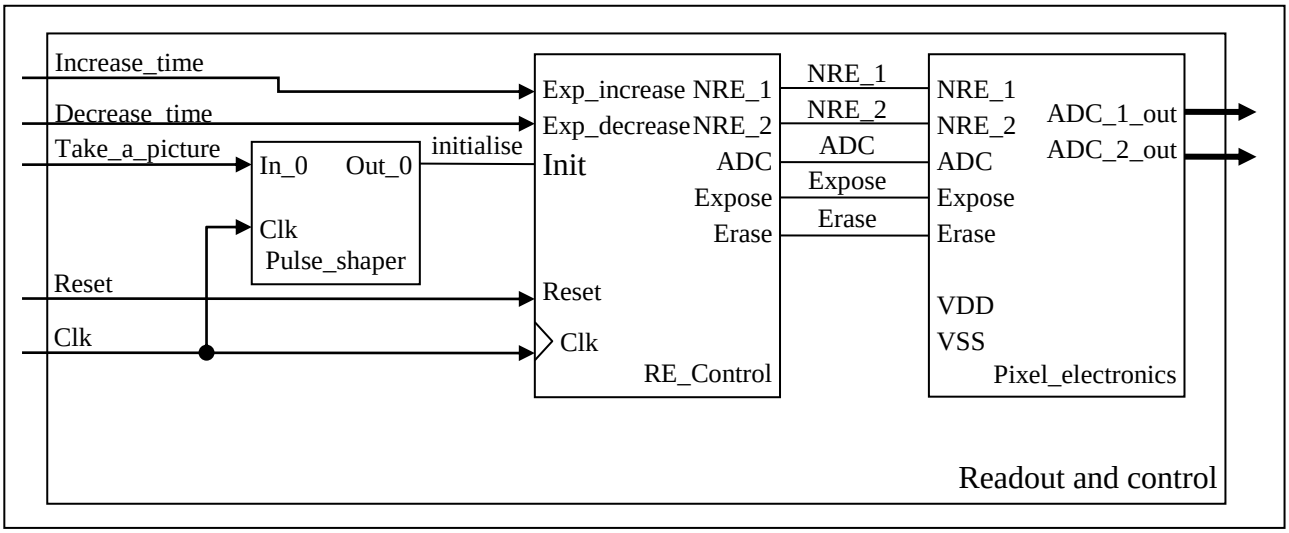


Figure 2 Block diagram for the readout and control circuit.

The transistor controlled by the signal ***Expose*** controls the charging of the capacitor C_S. The longer the transistor is open, the more current can flow into the capacitor. The transistor is open during the exposure time. In poor light conditions, it should be open for a longer time than in good light conditions.

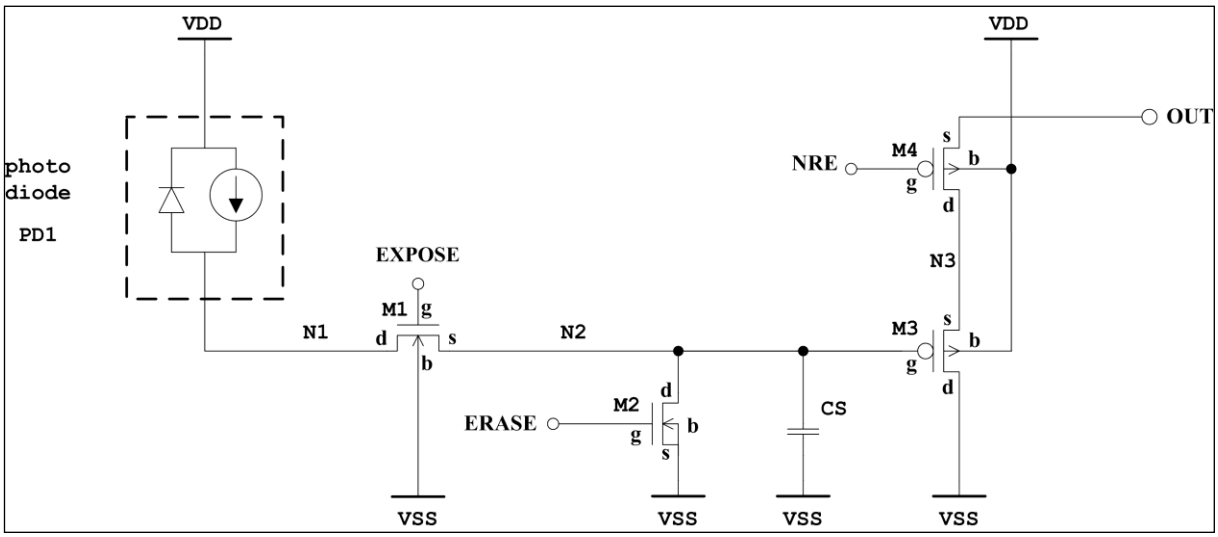


Figure 3 Pixel circuit diagram

The transistor controlled by the signal ***Erase*** can remove the charge (if any) stored in the capacitor. This must be done before every exposure, to be sure that the following exposure is correct. The ***Erase*** signal should never be active at the same time as ***Expose*** during the exposure time. Otherwise this would just send the current from the photo sensor to ground, and the capacitor would not be charged. However, this is not destructive and the circuit will survive. It just means that ***Erase*** has priority over ***Expose***.

The ***NRE***-signal (***N_REad***) is used to activate the readout of the charge that is stored on C_s. This is shown in Figure 5. The pixels in a column share an ADC and the connection of the pixels to the ADC is time multiplexed. To avoid that more than one pixel is connected simultaneously, the ***NRE***-signals must be timed correctly.

The four pixel readout circuitry to be designed is represented as a 2x2 pixel array as shown in Figure 5.

The pixel outputs in a column share the connection to one ADC. The switch transistor on the pixel output must be controlled by ***NRE*** such that only one pixel output is connected to the column line at a time. Between the readouts no pixel output must be connected.

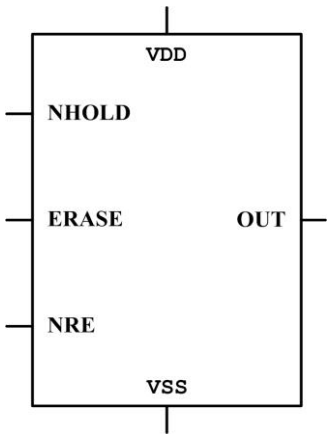


Figure 4 Pixel circuit symbol

As part of the assignment, you must determine suitable geometries for the transistors used in the pixel circuit. You must also design the digital control block for controlling the exposure and readout of new image data and erasing of old image data.

Circuit description

The photographer has chosen the exposure time, manually or automatically, depending on the surrounding lighting before the trigger is pressed. The trigger activates the exposure of the pixel for the preset time. After the exposure is completed, the camera must activate the readout. When the camera has completed the readout it returns to the initial state and prepares for a new picture.

From Figure 3, C_S is the sampling capacitor and it must be discharged before the exposure starts (using the signal ***Erase)***. When the exposure is activated, the photodiode is connected to the sampling capacitance (using the signal ***Expose)***. To control the exposure time a counter

counts a given number of cycles. When the counter is finished, the sampling capacitance is disconnected from the photodiode and the readout is activated.

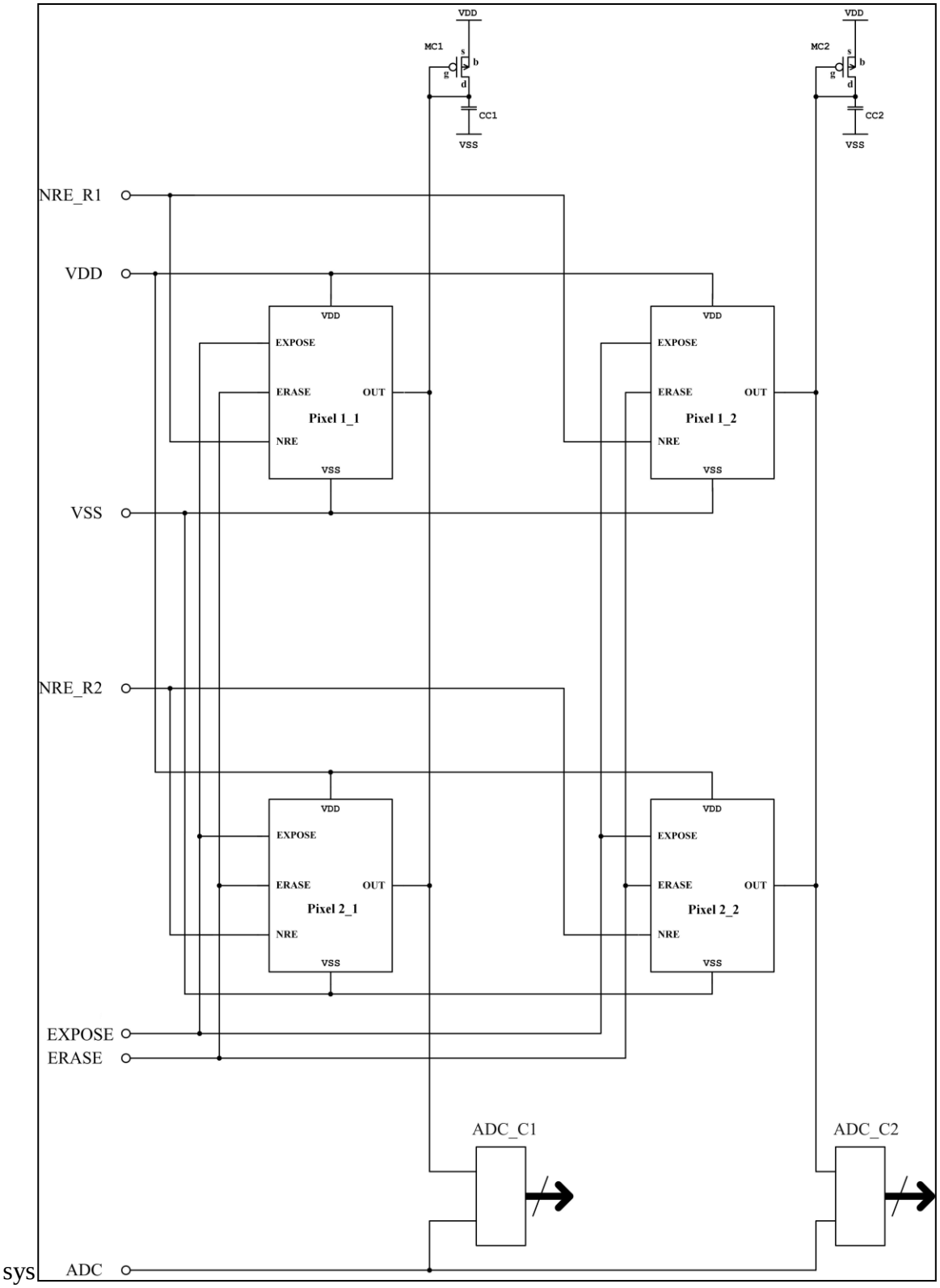


Figure 5 A 2x2 pixel array where each column has its own A/D and active load transistor. The capacitance CC1 and CC2 represents parasitic capacitance.

Turning our attention to Figure 5 for the readout, we see that two and two pixels are connected to the same A/D. For a successful reading only one pixel may use the wire at one time. In other words, at any time only one pixel may have its **NRE** signal set low. When one pixel from each column is selected and its **NRE**-signal set low, ***ADC*** is set high and two pixel values are converted in parallel. After the signal has been digitized, ***ADC*** is set low and the output of the next pixels from each column is connected to the A/D, and the process is repeated. After the readout is completed the camera waits for a new picture to be initiated.

Each column consists of a common active load and A/D, where the buffer transistor M_3 of Figure 3 uses the column transistor M_C of Figure 5 as active load. Remember that only one pixel output of each column is allowed to be connected to the A/D at any time. Also keep in mind that the pixels of the same row use the same control signals.

We will not be concerned with the digital representation of the pixels at the output of the A/D converters, but rather put our focus on everything that happens before the conversion. Your main task now will be to design the digital control circuit and design a circuit that do the exposure and readout.

How to solve the problem?

As you start working for a company you will see that tasks are not given to you as a set of concrete problem specifications, rather you will see a diffuse representation of a problem and it is your job to make the solution a detailed presentation of the problem.

When you see the representation of the pixel circuit given in Figure 3 and Figure 5 you should make sure you understand how it works and how the photocurrent is converted to a voltage. You should also try to figure out which transistors are used as switches, amplifiers and active loads.

The exposure and readout can be controlled using a state machine, and a programmable counter can control the exposure time. Most of the required signals to the analog circuitry are given in Figure 6 and a state machine for the digital part is given in Figure 7. Figure 6 is not complete. Figure 7 may be complete, but if you prefer to change the number of states, you are free to do so.

Figure 6 shows the time chart and as can be seen we require 12 time slots to complete a cycle for each photo. One possible block diagram solution to the digital part is shown in Figure 8. The input signals of this circuit are ***Init***, ***Exp_inc***, ***Exp_dec***, ***Reset***, and ***Clk***. ***Init***, ***Reset*** and ***Clk*** are input to the finite state machine that controls the readout, while ***Exp_inc***, ***Exp_dec***, ***Reset*** and ***Clk*** are inputs to the unit that controls the exposure time. ***Clk*** is the system clock signal. ***Init*** is a one cycle signal from the camera trigger. When the photographer wants to take a photo the trigger is activated and the pulse shaper inside the camera generates the single cycle pulse ***Init***. When ***Init*** is high a sequence of exposure and readout is started. Another team will design the pulse shaper.

If the photographer wants to change the exposure time he may use the signals ***Exp_inc*** and ***Exp_dec***. When ***Exp_inc*** is ‘1’ the exposure time shall increase by 1 ms for each clock period until it reaches the maximum value of 30 ms. When ***Exp_dec*** is ‘1’ the exposure time shall decrease by 1 ms for each clock period until it reaches the minimum value of 2 ms. If ***Exp_inc*** and ***Exp_dec*** are ‘1’ at the same time ***Exp_inc*** shall have priority and the exposure

time shall be increased. A state machine or a counter may control the exposure time. The selected exposure time shall be stored in a register. The exposure time may only be changed when the FSM of Figure 6 is in the state “Idle”.

The remaining signals in Figure 6 are the output signals from the RE_control that you are going to design.

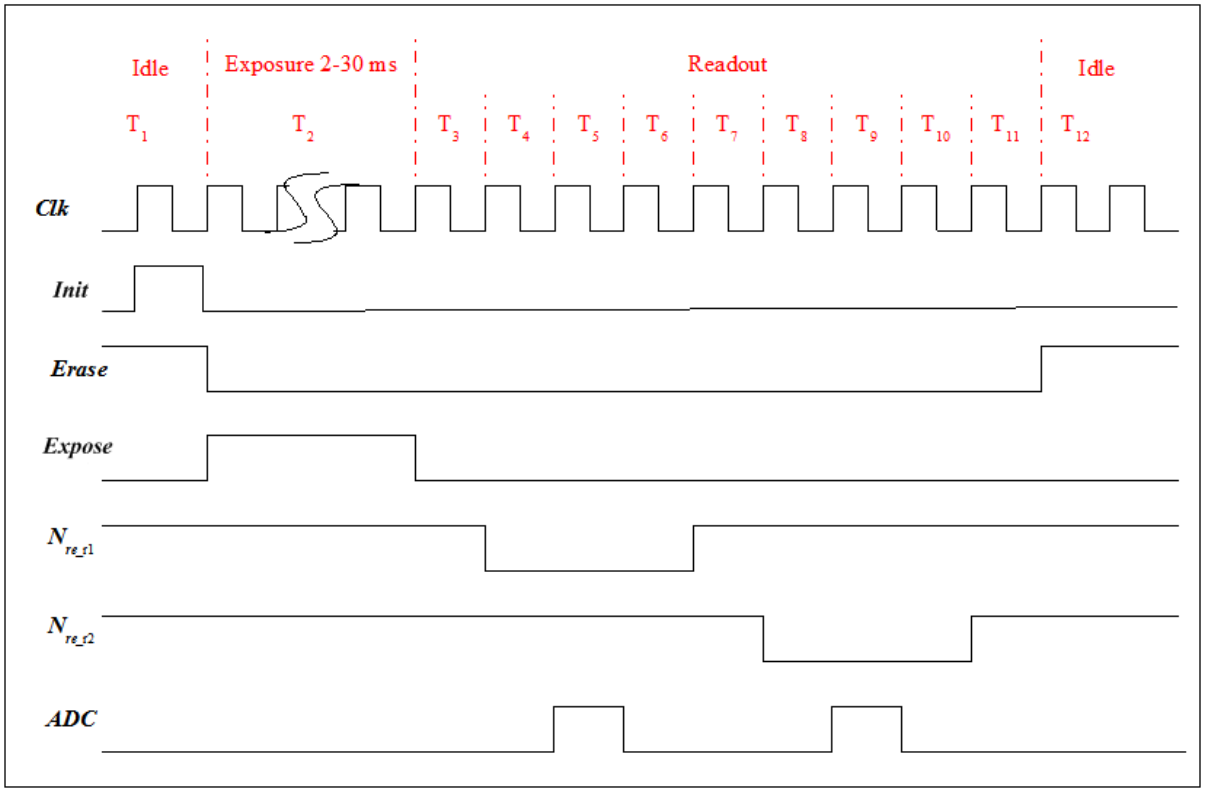


Figure 6 One possible time chart for the digital camera

While the camera waits for a photo to be initiated, ***Erase*** is set high to make sure that there is no charge on the sampling capacitor shown in Figure 3. Since ***Erase*** is high during “Idle”, the value of ***Expose*** is unimportant since C_S is connected to ground. It can either be high or low, but it should be low to avoid any problems. The next time slot is the exposure that can vary between 2 and 30 ms depending on the light conditions and the photographer’s preferences. After the picture is captured the readout starts with all the pixels of row 1 in parallel. The pixels are read one row at the time. When the camera is finished with the readout, it prepares for a new picture by setting ***Erase*** high again.

It is important for you to understand the sequence they need to be executed and that you understand how the state machine works. Use Figure 3 along with Figure 6 and the description of how the circuit functions, given above, to ensure yourself that you understand how the circuit works.

The state diagram of Figure 7 shows one possible state chart for the finite state machine, FSM. While the camera is in the state “Idle”, it will stay there until a photo is initiated. The transition from “Idle” to “Exposure” is activated by the user taking a photo. The camera will remain in “Exposure” until this exposure time is completed. This may be controlled by a counter which overflows when it has counted a number of clock periods corresponding to the

preset exposure time, and sets ***ovf5*** high. When this happens the FSM enters "Readout" and the readout starts.

"Readout" may be controlled by another FSM, a shift register or a counter or you may include all the states of "Readout" in this FSM. If it is controlled by another counter that counter must count until the "Readout" is completed and set the overflow flag ***ovf4*** high. It is better to use only one counter that counts from different starting positions. In that case ***ovf4*** and ***ovf5*** may be the same signal, ***ovf***. The counters may be binary or Gray-code counters. If you would rather use a shift register for counting that is also possible.

You must include the signal ***ovf*** (or ***ovf*** 4 and ***ovf5***) in Figure 6 and let this new time chart be a part of your report. Any other control signals you introduce must also be included.

The signal ***Reset*** will bring the FSM to "Idle" at the next positive clock edge, no matter what state it is in. If it enters a forbidden state, it must be brought to "Idle" on the next clock edge. The signal names on the transitions are the transition conditions.

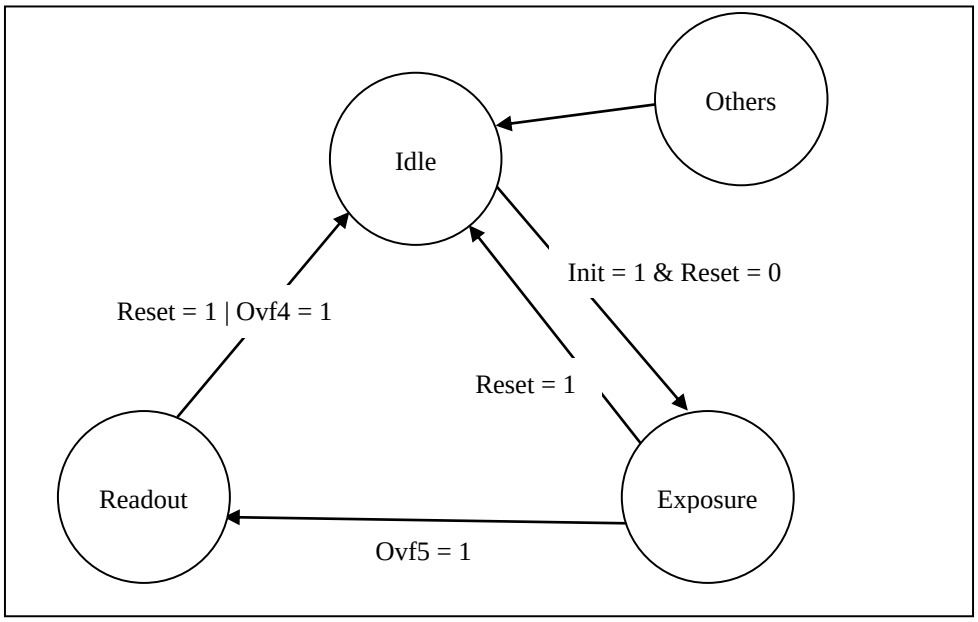


Figure 7 One possible state machine for the photo process

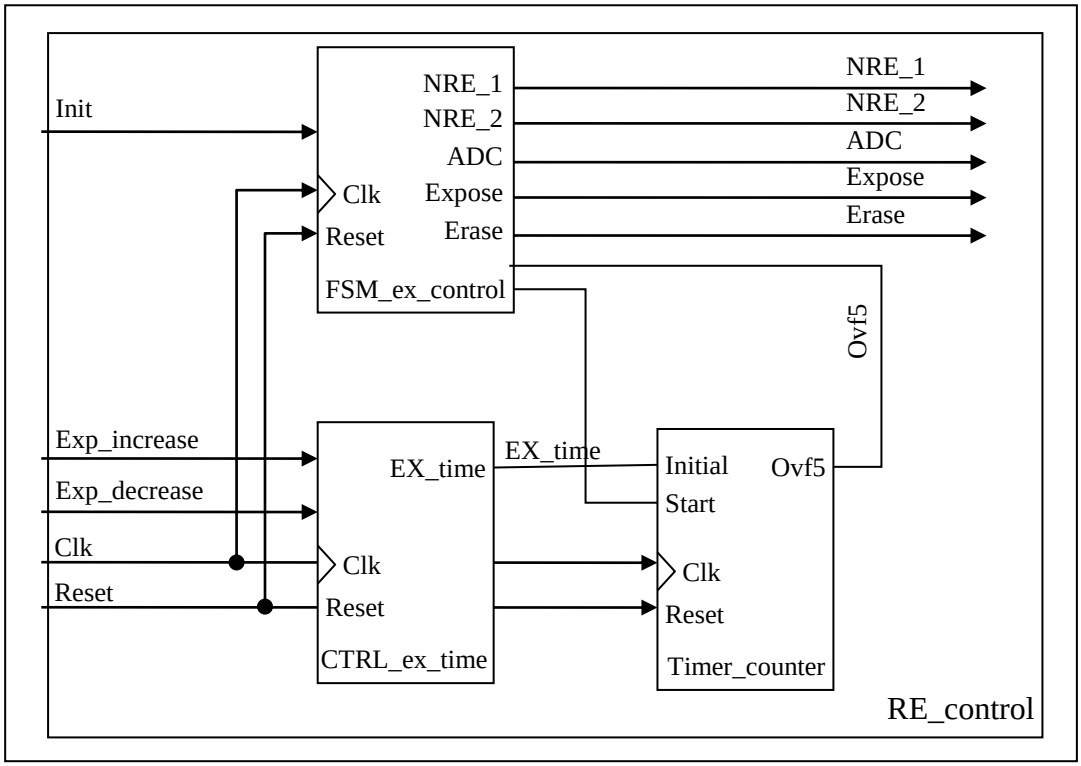


Figure 8 One possible block diagram for RE_control.

Design and simulation

When you are finished with the design phase it is very important that you simulate your design to verify its behaviour. After you have finished simulating the analog part, you need to define the state machine in Verilog and simulate the control signals. You must verify that the design works correctly for different Exposure times, also the minimum and maximum. This must be included in the report.

Specifications

These are the specifications for the project.

- For all transistors, 0.7 µm < L < 2 µm and 2 µm < W <10 µm
- For all sampling capacitances, $C_{S \leq}$ 3 pF
- Column capacitances, $C_{C1} = C_{C2} = 3$ pF
- Supply voltage, $V_{DD} = 1.8$ V
- Exposure time can vary between 2-30 ms
- The clock frequency is 1 kHz
- The photodiode current is around 50 pA in poor lighting, and around 750 pA with good light conditions
- Implement your circuit with 180 nm transistor technology

Some issues on debugging

As you might know, you may apply different kind of stimuli to a circuit to test factors like its frequency response or power gain. A test bench consists of the information needed to extract the simulation results you are interested in.

When you have a large circuit it is not very convenient to change every transistor width or length manually. Therefore it may be wise to use a common parameter for the transistors of equal size so you can easily change the parameter using the command *.param*.

These commands are valid for Spice, but no matter what program you are using, it is usually easier to determine errors if you divide your circuit up into smaller parts instead of collecting the whole circuit into one file.

With Verilog you may also write a test bench that verifies that your design is working. Let the test bench be a module of its own, and instantiate your camera circuit inside the module. The camera circuit shall have one single top module that contains a net list of the modules in your design.

Good luck

Typical design flow

This is a suggestion of the design flow:

1. While you are designing, document what you are doing.
2. Make sure you understand the time and state charts and the circuit functionality
3. Find suitable transistor geometries
4. Simulate with Spice
5. Complete the time- and state charts, if necessary
6. Write a net list in Verilog that satisfies your state diagram and simulate it.
7. Verify your results

Report Information

What needs to be included

The analog part of the report should include

- Description of the problem
- Description of your solution
- Theory
    - Every choice you make must be based on theory
    - Calculations of transistor sizes etc must be included
- Spice simulations
- Screen shots of relevant simulations
- Net lists

The digital part of the report should include

- Description of the problem
- Description of your solution
- Verilog code
- State diagrams
- Timing charts
- Screen shots of relevant simulations

All figures and tables must be numbered and commented in the report text.

Report Structure

This is an example of a report structure.

Your report has 3 parts:

- What are you going to do?
- What are you doing?
- What have you done?

These chapters are typical. Some may be embedded in neighbouring chapters or completely omitted. The pages must be numbered and the chapters should be numbered.

1) Title page: Including topic, date, group number and the name of each candidate.
2) Abstract: Providing the objective of the work and the outline of your report.
3) Contents: Listing individual sections in the report with page numbers.
4) Introduction: About the circuit, background etc.
5) Theoretical background.
6) Design: Assumptions made, design approach followed, state and time diagrams and schematics. The schematics from the assignment text should also be included as a part of your documentation.
7) Simulations: Plots of all parameters and discuss them individually. Verify that your design is correct.
8) Results and discussions: Are they what you expected and similar to your time chart? (This may be included in Chapter 6.)
9) Conclusions: What did you do and how? Does the design work according to the specifications? Why not? What did you learn, and did you achieve some thing out of it? This concludes from the previous in depth information. Do not introduce anything here that you have not written before.

- Appendix
    - Spice listing
    - Verilog listing

The “directors cut” of a report is Abstract, Introduction and Conclusion. It should be possible for the reader to know what you have done and why you did it as well as your results or recommendations by reading these chapters.