Project report intergrated circuits

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1 Introduction

"Hello Dirty talk"

2 Theory

2.1 Analog circuit

The analog circuit has input signals delivered by the digital circuitry, and delivers its output to two ADCs. The analog circuit diagram is given in figure 1, where each of the four pixel block has the circuit given in figure 2.

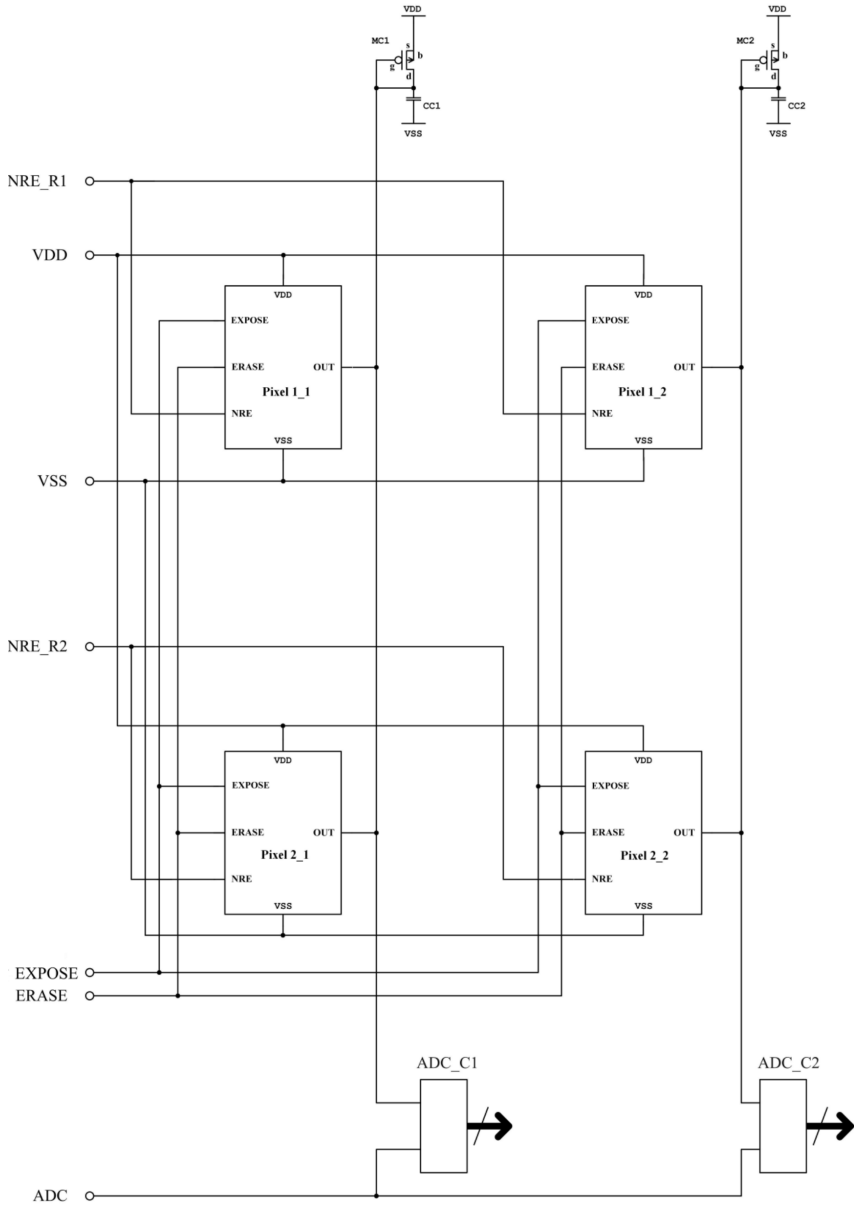


Figure 1: Analog circuit schematic.

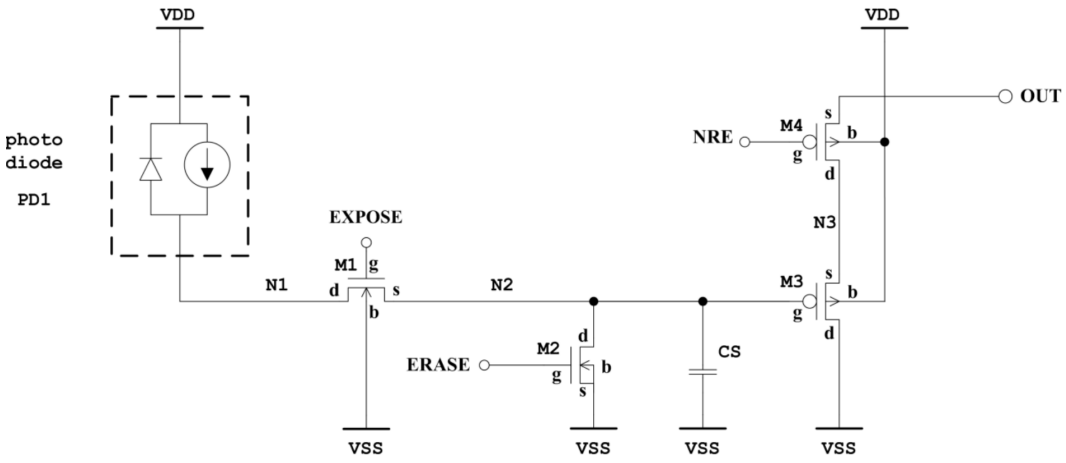


Figure 2: Pixel cicuit schematic.

In detail, the analog circuit consists of 4 pixels in a 2x2 array. Each pixel in the same row shares the same NRE (Not-REad) input which means they are sending data to the ADC at the same time. Each pixel in the same column share the same active load and readout wire, which means they need to send data to the ADC at different times.

2.1.1 Conceptual operation of pixel circuit

Schematics for the pixel circuit is given in figure 2. It consists of a photo diode PD1, three switch transistors M1, M2 and M4, one buffer transistor M3 and a charge storage capacitor C_S. The photo diode is modeled by a diode and an ideal current source in parallel. The current source outputs a current I_D that is proportional to the illumination intensity on that particular pixel. This current is used to charge the transistor C_S. Ideally, we want that all of I_D flows through M1 and into C_S when EXPOSE is high and all of I_D flows back through the diode in the photo diode model when EXPOSE is low. In that way the voltage on node N2 when EXPOSE has been high for a time t is given by

$$V_{CS}(t) = \frac{1}{C_S} \int_0^t I_D(t)dt. \tag{1}$$

This means the voltage V_{CS} is proportional to the total illumination on the pixel throughout the exposure time, which is exactly what we want.

But since the camera is supposed to be reusable, we need a way to erase that charge before taking a new picture. That is what M2 is for. Ideally we want M2 to be a perfect switch, so that when ERASE is high, C_S is instantly uncharged through M2 and when ERASE is low, M2 does not conduct any current at all.

For the readout we do not want to connect N2 directly to OUT, since the output wire might

be very long and have a big capacitance. Instead, the voltage V_{CS} controls the conductance through a transistor M3. The higher V_{CS}, the lower conductance through M3 and higher voltage on OUT. In that way, the current required to control the voltage on the output wire is supplied through the active load in the top of each output wire, outside the pixel circit.

But since all pixels in the same column share the same output wire we need a way to unconnect N3 from OUT, and that is what M4 is for. M4 is supposed to be an ideal switch so that the pixel is driving OUT only when NRE is low.

2.1.2 Dimensions for switch transistors

The transistors M1, M2 and M4 all function as switches, where a digital gate input decides whether the transistor should act as a short-circuit between drain and source, or as an open circuit. Since these transistors simply should have two possible states, it is key that the leakage current is minimized. This is particularly important for M1 and M2 to ensure that the voltage over C_s is as constant as possible during readout. In *Analog Circuit Design* by Tony Chan Carusone, one can read in section 1.4.1 that the subthreshold leakage current is given by

$$I_{off} = (n-1)\mu_n C_{ox} \left(\frac{W}{L}\right) \left(\frac{kT}{q}\right)^2 \exp\left(-qV_t/nkT\right). \tag{2}$$

In order to minimize this leakage current, $\frac{W}{L}$ need to be as small as possible, meaning the smallest possible width W and the largest possible length L is desired. The technology used will limit the possible width and length of the transistor, thus W and L can be chosen accordingly.

2.1.3 Value for C_s

To choose a suitable value for C_s spice simulations can be used. To know what values are the best we will look at the four corner cases for exposure time and light conditions. The corner cases will be denoted exposure-light, so for example max-min is maximum exposure time and minimum light. For each corner we will do a transient simulation. That means we will look at a graph that shows the voltage over C_s as a function of time. In each light-exposure corner, the resulting voltage value that we are interested in is the voltage over C_s at the end of the exposure. There are many possible approaches to how these corners should be tuned, and the one that we will apply is the following:

- Max-max corner should make C_s fully charged.
- Min-min corner should leave C_s uncharged.
- Min-max and max-min corners should make C_s half full charged.

The reason for why we want the corners to be like that is beyond the scope of this report.

2.1.4 Values for M3 and active load

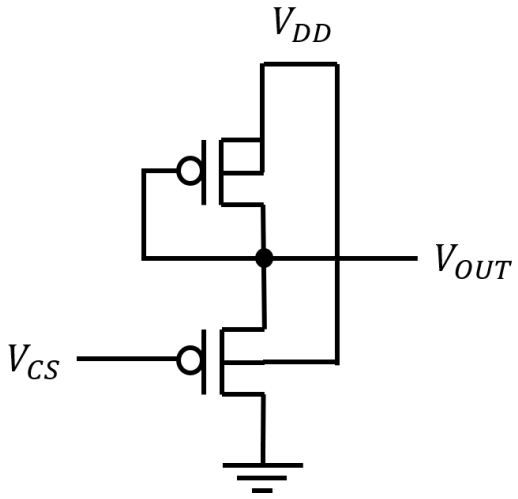


Figure 3: Simplified schematic for output voltage driving circuit.

Values for M3 and active load should be tuned for maximum dynamic range, but it will not have a very big impact since it is a very robust and self-regulating system. If we assume C_{C1} and C_{C2} are very small, the output system can be simplified to figure 3. Essentially, the output voltage V_{OUT} depends on how the conductance in the uppermost and downmost transistor are relative to each other. These conductances are proportional to W/L in the transistors and they also vary with the gate-source voltages. To avoid unnecessary simplifications, it is best to decide these W/L-ratios from SPICE-simulations. One simple way to do a such simulation is to use transient analysis on the netlist for the full analog circuit, set NRE_1 low and NRE_2 high. ERASE should first be high a little while, then when it gets low, EXPOSE goes high, and it should be high long enough for the voltage on the OUT wires to reach its maximum value. The dynamic range is the difference between the maximum and minimum of this curve, and it is preferable that it is as big as possible.

2.2 Digital camera controller

The digital input signals in the analog circuit need to be controlled by a digital circuit - the digital camera controller.

2.2.1 Finite state machine

The wanted behaviour of the digital camera controller is described in the finite state machine (FSM) in figure 4.

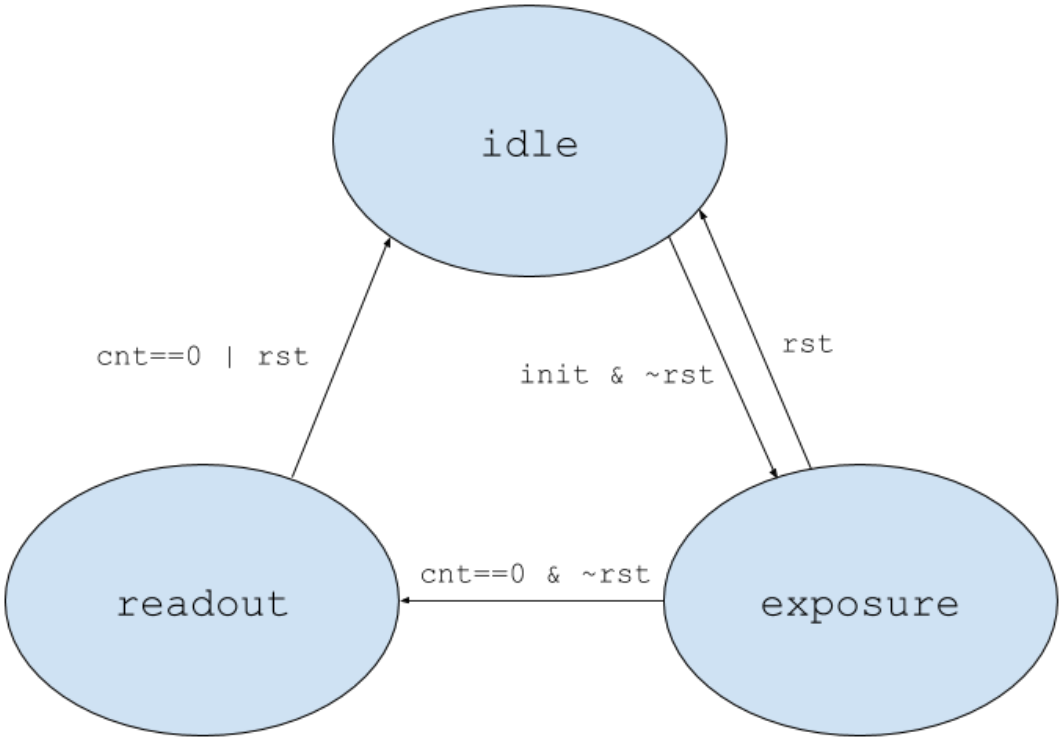


Figure 4: The finite state machine for the digital camera controller.

In the FSM, there are three states. The camera starts in the *idle* state. In this state, the camera isn't in the process of taking any picture, so output signals *expose* and *ADC* should be `LOW`, and *NRE_1* and *NRE_2* should be `HIGH`. The camera should also prepare itself for a new picture in this state, so *erase* should be `HIGH` to erase any voltage from the potential previous exposure. The user should be able to adjust the exposure time with the signals *exp_increase* and *exp_decrease* in the *idle* state. These signals will respectively increase or decrease the exposure time with 1ms for each clock cycle they're `HIGH` to a minimum of 2ms and a maximum of 30ms. When the signal *init* is `HIGH`, which happens when the user presses the shutter button on the camera, the camera will enter the *exposure* state. The exception is if the *rst* input signal is `HIGH`. In any state, *rst* being `HIGH` should override any process and take the camera back to *idle*.

When the camera is entering the *exposure* state, *erase* should be set `LOW` and *expose* should be set `HIGH` to begin the exposure. An internal register *cnt* should hold the exposure time as a number of clock cycles, and decrement for each clock cycle. If *rst* is `HIGH` at any time during *exposure*, the camera should return to the *idle* state. When the *cnt* register has reached 0, the camera should enter the *readout* state if *rst* is `LOW`.

The *readout* state is the final state, in which the data from the individual pixels are read and inputted in the ADC. First, *expose* should be set `LOW` since the exposure is done. Then, *NRE_1* should be `LOW` first at the same time as *ADC* is `HIGH`, to read from the top two

pixels and input it to the ADC. Lastly, *NRE_2* should be `LOW` at the same time as *ADC* is `HIGH` to do the same for the bottom two pixels. Exactly how the output signals should be will be properly explored in the next section. As with the *exposure* state, *rst* being `HIGH` at any time should return the camera to *idle*.

2.2.2 Output timing

The desired time chartis illustrated in figure 5.

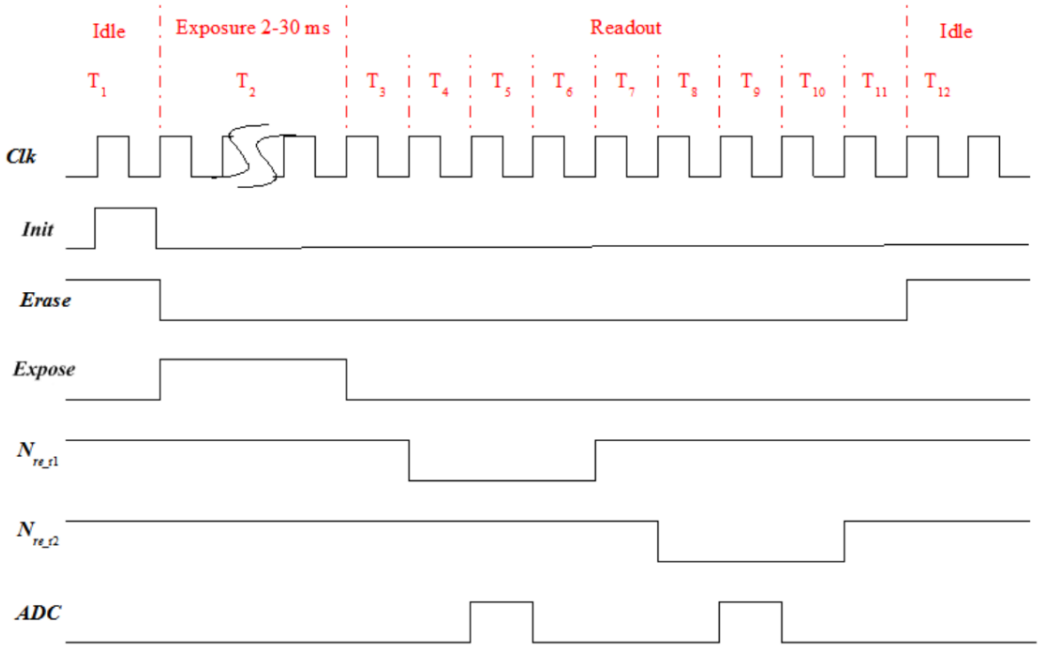


Figure 5: The desired time chart for the output signals of the digital camera controller.

In the *idle* state and *exposure* state, the output signals are as described in the previous subsection. Notably, *erase* is `HIGH` during *idle* and *expose* is `HIGH` during *exposure*. The *readout* state is more complex, as output signals are altered in every clock cycle. In the first cycle, T_3 in the figure, *expose* is set `LOW` to end exposure before readout begins. From T_4 to T_6, *NRE_1* is set `LOW`, with *ADC* being `HIGH` in the middle T_5. This is to ensure that *NRE_1* is not transienting from `HIGH` to `LOW` or `LOW` to `HIGH` while the ADC is reading. In T_7, *NRE_1* is set `HIGH` again. From T_8 to T_{10}, the reading process repeats for *NRE_2* to read the bottom two pixels. In the last clock cycle of the state, T_{11}, *NRE_2* is set `HIGH` again to end the readout.

2.2.3 Module interface

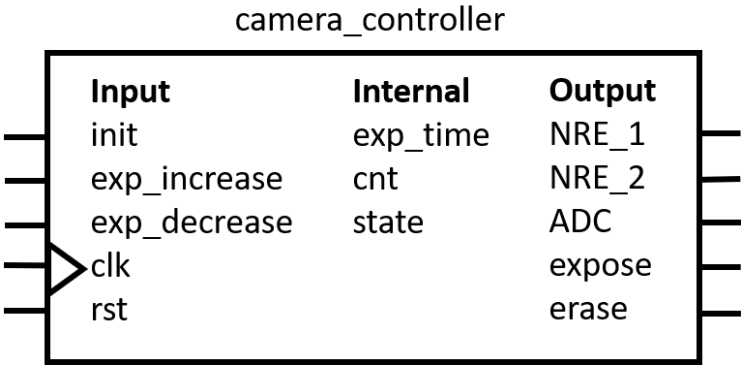


Figure 6: Overview of input and output pins as well as internal regististers for the camera controller module.

3 Results

3.1 Analog pixel circuit

3.1.1 Values and dimensions

The transistor technology used limits the width to

$$1.08\mu\text{m} \leq W \leq 5.04\mu\text{m} \tag{3}$$

and limits the length to

$$0.36\mu\text{m} \leq L \leq 1.08\mu\text{m}. \tag{4}$$

As explained in section 2.1.2, the length and width of the switch transistors will be 1.08μm.

CS was tuned to 2pF. The output from simulations with this value for the exposure-light corners min-min, min-max, max-min and max-max are shown respectively in figures 7, 8, 9 and 10.

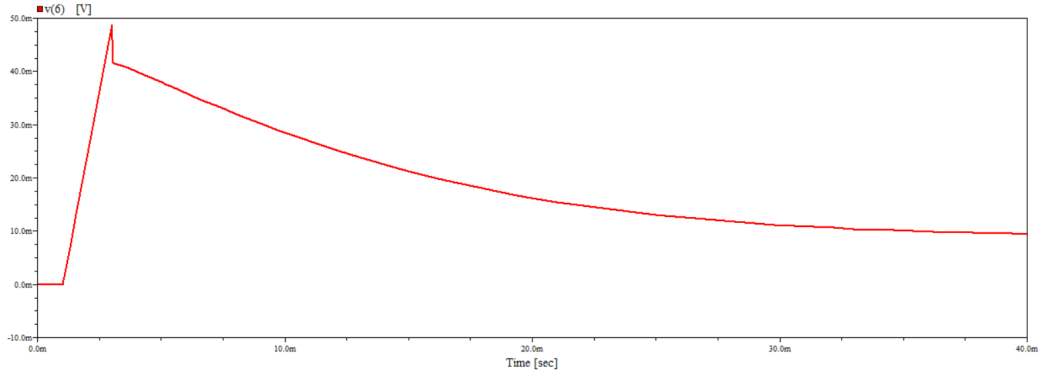


Figure 7: Minimum exposure time - minimum light

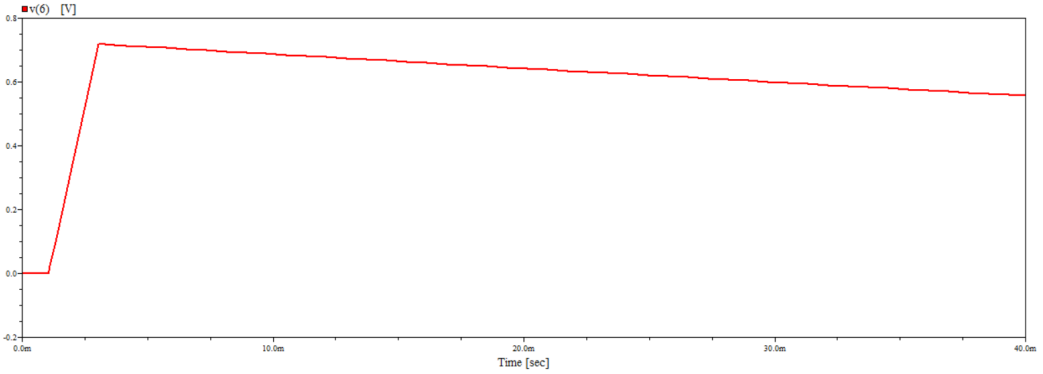


Figure 8: Minimum exposure time - maximum light

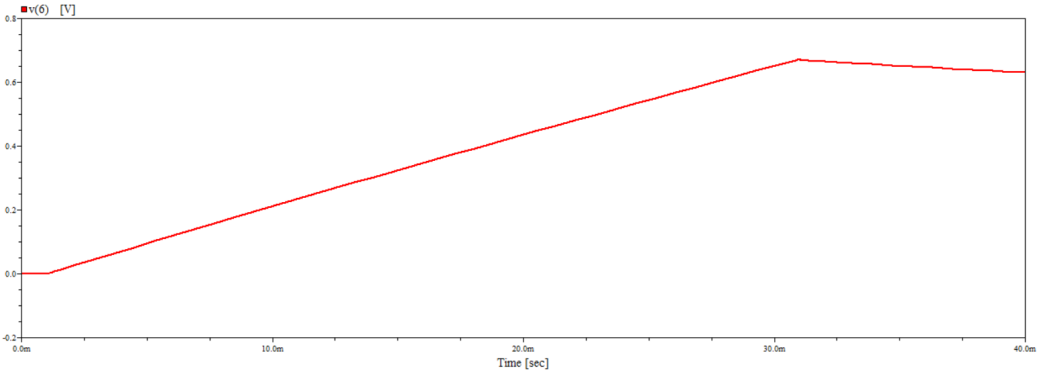


Figure 9: Maximum exposure time - minimum light

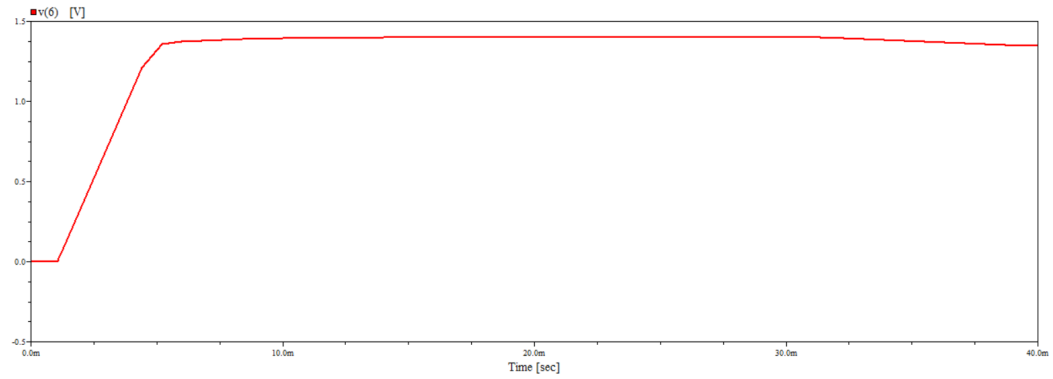
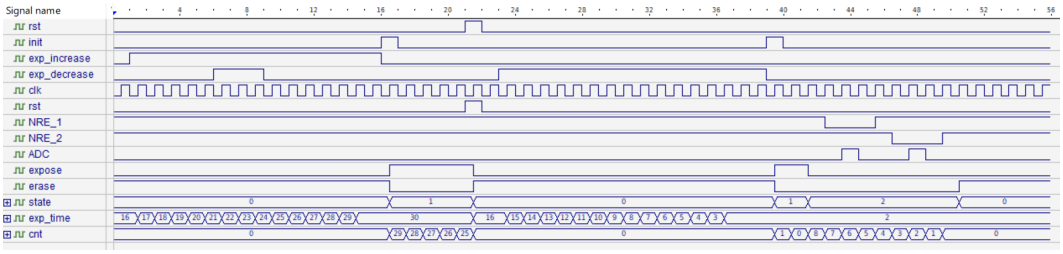


Figure 10: Maximum exposure time - maximum light



3.1.2 Analog circuit simulation

3.2 Digital circuit

3.2.1 Digital circuit simulation

Explaining the big waveform.

4 Discussion