Project report intergrated circuits

Sara Roberg Ghabeli, Sigurd Hagen Tullander

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1 Introduction

“Hello Dirty talk”

2 Theory

2.1 Analog circuit

The analog circuit has input signals delivered by the digital circuitry, and delivers its output to two ADCs. The analog circuit diagram is given in figure 1, where each of the four pixel block has the circuit given in figure 2.

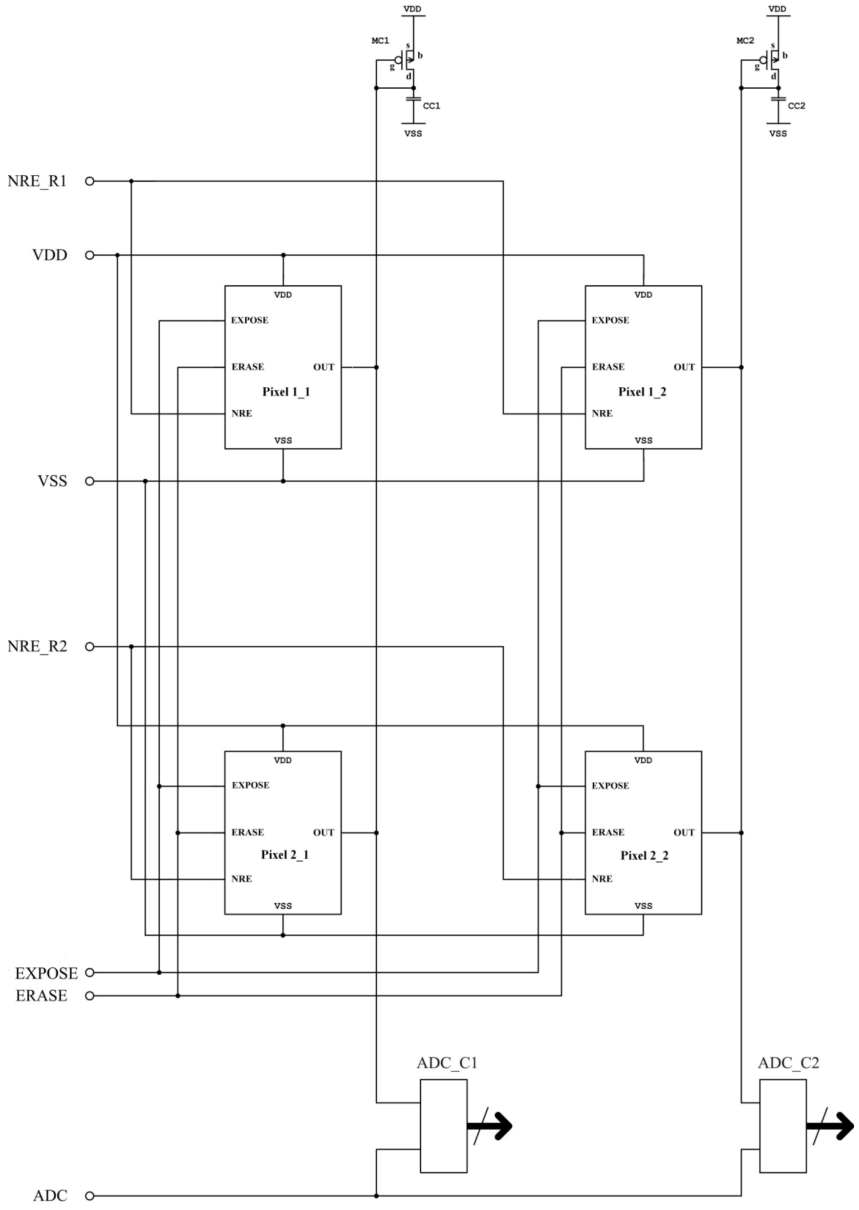


Figure 1: Analog circuit schematic.

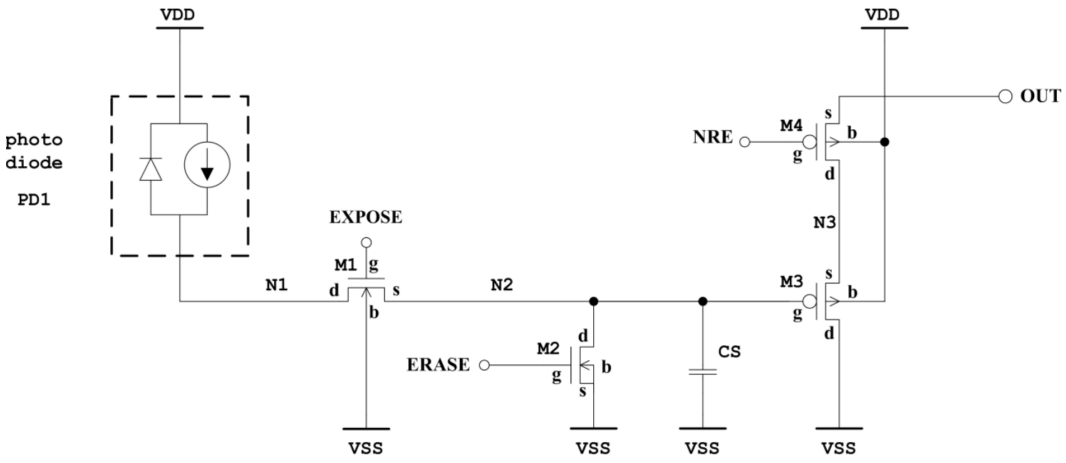


Figure 2: Pixel cicuit schematic.

In detail, the analog circuit consists of 4 pixels in a 2x2 array. Each pixel in the same row shares the same NRE (Not-REad) input which means they are sending data to the ADC at the same time. Each pixel in the same column share the same active load and readout wire, which means they need to send data to the ADC at different times.

2.1.1 Detailed decription of pixel circuit

The pixel circuit consists of

2.1.2 Dimensions for switch transistors

The transistors M1, M2 and M4 all function as switches, where a digital gate input decides whether the transistor should act as a short-circuit between drain and source, or as an open circuit. Since these transistors simply should have two possible states, it is key that the leakage current is minimized. This is particularly important for M1 and M2 to ensure that the voltage over C_s is as constant as possible during readout. In *Analog Circuit Design* by Tony Chan Carusone, one can read in section 1.4.1 that the subthreshold leakage current is given by

$$I_{off} = (n-1)\mu_n C_{ox} \left(\frac{W}{L}\right) \left(\frac{kT}{q}\right)^2 \exp\left(-qV_t/nkT\right). \tag{1}$$

In order to minimize this leakage current, $\frac{W}{L}$ need to be as small as possible, meaning the smallest possible width W and the largest possible length L is desired. The technology used will limit the possible width and length of the transistor, thus W and L can be chosen accordingly.

2.1.3 Value for C_s

To choose a suitable value for C_s spice simulations can be used. To know what values are the best we will look at the four corner cases for exposure time and light conditions. The corner cases will be denoted exposure-light, so for example max-min is maximum exposure time

and minimum light. For each corner we will do a transient simulation. That means we will look at a graph that shows the voltage over C_s as a function of time. In each light-exposure corner, the resulting voltage value that we are interested in is the voltage over C_s at the end of the exposure. There are many possible approaches to how these corners should be tuned, and the one that we will apply is the following:

- Max-max corner should make C_s fully charged.
- Min-min corner should leave C_s uncharged.
- Min-max and max-min corners should make C_s half full charged.

The reason for why we want the corners to be like that is beyond the scope of this report.

2.1.4 Values for M3 and active load

2.2 Digital camera controller

The digital input signals in the analog circuit need to be controlled by a digital circuit - the digital camera controller.

2.2.1 Finite state machine

The wanted behaviour of the digital camera controller is described in the finite state machine (FSM) in figure 3.

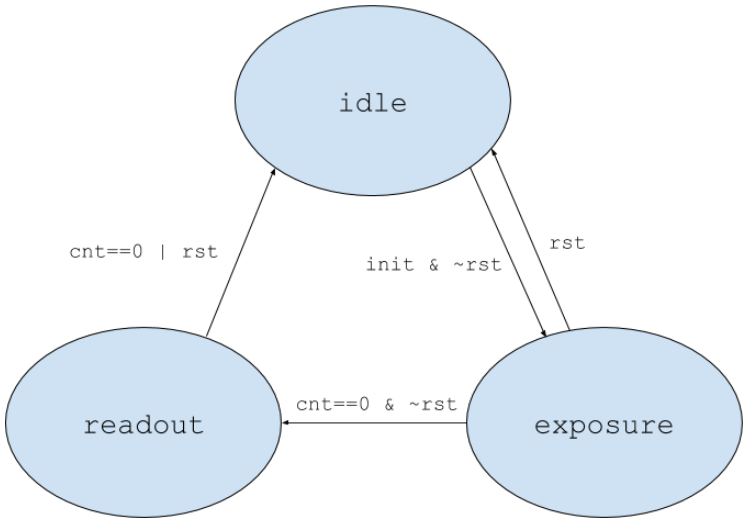


Figure 3: The finite state machine for the digital camera controller.

In the FSM, there are three states. The camera starts in the *idle* state. In this state, the camera isn't in the process of taking any picture, so output signals *expose* and *ADC* should be `LOW`, and *NRE_1* and *NRE_2* should be `HIGH`. The camera should also prepare itself for a new picture in this state, so *erase* should be `HIGH` to erase any voltage from the potential previous exposure. The user should be able to adjust the exposure time with the signals

exp_increase and *exp_decrease* in the *idle* state. These signals will respectively increase or decrease the exposure time with 1ms for each clock cycle they're `HIGH` to a minimum of 2ms and a maximum of 30ms. When the signal *init* is `HIGH`, which happens when the user presses the shutter button on the camera, the camera will enter the *exposure* state. The exception is if the *rst* input signal is `HIGH`. In any state, *rst* being `HIGH` should override any process and take the camera back to *idle*.

When the camera is entering the *exposure* state, *erase* should be set `LOW` and *expose* should be set `HIGH` to begin the exposure. An internal register *cnt* should hold the exposure time as a number of clock cycles, and decrement for each clock cycle. If *rst* is `HIGH` at any time during *exposure*, the camera should return to the *idle* state. When the *cnt* register has reached 0, the camera should enter the *readout* state if *rst* is `LOW`.

The *readout* state is the final state, in which the data from the individual pixels are read and inputted in the ADC. First, *expose* should be set `LOW` since the exposure is done. Then, *NRE_1* should be `LOW` first at the same time as *ADC* is `HIGH`, to read from the top two pixels and input it to the ADC. Lastly, *NRE_2* should be `LOW` at the same time as *ADC* is `HIGH` to do the same for the bottom two pixels. Exactly how the output signals should be will be properly explored in the next section. As with the *exposure* state, *rst* being `HIGH` at any time should return the camera to *idle*.

2.2.2 Output timing

2.2.3 Module interface

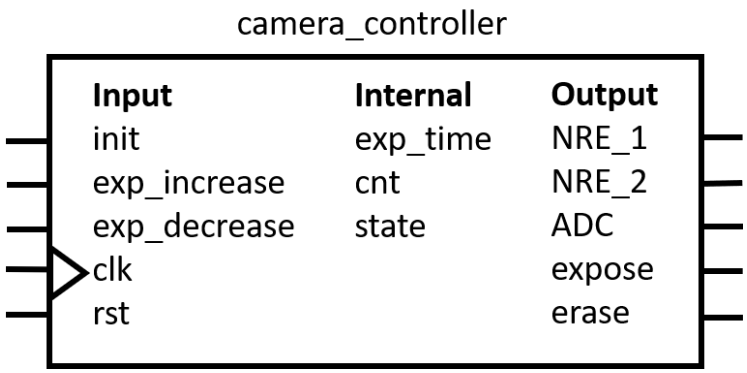


Figure 4: Overview of input and output pins as well as internal regististers for the camera controller module.

3 Results

3.1 Analog pixel circuit

3.1.1 Values and dimensions

The transistor technology used limits the width to

$$1.08\mu\text{m} \leq W \leq 5.04\mu\text{m} \tag{2}$$

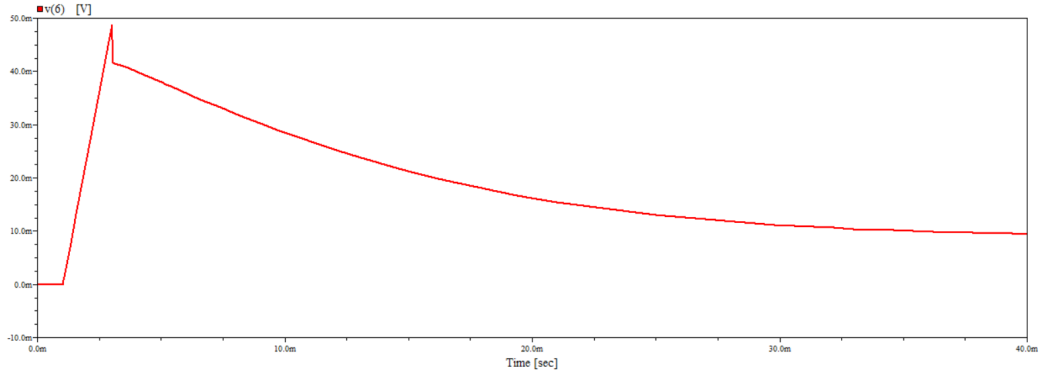


Figure 5: Minimum exposure time - minimum light

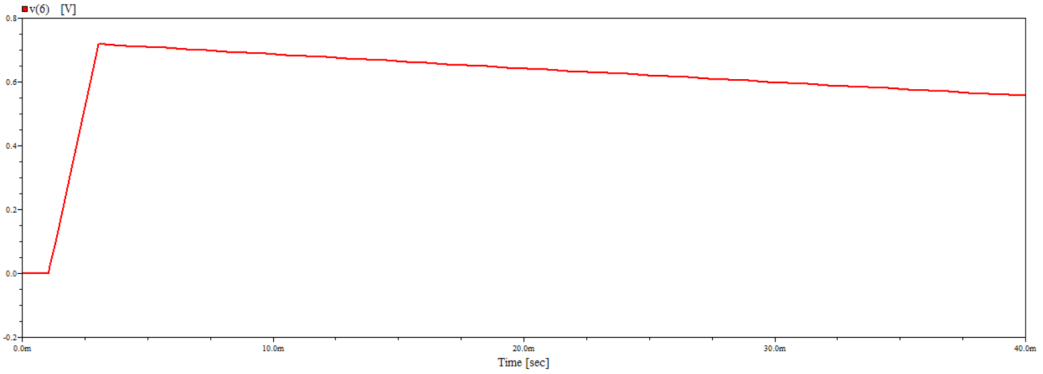


Figure 6: Minimum exposure time - maximum light

and limits the length to

$$0.36\mu\text{m} \leq L \leq 1.08\mu\text{m}. \tag{3}$$

As explained in section 2.1.2, the length and width of the switch transistors will be 1.08μm.

CS was tuned to 2pF. The output from simulations with this value for the exposure-light corners min-min, min-max, max-min and max-max are shown respectively in figures 5, 6, 7 and 8.

3.1.2 Analog circuit simulation

3.2 Digital circuit

3.2.1 Digital circuit simulation

Explaining the big waveform.

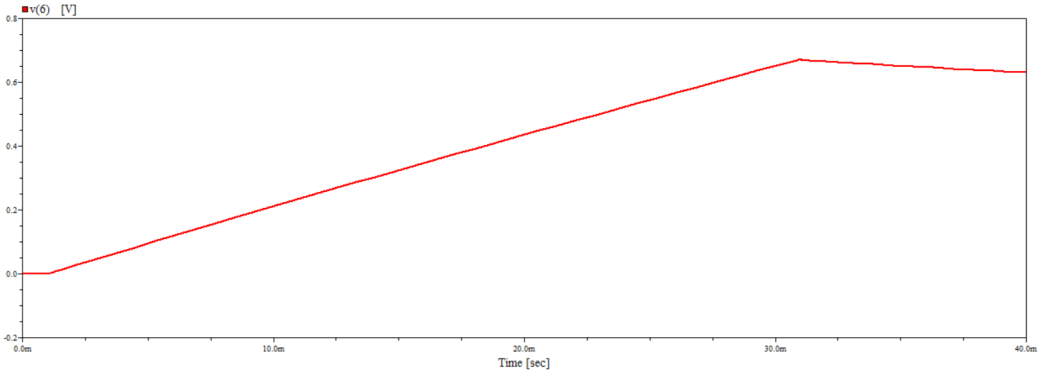


Figure 7: Maximum exposure time - minimum light

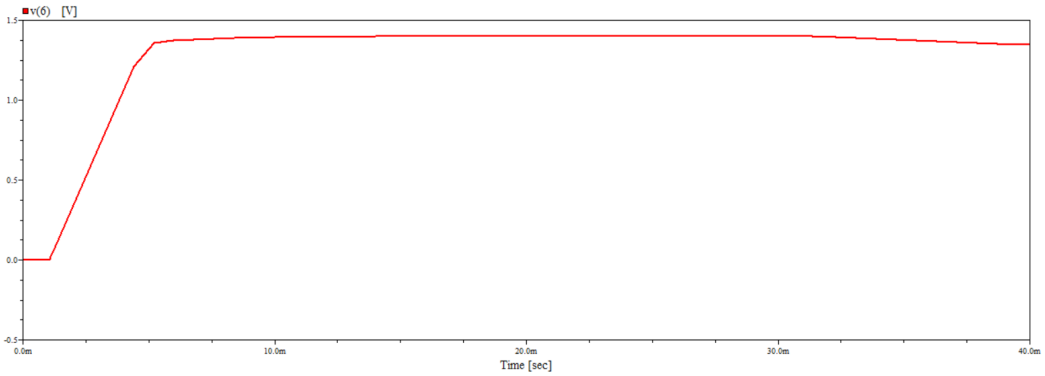
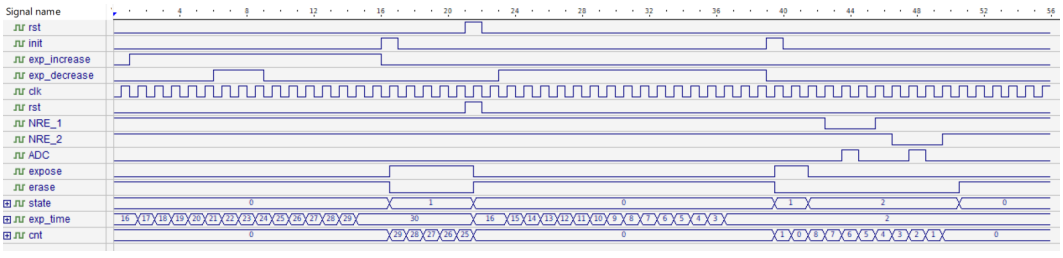


Figure 8: Maximum exposure time - maximum light



4 Discussion