Project report intergrated circuits

Sara Roberg Ghabeli, Sigurd Hagen Tullander

Fall 2020

1 Introduction

"Hello Dirty talk"

2 Theory

2.1 Analog circuit

The analog circuit has input signals delivered by the digital circuitry, and delivers its output to two ADCs. The analog circuit diagram is given in figure 1, where each of the four pixel block has the circuit given in figure 2.

In detail, the analog circuit consists of 4 pixels in a 2x2 array. Each pixel in the same row shares the same NRE (Not-REad) input which means they are sending data to the ADC at the same time. Each pixel in the same column share the same active load and readout wire, which means they need to send data to the ADC at different times.

2.1.1 Detailed decription of pixel circuit

Schematics for the pixel circuit is given in figure 2. It consists of a photo diode PD1, three switch transistors M1, M2 and M4, one buffer transistor M3 and a charge storage capacitor C_S. The photo diode is modeled by a diode and an ideal current source in parallel. The current source outputs a current I_D that is proportional to the illumination intensity on that particular pixel. This current is used to charge the transistor C_S. Ideally, we want that all of I_D flows through M1 and into CS when EXPOSE is high and all of I_D flows back through the diode in the photo diode model when EXPOSE is low.

2.1.2 Dimensions for switch transistors

The transistors M1, M2 and M4 all function as switches, where a digital gate input decides whether the transistor should act as a short-circuit between drain and source, or as an open circuit. Since these transistors simply should have two possible states, it is key that the leakage current is minimized. This is particularly important for M1 and M2 to ensure that the voltage over C_s is as constant as possible during readout. In *Analog Circuit Design* by Tony Chan Carusone, one can read in section 1.4.1 that the subthreshold leakage current is given by

$$I_{off} = (n-1)\mu_n C_{ox}\left(\frac{W}{L}\right)\left(\frac{kT}{q}\right)^2 \exp\left(-qV_t/nkT\right). \tag{1}$$

In order to minimize this leakage current, $\frac{W}{L}$ need to be as small as possible, meaning the smallest possible width W and the largest possible length L is desired. The technology used will limit the possible width and length of the transistor, thus W and L can be chosen accordingly.

2.1.3 Value for C_s

To choose a suitable value for C_s spice simulations can be used. To know what values are the best we will look at the four corner cases for exposure time and light conditions. The corner cases will be denoted exposure-light, so for example max-min is maximum exposure time

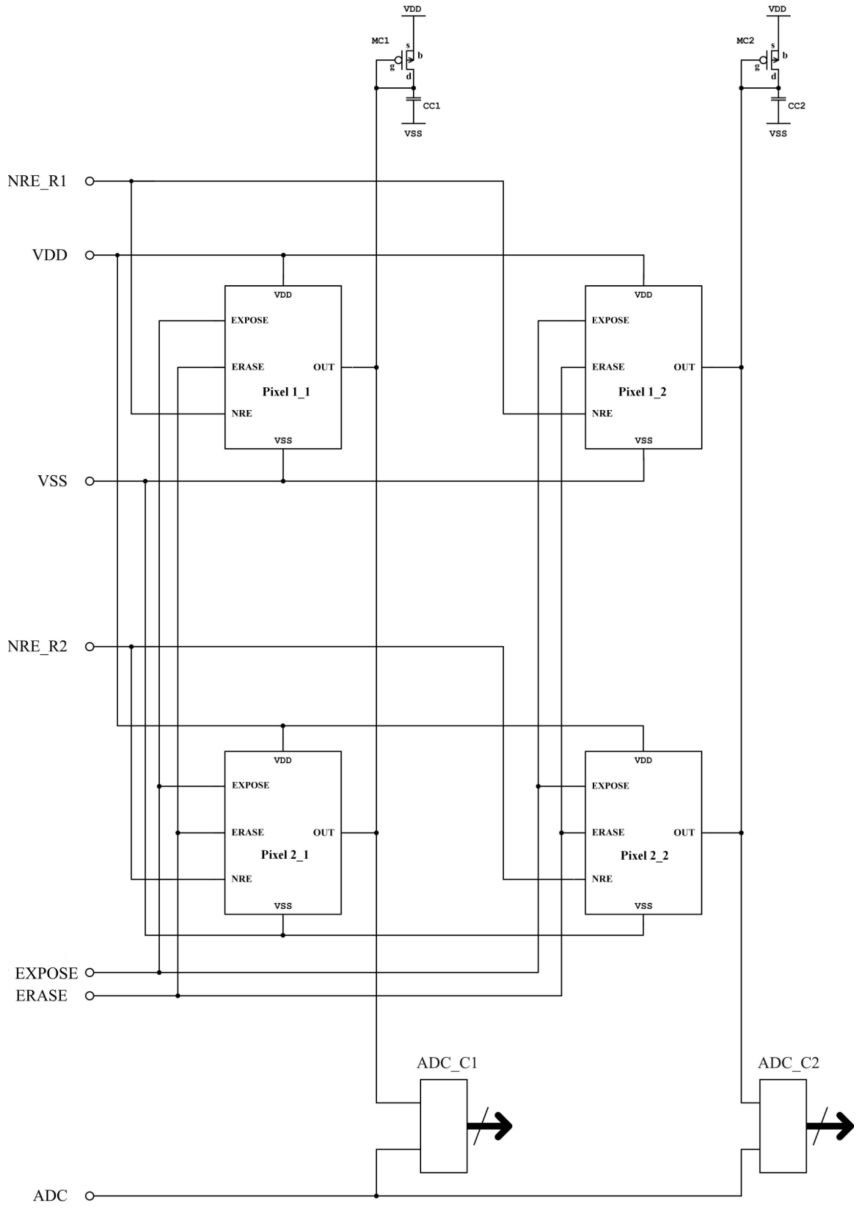


Figure 1: Analog circuit schematic.

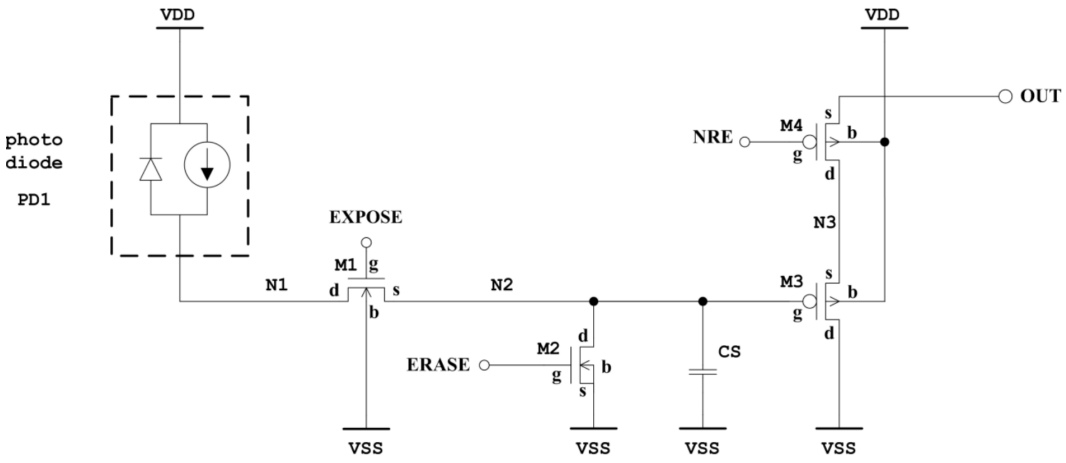


Figure 2: Pixel cicuit schematic.

and minimum light. For each corner we will do a transient simulation. That means we will look at a graph that shows the voltage over C_s as a function of time. In each light-exposure corner, the resulting voltage value that we are interested in is the voltage over C_s at the end of the exposure. There are many possible approaches to how these corners should be tuned, and the one that we will apply is the following:

- Max-max corner should make C_s fully charged.
- Min-min corner should leave C_s uncharged.
- Min-max and max-min corners should make C_s half full charged.

The reason for why we want the corners to be like that is beyond the scope of this report.

2.1.4 Values for M3 and active load

2.2 Digital camera controller

2.2.1 Finite state machine

2.2.2 Output timing

2.2.3 Module interface

3 Results

3.1 Analog pixel circuit

3.1.1 Values and dimensions

The transistor technology used limits the width to

$$1.08\mu\text{m} \leq W \leq 5.04\mu\text{m} \tag{2}$$

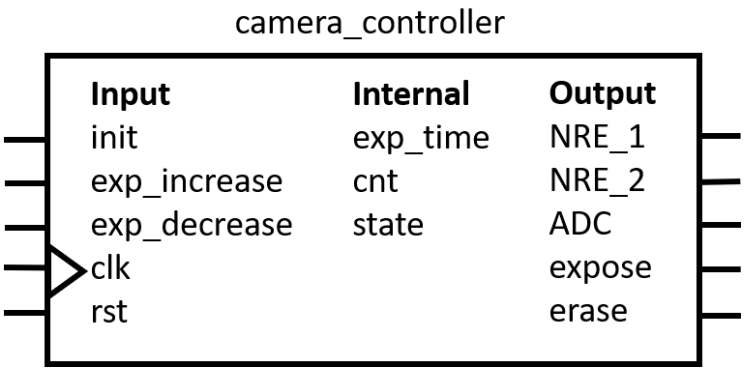


Figure 3: Overview of input and output pins as well as internal regististers for the camera controller module.

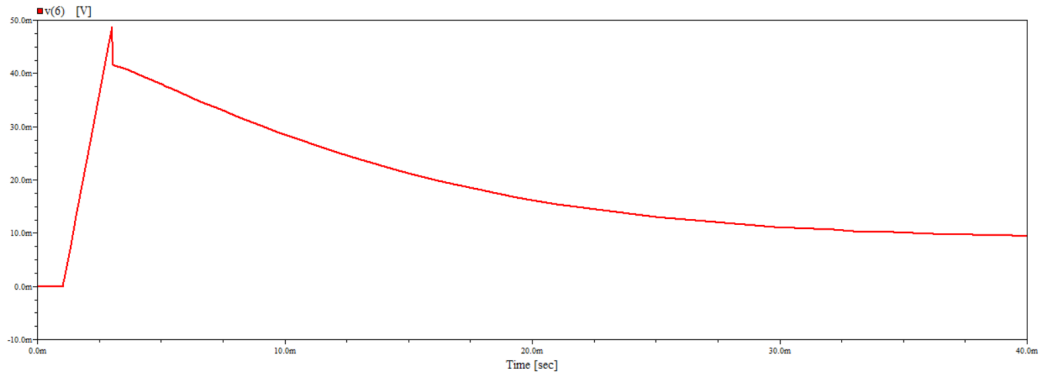


Figure 4: Minimum exposure time - minimum light

and limits the length to

$$0.36\mu\text{m} \leq L \leq 1.08\mu\text{m}. \tag{3}$$

As explained in section 2.1.2, the length and width of the switch transistors will be 1.08μm.

CS was tuned to 2pF. The output from simulations with this value for the exposure-light corners min-min, min-max, max-min and max-max are shown respectively in figures 4, 5, 6 and 7.

3.1.2 Analog circuit simulation

3.2 Digital circuit

3.2.1 Digital circuit simulation

Explaining the big waveform.

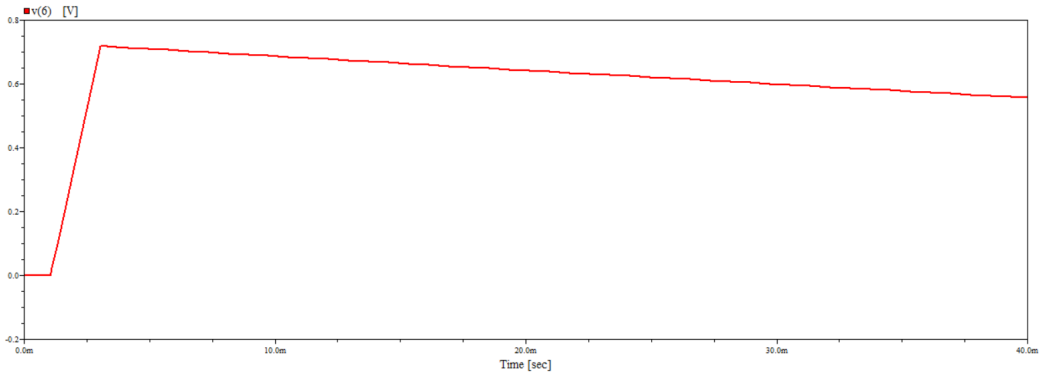


Figure 5: Minimum exposure time - maximum light

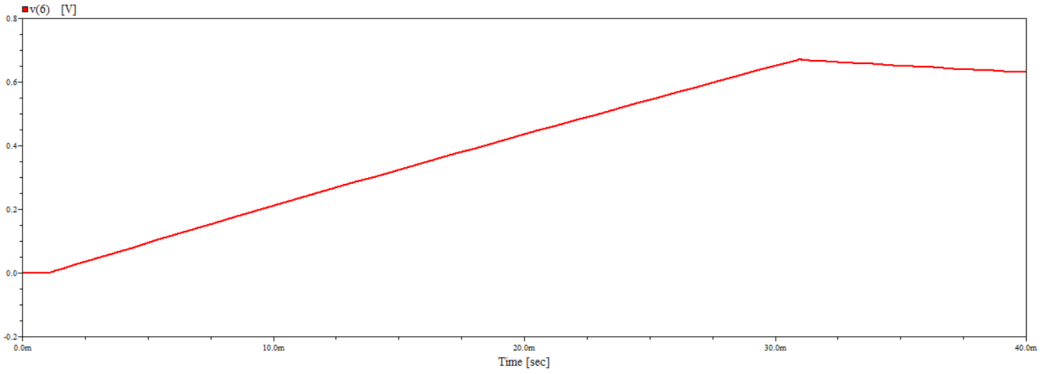


Figure 6: Maximum exposure time - minimum light

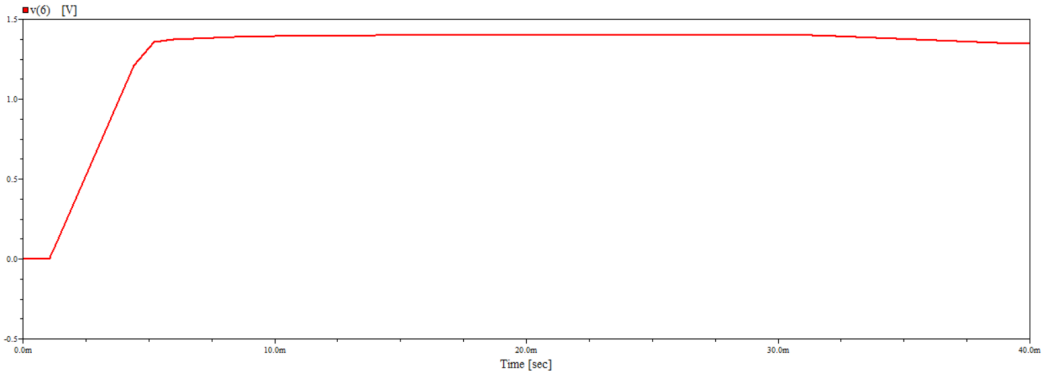
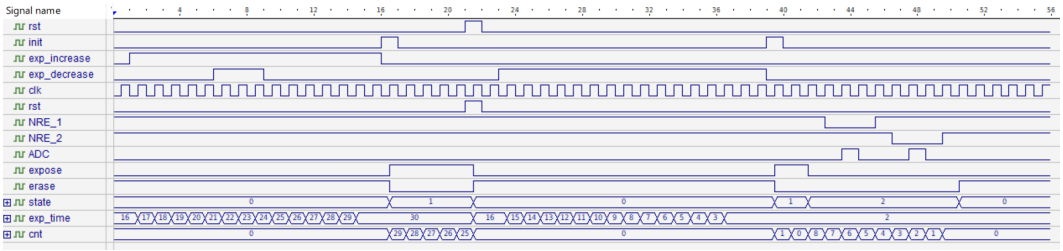


Figure 7: Maximum exposure time - maximum light



4 Discussion