

A

B

C

D

A

B

C

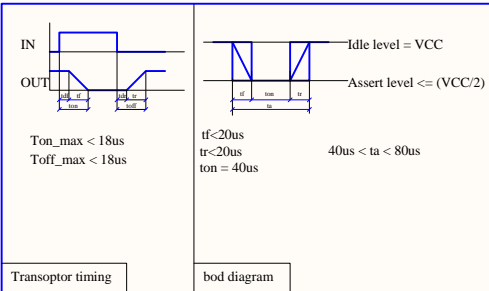
D

1

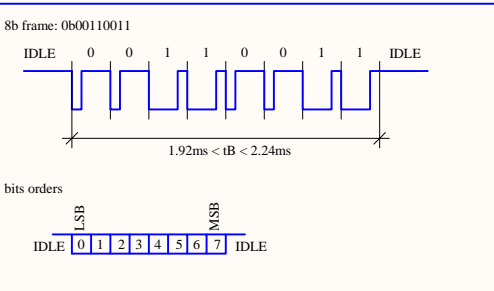
2

3

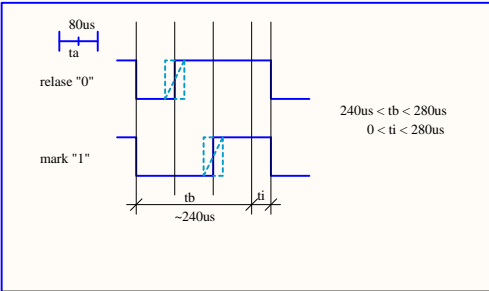
4



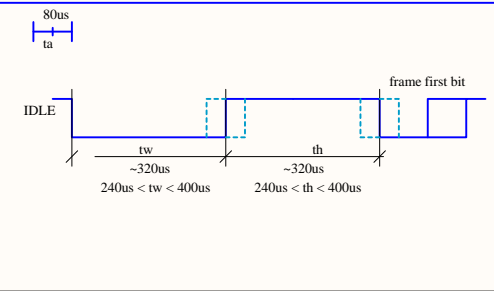
Timing diagrams for basic signals



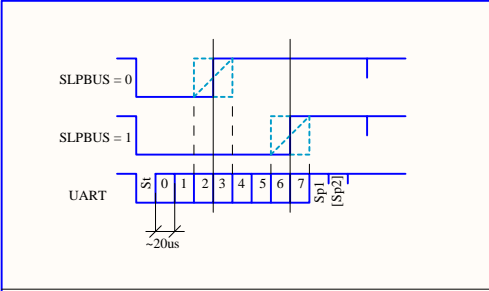
Byte format



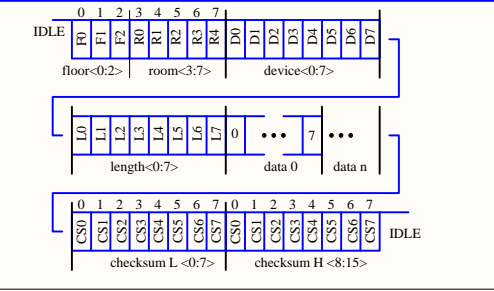
Timing diagrams for release "0" and mark "1" signals



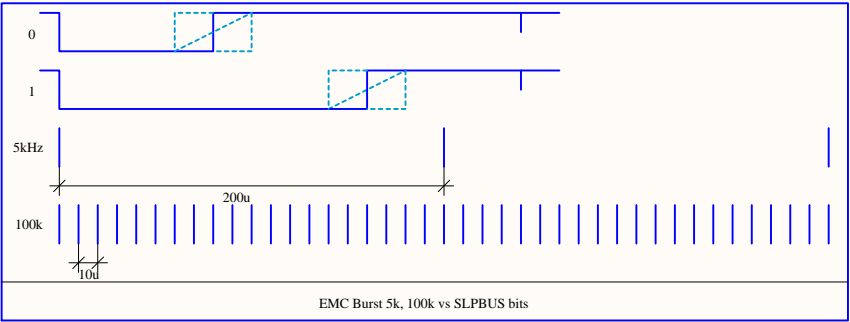
Wake Up frame



UART vs SLPBUS bit



Physical layer frame



1

2

3

4

Title		
Size	Number	Revision
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