8.6.1.3 Registers R10, R9, and R8

These registers control functions that are not disclosed to the user and the power on default values are not optimal. Therefore these registers need to be programmed to the values specified in the register map for proper operation.

8.6.1.4 Register R7

This register has words that control status pins, which would be LD, MUXout, and FLout

8.6.1.4.1 FL_PINMODE[2:0], MUXOUT_PINMODE[2:0], and LD_PINMODE[2:0] — Output Format for Status Pins

These words control the state of the output pin.

FL_PINMODE MUXOUT_PINMODE LD_PINMODE	OUTPUT TYPE
0	TRI-STATE (Default for LD_PINMODE)
1	Push-Pull (Default for MUXOUT_PINMODE)
2	Open Drain
3	High Drive Push-Pull (Can drive 5 mA for an LED)
4	High Drive Open Drain
5	High Drive Open Source
6,7	Reserved

8.6.1.4.2 FL_INV, MUX_INV, LD_INV - Inversion for Status Pins

The logic for the LD and MUXOUT pins can be inverted with these bits.

FL_INV MUX_INV LD_INV	PIN STATUS
0	Normal Operation
1	Inverted

8.6.1.4.3 FL_SELECT[4:0], MUXOUT_SELECT[4:0], LD_SELECT[4:0] — State for Status Pins

This word controls the output state of the MUXout, LD, and FLout pins. Note that during fastlock, the FL_SELECT word is ignored.

FL_SELECT MUXOUT_SELECT LD_SELECT	OUTPUT
0	GND
1	Digital Lock Detect (Based on Phase Measurement)
2	Vtune Lock Detect (Based on tuning voltage)
3	Lock Detect (Based on Phase Measurement AND tuning voltage)
4	Readback (Default for MUXOUT_SELECT)
5	PLL_N divided by 2
6	PLL_N divided by 4
7	PLL_R divided by 2
8	PLL_R divided by 4
9	Analog Lock Detect
10	OSCin Detect
11	Fin Detect
12	Calibration Running
13	Tuning Voltage out of Range
14	VCO calibration fails in the low frequency direction.
15	VCO Calibration fails in the high frequency direction.
16-31	Reserved