8.6.1.6 Register R5

8.6.1.6.1 OUT_LDEN — Mute Outputs Based on Lock Detect

When this bit is enabled, the RFoutA and RFoutB pins are disabled if the PLL digital lock detect circuitry indicates that the PLL is in the unlocked state.

OUT_LDEN	PLL DIGITAL LOCK DETECT STATUS	RFoutA / RFoutB PINS
0	Don't Care	Normal Operation
1	Locked	Normal Operation
1	Unlocked	Powered Down

8.6.1.6.2 OSC_FREQ[2:0] — OSCin Frequency for VCO Calibration

This word should be set to in accordance to the OSCin frequency BEFORE the doubler. It is critical for running internal calibrations for this device.

OSC_FREQ	OSCin FREQUENCY
0	f_{OSCin} < 64 MHz
1	64 ≤ f_{OSCin} < 128 MHz
2	128 ≤ f_{OSCin} < 256 MHz
3	256 ≤ f_{OSCin} < 512 MHz
4	512 ≤ f_{OSCin}
≥ 5	Reserved

8.6.1.6.3 BUFEN_DIS - Disable for the BUFEN Pin

This pin allows the BUFEN pin to be disabled. This is useful if one does not want to pull this pin high or use it for the readback ID.

BUFEN_DIS	BUFEN PIN
0	Impacts Output buffers
1	Ignored.

8.6.1.6.4 VCO_SEL_MODE — Method of Selecting Internal VCO Core

This word allows the user to choose how the VCO selected by the VCO_SEL word is treated. Note setting 0 should not be used if switching from a frequency above 3 GHz to a frequency below 2.2 GHz.

VCO_SEL_MODE	VCO SELECTION
0	VCO core is automatically selected based on the last one that was used. If none was used before, it chooses the lowest frequency VCO core.
1	VCO selection starts at the value as specified by the VCO_SEL word. However, if this is invalid, it will choose another VCO.
2	VCO is forced to the selection as defined by the VCO_SEL word, regardless of whether it is valid or not. Note that this mode is not ensured and is only included for diagnostic purposes.
3	Reserved

8.6.1.6.5 OUTB_MUX — Mux for RFoutB

This word determines whether RFoutB is the VCO frequency, the VCO frequency divided by VCO_DIV, or the fin frequency.

OUTB_MUX	RFoutB FREQUENCY
0	f_{VCO}
1	f_{VCO} / VCO_DIV
2	f_{Fin}
3	Reserved

8.6.1.6.6 OUTA_MUX — Mux for RFoutA

This word determines whether RFoutA is the VCO frequency, the VCO frequency divided by VCO_DIV, or the fin frequency.

OUTA_MUX	RFoutA FREQUENCY
0	f_{VCO}
1	f_{VCO} / VCO_DIV
2	f_{Fin}
3	Reserved

8.6.1.6.7 0_DLY - Zero Delay Mode

When this mode is enabled, the VCO divider is put in the feedback path of the PLL so that the delay from input to output of the device will be deterministic.

0_DLY	PHASE DETECTOR INPUT
0	Direct VCO or Fin signal.
1	Channel Divider output.

8.6.1.6.8 MODE[1:0] — Operating Mode

This word determines in what mode the device is run.

MODE	OPERATIONAL MODE	PLL	VCO	FIN PIN
0	Full Chip Mode	Powered Up	Powered Up	Powered Down
1	PLL Only Mode	Powered Up	Powered Down	Powered Down
2,3	Reserved	Reserved	Reserved	Reserved

8.6.1.6.9 PWDN_MODE - Powerdown Mode

This word powers the device up and down. Aside from the traditional power up and power down, there is the partial powerdown that powers down the PLL and VCO, but keeps the LDOs powered up to allow the device to power up faster.

PWDN_MODE	CE Pin	DEVICE STATUS
0	X	Powered Up
1	X	Full Powerdown
2	X	Reserved
3	X	Partial Powerdown
4	Low	Full Powerdown
	High	Powered Up
5	X	Reserved
6	Low	Partial Powerdown
	High	Powered Up
7	Low	Full Powerdown
	High	Partial Powerdown

8.6.1.6.10 RESET - Register Reset

When this bit is enabled, the action of programming register R5 resets all registers to their default power on reset status, otherwise the words in register 5 may be programmed without resetting all the registers.

RESET	ACTION of PROGRAMMING REGISTER R5
0	Registers and state machines are operational.
1	Registers and state machines are reset, then this reset is automatically released.