8.6.1 Programming Word Descriptions

8.6.1.1 Register R15

The programming of register R15 is only necessary when one wants to change the default value of VCO_CAPCODE for improving the VCO calibration time or use the VCO_CAP_MAN bit for diagnostic purposes.

8.6.1.1.1 VCO_CAP_MAN — Manual VCO Band Select

This bit determines if the value of VCO_CAPCODE is just used as a starting point for the initial frequency calibration or if the VCO is forced to this value. If this is forced, it is only for diagnostic purposes.

VCO_CAP_MAN	IMPACT of VCO_CAPCODE
0	VCO_CAPCODE value is initial starting point for VCO digital calibration.
1	VCO_CAPCODE value is forced all the time. For diagnostic purposes only.

8.6.1.1.2 VCO_CAPCODE[7:0] — Capacitor Value for VCO Band Selection

This word selects the VCO tank capacitor value that is initially used when VCO calibration is run or that is forced when VCO_CAP_MAN is set to one. The lower values correspond to less capacitance, which corresponds to a higher VCO frequency for a given VCO Core. If this word is not programmed, it is defaulted to 128.

VCO_CAPCODE	VCO TANK CAPACITANCE	VCO FREQUENCY
0	Minimum	Highest
...	...	...
255	Maximum	Lowest

8.6.1.2 Register R13

Register R13 gives access to words that are used for the digital lock detect circuitry.

8.6.1.2.1 DLD_ERR_CNT[3:0] - Digital Lock Detect Error Count

This is the amount of phase detector comparisons that may exceed the tolerance as specified in DLD_TOL before digital lock indicates an unlocked state. The recommended default is 4 for phase detector frequencies of 80 MHz or below; higher frequencies may require the user to experiment to optimize this value.

8.6.1.2.2 DLD_PASS_CNT[9:0] - Digital Lock Detect Success Count

This value multiplied by 8 is the amount of phase detector comparison within the tolerance specified by DLD_TOL and adjusted by DLD_ERR_CNT that are necessary to cause the digital lock to indicate a locked state. The recommended value is 32 for phase detector frequencies of 80 MHz or below; higher frequencies may require the user to experiment and optimize this value based on application.

8.6.1.2.3 DLD_TOL[2:0] — Digital Lock Detect

This is the tolerance that is used to compare with each phase error to decide if it is a success or a fail. Larger settings are generally recommended, but they are limited by several factors such as PFD_DLY, modulator order, and especially the phase detector frequency.

DLD_TOL	PHASE ERROR TOLERANCE (ns)	TYPICAL PHASE DETECTOR FREQUENCY
0	1	Fpd > 130 MHz
1	1.7	80 MHz < Fpd ≤ 130 MHz
2	3	60 MHz < Fpd ≤ 80 MHz
3	6	45 MHz < Fpd ≤ 60 MHz
4	10	30 MHz <Fpd ≤ 45 MHz
5	18	Fpd ≤ 30 MHz
6–7	Reserved	n/a