8.6.1.11 Register R0

Register R0 controls the frequency of the device. Also, unless disabled by setting NO_FCAL = 1, the action of writing to the R0 register triggers a frequency calibration for the internal VCO.

8.6.1.11.1 ID - Part ID Readback

When this bit is set, the part ID indicating the device is an LMX2581 is read back from the device. Consult the Feature Description for more details.

ID	READBACK MODE
0	Register
1	Part ID

8.6.1.11.2 FRAC_DITHER[1:0] — PLL Fractional Dithering

This word sets the dithering mode. When the fractional numerator is zero, it is recommended, although not required, to set the FRAC_DITHER mode to disabled for the best possible spurs. Doing this shuts down the fractional circuitry and eliminates fractional spurs for these frequencies. This is the reason why the FRAC_DITHER word is in the R0 register, so that it can be set correctly for every frequency if this setting changes.

FRAC_DITHER	DITHERING MODE
0	Weak
1	Medium
2	Strong
3	Disabled

8.6.1.11.3 NO_FCAL — Disable Frequency Calibration

Normally, when the R0 register is written to, a frequency calibration for the internal VCO is triggered. However, this feature may be disabled. If the frequency is changed, then this frequency calibration is necessary for the internal VCO.

NO_FCAL	VCO FREQUENCY CALIBRATION
0	Done upon write to R0 Register
1	Not done on write to R0 Register

8.6.1.11.4 PLL_N - PLL Feedback Divider Value

This is the feedback divider value for the PLL. There are some restrictions on this depending on the modulator order.

PLL_N	PLL_N[11:0]											
<7	Invalid state											
7	Possible only in integer mode or with a 1st order modulator											
8-9	Possible in integer mode, 1st order modulator, or 2nd order modulator											
10-13	Possible only in integer mode, 1st order modulator, 2nd order modulator, or 3rd order modulator											
14	0	0	0	0	0	0	0	0	1	1	1	0
...	...	...	...	...	...	...	...	...	...	...	...	...
4095	1	1	1	1	1	1	1	1	1	1	1	1

8.6.1.11.5 PLL_NUM[21:12] and PLL_NUM[11:0] — PLL Fractional Numerator

These words control the numerator for the PLL fraction.

PLL_NUM	PLL_NUM[21:12]										PLL_NUM[11:0]											
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
4095	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
4096	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1