8.6.1.10 Register R1

8.6.1.10.1 CPG[4:0] — PLL Charge Pump Gain

This word determines the charge pump current that used during steady state operation.

CPG	CHARGE PUMP CURRENT STATE
0	TRI-STATE
1	1X
2	2X
..	...
31	31X

Note that if the CPG setting is 400 µA or lower, then the CPG_BLEED word needs to be set to 0.

8.6.1.10.2 VCO_SEL[1:0] - VCO Selection

These words allow the user to specify which VCO the frequency calibration starts at. If uncertain, program this word to 0 to start at the lowest frequency VCO core. A programming setting of 3 (VCO 4) should not be used if switching to a frequency below 2.2 GHz.

VCO_SEL	VCO SELECTION
0	VCO 1 (Lowest Frequency)
1	VCO 2
2	VCO 3
3	VCO 4 (Highest Frequency)

8.6.1.10.3 FRAC_ORDER[2:0] — PLL Delta Sigma Modulator Order

This word sets the order for the fractional engine.

FRAC_ORDER	MODULATOR ORDER
0	Integer Mode
1	1st Order Modulator
2	2nd Order Modulator
3	3rd Order Modulator
4-7	Reserved

8.6.1.10.4 PLL_R[7:0] — PLL R divider

This word sets the value that divides the OSCin frequency.

PLL_R	PLL_R DIVIDER VALUE
0	256
1	1 (bypass)
...	...
255	255