8.6.1.7 Register R4

8.6.1.7.1 PFD_DLY[2:0] — Phase Detector Delay

This word controls the minimum on time for the charge pump. The minimum setting often yields the best phase detector spurs and integer mode PLL phase noise. Higher settings may be useful in reducing the delta sigma noise of the modulator when dithering is enabled. These settings are not generally recommended if the phase detector frequency exceeds 130 MHz. If unsure, program this word to zero.

PFD_DLY	PULSE WIDTH	WHEN RECOMMENDED
0	370 ps	Default Use with a 2nd order modulator , when dithering is disabled, or when the phase detector frequency is >130 MHz.
1	760 ps	Consider these settings for a 3rd order modulator when dithering is used.
2	1130 ps	
3	1460 ps	
4	1770 ps	
5	2070 ps	
6	2350 ps	
7	2600 ps	

8.6.1.7.2 FL_FRCE — Force Fastlock Conditions

This bit forces the fastlock conditions on, provided that the FL_TOC word is greater than zero.

FL_FRCE	FASTLOCK TIMEOUT COUNTER	FASTLOCK
0	0	Disabled
	> 0	Fastlock engaged as long as timeout counter is counting down
1	0	Invalid State
	> 0	Always Engaged

8.6.1.7.3 FL_TOC[11:0] — Fastlock Timeout Counter

This word controls the timeout counter used for fastlock.

FL_TOC	FASTLOCK TIMEOUT COUNTER	COMMENTS
0	Disabled	Fastlock Disabled
1	2 x Reference Cycles	Fastlock engaged as long as timeout counter is counting down
2	2 x 2 x Reference cycles	
...		
4095	2 x 4095 x Reference cycles	

Copyright © 2012–2014, Texas Instruments Incorporated

8.6.1.7.4 FL_CPG[4:0] — Fastlock Charge Pump Gain

This word determines the charge pump current that is active during fastlock.

FL_CPG	FASTLOCK CURRENT STATE
0	TRI-STATE
1	1X
2	2X
..	...
31	31X

8.6.1.7.5 CPG_BLEED[5:0]

The CPG bleed word is for advanced users who want to get the lowest possible integer boundary spur. The impact of this word is on the order of 2 dB. For users who do not care about this, the recommendation is to default this word to zero.

USER TYPE	FRAC_ORDER	CPG	CPG BLEED RECOMMENDATION
Basic User	X	X	0
Advanced User	< 2	X	0
	X	< 4X	0
	>1	4X ≤ CPG < 12X	2
		12X ≤ CPG	4

Copyright © 2012–2014, Texas Instruments Incorporated