

# Building a Differential Amplifier using 180nm CMOS Technology

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## Project Overview

- **Duration:** 2 Months (Feb-March)
  - **Project Mentors:** P N Aneesh Bharadwaj, Chinmay G S
  - **Team Members:** Surya Srinivas, P N Aneesh Bharadwaj, Chinmay G S
  - **Project Poster:**  
<https://drive.google.com/file/d/1nCpuzw9jsSBJGyWukiFfKqpANS5z2NPo/view>
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## 1. Introduction

### 1.0 Abbreviations

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PUN	Pull Up Network
PDN	Pull Down Network
DA	Differential Amplifier
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
AC	Alternating Current
LSM	Large Signal Model
SSM	Small Signal Model
IC	Integrated Circuit
PMOS	P-channel MOS
NMOS	N-channel MOS

## 1.1 Project Statement

This project involves the design and simulation of a differential amplifier using 180nm CMOS technology. Differential amplifiers are fundamental building blocks in analog circuit design due to their high gain, common-mode noise rejection, and improved signal-to-noise ratio. The objective of this simulation is to analyze the amplifier's performance parameters, such as gain, bandwidth, power consumption, and input/output noise characteristics, in a submicron process technology. Using a 180nm CMOS process allows for a balance between performance, power efficiency, and integration density, making it suitable for modern analog/mixed-signal applications

## 1.2 Background Survey

*A brief overview of key concepts, prior research, or technologies related to the project.*

Before formally starting the designing and scripting of the Differential Amplifier on NGSpice, the following concepts were studied extensively:

- a. MOSFETs - this included ground up study from the related semiconductor physics, biasing technologies and configurations, Large (LSM) and Small Signal Models (SSM), drain current - gate voltage plots, drain current - drain voltage plots, channel length modulation, pinch-off effect, as well as applications, most notably the Differential Pair.
- b. CMOS realization of logic gates - Using PMOS and NMOS transistors to realize logic gates helped form a clear understanding of MOSFET working under ON and OFF states.
- c. Differential Amplifier characteristics - this included the definition of a differential signal, DA configurations with both resistive and active loads, and a comparison of their tradeoffs in gain and power consumption.
- d. Introduction to NGSpice - learning to write netlists, run transient analyses, DC and AC sweeps.

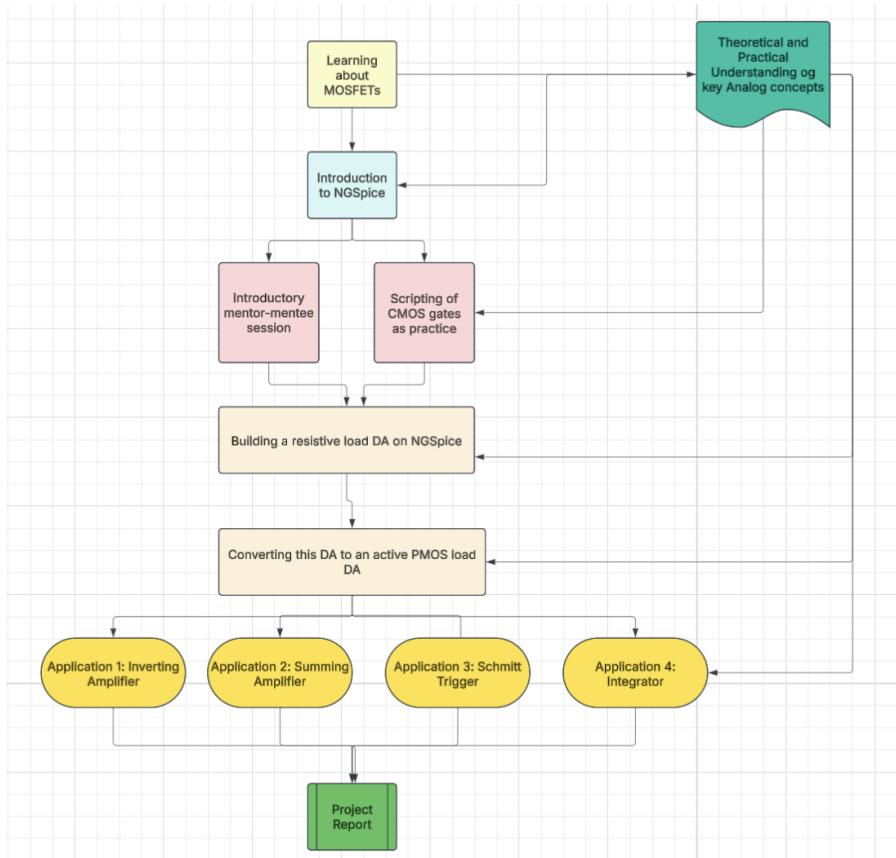
## 2. Methodology

### 2.1 Techniques & Approach

In order to run NGSpice simulations, we had to install a WSL (Windows Subsystem for Linux) via Ubuntu 20.04, and further connect VcXsrv (An open source Windows X-server) to view output plots. All netlisting pertinent to the project was done on Notepad, and run on NGSpice as

.txt files. The members chose to run either transient analyses or sweeps depending on the circuit being built and its application.

## 2.2 System Architecture & Workflow



CMOS Models Used:

### Level 1 model

```

.MODEL RITSUBN1 NMOS (LEVEL=1
+VTO=1.0 LAMBDA= 0.031 PB=0.95 CGSO=3.4E-10 CGDO=3.4E-10
+CGBO=5.75E-10 RSH=1082 CJ=6.8e-4 MJ=0.5 CJSW=1.26e-10
+MJSW=0.5 JS=3.23e-8 TOX=150E-10 NSUB=1.45e17 NSS=3E11
+TPG=+1 XJ=0.18U LD=0.15U UO=363)
*

```

\*2-15-2009

```
.MODEL RITSUBP1 PMOS (LEVEL=1
```

```
+VTO=-1.0 LAMBDA= 0.05 PB=0.94 CGSO=5.08E-10 CGDO=5.08E-10
+CGBO=5.75E-10 RSH=33.7 CJ=5.01e-4 MJ=0.5 CJSW=1.38e-10
+MJSW=0.5 JS=6.43e-8 TOX=150E-10 NSUB=7.23e16 NSS=1E11
+TPG=-1 XJ=0.28U LD=0.22U UO=463)
```

### **Level 3 model**

```
* DATE: Jun 11/01
* LOT: T14Y           WAF: 03
* DIE: N_Area_Fring   DEV: N3740/10
* Temp= 27

.MODEL CMOSN NMOS (          LEVEL = 3
+ TOX  = 5.7E-9      NSUB  = 1E17      GAMMA = 0.4317311
+ PHI  = 0.7        VTO   = 0.4238252    DELTA = 0
+ UO   = 425.6466519  ETA   = 0        THETA = 0.1754054
+ KP   = 2.501048E-4  VMAX  = 8.287851E4   KAPPA = 0.1686779
+ RSH  = 4.062439E-3  NFS   = 1E12       TPG   = 1
+ XJ   = 3E-7        LD    = 3.162278E-11  WD    = 1.232881E-8
+ CGDO = 6.2E-10     CGSO  = 6.2E-10     CGBO  = 1E-10
+ CJ   = 1.81211E-3   PB    = 0.5        MJ    = 0.3282553
+ CJSW = 5.341337E-10 MJSW  = 0.5      )

.MODEL CMOSP PMOS (          LEVEL = 3
+ TOX  = 5.7E-9      NSUB  = 1E17      GAMMA = 0.6348369
+ PHI  = 0.7        VTO   = -0.5536085    DELTA = 0
+ UO   = 250         ETA   = 0        THETA = 0.1573195
+ KP   = 5.194153E-5  VMAX  = 2.295325E5   KAPPA = 0.7448494
+ RSH  = 30.0776952   NFS   = 1E12       TPG   = -1
+ XJ   = 2E-7        LD    = 9.968346E-13  WD    = 5.475113E-9
+ CGDO = 6.66E-10     CGSO  = 6.66E-10     CGBO  = 1E-10
+ CJ   = 1.893569E-3   PB    = 0.9906013   MJ    = 0.4664287
+ CJSW = 3.625544E-10 MJSW  = 0.5      )
*
```

*The process:*

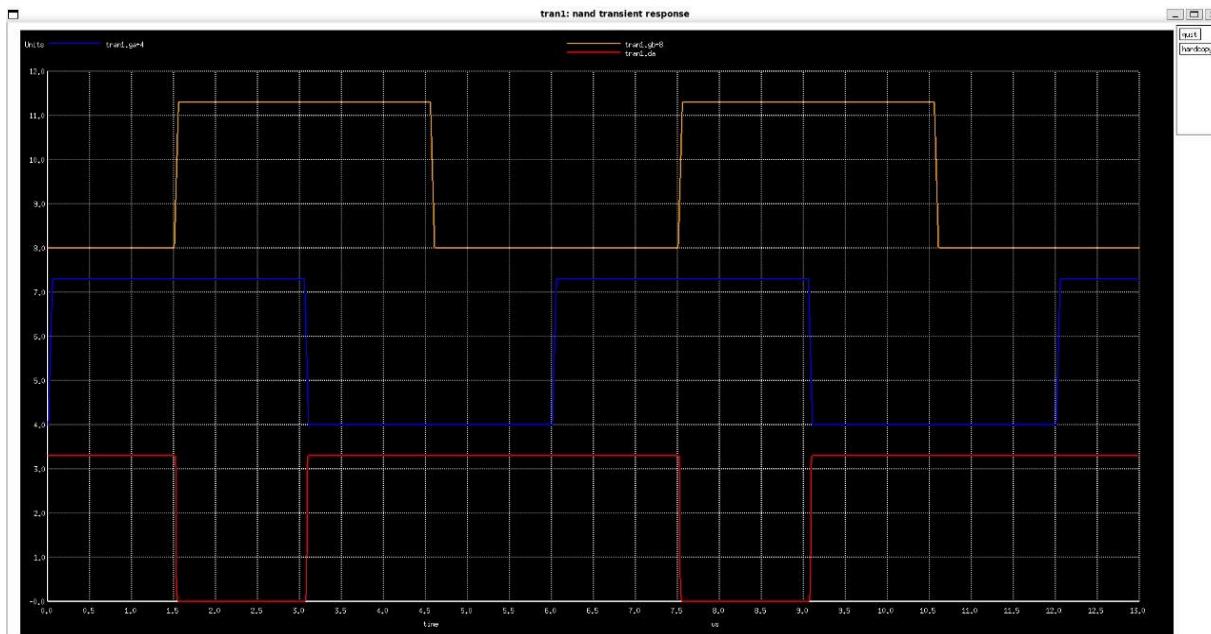
#### **Phase I - The learning phase**

This phase of the project was key in equipping the mentee with extensive knowledge on MOSFET physics, biasing techniques, non-idealities, applications and more. Fundamental concepts such as drain current - gate/drain voltage dependencies, input and output resistances, transconductance, intrinsic gain and its dependencies were learnt via this 1-month process. A vast majority of Phase I was accomplished through Behzad Razavi's lectures, and his textbook on Analog CMOS ICs.

## Phase II - Introduction to NGSpice - netlisting and simulation

Mentors held a session to introduce the mentee to the software. A CMOS Inverter gate (NOT gate) with resistive PUN was built as an example. Further the mentee built a NAND Gate along the same lines. All circuits henceforth were built using the Level 3 model.

*Fig 1.1 Transient Response of NAND Gate*



## Phase III and IV - Designing the DA, and its applications

A simple DA was first netlisted using resistive load with the following parameters:

1. NMOS w/l = 5u/1u
2. PMOS w/l = 5u/1u
3. Source Voltage vdd = 3.3 VDC
4. Load resistors = 20k
5. 150mV peak sine differential input

The script for the same follows:

[da1.txt](#)

```
*differential amplifier
.include ./t14y_tsmc_025_level3.txt
m1 d1 g1 s1 0 cmosn w=5u l=1u
m2 d2 g2 s1 0 cmosn w=5u l=1u
```

```

r1 vdd d1 20k
r2 vdd d2 20k
i1 s1 0 dc 100u ac 1u
*voltage sources
v_dd vdd 0 3.3
v_in1 g1 0 sin(0 150m 1meg 0 0 0)
v_in2 g2 0 sin(0 150m 1meg 0 0 180)
*transient response
.control
tran 0.01u 2u
plot tran1.d1 tran1.d2 tran1.g1 tran1.g2 title 'transient response'
.endc
.end

```

Next, the DA was built using active PMOS load by simply replacing the load resistors with P-channel MOSFETS. The ratio of nmos width to pmos width was set in accordance to mobility ratios.

Once the DA was found to be giving expected gain and stable levels (all relevant details and plots are discussed in section 3), we moved on the use the newly built DA in popular circuit applications (opamp applications):

### a. Summing Amplifier

Script:

```

*summing amplifier using DA (PMOS current mirror (active) load)
.include ./t14y_tsmc_025_level3.txt
m1 d1 g1 s1 0 cmosn w=240u l=0.18u
m2 d2 g2 s1 0 cmosn w=240u l=0.18u
m3 d1 d1 vdd vdd cmosp w=120u l=0.18u
m4 d2 d1 vdd vdd cmosp w=120u l=0.18u
iss vx 0 4m
*voltage sources
v_dd vdd 0 12
v_in1 n1 0 100m sin(0 1 2meg 0 0)
v_in2 n2 0 100m sin(0 2 2meg 0 0)
v_in3 n3 0 100m sin(0 3 2meg 0 0)
v_ref g1 0 0

*summing resistors

rs1 n1 g2 1k
rs2 n2 g2 1k

```

```

rs3 n3 g2 1k
rf d2 g2 20k

v_ids1 s1 vx 0
v_ids2 s2 vx 0

```

```

*transient response
.control
tran 0.1n 2u
let vout_tran = d2
plot vout_tran n1 n2 n3 title 'transient response'
.endc
.end

```

### **b. Schmitt Trigger**

Script:

```

* schmitt_trigger
.include ./t14y_tsmc_025_level3.txt

m1 vad vpos vx -12 cmosn w=120u l=0.18u
m2 vout vneg vx -12 cmosn w=120u l=0.18u
m3 vad vad vdd vdd cmosp w=180u l=0.18u
m4 vout vad vdd vdd cmosp w=180u l=0.18u
r1 vout vpos 1k
r2 vpos vj 1k

```

```

v_dd vdd 0 12
i_ss vx vg 4m
v_g vg 0 -12
v_in vneg 0 6 PULSE(-6 6 0 0 0 30u 60u)
v_ref vj 0 2

```

```

.control
tran 0.1n 160u

plot tran1.vout tran1.vj tran1.vneg tran1.vpos title 'Gain'
.endc
.end

```

### **c. Integrator**

```

* Integrator
.include ./t14y_tsmc_025_level3.txt

m1 vad v+ vx -12 cmosn w=120u l=0.18u
m2 vout v- vx -12 cmosn w=120u l=0.18u
m3 vad vad vdd vdd cmosp w=180u l=0.18u
m4 vout vad vdd vdd cmosp w=180u l=0.18u
rf v- vout 10k
c1 v- vout 1n
r2 v- vr1 1k

```

```

v_dd vdd 0 12
v_1 v+ 0 0
i_ss vx vg 4m
v_g vg 0 -12
v_in vr1 0 4 PULSE(-4 4 1n 0 0 0.5u 1u)

```

```

.control
tran 0.1n 50u
plot tran1.vr1 tran1.vout title 'Gain'
.endc
.end

```

#### d. Inverting Amplifier (IA)

```

* IA
.include ./t14y_tsmc_025_level3.txt

m1 vad v+ vx -12 cmosn w=120u l=0.18u
m2 vout v- vx -12 cmosn w=120u l=0.18u
m3 vad vad vdd vdd cmosp w=240u l=0.18u
m4 vout vad vdd vdd cmosp w=240u l=0.18u
r1 v- vout 3k
r2 v- vr1 1k
r3 v- vr2 2k
v_dd vdd 0 12
v_1 v+ 0 0
v_a vr1 0 1 SIN(0 1 2Meg 0 0)
v_b vr2 0 1 SIN(0 1 2Meg 0 0)
i_ss vx vg 3m
v_g vg 0 -12

```

```
.control
```

```

tran 0.1n 18u
plot tran1.vr1 tran1.vr2 tran1.vout title 'Gain'
.endc
.control
tran 0.1n 18u

plot vout vs vr1 title 'tf1'
plot vout vs vr2 title 'tf2'
.endc
.end

```

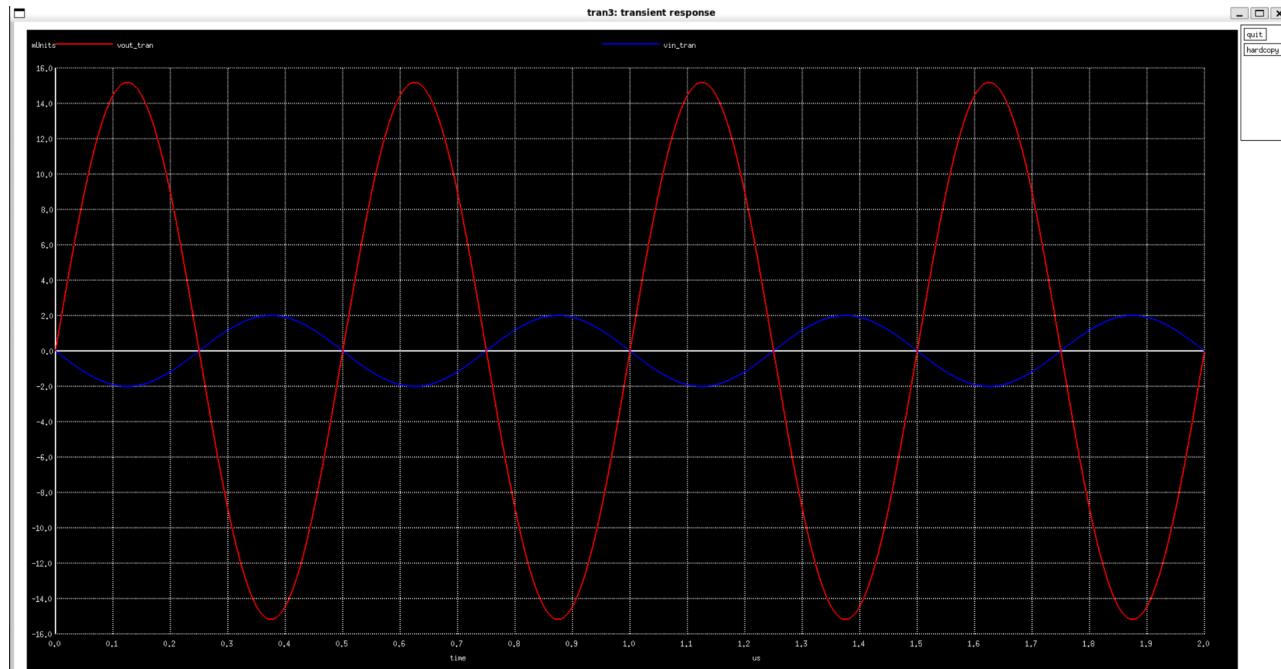
## 2.3 Tools & Technologies Used

- **Software:** NGSpice
- **Hardware:** NA

## 3. Results & Analysis

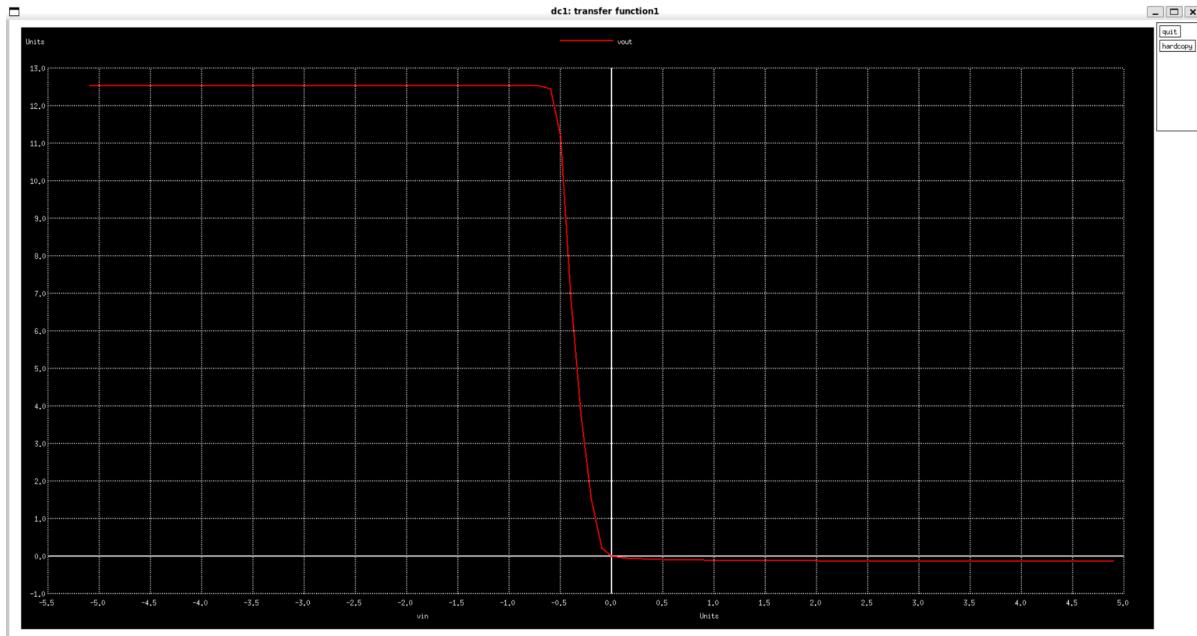
### A. Basic Differential Amplifier

*Fig 1.2 Basic DA Transient Response*



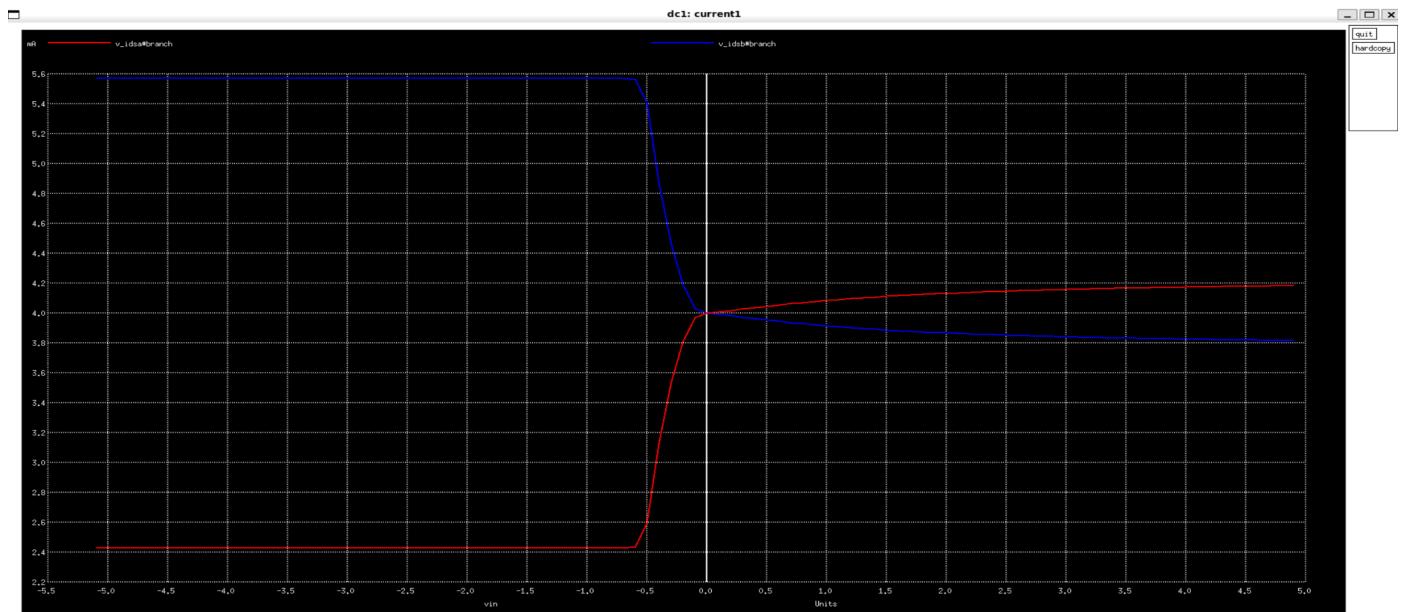
$$\text{Gain observed} = 15.6/2 = 7.8$$

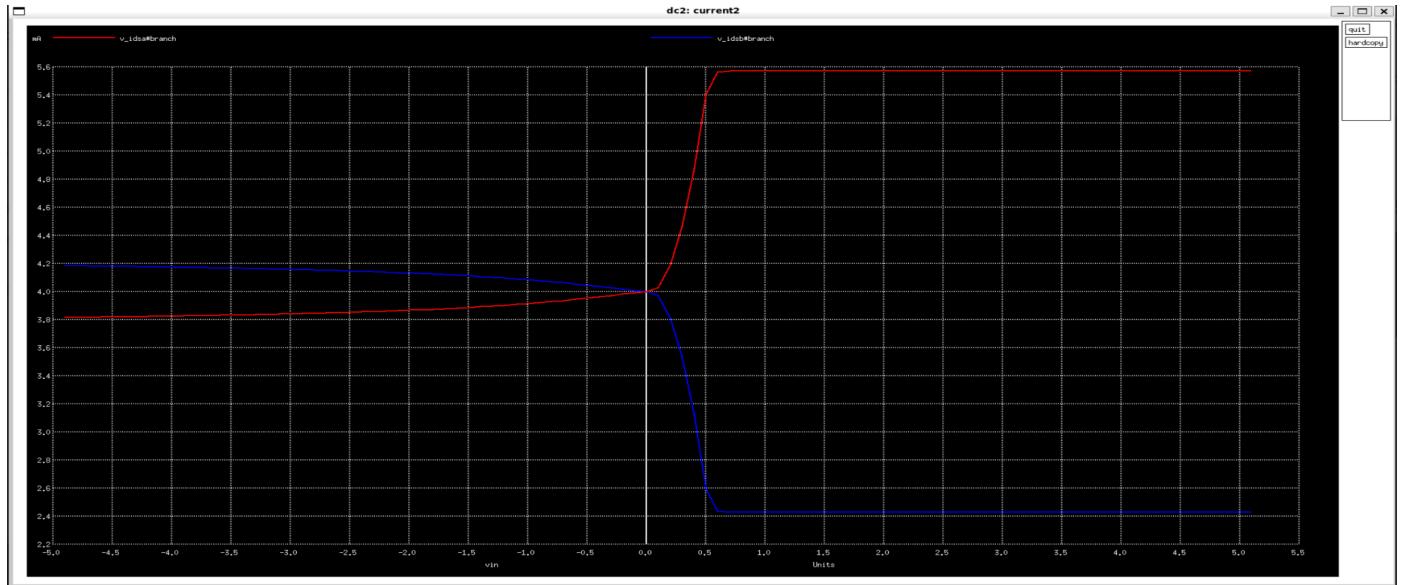
Fig 1.3 Basic DA Transfer Function



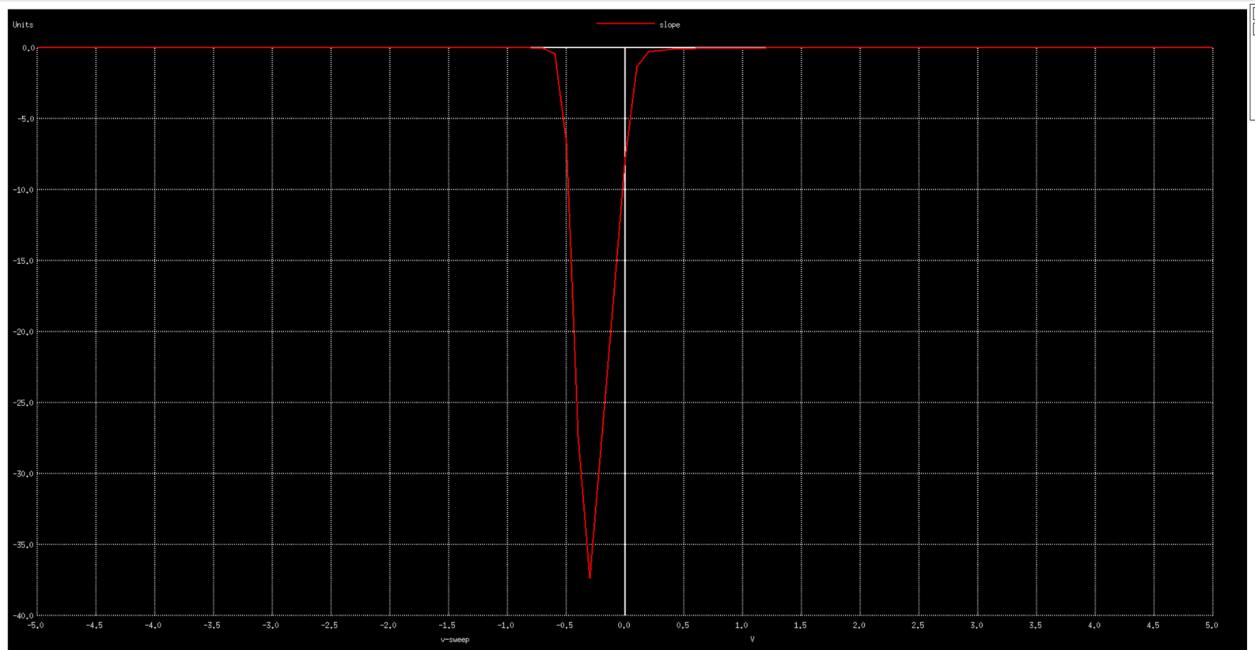
The transfer function  $V_{out}/V_{in}$  shows the expected behaviour: linear region in the middle, with saturation at the extremes. The DA is always operated in the linear region, where it provides a nearly constant gain.

Fig 1.4 Drain currents  $Id1$  and  $Id2$





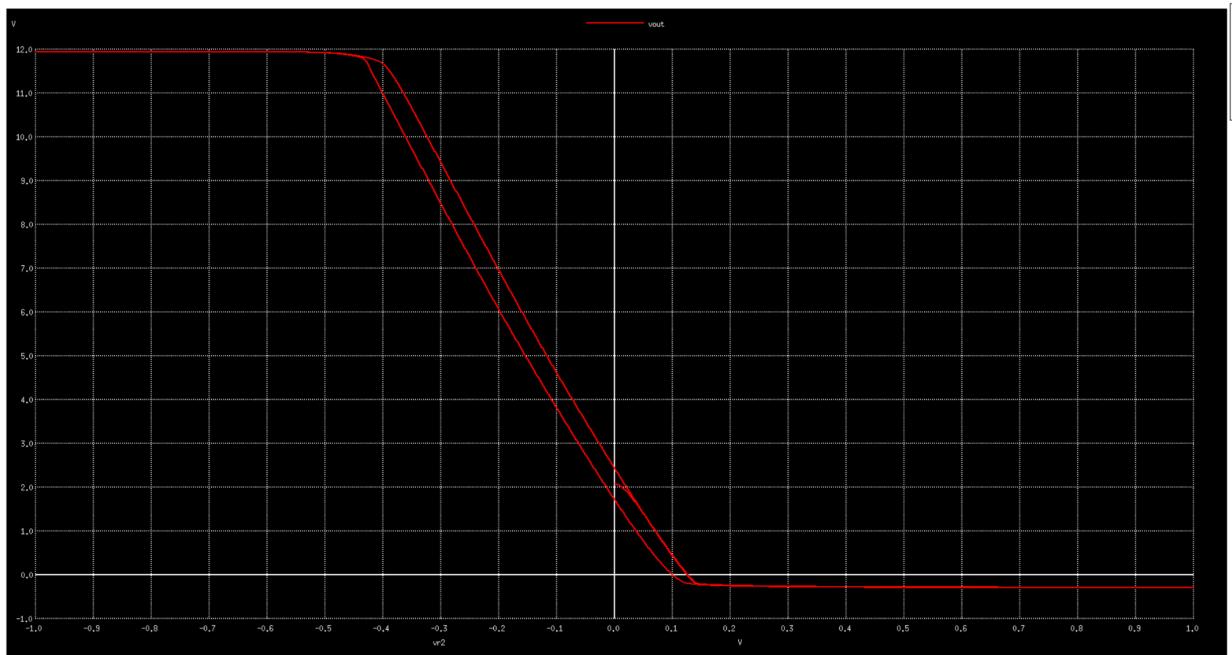
*Fig 1.5 Slope of Transfer Function (basic DA)*



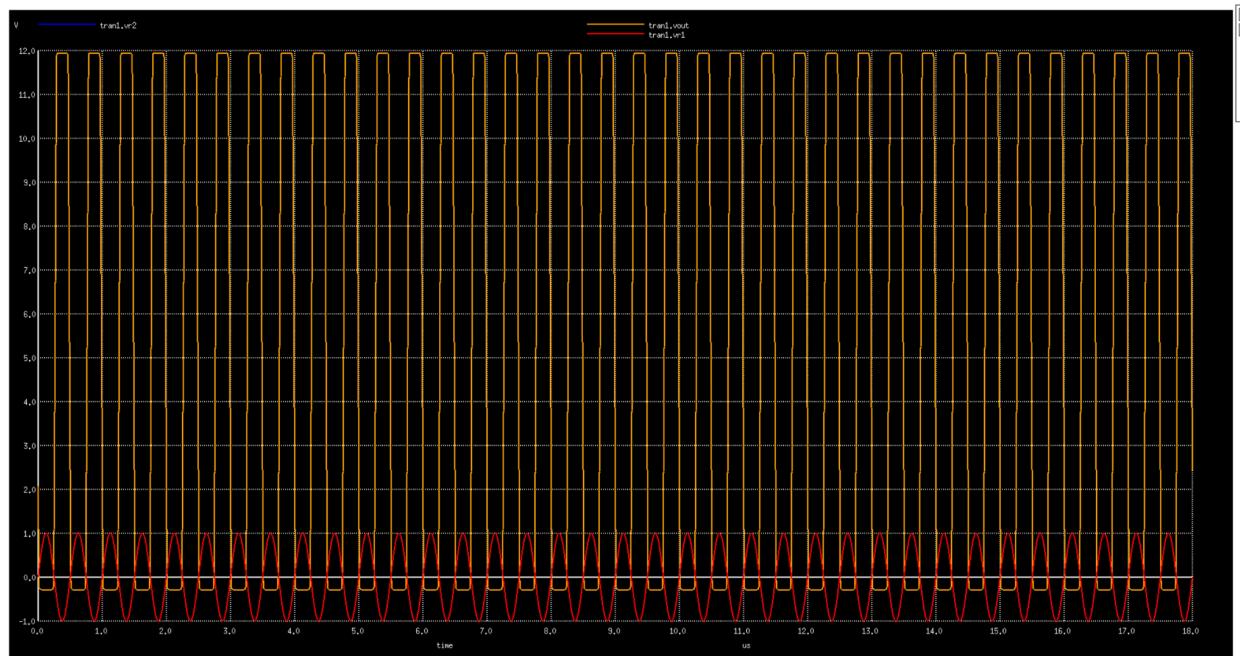
As expected there is a negative spike in the slope at linear region, and slope is zero in saturation.

## B. Inverting Amplifier

*Fig 1.6 Transfer function of inverting amplifier (saturating)*

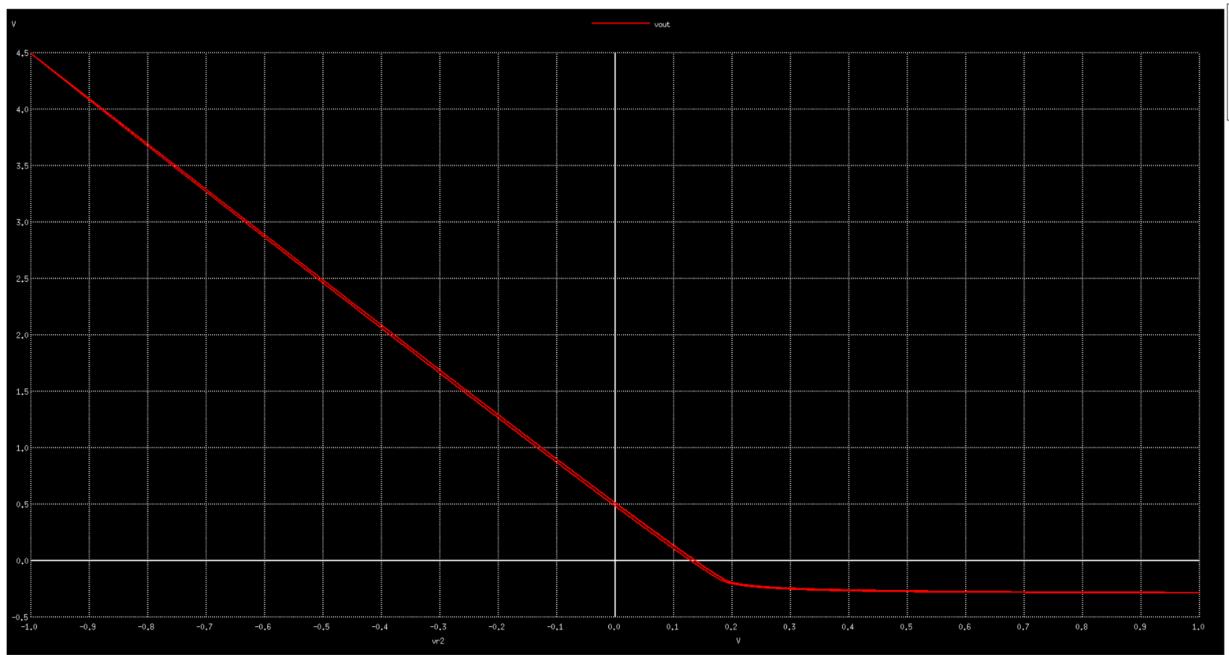


*Fig 1.7 Transient response of inverting amplifier (saturating)*

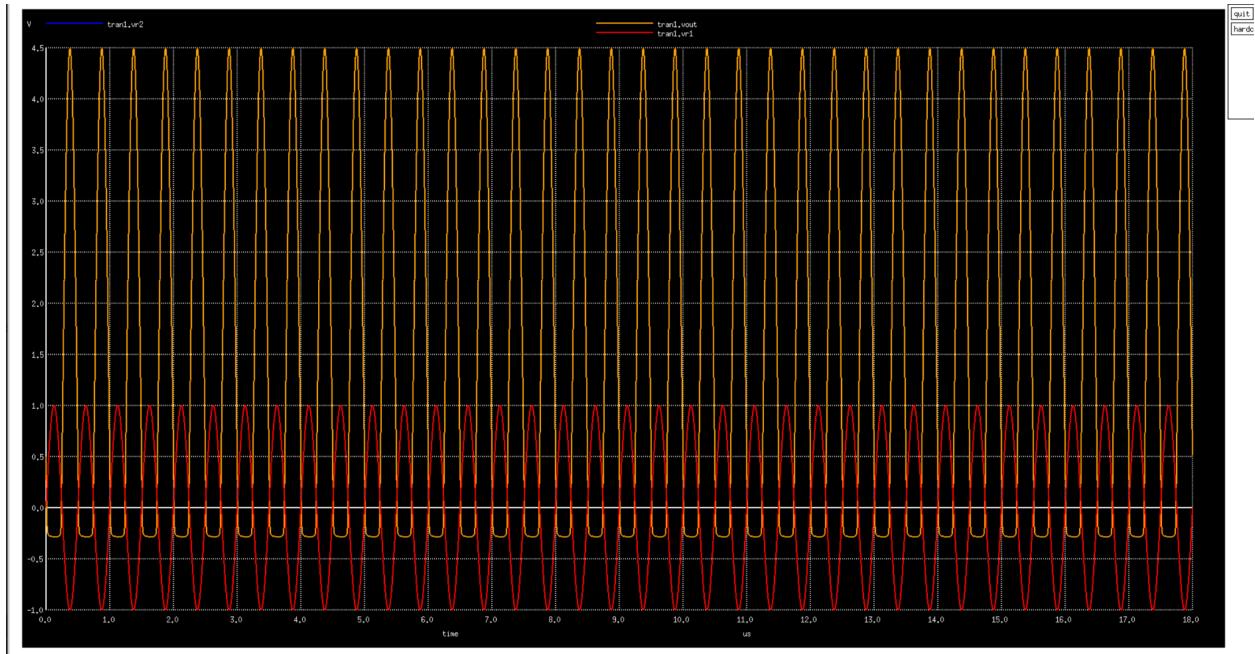


As is typical to saturation, the transient output voltage is clipped off at supply voltage = 12V.

*Fig 1.8 Transfer function of inverting amplifier (non-saturating)*



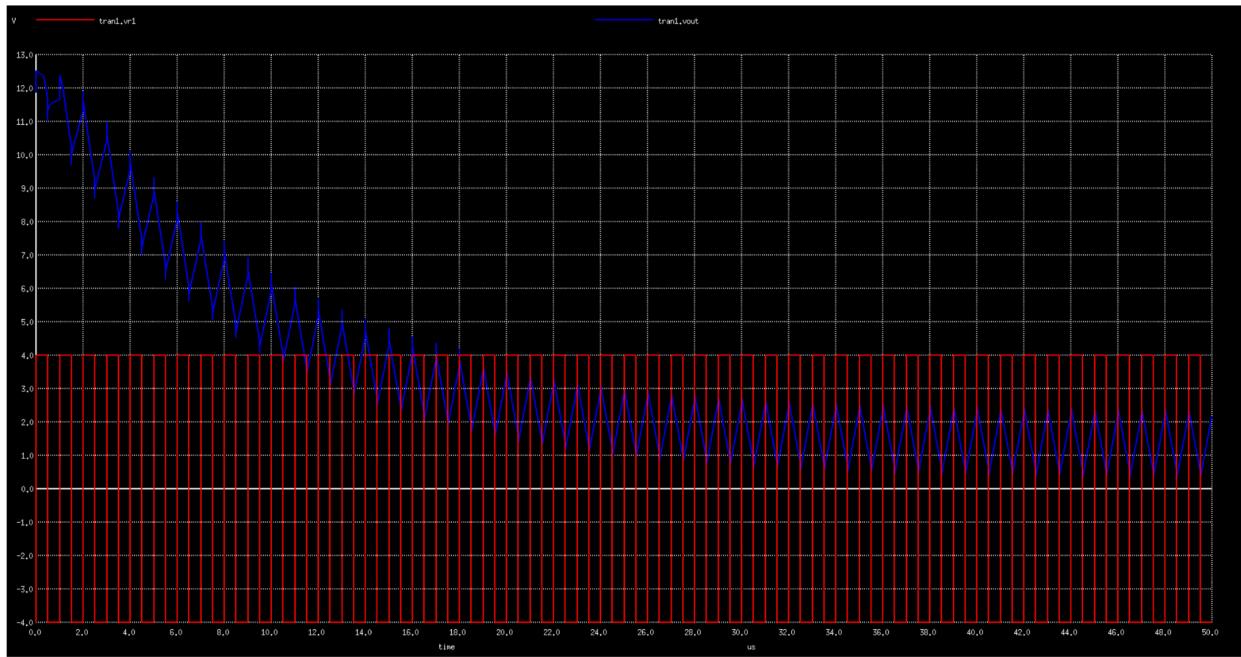
*Fig 1.9 Transient response of inverting amplifier (non saturating)*



Key observation: both the transient plots show a 180 degree phase shift between the output and input voltages, and also the output voltage is a scaled version of the input [ $V_o = -R_f/R_1 * V_{in}$ ]

### C. Integrator

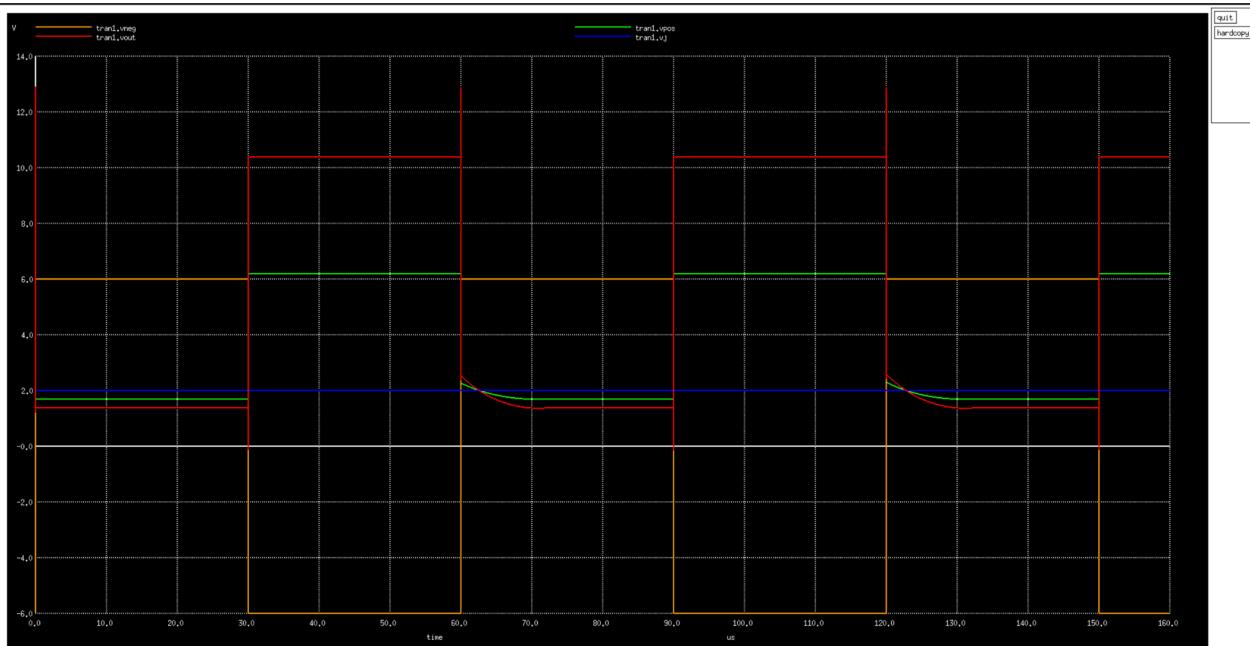
Fig 1.10 Integrator transient response



An integrator circuit produces the time integral of the input wave. Here the input wave (in red) is a -4V to 4V peak pulse wave of 1MHz frequency. Subsequently the output wave (in blue) is a triangular wave (which is the integral of a pulse)

### D. Schmitt Trigger

Fig 1.11 Schmitt Trigger transient response



*Vout - red, Vpos - green, Vneg - orange, Vref - blue*

*Observations from the Schmitt Trigger:*

- When  $V_{pos} > V_{neg}$ ,  $V_{out}$  is HIGH (ideally it should settle at 12V, however owing to real-life non-idealities, it settles at a value close to  $V_{dd}$ , here  $\sim 10.4V$ )
  - When  $V_{neg} > V_{pos}$ ,  $V_{out}$  is LOW. It settles at approximately  $V_{ref} = 0.2V$  (see script)
- 

## 4. Challenges & Learnings

### Obstacles Faced

*Logistic Challenges:*

- Having to reconfigure the VcXsrv server every time the project was reopened, this involved running a script in Ubuntu and re-launching Xlaunch.

*Technical Challenges:*

- Setting input wave frequency, keeping in mind the gain of the circuit, transient response duration, and especially the reference number in the simulator.
- Since NGSpice does not have a virtual building environment like LTSpice, naming nodes, components and sources legitimately and ensuring their connections are implicitly defined by virtue of node names itself (we do not ‘connect wires’ from node to node as in other softwares, the wiring is done by node naming)
- By far the biggest challenge was setting proper width and length values for the nmos and pmos transistors. We had to keep in mind their mobilities (as mentioned in the Level 3 model) , also the ratio w/l varies in accordance to the circuit we are building, hence there was a considerable amount of a mixture of trial and error, and theory knowledge involved in setting suitable w and l values.

### Solutions & Insights

- The above challenges and the roadblocks caused by them over the course of two months were effectively mitigated by revisiting notes, guidance from mentors and parallel reading from different resources.
  - Usage of AI in setting up the X server, and to some extent, in fixing w/l values.
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## 5. Conclusion & Applications

### ***Final Takeaways:***

A Differential Amplifier was successfully built and simulated on NGSpice. The project members thereby gained a deep understanding of MOS transistors, Differential Pair operation, biasing, netlisting and parameter fixing for ideal operation. We were exposed to the numerous intricacies of semiconductors, and how vastly they vary in both operation and simplicity to passive circuit elements.

### ***Real World Use Cases and Impact:***

The DA built can be extensively employed in place of an opamp for numerous circuit applications, three of which have been demonstrated in the project (Summing Amplifier, Integrator and Schmitt trigger), we can further build the following (not limited to):

- a. Opamp based oscillator
- b. Differentiator
- c. Buffer
- d. Filters (High pass, low pass, bandpass, allpass)

DAs are commonly used as input stages in Op-amps.

We can also use the DA in:

- a. Analog to Digital Converters (ADCs)
- b. Instrumentation Amplifiers
- c. RF (Radio Frequency) Communication Circuits
- d. Line Receivers
- e. Phase Locked Loops (PLLs)

### ***Benefits and Beneficiaries:***

This project benefits anyone with a deep interest in Analog electronics, MOS transistor physics, Operational Amplifiers, and a general intrigue in foundational small signal / mixed signal analog applications.

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## **6. Future Work & Enhancements**

There are numerous ways we can build upon the current project, key ones are listed as follows:

- a. Constructing more complex DA/Opamp applications such as oscillators, reviewing their transient responses and comparing with ideal case
- b. Calculating the maximum theoretical gain a DA can provide, and then verifying the same on simulation, with heed to level 3 model being employed
- c. Layout Level Implementation on Magic VLSI.
- d. Hardware implementation of the basic DA.

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## 7. References

1. Electronics 1 and 2 (until Frequency Response) - Behzad Razavi (Long Kong)  
[\[https://www.youtube.com/playlist?list=PLyYrySVqmyVPzvVIPW-TTzHhNWg1J\\_0LU\]](https://www.youtube.com/playlist?list=PLyYrySVqmyVPzvVIPW-TTzHhNWg1J_0LU)
  2. Design of Analog CMOS Integrated Circuits - Behzad Razavi
  3. NGSpice Users Manual - Paolo Nenzi, Holger Vogt
  4. <https://www.geeksforgeeks.org/cmos-logic-gate/>
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