Getting started with STM32MP13x lines hardware development

Introduction

This application note shows how to use the STM32MP13x microprocessors (MPUs). It describes the minimum hardware resources required to develop an application based on these products.

This document provides an overview of the hardware implementation of the development board. It focuses on the following features: power supply, package selection, clock management, reset control, Boot mode settings and debug management.

Reference design schematics are also included in this application note. They include the description of the main components, interfaces, and modes.

Table 1. Applicable products

Type	Product lines
Microcontrollers	STM32MP131, STM32MP133, STM32MP135

1 General information

This document applies to STM32MP13x Arm®-based MPUs.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

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Table 2. Reference documents

-	Reference	Title
[1]	AN2867	Oscillator design guide for STM8AF/AL/S, STM32 MCUs, and MPUs
[2]	AN1709	EMC design guide for STM8, STM32, and legacy MCUs
[3]	AN5105	Getting started with touch-sensing control on STM32 microcontrollers
[4]	AN4316	Tuning a touch-sensing application on MCUs
[5]	AN5275	USB DFU/USART protocols used in STM32MP1 Series bootloaders
[6]	AN5168	DDR configuration on STM32MP1 Series MPUs
[7]	AN5587	STM32MP13x lines and STPMIC1 integration on a wall-adapter supply
[8]	AN5592	STM32MP13x lines DDR memory routing guidelines
[9]	AN5585	STM32MP13x lines and STPMIC1 integration on a battery-powered application
[10]	AN5586	STM32MP13x lines discrete power supply hardware integration
[11]	AN4879	USB hardware and PCB guidelines using STM32 MCUs
[12]	UM2993	STM32MP135F-DK discovery board user manual
[13]	RM0475	STM32MP13x advanced Arm-based 32-bit MPUs
[14]	DSXXXX	STM32MP13xA/Dxx datasheet
[15]	DSXXXX	STM32MP13xC/Fxx datasheet
[16]	ES0539	STM32MP131x STM32MP133x STM32MP135x errata sheet

Table 3. Glossary

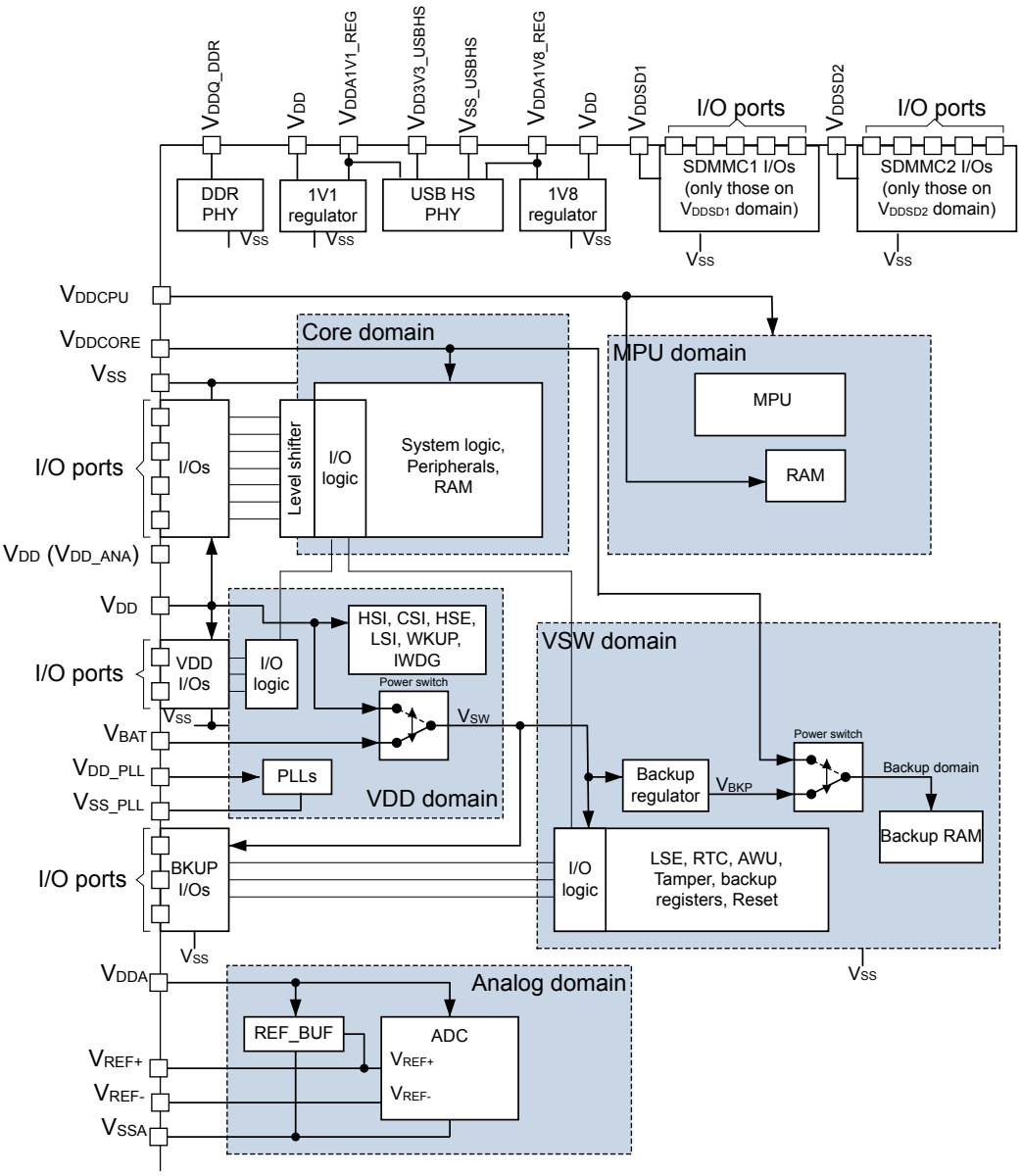
Acronym	Description
ADC	Analog to digital converter
AHB	Advanced high-performance bus
AXI	Advanced extensible interface (by extension, interconnect matrix based on AXI)
AXIM	AXI matrix (AXI-based interconnect)
AXIMC	AXI matrix configuration control
BKPSRAM	Backup SRAM
BSEC	Boot and security controller (OTP interface)
CEC	Consumer electronics control (part of HDMI standard)
CNT	Generic timer (inside Cortex®-A7)
CRYP	Cryptographic peripheral, supporting DES, triple-DES, and AES
CSI	Low-power internal oscillator
CTI	Cross-trigger interface
DAP	Debug access port
DCMI	Digital camera interface (parallel interface)
DDRCTRL	Double data rate SDRAM controller, supporting LPDDR2, and DDR3/DDR3L protocols

Acronym	Description
DDRPERFM	DDR performance monitor, linked to DDRCTRL
DDRPHYC	DDR physical interface control
DFSDM	Digital filter for sigma-delta modulators
DLYBQS	Delay block for QUASDPI, compensating external signals timings to reach highest data rates
DLYBSD	Delay block for SDMMC, compensating external signals timings to reach highest data rates
DMA	Direct memory access: bus master able to transfer data between peripheral and memory, or between memories, in an autonomous way
DMAMUX	DMA request multiplexer
ETH	Ethernet controller
ETM	Embedded Trace Macrocell™
ETZPC	Enhanced TrustZone® protection controller, used to configure some peripherals and ROM/RAM protection settings
EXTI	Extended interrupt and event controller
FDCAN	Controller area network with flexible data-rate (can also support time-triggered CAN (TT))
FMC	Flexible memory controller
GIC	Generic interrupt controller
GMAC	Gigabit Ethernet media access controller
GPIO	General-purpose input output
GPU	Graphic processing unit
HASH	Cryptographic hash peripheral, supporting secure hash algorithm (SHA)
HDMI	High-definition multimedia interface
HDP	Hardware debug port
HSE	High-speed external quartz oscillator
HSEM	Hardware semaphore, helping multiprocessor resources sharing
HSI	High-speed internal oscillator
I2C	Inter-integrated circuit interface
I2S	Inter-integrated circuit sound
IPCC	Interprocessor communication controller
IWDG	Independent watchdog
JTAG	Joint test action group (debug interface)
LCD	Liquid crystal display
LPTIM	Low-power timer
LSE	Low-speed external quartz oscillator
LSI	Low-speed internal oscillator
LTDC	LDC TFT display controller
MDIOS	Management data input/output slave, used to control Ethernet physical interface
MDMA	Master DMA
MLAHB	Multilayer AHB (AHB-based interconnect)
OTG	USB On-The-Go, standard USB interface, able to become host or device
OTP	One-time program memory
PMB	Process monitor block

Acronym	Description
PMIC	External power-management circuit that provides various platform power supplies, with large controllability through signals and serial interface
PWR	Power control
QUADSPI	Quad-data-lanes serial-peripheral interface
RCC	Reset and clock control
RNG	Random number generator
RMA	Return material analysis product life cycle state
ROM	Read-only memory
RTC	Real-time clock
SAI	Serial-audio interface
SDMMC	Secure digital and MultiMediaCard interface, supporting SD, MMC, e.MMC™, and SDIO protocols
SMPS	Switched-mode power supply
SPDIF	Sony/Philips digital interface format
SPI	Serial peripheral interface
SRAM	Static random access memory
STGEN	System timer generator, used for Cortex-A7 timers
STGENC	STGEN control: secure part of STGEN
STGENR	TGEN read: read-only part of STGEN
STM	System trace macrocell
SWD	Serial-wire debug
SWO	Single-wire output (trace port)
SYSCFG	System configuration
SYSRAM	System SRAM
TAMP	Tamper detection peripheral
TEMP	Temperature sensor
TFT	Thin-film transistor: LCD technology process
TIM	Timer
TSGEN	Debug time stamp generator, used to ensure multiple core traces synchronizations
TZC	TrustZone address space controller, used to protect access to external SDRAM
UART	Universal asynchronous receiver/transmitter
USART	Universal synchronous/asynchronous receiver/transmitter
USB	Universal serial bus
USBH	USB host controller
USBPHYC	USB physical interface control
VREFBUF	ADC voltage reference buffer
WWDG	Window watchdog

2 Power supplies

Figure 1. Power supply scheme



2.1 Overview

The main features of the STM32MP13x power supplies are listed below (details and guaranteed operating points in product datasheets):

- The main I/Os voltage supply (V_{DD}) range is 1.71 V to 3.6 V.
- The core logic-operating voltage supply (V_{DDCORE}) range is 1.21 V to 1.29 V.
- The MPU domain operating-voltage supply (V_{DDCPU}) range is:
  - 1.21 V to 1.38 V (OPP 650 MHz)
  - 1.32 V to 1.38 V (OPP 1000 MHz)
- The USB supplies (V_{DD3V3_USBHS}) range is 3.07 V to 3.6 V.
- Embedded regulators are used to supply some internal blocks:
  - 1.8 V LDO for USB available on VDDA1V8_REG, that is used to supply USB internally
    When BYPASS_REG1V8 = VDD, VDDA1V8_REG must be supplied externally. In that case, the range is 1.65 V to 1.95 V.
  - 1.1 V LDO for USB available on VDD1V1_REG for external decoupling
    Note: Embedded regulators must not be used to supply external components.
- The real-time clock (RTC) and backup registers can be powered from the V_{BAT} voltage when the main V_{DD} supply is powered off. This internal supply with automatic switch between V_{BAT} and V_{DD}, is named VSW domain. The VSW domain is also used to supply the PI3, PI2, PI1, PI0, PC13, PC14, PC15 pins.

Note: Because the analog switch can transfer only a limited amount of current (3 mA), the use of GPIO PI3, PI2, PI1, PI0, PC13, PC14, PC15 in output mode is restricted. The frequency has to be limited to 2 MHz, with a maximum load of 30 pF, and these I/Os must not be used as a current source (for instance to drive a LED).
V_{BAT} voltage range is 1.20 V to 3.6 V.
When V_{DD} is above V_{BAT}, a small charging current can be enabled on VBAT pin for an external backup voltage device (such as a super capacitor).

2.1.1 Independent ADC supply and reference voltage

To improve the conversion accuracy and dynamic range, the ADC and reference have an independent power supply that can be filtered separately. This power supply can be shielded from noise on the PCB.

The analog operating voltage supply (V_{DDA}) range is 1.71 V to 3.6 V:

- The ADC/VREFBUF voltage supply input is available on a separate VDDA pin.
- An isolated supply ground connection is provided on the VSSA pin.
  In all cases, the VSSA pin must be externally connected to the same supply ground than VSS.

External VREF

The user can connect a separate external reference voltage ADC input on the VREF+ pin. The voltage on VREF+ may range from 1.62 V to V_{DDA}.

Internal VREF

The user can enable, in the VREFBUF block, an internal reference voltage on VREF+.

The voltage on VREF+ can be selected between 1.5 V, 1.8 V, 2.048 V, and 2.5 V.

With internal V_{REF} available on the VREF+ pin, it can be used externally . It can be used for analog comparator reference for example, if the loading is kept within datasheet values.

The VREFBUF requires V_{DDA} equal to or higher than V_{REF+} + 0.3 V.

Caution: The VREF– pin must be externally tied to VSSA.

Booster for ADC analog input switches

The ADC inputs are multiplexed with analog switches that have reduced performances when V_{DDA} supply is below 2.7 V. In order to get maximum ADC analog performances, it is alternatively possible to supply analog switches with either:

- V_{DD}, if above 2.7 V
- an embedded 3.3 V booster from V_{DDA}.

The control is done in the SYSCFG_PMCR register, as shown in the table below.

Table 4. Recommended settings for ANASWVDD and EN_BOOSTER

V_{DDA} (V)	V_{DD} (V)	SYSCFG_PMCR.ANASWVDD	SYSCFG_PMCR.EN_BOOSTER	Switches supply	ADC analog performances
> 2.7	1.71 to 3.6	0	0	V_{DDA} (> 2.7 V)	Maximum
< 2.7	> 2.7	1	0	V_{DD} (> 2.7 V)	
	< 2.7	0	1(1)	Booster (~ 3.3 V)	
			0(2)	V_{DDA} (< 2.7 V)	Reduced

1. *Booster voltage can take up to 50 ms to stabilize.*
2. *If reduced ADC analog performance is acceptable, the booster disabled can save up to 250 mA.*

Supply decoupling recommendation

Supply V_{REF+} with an external low-noise reference is recommended.

If the internal VREFBUF is used to supply V_{REF+}, then it is recommended to use the below decoupling capacitances:

- between VREF+ and VREF-/VSSA pins: 1x 100 nF as close as possible and 1x 1 µF a bit further away
- between VDDA and VSSA pins: 1 x100 nF as close as possible and 1 x1 µF a bit further away

When only one capacitance can be used, it is recommended to keep the 1 µF and place it as close as possible to the VREF+ and VDDA pins.

If the V_{DDA} power supply is used as reference voltage V_{REF+}, then it is recommended to use the below decoupling capacitances:

- between VREF+/VDDA and VREF-/VSSA pins: 1x 100 nF as close as possible and 1x 1 µF a bit further away

When only one capacitance can be used, it is recommended to keep the 1 µF and place it as close as possible to the VREF+ and VDDA pins.

2.1.2 Independent I/O supply rail

External discrete level shifters are not needed when using SD-Cards in UHS-I mode by using the two sections of the I/Os. The IOs are supplied by independent V_{DDSD1} and V_{DDSD2} power supplies.

The I/Os supplied by independent V_{DDSD1} and V_{DDSD2} power supplies have some SDMMC signals. These signals are identified on the corresponding product's datasheet with the "VSD1" or "VSD2" suffix. VSD1 can be found on PC8, PC9, PC10, PC11, PC12, and PD2. VSD2 can be found on PB3, PB4, PB14, PB15, PE3, and PG6.

If no SD-Card is used on those I/Os, or if external level shifters are used, then V_{DDSD1} and V_{DDSD2} supplies can be connected to the V_{DD} power supply. Refer to Section 8.8 SD-Card without external level-shifters for more details.

The V_{DDSD1} or V_{DDSD2} power supply can be connected to V_{SS} if the two conditions below are met:

- no I/O is used on V_{DDSD1} or V_{DDSD2} I/Os section
- no other GPIO is > 3.6 V

Typically when a 5 V tolerant I/O has its input at 5 V, V_{DDSDx} cannot be disabled or cannot be below 1.4 V (5 V - 3.6 V).

It is possible during run time to power down V_{DDSD1} or V_{DDSD2} independently of the V_{DD} power level. In order to be able to do this, no other GPIO should be > 3.6. For example, a power cycle on SDMMC setting V_{DDSD1} to 0 is possible if

- V_{DDSD1} I/Os are used to connect on board SDMMC memory
- and if V_{DDSD1} is powered with on board SDMMC memory power-supply.

2.1.3 HSLV mode and compensation cells for GPIOs

HSLV (high-speed low voltage) mode is available for some GPIOs; this mode enables the possibility to increase the drive of the I/Os when 1.8 V is used.

The HSLV mode must be used only once the power supply of the I/Os is below 2.7 V, otherwise the device can suffer permanent damage.

The HSLVEN bits control the HSLV mode for the associated interface I/Os; this is done independently of the I/Os power supply. SYSCFG_HSLVEN4R and SYSCFG_HSLVEN5R control HSLV mode for all I/Os on SDMMC1 and SDMMC2 interfaces respectively. It includes the IOs powered by either V_{DD}, V_{DDSD1} or V_{DDSD2}.

HSLV mode is protected by the OTP bit (product_below_2V5) for I/Os powered by V_{DD}. In order to be able to use the HSLV mode, the OTP bit must be already fused. I/Os powered by V_{DDSD1} and V_{DDSD2} do not count on that type of protection.

Compensation cells are used to control the I/O commutation slew rate (tfall/trise). This is done to reduce the I/O noise on the power supply for a number of I/O pins. As compensation cells are related to power supplies, the following actions must be done:

- SYSCFG_CMPENSETR.EN must be programmed for I/Os powered by V_{DD}
- SYSCFG_CMPSD1ENSETR.EN must be programmed for I/Os powered by V_{SDDSD1}
- SYSCFG_CMPSD2ENSETR.EN must be programmed for I/Os powered by V_{SDDSD2}.

2.1.4 Battery backup

To retain the content of the backup registers and BKPSRAM, when V_{DD} is turned off, the VBAT pin can be connected to an optional standby voltage, supplied by a battery or another source.

The VBAT pin also powers the RTC, allowing it to operate even when the main digital supply (V_{DD}) is turned off. The switch to the V_{BAT} supply is controlled by the power-down reset (PDR) circuitry embedded in the reset block.

If no external battery is used in the application, it is required to connect VBAT externally to VDD.

2.1.5 Voltage regulators

The 1.8 V LDO (for USB) is always enabled after power-on reset if BYPASS_REG1V8 = V_{SS}. It is disabled on Standby entry and (LP/LPLV-) Stop does not affect it.

The 1.1 V LDO (for USB) is always enabled after power-on reset. It is disabled on Standby entry and (LP/LPLV-) Stop does not affect it.

The embedded regulators must not be used to supply external components (unless specifically mentioned).

2.2 Power supply schemes

The circuit is powered by the following power supplies:

- The V_{DD} is the main supply for I/Os. The internal part kept powered during the Standby mode. Useful voltage range is 1.71 V to 3.6 V (1.8 V, 2.5 V, 3.0 V, or 3.3 V typical).
  - Those supplies must be connected to external decoupling capacitors (see Table 5).
  - V_{DD_PLL} and V_{DD_ANA} must be connected to V_{DD}.
- The V_{DDSD1} and V_{DDSD2} are the dedicated power supplies for two independent I/Os sections. The voltage range is the same as V_{DD}.
  - Those supplies must be connected to external decoupling capacitors (see Table 5).

- The V_{DDCORE} is the digital core domain supply. It can be shut down externally during the Standby mode. Voltage range during Run mode is 1.21 V to 1.29 V (1.25 V typical).
  - This supply must be connected to external decoupling capacitors (see Table 5).
  - V_{DDCORE} can be reduced further in specific Stop mode (LPLV_Stop, LPLV_Stop2). This involves either:
    - PWR_ON signal: for example with STPMIC1, external power management circuit
    - PWR_LP signal with discrete SMPS components.
- The V_{DDCPU} is the MPU domain supply. It can be shut down externally during the Standby and LPLV-Stop2 mode. Voltage range is:
  - 1.21 V to 1.38 V (1.25 V typical) up to 650 MHz
  - 1.32 V to 1.38 V (1.35 typical) above 650 MHz.
  - This supply must be connected to external decoupling capacitors (see Table 5).
  - V_{DDCPU} can be reduced further in specific Stop mode (LPLV_Stop). This involves either:
    - PWR_ON signal with STPMIC1, external power management IC
    - PWR_CPU_ON and PWR_LP signal with discrete SMPS components
- The VBAT pin can be connected to the external battery (1.2 V < V_{BAT} < 3.6 V).
  - If the application does not support a backup battery, it is recommended to connect this pin to V_{DD}.
  - If the application supports a backup battery, it is recommended to add a ceramic decoupling capacitor between V_{BAT} and V_{SS}. Refer to Table 5.
  - If the application uses a super capacitor on VBAT, no additional decoupling is required.
- The VDDA pin is the analog (ADC/VREFBUF) supply and must be connected to external decoupling capacitors. Refer to Table 5.
- The VREF+ pin can be connected to the V_{DDA} external power supply. If a separate, internal, or external, reference voltage is applied on VREF+, a decoupling capacitor must be connected between this pin and VREF-. Refer to Table 5 and Section 2.1.1.
  Additional precautions can be taken to filter analog noise: VDDA can be connected to VDD through an inductor-based filter.
- V_{DDQ_DDR} is the DDR I/O supply and must be connected to external decoupling capacitors (seeTable 5).
  - Voltage range is 1.425 V to 1.575 V for interfacing DDR3 memories (1.5 V typical).
  - Voltage range is 1.283 V to 1.45 V for interfacing DDR3L memories (1.35 V typical).
  - Voltage range is 1.14 V to 1.3 V for interfacing LPDDR2 or LPDDR3 memories (1.2 V typical).
- V_{DD3V3_USBHS} is the USB high-speed PHY supply. Voltage range is 3.07 V to 3.6 V. It must be connected to external decoupling capacitors (see Table 5).
  V_{DD3V3_USBHS} is also used to supply OTG_VBUS (PI7) and OTG_ID (PA10) pins.
- The VDDA1V8_REG pin is the output of the internal regulator and must be connected to external decoupling capacitors. Refer to Table 5.
  - VDDA1V8_REG is connected internally to USB PHY and USB PLL.
  - The internal VDDA1V8_REG regulator is enabled by default and can be controlled by software. It is always shut down during Standby.

  For the 1.8 V voltage regulator configuration, there is a specific BYPASS_REG1V8 pin that must be connected either to V_{SS} or V_{DD} to activate or deactivate the voltage regulator. It is mandatory to bypass the 1.8 V regulator when V_{DD} is below 2.25 V:
  - When BYPASS_REG1V8 = VDD, the VDDA1V8_REG pin must be connected to V_{DD} (if below 1.98 V) or to a dedicated 1.65 V - 1.98 V supply (1.8 V typical).
  - When BYPASS_REG1V8 = VSS, V_{DD} must be above 2.25 V to allow correct behavior of the 1.8 V voltage regulator.

  Refer to Section 2.1.5 Voltage regulators and section "Embedded regulators characteristics" of the product datasheet for details.

- VDDA1V1_REG pin is the output of the internal regulator and must be connected to external decoupling capacitors. Refer to Table 5). The voltage range is 1.045 V to 1.155 V (1.1 V typical).
  - VDDA1V1_REG is connected internally to USB PHY.
  - The internal VDDA1V1_REG regulator is enabled by default and can be controlled by software. It is always shut down during Standby.

Caution: V_{DD3V3_USBHS} must not be present (unless VDDA1V8_REG is present), otherwise permanent device damage may occur. This is ensured by the STPMIC1 ranking order, or with an external component in case of a discrete component power supply implementation.

All supply grounds (V_{SS}, V_{SS_ANA}, V_{SS_PLL}, V_{SS_USBHS}, VSSA, and V_{REF-}) must be connected with power planes.

The table below can be used as a guideline. The real capacitor count and values can be adapted depending on various parameters (capacitor size, capacitor dielectric, PCB technology), and using the results of the product power integrity simulations.

Table 5. Decoupling recommendations by package

Supply pin	Decoupling point(1)	Value(2)	TFBGA289 (9 x 9)	TFBGA320 (11 x 1)	LFBGA289 (14 x 14)	Comments
VBAT	VSS	100 nF(3)	1	1	1	Can be skipped if VBAT is connected to VDD, or if a super capacitor is used instead of a battery.
VDDCORE	VSS	1 µF	8	8	8	Not including capacitors on PMIC/SMPS
VDDCPU	VSS	1 µF	7	7	7	Not including capacitors on PMIC/SMPS
VDDQ_DDR	VSS	1 nF	7	7	6	Not including capacitors on PMIC/SMPS and additional capacitors on DDR memory
		1 µF	3	3	3	
VDD_ANA	VSS_ANA	1 µF	1	1	1	-
VDD_PLL, VDD_PLL2	VSS_PLL, VSS_PLL2	1 µF	2	2	2	Not including capacitors on PMIC/SMPS
VDD	VSS	1 µF	4	4	4	
VDDSD1/VDDSD2	VSS	1 µF	1/1	1/1	1/1	
VDDA1V8_REG	VSS_USBHS	2.2 µF	1	1	1	-
VDDA1V1_REG						
VDD3V3_USBHS		1 µF				
VDD3V3_USB	VSS	1 µF				
VDDA	VSSA	100 nF + 1 µF	1+1	1+1	1+1	VSSA must be connected to VSS plane.
VREF+	VREF- and VSSA					VREF- must be connected to VSSA, then to the VSS plane.

1. *All VSS_X and VSSA must be connected to a common VSS plane.*
2. *All µF capacitors are MLCC (multilayer ceramic).*
3. *Rise time should be less than 33 us/V.*

Table 6. Supply usage for unused features

Supply	Usual connection	Possible connection	Pins or functions(1)	Related block
VDD3V3_USBHS	Dedicated 3.3 V supply	Open or VSS	USB_DP1/DM1 pins	USBH

Supply	Usual connection	Possible connection	Pins or functions(1)	Related block
VDD3V3_USBHS	Dedicated 3.3 V supply	Open or VSS	USB_DP2/DM2 pins	OTG or USBH
VDD3V3_USB	Dedicated 3.3 V supply	Open or VSS	USB_DP1/DM1 pins	USBH
			USB_DP1/DM1 pins	OTG or USBH
			PA10 pins as OTG_HS_ID	OTG
VDDA1V1_REG	Decoupling capacitor	Open	USB_DP1/DM1 pins	USBH
			USB_DP2/DM2 pins	OTG or USBH
VDDA1V8_REG	Decoupling capacitor or dedicated 1.8 V supply or VDD 1.8 V	Open	USB_DP1/DM1 pins	USBH
			USB_DP2/DM2 pins	OTG or USBH
VDDA	Dedicated supply or VDD	Open, VSS or VDD	ADC internal channels	ADC1/ADC2
			ADCx_INxx pins	ADC1/ADC2
			VREFBUF usage	VREFBUF
			VREF+ pin	ADC
VDDSD1	VDD or dedicated dynamic supply (3.3 V - 1.8 V) for SD-Card UHS-I mode	VDD	PC[12:8], PD[2] pins(2)	SDMMC1 and other AFmux functions
VDDSD2	VDD or dedicated dynamic supply (3.3 V - 1.8 V) for SD-Card UHS-I mode	VDD	PB[15, 14, 4, 3], PE3, PG6 pins (3)	SDMMC2 and other AFmux functions

1. *Possible connection only when all related pins/functions are not used.*
2. *When these pins are not used, VDDSD1 must be connected to VDD.*
3. *When these pins are not used, VDDSD2 must be connected to VDD.*

2.3 Reset and power supply supervisor

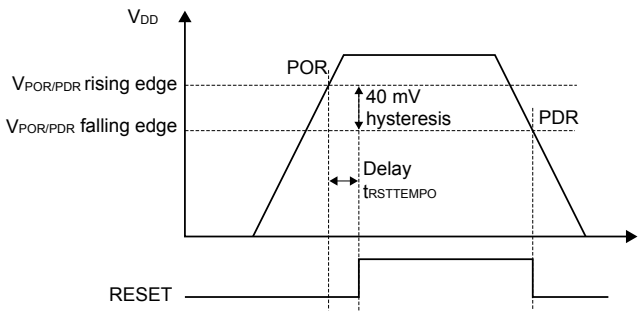
2.3.1 Power-on reset (POR)/power-down reset (PDR)

The device has an integrated POR/PDR circuitry that allows proper operation starting from 1.71 V.

The device remains in the reset mode as long as V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

For more details concerning the power-on/power-down reset threshold, refer to the electrical characteristics in the product datasheets.

Figure 2. Power-on reset/power-down reset waveform



Note: $t_{RSTTEMPO}$ is approximately 2.6 ms. $V_{POR/PDR}$ rising edge is 1.67 V (typ.) and $V_{POR/PDR}$ falling edge is 1.63 V (typical). Refer to the product datasheets for actual value.

The internal POR/PDR circuitry can be disabled through the PDR_ON pin. In that case, an external power-supply supervisor must monitor V_{DD} and must maintain the device in reset mode as long as V_{DD} is below a specified threshold.

2.3.2 Programmable voltage detector (PVD)

The user can use the PVD to monitor the V_{DD} power supply by comparing it to a threshold. The threshold can be selected by the PLS[2:0] bits in the power control register (PWR_CR).

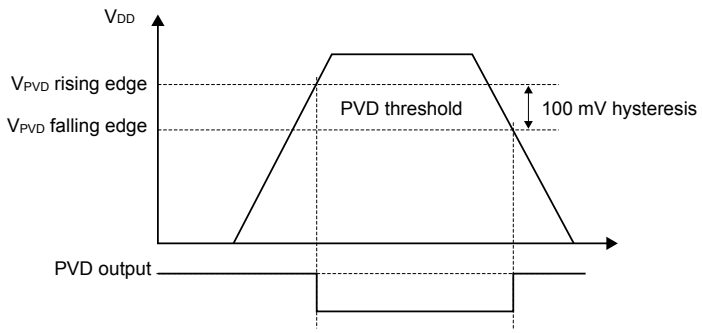
The PVD is enabled by setting the PVDE bit.

A PVDO flag is available, in the power control/status register (PWR_CSR), to indicate whether V_{DD} is higher or lower than the PVD threshold. This event is internally connected to EXTI Line16 and can generate an interrupt if enabled through the EXTI registers. Depending on the EXTI Line16 rising/falling edge configuration, the PVD output interrupt can be generated when:

- V_{DD} drops below the PVD threshold
- V_{DD} rises above the PVD threshold
- When both conditions are met

As an example, the service routine can perform emergency shutdown tasks.

Figure 3. PVD thresholds



2.3.3 Application and system resets

An application reset (app_rst) is generated from one of the following sources:

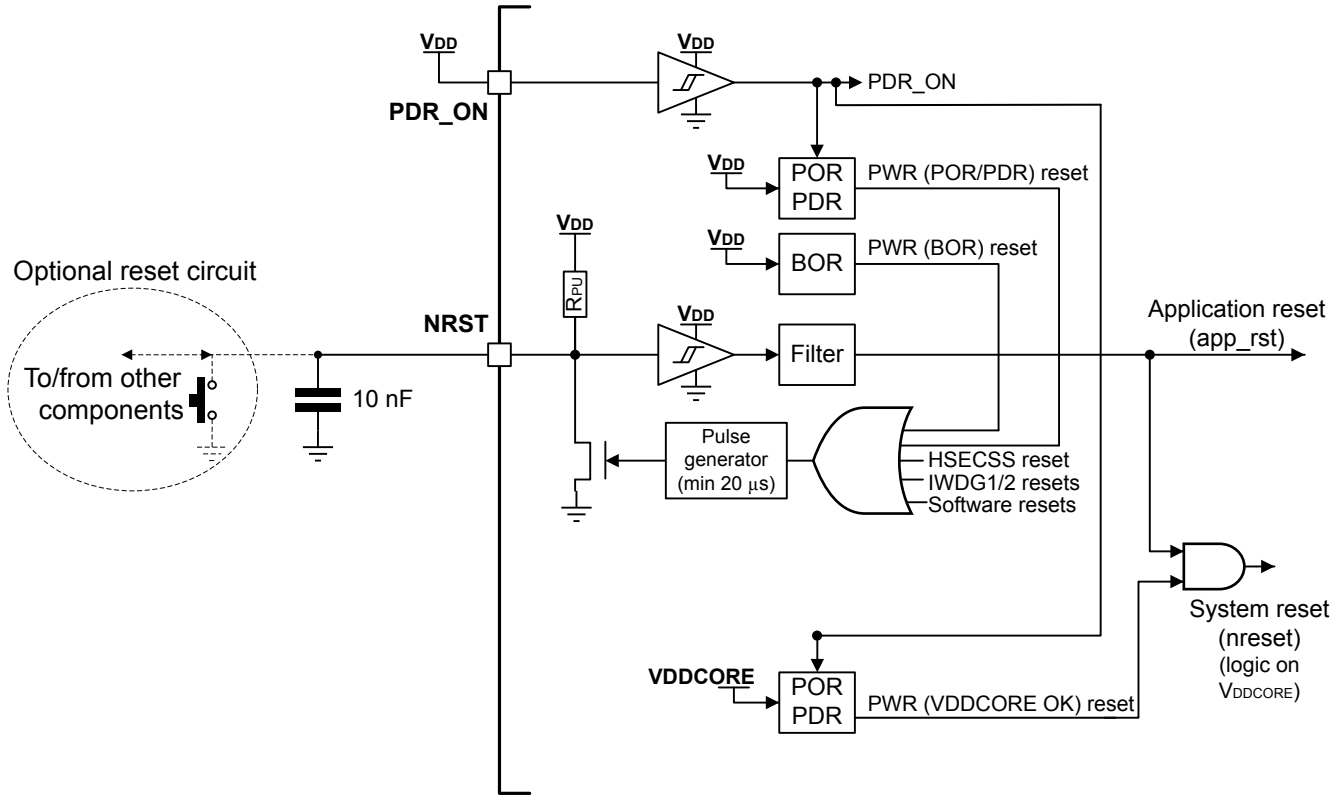
- reset from NRST pad
- reset from por_rst signal (generally called power-on reset)
- reset from bor_rst signal (generally called brownout)
- reset from the independent watchdog 1 (iwdg1_rst)
- reset from the independent watchdog 2 (iwdg2_rst)
- software reset from the RCC when the Cortex-A7 (MPU) sets the MPSYSRST bit to 1 (in the RCC)
- failure on HSE, when the clock security-system feature is activated (hcss_rst)

A system reset (nreset) is generated from one of the following sources:

- reset from app_rst signal (application reset)
- reset from vcore_rst signal

Note: When the system is in Standby, the V_{DDCORE} is switched off, but V_{DD} is still present. So when the system exits from Standby, the vcore_rst signal is activated, generating a nreset reset.

Figure 4. **Simplified reset pin circuit**



3 Packages

3.1 Package selection

The package must be selected by taking into account the constraints that are strongly dependent upon the application.

On STM32MP13x devices:

- All packages have identical pins and functions available (with the exception of TFBGA320 11 x 11, that does not provide DDR_DTO0 pin for DDR DLL test purposes).
- All packages have 135 GPIOs (including three BOOT signals and four JTAG signals multiplexed on GPIOs).

The list below summarizes the more frequent constraints:

- PCB technology constraints
  Small pitch and high ball density may require more PCB layers and higher PCB class requiring stackup with micro-via (laser via) technology.
- Package height
- PCB available area
- Thermal constraints (larger packages have better thermal dissipation capabilities)

The packages listed in the table below are available on all STM32MP13x devices.

Table 7. STM32MP13x package summary

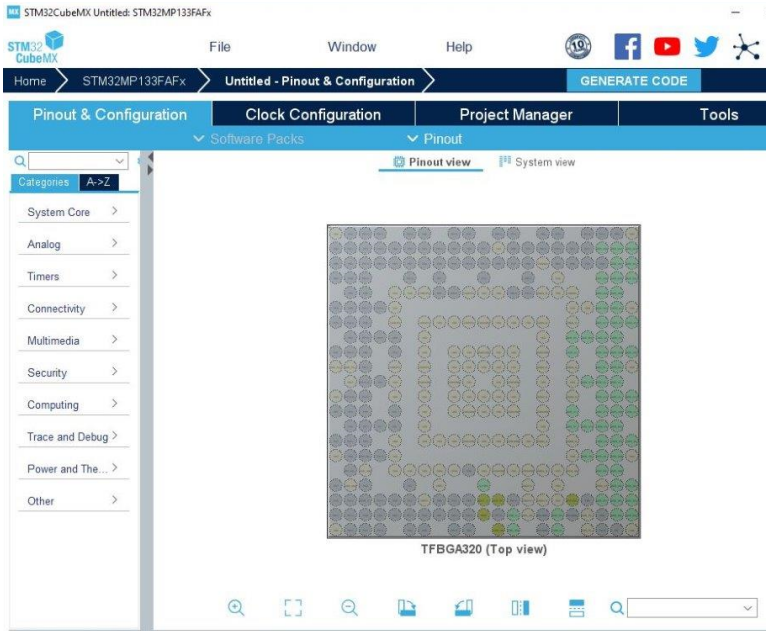
Package	Size(1) (mm x mm)	Minimum pitch (mm)	Height (mm)	Ball count
TFBGA289	9 x 9	0.5	1.2	289
TFBGA320	11 x 11	0.5	1.2	320
LFBGA289	14 x 14	0.8	1.4	289

1. *Typical body size.*

3.2 Alternate function mapping to pins

In order to easily explore peripheral alternate functions mapping to pins, it is recommended to use the STM32CubeMX tool.

Figure 5. STM32CubeMX example screen-shot



4 Clocks

Different clock sources can be used to drive the subsystem clocks:

- HSI oscillator clock (high-speed internal clock signal)
- CSI oscillator clock (low-power internal clock signal)
- HSE oscillator clock (high-speed external clock signal)
- PLL1/2/3/4 clocks
- PLL_USB to generate the USB clock (480 MHz)

The STM32MP13x devices have two secondary clock sources:

- 32 kHz low-speed internal RC (LSI RC). It drives the independent watchdog and optionally, the RTC used for auto wake-up from Stop and Standby modes
- 32.768 kHz low-speed external crystal (LSE crystal) that optionally drives the real-time clock (RTCCLK)

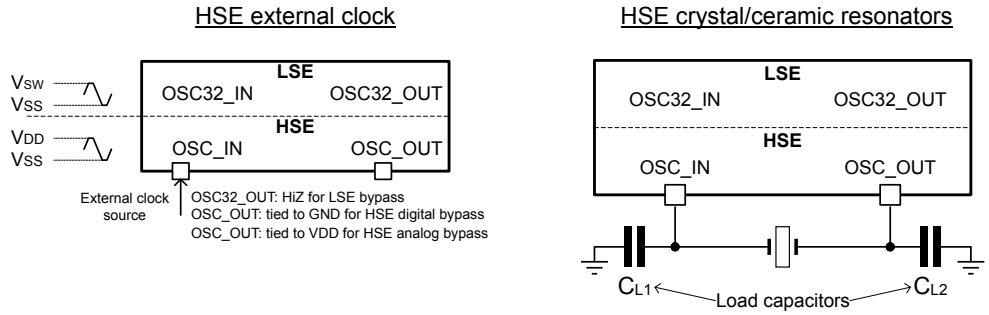
Each clock source can be switched on or off independently when it is not used, to optimize the power consumption. Refer to the product reference manual for the description of the clock tree.

4.1 HSE OSC clock

The HSE can be generated from two possible clock sources (see the figure below):

- HSE user external clock
- HSE external crystal/ceramic resonator

Figure 6. HSE clock sources



The next formula defines the load capacitance C_L:

$C_L = C_{L1} \times C_{L2}/(C_{L1} + C_{L2}) + Cstray$

Where Cstray is the pin capacitance and board or trace PCB-related capacitance (between 2 and 4 pF typical, see Section 7 Recommendations to minimize its value).

Refer to document [1] for more details.

4.1.1 External source (HSE bypass)

In this mode, an external clock source must be provided. This source can have a frequency from 8 to 50 MHz. Refer to product datasheets for actual maximum value.

The external digital or the analog clock signal with a duty cycle of about 50%, has to drive the OSC_IN pin. The external digital signal is V_{IL}/V_{IH} and the analog signal has an amplitude of 200 mV pk-pk minimum.

Note: To allow USB boot, the boot ROM automatically selects the HSE mode. It checks the OSC_OUT connection during the startup phase (on the NRST rising edge):

- *HSE digital bypass when OSC_OUT is tied to GND (1 kΩ max)*
- *HSE analog bypass when OSC_OUT is tied to V_{DD} (1 kΩ max)*
- *HSE crystal/ceramic resonator mode when OSC_OUT is high-impedance or connected to a crystal/ceramic resonator*

When the HSE bypass is used, PWR_ON can enable the external clock generator to save power (and disabled in Standby). In that case, the OSC_IN clock input must be stable within 10 ms after the PWR_ON rising edge occurs.

4.1.2 External crystal/ceramic resonator (HSE crystal)

The external oscillator frequency ranges from 8 to 48 MHz. The external oscillator produces a very accurate rate on the main clock. The associated hardware configuration is shown in Figure 6. Using a 24 MHz crystal frequency is a good choice to get accurate USB high-speed clocks.

The crystal/ceramic resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected crystal/ceramic resonator.

For C_{L1} and C_{L2}, it is recommended to use NP0/C0G capacitors in the 5 to 25 pF range (typical), selected to meet the load requirements of the crystal/ceramic resonator. C_{L1} and C_{L2} have usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}. The PCB and pin capacitances must be included when sizing C_{L1} and C_{L2} (10 pF can be used as a rough estimate of the combined pin and board capacitance).

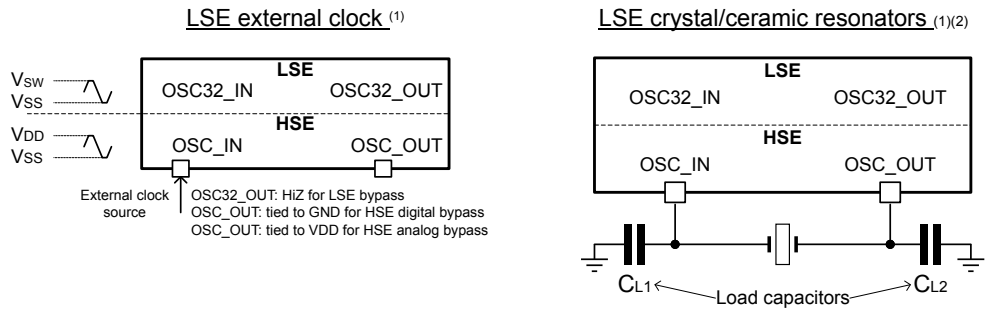
Refer to document [1] and electrical characteristics section in the product datasheet for more details.

4.2 LSE OSC clock

The LSE can be generated from two possible clock sources (see the figure below):

- LSE user external clock
- LSE external crystal/ceramic resonator

Figure 7. LSE source clocks



(1) OSC32_IN and OSC32_OUT pins can be used also as GPIO, but it is recommended not to use them as both RTC and GPIO pins in the same application.

(2) It is strongly recommended to use a resonator with a load capacitance $C_L \leq 12.5$ pF.

4.2.1 External source (LSE bypass)

In this mode, an external clock source must be provided, with a frequency of up to 1 MHz. The external digital or analog clock signal with a duty cycle of about 50% has to drive the OSC32_IN pin while the OSC32_OUT pin must be left high impedance. The external digital signal is V_{IL}/V_{IH} and the analog clock signal has an amplitude of 200 mV pk-pk minimum. Refer to Figure 7. The configuration of the bypass mode as well as the selection between the digital and analog is done within RCC registers.

4.2.2 External crystal/ceramic resonator (LSE crystal)

The LSE crystal is a 32.768 kHz low-speed external crystal or ceramic resonator. It provides a low-power, but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize the output distortion and startup stabilization time. The load capacitance values C_{L1} and C_{L2} must be adjusted according to the selected oscillator.

Refer to document [1] and electrical characteristics sections in the product datasheet for more details.

4.3 Clock security system (CSS) and clock monitoring

Details are available in the product reference manual.

4.3.1 HSE

HSE clock loss (clock not toggling) can be detected using CSS hardware. This works in Run and Stop modes, when the HSE oscillator is enabled. If a failure is detected on the HSE oscillator clock, a system reset can be generated and signaled to the TAMP for security protection. The CSS can be activated by software. In this case, the clock detector is enabled after the startup delay of the HSE oscillator. The clock detector is disabled when this oscillator stops.

The HSE over-frequency protection is performed using a secure low-power timer (LPTIM3) configured in timeout mode. In HSE over-frequency protection mode, LPTIM3 compares the HSE frequency to the HSI frequency. LPTIM3 then automatically triggers a tamper if the relative frequency exceeds the programmed limit. With this solution, the software can program the limit relative to the HSE nominal frequency that can be anything in the range.

Both HSE clock loss and HSE over-frequency protection outputs are ORed before the input of the corresponding internal tamper input (input tamper input #4).

4.3.2 LSE

LSE clock loss (clock not toggling for 200 µs) as well as over frequency (higher than 2 MHz) can be detected using LSE hardware and generate a tamper event. This works in all system modes, including VBAT mode. If a failure is detected on the LSE oscillator clock, the RTC/TAMP clock source is stopped and signaled to the TAMP for security protection (input tamper input #3).

5 Boot configuration

5.1 Boot mode selection

In the STM32MP13x devices, different boot modes can be selected by means of the BOOT[2:0] pins on a PI[6:4] GPIOs.

Table 8. Boot modes

BOOT2	BOOT1	BOOT0	Initial boot mode	Comments
0	0	0	UART and USB(1)	Wait incoming connection on: • USART3/6 and UART4/5/7/8 on default pins • USB HS device on OTG_HS_DP/DM pins (2)
0	0	1	Serial NOR-Flash(3)	Serial NOR-Flash on quad SPI(4)
0	1	0	eMMC(3)	eMMC on SDMMC2 (default)(4)(5)
0	1	1	NAND-Flash(3)	SLC NAND-Flash on FMC
1	0	0	Engineering boot (no flash boot)	Used to get debug access without boot from flash(6)
1	0	1	SD card(3)	SD card on SDMMC1 (default)(4)(5)
1	1	0	UART and USB(1)(3)	Wait incoming connection on: • USART3/6 and UART4/5/7/8 on default pins • USB HS device on OTG_HS_DP/DM pins(2)
1	1	1	Serial NAND-Flash(3)	Serial NAND-Flash on quad SPI(4)

1. *OTP settings can disable them. Note that an HSE clock/crystal is always required even for UART boot, unless USB and HSE frequency auto-detection are disabled in OTP.*
2. *USB requires an HSE clock/crystal if OTP is not programmed for different frequency (see Section 5.3 Embedded bootloader mode).*
3. *OTP settings can change boot source (example: initial boot on SD-Card, then eMMC with OTP settings).*
4. *OTP can alter default pins.*
5. *Alternatively, another SDMMC interface than this default can be selected by OTP.*
6. *Cortex-A7 Core0 in infinite loop toggling PA13.*

After a system reset, including exit from standby, the alternate function AF0 for the BOOT pins (PI[6:4]) is selected by default. The BOOT pins can be sampled in the SYSCFG_BOOTR register. The pins can then be used as GPIOs by programming the corresponding GPIOx_MODER and GPIOx_PUPDR registers.

Important: During a reset, the boot pins must be driven with the correct logic levels to select the required boot source.

In case of the UART boot using one of the possible U(S)ARTx_RX pins to avoid a floating signal sent to the host, and until the boot ROM receives and decodes the initialization character, it is required to have a 10 kΩ VDD pull-up on the respective U(S)ARTx_TX pin.

The UART_RX pin used for boot or system console should not be left floating to avoid a decoding of dummy serial characters. This could be ensured either by defining an internal pull-up in a uBoot/Linux device tree, or by using a 10 kΩ VDD pull-up on the board.

Table 9. UART possible boot pins

Peripheral	Signal	Pin
USART3	RX	PB12
	TX	PB10
UART4[1]	RX	PD8
	TX	PD6
UART5	RX	PB5
	TX	PB13
USART6	RX	PC7
	TX	PC6
UART7	RX	PF6
	TX	PF7
UART8	RX	PE0
	TX	PE1

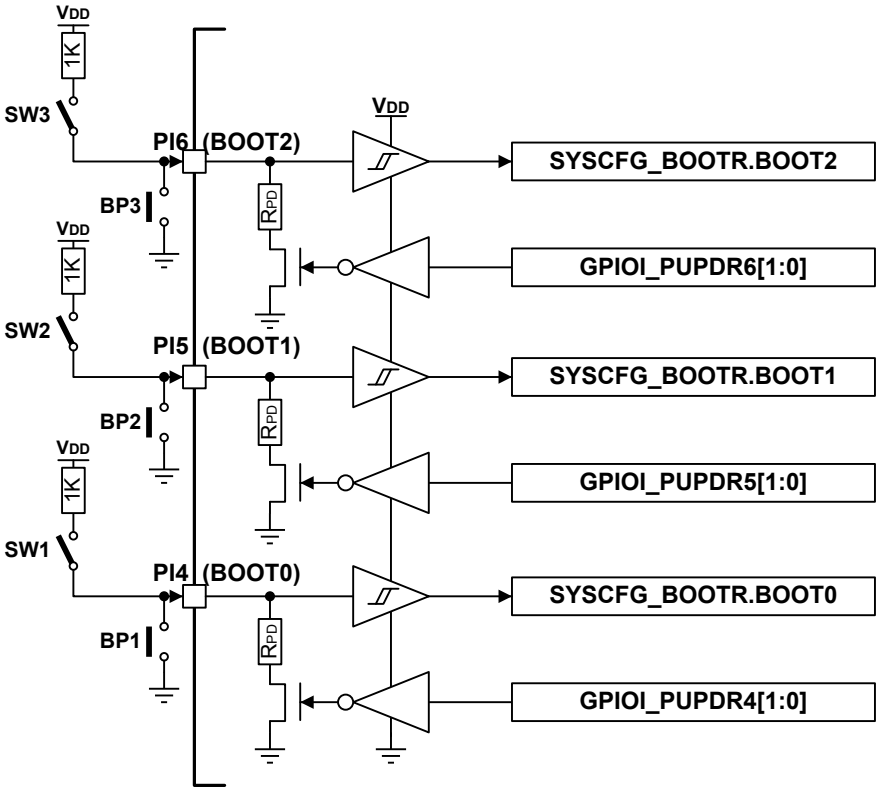
1. *Recommended default UART for Linux console (that is as VCP on STLINK STDC14 connector).*

5.2 Boot pin connection

The figure below shows an example of the external connection required to select the boot memory of the STM32MP13x devices.

The BOOT[2:0] pins on PI[6:4] GPIOs are selected by default after reset on AFmux.

Figure 8. Boot mode selection



Despite all the recovery cases in a software, there is a risk that, with wrong or corrupted Flash memory content the system may not start. This situation is also known as ‘bricked’. Wrong or corrupted Flash memory content can be the result of a user mistake, a bad Flash content programmed, or power lost.

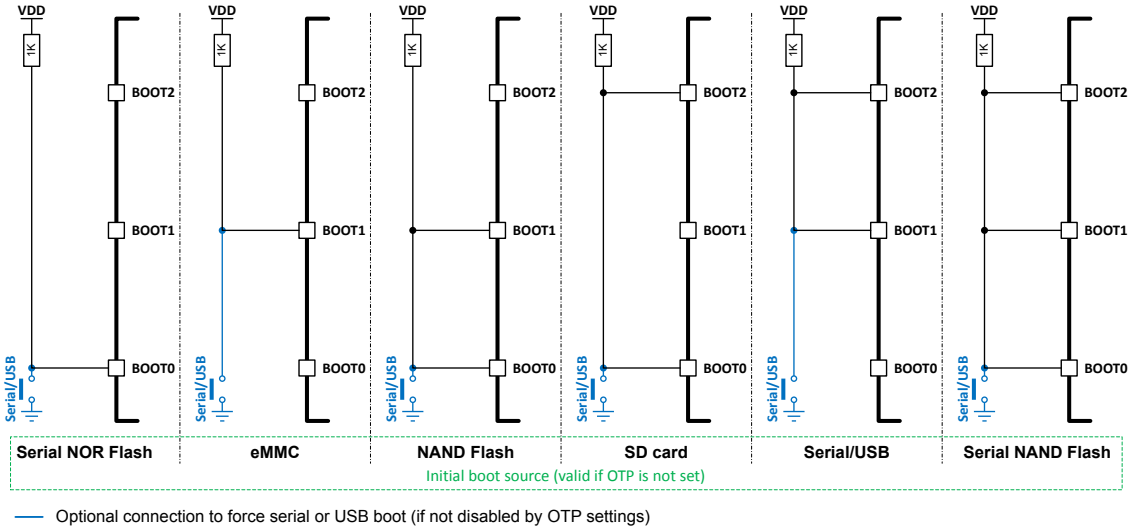
Note: On empty Flash, the boot code automatically switches to UART/USB connection.

It may be required to force use of an UART/USB connection to allow the board Flash memory to be reprogrammed. For example, after a sale services or a firmware update.

There are also cases where the initial boot is done on a different Flash than regular boot. The initial boot can be done from the SD-Card, that copies binary data in another Flash memory like a Serial NOR, a Serial NAND, an eMMC, or an SLC NAND. This is possible as the initial boot code can set the relevant OTP bits to force future boot from the programmed Flash (see Figure 10). This allows a simplified and flexible mass production without intervention on BOOT pins.

The typical connections examples for a final board are described in the figure below.

Figure 9. Typical connection schematics of BOOT pins



The switches can be done by various ways such as push-button, solder bridges, connector contacts, or test points. In any case, they are assumed open by default during normal product boot, to avoid current flow in external resistors.

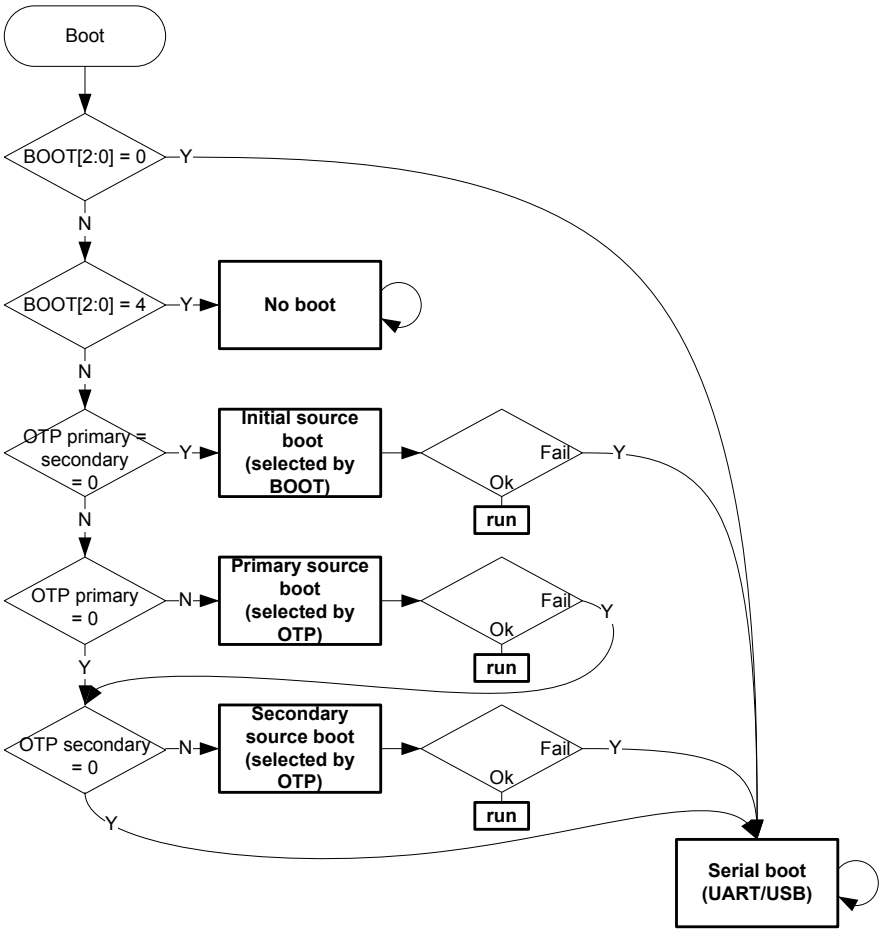
5.3 Embedded bootloader mode

This embedded bootloader is located in the boot ROM memory (refer to document [5] for additional information).

During boot, the QUADSPI, FMC, SDMMC and USART peripherals operate with the internal 64 MHz oscillator (HSI).

The USB OTG HS device, however operates only if an external clock (HSE) is present with a default frequency of either 8, 10, 12, 14, 16, 20, 24, 28, 32, 36, 40 or 48 MHz (automatic detection). Alternatively, a fixed 24, 25 or 26 MHz frequency could be used with OTP settings).

Figure 10. Simplified boot flow

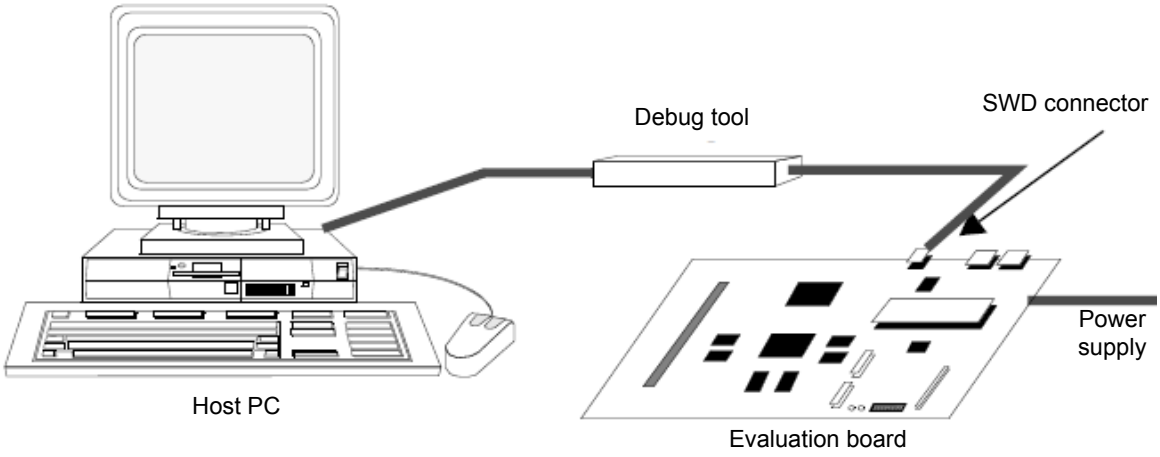


6 Debug management

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a JTAG, or SWD connector and a cable connecting the host to the debug tool.

The figure below shows the connection of the host to the evaluation board.

Figure 11. Host-to-board connection



6.1 SWJ debug port (serial-wire and JTAG)

The STM32MP13x core integrates the serial-wire/JTAG debug port (SWJ-DP). It is an Arm standard CoreSight™ debug port that combines:

- a JTAG debug port (JTAG-DP) providing a 5-pin standard JTAG interface to the AHP-AP port
- a serial-wire debug port (SW-DP) providing a 2-pin (clock + data) interface to the AHB-AP port

The two pins of the SW-DP are multiplexed with two of the five JTAG pins of the JTAG-DP.

On the STM32MP13x device, four JTAG signals are multiplexed on GPIOs on AFMux_00 as listed below:

- PF14 JTCK-SWCLK
- PF15 JTMS-SWDIO
- PH4 JTDI
- PH5 JTDO

NJTRST is available on a dedicated pin.

In order to use the RMA (return material acceptance) the JTAG pins (JTDI, JTCK, JTMS) must be accessible. The JTDO pin might be needed depending on the tool used to input the JTAG sequence into the STM32MP13x (some tools need to check the JTAG ID using JTDO output).

6.2 Pinout and debug port pins

6.2.1 Internal pull-up/pull-down resistors on JTAG pins

To avoid any uncontrolled I/O levels, the devices embed the following internal pull-up and pull-down resistors on JTAG pins:

- NJTRST: internal pull-up
- JTDI: internal pull-up
- JTDO-TRACESWO: internal pull-up
- JTMS-SWDIO: internal pull-up
- JTCK-SWCLK: internal pull-down

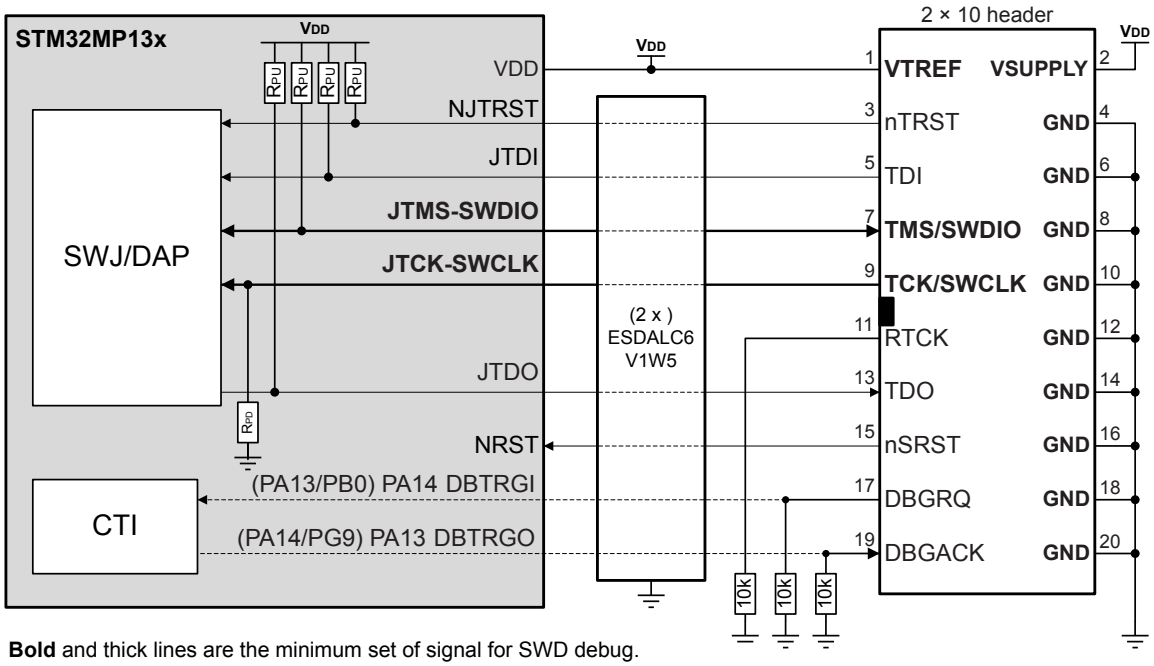
Note: The JTAG IEEE standard recommends adding pull-up resistors on TDI, TMS, and nTRST but there is no special recommendation for TCK. However, for the STM32MP13x devices, an integrated pull-down resistor is used for JTCK.

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

6.2.2 Debug port connection with standard JTAG connector

The figure below shows the connection between the STM32MP13x device and a standard JTAG/SWD connector.

Figure 12. JTAG/SWD MIPI10 connector implementation example

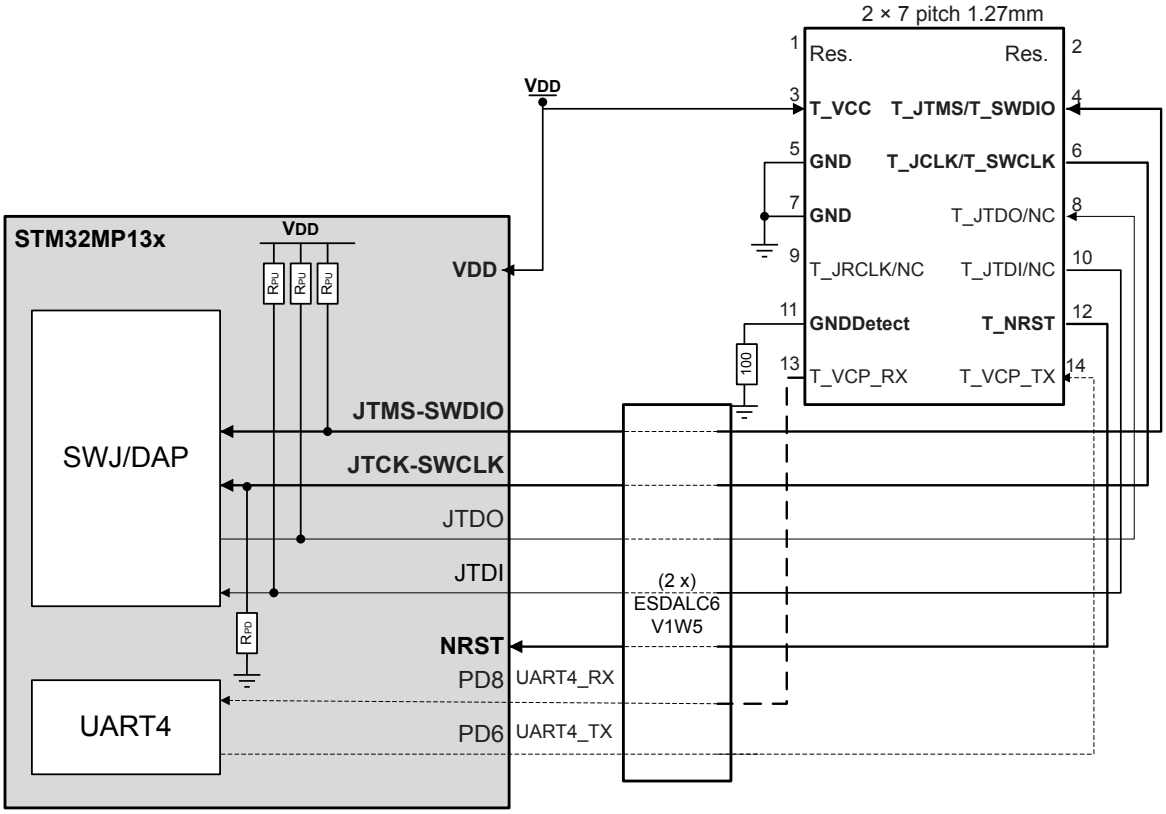


Bold and thick lines are the minimum set of signal for SWD debug.

6.2.3 Debug port and UART connection with STDC14 connector

The figure below shows the connection between the STM32MP13x device and an STDC14 connector, including an UART virtual communications port connection. The STDC14 header reference example is FTSH-107-01-L-DV-K-A.

Figure 13. JTAG/SWD/UART VCP STDC14 connector implementation example



Bold and thick lines: minimum set of signal for SWD debug.

Note: The STDC14 connector respects (from pin 3 to pin 12) the Arm10 pinout (Arm Cortex debug connector).

6.2.4 Parallel trace and HDP

6.2.4.1 Parallel trace

TRACED[15:0] and TRACECLK signals are available as alternate functions on I/O pins. The user can select the number of trace data N = 1, 2, 4, 8 or 16 pins. Less trace data means lower available trace bandwidth, so less information can be traced without trace overrun. There is a 4-Kbyte buffer in STM32MP13x devices. Information to be traced can be the number of trace sources, code, and/or data tracing. For each product, a trade-off between available features and trace bus leads to have reduced feature while using trace during product development.

The trace is compliant to Arm CoreSight trace. The trace needs a dedicated tracing tool in order to be interpreted and correlated with the debugging done through SWD or JTAG.

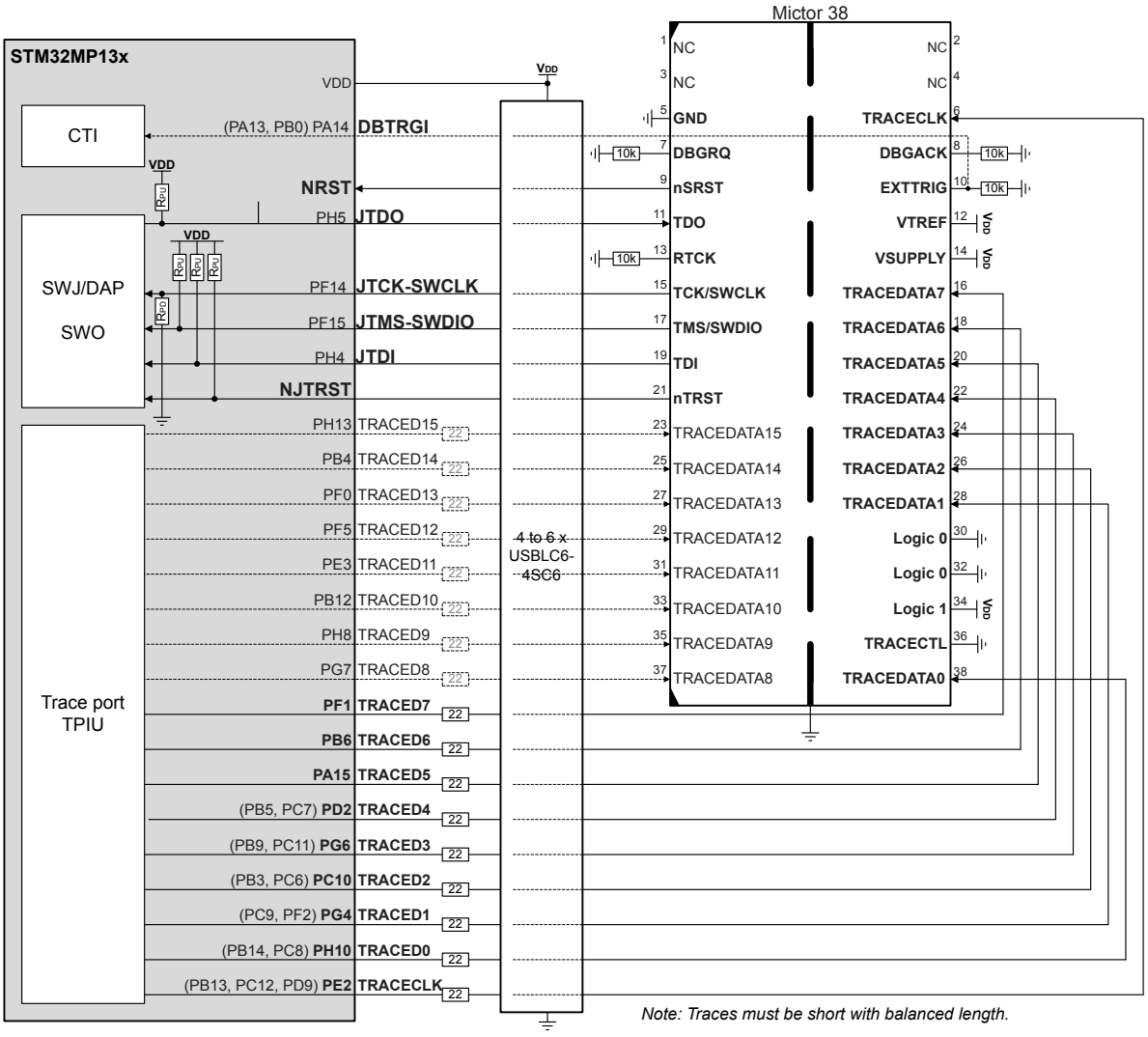
For more information on the TPI (trace port interface) CoreSight component, refer to the product reference manual and the CoreSight SoC-400 technical reference manual.

Note: For efficient tracing bandwidth, TRACECLK must run as fast as possible while maintaining good signal integrity on all parallel trace signals. This is dependent on board and connector choices, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DD} voltage.

When using V_{DD} = 1.8 V, a setting in the OTP bit product_below_2v5 and the register SYSCFG_HSLVEN0R (HSLVEN_TRACE bit) may be required. This setting ensures the best speed on the pads that are used on trace signals.

Warning: *HSLVEN must not be set when V_{DD} is above 2.7 V, otherwise permanent device damage may occur.*

Figure 14. Parallel trace port with JTAG/SWD on Mictor-38 implementation example



6.2.4.2 *Hardware debug port*

Some internal signals are available for deep debugging. Internal knowledge and an oscilloscope or logic analyzer are needed. For more information, refer to the product reference manual and datasheet.

6.2.5 Debug triggers and LEDs

The CoreSight CTI (cross-trigger interface) is available on pins as DBTRGI and DBTRGO:

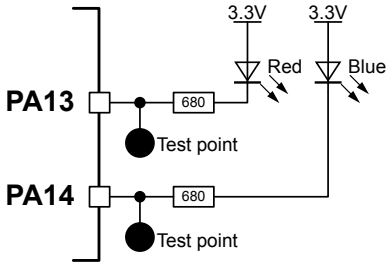
- DBTRGI pin can be generated by an external user signal. It can be programmed inside the CoreSight components to start/stop traces or to enter specific cores in debug mode (break). DBTRGI can be made available on PA13, PA14, or PB0.
- DBTRGO can be generated by CTI. It allows to see externally that one of the CoreSight components (such as core break or trace started) has reached a trigger condition. DBTRGO can be made available on PA13, PA14, or PG9.

The PA13 pin has the following specific behavior (see boot documentation for details):

- During a boot phase, in case of boot failure, PA13 is set to low open-drain. The error LED lights bright.
- During UART/USB boot, PA13 toggles open-drain at a rate of about 5 Hz until a connection starts. The error LED blinks fast.
- With BOOT[2:0] = 0b100 (no boot, used for specific debug), PA13 toggles open-drain at a rate of about 5 kHz. The error LED lights weak.
- In all other cases, PA13 is kept in its reset value (high-z until software setting).

It is a good idea to put a red LED on PA13 as shown in the figure below.

Figure 15. LED connections example



LEDs are useful for quick visual signaling of the system activity. So, it is a good choice to use PA13 and PA14. This does not avoid the usage of DBTRGI and DBTRGO on PA13 or PA14 for debug (assuming the software stops controlling LEDs during this specific debug).

7 Recommendations

7.1 PCB (printed circuit board)

For technical reasons, to have good decoupling and a good shielding effect, it is mandatory to use a multilayer PCB with:

- a separate layer dedicated to the ground (VSS)
- another layer dedicated to power supplies like V_{DD}, VDDCPU, and V_{DDCORE}.

7.2 Component position

A preliminary layout of the PCB must separate the different circuits according to their EMI contribution in order to reduce cross-coupling on the PCB, that is noisy, high-current circuits, low-voltage circuits, and digital components.

7.3 Ground and power supplies (V_{SSx}, V_{DDx})

Due to the large power and high frequencies involved in STM32MP13x devices, it is mandatory to use a PCB with the following characteristics:

- at least four layers
- dedicated power planes for V_{SSx} and V_{DDx}.

7.4 I/O speed settings

It is important to set the right output drive on the I/Os. This ensures to have sufficient rise and fall times, and also to avoid additional ringing and noise.

When there are no specific I/O speed requirements, OSPEEDR must be set to 0.

As a first approximation, the table below helps to quickly choose the right setting to apply according to signal frequency and capacitive load. This setting may need to be tailored in case of signal integrity issue.

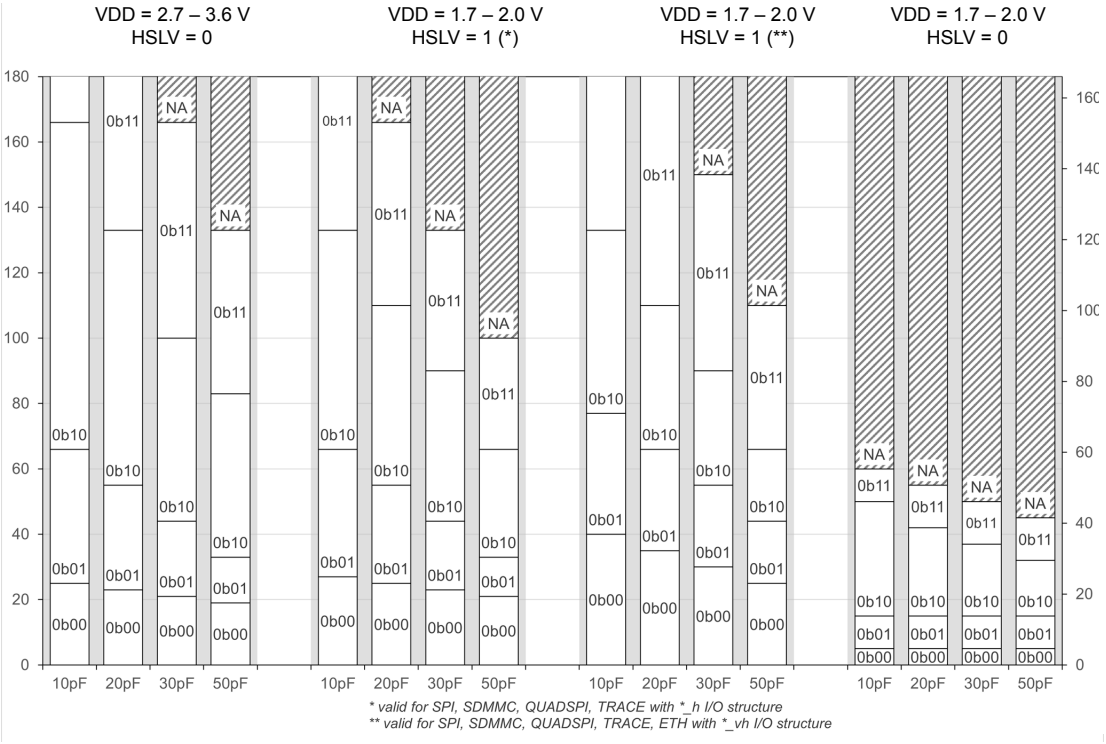
In most cases, the I/O compensation needs to be enabled in SYSCFG (refer to product datasheet for more details).

In the case of asynchronous or single-edge clocked data lanes (such as SDR), the maximum data frequency toggle is effectively half the data rate. For example, an SPI running at 10 Mbit/s has a maximum frequency of 5 MHz on data signal (for example: output serial data 01010101), but 10 MHz on the clock signal. On dual-edge clocked data lanes (such as DDR), the clock, and data have the same maximum toggling frequency.

For high-speed interfaces (SDMMC, QSPI, ETH, SPI, LTDC, and TRACE), high-speed low voltage (HSLV) mode must be enabled when the I/O supply is less than 2.7 V, to ensure sufficient slew rate. HSLV mode is enabled for each interface independently, by writing a special value into the corresponding SYSCFG_HSLVENxR register.

Warning: *Enabling HSLV mode when the I/O supply is greater than 2.7 V, may damage the device.*

Figure 16. I/O speed summary with various loads and voltages



The OTP bit product_below_2v5 must be programmed before HSLV is enabled, for all interfaces except SDMMC.

Table 10. OSPEEDR setting example for V_{DD} = 3.3 V typical

Peripheral	Signals	Toggling rate (MHz)	OSPEEDR			
			Speed with C_L = 30 pF		Speed with C_L = 10 pF	
FMC async	Data/controls	50	2	High speed	1	Medium speed
FMC sync	CLK	100	2	High speed	2	High speed
	Data/controls	50	2	High speed	1	Medium speed
QUADSPI (SDR)	CLK	133	2	High speed (1)	2	High speed
	Data/controls	66.5	2	High speed	2	High speed
QUADSPI (DDR)	All	66.5	2	High speed	2	High speed
LTDC (HDMI) (2)	CLK	74.25	2	High speed	2	High speed
	Data/controls	37.125	1	Medium speed	1	Medium speed
LTDC (2)	CLK	90	2	High speed	2	High speed
	Data/controls	45	2	High speed	1	Medium speed
LTDC	CLK	48	2	High speed	1	Medium speed
	Data/controls	24	1	Medium speed	0	Low speed
TIM/LPTIM	All	5	0	Low speed	0	Low speed
I2C	All	1	0	Low speed	0	Low speed
USART	All	5	0	Low speed	0	Low speed
SPI	CLK	50	2	High speed	1	Medium speed

Peripheral	Signals	Toggling rate (MHz)	OSPEEDR			
			Speed with C_L = 30 pF		Speed with C_L = 10 pF	
SPI	Data/controls	25	1	Medium speed	0	Low speed
SAI	MCLK	15	0	Low speed	0	Low speed
	CLK	1	0	Low speed	0	Low speed
	Data/controls	0.5	0	Low speed	0	Low speed
SDMMC (SDR)	CLK	130	2	High speed (1)	2	High speed
	Data/controls	65	2	High speed (1)	1	Medium speed
SDMMC (DDR)	All	52	2	High speed	1	Medium speed
FDCAN	All	5	0	Low speed	0	Low speed
ETH (MII)	CLK	50	2	High speed	1	Medium speed
	Data/controls	25	1	Medium speed	0	Low speed
ETH (RMII)	All	50	2	High speed	1	Medium speed
ETH (RGMII)	All	125	3	Very high speed	2	High speed
ETH (MDIO)	MDIO	2.5	0	Low speed	0	Low speed
TRACE	All	133	3	Very high speed	2	High speed
		100	2	High speed	2	High speed

1. *Value for CL = 20 pF.*
2. *Requires external oscillator for HSE.*

Table 11. OSPEEDR setting example for V_{DD} = 1.8 V typical

Peripheral	Signals	Toggling rate (MHz)	OSPEEDR C_L=30 pF		OSPEEDR C_L=10 pF	
FMC async	Data / controls	50	3	Very high speed	2	High speed
FMC sync	CLK	45	3	Very high speed	2	High speed
	Data / controls	22.5	2	High speed	2	High speed
QUADSPI (SDR) (1)	CLK	133	3	Very high speed(2)	2	High speed
	Data / controls	66.5	2	High speed	2	High speed
QUADSPI (DDR) (1)	All	66.5	2	High speed	2	High speed
LTDC (HDMI) (3)	CLK	74.25	2	High speed (2)	2	High speed
	Data / controls	37.125	1	Medium speed	1	Medium speed
LTDC (3)	CLK	69	2	High speed	2	High speed
	Data / controls	34.5	1	Medium speed	1	Medium speed
TIM/LPTIM	All	5	0	Low speed	0	Low speed
I2C	All	1	0	Low speed	0	Low speed
USART	All	5	0	Low speed	0	Low speed
SPI (4)	CLK	50	2	High speed	1	Medium speed
	Data / controls	25	1	Medium speed	0	Low speed
SAI	MCLK	15	1	Medium speed	1	Medium speed
	CLK	1	0	Low speed	0	Low speed
	Data / controls	0.5	0	Low speed	0	Low speed
SDMMC (SDR)(5)	CLK	130	3	Very high speed (2)	2	High speed
	Data / controls	65	2	High speed	1	Medium speed

Peripheral	Signals	Toggling rate (MHz)	OSPEEDR C_L=30 pF		OSPEEDR C_L=10 pF	
SDMMC (DDR) (5)	All	52	2	High speed	1	Medium speed
FDCAN	All	5	0	Low speed	0	Low speed
ETH (MII)	CLK	50	1	Medium speed	1	Medium speed
	Data / controls	25	0	Low speed	0	Low speed
ETH (RMII)	All	50	1	Medium speed	1	Medium speed
ETH (RGMII) (6)	All	125	3	Very high speed (2)	2	High speed
ETH (MDIO)	MDIO	2.5	0	Low speed	0	Low speed
TRACE (7)	All	133	3	Very high speed (2)	2	High speed
		100	3	Very high speed	2	High speed

1. *HSLVENxR enabled for QUADSPI.*
2. *Value for CL=20 pF.*
3. *HSLVENxR enabled for LTDC.*
4. *HSLVENxR enabled for SPI.*
5. *HSLVENxR enabled for SDMMC.*
6. *HSLVENxR enabled for ETH.*
7. *HSLVENxR enabled for TRACE.*

7.5 PCB stack and technology

A trade-off between the PCB cost and easy electrical connections has to be made. Examples for 6- and 4-layer PCB, are detailed in the figures below.

Using only PTH is possible for 14x14 0.8 mm pitch package and 11x11 0.5 mm pitch package. Using PTH, buried vias and laser drilled vias may be needed for 9x9 0.5 mm pitch package.

Figure 17. 4-layer PCB stack example (with only PTH via)

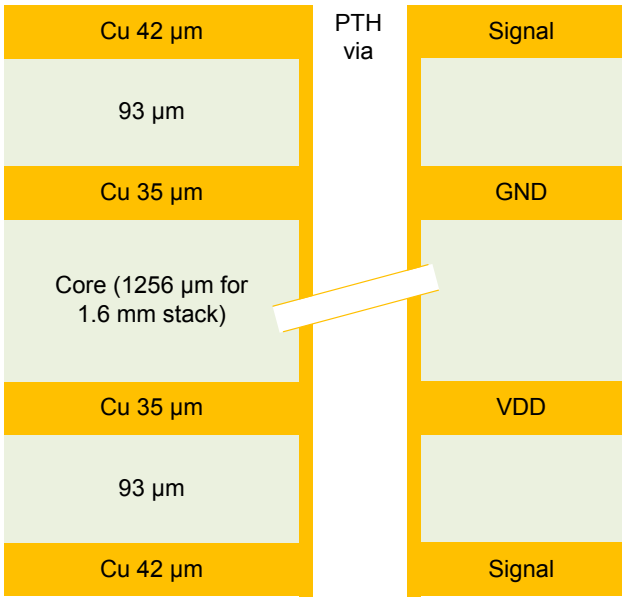


Figure 18. **6-layer PCB stack example (with PTH, buried via and laser via)**

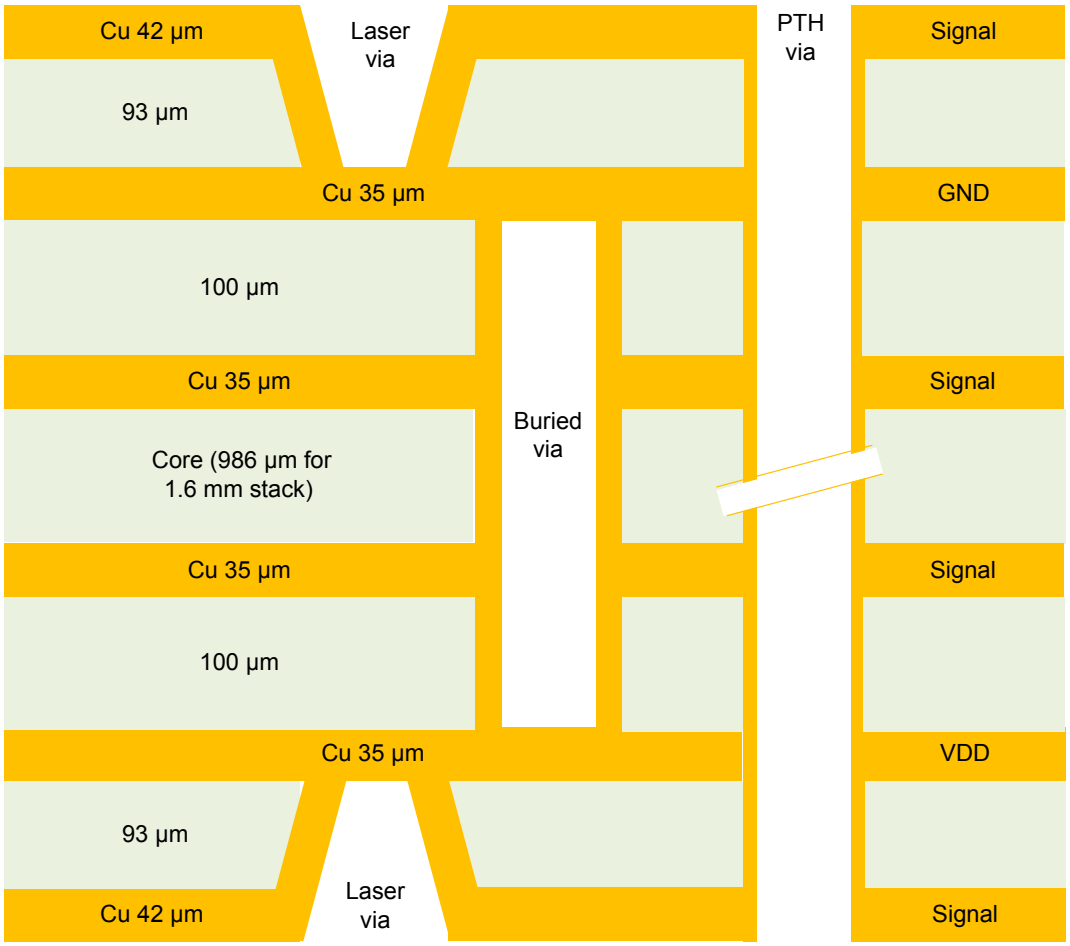


Figure 19. **PCB rule example for 0.8 mm pitch package (with PTH)**

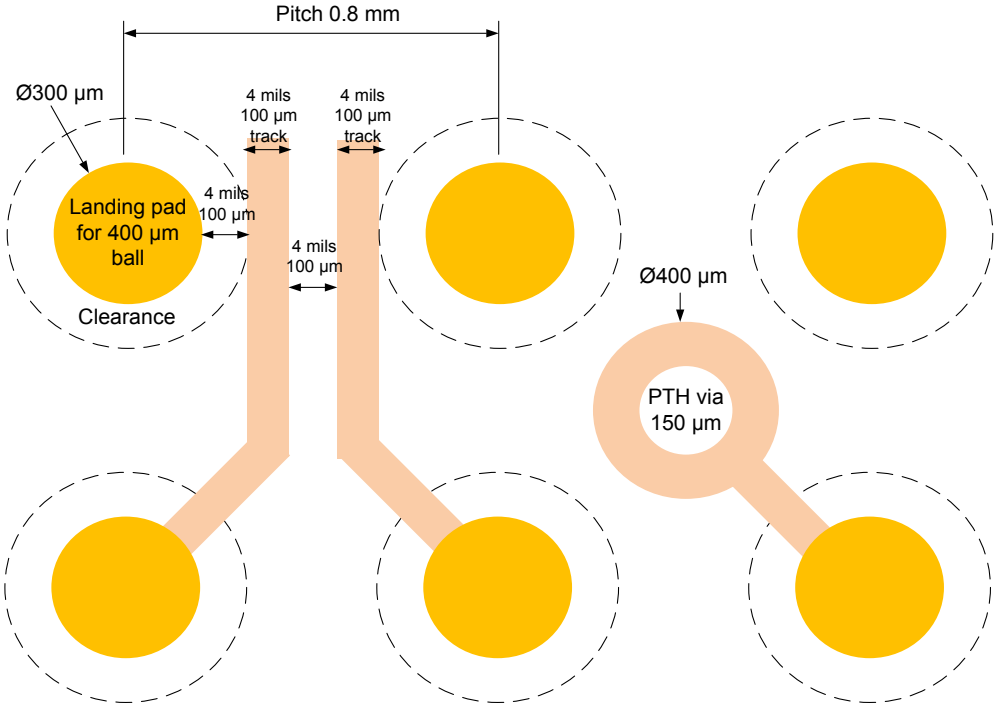
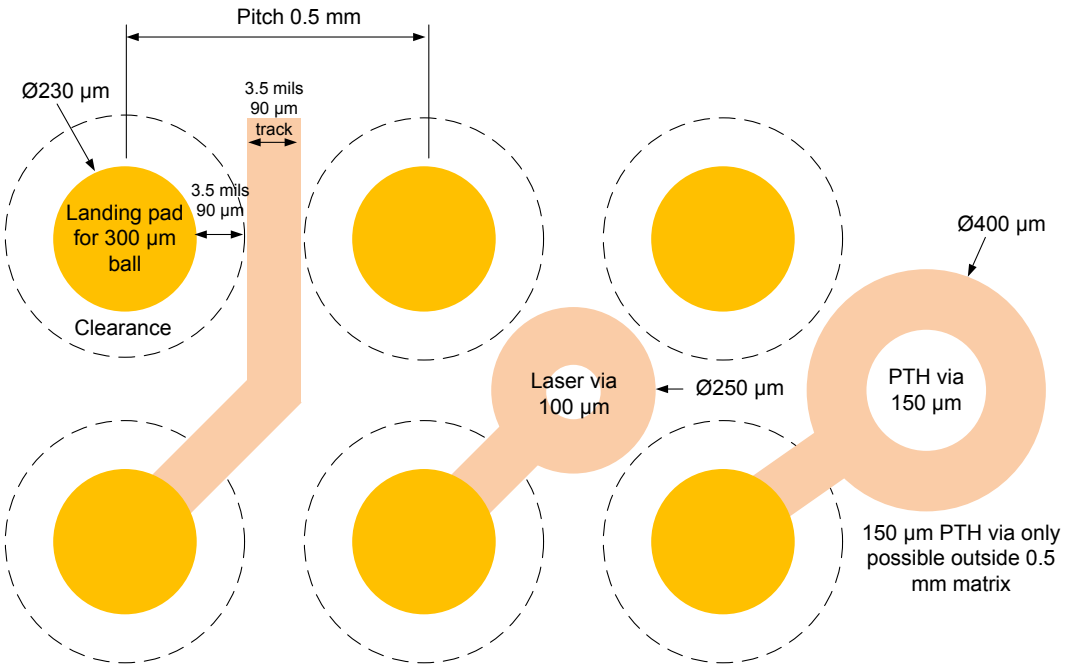


Figure 20. **PCB rule example for 0.5 mm pitch package (with laser via and PTH)**



7.6 Decoupling and package escape routing

All power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias must have an impedance as lowest as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair must be decoupled with ceramic capacitors (see Table 5 for details). These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Exact values depend on the application.

The recommended PCB layout and escape routing, as well as the placement of decoupling capacitances for various package types, can be found in the reference design attached to the *STM32MP13x lines DDR memory routing guidelines* (AN5692).

7.7 ESD/EMI protections

ESD (electrostatic discharge) and EMI (electromagnetic interference) must be taken into account from the beginning of a product development, as adding them later may be very complex and expensive.

ESD and EMI are driven by global standards (such as IEC 61000 or JESD 22) that, in most countries, require a certification to allow mandatory marking to be applied on a product (for example CE or FCC). ESD and EMI are also driven by standardized interface certification or requirements (such as USB).

The final product ESD protection should be done by external components, more especially on interfaces having external user access in the final product (such as Ethernet, USB, or SD-card).

Some components provide ESD protection as well as EMI common mode filtering (such as ECMF02-2AMX6 used on USB). Some examples of ESD/EMI protections are detailed in Section 8 Reference design examples.

For more details, refer to the document [2].

7.8 Sensitive signals

When designing an application, the study of the points listed below can improve the electromagnetic compatibility (EMC):

- signals for which a temporary disturbance affects the running process permanently. For example, interrupts and handshaking strobe signals. It is not the case for LED commands.
  The following actions improve the EMC performance for these signals:
  - a surrounding ground trace
  - shorter lengths
  - absence of noisy or sensitive traces nearby (crosstalk effect)

  For digital signals, the best possible electrical margin must be reached for the two logical states. Slow Schmitt triggers are recommended to eliminate parasitic states.
- noisy signals (such as clock)
- sensitive signals (such as high-impedance ones)

For more details, refer to the document [2].

7.9 Unused I/Os and features

The STM32MP13x devices are designed for a wide range of applications and a specific application rarely uses 100% of the MCU resources.

To increase the EMC performance, unused clocks, counters, or I/Os must not be left free: for example, I/Os must be set to 0 or 1 (pull-up or pull-down on unused I/O pins) and unused features must be frozen or disabled.

Refer to Table 6. Supply usage for unused features.

8 Reference design examples

This section provides examples to help the user to connect major and critical interfaces to the STM32MP13x devices.

8.1 Clock

The two following clock sources are used for STM32MP13x devices (see Section 4 for details):

- LSE: 32.768 kHz crystal for the embedded RTC
- HSE: 24 MHz crystal or external oscillator as MCU main clock

Figure 21. HSE recommended schematics for both oscillator/crystal options

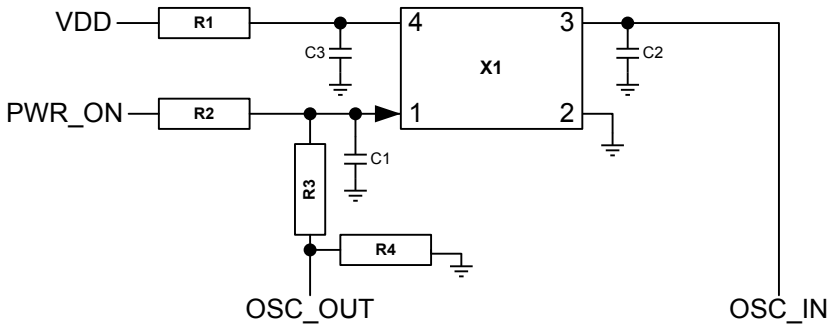


Table 12. HSE BOM for oscillator or crystal

-	Oscillator	Crystal option
X1	NZ2016SH 24 MHz	NX2016SA 24 MHz
R1	10 Ω	-
R2	10 KΩ	-
R3	-	0 Ω
R4	1 KΩ	-
C1	-	6.8 pF
C2	-	6.8 pF
C3	10 nF	-

8.2 Reset

The NRST reset signal is active low (see Figure 3. PVD thresholds). The reset sources include the "reset" button and debugging tools via the JTAG connector (refer to Section 2.3 Reset and power supply supervisor).

8.3 Boot mode

The boot option is configured by setting permanent wires or switches SW3 (BOOT2 on pin PI6), SW2 (BOOT1 on pin PI5) and SW1 (BOOT0 on pin PI4) and internal OTP. Refer to Section 5 Boot configuration.

A 10 kΩ VDD pull-up on the U(S)ARTx_TX pin is mandatory when the U(S)ART boots using this pin. This avoids a floating signal sent to the host, until the boot ROM receives and decodes the initialization character .

Table 13. U(S)ART possible boot pins

Peripheral	Signal	Pin
USART3	Rx	PB12
	Tx	PB10
UART4(1)	Rx	PD8
	Tx	PD6
UART5	Rx	PB5
	Tx	PB13
USART6	Rx	PC7
	Tx	PC6
UART7	Rx	PF6
	Tx	PF7
UART8	Rx	PE0
	Tx	PE1

1. *Recommended default UART for Linux® console (as VCP on STLINK STDC14 connector).*

In case of QUADSPI boot, the QUADSPI may boot from one of the following:

- from a dedicated default QUADSPI boot GPIO, used to connect a QUADSPI single bank on the board
- using some FMC Nand8 boot GPIOs (PD1, PD4, PD5, PD11, PD15, PE9), used to connect an FMC Nand8 on the board, with:
  - PD1: QUADSPI_BK1_NCS
  - PD4: QUADSPI_CLK
  - PD5: QUADSPI_BK1_IO0
  - PD11:QUADSPI_BK1_IO2
  - PD15: QUADSPI_BK1_IO3
  - PE9: QUADSPI_BK1_IO1

8.4 SWD/JTAG interface

The reference design shows the connections between the STM32MP25x devices and some standard connector (refer to Debug management).

Note: If available, it is recommended to connect the debugger probe system reset pin to NRST. This action permits resetting the application from the debugger.

Table 14. SWD/JTAG interface

Interface	Signal	Pin	I/O supply domain
UART6	USART6 Rx	PF4	VDD
	USART6 Tx	PF5	
UART8	UART8 Rx	PF3	VDD
	UART8 Tx	PG3	
UART9	UART9 Rx	PB14	VDD
	UART9 Tx	PD13	

8.5 Power supply

Refer to Section 2 Power supplies.

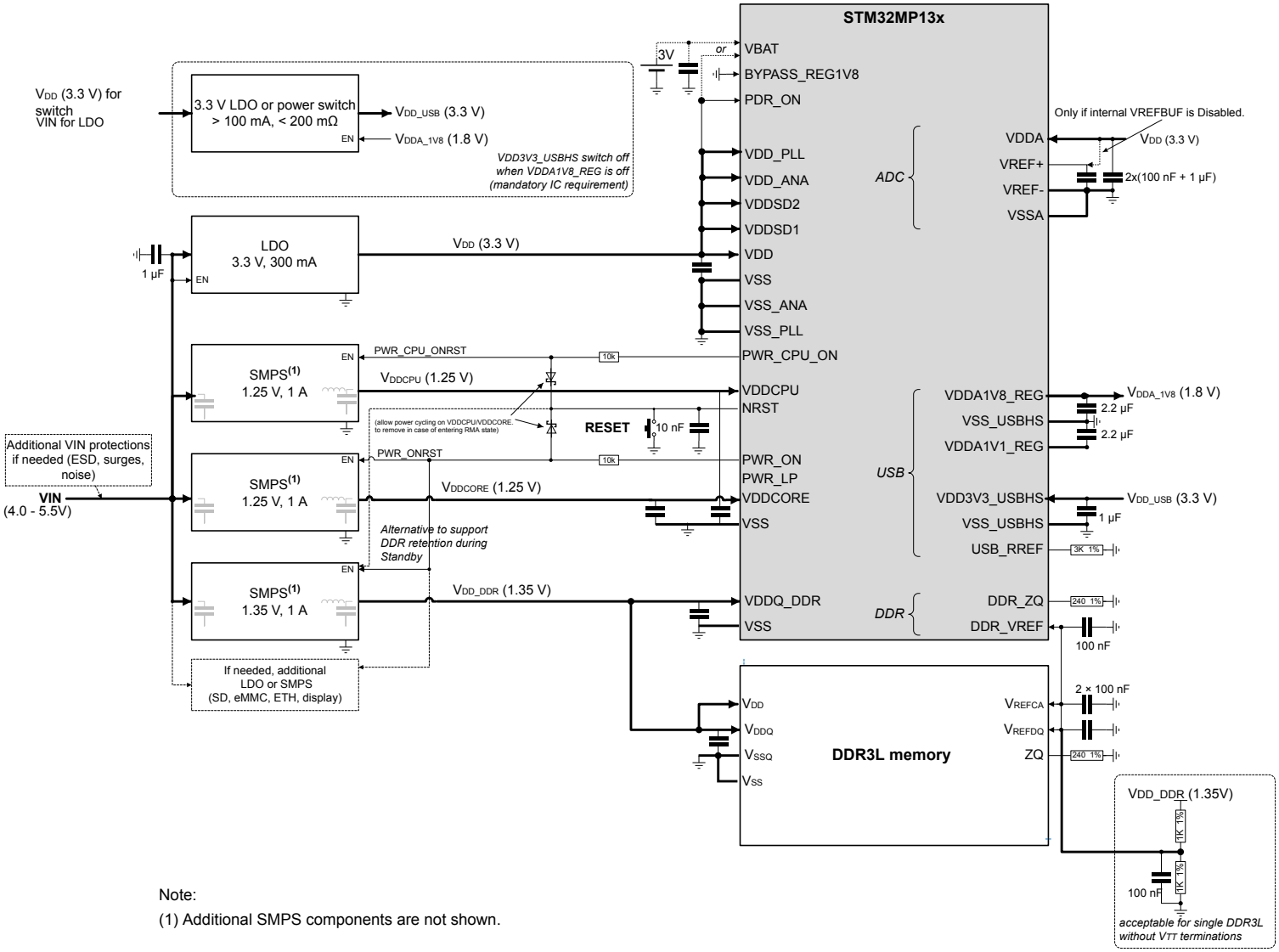
8.5.1 Discrete supply example 3.3 V I/Os with DDR3L

This reference design example targets a simple 3.3 V I/O platform with low-cost DDR3L without emphasis on power reduction. Sleep, Stop, and Standby modes are supported.

LP-Stop and low-power Standby with DDR3L retention can be supported. This support is not very interesting due to the use of DDR3L, which does not have a low-power target for self-refresh. Refer to the document [10] for more details.

A power cycle should be done on VDDCPU and VDDCORE when nRST is activated or when the STM32MP13x exits from Standby mode. Hence, the connection of SMPS enable signals to PWR_ONRST and PWR_CPU_ONRST. In the case of entering RMA state for returning devices for failure analysis, the power cycling should not be done. So, the two diodes connected to PWR_ONRST and PWR_CPU_ONRST must be removed.

Figure 22. Discrete supply example with 3.3 V I/Os and DDR3L



Note:

(1) Additional SMPS components are not shown.

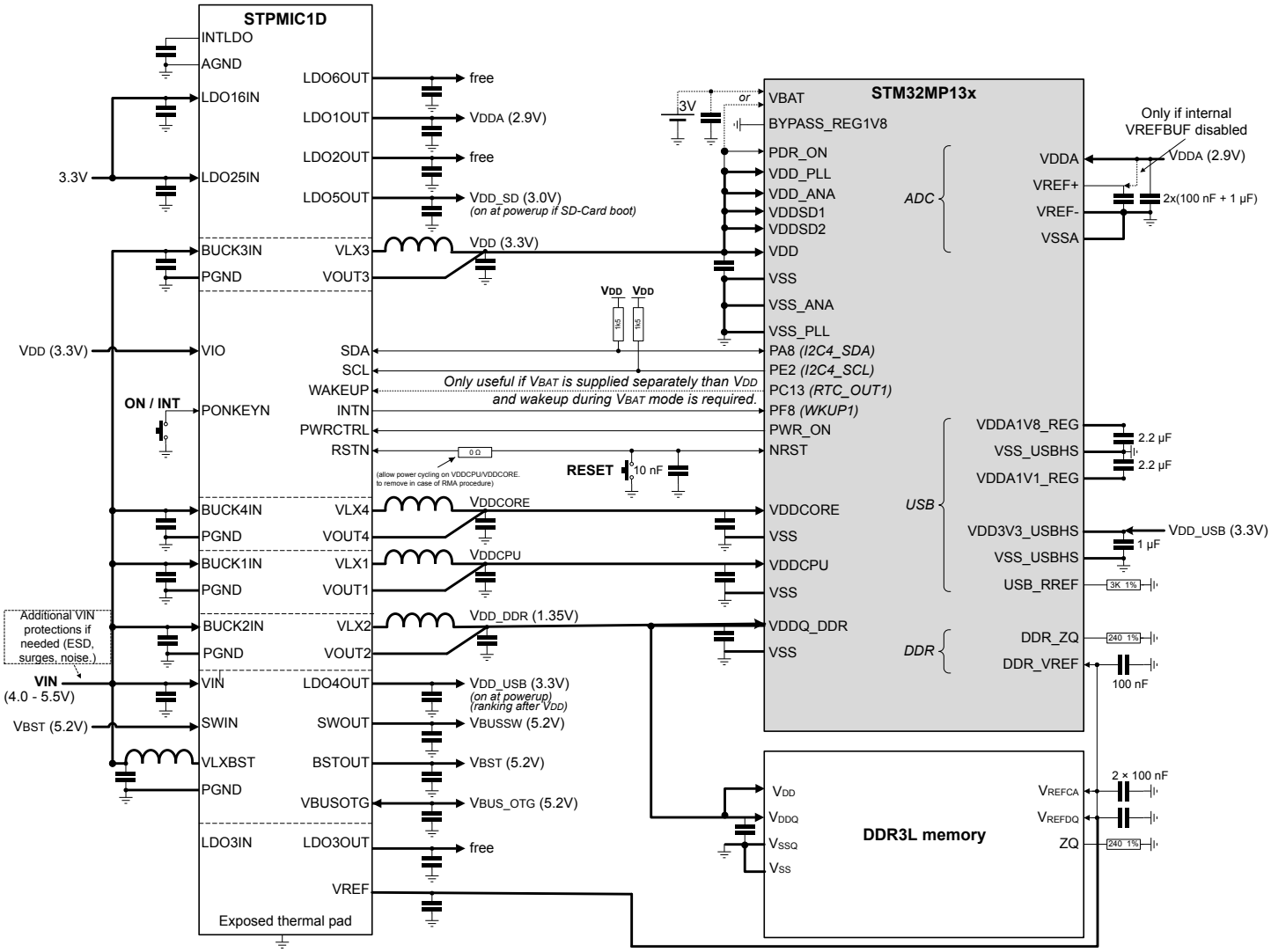
8.5.2 STPMIC1 supply example 3.3 V I/Os with DDR3L

This reference design example targets a complex 3.3V I/Os platform with low-cost DDR3L and high-integration STPMIC1. Usually, all platform components can be powered by the STPMIC1. Full power-supply control is supported thanks to STPMIC1 I²C and side-band signals. The Sleep, Stop, and Standby modes are supported (see STPMIC1 datasheet for more details).

The STPMIC1 automatically applies power cycling on VDDCORE and VDDCPU when nRST is activated (nRST button, exit from Standby, system reset). However, in the case of entering an RMA state, the power cycling should not be done. A 0 Ω resistance between STM32MP13x nRST and STPMIC1 can be set and removed in case of entering an RMA state.

On a same I²C bus, it is not possible to share I²C devices controlled from both secure and non-secure softwares. For example, a secure software controls STPMIC1 in our standard deliveries and a distinct and securable I²C master is used (I2C3, I2C4, or I2C5 on STM32MP13x).

Figure 23. STPMIC1 supply example 3.3 V I/Os with DDR3L

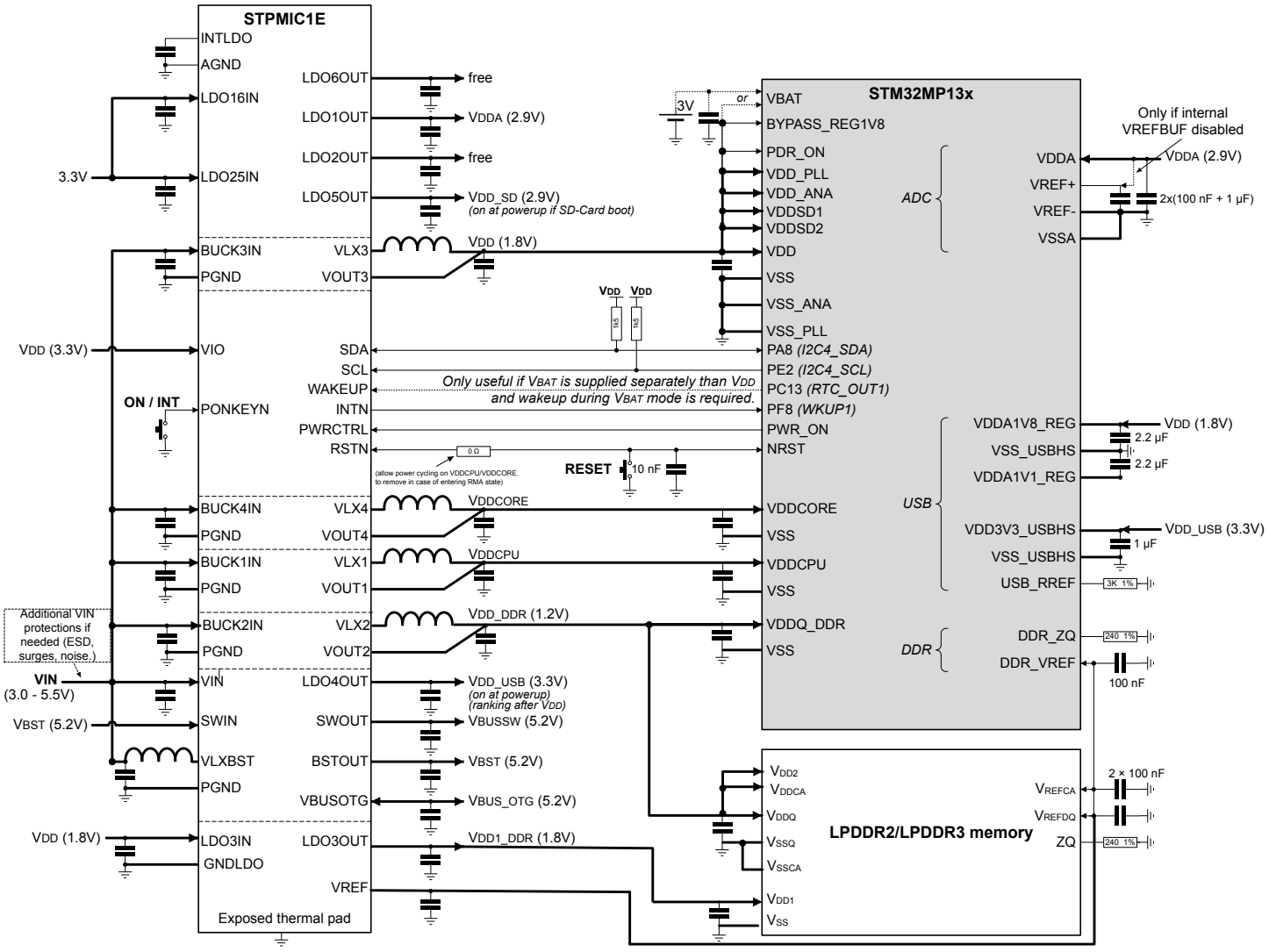


Note: BUCK1 and BUCK4 default values are 1.2 V. This value allows the product to boot at low frequency. Then the software should set the BUCK values to the expected runtime values (Typ is 1.25 V on VDDCORE and VDDCPU).

8.5.3 STPMIC1 supply example 1.8 V I/Os with LPDDR2/LPDDR3

This reference design example targets a complex 1.8 V I/Os platform with low-power LPDDR2/LPDDR3 and high-integration PMIC. Usually, all platform components can be powered by the STPMIC1. The full power-supply control is supported thanks to STPMIC1 I2C and side-band signals. The Sleep, Stop, and Standby modes are supported as well as very-low-power Standby with LPDDR2/LPDDR3 retention (see STPMIC1 datasheet for more details).

Figure 24. STPMIC1 supply example 1.8 V I/Os with LPDDR2/LPDDR3



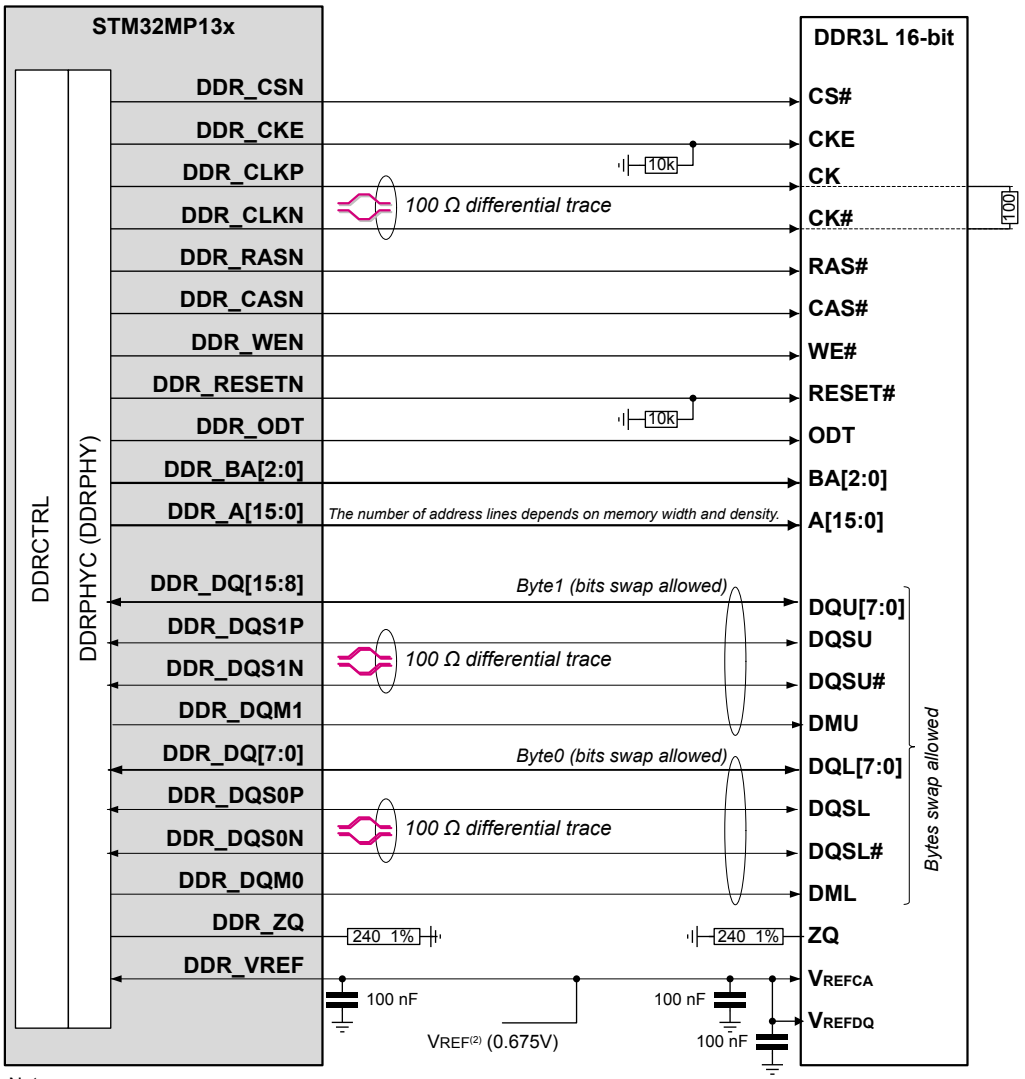
Note: BUCK1 and BUCK4 default values are 1.2 V. This value allows the product to boot at low frequency. Then the software should set the BUCK values to the expected Run time values (Typical is 1.25 V on VDDCORE and VDDCPU).

8.6 DDR3/DDR3L SDRAM

The DDR3 differs from DDR3L only by the supply voltage (1.5 V versus 1.35 V) and VREF level (0.75 V versus 0.675 V). DDR3L has superseded most DDR3 designs.

A 240 Ω, 1% resistor must be connected between DDR_ZQ. Values in the figure below work in most cases, but can be tailored to each side, I/O drive strengths and PCB impedance. Refer to the document [8] for routing examples.

Figure 25. DDR3L 16-bit connection example



Notes:
(1) Supplies and decoupling capacitors not shown.

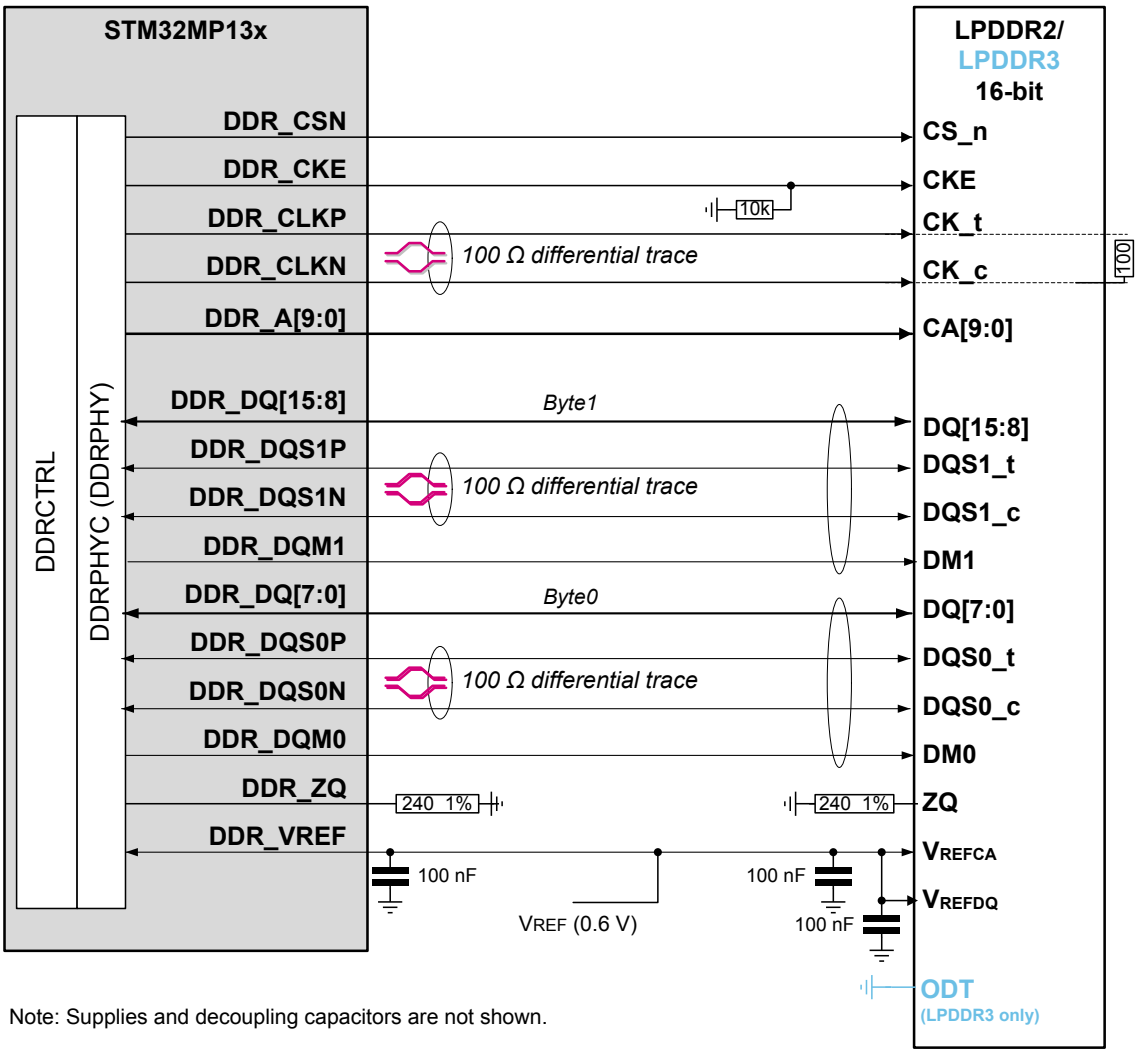
(2) Alternatively, to ease routing and avoid long VREF lines, V_{REF} can be generated locally by a 1 KΩ /1KΩ, 1% resistor divider on VDDQ close to each VREF pins.

Detailed routing examples are described in [8].

8.7 LPDDR2/3 SDRAM

A resistor (240 Ω, 1%) must be connected between DDR_ZQ and VSS. This resistor must not be shared with one or more ZQ resistors required on the LPDDR2 or LPDDR3 components. Refer to the document [8] for routing examples.

Figure 26. LPDDR2/LPDDR3 16-bit connection example



Note: Supplies and decoupling capacitors are not shown.

Detailed routing examples are described in [8].

8.8 SD-Card without external level-shifters

Thanks to the V_{DDSDx} dedicated power supplies, the UHS-I faster modes can be used without the need for external level-shifters. The UHS-I faster modes are up to SDR50 and DDR50, 50 Mbytes/s bus speed. For these modes, the user must switch to 1.8 V the VDDSDx I/Os voltage (SD-card is started with 3 V card I/Os).

Note: As boot is always done in "Standard" mode (3 V I/Os). If the card is used by the application in UHS-I, a power cycle on the card supply is required after reset or Standby.

This example is independent of MPU I/O voltage V_{DD}, that can be between 1.71 V and 3.6 V. In the case when V_{DD} is at 1.8 V Typ, V_{DDSDx} should be supplied with a voltage compatible with the SD-Card start transaction at "Standard" mode (2.7 V-3.6 V) during those starting phases.

Note: A good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DD} voltage.

When using V_{DD} = 1.8 V, the following settings might be required to ensure the best speed on pads used on the SDMMC output:

- a setting in the OTP bit product_below_2v5
- either a setting in the register SYSCFG_HSLVEN4R (HSLVEN_SDMMC1 bit) or a setting in the register SYSCFG_HSLVEN5R (HSLVEN_SDMMC2 bit)
- or a setting in both registers above at the same time

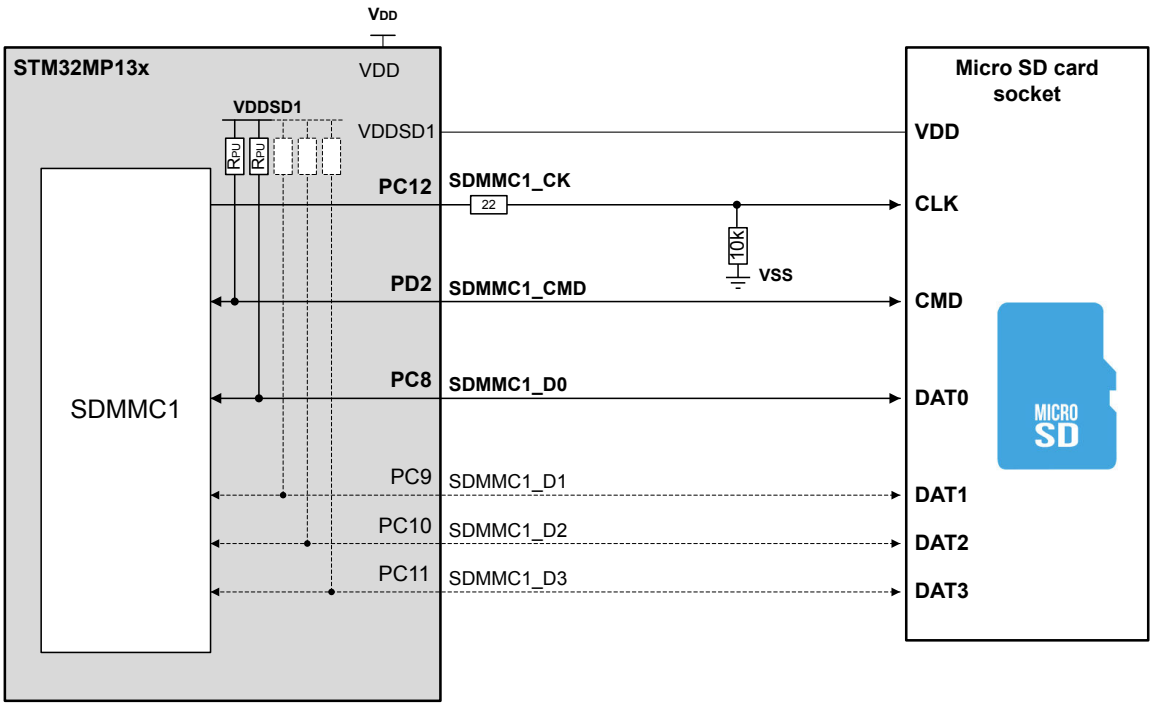
Warning: *HSLVEN must not be set when V_{DD} is above 2.7 V, otherwise permanent device damage may occur.*

If needed, the impedance-matching resistor must be placed as close as possible of the output driver pin. Values in the example below work in most cases, but can be tailored to I/O drive strengths and PCB impedance.

Before V_{DD_SD} shutdown (for example before Standby), all signals going to the card must be set to 0 or high-z by the SDMMC1 driver.

A connection example where UHS-I SD card mode is not used is shown in the figure below.

Figure 27. SD card without external level shifter example (no UHS-I mode connection)



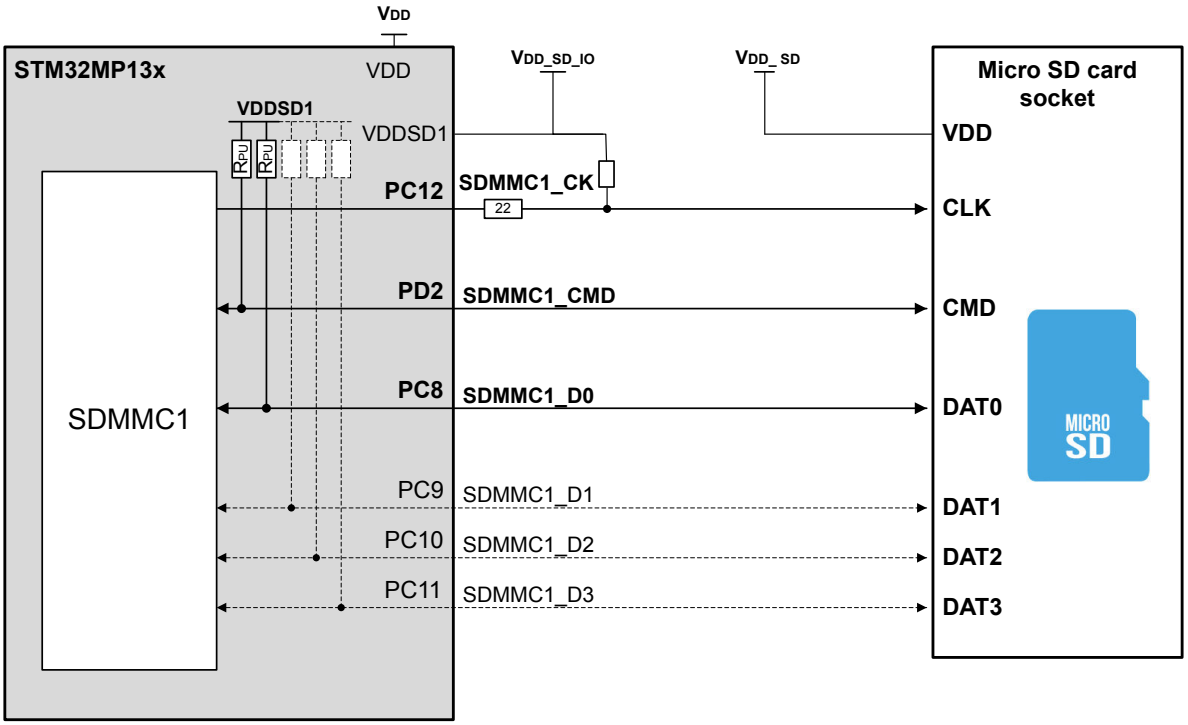
Notes: - **Bold** and plain lines: default pins and minimum set of signals required by low-level boot ROM during SD card boot.
- Traces must be short with balanced length.

If V_{DD} = 3.3 V, VDD_SD can be connected to V_{DD} to save a power supply source.

If V_{DD} = 1.8 V, VDD_SD should be supplied from an external power source with voltage compatible with the SD-card standard (2.7 V - 3.6 V).

When UHS-I SD-Card mode is used, the SDMMC1 (or SDMMC2) pad ring section must be supplied with a dedicated power supply (VDD_SD_IO). Software must be able to change this supply from V_{DD_SD} to 1.8 V when in UHS-I mode. The corresponding voltage supply is V_{DDSD1} for SDMMC1 (or V_{DDSD2} for SDMMC2). A possible connection is shown in the figure below.

Figure 28. SD card without external level shifter example (UHS-I mode connection)



Notes: **- Bold** and plain lines: default pins and minimum set of signals required by low-level boot ROM during SD card boot.
- Traces must be short with balanced length.

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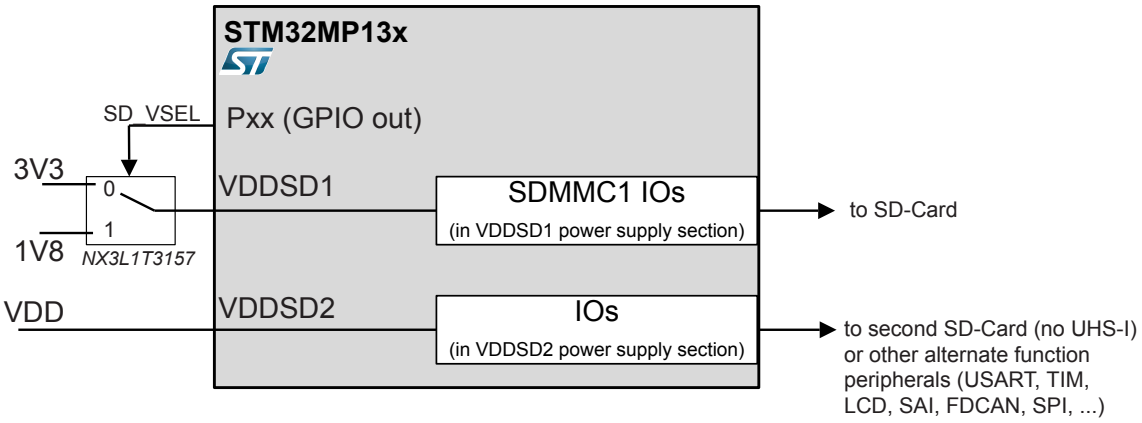
Same examples apply to the SDMMC2 interface, using PB3, PB4, PB14, PB15, PE3, and PG6 GPIOs.

Note: When the product should boot from the SD-Card using UHS-I mode, the STPMIC1 default configuration must be updated during production. This configuration must be set to allow two regulators to be available at 3.3 V.

It is possible to use and external switch (1.8 V, 3.3 V) programmed by a GPIO to supply the V_{DDSDx} power pin. Saving one programmable regulator (see figure below).

Figure 29. Using external power switch to supply VDDSDx



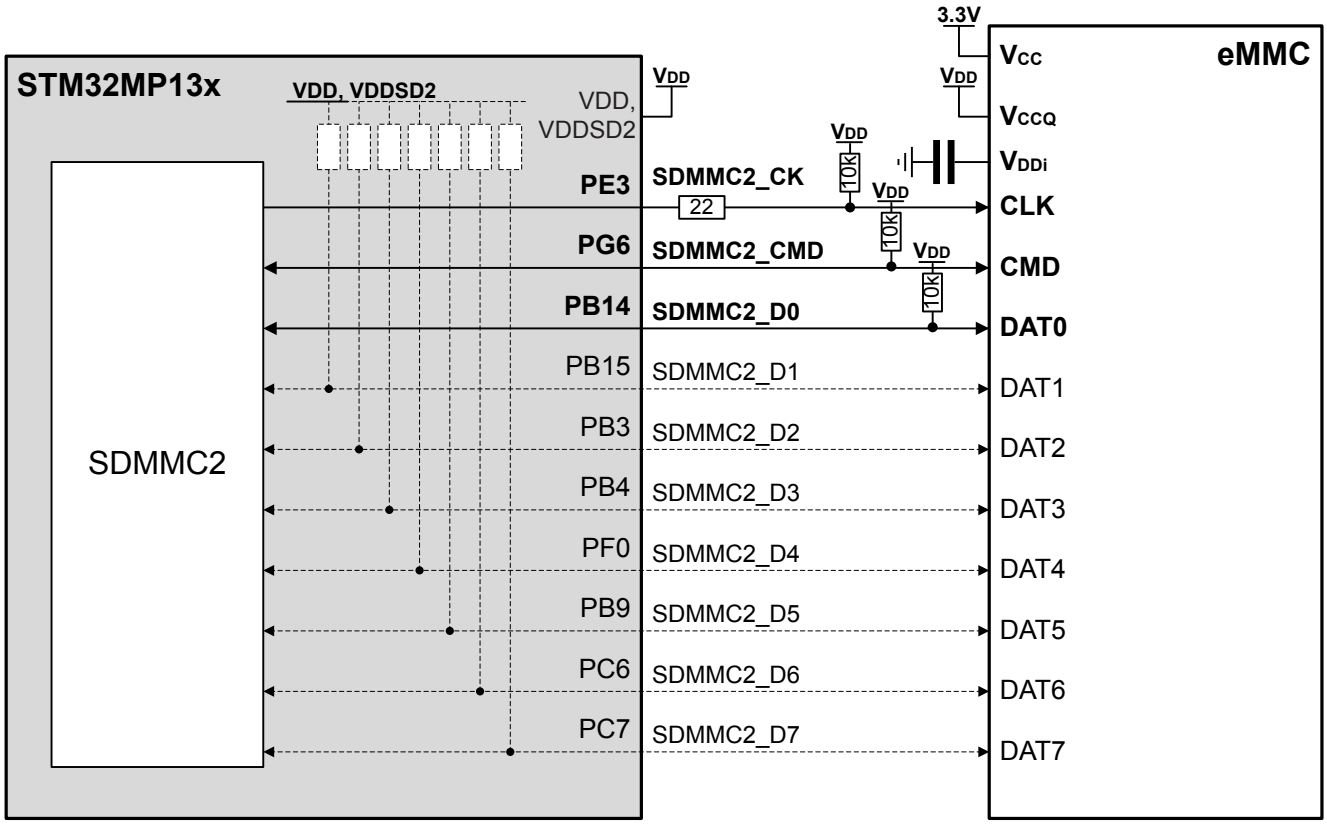
8.9 eMMC Flash

Note: A good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DD} voltage.

When using V_{DD} = 1.8 V, the following settings might be required to ensure the best speed on the pads used on the SDMMC outputs:

- a setting in the OTP bit product_below_2v5
- either a setting in the register SYSCFG_HSLVEN4R (HSLVEN_SDMMC1 bit) or in the register SYSCFG_HSLVEN5R (HSLVEN_SDMMC2 bit)
- a setting in both registers mentioned above.

Figure 30. eMMC connection example



Notes: **- Bold** and plain lines: default pins and minimum set of signals required by low-level boot ROM during eMMC boot.
- Traces must be short with balanced length. Decoupling capacitors are not shown.
- In this mode, VDD and VDDSD2 are tied together.

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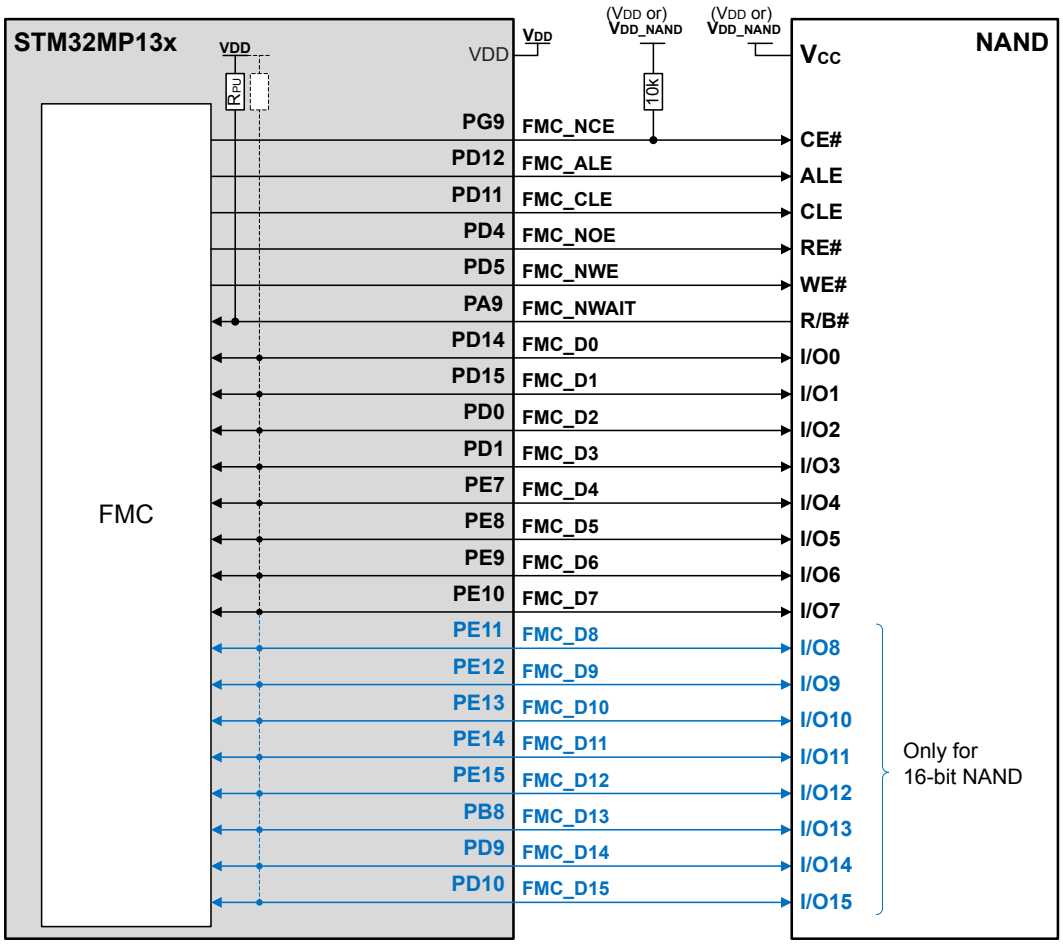
8.10 SLC NAND Flash

The single 8- or 16-bit SLC NAND memory device and two independent 8-bit SLC NAND memory devices are supported:

- single 8- or 16-bit SLC NAND memory device = CE# = FMC_NCE
- independent 8-bit SLC NAND memory devices = device1 CE# = FMC_NCE and device2 CE# = FMC_NCE2.

Note: Boot is only done on the SLC NAND memory device connected to FMC_NCE.

Figure 31. SLC NAND-Flash connection example



Notes: **- Bold** and plain lines: default pins and minimum set of signals required by low-level boot ROM during NAND boot.
- Traces must be short with balanced length. Decoupling capacitors are not shown.
- V_{DD_NAND} must be cut for > 1 ms in order to allow reboot (on reset or Standby exit).
Schematic for 16-bit NAND only.

Note: Only single-level cell (SLC) NAND-Flash is supported. It is supported with either Hamming, BCH4 or BCH8 error correction algorithms.

8.11 Serial NOR/NAND Flash

As boot is always done in SPI mode. A power cycle on serial Flash supply is required after reset or standby exit if:

- the application sets the serial Flash memory in multiple data lines
- or if the sector addressing has been changed.

Note: A good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DD} voltage.

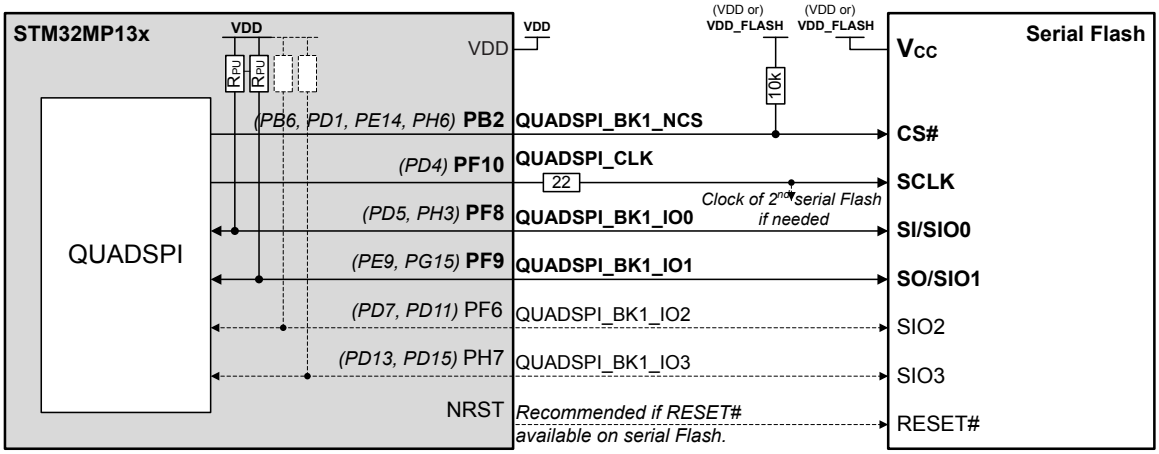
When using V_{DD} = 1.8 V the following settings might be required to ensure the best speed on pads used on QUADSPI outputs:

- a setting in the OTP bit product_below_2v5 and
- setting of the register SYSCFG_HSLVEN1R (HSLVEN_QUADSPI bit).

Warning: *HSLVEN must not be set when V_{DD} is above 2.7 V, otherwise permanent device damage may occur.*

If needed, the impedance-matching resistor must be placed as close as possible of the output driver pin. Values in the example below work in most cases, but can be tailored to the I/O drive strengths and PCB impedance.

Figure 32. Serial Flash connection example



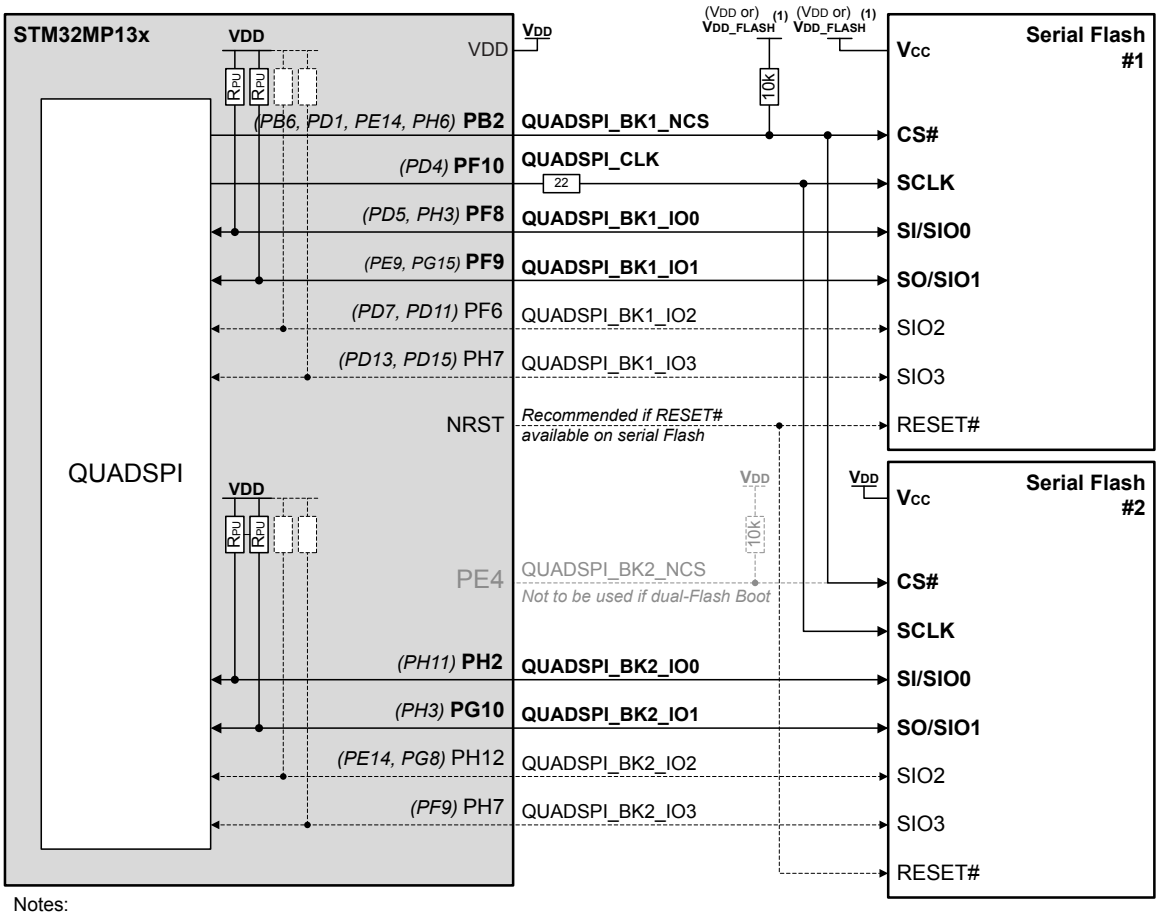
Notes:
- Bold and plain lines: default pins and minimum set of signals required by low-level boot ROM during Serial Flash boot.
- Decoupling capacitors are not shown.
- V_{DD_FLASH} must be cut for > 1 ms in order to allow reboot (on reset or Standby exit).
- During SPI mode boot using SI/SO, some serial memories could use IO2 and IO3 pins as additional feature like HOLD. In order to make this kind of device able to boot, it might be necessary to set those pins to inactive level by adding external pull-ups or by defining internal pull-up during Boot using OTP.

In the case of a blank or a corrupted serial Flash memory, the boot ROM tries to boot from the single serial Flash memory. After this, the boot ROM tries the dual-serial Flash mode, which means that PH2 and PG10 might conflict with the signals used on the board. If needed, this conflict on PH2 and PG10 is avoided by programming OTP (words 3, 5, 6, and 7). This programming forces the boot ROM to use only the four pins needed in the single serial Flash configuration.

QUADSPI serial Flash memory may boot either from dedicated GPIOs or using some FMC Nand8 boot GPIOs (PD4, PD1, PD5, PE9, PD11, PD15) in order to allow the same footprint usage on board for both type of Flash memory. In such case, the STM32MP13x default boot pin NVM should be reprogrammed during the production phase.

Also, the NAND configuration can be setup using OTP (word 9) for device page and block size.

Figure 33. Dual-serial Flash connection example



Notes:
- Bold and plain lines: default pins and minimum set of signals required by low-level boot ROM during dual-serial Flash boot.
- Decoupling capacitors are not shown.
- V_{DD_FLASH} must be cut for > 1 ms in order to allow reboot (on reset or Standby exit).
- During SPI mode boot using SI/SO, some serial memories could use IO2 and IO3 pins as additional feature like HOLD. In order to make this kind of device able to boot, it might be necessary to set those pins to inactive level by adding external pull-ups or by defining internal pull-up during Boot using OTP

If the memory I/O power supply can be shut down independently of V_{DD}, NRST must not be directly connected to the memory reset pin. Also, the following options can be used:

- memory reset pin left open if the memory has an internal POR (power-on reset)
- memory reset pin connected through a Schottky diode with the cathode on the NRST side

Otherwise, the NRST can be pulled-low by memory internal protections when its I/O supply is not present. This may cause an unwanted platform reset.

Refer to the memory documentation for details on the memory reset pin requirements (especially, the presence of internal power-on reset and/or internal pull-up on the RESET pin).

8.12 USB

Note: *USB Type-C™ is supported with some external component.*

A resistor (3 kΩ, 1%) must be connected between USB_RREF and VSS_USBHS (or VSS, if VSS_USBHS is not available on the selected package).

Figure 34. USB two-ports host high speed

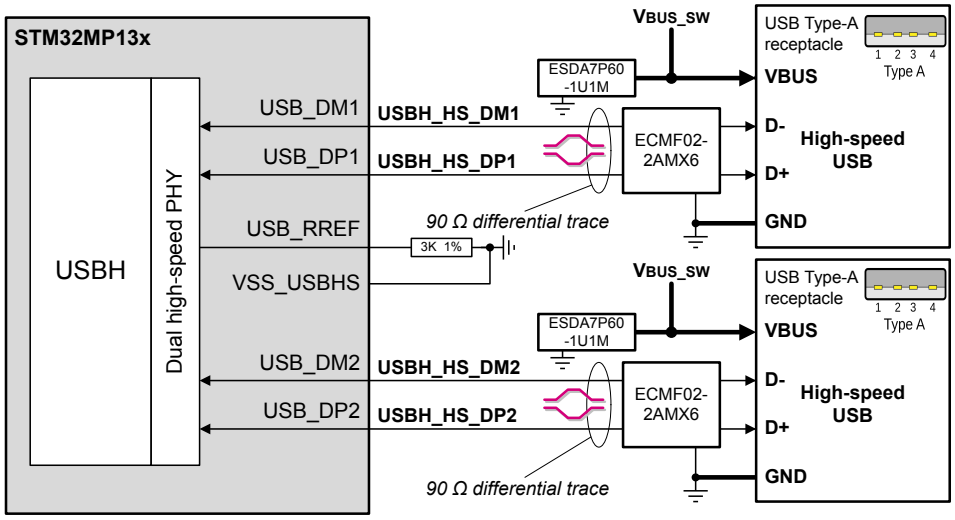
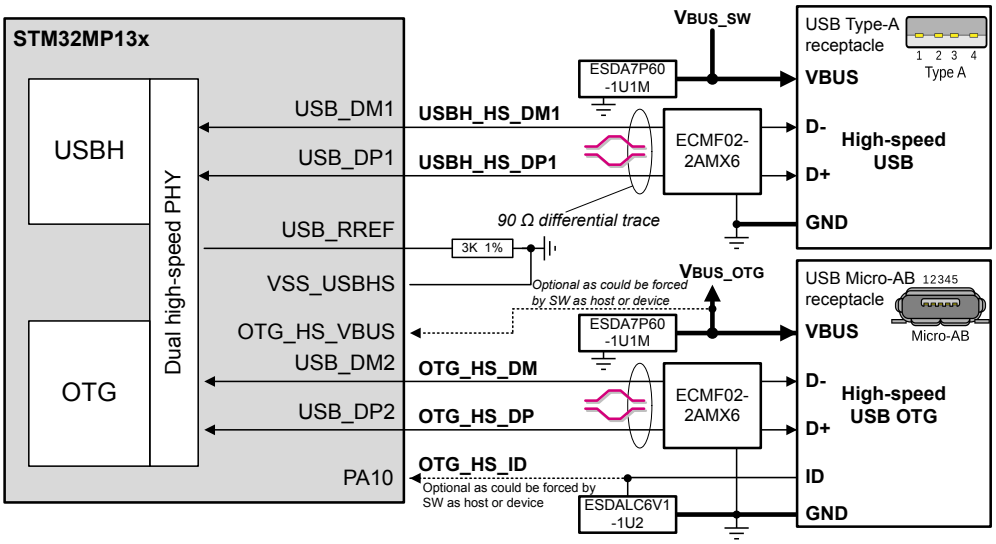


Figure 35. USB host high-speed + OTG high-speed connection example



Note: On the OTG peripheral, the USB high speed is also supported with the Micro-B receptacle instead of Micro-AB and leaving the OTG_ID pin unconnected.

Note: The use of the OTG_HS_VBUS signal may prevent USB certification in some cases. This is due to the USB_DPx pin pull-up being activated before the availability of the OTG_HS_VBUS signal. Also the OTG_HS_VBUS GPIO electrical characteristic requires to have V_{DD} present before OTG_HS_VBUS, which is not always the case, for example during a device attach to a host. Refer to the document [11].

As a result it is recommended to use a GPIO with some resistor bridge with an EXTI interrupt on this GPIO connected to the external USB VBUS signal. It is also recommended to do the same with the OTG_HS_ID signal (use a GPIO+EXTI connected to the external USB ID signal). Refer to the document [11] for implementation details. With this workaround, an additional wake up from low-power mode feature is possible thanks to the EXTI on both VBUS and ID USB signals.

The OTG_HS_VBUS and OTG_HS_ID signals are already available on some GPIOs. It is then possible to use these GPIOs with their associated EXTI, or use any other GPIOs. OTG_HS_VBUS is on PI7 (EXTI7) and OTG_HS_ID is on PA10 (EXTI10).

USB high-speed PCB track length matching

The USB (and also DDR) differential pair length matching is done considering the package and board layout. The inner ball connection length is smaller in the package. Thus, a longer connection at board level is preferred and is already considered inside the package.

The figure below shows four differential pairs with wire length already matched inside the package. It means that there is no need to compensate on the board for the differences in length due to inner- versus outer-row ball position.

Figure 36. USB high-speed PCB track example

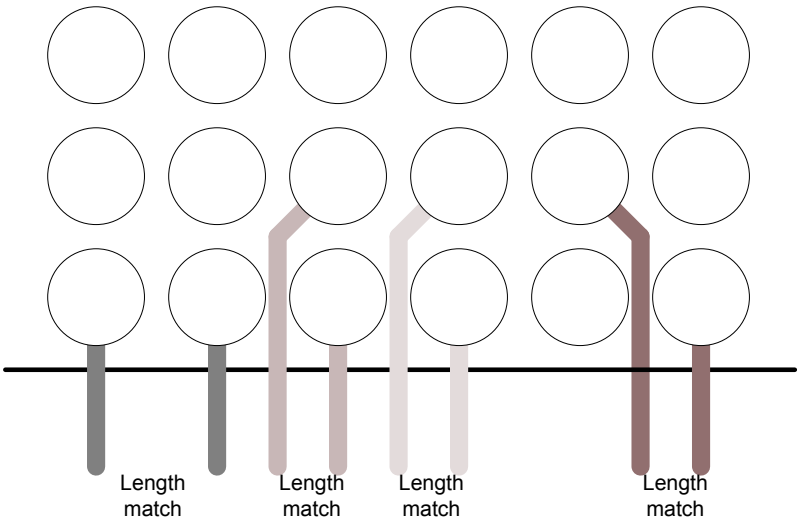


Table 15. USB high-speed PCB routing recommendations

Recommendation	Min	Typ	Max	Unit
Differential impedance	76.5	90	103.5	Ω
Single-ended impedance	38.25	45	51.75	Ω
Length matching within a pair (including package)	-50	-	+50	mils
	-1.27	-	+1.27	mm
Max traces length (up to connector or first active component)	-	-	8	inches
	-	-	203	mm
Max number of vias (recommended value)	-	-	2	-
Distance between any differential trace and other signals	S-2S	S-3S or more		-(1)
Do not route over power plane split. No subs (point to point only). No right angles.				

1. *Definition can be found in the application note DDR memory routing guidelines (AN5692).*

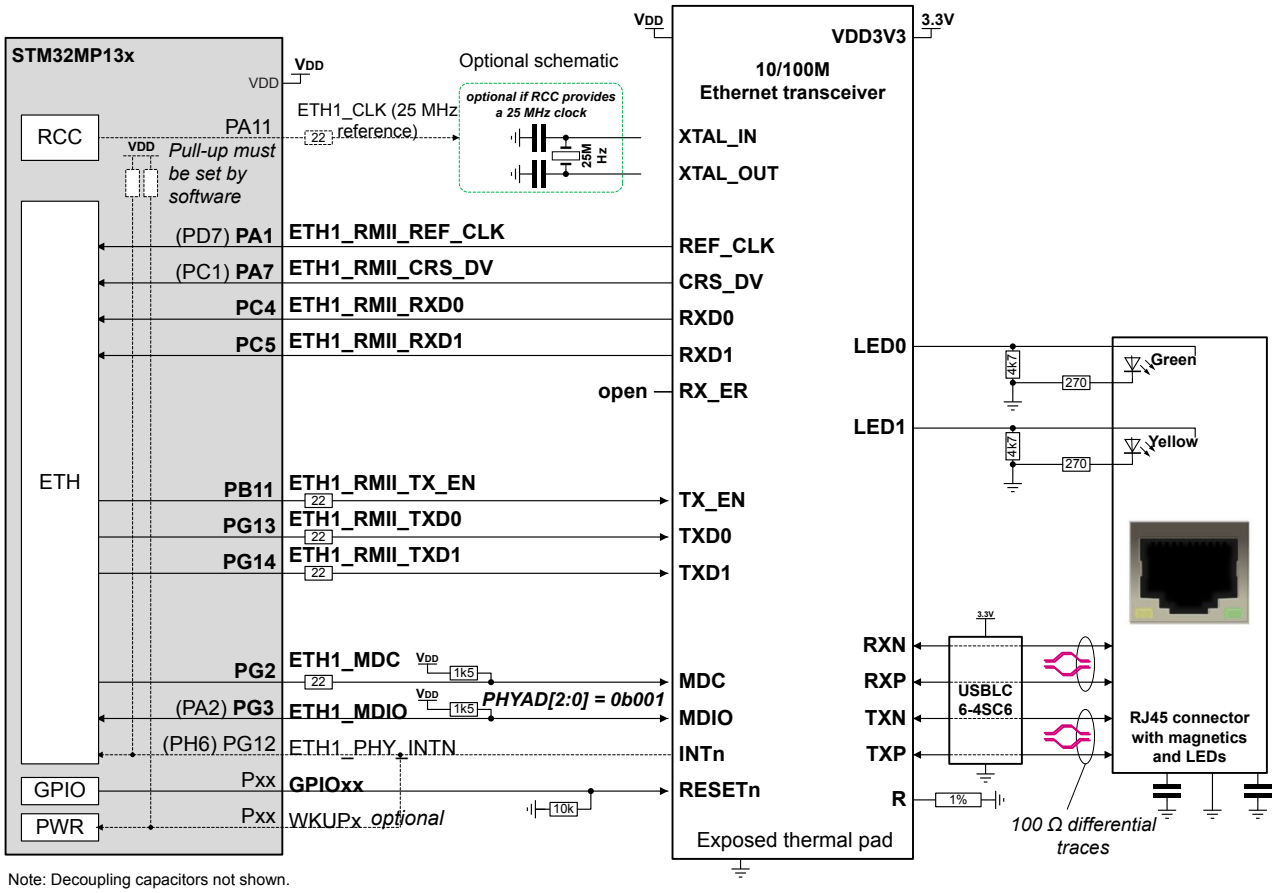
8.13 Ethernet

8.13.1 10/100 M Ethernet

Note: A good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers), and V_{DD} voltage.

If needed, the impedance matching resistors must be placed as close as possible of the output driver pin. Values in the example below works in most cases, but can be tailored to each side I/O drive strengths and PCB impedance.

Figure 37. 10/100 M Ethernet PHY connection example



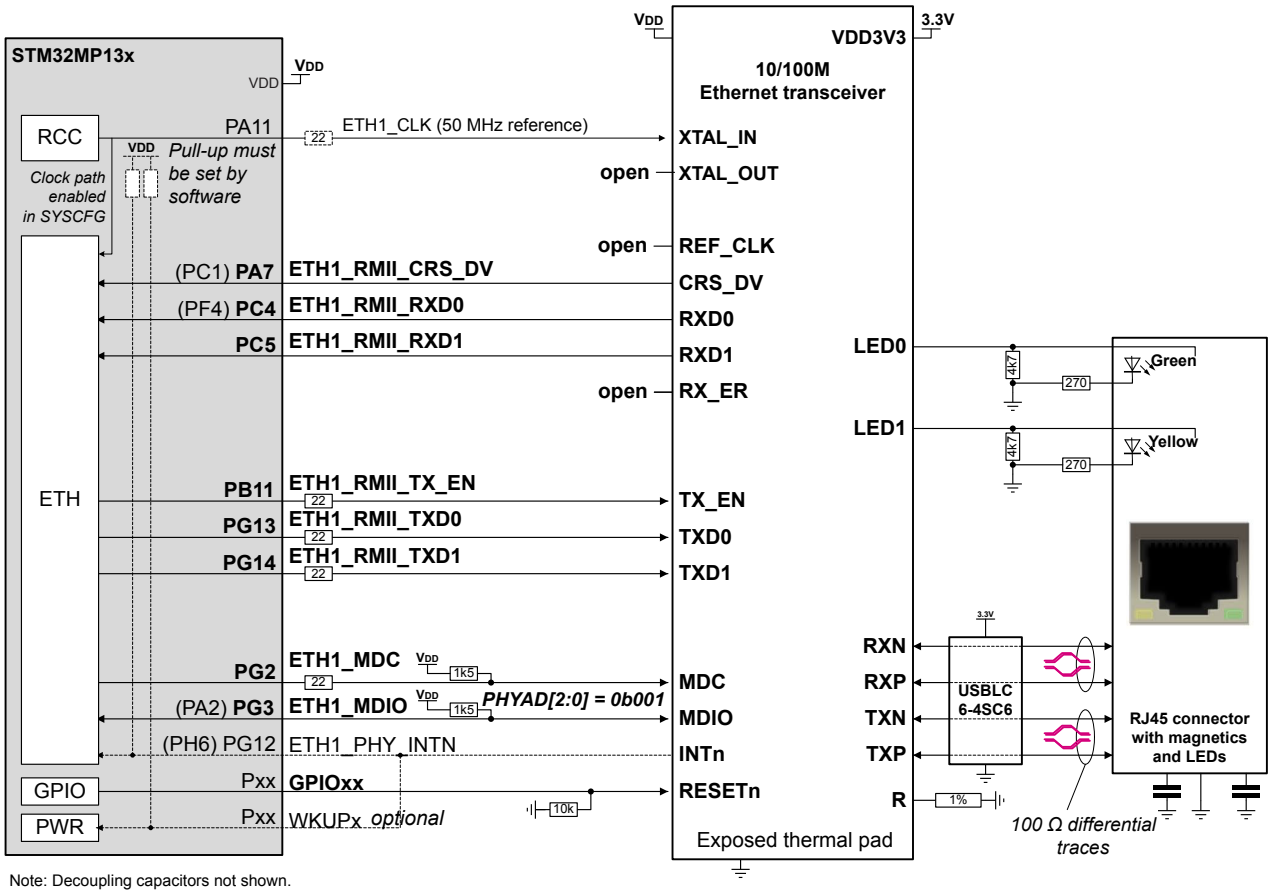
Note: Decoupling capacitors not shown.

The RCC cannot provide the 25 MHz reference clock to the PHY during low-power modes. So, the dedicated 25 MHz crystal is required on the PHY in case that a wake-up on LAN (WOL) is needed for the platform. Setting the RCC PLLs to get 25 MHz output for PHY clocking could constrain other RCC frequencies. In that case, it is more flexible to put a dedicated 25 MHz crystal on the PHY.

Alternatively, if PHY allows it and if the RCC can provide a precise 50 MHz clock, a 50 MHz ETH_CLK can be provided by the STM32MP13x device to the PHY. In this case, the REF_CLK is left unconnected on both sides. This saves BOM and area, as well as some power on some PHYs.

Note: To check if RCC can provide a precise 50 MHz clock (if PHY allows it), it must be done in respect to the HSE quartz frequency and the RCC other peripheral/core clocks frequency settings.

Figure 38. 10/100M Ethernet PHY connection example (with REFCLK from RCC)



Note: Decoupling capacitors not shown.

As the RCC cannot provide the 50 MHz reference clock to the PHY during low-power modes, this option is not possible in case wake-up on LAN (WOL) is needed for the platform. Setting the RCC PLLs to get 50 MHz output for PHY clocking could constrain other RCC frequencies. In that case, this option is not possible.

In the case of dual-Ethernet interfaces (ETH1, ETH2), the XTAL_IN clock of each Ethernet transceiver can be connected to either ETH1_CLK or ETH2_CLK.

8.13.2 Gigabit Ethernet

Note: A good signal integrity is dependent on board, GPIO strength settings (GPIO_OSPEEDR registers) and V_{DD} voltage.

When using V_{DD} = 1.8 V, a setting in the OTP bit product_below_2v5 and the register SYSCFG_HSLVEN2R (HSLVEN_ETH1 bit) and/or SYSCFG_HSLVEN3R (HSLVEN_ETH2 bit), is required to ensure the best speed on pads used on Ethernet outputs.

Warning: *HSLVEN must not be set when V_{DD} is above 2.7 V, otherwise permanent device damage may occur.*

If needed, the impedance matching resistors must be placed as close as possible of the output driver pin. Values in the example below works in most cases, but can be tailored to each side I/O drive strengths and PCB impedance.

As the RCC cannot provide the 25 MHz reference clock to the PHY during low power modes, the dedicated 25 MHz crystal is required on the PHY in case wakeup on LAN (WOL) is needed for the platform.

Setting the RCC PLLs to get 25 MHz output for PHY could constrain other RCC frequencies. In that case, it is more flexible to put a dedicated 25 MHz crystal on the PHY.

Figure 39. Gigabit Ethernet PHY connection example (with V_{DD} = 3.3 V, RTL8211E)

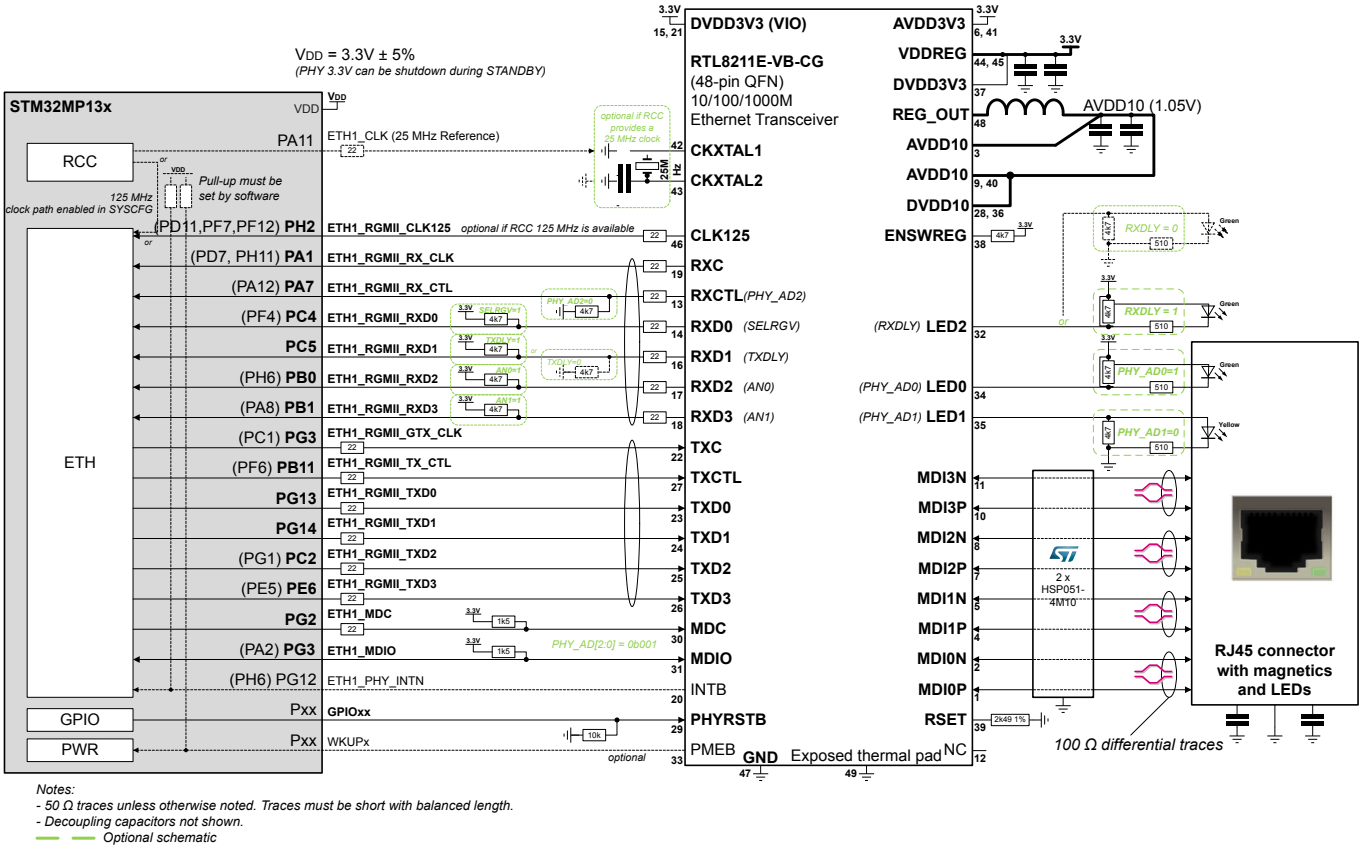
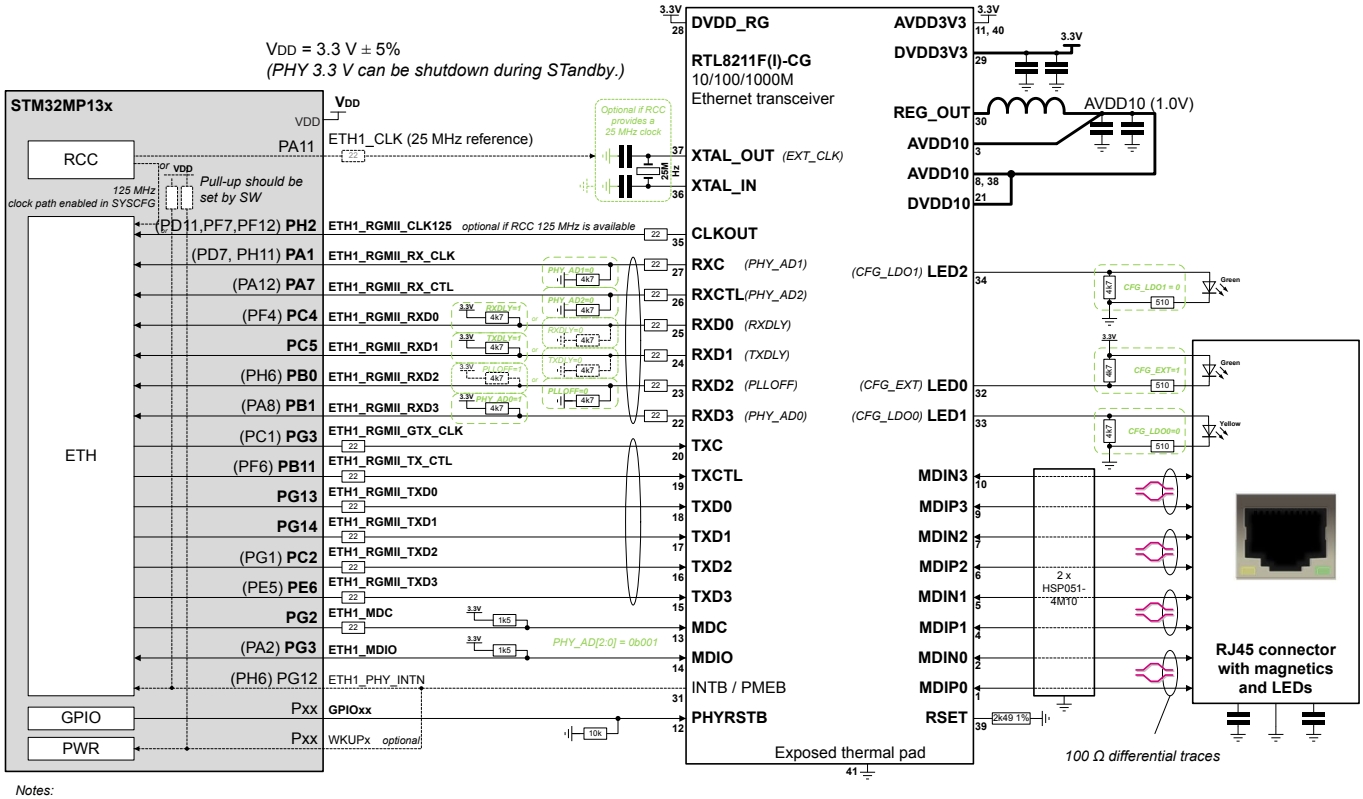
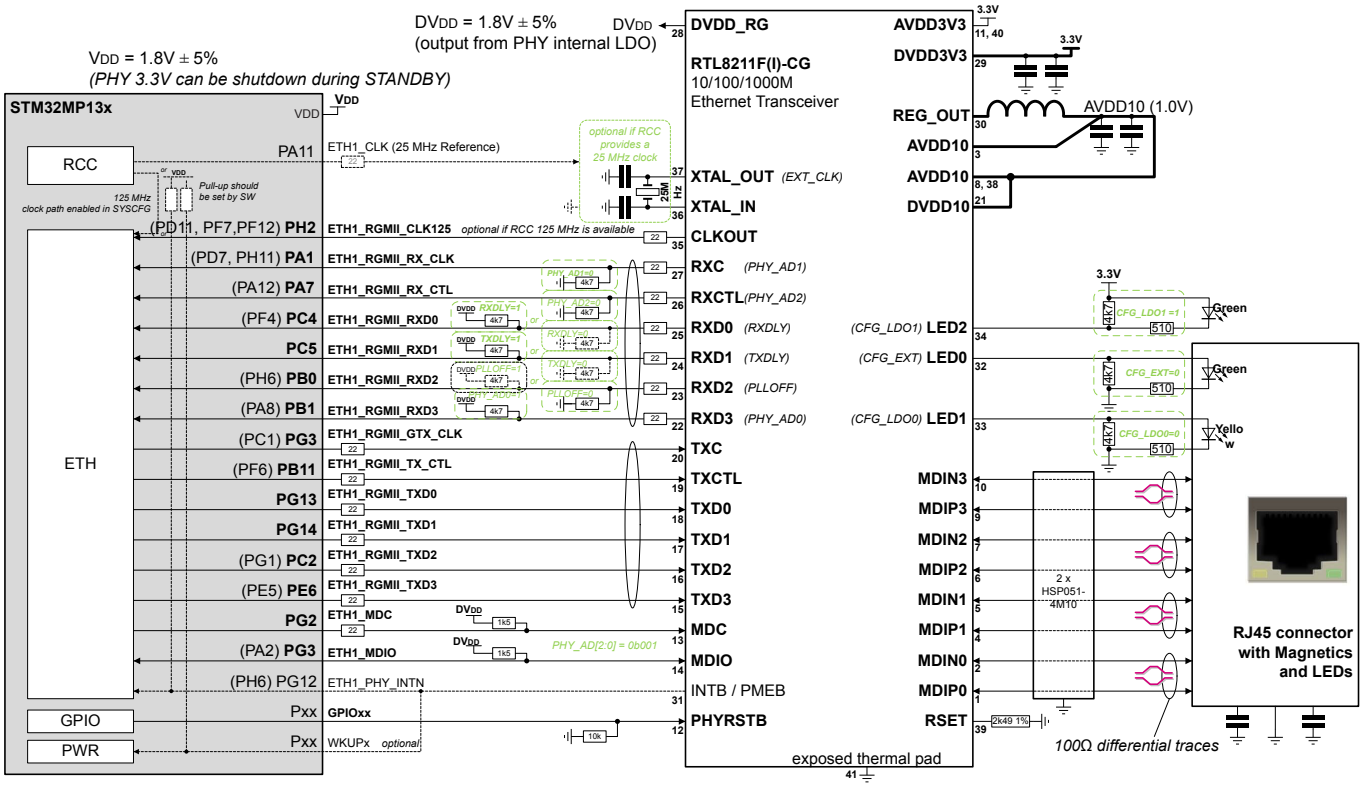


Figure 40. Gigabit Ethernet PHY connection example (with V_{DD} = 3.3 V, RTL8211F)



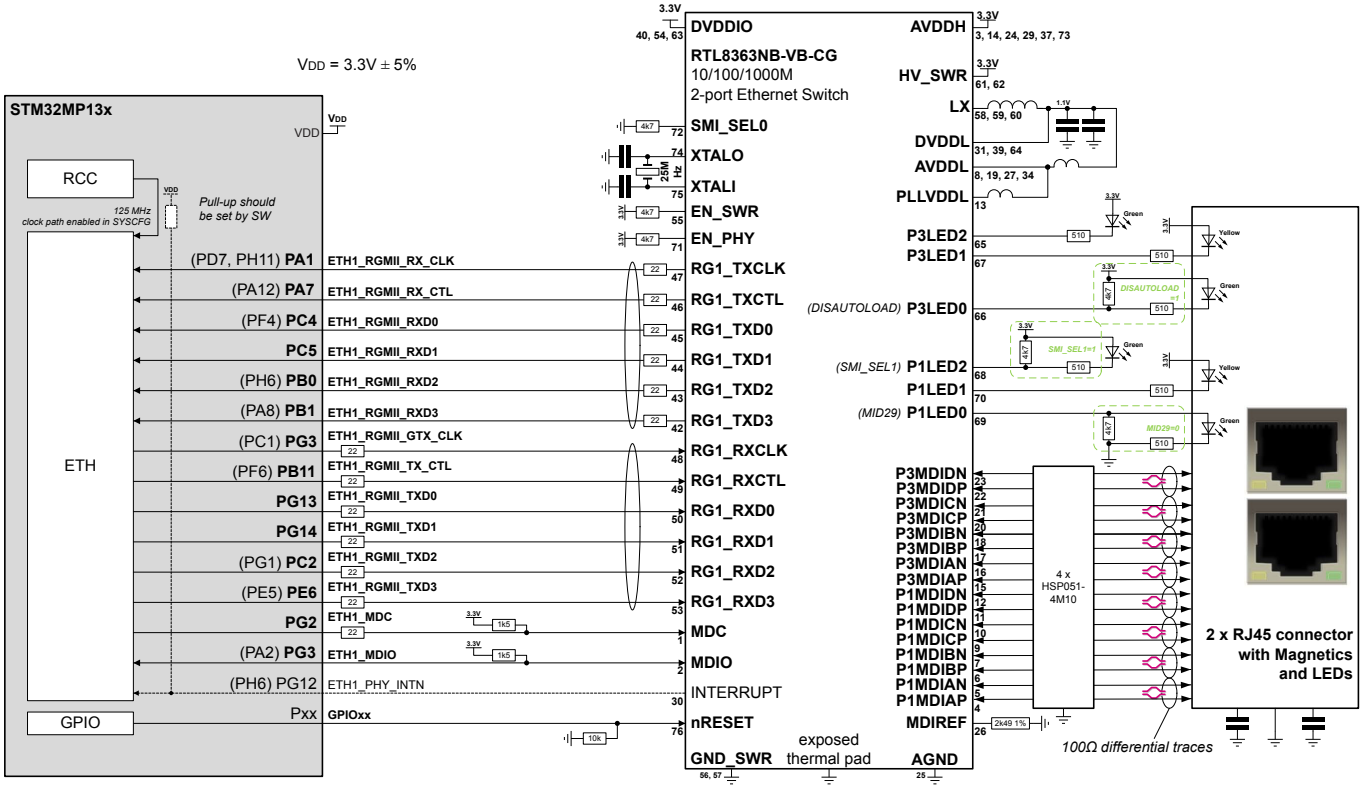
Notes:
- 50 Ω traces unless otherwise noted. Traces must be short with balanced length.
- Decoupling capacitors not shown.
— — — Optional schematic

Figure 41. Gigabit Ethernet PHY connection example with V_{DD}=1.8 V (RTL8211F)



Notes:
- 50 Ω traces unless otherwise noted. Traces must be short with balanced length.
- Decoupling capacitors not shown.
— — — Optional schematic

Figure 42. **Gigabit Ethernet 2-port switch example with V_{DD} = 3.3 V (RTL8363NB-VG)**



Notes:
- 50 Ω traces unless otherwise noted. Traces must be short with balanced length.
- Decoupling capacitors not shown.
— — — Optional schematic

Revision history

Table 16. **Document revision history**

Date	Revision	Changes
13-Feb-2023	1	Initial release
23-Jun-2023	2	Updated: • Section 8.1 Clock • Figure 28 • Table 2. Reference documents

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