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DOCUMENT DESCRIPTION

Schematic Checklist for the LAN7801, 64-pin SQFN Package

Microchip
80 Arkay Drive, Suite 100
Hauppauge, New York 11788

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Schematic Checklist for LAN7801

Information Particular for the 64-pin SQFN Package

RGMII Interface:

1. The following table indicates the proper connections for the 14 RGMII signals.

From:	Connects To:	
LAN7801 SQFN	**RGMII Phy Device**	**Notes**
RXD0 (pin 14)	RXD<0>	
RXD1 (pin 15)	RXD<1>	
RXD2 (pin 16)	RXD<2>	
RXD3 (pin 17)	RXD<3>	
RXD4	RXD<4>	Not Used in RGMII Mode
RXD5	RXD<5>	Not Used in RGMII Mode
RXD6	RXD<6>	Not Used in RGMII Mode
RXD7	RXD<7>	Not Used in RGMII Mode
RX_CTL (pin 13)	RXCTRL	
RX_DV	RX_DV	Not Used in RGMII Mode
RX_ER	RX_ER	Not Used in RGMII Mode
RXC (pin 12)	RX_CLK	
TX_ER	TX_ER	Not Used in RGMII Mode
TXD0 (pin 8)	TXD<0>	
TXD1 (pin 6)	TXD<1>	
TXD2 (pin 5)	TXD<2>	
TXD3 (pin 4)	TXD<3>	
TXD4	TXD<4>	Not Used in RGMII Mode
TXD5	TXD<5>	Not Used in RGMII Mode
TXD6	TXD<6>	Not Used in RGMII Mode
TXD7	TXD<7>	Not Used in RGMII Mode
TX_CTL (pin 9)	TXCTRL	
TX_EN	TX_EN	Not Used in RGMII Mode
TXC (pin 10)	TX_CLK	
GTXCLK	GTX_CLK	Not Used in RGMII Mode
CRS	CRS	Not Used in RGMII Mode
COL	COL	Not Used in RGMII Mode
MDIO (pin 55)	MDIO	
MDC (pin 56)	MDC	

2. Provisions should be made for series terminations for all outputs on the RGMII Interface. Series resistors will enable the designer to closely match the output driver impedance of the LAN7801 and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors might be 10.0 Ω.

3. REFCLK_25 (pin 61), this output pin of the LAN7801 can be used as a reference clock to the external Gigabit Ethernet Phy. Must be enabled (set) in the HARDWARE CONFIGURATION REGISTER (HW_CFG).

4. CLK125 (pin 19), an external 125 MHz clock can be supplied to this input pin of the LAN7801 in order to generate the internal RGMII TX clock. If this pin is not used, it should be tied low with a 10K ohm pull-down. In this case, if the 125 MHz is not supplied, the LAN7801 can generate it's own 125 MHz internally. This functionality must be enabled (set) in the HARDWARE CONFIGURATION REGISTER (HW_CFG).

5. DUPLEX (pin 33), this input pin of the LAN7801 connects to the Duplex Mode output pin from the external Phy. When asserted, the partner PHY is in Full Duplex mode. If the partner PHY does not have a duplex output signal then it is recommended that this signal be tied to VDD to force full duplex operation.

6. PHY_INT_N (pin 31), this input pin of the LAN7801 can be used to indicate an interrupt from the external Gigabit Phy.

7. PHY_RESET_N (pin 32), this output pin of the LAN7801 can be used to reset the external Gigabit Phy.

+3.3V Power Supply Connections:

1. The analog supply (VDD33A) pin on the LAN7801 SQFN is pin 50. This pin requires a connection to +3.3V. This pin is the +3.3V analog power supply for the USB 2.0 AFE.

2. The VDD33A pin should also have one .01 µF (or smaller) capacitor to decouple the LAN7801. The capacitor size should be SMD_0603 or smaller.

3. The supply (VDD33_REG_IN) pin for the +2.5V LDO regulator in the LAN7801 SQFN is pin 64. This pin requires a connection to +3.3V.

4. The VDD33_REG_IN pin should also have one .01 µF (or smaller) capacitor to decouple the LAN7801. The capacitor size should be SMD_0603 or smaller.

5. The supply (VDD_SW_IN) pin for the +1.2V switching regulator in the LAN7801 SQFN is pin 21. This pin requires a connection to +3.3V - +2.5V.

6. The VDD_SW_IN pin should also have one .01 µF (or smaller) capacitor to decouple the LAN7801. The capacitor size should be SMD_0603 or smaller.

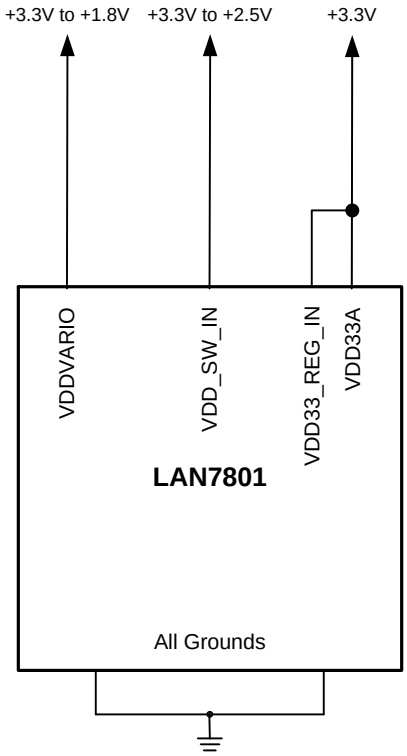


Figure 1 - +3.3V Power Supply Connections

VDDVARIO Power Supply Connections:

1. The VDDVARIO supply pins on the LAN7801 SQFN are 3, 7, 11, 18, 27, 48 & 51. These pins require a connection to +3.3V - +1.8V.

2. Each VDDVARIO pin should also have one .01 μF (or smaller) capacitor to decouple the LAN7801. The capacitor size should be SMD_0603 or smaller.

+2.5V Power Supply Connections:

1. VDD25_REG_OUT (pin 63), this pin is the output pin of the internal +2.5V LDO regulator for the LAN7801.

2. The VDD25_REG_OUT pin should have one .01 μF (or smaller) capacitor to bypass the LAN7801. The capacitor size should be SMD_0603 or smaller.

3. The VDD25_REG_OUT pin also requires a 1.0 uF, low ESR capacitor. The low ESR requirement is to ensure the proper stability of the +2.5V internal regulator of the LAN7801. We recommend a high quality, low ESR, ceramic type capacitor for this particular application. We recommend the ESR not be any higher than 2.0 ohms for frequency ranges from 10 KHz to 1 GHz.

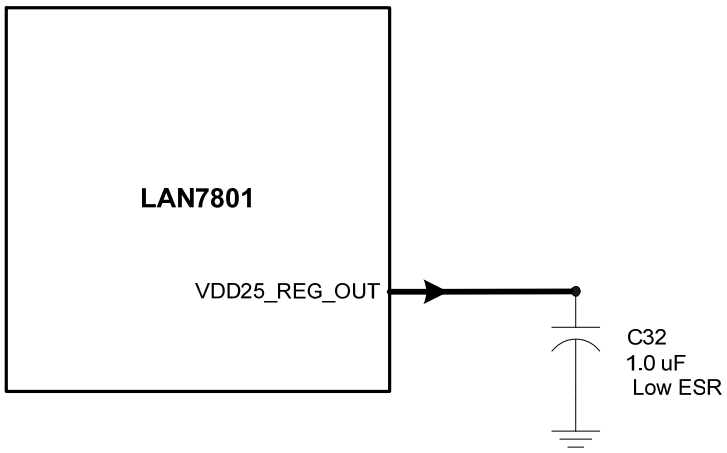


Figure 2 - LAN7801 +2.5V Power Connections

+1.2V Power Supply Connections:

1. VDD12_SW_OUT (pin 20), this pin is the output pin of the internal +1.2V switching regulator for the LAN7801. This pin must be connected directly to a series 3.3 uH inductor.

2. The VDD12_SW_OUT pin / 3.3 uH inductor node in the design should have one .01 μF (or smaller) capacitor to bypass the LAN7801. The capacitor size should be SMD_0603 or smaller.

3. The VDD12_SW_OUT pin / 3.3 uH inductor node also requires a 22 uF, low ESR capacitor. The low ESR requirement is to ensure the proper stability of the +1.2V internal regulator of the LAN7801. We recommend a high quality, low ESR, ceramic type capacitor for this particular application. We recommend the ESR not be any higher than 2.0 ohms for frequency ranges from 10 KHz to 1 GHz.

4. VDD12_SW_FB (pin 22), this pin supplies feedback for the internal +1.2V switching regulator. In this application, this pin should be connected directly to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7801. For applications where the +1.2V internal switching regulator is disabled, simply connect VDD12_SW_FB directly to VDD_SW_IN (pin 21).

5. The VDD12_SW_FB pin should have one .01 μF (or smaller) capacitor to decouple the LAN7801. The capacitor size should be SMD_0603 or smaller.

6. VDD12CORE (pins 28 & 54), these two core input power supply pins may be powered from the internal +1.2V switching regulator. In this application, these two pins should be connected directly to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7801. See figure 3 below for more details. These two pins can also be supplied from an external +1.2V power supply. In this application, the internal +1.2V switching regulator can be disabled.

7. The VDD12CORE pins should each have one .01 μF (or smaller) capacitor to decouple the LAN7801. The capacitor size should be SMD_0603 or smaller.

8. VDD12A (pins 37, 42, & 62), these three pins supply power to the analog blocks (the USB PLL / AFE section) of the LAN7801 from the internal +1.2V switching regulator through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. A 1.0 uF, low ESR cap is required on the pin 37, 42, & 62 side of the ferrite bead. In this application, the ferrite bead should be connected to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7801. See figure 3 below for more details. These three pins can also be supplied from an external +1.2V power supply. In this application, the internal +1.2V switching regulator can be disabled.

9. The VDD12A pins should each have one .01 μF (or smaller) capacitor to decouple the LAN7801. The capacitor size should be SMD_0603 or smaller.

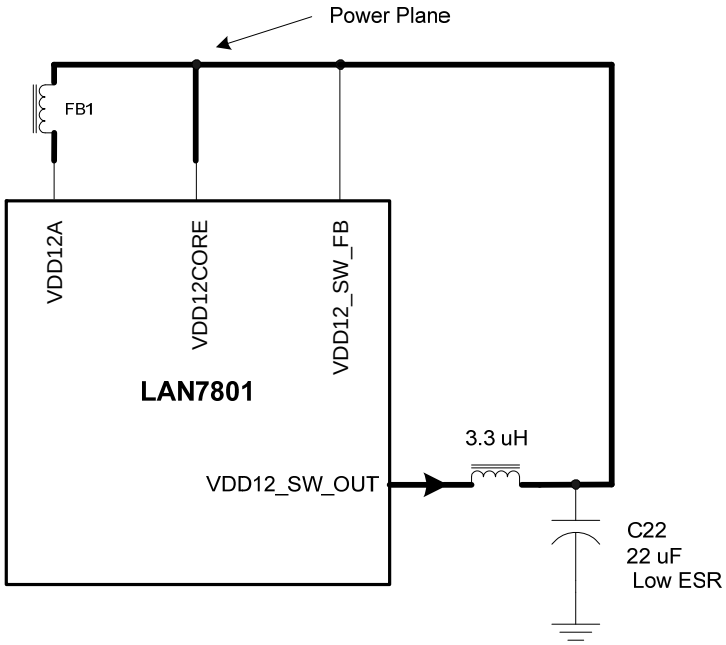


Figure 3 - LAN7801 +1.2V Power Connections

Ground Connections:

1. All grounds, the digital ground pins (GND), the core ground pins (GND_CORE) and the analog ground pins (VSS_A) on the LAN7801 SQFN, are all connected internally to the exposed die paddle ground (VSS). The EDP Ground pad on the underside of the LAN7801 must be connected directly to a solid, contiguous digital ground plane.

2. On the PCB, we recommend one Digital Ground. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN7801 SQFN. For exact specifications and tolerances refer to the latest revision LAN7801 data sheet.

2. XI (pin 52) on the LAN7801 SQFN is the clock circuit input. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XO (pin 53) on the LAN7801 SQFN is the clock circuit output. This pin requires a matching 15 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, the additional external 1.0M Ω resistor across the crystal is no longer required. The necessary resistance has been designed-in internally on the LAN7801 SQFN.

EEPROM Interface:

1. EECS (pin 23) on the LAN7801 SQFN connects to the external EEPROM's CS pin.

2. EECLK (pin 26) on the LAN7801 SQFN connects to the external EEPROM's serial clock pin.

3. EEDI (pin 24) on the LAN7801 SQFN connects to the external EEPROM's Data Out pin.

4. EEDO (pin 25) on the LAN7801 SQFN connects to the external EEPROM's Data In pin.

5. Be sure to select a 3-wire style 2K/4K EEPROM that is organized for 256/512 x 8-bit operation.

6. Be sure to select an EEPROM with an operational voltage that matches your design's VDDVARIO voltage level.

REF_REXT Resistor:

1. REF_REXT (pin 1) on the LAN7801 SQFN should connect to digital ground through a 2.00K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

REF_FILT Capacitor:

1. REF_FILT (pin 2) on the LAN7801 SQFN should connect to digital ground through a 1.0 uF capacitor. This pin is used as an external Phy reference filter for the embedded 10/100 Ethernet Physical device.

2. We recommend using a low ESR capacitor for the REF_FILT cap. The REF_FILT cap should be a high quality, low ESR, ceramic type capacitor for this particular application. We recommend the ESR not be any higher than 2.0 ohms for frequency ranges from 10 KHz to 1 GHz.

USBRBIAS Resistor:

1. USBRBIAS (pin 49) on the LAN7801 SQFN should connect to digital ground through a 12.0K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded USB Physical device.

Required External Pull-ups/Pull-downs:

1. When using the RGMII interface of the LAN7801 with a Phy device, a pull-up resistor on the MDIO signal (pin 55) is required. A pull-up resistor of 1.5KΩ to VDDVARIO is required for this application.

2. GPIO0 (pin 23) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

3. GPIO1 (pin 24) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

4. GPIO2 (pin 25) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

5. GPIO3 (pin 26) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

6. GPIO4 (pin 35) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

7. GPIO5 (pin 36) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

8. GPIO6 (pin 45) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

9. GPIO7 (pin 57) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

10. GPIO8 (pin 58) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

11. GPIO9 (pin 59) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

12. GPIO10 (pin 60) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

13. GPIO11 (pin 61) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

USB Interface:

1. USB2_DP (pin 38), this pin is the USB 2.0 channel positive data pin. This pin should be connected directly to pin 3 (D+) on an upstream USB connector (Type “B”).

2. USB2_DM (pin 39), this pin is the USB channel negative data pin. This pin should be connected directly to pin 2 (D-) on an upstream USB connector (Type “B”).

3. USB3_TXDP (pin 40), this pin is the USB SuperSpeed channel transmit positive data pin. This pin should be connected to pin 6 (SSTX+) on an upstream USB connector (Type “B”) through a 0.1 uF DC blocking capacitor.

4. USB3_TXDM (pin 41), this pin is the USB SuperSpeed channel transmit negative data pin. This pin should be connected to pin 5 (SSTX-) on an upstream USB connector (Type “B”) through a 0.1 uF DC blocking capacitor.

5. For the DC Blocking Caps, SMD_0402 capacitors are recommended (no larger).

6. USB3_RXDP (pin 43), this pin is the USB SuperSpeed channel receive positive data pin. This pin should be connected directly to pin 9 (SSRX+) on an upstream USB connector (Type “B”).

7. USB3_RXDM (pin 44), this pin is the USB SuperSpeed channel receive negative data pin. This pin should be connected directly to pin 8 (SSRX-) on an upstream USB connector (Type “B”).

8. For USB 3.0 Super Speed interconnects, the receiver pins have Auto-Polarity correction, by specification. This allows the pairs to be swapped to facilitate board layout concerns. This allows SSTXP to be swapped with SSTXN **or** SSRXP to be swapped with SSRXN. It does **not** allow for the SSTX channel to be swapped with the SSRX channel. Furthermore, the polarity of the USB 2.0 lines cannot be swapped.

9. Pins 4 & 7 on the USB SuperSpeed connector should be connected directly to digital ground.

10. The metal shield of the USB SuperSpeed connector should be connected directly to a suitable chassis ground plane.

11. For board applications where the USB 3.0 link is between two devices intra-board, the SSTX and SSRX channels must be crossed over. Two DC blocking caps (0.1 uF) should be placed as close as possible to USB3_TXDN & USB3_TXDP on the LAN7801 device. Two more DC blocking caps should be placed on the transmit pins of the other USB 3.0 device.

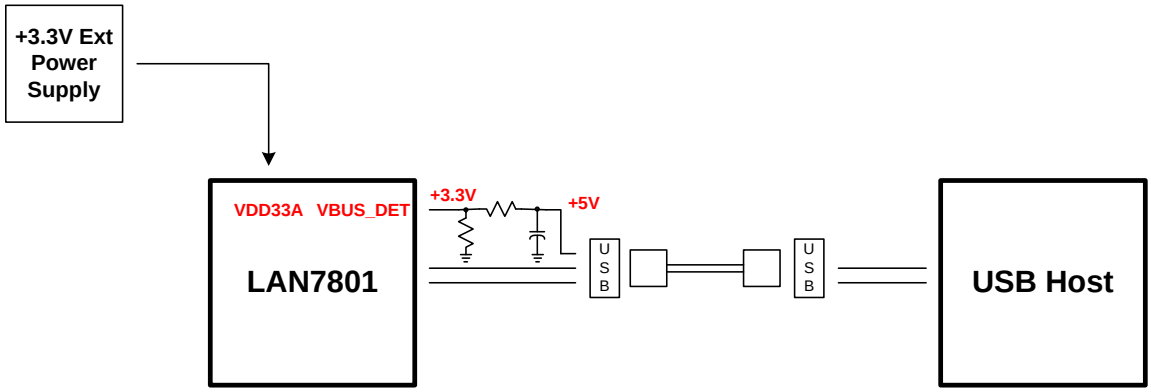
12. For board applications where the USB 3.0 link uses a USB connector, the RX and TX channels must not be crossed over to the connector. The cross over function is accomplished in the USB cable. Two DC blocking caps (0.1 uF) should be placed as close as possible to USB3_TXDN & USB3_TXDP on the USB connector. Two more DC blocking caps should exist on the transmit pins of the other USB 3.0 device on the other side of the cable.

13. SUSPEND_N (pin 30), this output pin of the LAN7801 indicates USB Suspend States. This pin is asserted when the device is in one of the suspend states as defined in Section 12.3, "Suspend States". This pin may be configured to place an external switcher into a low power state such as when the device is in SUSPEND2.

VBUS_DET Configurations:

Possible VBUS_DET pin (pin 29) connections are dictated by the hardware configuration of the USB link. Possible designs are “Self-Powered Mode”, “Self-Powered Permanently Attached Mode” and “Bus-Powered Mode”. These three possible configurations are depicted below.

Self-Powered Mode:

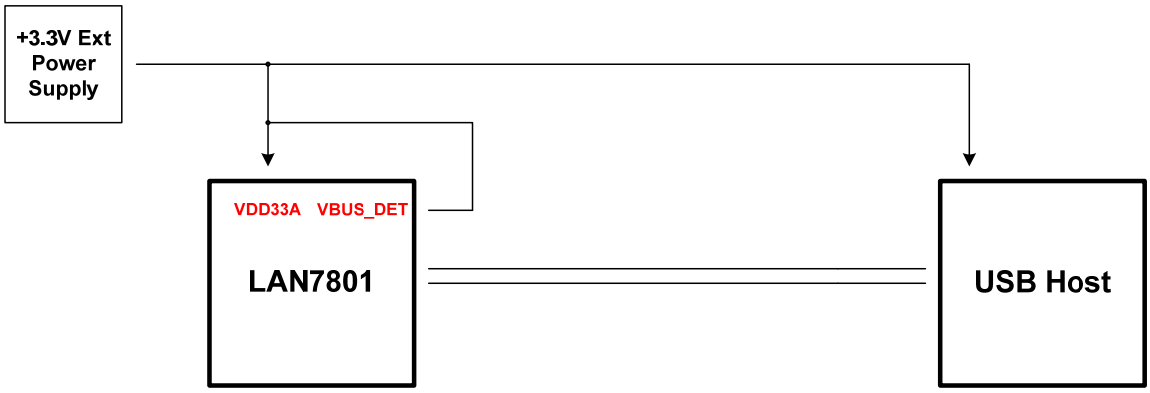


1. In this application, the VBUS_DET pin (pin 29) is driven by a voltage divider circuit that drops the +5V VBUS voltage to +3.3V.

2. For the voltage divider, a series 100K ohm resistor with a 200K ohm resistor to digital ground is recommended.

3. A 2.2 uF capacitor is also recommended on pin 1 (VBUS) of the USB connector.

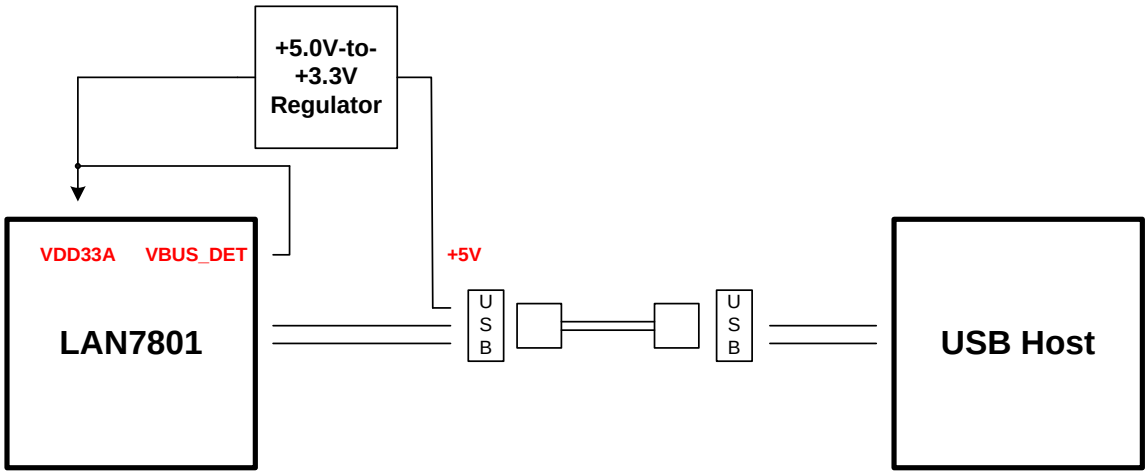
Self-Powered Permanently Attached Mode:



1. In this application, the VBUS_DET pin (pin 29) is driven by the same power rail that powers both the LAN7801 and the USB Host.

2. A series resistor (820 ohms to 10K ohms) may be used on the VBUS_DET pin in order to improve susceptibility characteristics.

Bus-Powered Mode:



1. Typical Bus-Powered applications will connect pin 1 (VBUS) on a standard 4-pin, upstream USB connector (Type “B”) directly to a 2000 mA ferrite bead. This ferrite bead will in turn feed a LDO +5.0V-to-+3.3V voltage regulator to power the LAN7801.

2. We recommend no bulk capacitance be placed on pin 1 (VBUS) of the USB connector in Bus-Powered applications. On the voltage regulator side of the ferrite bead, we recommend limiting the bulk capacitance to 4.7 uF. This should satisfy the 10.0 uF total capacitance to limit in-rush current as required by the USB-IF specification.

3. VBUS_DET (pin 29), this pin detects the state of the supplied upstream power. This pin must be tied to VDD33A when operating in Bus-Powered mode.

Miscellaneous:

1. There is one No-Connect pin on the LAN7801. It is very important that this pin (pin 34) remain a no-connect.

2. RESET_N (pin 47) A hardware reset will occur when the RESET_N pin is driven low. Assertion of RESET_N is not required at power-on. However, if used, RESET_N must be driven low for a minimum period as defined in Section 16.6.2, "RESET_N Timing," on page 229. The RESET_N pin is pulled-high internally but must be connected externally to VDDVARIO if unused.

3. RESET_N (pin 47), For a more robust LAN7801 design, a hardware reset (nRST assertion) is recommended following power-up. This signal resets all logic and registers within the LAN7801. SMSC does not recommend the use of an RC circuit for this pin reset. A reset generator / voltage monitor is one option to provide a proper reset. Better yet, for increased design flexibility, a controllable reset (GPIO, dedicated reset output) should be considered. In this case, SMSC recommends a push-pull type output (not an open-drain type) for the monotonic reset to ensure a sharp rise time transition from low-to-high.

4. TEST (pin 46), this pin must be tied directly to digital ground in order to ensure proper operation.

5. For a detailed description of the PME pins on the LAN7801, please refer to section 13.0 POWER MANAGEMENT EVENT (PME) OPERATION in the LAN7801 data sheet.

6. The JTAG inputs (pins 57, 58 & 59) should be terminated high, if not used, with 10K pull-ups. Pin 60, TDO, can be left as a no-connect.

7. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

8. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

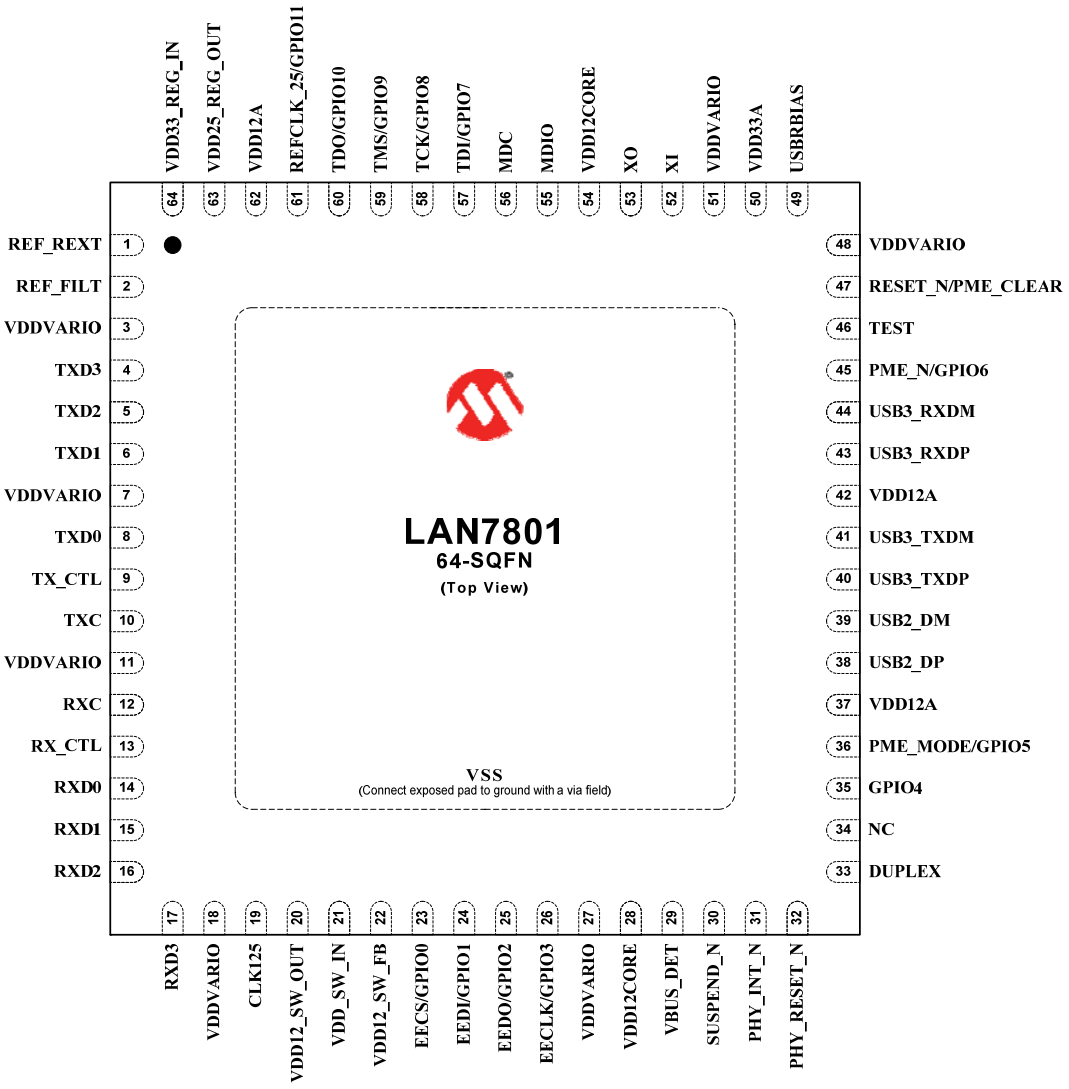
LAN7801 SQFN QuickCheck Pinout Table:

Use the following table to check the LAN7801 SQFN shape in your schematic.

LAN7801 SQFN			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
1	REF_REXT	33	DUPLEX
2	REF_FILT	34	NC
3	VDDVARIO	35	GPIO4
4	TXD3	36	PME_MODE / GPIO5
5	TXD2	37	VDD12A
6	TXD1	38	USB2_DP
7	VDDVARIO	39	USB2_DM
8	TXD0	40	USB3_TXDP
9	TX_CTL	41	USB3_TXDM
10	TXC	42	VDD12A
11	VDDVARIO	43	USB3_RXDP
12	RXC	44	USB3_RXDM
13	RX_CTL	45	PME_N / GPIO6
14	RXD0	46	TEST
15	RXD1	47	RESET_N / PME_CLEAR
16	RXD2	48	VDDVARIO
17	RXD3	49	USBRBIAS
18	VDDVARIO	50	VDD33A
19	CLK125	51	VDDVARIO
20	VDD12_SW_OUT	52	XI
21	VDD_SW_IN	53	XO
22	VDD12_SW_FB	54	VDD12CORE
23	EECS / GPIO0	55	MDIO
24	EEDI / GPIO1	56	MDC
25	EEDO / GPIO2	57	TDI / GPIO7
26	EECLK / GPIO3	58	TCK / GPIO8
27	VDDVARIO	59	TMS / GPIO9
28	VDD12CORE	60	TDO / GPIO10
29	VBUS_DET	61	REFCLK_25 / GPIO11
30	SUSPEND_N	62	VDD12A
31	PHY_INT_N	63	VDD25_REG_OUT
32	PHY_RESET_N	64	VDD33_REG_IN
65		**EDP Ground Connection Exposed Die Paddle Ground Pad on Bottom of Package**	

Notes:

LAN7801 SQFN Package Drawing:



Note: Exposed pad **(VSS)** on bottom of package must be connected to ground with a via field.

Reference Material:

1. Microchip LAN7801 Data Sheet; check web site for latest revision.
2. Microchip LAN7801 Reference Design, check web site for latest revision.
3. Microchip Reference Designs are schematics only; there are no associated PCBs.
4. EVB-LAN7801 Customer Evaluation Board & Schematics