LAN7800

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip LAN7800. These checklist items should be followed when utilizing the LAN7800 in a new design. A summary of these items is provided in Section 11.0, "Hardware Checklist Summary," on page 13. Detailed information on these subjects can be found in the corresponding section:

- Section 2.0, "General Considerations," on page 1
- Section 3.0, "Power," on page 3
- Section 4.0, "Ethernet Signals," on page 5
- Section 5.0, "Clock Circuit," on page 7
- Section 6.0, "EEPROM Interface," on page 8
- Section 7.0, "Required Discrete Components," on page 9
- Section 8.0, "Startup," on page 9
- Section 9.0, "USB Interface," on page 10
- Section 10.0, "Miscellaneous," on page 12

2.0 GENERAL CONSIDERATIONS

2.1 Required References

At a minimum, the circuit designer should have the following documents on hand:

• *LAN7800 Data Sheet*

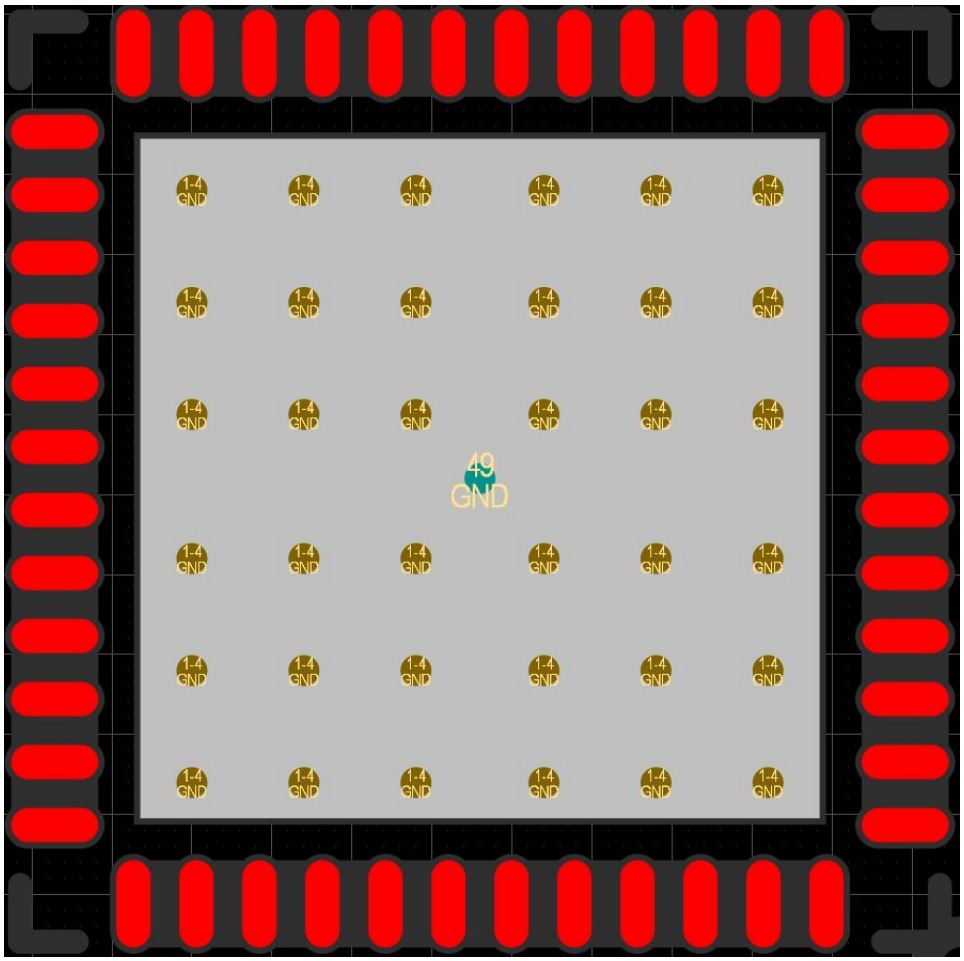
2.2 Pin Check

Check the pinout of the part against the data sheet. When creating schematic symbols ensure all pins match the data sheet and are configured as inputs, outputs, bidirectional, open drain, or power for schematics tool error checking.

2.3 Ground

- The LAN7800 has one exposed pad (e-PAD), which is also the GND pin.
- An array of vias should be added to the e-PAD area. Using a 20 mil (1 mil = 1/1000 inch) wide via with 10 mil hole size, 36 vias can be placed on the e-PAD. These vias should connect to a solid board ground plane.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.
- A recommended e-PAD layout with ground vias is shown in Figure 2-1 using 20 mil diameter vias with 10 mil hole size.

FIGURE 2-1: RECOMMENDED E-PAD LAYOUT WITH GROUND VIAS



3.0 POWER

3.1 3.3V Supply

- The analog supply (**VDD33A**) is located on pin 38 and requires a connection to **VDDA** (created from +3.3V through a ferrite bead). Bulk capacitance should be placed on each side of the ferrite bead. Generally, a 100-220Ω (at 100 MHz) ferrite bead is used.
- The **VDDA3.3** pin should include 0.1 µF and 22 µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The **VDD33_REG_IN** supply pin for the +2.5V LDO regulator in the LAN7800 SQFN is pin 46. This pin requires a connection to +3.3V and should also have one 0.1 µF capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.
- The **VDD_SW_IN** supply pin for the +1.2V switching regulator in the LAN7800 SQFN is pin 14. This pin requires a connection to +3.3V and should also have one 0.1 µF capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.

3.2 VDDVARIO Supply

- The **VDDVARIO** supply pins on the LAN7800 SQFN are pins 20, 36, and 39. These pins require a connection in the range of 1.8V to 3.3V.
- Each **VDDVARIO** pin should also have one 0.1 µF capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.

3.3 2.5V Supply

- **VDD25_REG_OUT** (pin 45) is the output pin of the internal +2.5V LDO regulator for the LAN7800. This pin should have one 0.1 µF capacitor to bypass the LAN7800. The capacitor size should be SMD_0603 or smaller.
- The **VDD25_REG_OUT** pin also requires a 1.0 µF, low-ESR capacitor. The low ESR requirement ensures the proper stability of the +2.5V internal regulator of the LAN7800. It is recommended to use a high-quality, low-ESR, ceramic-type capacitor for this particular application and that the ESR does not exceed 2.0Ω for frequency ranges from 10 kHz to 1 GHz.
- The **VDD25A** (pins 3, 6, 9, and 12) input power supply pins should be powered from the internal +2.5V switching regulator. These pins power the Gigabit Ethernet PHY Analog Front End (AFE) (see Figure 3-1). The **VDD25A** pins should each have one 0.1 µF capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.

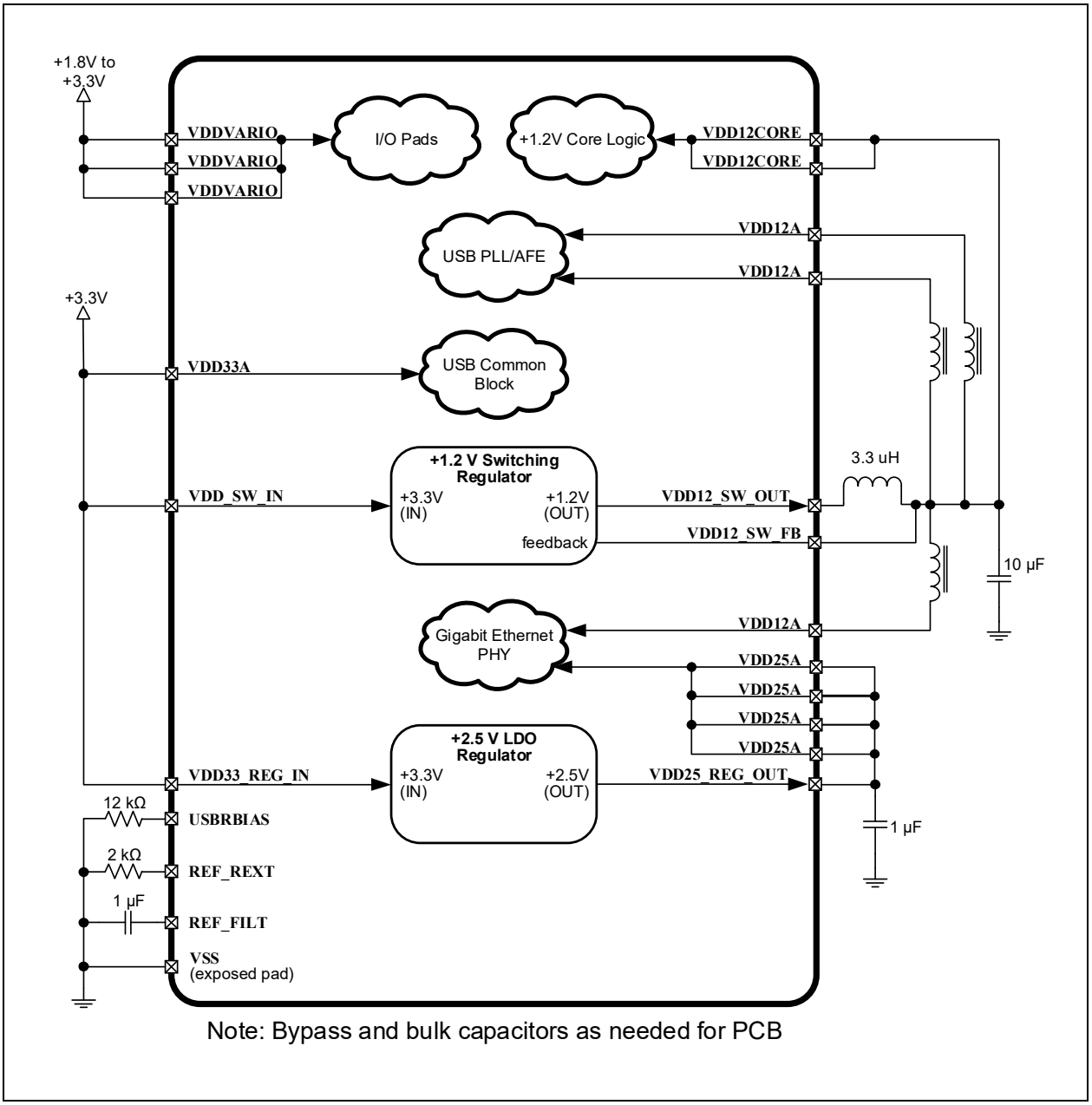
3.4 1.2V Supply

- **VDD12_SW_OUT** (pin 13) is the output pin of the internal +1.2V switching regulator for the LAN7800. This pin must be connected through a 3.3 uH inductor to **VDD12_SW_FB** (see Figure 3-1).
- The **VDD12_SW_OUT** pin/3.3 uH inductor node in the design should have one 0.1 µF capacitor to bypass the LAN7800. The capacitor size should be SMD_0603 or smaller.
- The **VDD12_SW_OUT** pin/3.3 uH inductor node also requires a 22 µF, low-ESR capacitor. The low ESR requirement ensures proper stability of the +1.2V internal regulator of the LAN7800. It is recommended to use a high-quality, low-ESR, ceramic-type capacitor for this particular application and that the ESR does not exceed 2.0Ω for frequency ranges from 10 kHz to 1 GHz.
- **VDD12_SW_FB** (pin 15) supplies feedback for the internal +1.2V switching regulator. In this application, this pin should be connected directly to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7800. For applications where the +1.2V internal switching regulator is disabled, simply connect **VDD12_SW_FB** directly to **VDD_SW_IN** (pin 14).
- The **VDD12_SW_FB** pin should have one 0.1 µF capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.
- The **VDD12CORE** (pins 21 and 42) core input power supply pins may be powered from the internal +1.2V switching regulator. In this application, these two pins should be connected directly to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7800 (see Figure 3-1). These two pins can also be supplied from an external +1.2V power supply. In this application, the internal +1.2V switching regulator can be disabled.
- The **VDD12CORE** pins should each have one 0.1 µF capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.

- The **VDD12A** (pins 25, 30, and 44) pins supply power to the analog blocks (Gigabit Ethernet PHY and the USB Phase Locked-Loop (PLL)/AFE section) of the LAN7800 from the internal +1.2V switching regulator through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. A 1.0 µF, low-ESR capacitor is required on the pin 25, 30, and 44 side of the ferrite bead. In this application, the ferrite bead should be connected to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7800 (see Figure 3-1). These three pins can also be supplied from an external +1.2V power supply. In this application, the internal +1.2V switching regulator can be disabled.
- The **VDD12A** pins should each have one 0.1 µF capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER CONNECTION DIAGRAM



Note: Bypass and bulk capacitors as needed for PCB

Caution: This +1.2V supply is for internal logic only. **Do not** power other circuits or devices with this supply.

4.0 ETHERNET SIGNALS

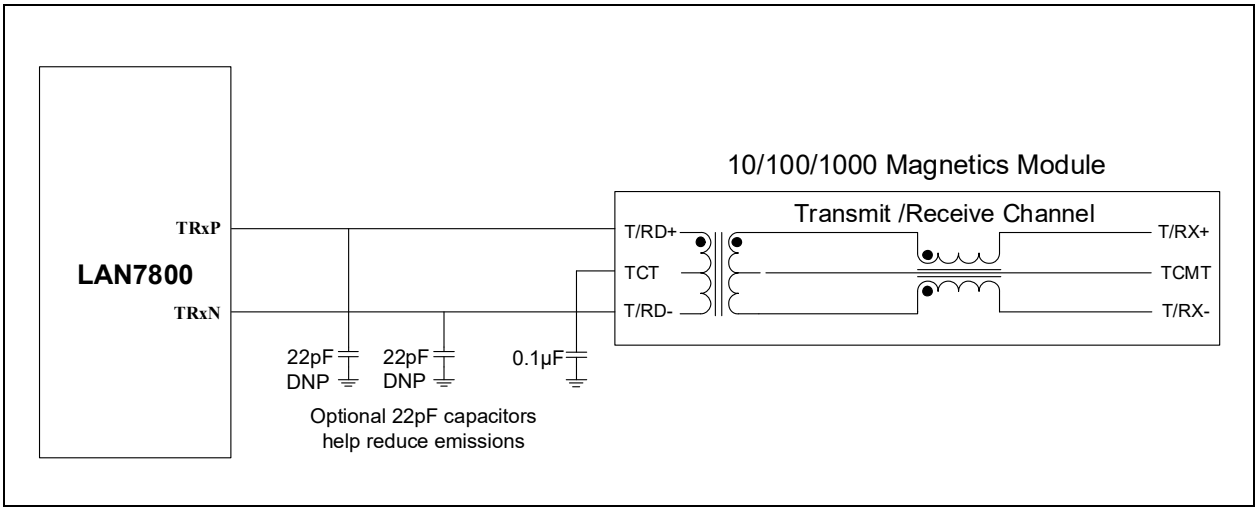
4.1 PHY Interface

- **TR0P** (pin 1): This pin is the transmit (TX) or receive (RX) positive channel 0 input/output (I/O) connection of the internal PHY. This pin connects to the 10/100/1000 magnetics.
- **TR0N** (pin 2): This pin is the TX/RX negative channel 0 I/O connection of the internal PHY. This pin connects to the 10/100/1000 magnetics.
- **TR1P** (pin 4): This pin is the TX/RX positive channel 1 I/O connection of the internal PHY. This pin connects to the 10/100/1000 magnetics.
- **TR1N** (pin 5): This pin is the TX/RX negative channel 1 I/O connection of the internal PHY. This pin connects to the 10/100/1000 magnetics.
- **TR2P** (pin 7): This pin is the TX/RX positive channel 2 I/O connection of the internal PHY. This pin connects to the 10/100/1000 magnetics.
- **TR2N** (pin 8): This pin is the TX/RX negative channel 2 I/O connection of the internal PHY. This pin connects to the 10/100/1000 magnetics.
- **TR3P** (pin 10): This pin is the TX/RX positive channel 3 I/O connection of the internal PHY. This pin connects to the 10/100/1000 magnetics.
- **TR3N** (pin 11): This pin is the TX/RX negative channel 3 I/Os connection of the internal PHY. This pin connects to the 10/100/1000 magnetics.

Note:	The LAN7800 does not require the usual 49.9Ω terminations resistors. These have been designed internally in the device.

For TX and RX channel connections details, refer to Figure 4-1.

FIGURE 4-1: TRANSMIT/RECEIVE CHANNEL CONNECTIONS



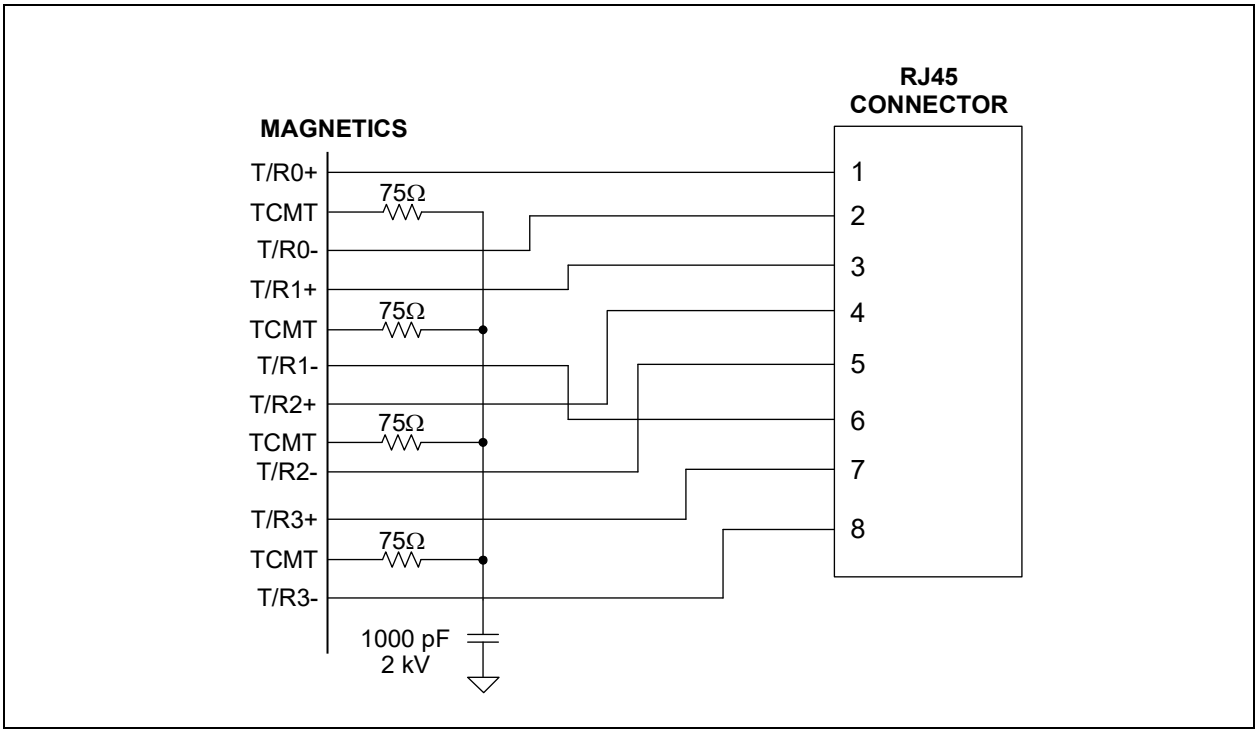
4.2 Magnetics Connection

- The center tap connection on the LAN7800 side for each channel connects to a 0.1 µF capacitor to GND, and no bias is needed.
- The center tap connection on the cable side (RJ45 side) for each channel should be terminated with a 75Ω resistor through a 1000 pF, 2 KV capacitor to chassis ground.
- **TR0P** (pin 1) of the LAN7800 should trace through the magnetics to pin 1 of the RJ45 connector.
- **TR0N** (pin 2) of the LAN7800 should trace through the magnetics to pin 2 of the RJ45 connector.
- **TR1P** (pin 4) of the LAN7800 should trace through the magnetics to pin 3 of the RJ45 connector.
- **TR1N** (pin 5) of the LAN7800 should trace through the magnetics to pin 6 of the RJ45 connector.
- **TR2P** (pin 7) of the LAN7800 should trace through the magnetics to pin 4 of the RJ45 connector.
- **TR2N** (pin 8) of the LAN7800 should trace through the magnetics to pin 5 of the RJ45 connector.
- **TR3P** (pin 10) of the LAN7800 should trace through the magnetics to pin 7 of the RJ45 connector.
- **TR3N** (pin 11) of the LAN7800 should trace through the magnetics to pin 8 of the RJ45 connector.

4.3 RJ45 Connector

The RJ45 shield should be attached directly to chassis ground.

FIGURE 4-2: RJ45 CONNECTIONS



5.0 CLOCK CIRCUIT

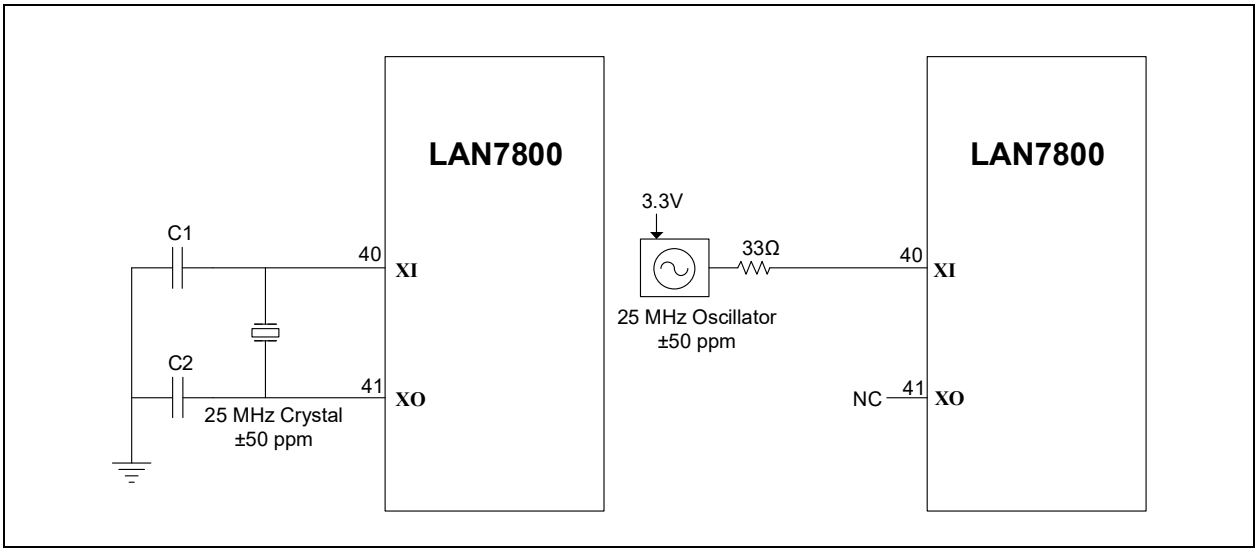
5.1 Crystal and External Clock Connection

A 25.000 MHz (±50 ppm) crystal should be used to provide the clock source. For exact specifications and tolerances, refer to the latest revision of the *LAN7800 Data Sheet*.

- **XI** (pin 40) is the clock circuit input for the LAN7800. This pin requires a 15-33 pF capacitor to ground. One side of the crystal connects to this pin.
- **XO** (pin 41) is the clock circuit output for the LAN7800. This pin requires a matching 15-33 pF capacitor to ground. One side of the crystal connects to this pin.
- Since every system design is unique, the capacitor values are system-dependent, based on the C_L specification of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.

Alternately, a 25.000 MHz, 3.3V clock oscillator may be used to provide the clock source for the LAN7800. When using a single-ended clock source, the **XO** should be left floating as a No Connect (NC). To reduce ringing and reflections, it is recommended to add a serial termination resistor (typically 33Ω) to the clock oscillator output connected to **XI**.

FIGURE 5-1: CRYSTAL AND OSCILLATOR CONNECTIONS



6.0 EEPROM INTERFACE

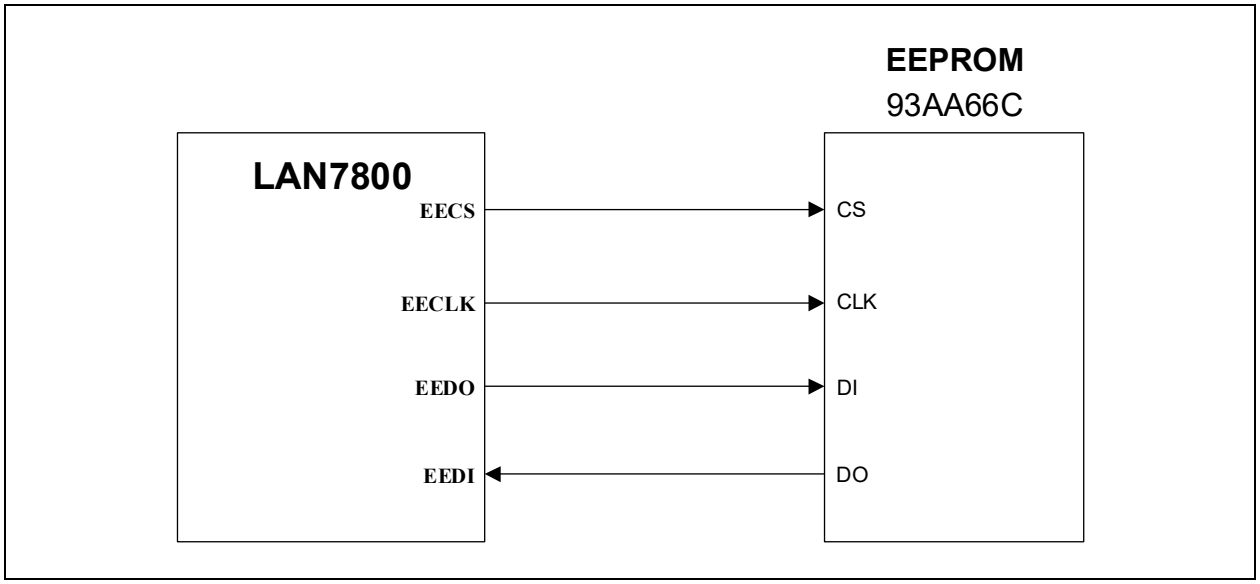
6.1 EEPROM Interface Connections

- The LAN7800 includes 1 KB of One-Time Programmable (OTP) memory for configuration data. For more flexibility, an external EEPROM can be used to load USB and Ethernet configuration parameters.
- The LAN7800 requires a 4-wire style 2k/4k EEPROM organized as 256/512 x 8-bit such as the Microchip 93AA66C.
- **EECS** (pin 16) on the LAN7800 connects to the external EEPROMCS pin.
- **EECLK** (pin 19) on the LAN7800 connects to the external EEPROM serial clock pin.
- **EEDI** (pin 17) on the LAN7800 connects to the external EEPROM Data Out pin.
- **EEDO** (pin 18) on the LAN7800 connects to the external EEPROM Data In pin.

Note: One typical mistake is to connect the LAN7800 **EEDO** pin to the EEPROM DO pin, and similarly the **EEDI** pin to the DI pin of the EEPROM. Note how the **EEDO** pin connects to DI and the **EEDI** pin connects to DO.

The EEPROM operating voltage should match the VDDVARIO voltage in the design.

FIGURE 6-1: EEPROM CONNECTIVITY



6.2 External EEPROM Programming

It may be desirable to program the EEPROM externally in some cases. This could be during initial board bring-up or it could be in a production environment where a board tester can be used to program the EEPROM. To avoid signal contention with signals driven from the LAN7800 to the EEPROM, the LAN7800 **RESET_N** pin input (pin 35) must be held low. This forces all LAN7800 signals to be in a high impedance state, and external signals can be applied to program the EEPROM without contention.

7.0 REQUIRED DISCRETE COMPONENTS

- **REF_REXT** (pin 47) should be connected to a 2 kΩ resistor with a 1% tolerance connected to ground. This pin is used to set critical bias currents for the 10/100 Ethernet PHY.
- **REF_FILT** (pin 48) should be connected to a 1.0 µF capacitor to ground. This pin is used as a reference filter for the 10/100 Ethernet PHY. The capacitor should be a low-ESR (<2Ω) ceramic capacitor.
- **USBRBIAS** (pin 37) should be connected to a 12 kΩ 1% resistor to ground. This pins sets the critical bias currents for the USB PHY device.

8.0 STARTUP

8.1 Power-On Reset (POR)

A Power-On Reset (POR) occurs whenever power is initially applied to the LAN7800. An internal timer asserts the internal reset for about 20 ms. This reset loads the EEPROM/OTP contents.

8.2 External Reset (RESET_N)

- A hardware reset occurs when the **RESET_N** pin is driven low. Assertion of **RESET_N** is not required at power-on. However, if used, **RESET_N** must be driven low for a minimum period as defined in the *"RESET_N Timing"* section of the *LAN7800 Data Sheet*. The **RESET_N** pin is pulled high internally but must be connected externally to **VDDVARIO** if unused.
- **RESET_N** (pin 35): For a more robust LAN7800 design, a hardware reset (nRST assertion) is recommended following power-up. This signal resets all logic and registers within the LAN7800. Microchip does not recommend the use of an RC circuit for this pin reset. A reset generator or voltage monitor is one option to provide a proper reset. Moreover, for increased design flexibility, a controllable reset (GPIO, dedicated reset output) should be considered. In this case, it is recommended to use a push-pull type output (not an open-drain type) for monotonic reset to ensure a sharp rise time transition from low to high.

8.3 LED Pins

- The LAN7800 Ethernet PHY provides four LED pins (LED[0:3]). These indicators display speed, link, and activity information about the current state of the PHY. The default active LED state is low but this can be changed via the **Invert LED Polarity** field of the Ethernet PHY Page 2 EEE Control Register. The blink/pulse-stretch and other LED setting can also be configured (for details see the *LAN7800 Data Sheet*).
- **LED0** (pin 18), **LED1** (pin 19), **LED2** (pin 24), and **LED3** (pin 33) can be programmed via the register settings to display various Ethernet activity such as speed, link, and duplex status. See the *LAN7800 Data Sheet* for complete details.

9.0 USB INTERFACE

9.1 USB Connector

- **USB2_DP** (pin 26) is the USB 2.0 positive data pin. This pin should be connected directly to pin 3 (D+) on an upstream USB 3 Type-B connector.
- **USB2_DM** (pin 27) is the USB 2.0 negative data pin. This pin should be connected directly to pin 2 (D-) on an upstream USB 3 Type-B connector.
- A USB 3 connector should be used to take advantage of the additional performance of USB 3. If this is not required a USB 2 connector can be used. In this case, the USB 3 signals should be left unconnected.
- **USB3_TXDP** (pin 28) is the USB SuperSpeed TX+ data pin. This pin should be connected to pin 6 (SSTX+) on an upstream USB 3 Type-B connector through a 0.1 µF DC blocking capacitor. An SMD 0402 capacitor is recommended.
- **USB3_TXDM** (pin 29) is the USB SuperSpeed TX- data pin. This pin should be connected to pin 5 (SSTX-) on an upstream USB 3 Type-B connector through a 0.1 µF DC blocking capacitor. An SMD 0402 capacitor is recommended.
- **USB3_RXDP** (pin 31) is the USB SuperSpeed RX+ data pin. This pin should be connected directly to pin 9 (SSRX+) on an upstream USB 3 Type-B connector
- **USB3_RXDM** (pin 32) is the USB SuperSpeed RX- data pin. This pin should be connected directly to pin 8 (SSRX+) on an upstream USB 3 Type-B connector.
- For USB 3.0 SuperSpeed interconnects, the receiver pins have an Auto-Polarity correction by specification. This allows the pairs to be swapped to facilitate board layout concerns, and the SSTXP to be swapped with SSTXN or the SSRXP to be swapped with SSRXN. However, this does not allow the SSTX channel to be swapped with the SSRX channel. Furthermore, the polarity of the USB 2.0 lines cannot be swapped.
- Pins 4 and 7 on the USB 3 Type-B connector should be connected directly to digital ground.
- The metal shield of the USB SuperSpeed connector should be connected directly to a suitable chassis ground plane.
- For board applications where the USB 3.0 link is between two devices intra-board, the SSTX and SSRX channels must be crossed over. Two DC blocking capacitors (0.1 µF) should be placed as close as possible to **USB3DP_TXDNx** and **USB3DM_TXDNx** on the LAN7800 device. Two more DC blocking capacitors should be placed on the transmit pins of the other USB 3.0 device.
- For board applications where the USB 3.0 link uses a USB connector, the RX and TX channels must not be crossed over to the connector. The crossover function is accomplished in the USB cable. Two DC blocking capacitors (0.1 µF) should be placed as close as possible to **USB3DP_TXDNx** and **USB3DM_TXDNx** on the USB connector. Two more DC blocking capacitors should exist on the transmit pins of the other USB 3.0 device on the other side of the cable.

9.2 VBUS_DET Configuration

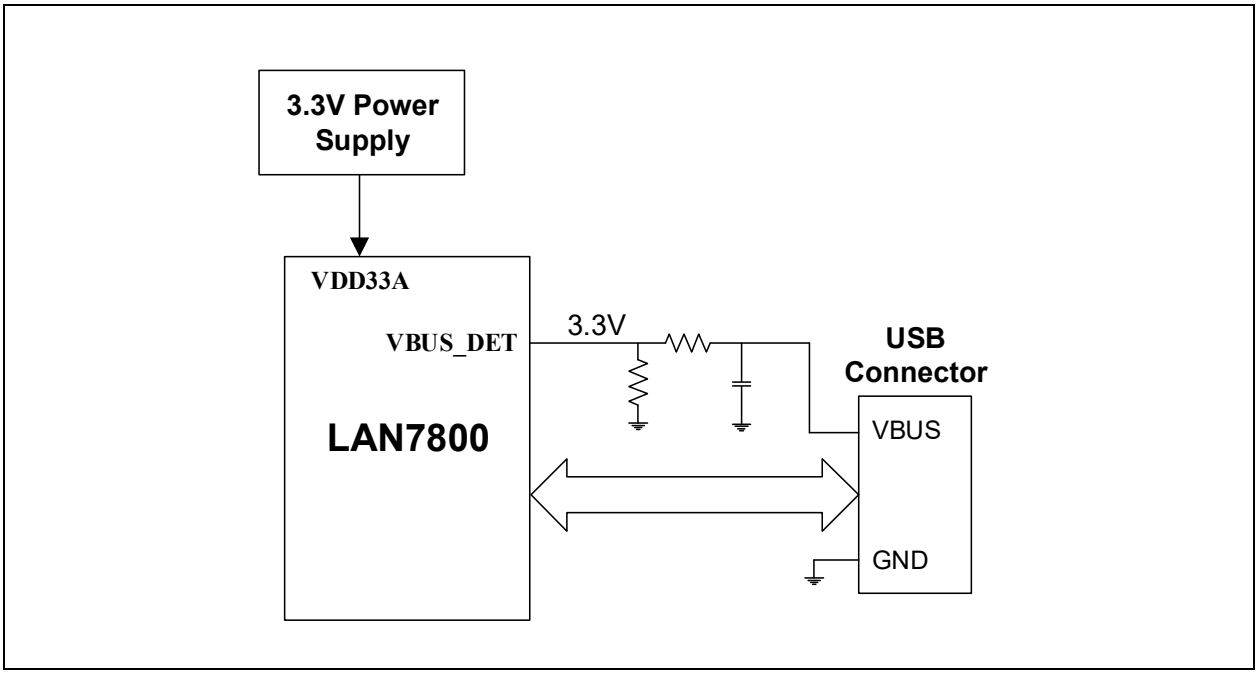
VBUS_DET (pin 23) connections are dictated by the hardware configuration of the USB link. Possible designs are:

- Self-Powered mode
- Self-Powered Permanently Attached mode
- Bus-Powered mode

9.2.1 SELF-POWERED MODE

- In this configuration, the **VBUS_DET** pin is driven by a voltage divider circuit that drops the nominal 5V VBUS to 3.3V.
- For the voltage divider, it is recommended to use a 100 kΩ series resistor with a 200 kΩ resistor to digital ground.
- A 2.2 µF ceramic capacitor is also recommended on VBUS.

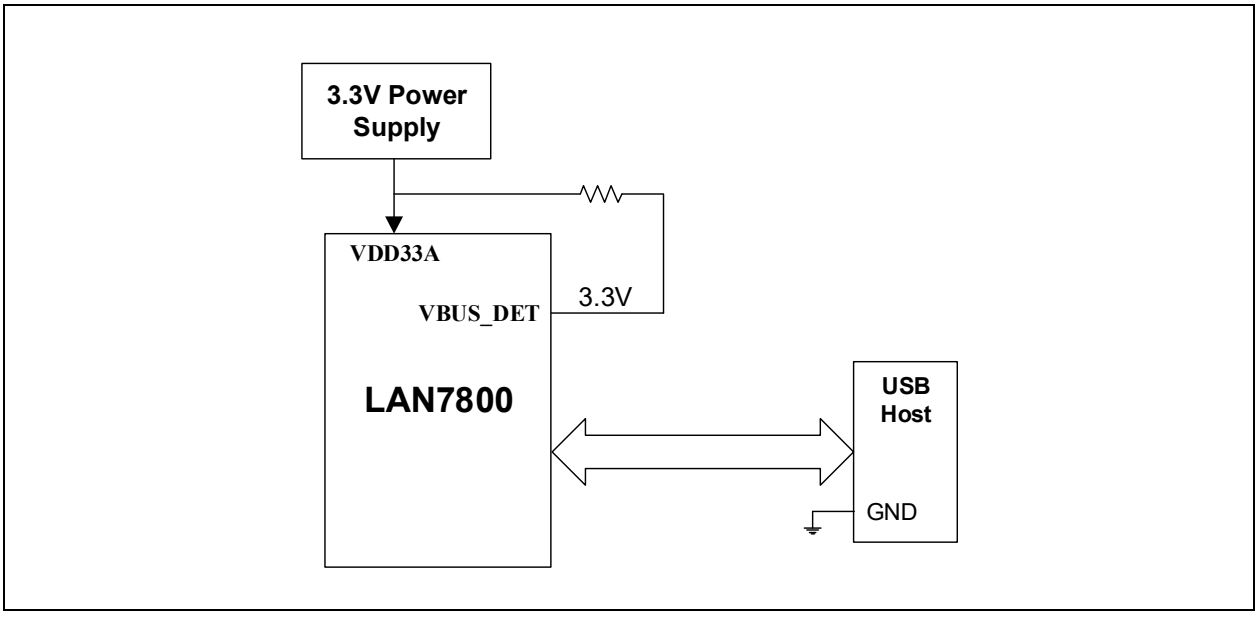
FIGURE 9-1: SELF-POWERED MODE



9.2.2 SELF-POWERED PERMANENTLY ATTACHED MODE

- In this configuration, the **VBUS_DET** pin is driven by the same power rail that powers the LAN7800 **VDD33A** pin.
- A series resistor (820Ω to 10 kΩ) may be used on the VBUS_DET net to reduce noise in the LAN7800.

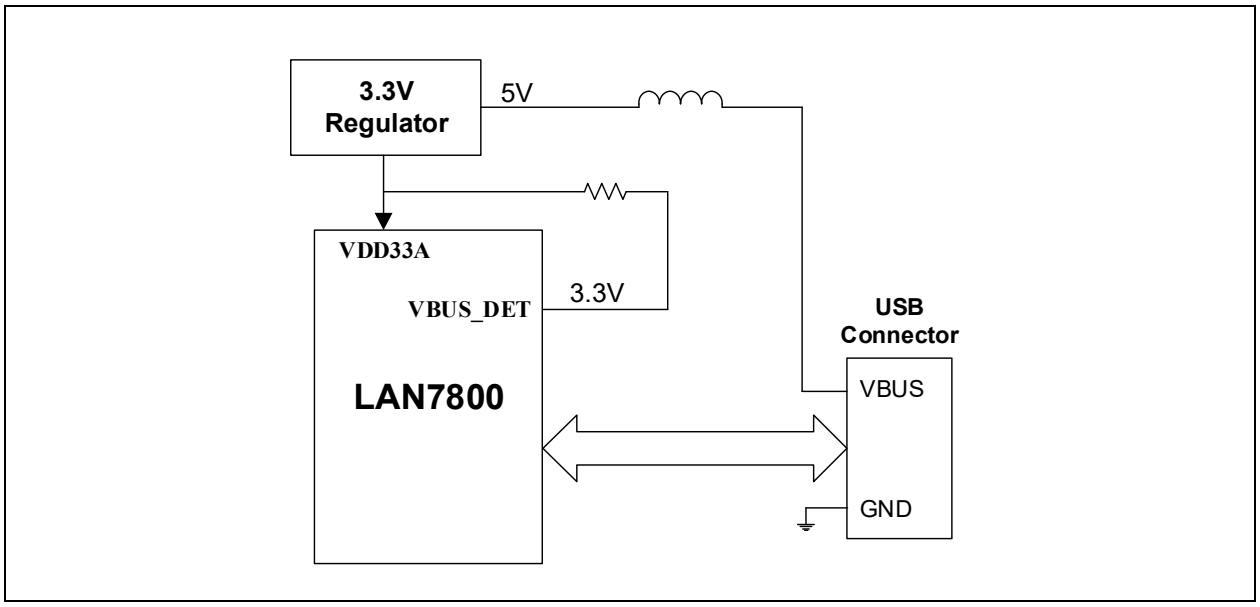
FIGURE 9-2: SELF-POWERED PERMANENTLY ATTACHED MODE



9.2.3 BUS-POWERED MODE

- In this configuration, the **VBUS_DET** pin is driven by the same power rail that powers the LAN7800 **VDD33A** pin.
- A series resistor (820Ω to 10 kΩ) may be used on the VBUS_DET net to reduce noise in the LAN7800.
- The USB connector **VBUS** pin connects to a ferrite bead to power a 5V to 3.3V regulator to provide power to the LAN7800.

FIGURE 9-3: BUS-POWERED MODE



10.0 MISCELLANEOUS

10.1 Other Considerations

- For a detailed description of the power management event (PME) pins on the LAN7800, please refer to the *"Power Management Event (PME) Operation"* section of the *LAN7800 Data Sheet*.
- Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at Electro Magnetic Interference (EMI) testing for different grounding options. Leave the resistor out; the two grounds are separate. Short them together with a 0Ω resistor. Short them together with a capacitor or a ferrite bead for best performance.
- Be sure to incorporate enough bulk capacitors (4.7 µF to 22 µF) for each power plane.

11.0 HARDWARE CHECKLIST SUMMARY

TABLE 11-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.2, "Pin Check"	Verify that the pins match the data sheet.		
	Section 2.3, "Ground"	Verify that an array of vias connects the LAN7800 ePAD to a solid ground plane.		
Section 3.0, "Power"	Section 3.0, "Power"	• Ensure **VDD33A** and **VDDIO** are in the range 3.135V to 3.465V and a 22 µF capacitor is on each pin. • **VDDVARIO** • **VDD25A** • **VDD12A** requires two 0.1 µF capacitors.		
Section 4.0, "Ethernet Signals"	Section 4.1, "PHY Interface"	Verify that the TRxP and TRxN pins do not contain any termination resistors.		
	Section 4.2, "Magnetics Connection"	Verify that the center taps are connected to the GND using separate 0.1 µF capacitors on the LAN7800 device side, and are terminated with 75Ω resistors through a 1000 pF, 2 kV capacitor to chassis ground on the RJ45 line side.		
	Section 4.3, "RJ45 Connector"	Verify pins 4/5 and 7/8 of the RJ45 connect to CAT-5 cable and are terminated to chassis ground through a 1000 pF, 2 kV capacitor.		
Section 5.0, "Clock Circuit"	Section 5.1, "Crystal and External Clock Connection"	Verify usage of 25 MHz ±50 ppm crystal or a 25 MHz oscillator.		
Section 6.0, "EEPROM Interface"	Section 6.1, "EEPROM Interface Connections"	Confirm that EEDO from the LAN7800 connects to DI on the EEPROM and that EEDI from the LAN7800 connects to DO on the EEPROM. To boot the LAN7800 without the EEPROM, a shunt jumper can be connected to disconnect the LAN7800 EECS from the EEPROM CS pin. If this is done add a 100k pulldown on the EEPROM CS pin.		
Section 7.0, "Required Discrete Components"	Section 7.0, "Required Discrete Components"	Verify that **REF_REXT** pin 47 is connected to a 2 kΩ pull-down resistor. Verify that **REF_FILT** pin 48 is connected to a 1.0 µF capacitor to GND. Verify that **USBRBIAS** pin 37 is connected to a 12 kΩ pull-down resistor.		
Section 8.0, "Startup"	Section 8.1, "Power-On Reset (POR)" and Section 8.2, "External Reset (RESET_N)"	Confirm proper reset circuit design: standalone reset or external CPU/FPGA reset.		
	Section 8.3, "LED Pins"	In systems where the MAC receive input pins are driven high after reset, it is recommended to add 1 kΩ pull-downs on the PHY strap pins.		
Section 9.0, "USB Interface"	Section 9.2, "VBUS_DET Configuration"	See Figure 9-1 for Self-Powered mode. See Figure 9-2 for Self-Powered Permanently Attached mode. See Figure 9-3 for Bus-Powered mode.		
Section 10.0, "Miscellaneous"	Section 10.1, "Other Considerations"	• See PME, if applicable. • Check for separation between chassis ground and digital ground. • Check that enough bulk capacitors have been used.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003446A (04-15-20)	Initial release	

NOTES:

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
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- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

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