AN 26.16
USB Super Speed Receiver Jitter Tolerance

1 Super Speed Jitter Tolerance (JTOL)

The USB-IF designed the Receiver Jitter Tolerance Test to test the quality of the USB 3.0 receiver of a system. This test uses a waveform generator/oscilloscope combination, or a data generator/analyzer to send data to the Super Speed receiver which is then looped back through the transmitter back to the instrument. The data received is compared to the data generated and the errors are counted. The data generator is able to introduce jitter into the transmit data pattern to see how well the receiver functions under non-ideal conditions.

1.1 Objectives

This application note will educate the Super Speed system designer on what to be aware of when testing JTOL. The following topics will be covered:

1. JTOL Procedure
2. JTOL Calibration
3. External Noise Sources

1.2 References

USB 3.0 Specification

SuperSpeed USB Compliance Testing References

USB Electrical Compliance Test Specification for SuperSpeed Rev. 0.90

SuperSpeed USB Software and Hardware Tools

Sigtest version 3.2.3

2 JTOL Test Procedure

The JTOL test is broken up into a subset of loopback tests with a different noise profile applied.

2.1 Physical Connections

The connections from the data generator to the DUT are specified by USB-IF in the Electrical Compliance Test Specification listed in references. The SMA connectors of the data generator are connected to a USB-IF test fixture that has 11 inches (Device) or 5 inches (Host) of PCB trace going to a standard USB3 connector. From that connector, a 3m USB 3.0 cable connects to another USB-

IF test fixture that splits out the Transmit (TX) signals from the DUT to the data analyzer through SMA cables, and combines the TX and RX signals into a standard USB connector to connect to the DUT.

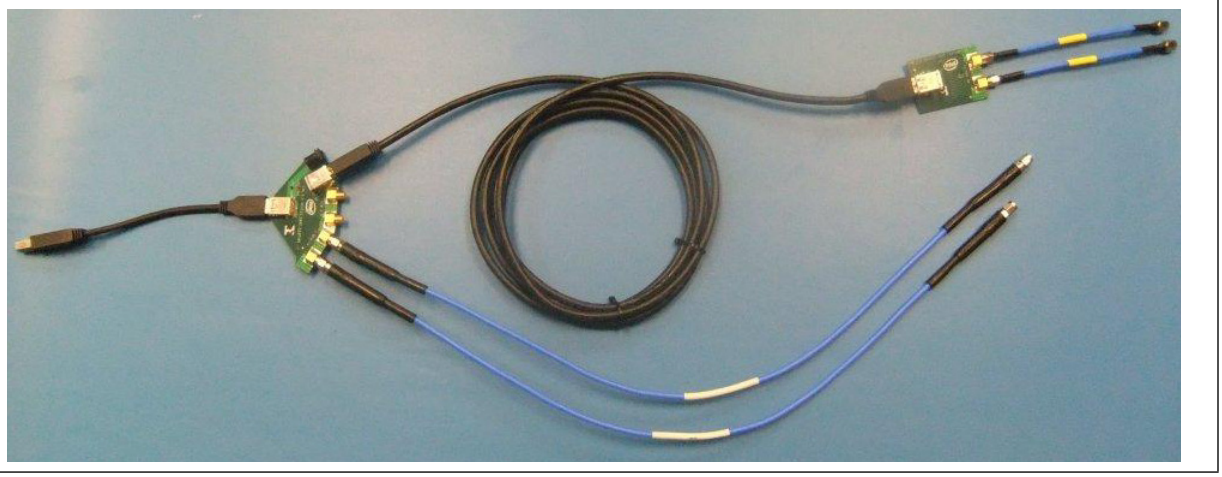

Figure 2.1 USB-IF Upstream Compliance Connections

It is important that the SMA cables be phase and attenuation matched and connected to the test boards with the proper torque (5in-lb).

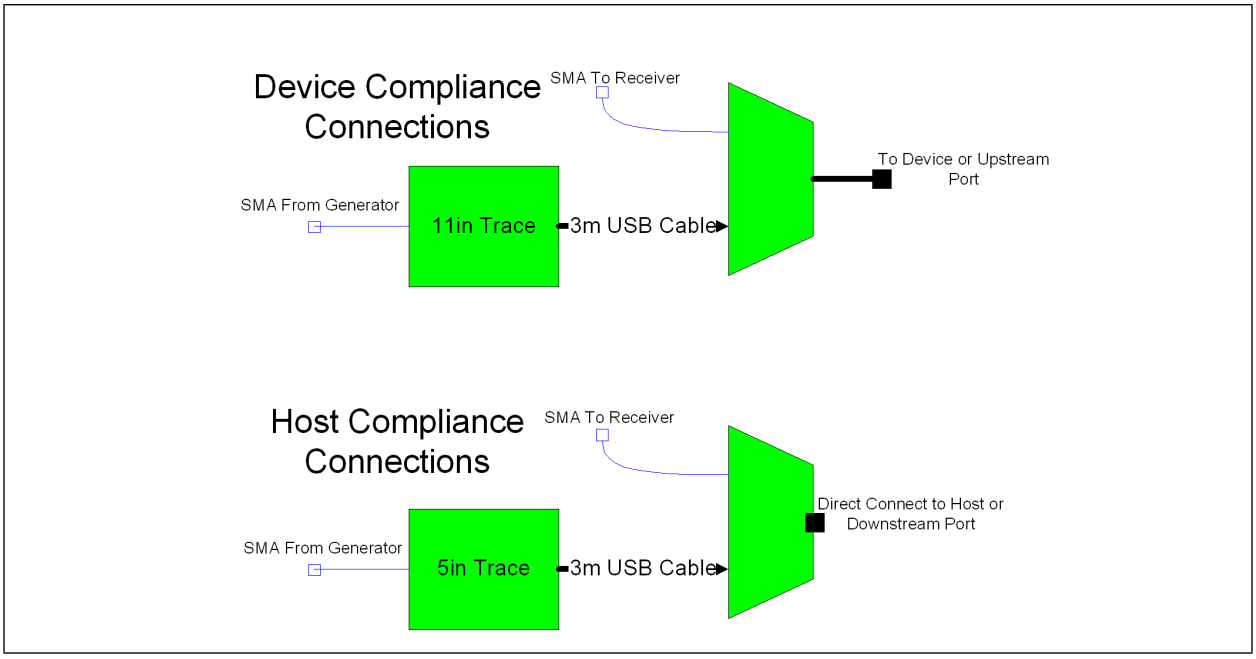

Figure 2.2 Device and Host Compliance Connections

2.2 Training

The data generator begins each test by configuring the SuperSpeed (SS) port to enter loopback, the procedure is as follows:

1. Data generator transmits Low Frequency Periodic Signals (LFPS) to imitate SS communication.
2. Device Under Test (DUT) responds with LFPS signal handshake.
3. Data generator transmits Training Sequence Signal (TSEQ) with the proper noise applied.
4. DUT trains to the TSEQ signal and adapts the internal filters for best performance.
5. Data generator transmits Training Sequence ordered set with loopback bit enabled (TS1)
6. DUT responds with TS1 or TS2 while training, then sends 8 TS2 or TS1 signals when complete.
7. Data generator transmits TS2 also with loopback set 16 times or more.
8. DUT responds with identical TS2 patterns.
9. Data generator prepares for data packets and the DUT is in loopback.

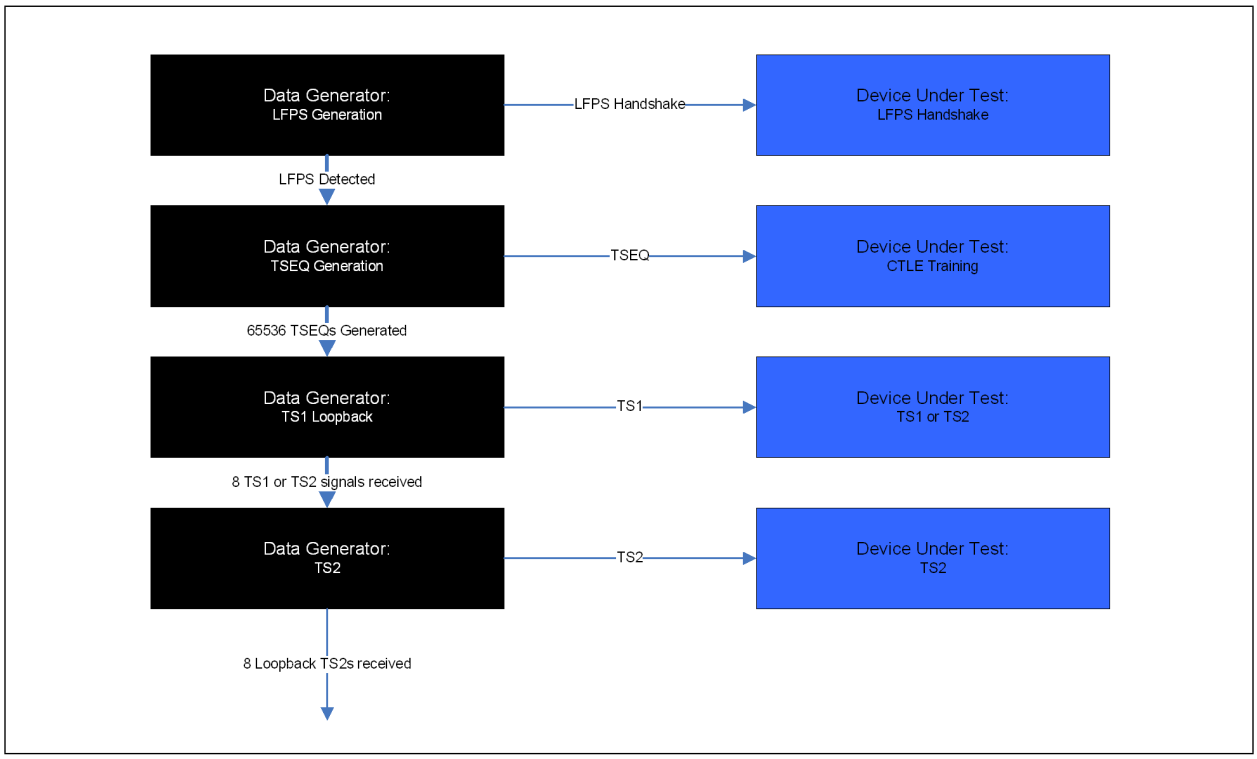

Figure 2.3 Loopback Training Sequence

2.3 Noise Test

After the DUT is trained, the data generator will then generate a random data pattern for about 6s or 3^{10} bits. The DUT loops back the same data and the two data sets are compared, only one error is allowed. The test then repeats for each noise profile as follows:

1. 400ps of noise at 500kHz
2. 200ps of noise at 1MHz

3. 100ps of noise at 2MHz
4. 40ps of noise at 4.9MHz
5. 40ps of noise at 10MHz
6. 40ps of noise at 20MHz
7. 40ps of noise at 33MHz
8. 40ps of noise at 50MHz

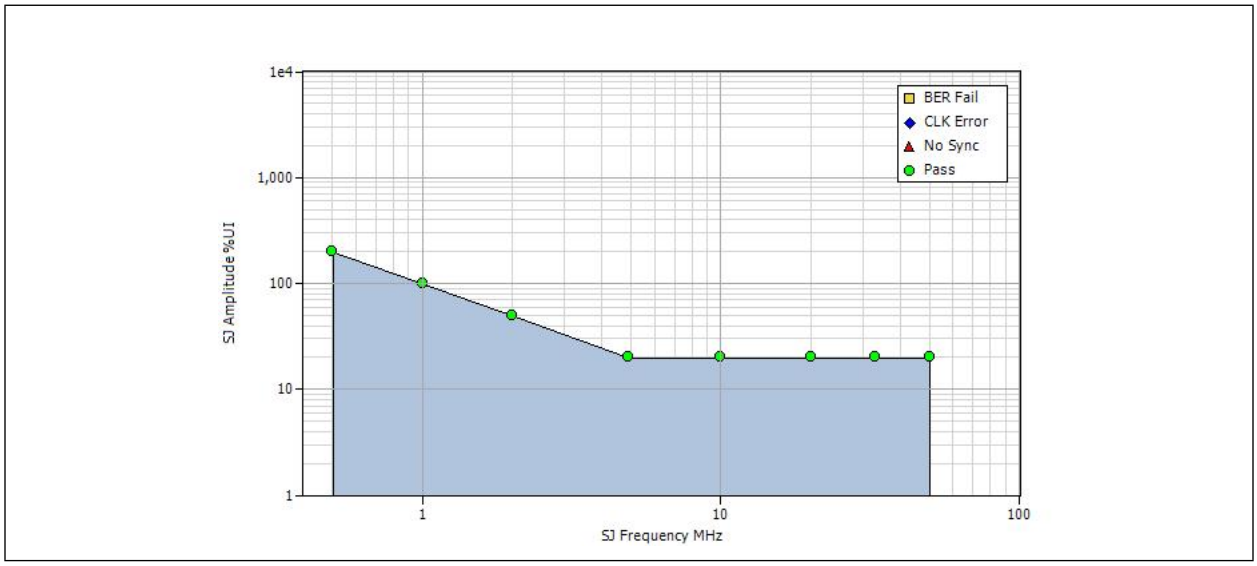

Figure 2.4 JTOL Test Results

3 JTOL Calibration

Before a test can be run, the system needs to be calibrated. The calibration procedure contains many steps and many sources of error. It is always important to check and confirm the calibration before beginning any compliance test.

3.1 De-emphasis Calibration

De-emphasis calibration is done differently on different test solutions, although the fundamental test itself is consistent across all platforms, every test vendor uses their own tool to calculate the de-emphasis. The data generator is connected directly to an oscilloscope through short SMA cables. The oscilloscope then measures the De-emphasis on a large packet of random data (generally 20us of a 5GHz signal). The De-emphasis is then calculated and adjusted to ensure it is within the -3dB specification.

This de-emphasis calibration is important because the waveform changes across the PCB trace and 3m test cable, this affects the quality of the eye that the receiver sees. The Microchip SuperSpeed receivers are able to successfully compensate for small de-emphasis calibration errors through the adapt circuitry. This allows the Microchip solutions to be compatible with more devices and cable lengths on the market. This variation in cable length and receiver type cannot be tested in a compliance environment due to time constraints.

3.2 Random Jitter Calibration (RJ)

After the de-emphasis is calibrated, the data generator is connected through the certification test fixtures to the scope. The generator is set to generate a clean sine wave (CP1) with only the random jitter applied. The USB-IF SigTest tool (see references) is then used to process the signal and calculate the RJ. RJ is adjusted until it falls within the specification (2.42ps +/-10%). The sine wave is used to give the cleanest signal through the loss of the cable for a consistent RJ measurement.

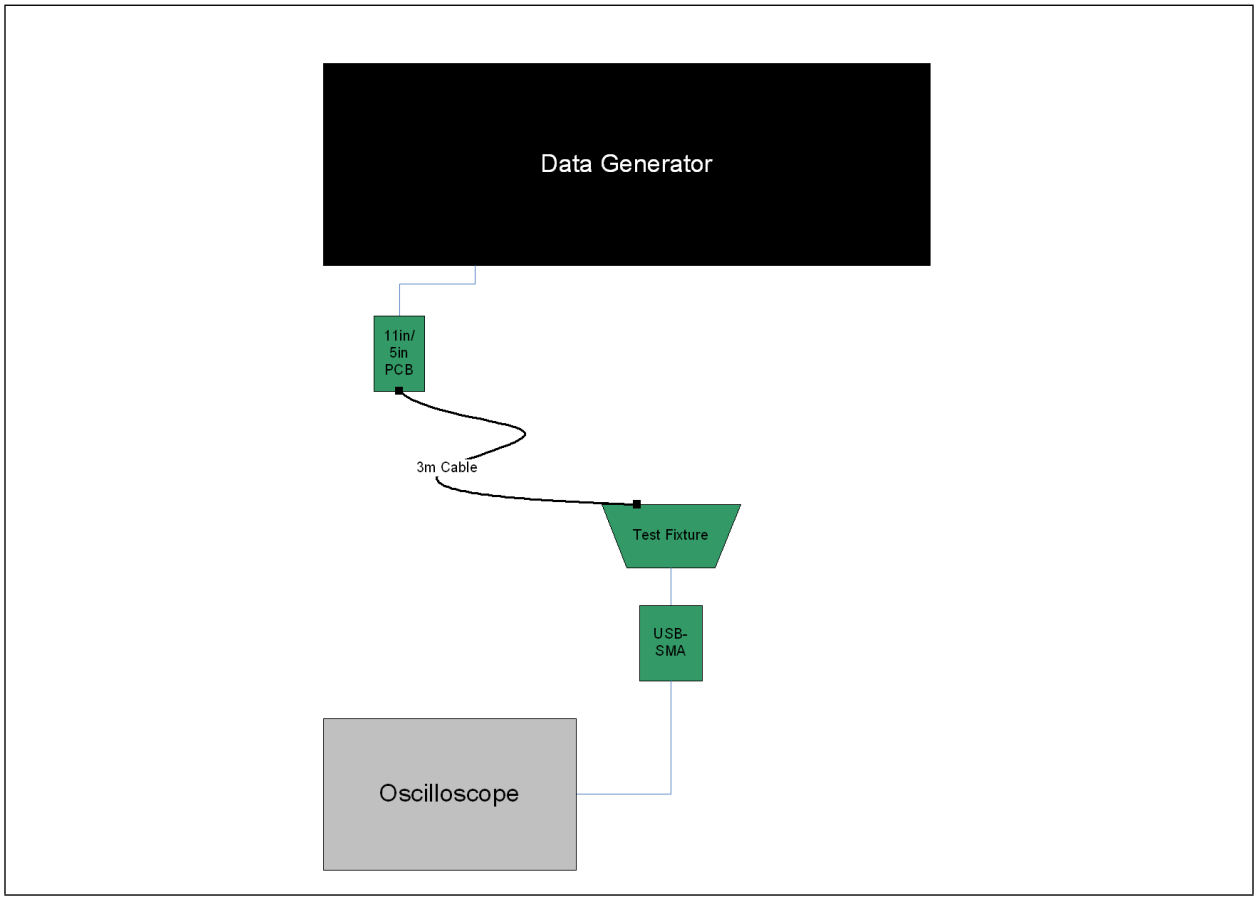

Figure 3.1 RJ, SJ and Amplitude Calibration Setup

Calibrating the random jitter through the compliance test fixtures presents a few challenges. The first challenge is repeatability; jitter measurements always have uncertainty incorporated into the results. The second challenge is that the jitter introduced is random which adds uncertainty to the measurement. There will be variation between different scope captures even though everything else is constant.

3.3 Sinusoidal Jitter Calibration (SJ)

With SJ calibration, the data generator is set to generate a random data pattern (CP0) with random jitter enabled. The signal is then passed through the test fixtures into the scope. Sigtest is again used to calculate the total jitter of the signal. Sinusoidal jitter is than applied and the measurement is repeated. The difference in the total jitter for both measurements is used to calibrate the SJ setting on the data generator.

With this procedure, the errors in the measurements are added each time the measurement is taken. This creates a lot of variation between sequential calibration runs. The first source of error is that the data pattern is random instead of a uniform sine wave, this creates some small differences between total jitter measurements for each scope capture. The second source of error is that the jitter is measured at the end of the compliance test fixture. The high frequency loss through the PCB traces and 5m cable causes the edges of the waveforms to become smoother and smaller. Because the edges aren't as sharp, the jitter calculations will not be as consistent because jitter is calculated based on the edge placement. Combine this uncertainty with the errors introduced by the random jitter applied previously, then take the measurement twice. It is possible that two calibration runs could yield data generator set points up to 4ps apart. That is equal to the entire range of specification.

3.4 Amplitude Calibration

Finally, the RJ, SJ and de-emphasis is applied to a random data pattern (CP0) and the signal is passed through the compliance test fixtures. Sigtest is used to calculate the eye measurements of the signal, and the amplitude is adjusted to ensure that the smallest possible signal is being generated. The receiver is tested with the minimum allowable margin on the eye of the random data.

Because all of these measurements have some variation in their results, it is recommend that the calibration be run three to five times to check the reliability of the calibration algorithm.

4 External Noise Sources

Because the receiver test introduces noise into the signal coming into the DUT, any extra noise is just going to add to the noise generated by the instrument. There are many external sources of noise in a system that can impact the tested tolerance of the receiver. Power supplies, connector quality and PCB loss all can impact the results of the JTOL test.

4.1 Power Supply/Ground Noise

If the voltage applied to the chip contains noise, it will be added to the signal as it travels through the receivers buffers. This noise adds jitter to the total signal, causing the JTOL test results to be less than that of an ideal system. To reduce this noise there are a few PCB layout techniques that can be used.

Selecting a quieter noise source is the first step in cleaning up this noise. Then isolating the supply from other system components through a ferrite bead or inductor can clean the system up further. Ensure that the ferrite bead or inductor has a low resistance so the supply does not drop. Finally, adding 0.1uF bypass caps can filter out the high frequency noise that may still remain on the supply. Cleaning up these supplies is necessary for consistent operation of the receiver and the entire chip

itself. Please refer to the PCB layout guidelines for the particular Microchip product being used for more details.

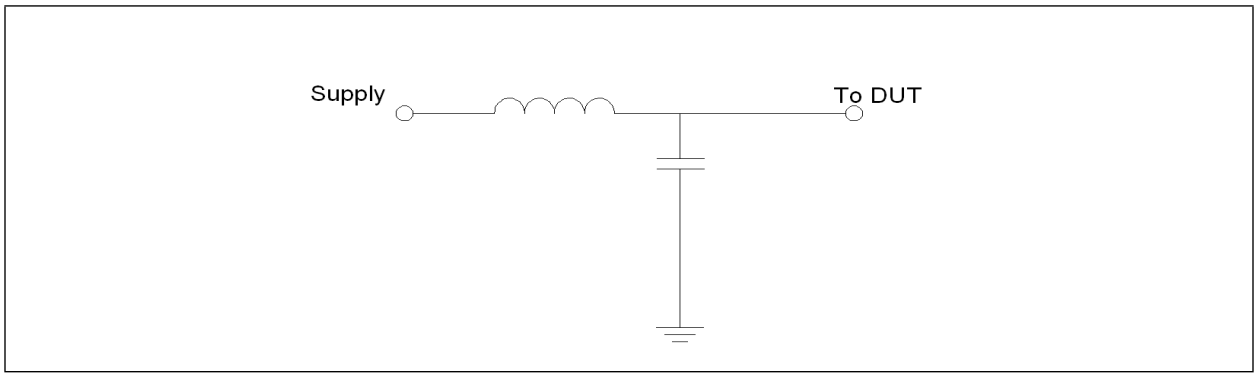

Figure 4.1 Power Supply Isolation Circuit

4.2 Connector Quality

Because USB 3.0 SuperSpeed signaling is in the 2.5GHz, not all connectors are equal in performance. The quality of the connector (impedance, isolation, crosstalk etc) can greatly impact the amount of noise that can be added to the signal. The standard B connector is known to affect the signal quality the most. The large size of the B connector has more potential for impedance mismatch. Also, the paths that connect the USB lines to the PCB board can vary from vendor to vendor, each with a different noise profile. The quality of these paths can introduce more noise into the signals through ground isolation and crosstalk. It is recommended to try samples of different USB connectors to find one that is optimal for your system.

The standard A connector also has potential problems, but because the profile is smaller, the distance from the USB-A line to the PCB is much shorter. Also there are surface mount options for this connector that can also clean up the signal.

The micro B connector has the best performance of the connectors because of its small form factor and the surface mount connection to the board.

4.3 PCB Trace

The signal path from the DUT to the connector also has an impact on the JTOL results. The biggest impact is the length of the trace itself and the loss of the dielectric. The 5GB/s signal will lose amplitude along the trace from the connector to the DUT through the dielectric material of the PCB. The performance of the receiver is tied to the amplitude of the signal, so if the trace is shorter, the amplitude at the receiver will be higher and the receiver will perform better. Because the device or upstream hub port JTOL tests have the lowest initial amplitude, the traces from the DUT to those connectors should be the shortest.

Another factor that can affect the JTOL performance of a USB device is branching. The ideal path of the signal should have one source and one destination. If the trace branches in any way the signal will be affected. If the traces branch to another terminated receiver, much of the signal energy will be lost which affects JTOL performance. If the traces branch to an unterminated test point, the signal will be reflected back to the main trace adding noise which will cause the receiver to have sub optimal JTOL results. This open circuit stub is also present in the standard through hole connector, so how the traces are routed to the connector are important. The ideal option would be to have no through hole connector and have the traces go directly from the DUT to the connector.

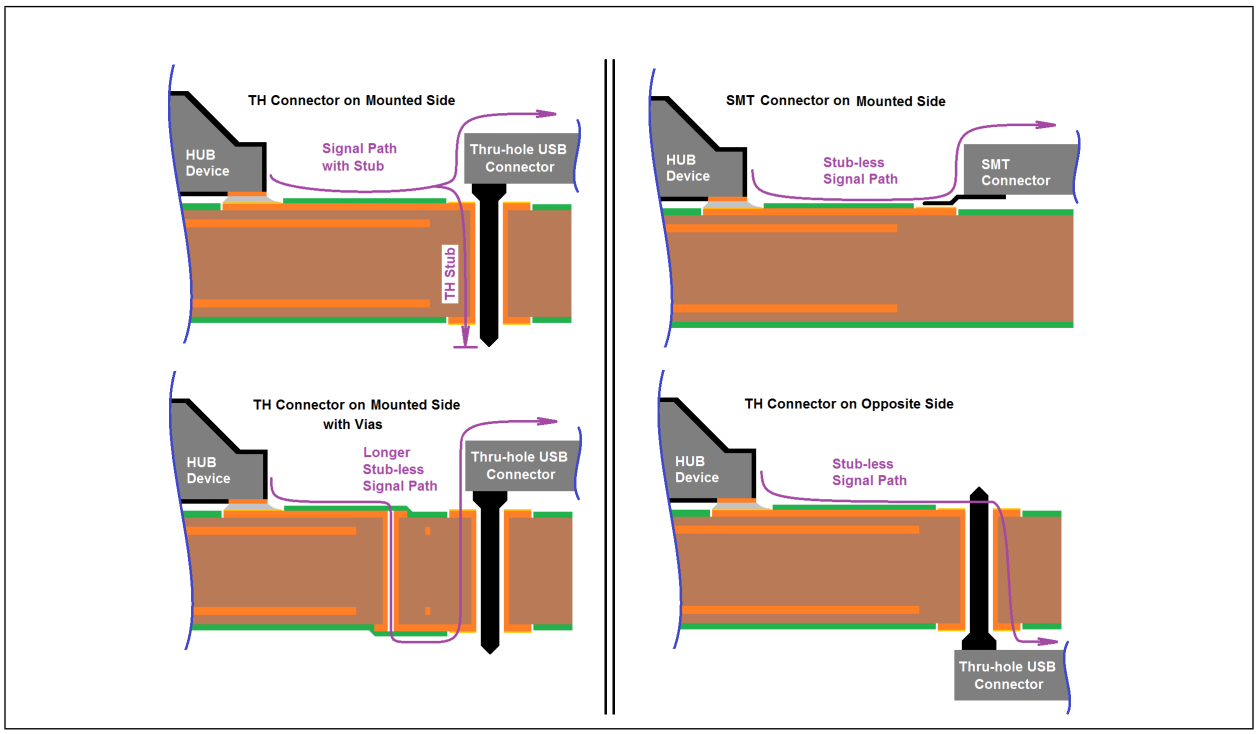

Figure 4.2 PCB Trace Paths to a Thru-Hole Connector

5 Optimal JTOL

Optimal JTOL results can be achieved if the following items are checked:

1. Confirm that the test fixtures used are high quality cables and connectors. The bandwidth of the SMA cables should be high enough to pass the USB3 signals through, and the phase of the cables should be matched. If there is something wrong with the SMA cables, the whole test is invalid.
2. Check that the calibration of the test system is correct, there is a lot of variation in the calibration results, so multiple runs may be required to trust the final results.
3. The USB system needs to have the right connectors installed with the cleanest, shortest possible traces going from the connector to the device.

Careful attention to the USB system design and test environment is necessary to get a fully compliant USB device. The high speed signals require

6 Application Note Revision History

Table 6.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.01 (05-31-13)	Document Release	