

## Microchip KSZ9131MNX to LAN8831 Migration Guide

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### INTRODUCTION

This document is for customers with an existing KSZ9131MNX board design migrating to the LAN8831 for their board design. This features a comparison of hardware and software register specifications between the two products. Details on the hardware and software of each device can be found on each product's Microchip web page.

[Table 1](#) summarizes the hardware attribute differences between the KSZ9131MNX and the LAN8831. [Table 2](#) summarizes the register differences between the KSZ9131MNX and the LAN8831. For LAN8831 RGMII usage, please see the [AN4742 KSZ9131RNX to LAN8830 Migration Guide](#).

**TABLE 1: HARDWARE DIFFERENCES BETWEEN KSZ9131MNX AND LAN8831**

| Device Attribute    | KSZ9131MNX  | LAN8831   |
|---------------------|---|---|
| Analog Low Voltage  | AVDDL – 1.2V  | VDDAL – 1.1V  |
| Digital Low Voltage | DVDDL – 1.2V  | VDD – 1.1V  |
| Management Modes    | GMII/MII Only   | RGMII_EN Strap PU: RGMII<br>RGMII_EN Strap PD: GMII/RGMII   |
| MODE Strapping Pins | <b>MODE[3:0]</b><br>– 0001: GMII mode – Advertise all capabilities (10/100/1000 speed Half-/Full-duplex), except 1000BASE-T Half-duplex<br>– 0100: NAND Tree<br>– 0111: Chip Power Down<br>– 1001: GMII/MII mode – 10/100 FD/HD, PME on LED1<br>– 1001: GMII/MII mode – 10/100 FD/HD, PME on LED2 | <b>MODE[4:0]</b><br>– 10000: GMII mode – Advertise all capabilities (10/100/1000 speed Half-/Full-duplex), except 1000BASE-T Half-duplex, EEE Disabled<br>– 11000: GMII mode – Advertise all capabilities (10/100/1000 speed Half-/Full-duplex), except 1000BASE-T Half-duplex, EEE Enabled<br>– 00100: NAND Tree<br>– 00111: Device Power Down mode<br>– 01000: Chip Power Down – PLL Enabled<br>– 01001: Chip Power Down – PLL Disabled<br><br>Note that PME can map to any GPIO. |
| PME                 | Needs mode setting to set LED1/LED2 as PME signal   | No mode setting needed to set PME. Registers set the GPIO pin to set as PME signal.   |
| ALL-PHYAD           | Pin 53 can be set to respond to the KSZ9131MNX PHY Address (from PHYAD[2:0]) and PHY Address 0.   | Pin 16 can be set to respond to the LAN8831 PHY Address (from PHYAD[4:0]) and PHY Address 0.  |
| Fast Link Failure   | None  | Can indicate link failure in 1 ms when enabled at 100/1000  |
| PHYAD Strap Range   | PHYAD[2:0]  | PHYAD[4:0]  |

**TABLE 1: HARDWARE DIFFERENCES BETWEEN KSZ9131MNX AND LAN8831**

| Device Attribute                    | KSZ9131MNX              | LAN8831   |
|-------------------------------------|-------------------------|---|
| LED Modes                           | No straps for LED modes | LED mode strap for Individual (PU) and Tri-color (PD) |
| LED Polarity Control                | None                    | LEDPOL[5:1] available                                 |
| LEDs                                | 2 LEDs (LED1, LED2)     | 5 LEDs (LED1, LED2, LED3, LED4, LED5)                 |
| GPIOs                               | None                    | 10 GPIOs (GPIO0-GPIO10)                               |
| Shorted-center Tap Magnetic Support | None                    | MAGJACK Strap   |
| Quiet-WIRE                          | Supported               | No Functionality                                      |

**TABLE 2: REGISTER DIFFERENCES BETWEEN KSZ9131MNX AND LAN8831**

| Register           | KSZ9131MNX  | LAN8831  |
|--------------------|---|--|
| 16h                | Bits[15:8] – Reserved<br>Bits[7:4] – LED2 Configuration<br>Bits[3:0] – LED1 Configuration   | Bits[15:12] - LED4 Configuration<br>Bits[11:8] - LED3 Configuration<br>Bits[7:4] - LED2 Configuration<br>Bits[3:0] - LED1 Configuration  |
| 17h                | Bits 15, 13, [9:7], [4:2] – Reserved<br>Bits[6:5] – LED Pulse Stretch Enables<br>Bits[1:0] – LED Combination Disables   | Bits 15, 13, 9, 4 – Reserved<br>Bits[8:5] – LED Pulse Stretch Enables<br>Bits[3:0] – LED Combination Disables  |
| 19h                | Bit 15 – Reserved<br>Bit 1 – MDIO Drive<br>Bit 0 – Reserved   | Bit 15 – MDIO Buffer Type<br>Bit 14 – INT Buffer Type<br>Bits[13:8] LED Buffer Type<br>Bit[7] – PME Polarity<br>Bits[5:0] – LED Polarity   |
| 1Bh                | Bit 15 – Jabber Interrupt Enable<br>Bit 14 – Receive Error Interrupt<br>Bit 13 – Page Receive Interrupt<br>Bit 12 – Parallel Detect Fault Interrupt<br>Bit 11 – Link Partner Acknowledgment Interrupt<br>Bit 10 – Link Down Interrupt<br>Bit 9 – Remote Fault Interrupt<br>Bit 1 – Remote Fault Interrupt | Bits[15:12], 9 – Reserved<br>Bit 11 – Energy Not Detected Interrupt<br>Bit 10 – Energy Detected Interrupt<br>Bit 1 – ADC FIFO Error Interrupt  |
| Address 2, Reg. 1h | Bits[13:8] – Reserved   | Bits[13:8] – LED Polarity  |
| Address 2, Reg. 2h | Bits 14, 8, 0 – Reserved<br>Bit 11 – GMII mode with PME_N2 mapped to INT_N<br>Bit 9 – GMII mode with PME_N1 mapped to LED1<br>Bit 7 – Chip Power-Down Strap Override<br>Bit 4 – NAND Tree Strap Override<br>Bit 1 – GMII/MII Strap Override   | Bits 11, 7, 0 – Reserved<br>Bit 14 – MagJack Strap<br>Bit 9 – Software Power Down w/ PLL Disabled<br>Bit 8 – Software Power Down w/ PLL Enabled<br>Bit 4 – NAND Tree Strap Override<br>Bit 1 – GMII/MII Strap Override<br>Bit 0 – RGMII mode                                   |
| Address 2, Reg. 3h | Bits 14, 8, 0 – Reserved<br>Bit 11 – GMII mode with PME_N2 mapped to INT_N Status<br>Bit 9 – GMII mode with PME_N1 mapped to LED1 Status<br>Bit 7 – Chip Power-Down Strap Override Status<br>Bit 4 – NAND Tree Strap Override<br>Bit 1 – GMII/MII Strap Status  | Bits 11, 7, 0 – Reserved<br>Bit 14 – MagJack Strap Status<br>Bit 9 – Software Power-down w/ PLL Disabled Status<br>Bit 8 – Software Power-down w/ PLL Enabled Status<br>Bit 4 – NAND Tree Strap Override Status<br>Bit 1 – GMII/MII Strap Status<br>Bit 0 – RGMII Strap Status |

**TABLE 2: REGISTER DIFFERENCES BETWEEN KSZ9131MNX AND LAN8831**

| Register                | KSZ9131MNX                    | LAN8831  |
|-------------------------|-------------------------------|--|
| Address 2,<br>Reg. 4h   | Reserved (not used)           | When LAN8831 is in RGMII mode:<br>Bits[7:4] – RX_CTL Pad Skew<br>Bits[3:0] – TX_CTL Pad Skew<br><br>When LAN8831 is in GMII mode, Bits[7:0] should remain unchanged.   |
| Address 2,<br>Reg. 5h   | Reserved (not used)           | When LAN8831 is in RGMII mode:<br>Bits[15:12] – RXD3 Pad Skew<br>Bits[11:8] – RXD2 Pad Skew<br>Bits[7:4] – RXD1 Pad Skew<br>Bits[3:0] – RXD0 Pad Skew<br><br>When LAN8831 is in GMII mode, Bits[15:0] should remain unchanged. |
| Address 2,<br>Reg. 6h   | Reserved (not used)           | When LAN8831 is in RGMII mode:<br>Bits[15:12] – TXD3 Pad Skew<br>Bits[11:8] – TXD2 Pad Skew<br>Bits[7:4] – TXD1 Pad Skew<br>Bits[3:0] – TXD0 Pad Skew<br><br>When LAN8831 is in GMII mode, Bits[15:0] should remain unchanged. |
| Address 2,<br>Reg. 40h  | Bits[15:0] – Bad SFD Count Lo | Reserved (Not shown)   |
| Address 2,<br>Reg. 41h  | Bits[15:0] – Bad SFD Count Hi | Reserved (Not shown)   |
| Address 1C,<br>0Dh      | Bit 15 – LDO Enabled          | Bit 15 – LDO Enabled<br>Bits 14:12 – LDO Reference Tune  |
| Address 1F,<br>Reg. 13h | Bit 10 – Quiet-WIRE Enable    | Reserved (Not shown)   |

Additional features, such as EEE, MSE/SQI, and self-test for frame generation or checking, are accessible in the Indirect Address Registers.

## APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

| Revision Level & Date     | Section/Figure/Entry | Correction |
|---------------------------|----------------------|------------|
| DS00004744A<br>(09-19-22) | Initial release.     |            |

NOTES:

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