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Component Placement Checklist for the LAN7801, 64-pin SQFN Package

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Component Placement Checklist for LAN7801

Information Particular for the 64-pin SQFN Package

RGMII Interface:

1. When physically placing the LAN7801 in an RGMII application, the designer should be aware of the relative trace lengths determined by the relationship of the LAN7801 and the Phy in the application. By placing the Phy too far away from the LAN7801, this may result in operational problems associated with excessive trace lengths.

2. SMSC recommends the final RGMII interface trace lengths to remain under 6” long.

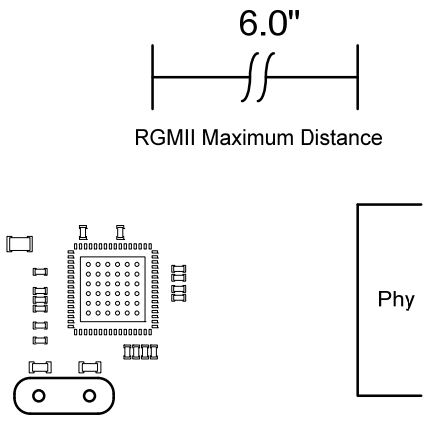

Figure No. 1

RGMII Series Terminations:

1. If the designer has elected to use impedance matching terminations in his design, these series resistors should be placed as close as possible to the source of the driving signal.

2. The RGMII Series Terminations should be considered critical components. To ensure the best signal integrity and good EMI performance, these critical components should be placed on the component side of the PCB. This will ensure that these components will be referenced to a contiguous ground plane reference on Layer 2 of the design. This will also minimize the use of vias in routing these signals.

+3.3V Power Supply Connections:

1. Place the VDD33A decoupling capacitor for the LAN7801 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

2. Place the VDD33_REG_IN decoupling capacitor for the LAN7801 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

3. Place the VDD_SW_IN decoupling capacitor for the LAN7801 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

VDDVARIO Power Supply Connections:

1. Place the (7) VDDVARIO decoupling capacitors for the LAN7801 SQFN as close to each power pin as possible. Using an SMD_0603 package will make this task easier.

+2.5V Power Supply Connections:

1. Place the VDD25_REG_OUT low ESR capacitor for the LAN7801 SQFN as close to the power pin as possible.

2. Place the VDD25_REG_OUT bypass capacitor for the LAN7801 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

+1.2V Power Supply Connections:

1. Place the 3.3 uH inductor as close as possible to the VDD12_SW_OUT (pin 20) on the LAN7801.

2. Also place the 22 uF Low ESR capacitor as close as possible to the 3.3 uH inductor and the VDD12_SW_OUT (pin 20) on the LAN7801.

3. Place the VDD12_SW_OUT bypass capacitor for the LAN7801 SQFN as close to the 3.3 uH inductor as possible. Using an SMD_0603 package will make this task easier.

4. Keep the VDD12_SW_OUT node away from any other sensitive circuitry (address lines, data lines, Ethernet traces, other components, etc.) as this node is very noisy.

5. Place the VDD12_SW_FB decoupling capacitor for the LAN7801 SQFN as close to the power pin as possible. Using an SMD_0603 package will make this task easier.

6. Place the (2) VDD12CORE decoupling capacitors for the LAN7801 SQFN as close to each power pin as possible. Using an SMD_0603 package will make this task easier.

7. Place the ferrite bead associated with the VDD12A power rail as close as possible to the (3) VDD12A power pins on the LAN7801.

8. Place the (3) VDD12A decoupling capacitors for the LAN7801 SQFN as close to each power pin as possible. Using an SMD_0603 package will make this task easier.

9. Place the VDD12A 1.0 uF, low ESR cap close to pin 37 in the board design.

Ground Connections:

1. There are no component placement issues associated with the LAN7801 SQFN ground connections. Since the PCB design has an all encompassing digital ground plane, the ground plane connections will automatically be as short as possible.

Crystal Connections:

1. Place the 25.000 MHz crystal and the associated 15 – 33 ρF capacitors as close together as possible and as close to the LAN7801 SQFN (XI, pin 52 & XO, pin 53) as possible. They should form a tight loop. Keep the crystal circuitry away from any other sensitive circuitry (address lines, data lines, Ethernet traces, etc.)

2. Place all the crystal components on the component side of the PCB with a digital ground plane layer on the next layer. This will minimize vias in the circuit connections and assure that all the crystal components are referenced to the same reference plane.

EEPROM Interface:

1. There are no component placement issues associated with the Phy Interface of the LAN7801 SQFN.

REF_REXT Resistor:

1. Place the REF_REXT resistor as close to pin 1 of the LAN7801 SQFN as possible.

REF_FILT Capacitor:

1. Place the REF_FILT capacitor as close to pin 2 of the LAN7801 SQFN as possible.

USBRBIAS Resistor:

1. Place the USBRBIAS resistor as close to pin 49 of the LAN7801 SQFN as possible.

Required External Pull-ups/Pull-downs:

1. There are no component placement issues associated with the External Pull-ups / Pull-downs of the LAN7801 SQFN.

USB Interface:

1. For board applications where the USB 3.0 link is between two devices intra-board, the SSTX and SSRX channels must be crossed over. Two DC blocking caps (0.1 uF) should be placed as close as possible to USB3_TXDP & USB3_TXDM on the LAN7801 device. Two more DC blocking caps should be placed on the transmit pins of the other USB 3.0 device.

2. For board applications where the USB 3.0 link uses a USB connector, the RX and TX channels must not be crossed over to the connector. The cross over function is accomplished in the USB cable. Two DC blocking caps (0.1 uF) should be placed as close as possible to USB3_TXDP & USB3_TXDM on the USB connector. Two more DC blocking caps should exist on the transmit pins of the other USB 3.0 device on the other side of the cable.

Miscellaneous:

1. Bulk capacitors for each power plane can reside anywhere on the plane they serve.

2. Place the SMD_1210 Digital Ground / Chassis Ground shorting resistor near the USB connector in a logical place to short the two planes.