AN4754

Using Microchip Bridge Controllers with External Ethernet PHYs

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1.0 INTRODUCTION

Microchip offers several USB and PCIe® to Ethernet bridge controllers that may connect to an external Ethernet PHY. This allows for flexibility to utilize different Ethernet standards such as BASE-T1 for single twisted pair cabling or BASE-X for optical cables. Microchip offers several options for Ethernet PHYs, and PHYs from other vendors are also supported as long as they support standard MDIO and MII/RGMII interfaces.

TABLE 1: MICROCHIP ETHERNET BRIDGE CONTROLLERS WITH EXTERNAL PHY SUPPORT

Product	Host Connection	Maximum Ethernet Speed	MII	RMII	GMII	RGMII	Recommended Microchip PHY Options	PHY Notes
LAN9500A	USB2.0	100 Mbit/s	X	—	—	—	KSZ8081MNX	10/100BASE-T Copper PHY
			X	—	—	—	LAN8740A	10/100BASE-T Copper PHY
			X	—	—	—	LAN8670/LAN8672	10BASE-T1S Copper PHY
			X	—	—	—	LAN8770	100BASE-T1 Copper PHY
LAN89530 (Automotive)	USB2.0	100 Mbit/s	X	—	—	—	KSZ8081MNL	10/100BASE-T Copper PHY
			X	—	—	—	LAN8770	100BASE-T1 Copper PHY
LAN9730	HSIC	100 Mbit/s	X	—	—	—	KSZ8081MNX	10/100BASE-T Copper PHY
			X	—	—	—	LAN8740A	10/100BASE-T Copper PHY
			X	—	—	—	LAN8670/LAN8672	10BASE-T1S Copper PHY
			X	—	—	—	LAN8770	100BASE-T1 Copper PHY
LAN89730 (Automotive)	HSIC	100 Mbit/s	X	—	—	—	KSZ8081MNL	10/100BASE-T Copper PHY
			X	—	—	—	LAN8770	100BASE-T1 Copper PHY
LAN7801	USB3.0	1000 Mbit/s	—	—	—	X	KSZ9131	10/100/1000BASE-T Copper PHY
			—	—	—	X	VSC8541	10/100/1000BASE-T Copper PHY
			—	—	—	X	LAN8770R	100BASE-T1 Copper PHY
LAN7431	PCIe 3.1	1000 Mbit/s	—	—	—	X	KSZ9131	10/100/1000BASE-T Copper PHY
			—	—	—	X	VSC8541	10/100/1000BASE-T Copper PHY
			—	—	—	X	LAN8770R	100BASE-T1 Copper PHY

1.1 Sections

This document includes the following topics:

1.2 References

The following documents should be referenced when using this application note. See your Microchip representative for availability.

- *LAN9500A Data Sheet* (www.microchip.com/DS00001875)
- *LAN89530 Data Sheet* (www.microchip.com/DS60001347)
- *LAN9730 Data Sheet* (www.microchip.com/DS00001946)
- *LAN89730 Data Sheet* (www.microchip.com/DS60001348)
- *LAN7801 Data Sheet* (www.microchip.com/DS00002123)
- *LAN7431 Data Sheet* (www.microchip.com/DS00002631)
- IEEE 802.3 Ethernet Standards (a collection of numerous standards)

1.3 Terms and Abbreviations

- **10/100:** Shorthand for an Ethernet interface that supports both 10 Mbit/s and 100 Mbit/s signal rate
- **10/100/1000:** Shorthand for an Ethernet interface that supports 10 Mbit/s, 100 Mbit/s, and 1000 Mbit/s signal rate
- **10BASE-T:** 10 Mbit/s standard defined in IEEE 802.3i-1990 (CL14), requires dual twisted pair Cat3 cable
- **10BASE-T1:** 10 Mbit/s standard defined in IEEE 802.3cg-2019, requires single twisted pair Cat5 cable
- **100BASE-TX:** 100 Mbit/s standard defined in IEEE 802.3u-1995, requires dual twisted pair Cat5 cable
- **100BASE-T1:** 100 Mbit/s standard defined in IEEE 802.3bw-2015 (CL96), requires single twisted pair Cat5e cable
- **100BASE-X:** A term used to describe a collection of various of standards for 100 Mbit/s over fiber optic cable
- **1000BASE-T:** 1000 Mbit/s standard defined in IEEE 802.3ab-1999 (CL40), requires quad twisted pair Cat5 cable
- **1000BASE-T1:** 1000 Mbit/s standard defined in IEEE 802.3bp-2016, requires single twisted pair Cat6A cable
- **1000BASE-X:** A term used to describe a collection of various of standards for 1000 Mbit/s over fiber optic cable
- **GigE:** Shorthand for Gigabit Ethernet supporting 1000 Mbit/s signal rate
- **GMII:** Gigabit Media-Independent Interface
- **HSIC:** High-Speed Inter-Chip (USB)
- **MAC:** Media Access Control
- **MDIO:** Management Data Input/Output
- **MII:** Media-Independent Interface
- **PCIE 3.1:** Peripheral Component Interconnect Express v3.1
- **PHY:** A shorthand term for Ethernet transceiver; may be a standalone, discrete device, or integrated directly into an Ethernet controller
- **RMII:** Reduced Media-Independent Interface
- **RGMII:** Reduced Gigabit Media-Independent Interface
- **SFP:** Small Form-Factor Pluggable
- **USB2.0:** Universal Serial Bus version 2.0
- **USB3.0:** Universal Serial Bus version 3.0

2.0 EXECUTIVE SUMMARY

When working with Microchip bridge controller products with external PHYs, the following points are essential:

- Select a PHY that aligns with the end product speed and necessary feature set.
- If using special features of the PHY (PTP, MACsec, and so on), ensure that the PHY supplier provides and supports drivers for the target operating systems. If a driver is not available, it is usually possible to control a PHY using generic PHY drivers included in Linux® or Windows®, but special features and configuration cannot be set through these drivers.
- Ensure that the PHY MII interface aligns with the available MII/RGMII interface of the Microchip bridge controller. For example, an MII-capable MAC cannot connect to a PHY that only supports RMII.
- Whenever possible, connect the MDIO interface in your schematic—this interface allows for easy PHY control and configuration and is usually essential when using special PHY features.

  Note 1: MDIO-less operation is possible in cases where MDIO simply cannot be used, but has numerous drawbacks and is not usually recommended.

- Verify your schematic design and layout design against the provided design/routing/placement checklists of your specific Microchip bridge controller or PHY. See Section 6.2, "Additional Product-Specific Resources".
- The Ethernet bridge controller must be configured by the end system integrator. Check the selected Ethernet bridge controller product web page for product-specific configuration tools. Pay special attention to the following aspects:
  - *MAC Address*: For systems that connect to the Internet, every bridge controller must be programmed with a unique MAC address. MAC addresses should be procured from IEEE.
  - *MII/RGMII TX and RX Clock Delay*: Ensure that TX and RX clock delay is accounted for in the PCB design, MAC configuration, and/or PHY configuration.
- The selected PHY may also require its own configuration. This is achieved through various means depending on the PHY. Some may be configured solely from MDIO controlled by a generic PHY driver. Other PHYs have many hardware pin-strap options.
- The Ethernet bridge controller OTP or EEPROM must be programmed on the end-product production line. For Linux, this can be achieved using ethtool. For Windows, Microchip provides product-specific programming tools.
- Understand the basics of what Ethernet MAC and PHY actually do. Table 2 lists them down into simplest terms:

TABLE 2: ETHERNET MAC AND PHY FUNCTIONS

Ethernet MAC Functions	Ethernet PHY Function
Transmit: Encapsulate Data: • Add Header Data (including addresses) • Add CRC • Add Preamble (including start frame delimiter) • Ensure inter-frame gap Receive: Detect invalid frames: • Incorrect CRC • Runt Frame • Giant Frame (if Jumbo frame support is not supported) • Misaligned Frame • No Address Match	Physical Coding Sublayer (PCS): • Transmit: - Encode - Scramble - Serialize data • Receive: - Deserialize data - Descramble - Decode - Carrier Sense - Collision Detection Physical Media Attachment sublayer (PMA): • Transmit: - Data bit to data symbol conversion • Receive: - Clock recovery - Data symbol to data bit conversion - Link Monitoring Physical Medium Dependent sublayer (PMD): • Dependent on the standards supported by the PHY • Line drivers/line receivers

3.0 MII/RMII AND GMII/RGMII

There are several Media-Independent Interface (MII) options available for connecting an Ethernet MAC to a PHY. Microchip's bridge controllers support either MII for 10/100 Ethernet connections, or Reduced Gigabit Media-Independent Interface (RGMII) for 10/100/1000 Ethernet connections; however Microchip does offer PHYs and Ethernet switches that support all Reduced Media-Independent Interface (RMII) and Gigabit Media-Independent Interface (GMII).

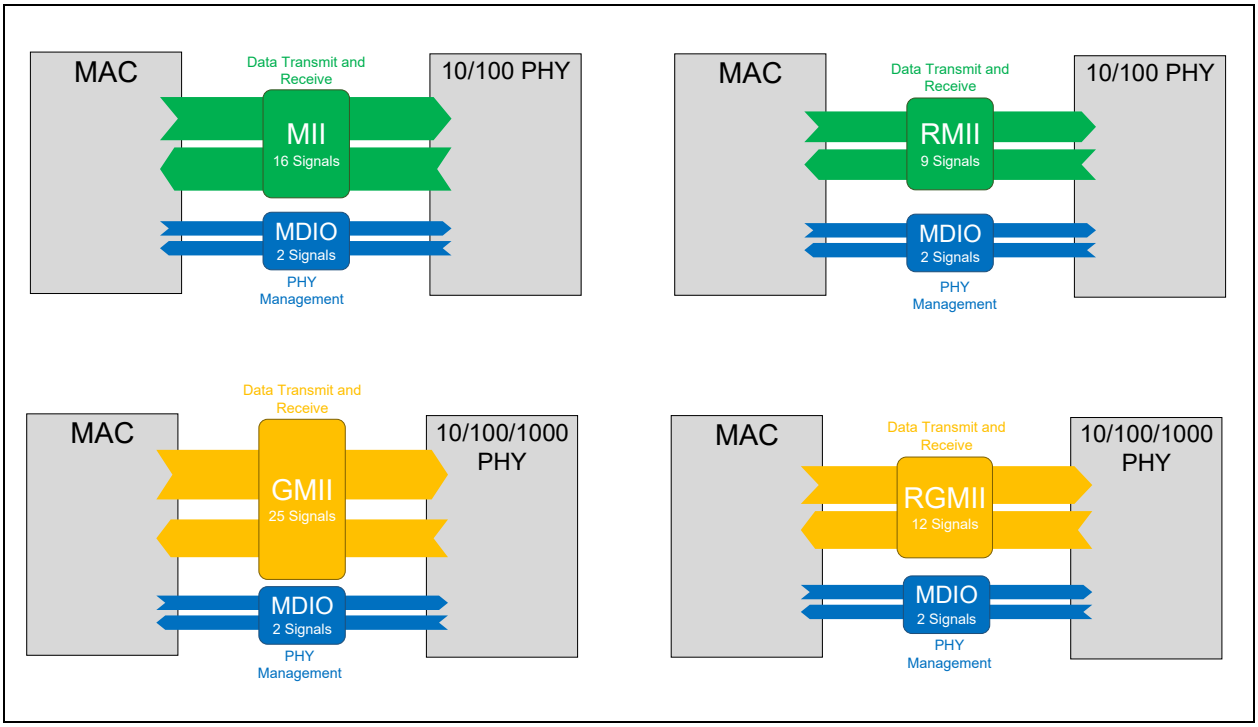
The MII/RMII/GMII/RGMII interface can be used to control PHYs that operate under one of the various twisted pair or optical specifications. The primary differences are:

- MII and RMII support up to 100 Mbit/s
- RMII is the reduced pin count version of MII
- GMII and RGMII support up to 1000 Mbit/s
- RGMII is the reduced pin count version of GMII

Management Data Input/Output (MDIO) is a two-wire bus that allows the controller to configure the PHY as needed. This channel allows the host to interrogate and set important PHY parameters (such as enabling/disabling auto-negotiation, auto-MDIX, and so on). MDIO is technically optional and it is possible to design systems without MDIO as long as both the MAC and PHY can be configured as-needed to operate with one another by other means.

Note: SFP modules do not have MDIO interfaces, so they technically operate without MDIO. However, SFP modules do adhere to a separate management standard through an I^2C channel.

FIGURE 1: MII AND RMII INTERFACES

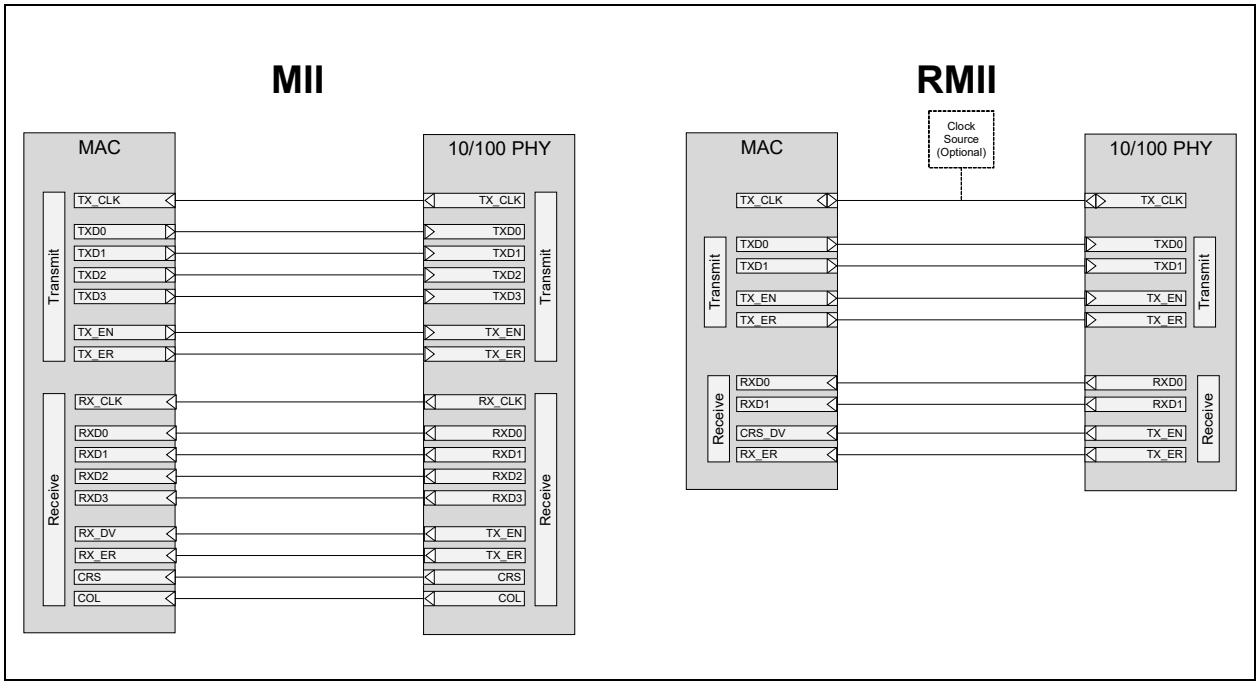


3.1 MII/RMII

The MII was specifically designed as a standard connection for 100 Mbit/s Ethernet between the media access control (MAC) and a PHY. RMII was introduced later to offer a lower pin count option while maintaining full functionality of the MII interface.

Note: Microchip does not offer any bridge controllers that support RMII. The RMII details are shown in this document for completeness.

FIGURE 2: MII AND RMII INTERFACES



3.1.1 MII SIGNAL DETAILS

The MII has the following fundamental properties:

- TX_CLK and RX_CLK are separate clocks relative to their respective directions (transmit and receive). Both are driven by the PHY.
- Clock frequency is 25 MHz in 100 Mbit/s mode and 2.5 MHz in 10 Mbit/s mode.
- Both transmit and receive have four signals for data (that is, 4-bits wide).
- Data lines are sampled relative to the rising clock edge.

MII signals are described in Table 3.

TABLE 3: MII SIGNALS

Direction	Signal Name	Description
PHY→MAC	TX_CLK	**Transmit Clock** Free-running 2.5 MHz (in 10 Mbit/s mode) or 25MHz clock (in 100 Mbit/s mode).
MAC→PHY	TXD[0:3]	**Transmit data bit signals** (four separate parallel signals)
MAC→PHY	TX_EN	**Transmit Enable** This signal is asserted during frame transmission.

TABLE 3: MII SIGNALS (CONTINUED)

Direction	Signal Name	Description
MAC→PHY	TX_ER	**Transmit Error** This signal may be asserted during frame transmission to instruct the PHY to intentionally corrupt the frame. This is done so that the recipient of the frame will detect this packet as corrupted. This can be used as kind of 'frame abort' function in the case that a problem is detected in the midst of active frame transmission. This signal is optional per specification.
PHY→MAC	RX_CLK	**Receive Clock** Free-running 2.5 MHz (in 10 Mbit/s mode) or 25 MHz clock (in 100 Mbit/s mode)
PHY→MAC	RXD[0:3]	**Transmit data bit signals** (four separate parallel signals)
PHY→MAC	RX_DV	**Receive Data Valid** Asserts when received data is valid. Some preamble bits may be missed due to slight delay in assertion of the signal, but must be asserted sufficiently fast to ensure that the start of frame delimiter byte is received by the MAC.
PHY→MAC	RX_ER	**Receive Error** Asserts to indicate that the received data was not properly decoded.
PHY→MAC	CRS	**Carrier Sense** Signal is asserted when PHY is: • Transmitting • Receiving • Otherwise considered "in-use" This signal is asynchronous to the RX_CLK.
PHY→MAC	COL	**Collision Detect** Signal is asserted when a collision is detected. This signal is asynchronous to the RX_CLK.

3.1.2 RMII SIGNAL DETAILS

RMII reduces the overall pin count of MII while maintaining the same capabilities. The changes include:

- TX_CLK and RX_CLK are combined into a single clock signal, REF_CLK. The clock source is flexible and may be sourced from MAC to PHY, PHY to MAC, or from an external source. This allows a single clock source to be supplied to multiple PHYs in multi-port systems.
- Clock frequency is doubled to 50 MHz in 100 Mbit/s mode.
- Data signals TXD and RXD are reduced from four to two.
- Receive Data Valid (RX_DV) and Carrier Sense (CRS) signals are combined into one signal, RX_DV.
- Collision detection (COL) signal is removed.

Note: Microchip does not offer any bridge controllers that support RMII. The RMII details are shown in this document for completeness.

RMII signals are described in Table 4.

TABLE 4: RMII SIGNALS

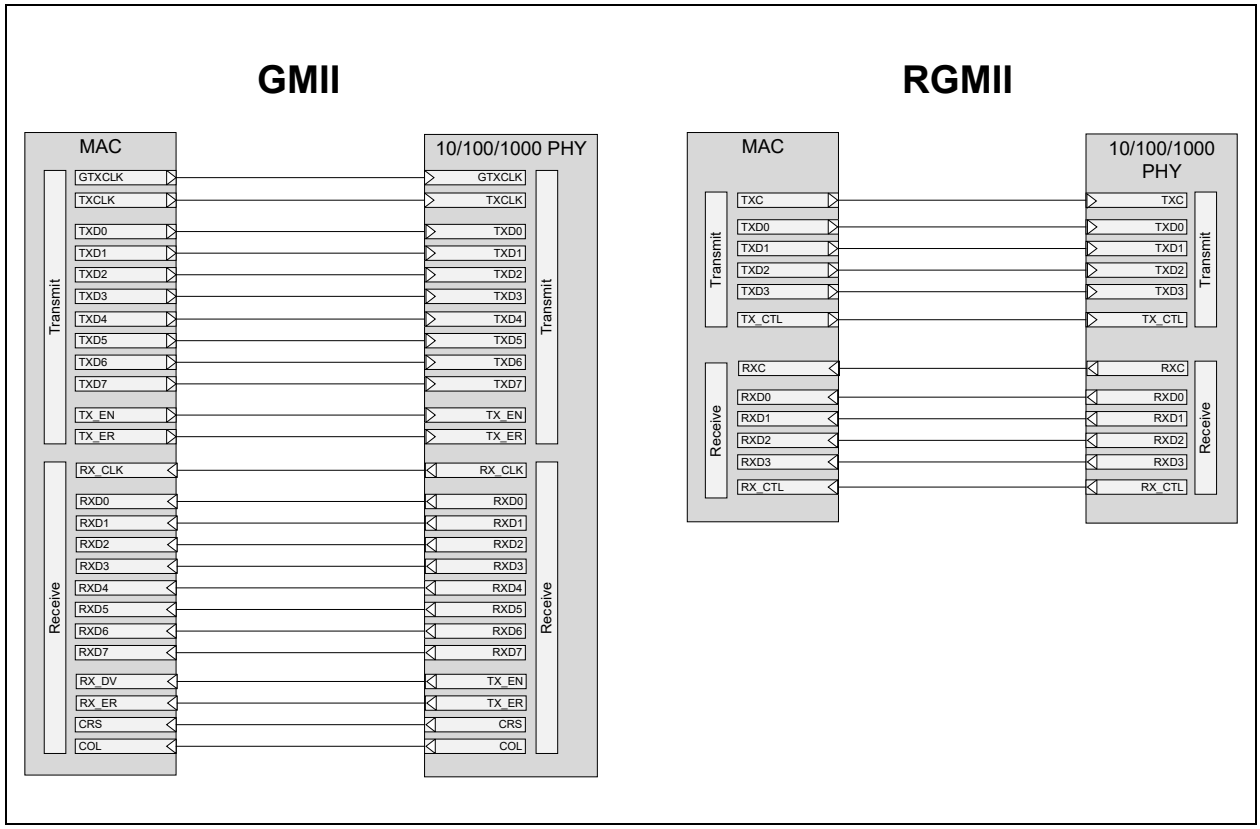
Direction	Signal Name	Description
MAC→PHY, PHY→MAC, or externally sourced	TX_CLK	**Transmit and Receive Clock** Free-running 5 MHz (in 10 Mbit/s mode) or 50 MHz clock (in 100 Mbit/s mode)
MAC→PHY	TXD[0:1]	**Transmit data bit signals** (two separate parallel signals)
MAC→PHY	TX_EN	**Transmit Enable** This signal is asserted during frame transmission.
MAC→PHY	TX_ER	**Transmit Error** This signal may be asserted during frame transmission to instruct the PHY to intentionally corrupt the frame. This is done so that the recipient of the frame will detect this packet as corrupted. This can be used as kind of ‘frame abort’ function in the case that a problem is detected in the midst of active frame transmission. This signal is optional per specification.
PHY→MAC	RXD[0:1]	**Receive data bit signals** (two separate parallel signals)
PHY→MAC	CRS_DV	**Carrier Sense and Receive Data Valid** 100 Mbit/s Mode: Carrier Sense (CRS) and RX_Data Valid (RX_DV) are multiplexed on alternate clock cycles. 10 Mbit/s mode: Carrier Sense (CRS) and RX_Data Valid (RX_DV) are multiplexed and alternate every 10 clock cycles. Carrier Sense Signal asserts when PHY is: • Transmitting • Receiving • Otherwise considered “in-use” Receive Data Valid Signal asserts when received data is valid. Some preamble bits may be missed due to slight delay in assertion of the signal, but must be asserted sufficiently fast to ensure that the start of frame delimiter byte is received by the MAC.
PHY→MAC	RX_ER	**Receive Error** Asserts to indicate that the received data was not properly decoded.

3.2 GMII/RGMII

The GMII was introduced to enable increased speeds necessary to support 1000 Mbit/s Ethernet. RGMII was introduced later to offer a lower pin count option while maintaining full functionality of the GMII interface.

Note: Microchip does not offer any bridge controllers which support GMII. The GMII details are shown in this document for completeness.

FIGURE 3: GMII AND RGMII INTERFACES



3.2.1 GMII SIGNAL DETAILS

GMII allows for up to 1000 Mbit/s Ethernet. The changes from MII/RMII include:

- Dedicated clock for Gigabit transmission is added, GTX_CLK.
- Clock frequency is 125 MHz in 1000 Mbit/s mode, 25 MHz in 100 Mbit/s mode, and 2.5 MHz in 10 Mbit/s mode.
- Both transmit and receive have eight signals for data (that is, 8-bits wide).

GMII signals are described in Table 5.

Note: Microchip does not offer any bridge controllers that support GMII. The GMII details are shown in this document for completeness.

TABLE 5: GMII SIGNALS

Direction	Signal Name	Description
MAC→PHY	GTX_CLK	**Clock signal used for 1000 Mbit/s connections** Always 125 MHz
MAC→PHY	TX_CLK	**Clock signal used for 10/100 Mbit/s connections**
MAC→PHY	TXD[7:0]	**Transmit data bit signals** (eight separate parallel signals)
MAC→PHY	TX_EN	**Transmit Enable** This signal is asserted during frame transmission.
MAC→PHY	TX_ER	**Transmit Error** This signal may be asserted during frame transmission to instruct the PHY to intentionally corrupt the frame. This is done so that the recipient of the frame will detect this packet as corrupted. This can be used as kind of 'frame abort' function in the case that a problem is detected in the midst of active frame transmission. This signal is optional per specification.
PHY→MAC	RX_CLK	**Received Signal Clock**
PHY→MAC	RXD[7:0]	Receive data bit signals (8 separate parallel signals).
PHY→MAC	RX_DV	**Receive Data Valid** Asserts when received data is valid. Some preamble bits may be missed due to slight delay in assertion of the signal, but must be asserted sufficiently fast to ensure that the start of frame delimiter byte is received by the MAC.
PHY→MAC	RX_ER	**Receive Error** Asserts to indicate that the received data was not properly decoded.
PHY→MAC	COL	(Half-Duplex Connections Only) **Collision Detect** Signal is asserted when a collision is detected.
PHY→MAC	CRS	(Half-Duplex Connections Only) **Carrier Sense** Signal is asserted when PHY is: • Transmitting • Receiving • Otherwise considered "in-use"

3.2.2 RGMII SIGNAL DETAILS

RGMII reduces the overall pin count of GMII while maintaining the same capabilities. The changes include:

- GTX_CLK is eliminated.
- Clock frequency remains the same as in GMII, but data is sampled relative to both the rising edge and falling edge of the clock.
- Data signals TXD and RXD are reduced from eight to four.
- Receive Data Valid (RX_DV) and Receive Error (RX_ER) signals are combined into one signal, RX_CTL.
- Collision detection signal (COL) and Carrier Sense (CRS) signals are removed.

RGMII signals are described in Table 6.

TABLE 6: RGMII SIGNALS

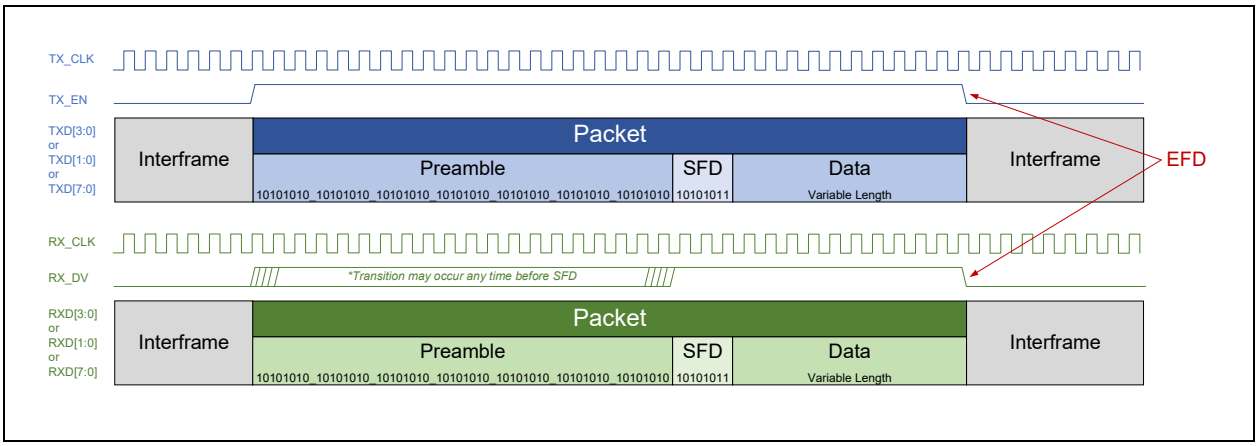
Direction	Signal Name	Description
MAC→PHY	TXC	**Transmit Signal Clock**
MAC→PHY	TXD[3:0]	**Transmit data bit signals** (four separate parallel signals)
MAC→PHY	TX_CTL	**Multiplexing Transmit Enable and Transmit Error** Transmit Enable This signal is asserted during frame transmission. Transmit Error This signal may be asserted during frame transmission to instruct the PHY to intentionally corrupt the frame. This is done so that the recipient of the frame will detect this packet as corrupted. This can be used as kind of 'frame abort' function in the case that a problem is detected in the midst of active frame transmission. This signal is optional per specification.
PHY→MAC	RXC	**Receive Signal Clock**
PHY→MAC	RXD[3:0]	**Receive data bit signals** (four separate parallel signals)
PHY→MAC	RX_CTL	**Multiplexing of Receive Data Valid and Receive Error** Receive Data Valid Asserts when received data is valid. Some preamble bits may be missed due to slight delay in assertion of the signal, but must be asserted sufficiently fast to ensure that the start of frame delimiter byte is received by the MAC. Receive Error Asserts to indicate that the received data was not properly decoded.

3.3 MII/RMII/GMII/RGMII Packet Format

MII/RMII/GMII/RGMII differ on transmission frequency and pin count, but all generally follow the same packet transmission structure. Figure 4 shows an example of the basic components of an MII packet in a simplified format.

Note: The clock waveform is not to scale and many more clock oscillations occur during a packet transmission than what is shown in the figure.

FIGURE 4: MII PACKET FORMAT (SIMPLIFIED)



3.3.1 PREAMBLE

Every frame begins with a preamble of seven octets of alternating 1’s and 0’s. The preamble contains no usable data.

3.3.2 START OF FRAME DELIMITER

The Start of Frame Delimiter (SFD) follows the preamble. It is a single octet in length, beginning with six alternating 1’s and 0’s followed with two final 1’s.

3.3.3 DATA

Data in a frame consists of N octets of data. The size of N depends on the underlying protocol being transmitted. Notice that MII does not explicitly contain any contextual or error checking components. That is handled by the controller/MAC

3.3.4 END OF FRAME DELIMITER

The End of Frame Delimiter is not a pattern of octets, but rather is signaled by deassertion of TX_EN (for transmit case) or RX_DV (for receive case).

3.3.5 INTERFRAME – TRANSMIT

During a normal interframe period, the TX_CLK continues to run, but TX_EN and TX_ER are both deasserted. The data signals become ‘don’t cares’ and can be all 0’s, all 1’s, or any other mix of 1 and 0.

3.3.6 INTERFRAME – RECEIVE

During a normal interframe period, the RX_CLK continues to run, but RX_DV and RX_ER are both deasserted. The data signals become ‘don’t cares’ and can be all 0’s, all 1’s, or any other mix of 1 and 0.

If RX_ER = 1 while RX_DV = 0, then either ‘Assert LPI’ or ‘False Carrier Indication’ can be encoded on the data lines.

4.0 MDIO

MDIO is a two-wire serial bus that is electrically very similar to I^2C/SMBus. MDIO is used to manage PHYs through a sideband channel that operates asynchronously and entirely separate from MII/RMII/GMII/RGMII. Management of PHYs is performed through reading or writing of a standard set of registers. MDIO is used as the sideband channel for MII, RMII, GMII, and RGMII.

4.1 Electrical Interface

The MDIO bus has two signals:

- Management Data Clock or MDC
- Management Data Input/Output or MDIO

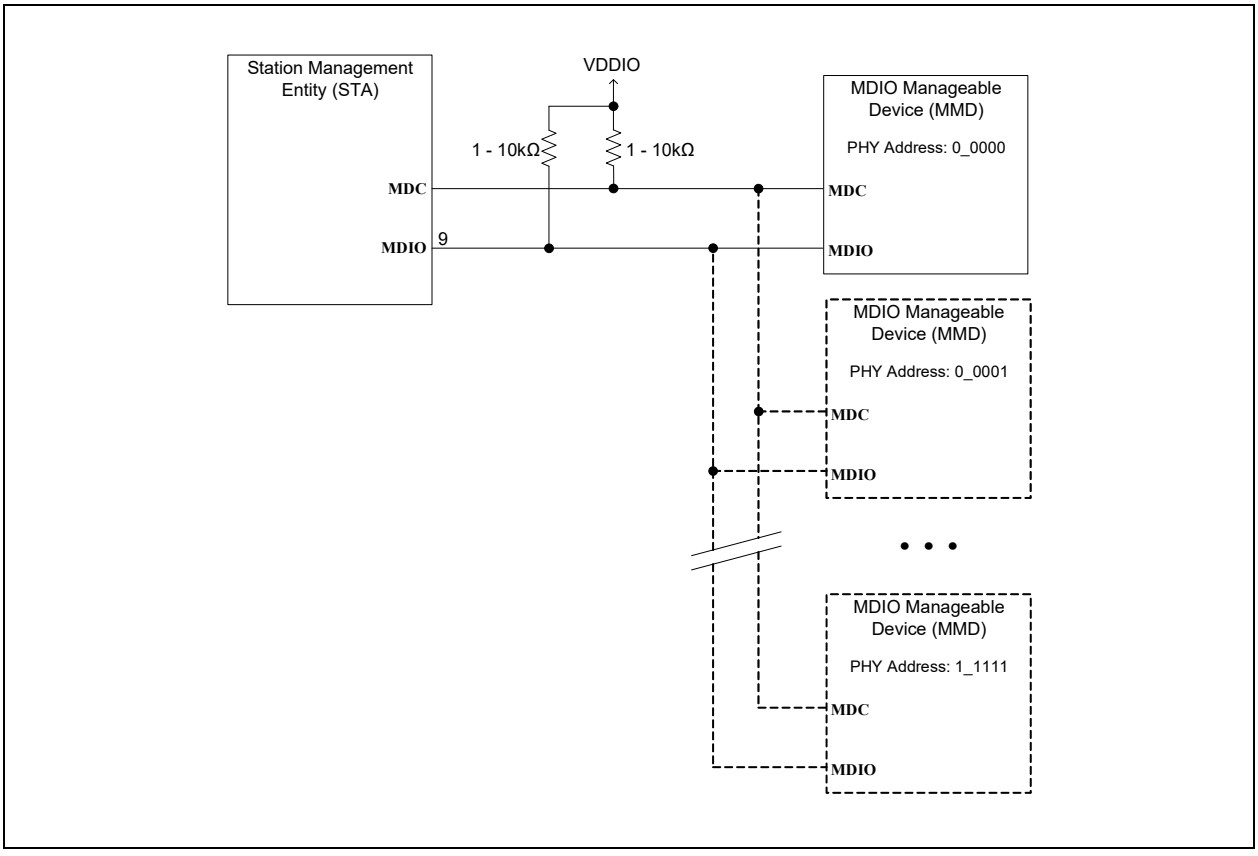
The controller of the MDIO bus is referred to as the Station Management Entity (STA). There can only be one STA on a bus. The STA initiates all communication and controls the clock (MDC signal).

The targets are referred to as MDIO Manageable Devices (MMD), of which there can be up to 32 devices on each bus. Each MMD must have its own unique 5-bit address.

MDIO is an open-drain electrical interface (similar to I^2C/SMBus), which requires external pull-up resistors to the supported I/O voltage. The value of the pull-up resistors must be selected to ensure signal timing while taking into account the total number of devices on the bus, their inherent pin leakage, and the PCB layout (trace length and impedance).

The MDC frequency can be up to 2.5 MHz (or a minimum period of 400 ns), although modern STAs and MMDs may have increased supported speeds.

FIGURE 5: MDIO ELECTRICAL/SCHEMATIC



4.2 Clause 22 Protocol

MDIO was first defined in Clause 22 of IEEE 802.3 Specification. The MDIO interface can access up to 32 PHY devices on a single bus. Each PHY device may have 32 registers for control and configuration, such as:

- Link Connection Status
- Supported Speeds (10/100/1000 and Full-Duplex/Half-Duplex)
- Selection of Speed
- Auto-negotiation Enable/Disable and Advertisement Configuration
- Low Power Support
- Full-/Half-Duplex Mode
- Fault Indication
- PHY Soft Reset
- Test Modes such as Loopback/Collision Test
- PHY Identification (Organizationally Unique Identifier (OUI), Model number, Revision Number)

Clause 22 protocol follows a rigid packet format that is always 64 bits long (32 bit preamble + 32 bits of packet content). Details on a Clause 22 packet are described in Table 7.

TABLE 7: CLAUSE 22 FRAME FORMAT

Symbol	Name	Width (bits)	Notes
PRE_32	Preamble	32	MDIO stays a ‘1b’ for entire duration. MDC oscillates continuously for entire duration.
ST	Start of Frame	2	Always ‘01b’ for Clause 22
OP	Opcode	2	‘01b’ Write ‘10b’ Read
PHYADR5	PHY Address	5	Target PHY Address value All possible values from 0_0000b to 1_1111b are supported.
REGADR5	SMI Register Address	5	See Section 4.5, "Standard SMI Registers"
TA	Turnaround	2	Turnaround time if bus ownership changes from STA to MMD during read
DATA	Data Payload	16	Write: • MDIO driven by STA • MDC driven by STA Read: • MDIO driven by MMD • MDC driven by STA

Signal levels may be 5V or 3.3V.

Setup Time/Hold time when MDIO driven by STA:

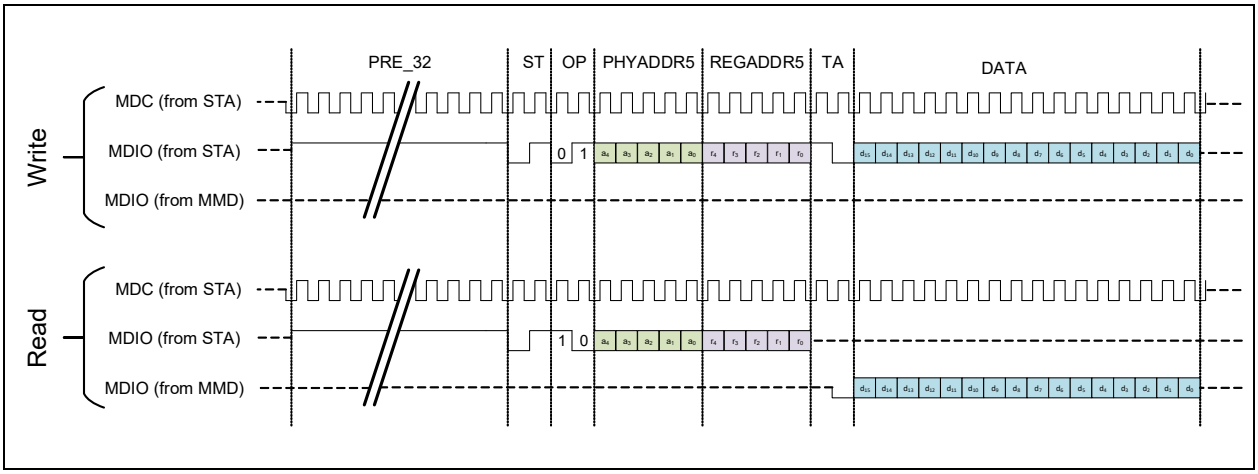
- Setup: 10 ns
- Hold: 10 ns

Setup Time/Hold time when MDIO driven by MMD:

- Setup: 0 ns
- Hold: 300 ns

The PHY Address, SMI Register Address, and Data Payload are always sent with the most-significant bits (msb) first.

FIGURE 6: MDIO CLAUSE 22 PACKET (WRITE AND READ)



4.3 Clause 45 Protocol

The IEEE 802.3ae specification introduced Clause 45 register access to allow for significant register expansion being demanded by 10 Gigabit PHYs and beyond. The main Clause 45 features include:

- Up to 32 devices (same as Clause 22)
- Up to 32 different device IDs (allows MDIO to access other devices beyond PHYs)
- Up to 65,536 registers on each PHY/device (32-bit register addresses)
- Support for 1.2V I/O on MDIO
- Fault Signaling
- Additional Loopback Functionality

Clause 45 adds two new opcodes and changes the method by which registers are addressed. Register Read/Write access is now minimally a 2-step process. This allows Clause 45 to also remain backward compatible with Clause 22.

The new ‘Address’ opcode sets the 32-bit address pointer, and a subsequent Read or Write command is required that is targeted to the address pointer that was set.

The new ‘Read-Increment-Address” opcode automatically increments the address pointer by one, so that a subsequent Read command can retrieve the data from the next address.

The Clause 22 Address field is replaced with a Device Type field, which allows the MDIO to access and control multiple kinds of devices beyond Ethernet PHYs.

Clause 45 protocol follows the same fixed length frame format as Clause 22, which is always 64 bits long (32-bit preamble plus 32 bits of packet content). Details on a Clause 45 packet are described in Table 8.

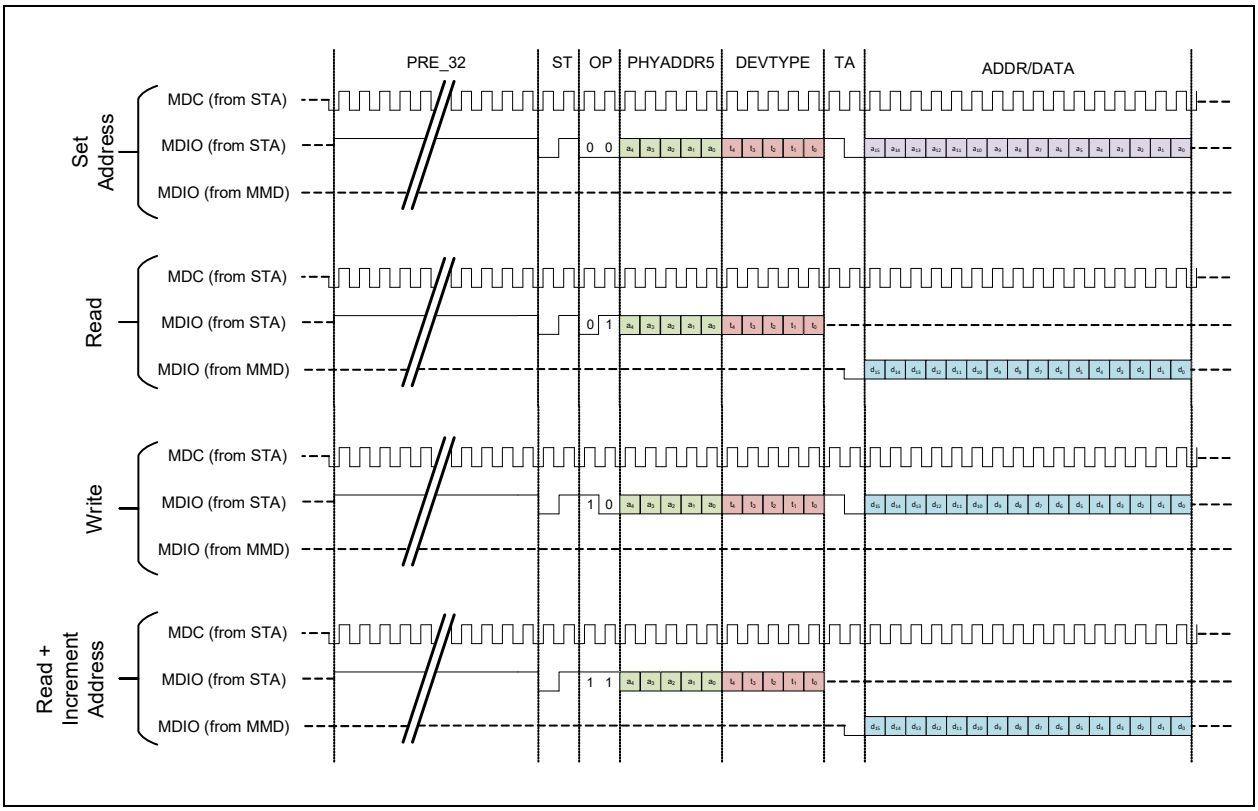
TABLE 8: CLAUSE 45 FRAME FORMAT

Symbol	Name	Width (bits)	Notes
PRE_32	Preamble	32	MDIO stays a ‘1b’ for entire duration. MDC oscillates continuously for entire duration.
ST	Start of Frame	2	Always ‘01b’ for Clause 22
OP	Opcode	2	‘00b’ Address ‘01b’ Write ‘10b’ Read ‘11b’ Read-Increment-Address
PHYADR5	PHY Address	5	Target PHY Address value. All possible values from 0_0000b to 1_1111b are supported.

TABLE 8: CLAUSE 45 FRAME FORMAT (CONTINUED)

Symbol	Name	Width (bits)	Notes
DEVTYPE	Device Type	5	Device Type/Device Address Allows other devices other than PHYs to be accessed on the MDIO bus. Up to 32 different device addresses can be supported.
TA	Turnaround	2	Turnaround time if bus ownership changes from STA to MMD during read
DATA	Data Payload	16	See Section 4.5, "Standard SMI Registers" For Opcode = ‘00b’, this field contains the target Register Address. For Opcodes =’10b’ - ‘11b’, the field contains a data payload. Address: • MDIO driven by STA • MDC driven by STA Write: • MDIO driven by STA • MDC driven by STA Read: • MDIO driven by MMD • MDC driven by STA Read-Increment-Address: • MDIO driven by MMD • MDC driven by STA

FIGURE 7: MDIO CLAUSE 45 PACKET (WRITE AND READ)



4.4 Clause 22 Access to Clause 45 Registers

Standard Clause 22 SMI registers 13 and 14 allow for access into the extended Clause 45 register space if the MAC does not directly support Clause 45, but the PHY does support Clause 45 registers. These registers are:

- MMD Access Control
- MMD Access Address Data

4.4.1 CLAUSE 22 WRITE TO CLAUSE 45 REGISTER

The following steps allow Clause 22 write access to Clause 45 registers:

1. Register 13: Set ‘Function’ to 00b (address) and ‘DEVAD’ field to the selected device address.
2. Register 14: Set the ‘Address Data’ to the target Clause 45 register address.
3. Register 13: Set ‘Function’ to 01b (data, no post increment) and ‘DEVAD’ field to the selected device address (as in step 1.)
4. Register 14: Set the ‘Address Data’ to the desired write value for the target Clause 45 register

4.4.2 CLAUSE 22 READ FROM CLAUSE 45 REGISTER

The following steps allow Clause 22 read access from Clause 45 registers:

1. Register 13: Set ‘Function’ to 00b (address) and ‘DEVAD’ field to the device address value for the desired Clause 45 register address.
2. Register 14: Set the ‘Address Data’ to the target Clause 45 register address.
3. Register 13: Set ‘Function’ to 01b (data, no post increment) and ‘DEVAD’ field to the selected device address (as in step 1.)
4. Register 14: Read the content of the MMD’s selected Clause 45 register.

4.5 Standard SMI Registers

Note: Only a few of the most basic or commonly used SMI registers are shown in this section to help explain the mechanisms behind the MDIO protocol trace example in MDIO Configuration Example – LAN7801 and KSZ9131. Refer to the IEEE 802.3 specifications for full register details as well as PHY-specific data sheets for vendor-defined register use.

MDIO communication is typically limited to access of just a few crucial registers. There are many other extended registers and vendor-defined registers that may be used for development, test, and debug purposes. The most basic registers are displayed here in this document to provide some context for their use. Refer to the relevant specifications and vendor-supplied data sheets for full definitions.

- *Basic*: Required for all MII/RMII/GMII/RGMII PHYs
- *Extended*: Required for all GMII/RGMII PHYs
- *Vendor-Specific*: Allows special vendor-defined features/capabilities/test modes

TABLE 9: MICROCHIP ETHERNET BRIDGE CONTROLLERS WITH EXTERNAL PHY SUPPORT

Index	Register Name	Type	Link
00h	Basic Mode Control	Basic	Basic Control Register
01h	Basic Mode Status	Basic	Basic Status Register
02h	PHY Identifier 1	Extended	PHY Identifier 1
03h	PHY Identifier 2	Extended	PHY Identifier 2
04h	Auto-Negotiation Advertisement	Extended	Auto-Negotiation Advertisement
05h	Auto-Negotiation Link Partner Base Page Ability	Extended	Auto-Negotiation Link Partner Ability
06h	Auto-Negotiation Expansion	Extended	See the IEEE 802.3 and/or product-specific PHY data sheet
07h	Auto-Negotiation Next Page TX	Extended	See the IEEE 802.3 and/or product-specific PHY data sheet
08h	Auto-Negotiation Link Partner Received Next Page	Extended	See the IEEE 802.3 and/or product-specific PHY data sheet
09h	Controller-Target Control	Extended	See the IEEE 802.3 and/or product-specific PHY data sheet
0Ah	Controller-Target Status	Extended	See the IEEE 802.3 and/or product-specific PHY data sheet
0Bh	PSE Control	Extended	See the IEEE 802.3 and/or product-specific PHY data sheet
0Ch	PSE Status	Extended	See the IEEE 802.3 and/or product-specific PHY data sheet
0Dh	MMD Access Control	Extended	MMD Access Control
0Eh	MMD Address Data	Extended	MMD Access Address Data
0Fh	Extended Status	Extended	Unused/Reserved for MII/RMII PHYs Extended Status
10h-1Fh	Vendor Specific	Extended	See the product-specific PHY data sheet
001Fh-FFFFh	Clause 45 MMD Register Space	Clause 45	See the IEEE 802.3 and/or product-specific PHY data sheet

TABLE 10: BASIC CONTROL REGISTER

SMI Basic Mode Control Register Address: 00h		Description
Bit	**Name**	
15	PHY Soft Reset	When set, resets PHY and all registers to default state (self clearing).
14	Loopback	0b = Loopback Mode Disabled 1b = Loopback Mode Enabled
13	Speed Select[0]	Together with Speed Select[1], Selects Speed. Ignored if auto-negotiation is enabled. 00b = 10 Mbps 01b = 100 Mbps 10b = 1000 Mbps 11b = Reserved
12	Auto-Negotiation Enable	0b = Auto-negotiation Disabled 1b = Auto-negotiation Enabled
11	Power Down	0b = Normal Operation 1b = General Power Down Mode
10	Isolate	0b = Normal Operation 1b = PHY Isolated from MII interface
9	Restart Auto Negotiation	When set, restarts Auto-negotiation (self clearing).
8	Duplex Mode	0b = Half duplex 1b = Full duplex
7	Collision Test Mode	0b = Collision Test mode disabled 1b = Collision Test mode enabled
6	Speed Select[1]	Together with Speed Select[0], Selects Speed. Ignored if auto-negotiation is enabled.
5:0	Reserved	Reserved

TABLE 11: BASIC STATUS REGISTER

SMI Basic Mode Status Register Address: 01h		Description
Bit	**Name**	
15	100BASE-T4	0b = PHY is not capable of 100BASE-T4 1b = PHY is capable of 100BASE-T4
14	100BASE-X Full Duplex	0b = PHY is not capable of 100BASE-X Full Duplex 1b = PHY is capable of 100BASE-X Full Duplex
13	100BASE-X Half Duplex	0b = PHY is not capable of 100BASE-X Half Duplex 1b = PHY is capable of 100BASE-X Half Duplex
12	10BASE-T Full Duplex	0b = PHY is not capable of 10BASE-T Full Duplex 1b = PHY is capable of 10BASE-T Full Duplex
11	10BASE-T Half Duplex	0b = PHY is not capable of 10BASE-T Half Duplex 1b = PHY is capable of 10BASE-T Half Duplex
10	100BASE-T2 Full Duplex	0b = PHY is not capable of 100BASE-T2 Full Duplex 1b = PHY is capable of 100BASE-T2 Full Duplex
9	100BASE-T2 Half Duplex	0b = PHY is not capable of 100BASE-T2 Half Duplex 1b = PHY is capable of 100BASE-T2 Half Duplex
8	Extended Status	0b = No extended status info 1b = Extended status info available in Register 15

TABLE 11: BASIC STATUS REGISTER (CONTINUED)

SMI Basic Mode Status Register Address: 01h		Description
Bit	**Name**	
7	Unidirectional Ability	0b = Transmit only when valid link is up 1b = Can transmit even without valid link
6	MF Preamble Suppression	0b = Preamble suppressed frames not accepted 1b = Preamble suppressed frames accepted
5	Auto-Negotiation Complete	0b = Auto-negotiation not complete 1b = Auto-negotiation complete
4	Remote Fault	0b = No remote fault detected 1b = Remote fault detected
3	Auto-Negotiation Ability	0b = PHY not capable of auto-negotiation 1b = PHY capable of auto-negotiation
2	Link Status	0b = Link down 1b = Link up
1	Jabber Detect	0b = No jabber detected 1b = Jabber detected
0	Extended Capability	0b = Basic register capability only (reg 00h and 01h) 1b = Extended register set capability

TABLE 12: PHY IDENTIFIER 1

SMI PHY Identifier Register #1 Address: 02h		Description
Bit	**Name**	
15:0	PHY ID Number [3:18]	Bits 3-18 of the Organizationally Unique Identifier (OUI)

TABLE 13: PHY IDENTIFIER 2

SMI PHY Identifier Register #2 Address: 03h		Description
Bit	**Name**	
15:10	PHY ID Number [19:24]	Bits 19-24 of the Organizationally Unique Identifier (OUI)
9:4	Model Number	Model number assigned by PHY manufacturer
3:0	Revision Number	Revision number assigned by PHY manufacturer

TABLE 14: AUTO-NEGOTIATION ADVERTISEMENT

SMI Auto-Negotiation Advertisement Register Address: 04h		Description
Bit	**Name**	
15	Next Page	0 = No next page ability 1 = Next page capable
14	Reserved	Reserved
13	Remote Fault	0 = Remote fault indication not advertised 1 = Remote fault indication advertised
12	Extended Next Page	0 = No extended next page ability 1 = Extended next page capable

TABLE 14: AUTO-NEGOTIATION ADVERTISEMENT (CONTINUED)

SMI Auto-Negotiation Advertisement Register Address: 04h		Description
Bit	**Name**	
11	Asymmetric Pause	0 = No Asymmetric Pause toward link partner advertised 1 = Asymmetric Pause toward link partner advertised
10	Symmetric Pause	0 = No Symmetric Pause toward link partner advertised 1 = Symmetric Pause toward link partner advertised
9	100BASE-T4	0 = Not Supported/Advertised 1 = Supported/Advertised
8	100BASE-X Full Duplex	0 = Not Supported/Advertised 1 = Supported/Advertised
7	100BASE-X Half Duplex	0 = Not Supported/Advertised 1 = Supported/Advertised
6	10BASE-T Full Duplex	0 = Not Supported/Advertised 1 = Supported/Advertised
5	10BASE-T Half Duplex	0 = Not Supported/Advertised 1 = Supported/Advertised
4:0	Selector Field	Identifies the type of message being sent 00001b = IEEE 802.3

TABLE 15: AUTO-NEGOTIATION LINK PARTNER ABILITY

SMI Auto-Negotiation Link Partner Ability Register Address: 05h		Description
Bit	**Name**	
15	Next Page	0 = Link partner does not advertise next page ability 1 = Link partner is next page capable
14	Reserved	Reserved
13	Remote Fault	0 = Link partner does not advertise remote fault indication capability 1 = Link partner is capable of remote fault indication
12	Extended Next Page	0 = Link partner does not advertise extended next page capability 1 = Link partner is extended next page capable
11	Asymmetric Pause	0 = Link partner does not advertise Asymmetric Pause capability 1 = Link partner is Asymmetric Pause capable
10	Symmetric Pause	0 = Link partner does not advertise Symmetric Pause capability 1 = Link partner is Symmetric Pause capable
9	100BASE-T4	0 = Link partner does not advertise this capability 1 = Link partner supports this capability
8	100BASE-X Full Duplex	0 = Link partner does not advertise this capability 1 = Link partner supports this capability
7	100BASE-X Half Duplex	0 = Link partner does not advertise this capability 1 = Link partner supports this capability
6	10BASE-T Full Duplex	0 = Link partner does not advertise this capability 1 = Link partner supports this capability
5	10BASE-T Half Duplex	0 = Link partner does not advertise this capability 1 = Link partner supports this capability
4:0	Selector Field	Identifies the type of message being sent 00001b = IEEE 802.3

TABLE 16: MMD ACCESS CONTROL

SMI MMD Access Address Data Register Address: 0Dh		Description
Bit	**Name**	
15:14	Function	00b = Address 01b = Data, no post increment 10b = Data, post increment on reads and writes 11b = Data, post increment on writes only
13:5	Reserved	Always 0
4:0	DEVAD	Device Address

TABLE 17: MMD ACCESS ADDRESS DATA

SMI MMD Access Address Data Register Address: 0Eh		Description
Bit	**Name**	
15:0	Address Data	Contains either a register address value or data value, depending on the Function value in the SMI MMD Access Address Data Control Register.

TABLE 18: EXTENDED STATUS

SMI Extended Status Register Address: 0Fh		Description
Bit	**Name**	
15	1000BASE-X Full Duplex	0b = PHY is not capable of 1000BASE-X Full Duplex 1b = PHY is capable of 1000BASE-X Full Duplex
14	100BASE-X Half Duplex	0b = PHY is not capable of 1000BASE-X Half Duplex 1b = PHY is capable of 1000BASE-X Half Duplex
13	1000BASE-T Full Duplex	0b = PHY is not capable of 1000BASE-T Full Duplex 1b = PHY is capable of 1000BASE-T Full Duplex
12	1000BASE-T Half Duplex	0b = PHY is not capable of 1000BASE-T Half Duplex 1b = PHY is capable of 1000BASE-T Half Duplex
11:0	Reserved	Reserved

5.0 PHY DRIVERS

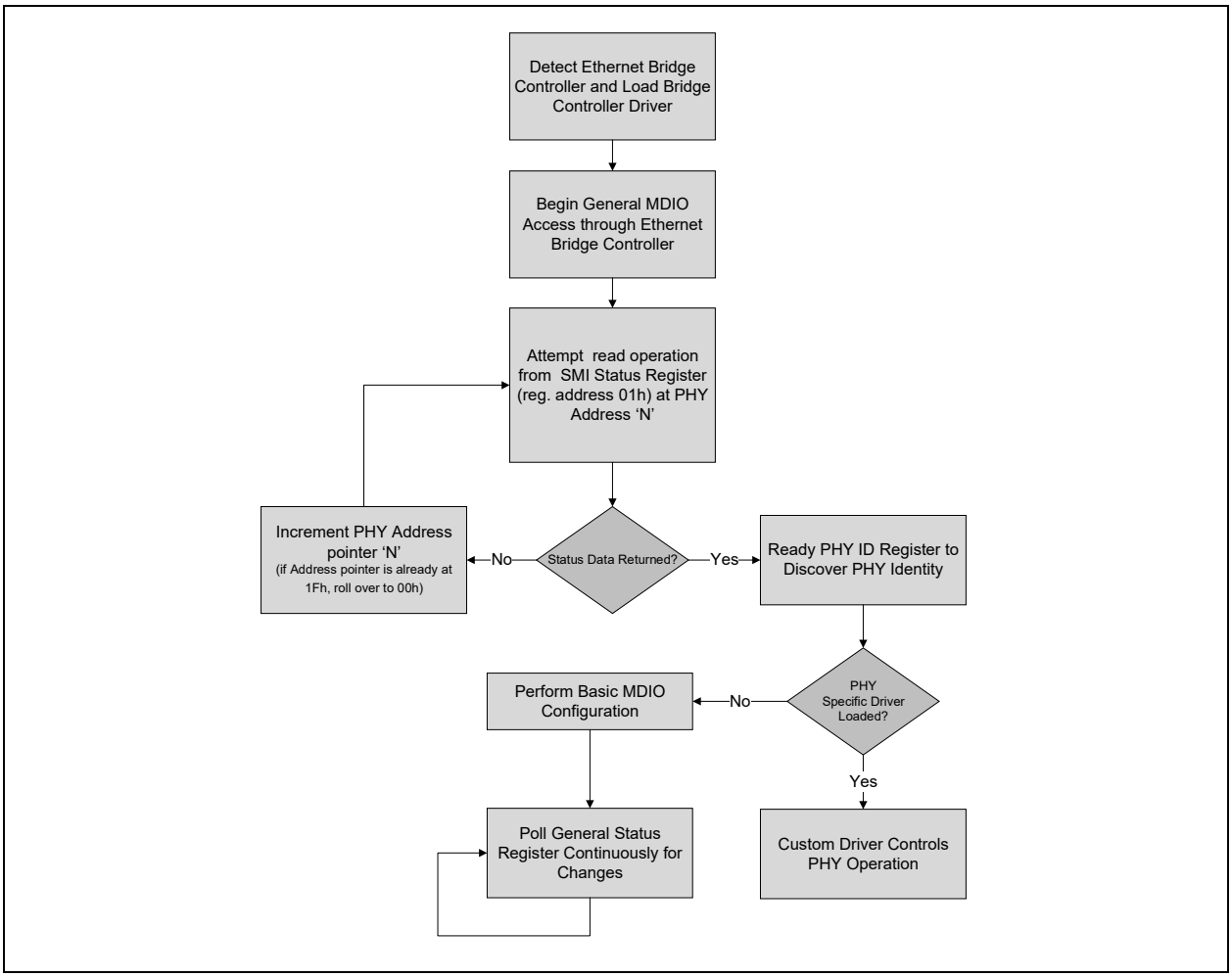
Operating systems include generic PHY drivers that access general MDIO registers for configuration. The generic PHY drivers generally perform the following tasks:

1. Obtain the PHY driver ID.

   Note: If the ID matches an installed PHY-specific/custom driver, then that driver may be loaded and used to control the PHY. Special features, such as 1588 and MACsec, may not be usable if using generic PHY drivers.

2. Check for basic capabilities of the PHY (speed support, full-duplex/half-duplex support, auto-negotiation advertisement, and so on).
3. Configure auto-negotiation advertisement based on PHY capabilities.
4. Enable and restart auto-negotiation.
5. Poll link status periodically to monitor for Link UP/Link Down status, auto-negotiation result.

FIGURE 8: MDIO PHY DETECTION AND CONFIGURATION GENERALIZED FLOW



5.1 MDIO Configuration Example – LAN7801 and KSZ9131

The following is a real-world example of a PC interrogating and configuring an Ethernet PHY through MDIO.

- Operating System: Windows
- PHY Driver: Generic Windows PHY Driver
- Ethernet bridge controller: LAN7801
- Ethernet PHY: KSZ913
- Ethernet PHY Address: 03h

TABLE 19: CLAUSE 22

N	Op	PHY Addr	Reg Addr	Data	Description
1	R	1Fh	01h	FFFFh	No Response, No PHY At Address 1Fh
2	R	1Fh	01h	FFFFh	Second Attempt at PHY Address 1Fh
3	R	1Eh	01h	FFFFh	No Response, No PHY At Address 1Eh
4	R	1Eh	01h	FFFFh	Second Attempt at PHY Address 1Eh
...					
53	R	05h	01h	FFFFh	No Response, No PHY At Address 05h
54	R	05h	01h	FFFFh	Second Attempt at PHY Address 05h
55	R	04h	01h	FFFFh	No Response, No PHY At Address 04h
56	R	04h	01h	FFFFh	Second Attempt at PHY Address 04h
57	R	03h	01h	7949h	Read: Basic Status Register *Raw Binary: 0111_1001_0100_1001b* This response indicates the follow STATUS: • Link Status is DOWN • Auto-Negotiation is NOT COMPLETE • No Fault or Jabber Detected This response also indicates the PHY's basic capabilities are: • 100BASE-X Full Duplex and Half Duplex • 10BASE-X Full Duplex and Half Duplex • Extended Status Registers in Reg 15 • PHY accepts management frames with the preamble suppressed • PHY supports auto-negotiation • Extended Register Set
58	R	03h	01h	7949h	Read: Basic Status Register (Second Time) No change to this register since first read-back.
59	R	03h	02h	0022h	Read: Auto-Negotiation Advertisement *Raw Binary: 0001h_0110h_0100_0010b* Organizationally Unique Identifier (bits 3-18): 0000_0000_0010_0010b
60	R	03h	03h	1642h	Read: PHY Identifier 1 *Raw Binary: 0001h_0110h_0100_0010b* Organizationally Unique Identifier (bits 19-24): 000101b Model Number: 100100b Revision Number: 0010b
61	R	03h	04h	05E1h	Read: Auto-Negotiation Advertisement *Raw Binary: 0000_0101_1110_0001b* This response indicates that the following capabilities are being advertised during auto-negotiation: • 100BASE-X Full Duplex and Half Duplex • 10BASE-X Full Duplex and Half Duplex • Symmetric PAUSE • Auto-Negotiation Type: IEEE 802.3
62	W	03h	04h	05E1h	Write: Auto-Negotiation Advertisement This command is writing the same value that was read back to the PHY. It can be considered unnecessary.

TABLE 19: CLAUSE 22 (CONTINUED)

N	Op	PHY Addr	Reg Addr	Data	Description
63	R	03h	09h	0200h	Read: Controller-Target Control Register *Raw Binary: 0000_0010_0000_0000b* This response also indicates that the PHY is capable of 1000BASE-T Full Duplex operation, and 1000BASE-T Half Duplex is unsupported. **Note:** This register can also be used to enable transmitter test modes.
64	W	03h	09h	0200h	Write: Controller-Target Control Register This command is writing the same value that was read back to the PHY. It can be considered unnecessary.
65	W	03h	0Dh	0007h	Write: MMD Access Control *Raw Binary: 0000_0000_0000_0111b* **Note:** This command is utilizing special Clause 22 registers to access Clause 45 register space. See Section 4.4, "Clause 22 Access to Clause 45 Registers" for more info. This command is selecting: • MMD Function - Register Address • MMD Device Address (DEVAD) - 7h
66	W	03h	0Eh	003Ch	Write: MMD Access Address Data *Raw Binary: 0000_0000_0011_1100b* **Note:** This command is utilizing special Clause 22 registers to access Clause 45 register space. See Section 4.4, "Clause 22 Access to Clause 45 Registers" for more info. This command is selecting: • MMD Register Data - 003C Since the previous MMD Function Command was 'Register Address', this is indicating the register address that the following command will read or write to in DEVAD 07h.
67	W	03h	0Dh	4007h	Write: MMD Access Control *Raw Binary: 0100_0000_0000_0111b* **Note:** This command is utilizing special Clause 22 registers to access Clause 45 register space. See Section 4.4, "Clause 22 Access to Clause 45 Registers" for more info. This command is selecting: • MMD Function - Data, No Post Increment • MMD Device Address (DEVAD) - 7h
68	W	03h	0Eh	0006h	Write: MMD Access Address Data *Raw Binary: 0000_0000_0000_0110b* **Note:** This command is utilizing special Clause 22 registers to access Clause 45 register space. See Section 4.4, "Clause 22 Access to Clause 45 Registers" for more info. This command is selecting: • MMD Register Data - 0006h Since the previous MMD Function Command was 'Data, No Post Increment', this command is writing 0006h to Register 003Ch of DEVAD 07h. This particular register is an Energy Efficient Ethernet register. The register write is enabling 100BASE-TX EEE and 1000BASE-TX EEE Advertisement.

TABLE 19: CLAUSE 22 (CONTINUED)

N	Op	PHY Addr	Reg Addr	Data	Description
69	W	03h	00h	1200h	Write: Basic Control Register *Raw Binary: 0001_0010_0000_0000b* Enable Auto-Negotiation (set bit 12) Restart Auto-Negotiation (set bit 9)
70	R	03h	01h	7949h	Read: PHY Status Register This response indicates that no change to the PHY status has occurred.
71	R	03h	01h	7949h	Read: PHY Status Register This response indicates that no change to the PHY status has occurred.
72	R	03h	01h	7949h	Read: PHY Status Register This response indicates that no change to the PHY status has occurred.
...					
90	R	03h	01h	7969h	Read: PHY Status Register *Raw Binary: 0111_1001_0110_1001b* Bit 5 has changed 0b→1b This means that auto-negotiation has completed
91	R	03h	01h	796Dh	Read: PHY Status Register *Raw Binary: 0111_1001_0110_1101b* Bit 2 has changed 0b→1b This means that the link is now up.

6.0 HARDWARE CONSIDERATIONS

It is important to ensure that general design rules are followed for MDIO and MII/RGMII interconnections between Microchip bridge controllers and external PHYs.

Note: GMII and RMII information are not included in this section as Microchip bridge controllers do not support those variations of interconnect.

6.1 MII/RGMII Trace Properties

TABLE 20: MICROCHIP ETHERNET BRIDGE CONTROLLERS WITH EXTERNAL PHY SUPPORT

Parameter	Design Recommendation
Trace Impedance	50Ω to 68Ω
Trace Spacing	Route Transmit Signals (TX0:3) Together and Receive Signals Together Isolate RX CLK and TX CLK from other RGMII signals
Trace Length Matching	±10 mm (±400 mils)
Total Trace Length	For FR4 equivalent material and no layer transitions or connectors, 150 mm (6 inches) is the recommended maximum. If the design can stay within these guidelines, there is usually no need to simulate or verify signal quality in the lab. It is still very much possible to implement a system with longer than 150 mm in trace length, but careful PCB design becomes paramount. It is strongly recommended to take rise/fall measurements to ensure RGMII signal compliance is being met. PCB simulation may also help to ensure the design can meet signal requirements before manufacturing (though measurement in the lab is still required). Keep in mind the following factors: • PCB material: High-speed PCB materials can extend maximum possible signal length. • Layer transitions through vias: Each board layer transition will degrade signal integrity and decrease the maximum signal length. • Board-to-board connectors: Board-to-board connectors should be designed for high-speed signals. Each board-to-board connector will degrade signal quality and decrease the maximum possible signal length.
Clock Delay	See Section 6.1.1, "RGMII TXC and RXC Delay"
Other	The use of vias should be kept to a minimum on the RGMII interface, and switching layers on the PCB is not recommended. RGMII signals considered critical should be routed on the top layer next to a contiguous, digital ground plane. Slower RGMII signals can be routed on the bottom layer of the PCB.

6.1.1 RGMII TXC AND RXC DELAY

Due to the high speeds associated with the RGMII interface, it is recommended to introduce clock delay to the TXC and RXC signals. This ensures that the edges of the clocks are intentionally skewed so that sampling on the data lines is always accurate. There are generally three options for managing this delay:

- *Option A*: A delay of 1.5 ns to 2 ns can be added to the TX and RX CLK signals by routing them through a long PCB “serpentine” trace delay.
- *Option B*: A delay can be enabled on the TX and RX CLK transmitter side in the MAC settings of the Microchip Ethernet bridge controller. This may be referred to as RGMII-ID (ID = Internal Delay) in some products.
- *Option C*: A delay can be enabled on the TX and RX CLK receiver side in the PHY settings of the PHY. Verify that the option exists through the PHY documentation for the selected PHY. This delay would not be observable while probing the system using an oscilloscope. This may be referred to as RGMII-ID (ID = Internal Delay) in some products.

Note: It is also possible to combine the various clock delay methodologies if desired (that is, enable only the internal TXC delay of the MAC and only the internal RXC delay of the PHY, or vice versa).

FIGURE 9: RGMII CLOCK DELAY OPTION A: PCB TRACE DELAY

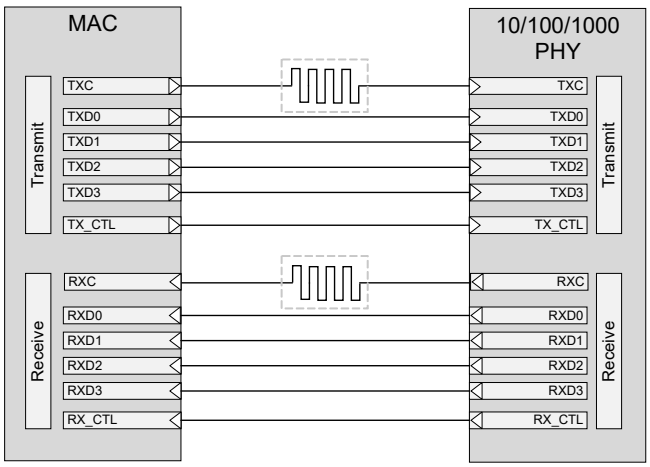


FIGURE 10: RGMII CLOCK DELAY OPTION B: MAC-SIDE DELAY SETTINGS

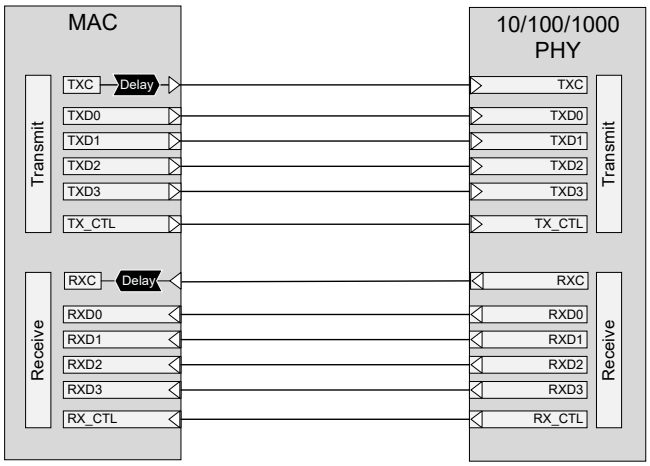
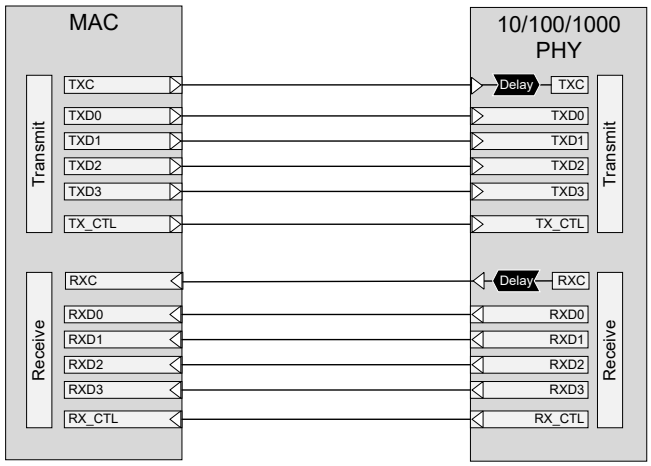


FIGURE 11: RGMII CLOCK DELAY OPTION C: PHY-SIDE DELAY SETTINGS



6.2 Additional Product-Specific Resources

For guidance on general hardware design with Microchip Ethernet bridge controllers, please refer to the following links:

TABLE 21: MICROCHIP ETHERNET BRIDGE CONTROLLERS WITH EXTERNAL PHY SUPPORT

Product	Resource	Link
LAN9500A	*AN18.0 - LAN9500/LAN9500i/LAN9500A/ LAN9500Ai Layout Guidelines*	https://www.microchip.com/en-us/product/LAN9500A
	LAN9500AI QFN Rev B Schematic Checklist	
	LAN9500A 56-pin QFN Package Routing Checklist	
LAN89530	*LAN89530 56-pin QFN Package Routing Checklist*	https://www.microchip.com/en-us/product/LAN89530
	LAN89530 QFN Rev B Schematic Checklist	
	LAN89530 56-pin QFN Package Component Placement Checklist	
LAN9730	*LAN9730 56-pin QFN Package Component Placement Checklist*	https://www.microchip.com/en-us/product/LAN9730
	LAN9730 56-pin QFN Package Routing Checklist	
	LAN9730 QFN Rev B Schematic Checklist	
LAN89730	*LAN89730 56-pin QFN Package Component Placement Checklist*	https://www.microchip.com/en-us/product/LAN89730
	LAN89730 56-pin QFN Package Routing Checklist	
	LAN89730 QFN Rev A Schematic Checklist	
LAN7801	*LAN7801 Placement Checklist*	https://www.microchip.com/en-us/product/LAN7801
	LAN7801 Routing Checklist	
	LAN7801 Schematic Checklist	
LAN7431	*LAN7431 Hardware Design Checklist*	https://www.microchip.com/en-us/product/LAN7431

7.0 DEBUGGING AND DEVELOPMENT TOOLS

7.1 Microchip Configuration and Programming Tools

TABLE 22: MICROCHIP ETHERNET BRIDGE CONTROLLERS WITH EXTERNAL PHY SUPPORT

Product	Operation System	Type	Tool	Notes
LAN9500A, LAN89530, LAN9730, LAN89730 (Automotive)	DOS	Programming and Test	LAN95XXDosUtility	The LAN95XX DOS Utility Suite provides support for programming the EEPROM and testing basic LAN9500/LAN9500A/ LAN9512/LAN9513/LAN9514 functionality in a production environment.
	Windows	Programming and Test	LAN95xxUtility GUI	The LAN95xx Utility application provides a graphical user interface to program the EEPROM of LAN95xx USB to Ethernet and USB Hub with Integrated Ethernet devices as well as perform tests on the device.
		Programming	9500eepApp	The LAN9500 Command Line Utility runs in a Windows Command prompt providing support for programming the EEPROM and testing basic LAN95xx functionality.
	Linux	Programming	ethtool	Included in most Linux distributions
LAN7801 and LAN7431	Windows	Configuration	MPLAB® Connect GUI	Simplified menu-based tool for selecting configuration options
		Programming	MPLAB Connect GUI	Programming Tab allows for easy programming during prototyping and development
		Programming	MPLAB Connect CLI	Command Line Interface with mass-production programming option
	Linux	Programming	ethtool	Included in most Linux distributions

7.2 MDIO Exercisers/Analyzers

MDIO analyzers are available in a few different form factors:

- *Dedicated Hardware*: Requires specialized equipment, but usually is capable of storing across long time scales, have good triggering capabilities, and supported software that fully decodes traffic and can even detect protocol errors.
- *Logic Analyzer Plug-ins*: Logic Analyzer plug-ins are a good option that allow general logic analyzer hardware to decode MDIO traffic.
- *Oscilloscope Plug-ins*: Allow you to do basic analysis using an oscilloscope. Oscilloscopes may sometimes be necessary when examining MDIO timing and waveforms for abnormalities that dedicated hardware tools and logic analyzers cannot detect. However, oscilloscopes are memory intensive and can usually only store a very short window of time.

TABLE 23: MDIO EXERCISER/ANALYZERS

Type	Product	Notes
Dedicated Analyzer Hardware	Total Phase Beagle Analyzer	Good low-cost option with quality software support. The tool also supports I^2C and SPI analysis. https://www.totalphase.com/products/beagle-i2cspi/
	Prodigy Technovations PGY-MDIO-EX-PD	High-end option with MDIO traffic generation capability and other advanced capabilities. https://prodigytechno.com/device/mdio-protocol-exerciser-and-analyzer/
Logic Analyzer Plug-in	Saleae Logic	Adds support for MDIO analysis on Saleae Logic branded logic analyzers. https://github.com/saleae/mdio-analyzer
Oscilloscope Plug-in	Teledyne LeCroy MDIO Decode	Decodes waveforms and translates to an interactive decode table. Clause 22 and Clause 45 support. Provides bit rate measurements. Available for many flagship Teledyne LeCroy oscilloscopes. https://teledynelecroy.com/options/productseries.aspx?mseries=544&groupid=88

7.3 MDIO Register Access Tools

The phytool for Linux provides read/write access to MDIO registers. More information can be found from: https://github.com/wkz/phytool.

7.4 MII/RMII/GMII/RGMII Analyzers

MII/RMII/GMII/RGMII analyzers are available from some major test equipment vendors. These are specialized and costly pieces of equipment, with limited availability and/or long lead times. It is recommended to reach out to your preferred equipment sales representative to discuss availability and options directly.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004754A (09-29-22)	Initial release	

NOTES:

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ISBN: 978-1-6683-1325-1

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