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A	Release		1-20-16
B	Increased +1.2V Capacitor Value & VDD12A Cap Requirement		1-16-17

DOCUMENT DESCRIPTION

Schematic Checklist for the LAN7800, 48-pin SQFN Package

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Document Number	Revision
SC471254	B

Schematic Checklist for LAN7800

Information Particular for the 48-pin SQFN Package

LAN7800 SQFN Phy Interface:

1. TR0P (pin 1); This pin is the transmit/receive positive channel 0 input/output connection of the internal Phy. This pin connects to the 10/100/1000 magnetics.

2. TR0N (pin 2); This pin is the transmit/receive negative channel 0 input/output connection of the internal Phy. This pin connects to the 10/100/1000 magnetics.

3. TR1P (pin 4); This pin is the transmit/receive positive channel 1 input/output connection of the internal Phy. This pin connects to the 10/100/1000 magnetics.

4. TR1N (pin 5); This pin is the transmit/receive negative channel 1 input/output connection of the internal Phy. This pin also connects to the 10/100/1000 magnetics.

5. TR2P (pin 7); This pin is the transmit/receive positive channel 2 input/output connection of the internal Phy. This pin also connects to the 10/100/1000 magnetics.

6. TR2N (pin 8); This pin is the transmit/receive negative channel 2 input/output connection of the internal Phy. This pin also connects to the 10/100/1000 magnetics.

7. TR3P (pin 10); This pin is the transmit/receive positive channel 3 input/output connection of the internal Phy. This pin also connects to the 10/100/1000 magnetics.

8. TR3N (pin 11); This pin is the transmit/receive negative channel 3 input/output connection of the internal Phy. This pin also connects to the 10/100/1000 magnetics.

9. For Transmit/Receive Channel connections and termination details, refer to Figure 1.

10. **Note:** Unlike all previous generations of SMSC / Microchip Ethernet Phys, the Phy within the LAN7800 **does not** require the usual, external 49.9 ohm, 1.0% Ethernet terminations. These terminations have been designed internal to the device.

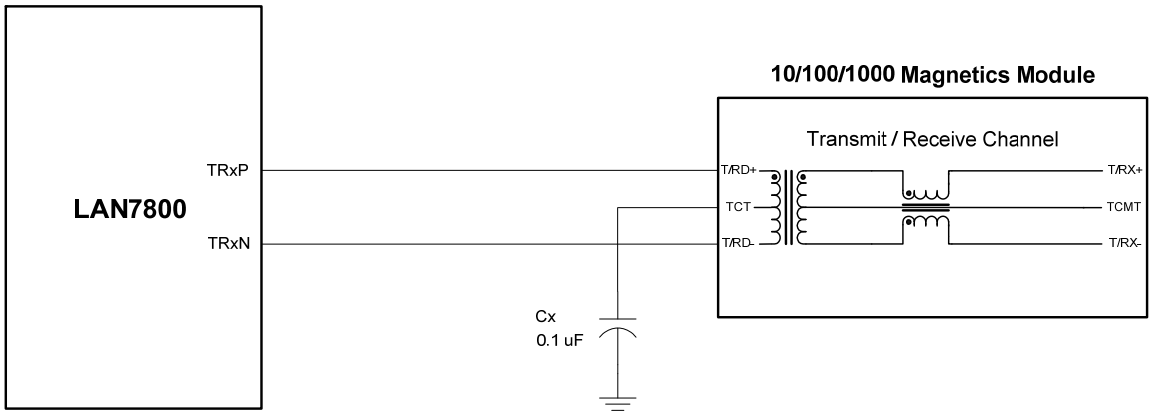


Figure 1 – Transmit / Receive Channel x Connections and Terminations

LAN7800 SQFN Magnetics:

1. The center tap connection on the LAN7800 side for each channel must be AC coupled to digital ground through a 0.1 uF capacitor.

2. The center tap connection on the cable side (RJ45 side) for each channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

3. Assuming the design of an end-point device (NIC), TR0P (pin 1) of the LAN7800 SQFN should trace through the magnetics to pin 1 of the RJ45 connector.

4. Assuming the design of an end-point device (NIC), TR0N (pin 2) of the LAN7800 SQFN should trace through the magnetics to pin 2 of the RJ45 connector.

5. Assuming the design of an end-point device (NIC), TR1P (pin 4) of the LAN7800 SQFN should trace through the magnetics to pin 3 of the RJ45 connector.

6. Assuming the design of an end-point device (NIC), TR1N (pin 5) of the LAN7800 SQFN should trace through the magnetics to pin 6 of the RJ45 connector.

7. Assuming the design of an end-point device (NIC), TR2P (pin 7) of the LAN7800 SQFN should trace through the magnetics to pin 4 of the RJ45 connector.

8. Assuming the design of an end-point device (NIC), TR2N (pin 8) of the LAN7800 SQFN should trace through the magnetics to pin 5 of the RJ45 connector.

9. Assuming the design of an end-point device (NIC), TR3P (pin 10) of the LAN7800 SQFN should trace through the magnetics to pin 7 of the RJ45 connector.

10. Assuming the design of an end-point device (NIC), TR3N (pin 11) of the LAN7800 SQFN should trace through the magnetics to pin 8 of the RJ45 connector.

RJ45 Connector:

1. The RJ45 shield should be attached directly to chassis ground.

+3.3V Power Supply Connections:

1. The analog supply (VDD33A) pin on the LAN7800 SQFN is pin 38. This pin requires a connection to +3.3V. This pin is the +3.3V analog power supply for the USB 2.0 AFE.

2. The VDD33A pin should also have one .01 µF (or smaller) capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.

3. The supply (VDD33_REG_IN) pin for the +2.5V LDO regulator in the LAN7800 SQFN is pin 46. This pin requires a connection to +3.3V.

4. The VDD33_REG_IN pin should also have one .01 µF (or smaller) capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.

5. The supply (VDD_SW_IN) pin for the +1.2V switching regulator in the LAN7800 SQFN is pin 14. This pin requires a connection to +3.3V - +2.5V.

6. The VDD_SW_IN pin should also have one .01 µF (or smaller) capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.

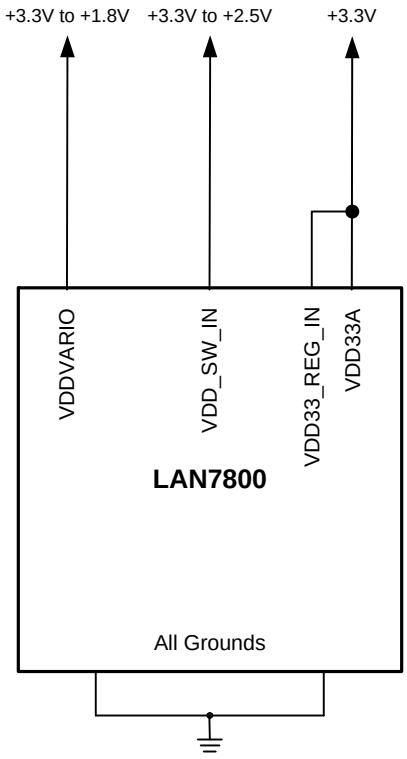


Figure 2 - +3.3V Power Supply Connections

VDDVARIO Power Supply Connections:

1. The VDDVARIO supply pins on the LAN7800 SQFN are 20, 36 & 39. These pins require a connection to +3.3V - +1.8V.

2. Each VDDVARIO pin should also have one .01 μF (or smaller) capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.

+2.5V Power Supply Connections:

1. VDD25_REG_OUT (pin 45), this pin is the output pin of the internal +2.5V LDO regulator for the LAN7800.

2. The VDD25_REG_OUT pin should have one .01 µF (or smaller) capacitor to bypass the LAN7800. The capacitor size should be SMD_0603 or smaller.

3. The VDD25_REG_OUT pin also requires a 1.0 uF, low ESR capacitor. The low ESR requirement is to ensure the proper stability of the +2.5V internal regulator of the LAN7800. We recommend a high quality, low ESR, ceramic type capacitor for this particular application. We recommend the ESR not be any higher than 2.0 ohms for frequency ranges from 10 KHz to 1 GHz.

4. VDD25A (pins 3, 6, 9, & 12), these four input power supply pins should be powered from the internal +2.5V switching regulator. These pins power the Gigabit Ethernet Phy AFE. See figure 3 below for more details.

5. The VDD25A pins should each have one .01 µF (or smaller) capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.

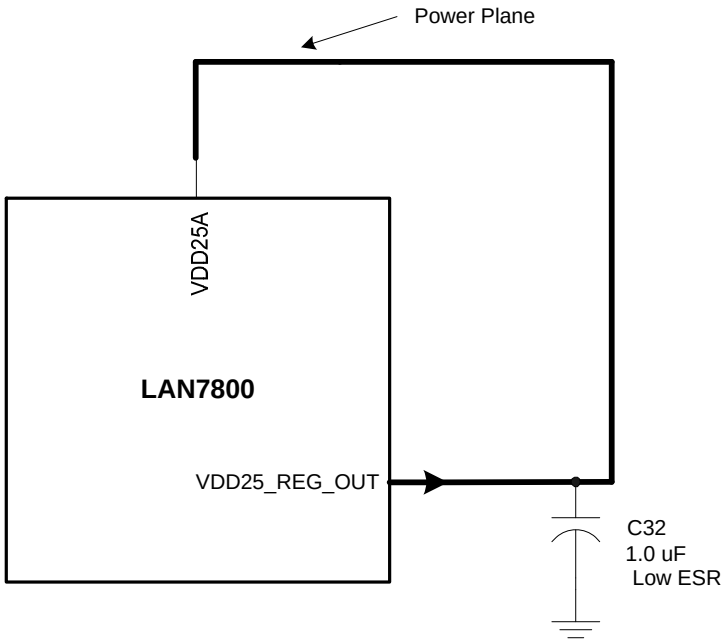


Figure 3 - LAN7800 +2.5V Power Connections

+1.2V Power Supply Connections:

1. VDD12_SW_OUT (pin 13), this pin is the output pin of the internal +1.2V switching regulator for the LAN7800. This pin must be connected directly to a series 3.3 uH inductor.

2. The VDD12_SW_OUT pin / 3.3 uH inductor node in the design should have one .01 μF (or smaller) capacitor to bypass the LAN7800. The capacitor size should be SMD_0603 or smaller.

3. The VDD12_SW_OUT pin / 3.3 uH inductor node also requires a 22 uF, low ESR capacitor. The low ESR requirement is to ensure the proper stability of the +1.2V internal regulator of the LAN7800. We recommend a high quality, low ESR, ceramic type capacitor for this particular application. We recommend the ESR not be any higher than 2.0 ohms for frequency ranges from 10 KHz to 1 GHz.

4. VDD12_SW_FB (pin 15), this pin supplies feedback for the internal +1.2V switching regulator. In this application, this pin should be connected directly to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7800. For applications where the +1.2V internal switching regulator is disabled, simply connect VDD12_SW_FB directly to VDD_SW_IN (pin 14).

5. The VDD12_SW_FB pin should have one .01 μF (or smaller) capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.

6. VDD12CORE (pins 21 & 42), these two core input power supply pins may be powered from the internal +1.2V switching regulator. In this application, these two pins should be connected directly to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7800. See figure 4 below for more details. These two pins can also be supplied from an external +1.2V power supply. In this application, the internal +1.2V switching regulator can be disabled.

7. The VDD12CORE pins should each have one .01 μF (or smaller) capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.

8. VDD12A (pins 25, 30, & 44), these three pins supply power to the analog blocks (Gigabit Ethernet Phy & the USB PLL / AFE section) of the LAN7800 from the internal +1.2V switching regulator through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead. A 1.0 uF, low ESR cap is required on the pin 25, 30 & 44 side of the ferrite bead. In this application, the ferrite bead should be connected to the 3.3 uH output inductor of the +1.2V switching regulator of the LAN7800. See figure 4 below for more details. These three pins can also be supplied from an external +1.2V power supply. In this application, the internal +1.2V switching regulator can be disabled.

9. The VDD12A pins should each have one .01 μF (or smaller) capacitor to decouple the LAN7800. The capacitor size should be SMD_0603 or smaller.

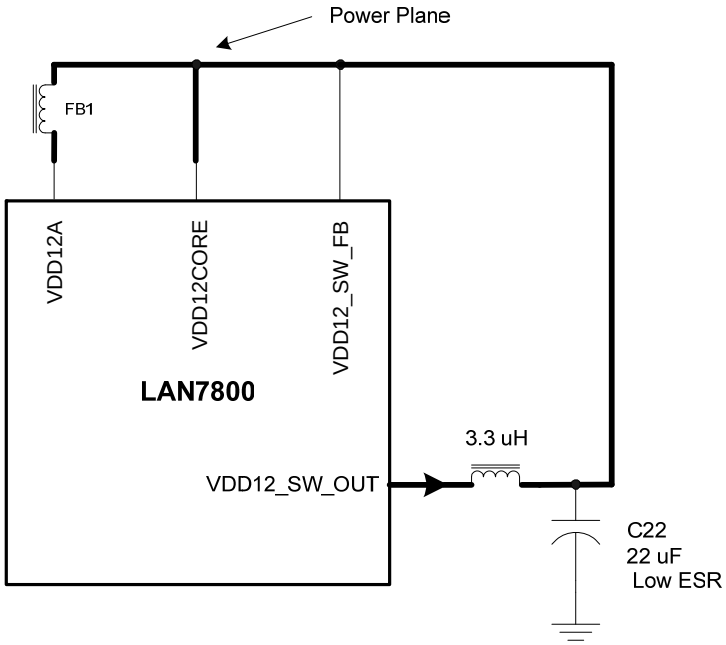


Figure 4 - LAN7800 +1.2V Power Connections

Ground Connections:

1. All grounds, the digital ground pins (GND), the core ground pins (GND_CORE) and the analog ground pins (VSS_A) on the LAN7800 SQFN, are all connected internally to the exposed die paddle ground (VSS). The EDP Ground pad on the underside of the LAN7800 must be connected directly to a solid, contiguous digital ground plane.

2. On the PCB, we recommend one Digital Ground. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN7800 SQFN. For exact specifications and tolerances refer to the latest revision LAN7800 data sheet.

2. XI (pin 40) on the LAN7800 SQFN is the clock circuit input. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XO (pin 41) on the LAN7800 SQFN is the clock circuit output. This pin requires a matching 15 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, the additional external 1.0M Ω resistor across the crystal is no longer required. The necessary resistance has been designed-in internally on the LAN7800 SQFN.

EEPROM Interface:

1. EECS (pin 16) on the LAN7800 SQFN connects to the external EEPROM's CS pin.

2. EECLK (pin 19) on the LAN7800 SQFN connects to the external EEPROM's serial clock pin.

3. EEDI (pin 17) on the LAN7800 SQFN connects to the external EEPROM's Data Out pin.

4. EEDO (pin 18) on the LAN7800 SQFN connects to the external EEPROM's Data In pin.

5. Be sure to select a 3-wire style 2K/4K EEPROM that is organized for 256/512 x 8-bit operation.

6. Be sure to select an EEPROM with an operational voltage that matches your design's VDDVARIO voltage level.

REF_REXT Resistor:

1. REF_REXT (pin 47) on the LAN7800 SQFN should connect to digital ground through a 2.00K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

REF_FILT Capacitor:

1. REF_FILT (pin 48) on the LAN7800 SQFN should connect to digital ground through a 1.0 uF capacitor. This pin is used as an external Phy reference filter for the embedded 10/100 Ethernet Physical device.

2. We recommend using a low ESR capacitor for the REF_FILT cap. The REF_FILT cap should be a high quality, low ESR, ceramic type capacitor for this particular application. We recommend the ESR not be any higher than 2.0 ohms for frequency ranges from 10 KHz to 1 GHz.

USBRBIAS Resistor:

1. USBRBIAS (pin 37) on the LAN7800 SQFN should connect to digital ground through a 12.0K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded USB Physical device.

Required External Pull-ups/Pull-downs:

1. GPIO0 (pin 16) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

2. GPIO1 (pin 17) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

3. GPIO2 (pin 18) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

4. GPIO3 (pin 19) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

5. GPIO4 (pin 22) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

6. GPIO5 (pin 24) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

7. GPIO6 (pin 33) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

8. GPIO7 (pin 43) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

USB Interface:

1. USB2_DP (pin 26), this pin is the USB 2.0 channel positive data pin. This pin should be connected directly to pin 3 (D+) on an upstream USB connector (Type “B”).

2. USB2_DM (pin 27), this pin is the USB channel negative data pin. This pin should be connected directly to pin 2 (D-) on an upstream USB connector (Type “B”).

3. USB3_TXDP (pin 28), this pin is the USB SuperSpeed channel transmit positive data pin. This pin should be connected to pin 6 (SSTX+) on an upstream USB connector (Type “B”) through a 0.1 uF DC blocking capacitor.

4. USB3_TXDM (pin 29), this pin is the USB SuperSpeed channel transmit negative data pin. This pin should be connected to pin 5 (SSTX-) on an upstream USB connector (Type “B”) through a 0.1 uF DC blocking capacitor.

5. For the DC Blocking Caps, SMD_0402 capacitors are recommended (no larger).

6. USB3_RXDP (pin 31), this pin is the USB SuperSpeed channel receive positive data pin. This pin should be connected directly to pin 9 (SSRX+) on an upstream USB connector (Type “B”).

7. USB3_RXDM (pin 32), this pin is the USB SuperSpeed channel receive negative data pin. This pin should be connected directly to pin 8 (SSRX-) on an upstream USB connector (Type “B”).

8. For USB 3.0 Super Speed interconnects, the receiver pins have Auto-Polarity correction, by specification. This allows the pairs to be swapped to facilitate board layout concerns. This allows SSTXP to be swapped with SSTXN **or** SSRXP to be swapped with SSRXN. It does **not** allow for the SSTX channel to be swapped with the SSRX channel. Furthermore, the polarity of the USB 2.0 lines cannot be swapped.

9. Pins 4 & 7 on the USB SuperSpeed connector should be connected directly to digital ground.

10. The metal shield of the USB SuperSpeed connector should be connected directly to a suitable chassis ground plane.

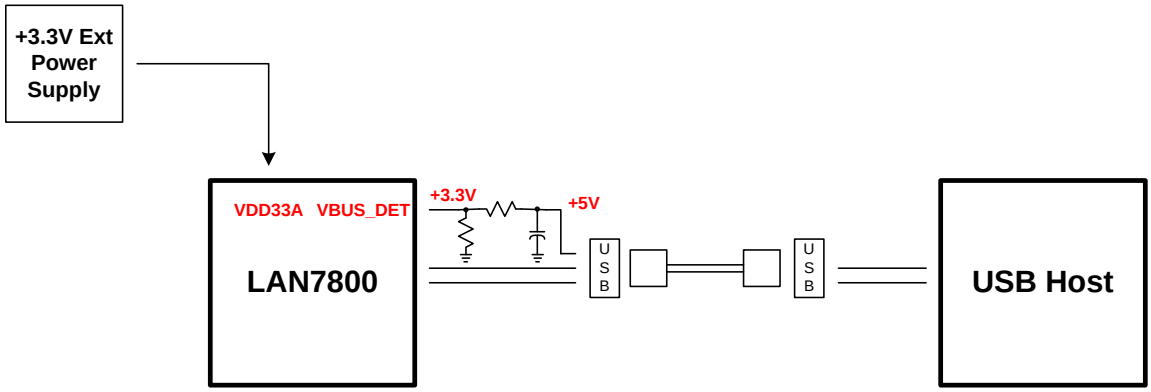
11. For board applications where the USB 3.0 link is between two devices intra-board, the SSTX and SSRX channels must be crossed over. Two DC blocking caps (0.1 uF) should be placed as close as possible to USB3DP_TXDNx & USB3DM_TXDNx on the LAN7800 device. Two more DC blocking caps should be placed on the transmit pins of the other USB 3.0 device.

12. For board applications where the USB 3.0 link uses a USB connector, the RX and TX channels must not be crossed over to the connector. The cross over function is accomplished in the USB cable. Two DC blocking caps (0.1 uF) should be placed as close as possible to USB3DP_TXDNx & USB3DM_TXDNx on the USB connector. Two more DC blocking caps should exist on the transmit pins of the other USB 3.0 device on the other side of the cable.

VBUS_DET Configurations:

Possible VBUS_DET pin (pin 23) connections are dictated by the hardware configuration of the USB link. Possible designs are “Self-Powered Mode”, “Self-Powered Permanently Attached Mode” and “Bus-Powered Mode”. These three possible configurations are depicted below.

Self-Powered Mode:

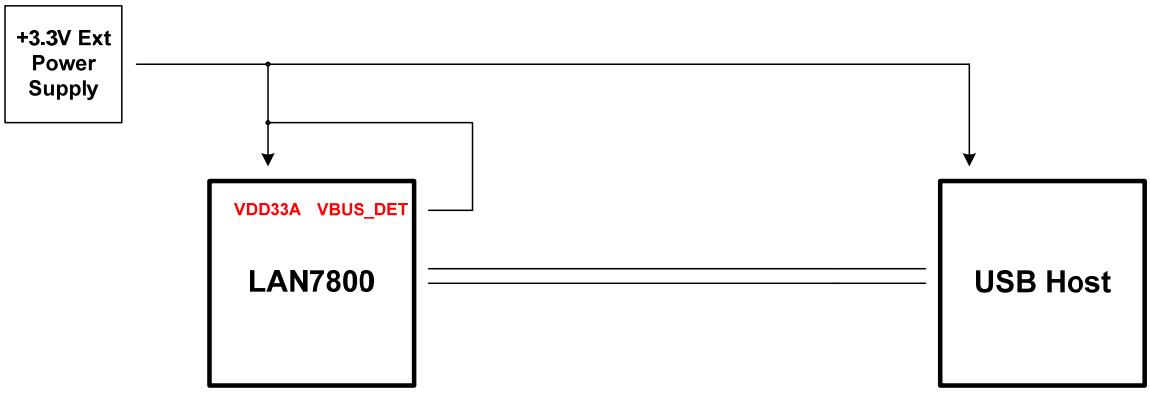


1. In this application, the VBUS_DET pin (pin 23) is driven by a voltage divider circuit that drops the +5V VBUS voltage to +3.3V.

2. For the voltage divider, a series 100K ohm resistor with a 200K ohm resistor to digital ground is recommended.

3. A 2.2 uF capacitor is also recommended on pin 1 (VBUS) of the USB connector.

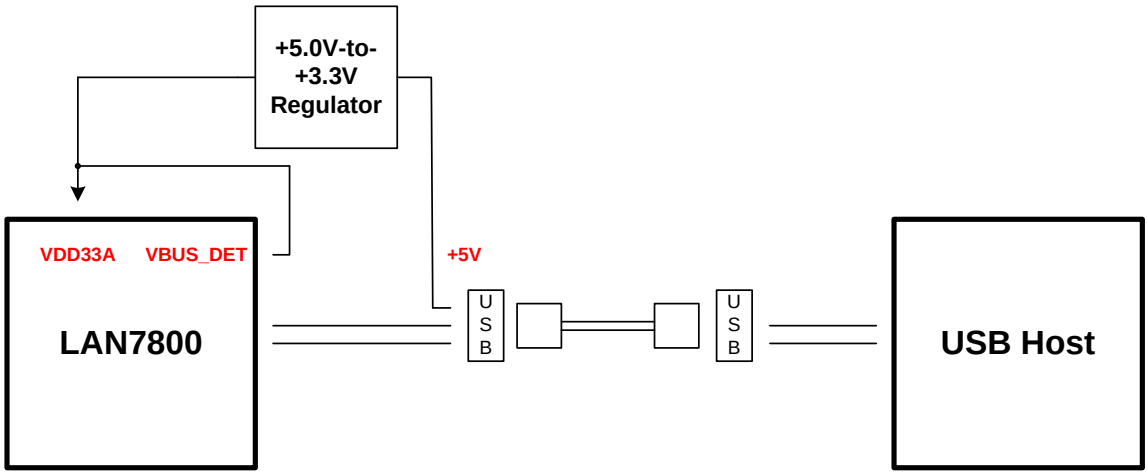
Self-Powered Permanently Attached Mode:



1. In this application, the VBUS_DET pin (pin 23) is driven by the same power rail that powers both the LAN7800 and the USB Host.

2. A series resistor (820 ohms to 10K ohms) may be used on the VBUS_DET pin in order to improve susceptibility characteristics.

Bus-Powered Mode:



1. Typical Bus-Powered applications will connect pin 1 (VBUS) on a standard 4-pin, upstream USB connector (Type “B”) directly to a 2000 mA ferrite bead. This ferrite bead will in turn feed a LDO +5.0V-to-+3.3V voltage regulator to power the LAN7800.

2. We recommend no bulk capacitance be placed on pin 1 (VBUS) of the USB connector in Bus-Powered applications. On the voltage regulator side of the ferrite bead, we recommend limiting the bulk capacitance to 4.7 uF. This should satisfy the 10.0 uF total capacitance to limit in-rush current as required by the USB-IF specification.

3. VBUS_DET (pin 23), this pin detects the state of the supplied upstream power. This pin must be tied to VDD33A when operating in Bus-Powered mode.

Miscellaneous:

1. RESET_N (pin 35) A hardware reset will occur when the RESET_N pin is driven low. Assertion of RESET_N is not required at power-on. However, if used, RESET_N must be driven low for a minimum period as defined in Section 16.6.2, "RESET_N Timing," on page 280. The RESET_N pin is pulled-high internally but must be connected externally to VDDVARIO if unused.

2. RESET_N (pin 35), For a more robust LAN7800 design, a hardware reset (nRST assertion) is recommended following power-up. This signal resets all logic and registers within the LAN7800. SMSC does not recommend the use of an RC circuit for this pin reset. A reset generator / voltage monitor is one option to provide a proper reset. Better yet, for increased design flexibility, a controllable reset (GPIO, dedicated reset output) should be considered. In this case, SMSC recommends a push-pull type output (not an open-drain type) for the monotonic reset to ensure a sharp rise time transition from low-to-high.

3. LED0 (pin 18), LED1 (pin 19), LED2 (pin 24) & LED3 (pin 33), can be programmed via register settings to display various Ethernet activity such as Speed, Link & Duplex Status. See the latest version of the LAN7800 data sheet for complete details.

4. TEST (pin 34), this pin must be tied directly to digital ground in order to ensure proper operation.

5. For a detailed description of the PME pins on the LAN7800, please refer to section 14.0 POWER MANAGEMENT EVENT (PME) OPERATION in the LAN7800 data sheet.

6. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

7. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

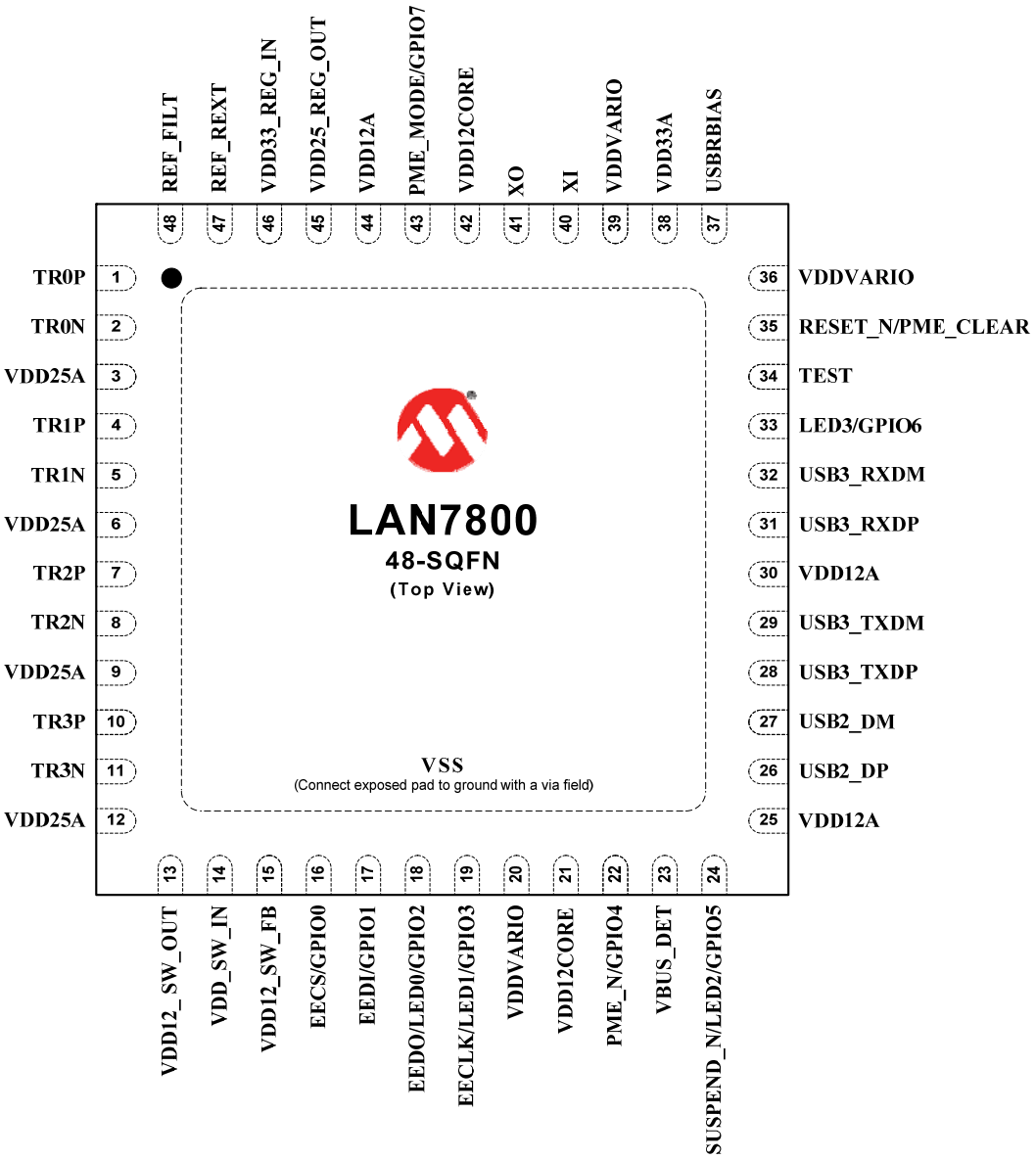
LAN7800 SQFN QuickCheck Pinout Table:

Use the following table to check the LAN7800 SQFN shape in your schematic.

LAN7800 SQFN			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
1	TR0P	25	VDD12A
2	TR0N	26	USB2_DP
3	VDD25A	27	USB2_DM
4	TR1P	28	USB3_TXDP
5	TR1N	29	USB3_TXDM
6	VDD25A	30	VDD12A
7	TR2P	31	USB3_RXDP
8	TR2N	32	USB3_RXDM
9	VDD25A	33	LED3 / GPIO6
10	TR3P	34	TEST
11	TR3N	35	RESET_N / PME_CLEAR
12	VDD25A	36	VDDVARIO
13	VDD12_SW_OUT	37	USBRBIAS
14	VDD_SW_IN	38	VDD33A
15	VDD12_SW_FB	39	VDDVARIO
16	EECS / GPIO0	40	XI
17	EEDI / GPIO1	41	XO
18	EEDO / LED0 / GPIO2	42	VDD12CORE
19	EECLK / LED1 / GPIO3	43	PME_MODE / GPIO7
20	VDDVARIO	44	VDD12A
21	VDD12CORE	45	VDD25_REG_OUT
22	PME_N / GPIO4	46	VDD33_REG_IN
23	VBUS_DET	47	REF_REXT
24	SUSPEND_N / LED2 / GPIO5	48	REF_FILT
49		**EDP Ground Connection Exposed Die Paddle Ground Pad on Bottom of Package**	

Notes:

LAN7800 SQFN Package Drawing:



Note: Exposed pad (VSS) on bottom of package must be connected to ground with a via field.

Reference Material:

1. Microchip LAN7800 Data Sheet; check web site for latest revision.
2. Microchip LAN7800 Reference Design, check web site for latest revision.
3. Microchip Reference Designs are schematics only; there are no associated PCBs.
4. EVB-LAN7800 Customer Evaluation Board & Schematics