REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		1-20-17

DOCUMENT DESCRIPTION

Routing Checklist for the LAN7801, 64-pin SQFN Package

Microchip
80 Arkay Drive, Suite 100
Hauppauge, New York 11788

Document Number	Revision
RC614963	A

Routing Checklist for LAN7801

Information Particular for the 64-pin SQFN Package

RGMII Interface:

1. The RGMII interface on the LAN7801 can be designed using 50-ohm to 68-ohm traces.
2. Similar groups of the RGMII interface should be routed together on the PCB. Transmit channel signals should be routed together and separate from Receive channel signals.
3. RX_CLK and TX_CLK signals should be given sufficient spacing from all other RGMII signals.
4. All RGMII signals should be matched in length with a tolerance of +/- 0.4 inches (400 mils).
5. RGMII signals considered critical should be routed on the top layer next to a contiguous, digital ground plane. Slower RGMII signals can be routed on the bottom layer of the PCB.
6. As with any high-speed digital design, inter-space and intra-space guidelines between MII signals should help to improve crosstalk and signal integrity issues.
7. The use of vias should be kept to a minimum on RGMII interface and switching layers on the PCB is not recommended.

+3.3V Power Supply Connections:

1. Route the VDD33A pin of the LAN7801 SQFN directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

2. In addition, route the VDD33A decoupling capacitor for the LAN7801 SQFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each of the power planes (+3.3V & digital ground plane) for the cap.

3. Route the VDD33_REG_IN pin of the LAN7801 SQFN directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

4. In addition, route the VDD33_REG_IN decoupling capacitor for the LAN7801 SQFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each of the power planes (+3.3V & digital ground plane) for the cap.

5. Route the VDD_SW_IN pin of the LAN7801 SQFN directly into a solid, +3.3V / +2.5V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

6. In addition, route the VDD_SW_IN decoupling capacitor for the LAN7801 SQFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each of the power plane (+3.3V / +2.5V & digital ground plane) for the cap.

VDDVARIO Power Supply Connections:

1. Route the (7) VDDVARIO pins of the LAN7801 SQFN directly into a solid, +1.8V / +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

2. In addition, route the (7) VDDVARIO decoupling capacitors for the LAN7801 SQFN power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+1.8V / +3.3V & digital ground plane) for each cap.

+2.5V Power Supply Connections:

1. Route the VDD25_REG_OUT pin of the LAN7801 SQFN directly into a solid, +2.5V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

2. In addition, route the VDD25_REG_OUT bypass capacitor for the LAN7801 SQFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each of the power plane (+2.5V & digital ground plane) for the cap.

3. In addition, route the VDD25_REG_OUT 1.0 uF low ESR capacitor for the LAN7801 SQFN power pin as short as possible to the power pin. There should be a short, direct copper connection as well as a connection to each of the power plane (+2.5V & digital ground plane) for the cap.

+1.2V Power Supply Connections:

1. The VDD12_SW_OUT pin should be routed to the 3.3 uH inductor with a very short, wide trace.

2. In addition, route the VDD12_SW_OUT / 3.3 uH inductor node bypass capacitor for the LAN7801 SQFN power pin as short as possible to the node. There should be a short, direct copper connection as well as a short connection to the digital ground plane for the cap.

3. In addition, route the VDD12_SW_OUT / 3.3 uH inductor node 22 uF, low ESR bulk capacitor for the LAN7801 SQFN power pin as short as possible to the node. There should be a short, direct copper connection as well as a short connection to the digital ground plane for the cap.

4. Using a mini-plane for the VDD12_SW_OUT / 3.3 uH inductor node is recommended.

5. Route the (2) VDD12CORE pins of the LAN7801 SQFN directly into the solid, +1.2V mini power plane referenced above. The pin-to-plane trace should be as short as possible and as wide as possible.

6. In addition, route the (2) VDD12CORE decoupling capacitors for the LAN7801 SQFN power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+1.2V mini-plane & digital ground plane) for each cap.

7. Route the (3) VDD12A pins of the LAN7801 SQFN directly into a solid, +1.2V mini-power plane (created with a ferrite bead). The pin-to-plane trace should be as short as possible and as wide as possible.

8. In addition, route the (3) VDD12A decoupling capacitors for the LAN7801 SQFN power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+1.2V & digital ground plane) for each cap.

9. The bulk capacitance (1.0 uF, low ESR cap) for the VDD12A power plane can reside anywhere on the plane near pin 37.

Ground Connections:

1. The single digital ground pin (pin 65, EDP) on the LAN7801 SQFN should be connected directly into a solid, contiguous, internal ground plane. The EDP pad on the component side of the PCB should be connected to the internal digital ground plane with 36 power vias in a 6x6 grid.

2. We recommend that all Ground pins be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. The routing for the crystal or clock circuitry should be kept as small as possible and as short as possible.

2. A small ground flood routed under the crystal package on the component layer of PCB may improve the emissions signature. Stitch the flood with multiple vias into the digital ground plane directly below it.

EEPROM Interface:

1. There are no critical routing instructions for the EEPROM interface. Since it is a relatively slow interface, normal board routing measures should suffice.

REF_REXT Resistor:

1. The REF_REXT resistor (pin 1) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the REF_REXT resistor.

REF_FILT Capacitor:

1. The REF_FILT capacitor (pin 2) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the REF_FILT capacitor.

USBRBIAS Resistor:

1. The USBRBIAS resistor (pin 49) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the USBRBIAS resistor.

Required External Pull-ups/Pull-downs:

1. There are no critical routing instructions for the Required External Pull-up/ Pull-down connections.

USB Interface:

1. All USB traces must be routed as differential pairs.

2. Avoid using any stubs on these lines.

3. Use 45 degree turns to minimize impedance discontinuities.

4. In order to further reduce impedance discontinuities, minimize signal reflections and further improve signal integrity, the SuperSpeed pairs should be routed using arcs (recommended).

5. Route the differential pairs over unbroken ground planes or floods.

6. Vias are not typically needed to route the USB signal pairs for Microchip devices. Eliminate or minimize the number of vias used and use a balanced number and placement of them per pair if used.

7. If there is a via requirement for the SuperSpeed traces, (if no other option is available), Microchip recommends the use of coaxial vias and drill out the stubs.

8. Keep the USB pairs as short as possible to reduce signal loss. Traces longer than ~15 cm (~6 in) may significantly degrade signal quality. Minimize the trace length of the differential pairs whenever possible.

9. USB 3.0 SuperSpeed differential pair signals should be length matched to within 5 mils of each other (SSTX+ to SSTX- and SSRX+ to SSRX-).

10. The length of the USB 3.0 SuperSpeed transmit differential pair (SSTX+ and SSTX-) does **not** have to be the same length as the USB 3.0 SuperSpeed receive differential pair (SSRX+ and SSRX-).

11. Route the USB 3.0 SuperSpeed pairs such that they are spaced at least 5 times the trace width away from other non-USB signals.

12. For the LAN7801, the differential impedance of USB 3.0 SuperSpeed signals (SSTX+/- & SSRX+/-) should be 90 ohms +/- 15%. Refer to the USB 3.0 specification for additional information.

13. Trace widths of less than 5 mils is very lossy. We recommend using trace widths of ~8 mils.

14. The +/- signals in each of the USB 3.0 SuperSpeed differential pair can be swapped for easier routing. See the product datasheet for more information on PortSwap.

15. For board applications where the USB 3.0 link is between two devices intra-board, the SSTX and SSRX channels must be crossed over. Two DC blocking caps (0.1 uF) should be placed as close as possible to USB3DP_TXDNx & USB3DM_TXDNx on the USB553XB device. Two more DC blocking caps should be placed on the transmit pins of the other USB 3.0 device.

16. For board applications where the USB 3.0 link uses a USB connector, the RX and TX channels must not be crossed over to the connector. The cross over function is accomplished in the USB cable. Two DC blocking caps (0.1 uF) should be placed as close as possible to USB3DP_TXDNx & USB3DM_TXDNx on the USB connector. Two more DC blocking caps should exist on the transmit pins of the other USB 3.0 device on the other side of the cable.

17. For the DC Blocking Caps, SMD_0402 capacitors are recommended (no larger).

Miscellaneous:

1. Microchip recommends utilizing at least a four-layer design for boards for the LAN7801 SQFN device. The design engineer should be aware, however, as tighter EMC standards are applied to his product and as faster signal rates are utilized by his design, the product design may benefit by utilizing up to eight layers for the PCB construction.

2. As with any high-speed design, the use of series resistors and AC terminations is very application dependant. Buffer impedances should be anticipated and series resistors added to ensure that the board impedance matches the driver. Any critical clock lines should be evaluated for the need for AC terminations. Prototype validation will confirm the optimum value for any series and/or AC terminations.

3. Bulk capacitors for each power plane should be routed immediately into power planes with traces as short as possible and as wide as possible.

4. Following these guidelines and other general design rules in PCB construction should ensure a clean operating system.

5. Trace impedance depends upon many variables (PCB construction, trace width, trace spacing, etc.). The electrical engineer needs to work with the PCB designer to determine all these variables.