AN4746

Microchip KSZ9031MNX to LAN8831 Migration Guide

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INTRODUCTION

This document is for customers with an existing KSZ9031MNX board design migrating to the LAN8831 for their board design. This features a comparison of hardware and software register specifications between the two products. Details on the hardware and software of each device can be found on each product's Microchip web page.

Table 1 summarizes the hardware attribute differences between the KSZ9031MNX and the LAN8831. Table 2 summarizes the register differences between the KSZ9031MNX and the LAN8831. For LAN8831 RGMII usage, please see the *AN4743 KSZ9031RNX to LAN8830 Migration Guide*.

TABLE 1: HARDWARE DIFFERENCES BETWEEN KSZ9031MNX AND LAN8831

Device Attribute	KSZ9031MNX	LAN8831
Analog Low Voltage	AVDDL – 1.2V	VDDAL – 1.1V
Digital Low Voltage	DVDDL – 1.2V	VDD – 1.1V
Management Modes	GMII/MII Only	RGMII_EN Strap PU: RGMII RGMII_EN Strap PD: GMII/RGMII
MII Mode: **TXD4**, **TXD5**, **TXD6**, **TXD7**	In MII Mode, these pins are unused and can be driven high or low.	RGMII/MII: These pins are unused and can be driven high or low. If not driven, these signals require external pull-down resistors.
MII Mode: **GTX_CLK**	Nothing mentioned.	If this pin is not driven, this requires an external pull-down resistor.
MII Mode: **RXD4**, **RXD5**, **RXD6**, **RXD7**	These pins are unused and are driven low.	These pins are unused.
CRS, COL	Nothing mentioned about Duplex mode	Used in Half-duplex mode only
MODE Strapping Pins	**MODE[3:0]** – 0001: GMII mode – Advertise all capabilities (10/100/1000 speed Half-/Full-duplex), except 1000BASE-T Half-duplex – 0100: NAND Tree – 0111: Chip Power Down	**MODE[4:0]** – 10000: GMII mode – Advertise all capabili-ties (10/100/1000 speed Half-/Full-duplex), except 1000BASE-T Half-duplex, EEE Dis-abled – 11000: GMII mode – Advertise all capabili-ties (10/100/1000 speed Half-/Full-duplex), except 1000BASE-T Half-duplex, EEE Enabled – 00100: NAND Tree – 00111: Device Power Down Mode – 01000: Chip Power Down – PLL Enabled – 01001: Chip Power Down – PLL Disabled

TABLE 1: HARDWARE DIFFERENCES BETWEEN KSZ9031MNX AND LAN8831

Device Attribute	KSZ9031MNX	LAN8831
PME	Register setting (MMD 2.2) brings PME signal on either PME_N1 or PME_N2	Register setting sets PME on any of the GPIOs.
ALL-PHYAD	No functionality	Pin 16 can be set to respond to the LAN8831 PHY Address (from PHYAD[4:0]) and PHY Address 0.
Fast Link Failure	None	Can indicate link failure in 1 ms when enabled at 100/1000
PHYAD Strap Range	PHYAD[2:0]	PHYAD[4:0]
Energy Efficient Ethernet (EEE)	No functionality	Supports EEE
LED Modes	Single and Tricolor	Individual (Single), Tricolor, and Enhanced. Enhanced LED mode has more controls for LED function. LED Mode strap for Individual (PU) and Tri-color (PD)
LED Polarity Control	None	LEDPOL[5:1] available
LEDs	2 LEDs (LED1, LED2)	5 LEDs (LED1, LED2, LED3, LED4, LED5)
GPIOs	None	10 GPIOs (GPIO0-GPIO10)
Shorted-Center Tap Magnetic Support	None	MAGJACK Strap
External Connector Loopback	None	Supported
Dynamic Channel Quality	No functionality	Dynamic Channel Quality features: – Mean Square Error (MSE) – Signal Quality Indicator (SQI) – Peak Mean Square Error (pMSE)
ISET Resistor	12.1 kΩ	6.04 kΩ

TABLE 2: REGISTER DIFFERENCES BETWEEN KSZ9031MNX AND LAN8831

Register	KSZ9031MNX	LAN8831
6h	Bit[6:5] – Reserved	Bit 6 – Receive Next Page Location Able Bit 5 – Received Next Page Storage Location
9h	Bit 8 can be set to advertise that PHY is 1000BASE-T Half-duplex capable.	Bit 8 should be set to 0 to advertise that PHY is not 1000BASE-T Half-duplex capable. The KSZ9131MNX does not support this mode.

TABLE 2: REGISTER DIFFERENCES BETWEEN KSZ9031MNX AND LAN8831

Register	KSZ9031MNX	LAN8831
12h	Bits[7:0] – For the open-or short-cable Fault detected in Bits[9:8] of this register, this 8-bit value represents the distance to the cable Fault.	Bits[7:0] – When VCT_SEL = 00, this is the data of cable diagnostics. Valid only when VCT_EN = 0. (1) If cable is normal, i.e., VCT_ST = 00, VCT_DATA don't care. (2) If cable is open or short, i.e., VCT_ST = 01 or 10, the distance to Fault is approximately 0.8 * (VCT_DATA - 22) (Meters) (3) If cable diagnostics failed, i.e., VCT_ST = 11, Bit[7] = 1 means invalid reflected pulse width, i.e. equal or greater than 152 ns, equal or less than 48 ns. Bit[6] = 1 means cable has signal for too long time during WAIT state. It is unusual and for debug only. Bit[5] = 1 means mask100 is detected, and no silent time window can be found for diagnostics. It means high-frequency signal is found on the line. The link partner probably is in forced 100BT or 1000BT mode. Bit[4] = 1 means signals faster than NLP and FLP exist, and no silent time window can be found for diagnostics. It is unusual and for debug only. Bit[3:2] = Number of low pulses detected. If more than 3, stay at 3. Bit[1:0] = Number of high pulses detected. If more than 3, stay at 3.
13h	Bits[15:3] – Reserved Bit 2 – 1000BASE-T Link Status Bit 1 – 100BASE-TX Link Status Bit 0 – Reserved	Bits[15:2] – Reserved Bit 1 – 1000BASE-T Link Status Bit 0 – 100BASE-TX Link Status
16h	Reserved	Bits[15:12] – LED4 Configuration Bits[11:8] – LED3 Configuration Bits[7:4] – LED2 Configuration Bits[3:0] – LED1 Configuration
17h	Reserved	Bits 15, 13, [9:7], [4:2] – Reserved Bit 14 – LED Activity Output Select Bit 12 – LED Pulsing Enable Bits[11:10] – LED Blink/Pulse-Stretch Rate Bits[8:5] – LED Pulse Stretch Enables Bits[3:0] – LED Combination Disables
19h	Reserved	Bit 15 – MDIO Buffer Type Bit 14 – INT Buffer Type Bits[13:8] – LED Buffer Type Bit[7] – PME Polarity Bits[5:0] – LED Polarity
1Ah	Reserved	Bit 15 – Reserved Bit 14 – KSZ9031 LED Mode Bits[13:0] – Reserved

TABLE 2: REGISTER DIFFERENCES BETWEEN KSZ9031MNX AND LAN8831

Register	KSZ9031MNX	LAN8831
1Bh	Bit 15 – Jabber Interrupt Enable Bit 14 – Receive Error Interrupt Bit 13 – Page Receive Interrupt Bit 12 – Parallel Detect Fault Interrupt Bit 11 – Link Partner Acknowledgment Interrupt Bit 10 – Link Down Interrupt Bit 9 – Remote Fault Interrupt Bit 1 – Remote Fault Interrupt	Bits[15:12], 9 – Reserved Bit 11 – Energy Not Detected Interrupt Bit 10 – Energy Detected Interrupt Bit 1 – ADC FIFO Error Interrupt
1Dh	Reserved	Bits[15:12], [9:8], [5:0] – Reserved Bit 11 – spd_clock_gate_override Bit 10 – spd_pll_disable Bit 7 – IO_DC_test_en Bit 6 – VOH
1Eh	Reserved	Bits[15:4], [2:0] – Reserved Bit 3 – External Loopback Enable
1Fh	Bits 8 and 1 – Reserved	Bit 8 – Enable SQE Test Bit 1 – Software Reset
Address 0, Reg. 3h	AN FLP Burst Transmit – LO	Reserved
Address 0, Reg. 4h	AN FLP Burst Transmit – HI	Reserved
Address 1, Reg. 5Ah	Bits[15:4] – Reserved Bits[3:1] – 1000BASE-T Link-Up Time Bit 0 – Reserved	Reserved
Address 2, Reg. 0h	Bits[15:5], 2, 0 – Reserved Bit 4 – LED Mode Override Bit 3 – Single LED Bit 1 – 125 MHz Clock Enable	Bits[15:5], [3:2] – Reserved Bit 4 – Single LED Bit 1 – 125 MHz Clock Enable Bit 0 – All-PHYAD Enable
Address 2, Reg. 1h	Bits[13:8] = Reserved	Bits[13:8] = LED Polarity
Address 2, Reg. 2h	Bits 14, 9, 0 – Reserved Bit 10 – PME_N2 Output Enable Bit 8 – LED1/PME_N1 Strap Override Bit 7 – Chip Power-Down Strap Override Bit 4 – NAND Tree Strap Override Bit 1 – GMII/MII Strap Override	Bits 10, 7 – Reserved Bit 14 – MagJack Strap Bit 9 – Software Power Down w/ PLL Disabled Bit 8 – Software Power Down w/ PLL Enabled Bit 4 – NAND Tree Strap Override Bit 1 – GMII/MII Strap Override Bit 0 – RGMII Mode
Address 2, Reg. 3h	Bits[15:8], [6:5], [3:2], 0 – Reserved Bit 7 – Chip Power-Down Strap Status Bit 4 – NAND Tree Strap Status Bit 1 – GMII/MII Strap Override	Bits 10, 7 – Reserved Bit 14 – MagJack Strap Status Bit 9 – Software Power Down w/ PLL Disabled Status Bit 8 – Software Power Down w/ PLL Enabled Status Bit 4 – NAND Tree Strap Override Status Bit 1 – GMII/MII Strap Status Bit 0 – RGMII Strap Status
Address 1C, Reg. 4h	Bits[15:11], [9:0] – Reserved Bit 10 – 10BASE-Te Mode	Reserved
Address 1C, 0Dh	Reserved	Bit 15 – LDO Enabled Bits 14:12 – LDO Reference Tune
Address 1C, Reg. 23h	Bits[15:1] – Reserved Bit 0 – Energy Detect Power Down Mode	Reserved

Additional features, such as EEE, MSE/SQI and Self-test for frame generation/checking, are accessible in the Indirect Address Registers.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004746A (09-19-22)	Initial release.	

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