AU7860EA Datasheet

USB Host MP3/WMA Decoder SOC

Rev0.1

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Revision History

Date	Revision	Description
2011/10	V0.1	Initial

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Figures

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1. Overview

A highly integrated SOC for MP3/WMA player, AU7860EA integrates MCU, MP3/WMA decoder, OTG, SD/MMC card controller, SARADC, Audio codec, MIC and an IR decoder in a single chip. Compared with traditional flash-MP3 player, AU7860EA offers low cost, low power consumption, flexible and more powerful host MP3/WMA player solution.

1.1 Features

- Enhanced 8051, up to 10 times faster than standard 8051
- OTG 2.0 full-speed controller
- SD/MMC card controller
- Support MP3 decode
- Support WMA decode
- Embedded sound equalizer
- Support tag format ID3v1 and ID3v2.4
- Support FAT16/FAT32 file system
- Embedded 18-bit Audio CODEC
- Support auxiliary audio input
- Support FM audio input
- Embedded SARADC for peripheral controls
- Support record from Microphone/FM input
- Support IR Remote control
- GPIO for various purposes
- Embedded LDO
- Embedded Power-on-Reset
- Embedded 64KB OTP for program code storage

1.2 Chip Architecture

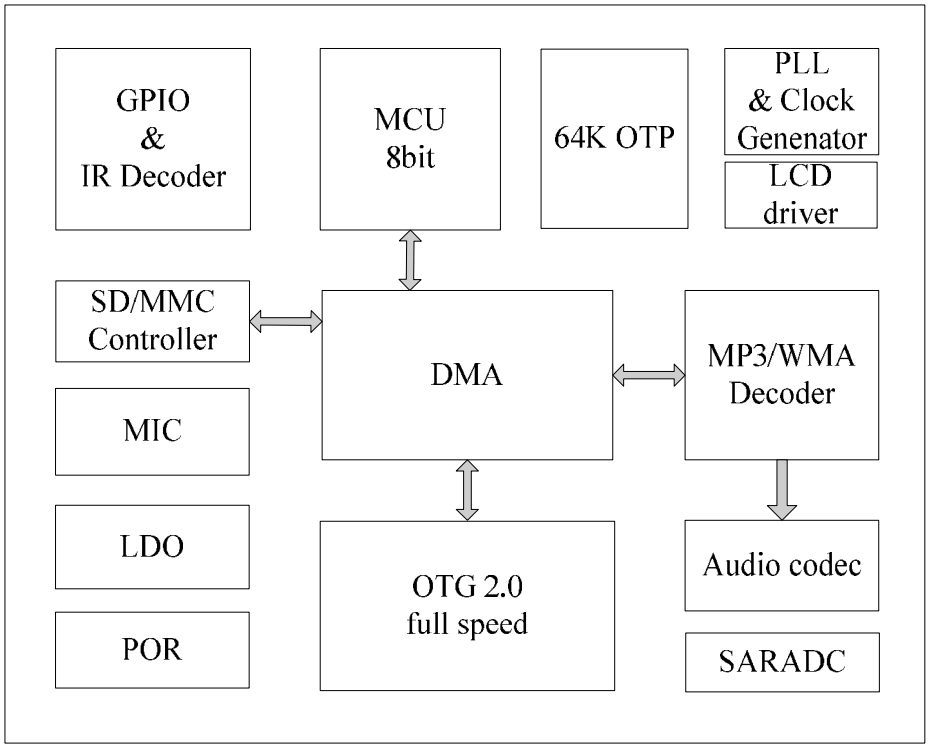

Figure 1 AU7860EA Functional Block Diagram

2. System Application

MP3/WMA audio system

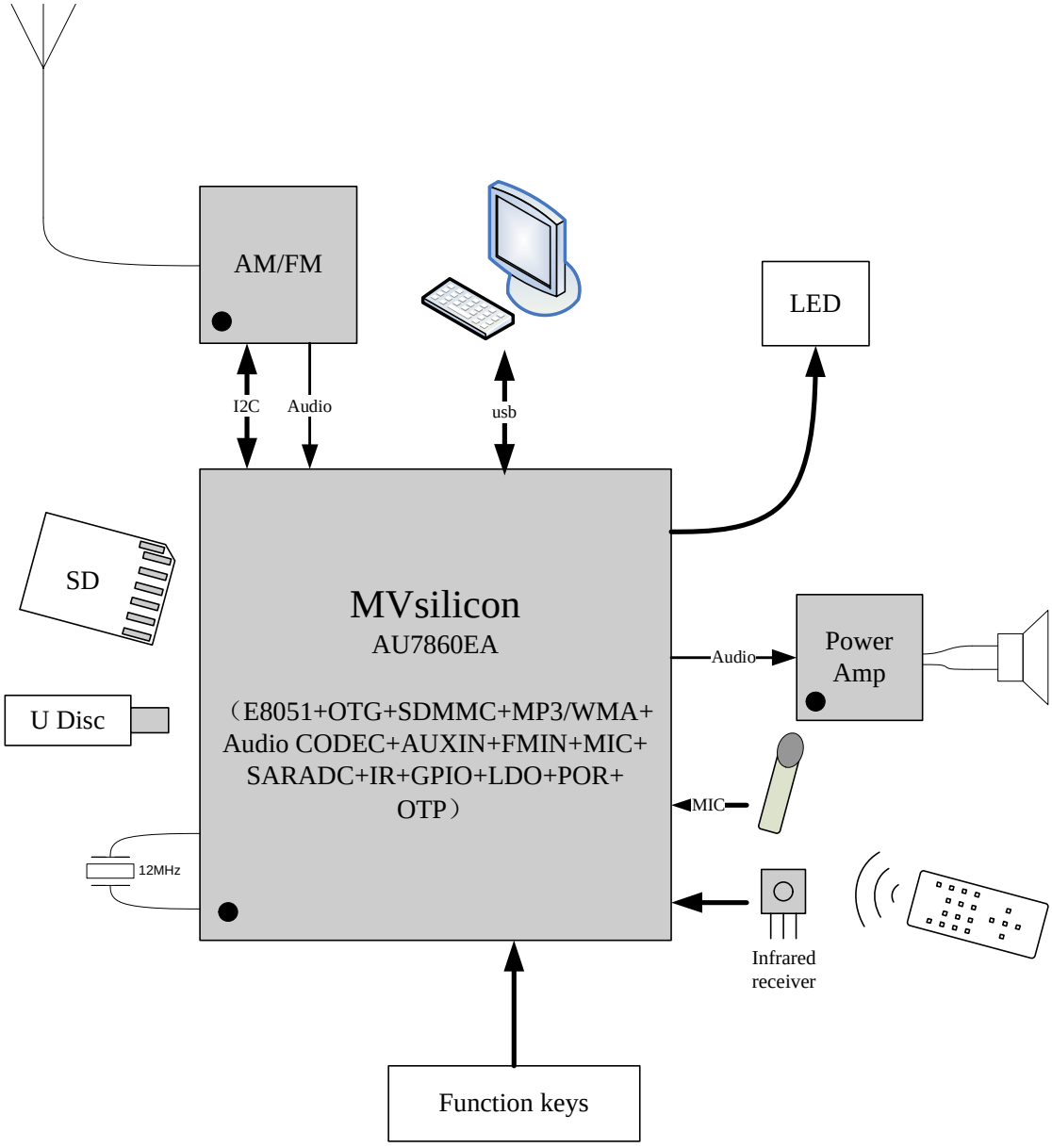

Figure 2 MP3/WMA Audio System

3. Pin Description

AU7860EA is a CMOS device. Floating level on input signals causes unstable device operation and abnormal current consumption. Pull-up or Pull-down resistors should be used appropriately for input or bidirectional pins.

Notation	Description
I	Input
O	Output
I/O	Bidirectional
PWR	Power
GND	Ground

3.1 Pin Description

Table 1 Pin Description

Pin name	Pin #	Type	Description
			USB interface pins
USB_DP	25	I/O	USB Function D+ bus
USB_DM	24	I/O	USB Function D- bus
			Audio CODEC interface pins
DAC_R	13	AO	audio right channel output
DAC_L	14	AO	audio left channel output
DACVMID	12	AI	Internal voltage reference
DAC_AUX_R	15	AI	AUX right channel in
DAC_AUX_L	16	AI	AUX left channel in
MIC	17	AI	Microphone in
			GPIO/MCU IO pins
GPIO_A[1]	6	I/O	GPIO PORT, bank A
GPIO_A[3]	21	I/O	GPIO PORT, bank A
GPIO_A[4]	23	I/O	GPIO PORT, bank A
GPIO_A[5]	22	I/O	GPIO PORT, bank A
GPIO_A[7:6]	19:18	I/O	GPIO PORT, bank A
GPIO_B[2:0]	5:3	I/O	GPIO PORT, bank B
GPIO_C[2:0]	9:7	I/O	GPIO PORT, bank C
			CLK pins
XIN	1	I	12MHz Crystal oscillator input for PLL
XOUT	2	O	12MHz Crystal oscillator output for PLL
			Power/Ground pins
IOVDD	26	PWR	power for IO
COREVDD	28	PWR	power for core
DVSS	20	GND	ground for digital

LDOIN	27	PWR	LDO power in
DACVDD	10	PWR	power for DAC
DACVSS	11	GND	ground for DAC

4. Package

4.1 Package Diagram

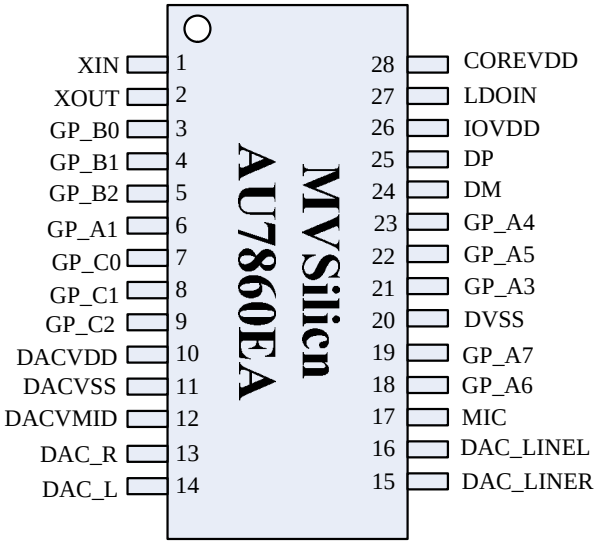

Figure 3 Package Diagram (SOP28 TOP View)

4.2 Package Dimension Parameter

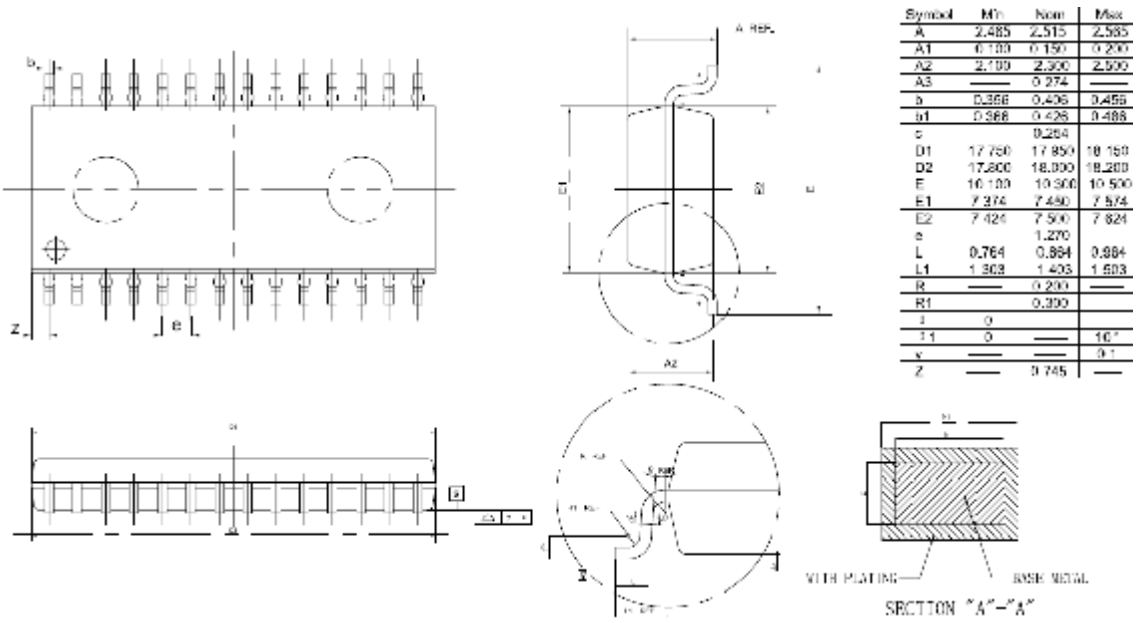

Figure 4 SOP28 Package Dimension Parameter

5. Electrical Specification

5.1 Absolute Maximum Ratings (Note 1)

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Storage Temperature	TEMP_STG	-65 to 150	C

5.2 Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (LDO)	VCC_LDO	3.7		5	V
IO Input Voltage	VIN	0		3.6	V
IO Input Voltage (GPIO_C2)	VIN	0		5.5	V
Operating Free Air Temperature	TEMP_OPR	-40		85	C

5.3 Electrical Characteristics

Table 4 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	Input High Voltage		1.6		3.6	V
VIL	Input Low Voltage		-0.3		1.4	V
VOH	Output high voltage	@IOH=2mA	3.0			V
VOL	Output low voltage	@IOL=2mA			0.3	V
IL	Input leakage current		-10		10	uA
P_PLAY	Power consumption when playing	Playing mode		70		mW

5.4 Audio Performance

Table 5 Audio Performance

Characteristics	Min	Typ	Max	Unit
Frequency Response 20Hz ~ 20KHz		<0.5		DB
THD+N(1KHz out = 800mv rms)		0.1%		%
S/N (1KHz out = 800mv rms)		75		DB
L/R Channel Difference		0		DB
L/R Channel Separation		75		DB
DAC WITH 32OHM Loading OUT POWER		25		MW

Note:

1. "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

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