

# Xilinx Zynq FPGA, TI DSP, MCU

## 프로그래밍 및 회로 설계 전문가 과정

PL GPIO 문서화

강사 – Innova Lee(이상훈)

[gcccompil3r@gmail.com](mailto:gcccompil3r@gmail.com)

학생 – 최준호

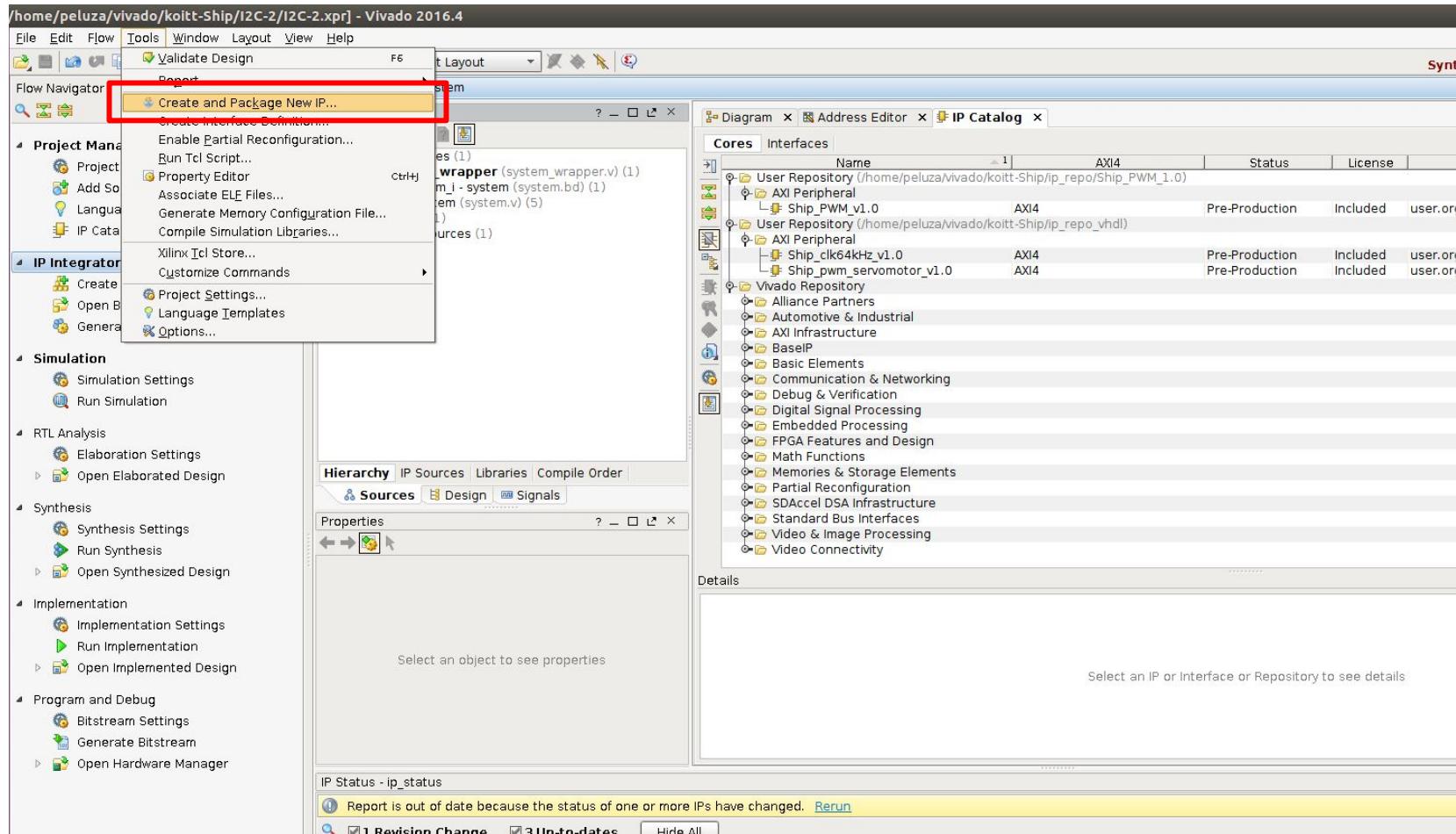
[peluza6332@gmail.com](mailto:peluza6332@gmail.com)

# 목차

- Vivado Custom IP 생성
- Vivado Block Design 수정
- Petalinux로 포팅
- 구동 테스트

# Vivado Custom IP 생성

작업 할 비바도 프로젝트에서 Tools - Create and Package New IP를 누른다.



## Create and Package New IP

### Create Peripheral, Package IP or Package a Block Design

Please select one of the following tasks.



#### Packaging Options

- Package your current project  
Use the project as the source for creating a new IP Definition.
- Package a block design from the current project  
Choose a block design as the source for creating a new IP Definition.  
Select a block design:
- Package a specified directory  
Choose a directory as the source for creating a new IP Definition.

#### Create AXI4 Peripheral

- Create a new AXI4 peripheral  
Create an AXI4 IP, driver, software test application, IP Integrator AXI4 BFM simulation and debug demonstration design.

AXI4 프로토콜의 페리페럴로 만든다.

?

< Back

Next >

Finish

Cancel

## Create and Package New IP

### Peripheral Details

Specify name, version and description for the new peripheral



Name:	Ship_GPIO	<input type="button" value="x"/>
Version:	1.0	<input type="button" value="x"/>
Display name:	Ship_GPIO_v1.0	<input type="button" value="x"/>
Description:	My new AXI IP	<input type="button" value="x"/>
IP location:	/home/peluza/vivado/koitt-Ship/ip_repo	<input type="button" value="x"/> ...

Overwrite existing

IP 이름과 IP 경로를 지정한다.

?

< Back

Next >

Finish

Cancel

**Create and Package New IP**

**Add Interfaces**  
Add AXI4 interfaces supported by your peripheral



Enable Interrupt Support

**Interfaces**

- + -
- S00\_AXI

**S00\_AXI**

**Ship\_GPIO\_v1.0**

Name: S00\_AXI  
Interface Type: Lite  
Interface Mode: Slave  
Data Width (Bits): 32  
Memory Size (Bytes): 64  
Number of Registers: 4 [4..512]

최소 레지스터 갯수인 4개를 사용하며,  
모두 기본 옵션으로 둔다.

? Back Next > Finish Cancel

## Next Steps:

- Add IP to the repository
- Edit IP**
- Verify peripheral IP using AXI4 BFM Simulation interface
- Verify peripheral IP using JTAG interface

바로 IP를 수정할 것이므로 Edit IP를 선택한다.

```
Project Summary x Package IP - Ship_GPIO x Ship_GPIO_v1_0.v x Ship_GPIO_v1_0_S00_AXI.v x
/home/peluzza/vivado/koitt-Ship/ip_repo/Ship_GPIO_1.0/hdl/Ship_GPIO_v1_0_S00_AXI.v

1 `timescale 1 ns / 1 ps
2
3
4 module Ship_GPIO_v1_0_S00_AXI #
5 (
6     // Users to add parameters here
7
8     // User parameters ends
9     // Do not modify the parameters beyond this line
10
11    // Width of S_AXI data bus
12    parameter integer C_S_AXI_DATA_WIDTH      = 32,
13    // Width of S_AXI address bus
14    parameter integer C_S_AXI_ADDR_WIDTH      = 4
15
16 )
17 (
18     // Users to add ports here
19     output wire GPIO0,
20     output wire GPIO1,
21     output wire GPIO2,
22     output wire GPIO3,
23     // User ports ends
24     // Do not modify the ports beyond this line
25
26 endmodule
```

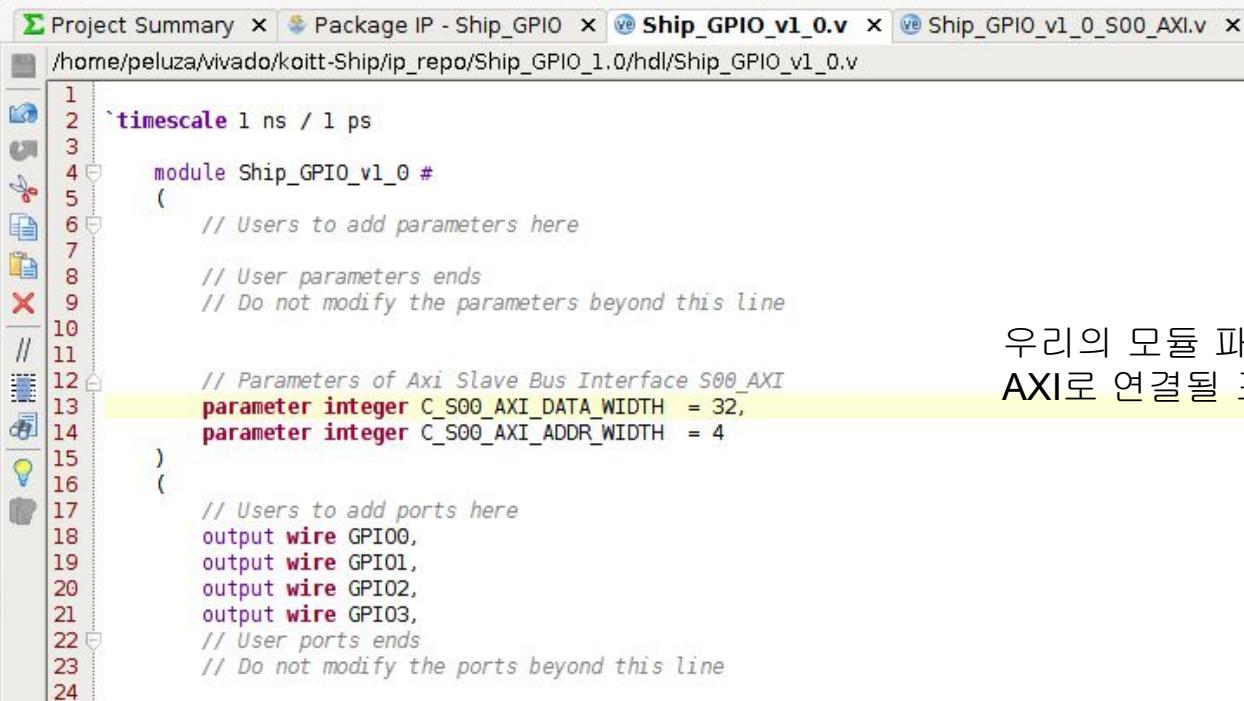
우리 모듈의 하위 AXI 모듈에서  
GPIO를 위한 포트 4개를 만든다.  
(레지스터를 눌렸다면 그에 맞게 눌려준다.)

```

394
395 // Add user logic here
396 assign GPIO0 = slv_reg0 ? 1'b1 : 1'b0;
397 assign GPIO1 = slv_reg1 ? 1'b1 : 1'b0;
398 assign GPIO2 = slv_reg2 ? 1'b1 : 1'b0;
399 assign GPIO3 = slv_reg3 ? 1'b1 : 1'b0;
400 // User logic ends
401
402 endmodule

```

유저 로직 쪽에 레지스터의 값에 따라 GPIO의 비트를 설정해주는 코드를 추가한다.



The screenshot shows the Vivado IP Integrator interface with the 'Ship\_GPIO\_v1\_0.v' file open. The code defines a module named 'Ship\_GPIO\_v1\_0' with parameters for AXI interface widths and four output wires (GPIO0, GPIO1, GPIO2, GPIO3) based on slave register values.

```

Project Summary × Package IP - Ship_GPIO × Ship_GPIO_v1_0.v × Ship_GPIO_v1_0_S00_AXI.v ×
/home/peluzo/vivado/koitt-Ship/IP_repo/Ship_GPIO_1.0/hdl/Ship_GPIO_v1_0.v

1 `timescale 1 ns / 1 ps
2
3
4 module Ship_GPIO_v1_0 #
5 (
6     // Users to add parameters here
7
8     // User parameters ends
9     // Do not modify the parameters beyond this line
10
11
12     // Parameters of Axi Slave Bus Interface S00_AXI
13     parameter integer C_S00_AXI_DATA_WIDTH = 32;
14     parameter integer C_S00_AXI_ADDR_WIDTH = 4
15
16 )
17
18     // Users to add ports here
19     output wire GPIO0,
20     output wire GPIO1,
21     output wire GPIO2,
22     output wire GPIO3,
23
24     // User ports ends
25     // Do not modify the ports beyond this line

```

우리의 모듈 파일(Ship\_GPIO)에서 AXI로 연결될 포트를 똑같이 만들어준다.

```
53 ) Ship_GPIO_v1_0_S00_AXI_inst( -  
54     .GPIO1(GPIO1),  
55     .GPIO2(GPIO2),  
56     .GPIO3(GPIO3),  
57     .GPIO4(GPIO4),  
      ...  
      );
```

4개의 포트들을 이쁘게 잘 넣어준다.

The screenshot shows the Vivado IP Catalog interface. The top navigation bar includes tabs for Project Summary, Package IP - Ship\_GPIO, Ship\_GPIO\_v1\_0.v, and Ship\_GPIO\_v1\_0\_S00\_AXI.v. The main area is titled 'Identification' and contains the following fields:

Vendor:	user.org
Library:	user
Name:	Ship_GPIO
Version:	1.0
Display name:	Ship_GPIO_v1.0
Description:	My new AXI IP
Vendor display name:	(empty)
Company url:	(empty)
Root directory:	/home/peluza/vivado/koitt-Ship/ip_repo/Ship_GPIO_1.0
Xml file name:	/home/peluza/vivado/koitt-Ship/ip_repo/Ship_GPIO_1.0/component.xml

Below the fields is a 'Categories' section with a tree view. The 'AXI\_Peripheral' category is expanded, showing a plus sign (+) icon.

At the bottom of the window, there is a red text message in Korean: "그 후에 패키징을 진행한다." (Proceed with packaging after this).

Packaging Steps &lt;&lt;

✓ Identification

✓ Compatibility

**File Groups**

Customization Pa

Ports and Interface

Addressing and M

Customization GI

Review and Pack:

**File Groups****Merge changes from File Groups Wizard**

Name	Library Name	Type
Standard		
Advanced		
Verilog Synthesis (2)		
Verilog Simulation (2)		
Software Driver (6)		
UI Layout (1)		
Block Diagram (1)		

파일 그룹들 탭에서 변경 사항 머지한다.  
아래는 머지 결과

Packaging Steps &lt;&lt;

✓ Identification

✓ Compatibility

**File Groups**

Customization Pa

Ports and Interface

Addressing and M

Customization GI

Review and Pack:



Name	Library Name	Type
Standard		
Advanced		
Verilog Synthesis (2)		
Verilog Simulation (2)		
Software Driver (6)		
UI Layout (1)		
Block Diagram (1)		

Project Summary × Package IP - Ship\_GPIO × Ship\_GPIO\_v1\_0.v × Ship\_GPIO\_v1\_0\_S00\_AXI.v ×

Packaging Steps <>

- ✓ Identification
- ✓ Compatibility
- ✓ File Groups
- Customization**
- Ports and Interface
- ✓ Addressing and Memory
- Customization GUI
- ✓ Review and Pack:

### Customization Parameters

Merge changes from Customization Parameters Wizard

Name	Description	Display Name	Value
Customization Parameters			
C_S00_AXI_DATA_WIDTH	Width of S_AXI data bus	C S00 AXI DATA WIDTH	32
C_S00_AXI_ADDR_WIDTH	Width of S_AXI address bus	C S00 AXI ADDR WIDTH	4
C_S00_AXI_BASEADDR		C S00 AXI BASEADDR	0xFFFFFFF
C_S00_AXI_HIGHADDR		C S00 AXI HIGHADDR	0x0000000

마찬가지로 커스터마이제이션도 마진

Project Summary × Package IP - Ship\_GPIO × Ship\_GPIO\_v1\_0.v × Ship\_GPIO\_v1\_0\_S00\_AXI.v ×

Packaging Steps <>

- ✓ Identification
- ✓ Compatibility
- ✓ File Groups
- Customization**
- Ports and Interface
- ✓ Addressing and Memory
- Customization GUI
- Review and Pack:

### Customization Parameters

Name	Description	Display Name	Value
Customization Parameters			
C_S00_AXI_DATA_WIDTH	Width of S_AXI data bus	C S00 AXI DATA WIDTH	32
C_S00_AXI_ADDR_WIDTH	Width of S_AXI address bus	C S00 AXI ADDR WIDTH	4
C_S00_AXI_BASEADDR		C S00 AXI BASEADDR	0xFFFFFFF
C_S00_AXI_HIGHADDR		C S00 AXI HIGHADDR	0x00000000

## Packaging Steps &lt;

Identification

Compatibility

File Groups

Customization Pa

## Ports and Inter

Addressing and T

Customization GL

Review and Pack:

## Ports and Interfaces

1 warning

Name	Interface Mode	Enablement Dependency	Is Declaration	Direction	Dr
S00_AXI	slave		<input type="checkbox"/>		
Clock and Reset Signals			<input type="checkbox"/>		
GPIO0			<input type="checkbox"/>	out	
GPIO1			<input type="checkbox"/>	out	
GPIO2			<input type="checkbox"/>	out	
GPIO3			<input type="checkbox"/>	out	

경고가 날 수도 있고 아닐 수도 있으나 무시해도 된다.

## Packaging Steps &lt;&lt;

 Identification Compatibility File Groups Customization Pa Ports and Interfa Addressing and M Customization

Review and Pack:

## Customization GUI

## Layout



- Window
- Component Name
- Page 0
  - C S00 AXI DATA WIDTH
  - C S00 AXI ADDR WIDTH
  - C S00 AXI BASEADDR
  - C S00 AXI HIGHADDR
- Hidden Parameters

## Preview

 Show disabled portsComponent Name C S00 AXI DATA WIDTH C S00 AXI ADDR WIDTH C S00 AXI BASEADDR C S00 AXI HIGHADDR 

우리가 만든 간단한 GPIO는 파라미터 따위 없다.  
(하드웨어 단에서 GPIO 초기화 하고 싶다면 만들어라! 하!  
하하!)

## Packaging Steps &lt;&lt;

✓ Identification

✓ Compatibility

✓ File Groups

✓ Customization Pa

⚠ Ports and Interfa

✓ Addressing and M

✓ Customization GL

## Review and Pa

## Review and Package

! 1 warning 2 info messages

## Summary

Display name: Ship\_GPIO\_v1.0

Description: My new AXI IP

Root directory: /home/peluzza/vivado/koitt-Ship/ip\_repo/Ship\_GPIO\_1.0

## After Packaging

- An archive will not be generated. Use the settings link below to change your preference
- Project will be removed after completion

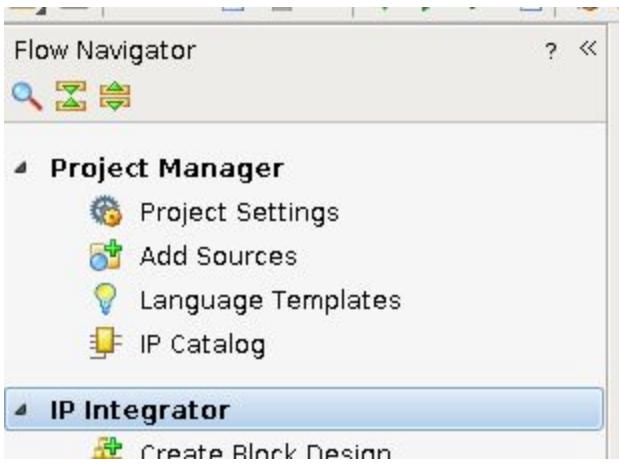
[edit packaging settings](#)

아래 패키지 IP를 눌러서 마무리.

[Re-Package IP](#)



예아를 눌러 끈다.



그 후에 원 프로젝트로 돌아와서 Flow Navigator에서 IP Catalog를 눌러 이동한다.

# Vivado Block Design 수정

Flow Navigator ? < >

**Block Design system**

Sources ? - □ x

Project Manager

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

**IP Integrator**

- Create Block Design
- Open Block Design
- Generate Block Design

Simulation

- Simulation Settings
- Run Simulation

RTL Analysis

- Elaboration Settings
- Open Elaborated Design

Synthesis

- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

Implementation

- Implementation Settings
- Run Implementation
- Open Implemented Design

Program and Debug

- Bitstream Settings
- Generate Bitstream
- Open Hardware Manager

Block Design system

Design Sources (1)

- system\_wrapper (system\_wrapper.v) (1)
  - system - system (system.bd) (1)
  - system (system.v) (5)
- Constraints (1)
- Simulation Sources (1)

Cores | Interfaces

Name	AXI4	Status	License	VLAN
User Repos /home/peluz/vivado/koitt-Ship/ip_repo/Ship_GPIO_1.0	Properties... Ctrl+E	Pre-Production	Included	user.org:user:Ship_GPIO:1.0
User Repos /repo/Ship_PWM_1.0	Properties... Ctrl+E	Pre-Production	Included	user.org:user:Ship_PWM:1.0
User Repos /repo_vhdl	Properties... Ctrl+E	Pre-Production	Included	user.org:user:Ship_clk64kHz:1.0
Vivado Repo	Properties... Ctrl+E	Pre-Production	Included	user.org:user:Ship_pwm_servomotor:1.0

Hierarchy IP Sources Libraries Compile Order

Sources Design Signals

Repository Properties ? - □ x

User Repository

Path : /home/peluz/vivado/koitt-Ship/ip\_repo/Ship\_GPIO\_1.0

Number of IPs : 1

Number of interfaces : 0

General IPs

Path: /home/peluz/vivado/koitt-Ship/ip\_repo/Ship\_GPIO\_1.0

Number of IPs: 1

Number of interfaces: 0

IP Status - ip\_status

Report is out of date because the status of one or more IPs have changed. [Rerun](#)

1 Revision Change 3 Up-to-dates Hide All

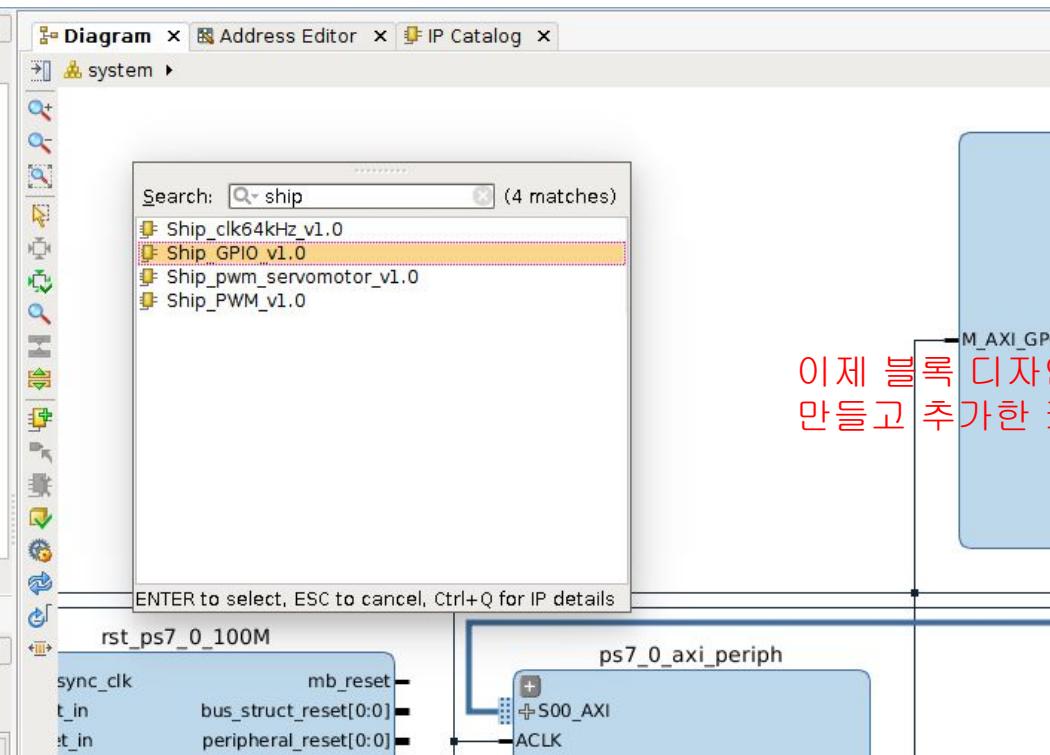
Source File	IP Status	Recommendation	Change Log	IP Name	Current Version	Recommended Version	Licenses
/system (4)	IP revision change. IP definition 'Ship_PWM_v1.0 (1.0)' changed on disk. <a href="#">Upgrade IP</a>	No changes required	<a href="#">More Info</a>	Ship_PWM_v1.0	1.0 (Rev. 13)	1.0 (Rev. 14)	Included
/rst_ps7_0_100M	Up-to-date	No changes required	<a href="#">More Info</a>	Processor System Reset	5.0 (Rev. 10)	5.0 (Rev. 10)	Included
/processing_system7_0	Up-to-date	No changes required	<a href="#">More Info</a>	ZYNQ Processing System	5.5 (Rev. 3)	5.5 (Rev. 3)	Included
/ps7_0_axi_periph	Up-to-date	No changes required	<a href="#">More Info</a>	AXI Interconnect	2.1 (Rev. 12)	2.1 (Rev. 12)	Included

Upgrade Selected

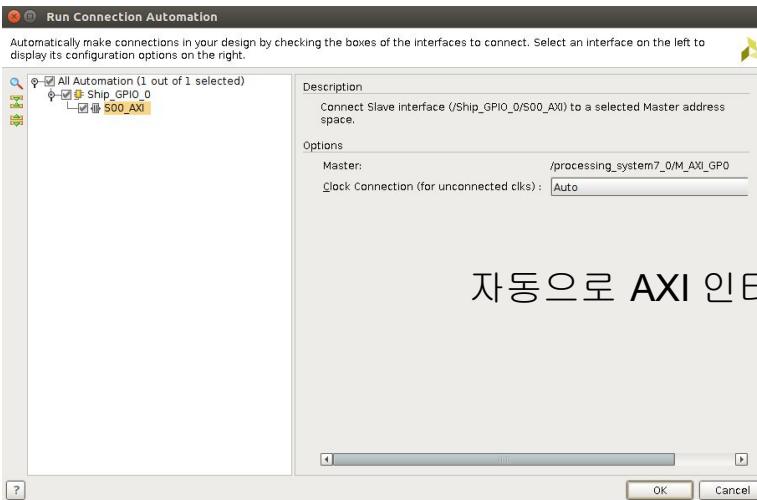
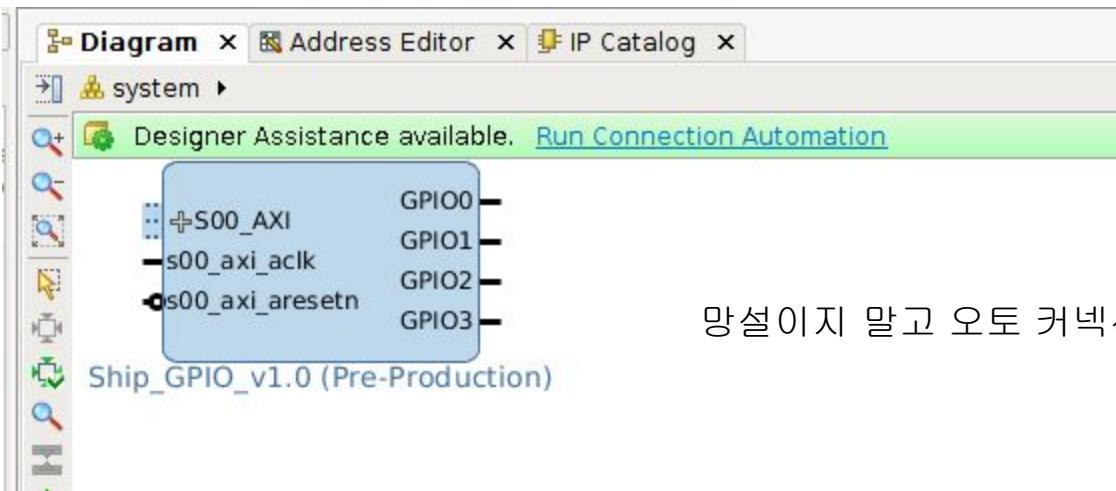
Tcl Console Messages Log IP Status Reports Design Runs

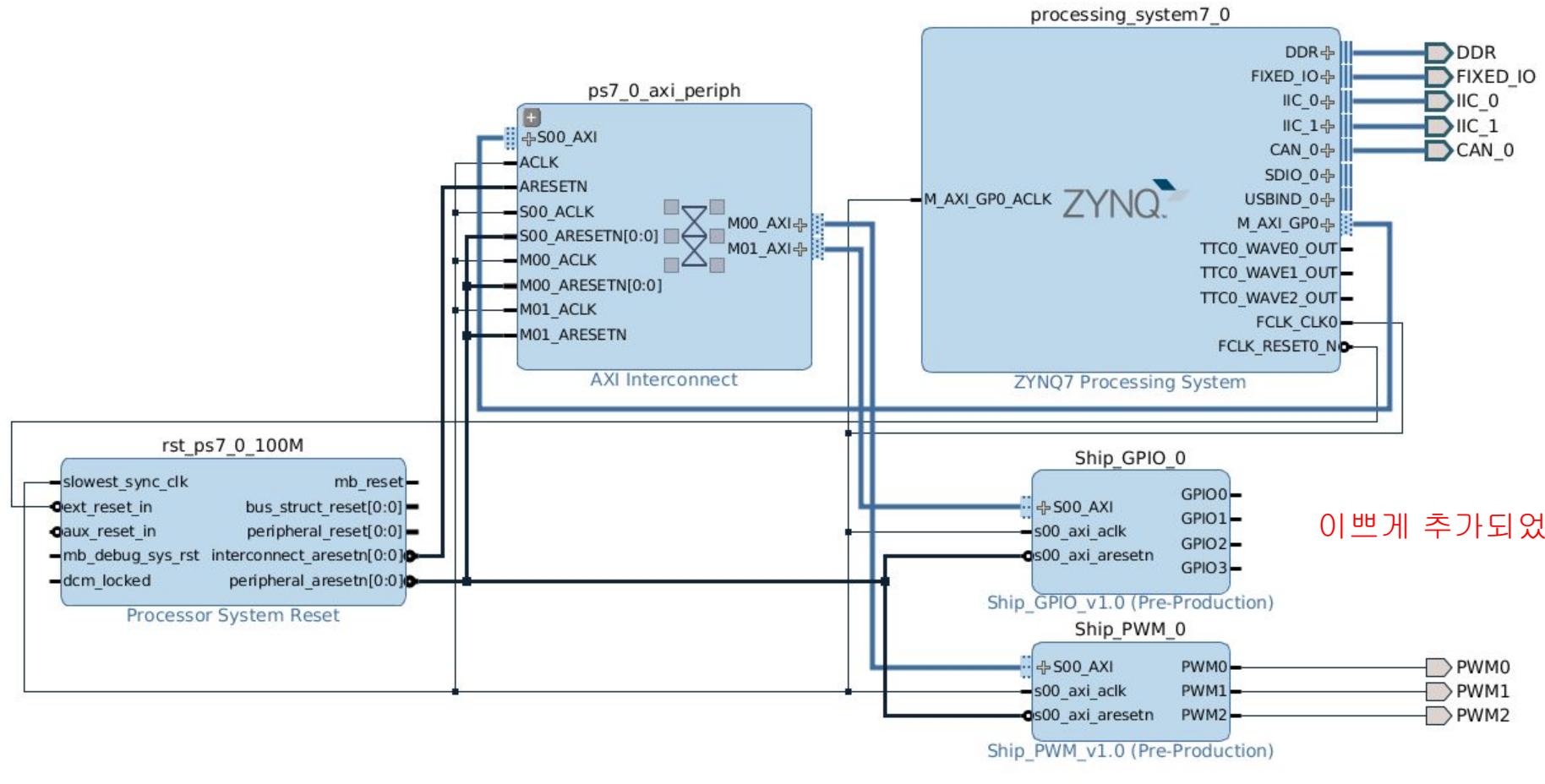
리프레시 레파지토리 한 번 해준다.

추가된 IP를 확인하시라.



이제 블록 디자인 화면에서,  
만들고 추가한 커스텀 IP를 하나 가져온다.





**Flow Navigator**

**Project Manager**

- Project Settings
- Add Sources
- Language Templates
- IP Catalog

**IP Integrator**

- Create Block Design
- Open Block Design
- Generate Block Design

**Simulation**

- Simulation Settings
- Run Simulation

**RTL Analysis**

- Elaboration Settings
- Open Elaborated Design

**Synthesis**

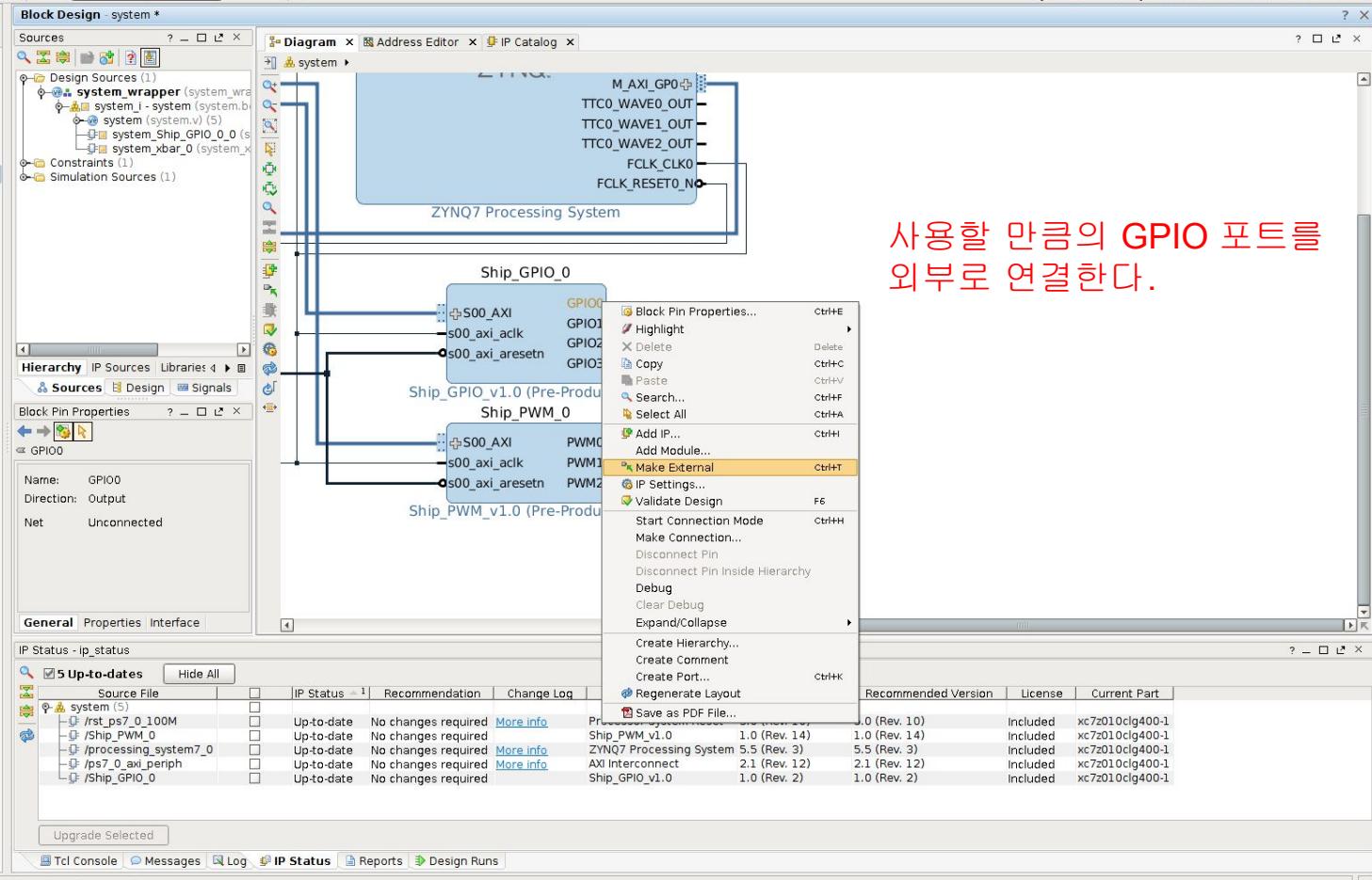
- Synthesis Settings
- Run Synthesis
- Open Synthesized Design

**Implementation**

- Implementation Settings
- Run Implementation
- Open Implemented Design

**Program and Debug**

- Bitstream Settings
- Generate Bitstream
- Open Hardware Manager



사용할 만큼의 GPIO 포트를 외부로 연결한다.



구성에 문제가 없는지 유효성 검사를 한다.

File Edit Flow Tools Window Layout View Help

Default Layout

Sources Diagram Address Editor IP Catalog

Block Design system \*

Design Sources (1)

- system\_wrapper (system\_wrapper)
- system\_i - system
- system\_sh
- system\_xba

Constraints (1)

Simulation Sources (1)

Create HDL Wrapper...

View Instantiation Template

Generate Output Products...

Reset Output Products...

Replace File...

Copy File Into Project

Copy All Files Into Project

Remove File from Project...

Enable File

Disable File

Hierarchy Update

Refresh Hierarchy

IP Hierarchy

Set as Top

Add Module to Block Design

Set File Type...

Set Used In...

Edit Constraints Sets...

Edit Simulation Sets...

Associate ELF Files...

Add Sources...

Report IP Status

Go to Source

Enabled

Location: /home/pe

Type: Block De

Part: xc7z010clg400-1

Size: 54.1 KB

Modified: Today at 22:18:59 P

General Properties

Hierarchy IP Sources Lib

Sources Design

Source File Properties

system.bd

ZYNQ7 Processing System

M\_AXI\_GP0+  
TTC0\_WAVE0\_OUT  
TTC0\_WAVE1\_OUT  
TTC0\_WAVE2\_OUT  
FCLK\_CLK0  
FCLK\_RESET0\_N

Ship\_GPIO\_0

S00\_AXI GPIO0  
s00\_axi\_aclk GPIO1  
s00\_axi\_araddr GPIO2  
s00\_axi\_arprot GPIO3

Ship\_PWM\_0

S00\_AXI PWM0  
s00\_axi\_aclk PWM1  
s00\_axi\_araddr PWM2

Ship\_GPIO\_v1.0 (Pre-Production)

Ship\_PWM\_v1.0 (Pre-Production)

IP Status - ip\_status

5 Up-to-dates Hide All

Source File	IP Status	Recommendation	Change Log	IP Name	Current Version	Recommended Version	License	Current Part
/rst_ps7_0_100M	Up-to-date	No changes required	<a href="#">More info</a>	Processor System Reset	5.0 (Rev. 10)	5.0 (Rev. 10)	Included	xc7z010clg400-1
/ship_PWM_0	Up-to-date	No changes required	<a href="#">More info</a>	Ship_PWM_v1.0	1.0 (Rev. 14)	1.0 (Rev. 14)	Included	xc7z010clg400-1
/ps7_0_axi_periph	Up-to-date	No changes required	<a href="#">More info</a>	ZYNQ7 Processing System	5.5 (Rev. 3)	5.5 (Rev. 3)	Included	xc7z010clg400-1
/Ship_GPIO_0	Up-to-date	No changes required	<a href="#">More info</a>	AXI Interconnect	2.1 (Rev. 12)	2.1 (Rev. 12)	Included	xc7z010clg400-1
				Ship_GPIO_v1.0	1.0 (Rev. 2)	1.0 (Rev. 2)	Included	xc7z010clg400-1

Upgrade Selected

Tcl Console Messages Log IP Status Reports Design Runs

Generate HDL wrapper file and copy into project

Synthesis and implementation out-of-date more info

처음 프로젝트를 만들었다면,  
Output Product와  
HDL Wrapper를 만들자.

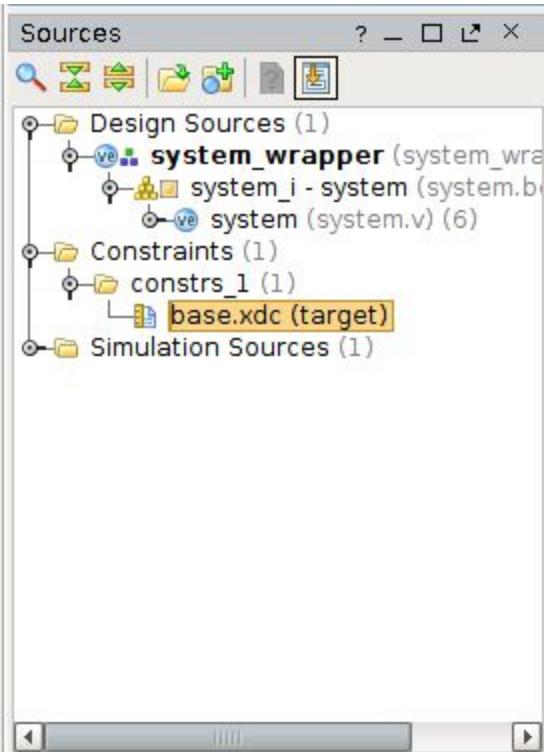


Diagram Address Editor IP Catalog base.xdc \*

/home/peluza/Vivado/koitt-Ship/I2C-2/I2C-2.srcts/constrs\_1/new/base.xdc

```
1 set_property PACKAGE_PIN J15 [get_ports iic_0_scl_io]
2 set_property PACKAGE_PIN H15 [get_ports iic_0_sda_io]
3 set_property IOSTANDARD LVCMOS33 [get_ports iic_0_scl_io]
4 set_property IOSTANDARD LVCMOS33 [get_ports iic_0_sda_io]
5 set_property PULLUP true [get_ports iic_0_scl_io]
6 set_property PULLUP true [get_ports iic_0_sda_io]
7
8 set_property PACKAGE_PIN P14 [get_ports iic_1_scl_io]
9 set_property PACKAGE_PIN R14 [get_ports iic_1_sda_io]
10 set_property IOSTANDARD LVCMOS33 [get_ports iic_1_scl_io]
// 11 set_property IOSTANDARD LVCMOS33 [get_ports iic_1_sda_io]
12 set_property PULLUP true [get_ports iic_1_scl_io]
13 set_property PULLUP true [get_ports iic_1_sda_io]
14
15 set_property PACKAGE_PIN V15 [get_ports CAN_0_rx]
16 set_property PACKAGE_PIN W15 [get_ports CAN_0_tx]
17 set_property IOSTANDARD LVCMOS33 [get_ports CAN_0_rx]
18 set_property IOSTANDARD LVCMOS33 [get_ports CAN_0_tx]
19
20 set_property IOSTANDARD LVCMOS33 [get_ports PWM0]
21 set_property IOSTANDARD LVCMOS33 [get_ports PWM1]
22 set_property IOSTANDARD LVCMOS33 [get_ports PWM2]
23 set_property PACKAGE_PIN U14 [get_ports PWM0]
24 set_property PACKAGE_PIN U15 [get_ports PWM1]
25 set_property PACKAGE_PIN V17 [get_ports PWM2]
26
27 set_property IOSTANDARD LVCMOS33 [get_ports GPIO0]
28 set_property PACKAGE_PIN V18 [get_ports PWM0]
29
```

제약 사항을 추가한다.

system &gt;

이런 모양의 블록도로 합성과 및 구현,  
최종적으로 비트 스트림을 만들 것이다.

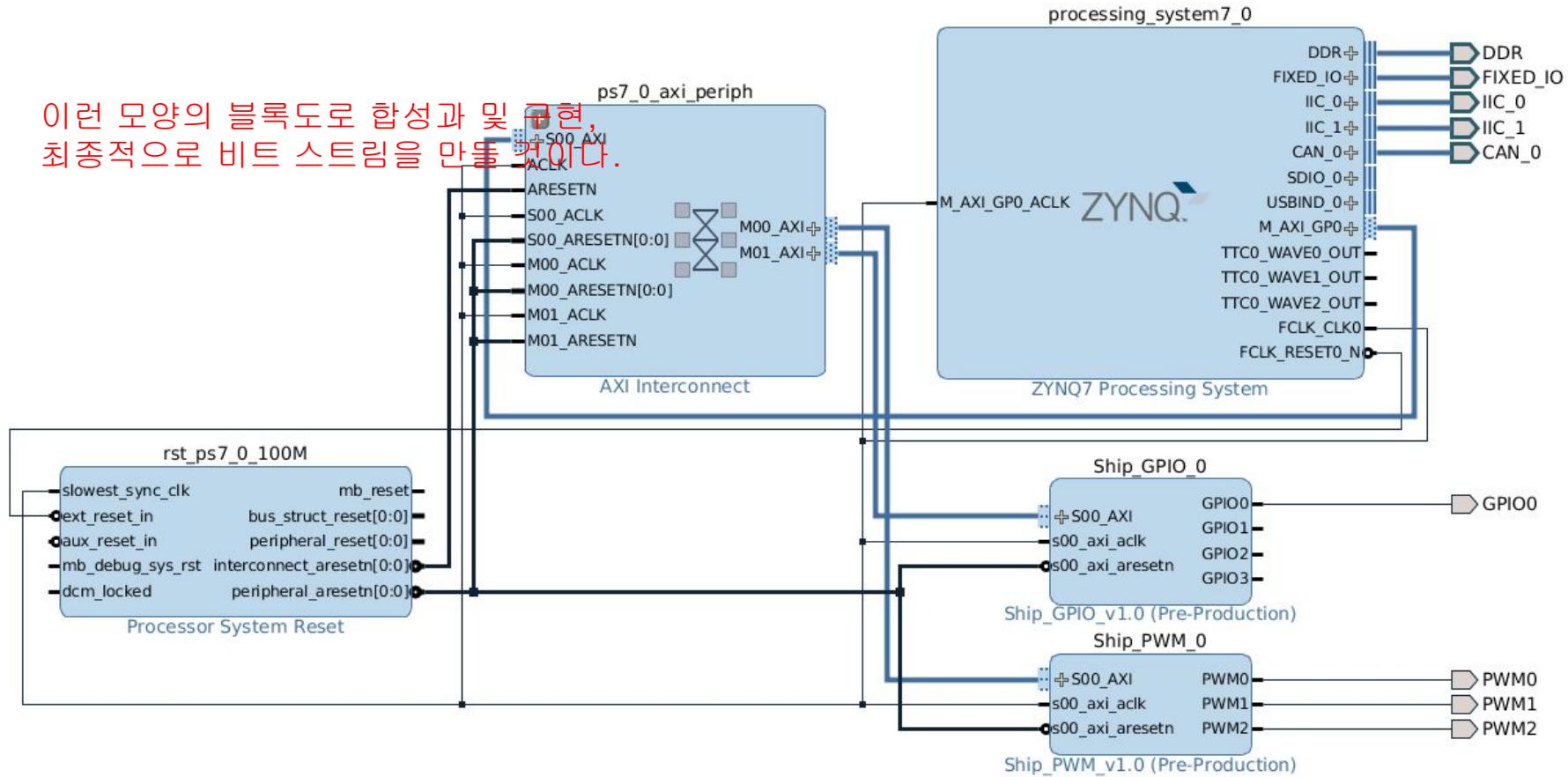
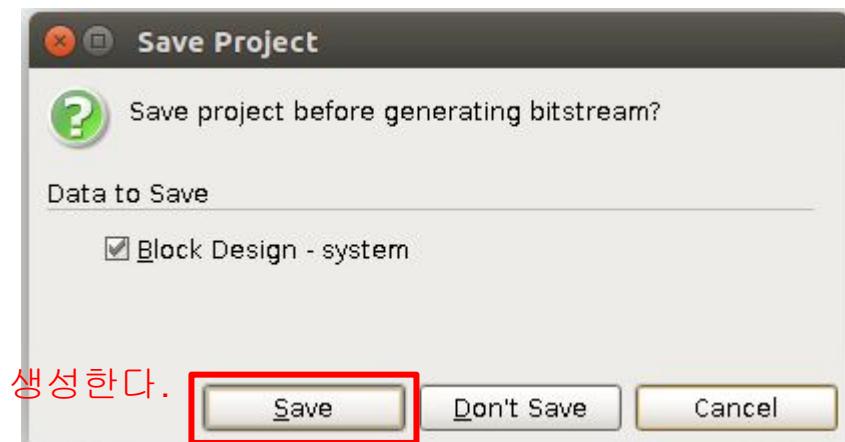


Diagram × Address Editor × IP Catalog × base.xdc ×

Cell	Slave Interface	Base Name	Offset Address	Range	High Address
processing_system7_0					
Data (32 address bits : 0x40000000 [1G])					
Ship_PWM_0	S00_AXI	S00_AXI_reg	0x43C0_0000	64K	0x43C0_FFFF
Ship_GPIO_0	S00_AXI	S00_AXI_reg	0x43C1_0000	64K	0x43C1_FFFF

건드려야 할 레지스터 주소를 잘 기억하도록 한다.



자 이제 Generate Bitstream을 하여 데이터를 생성한다.

## Launch Runs

Launch the selected synthesis or implementation runs.

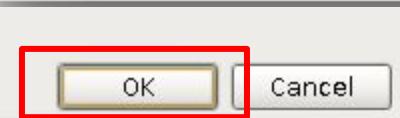
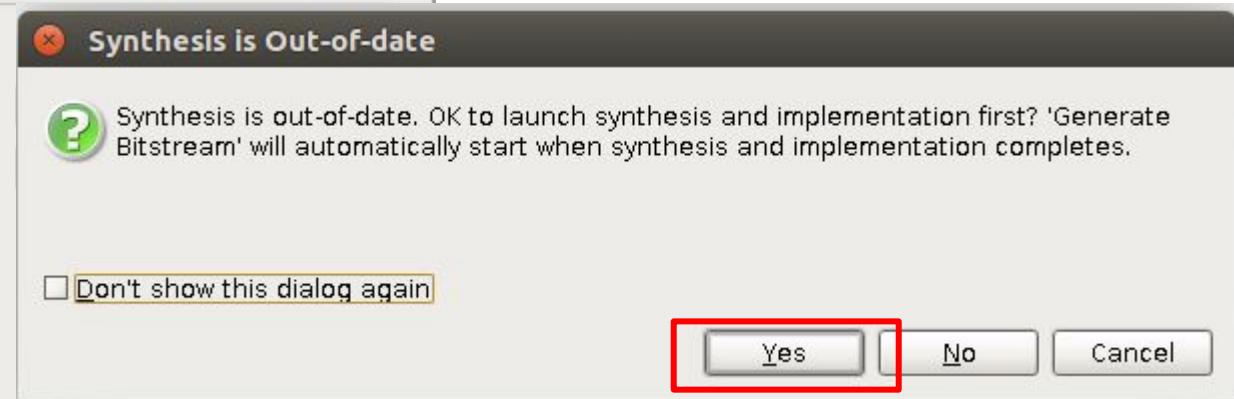


Launch directory:

### Options

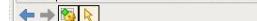
- Launch runs on local host:
- Launch runs on remote hosts
- Launch runs using LSF
- Generate scripts only

Don't show this dialog again



컴퓨터로 기본 환경이라면 당연히 local host,  
Generate Bitstream 이전에 합성과 구현을 먼저 할거에요? '네!'

- Design Sources (1)
  - system\_wrapper (system\_wrapper)
- Constraints (1)
  - base.xdc (target)
- Simulation Sources (1)



Version: 1.0 (Rev. 2)  
 Interfaces: AXI4  
 Description: My new AXI IP  
 Status: Pre-Production  
 License: Included  
 Change Log: [View Change Log](#)  
 Vendor: user.org  
 VLN: user.org:user:Ship\_GPIO

4 errors 2 critical warnings 17 warnings 132 infos 245 statuses Show All

| [Synth 8-448] named port connection 'GPIO4' does not exist for instance 'Ship\_GPIO\_v1\_0\_S00\_AXI\_inst' of module 'Ship\_GPIO\_v1\_0\_S00\_AXI' [Ship\_GPIO\_v1\_0.v:57]

| [Synth 8-285] failed synthesizing module 'Ship\_GPIO\_v1\_0' [Ship\_GPIO\_v1\_0.v:4] (more like this)

```

37   output wire [1 : 0] s00_axi_bresp,
38   output wire s00_axi_bvalid,
39   input wire s00_axi_bready,
40   input wire [C_S00_AXI_ADDR_WIDTH-1 : 0] s00_axi_araddr,
41   input wire [2 : 0] s00_axi_arprot,
42   input wire s00_axi_arvalid,
43   output wire s00_axi_arready,
44   output wire [C_S00_AXI_DATA_WIDTH-1 : 0] s00_axi_rdata,
45   output wire [1 : 0] s00_axi_rresp,
46   output wire s00_axi_rvalid,
47   input wire s00_axi_ready
48 );
49 // Instantiation of Axi Bus Interface S00_AXI
50 Ship_GPIO_v1_0_S00_AXI #(
51   .C_S_AXI_DATA_WIDTH(C_S00_AXI_DATA_WIDTH),
52   .C_S_AXI_ADDR_WIDTH(C_S00_AXI_ADDR_WIDTH)
53 ) Ship_GPIO_v1_0_S00_AXI_inst (
54   .GPIO1(GPIO1),
55   .GPIO2(GPIO2),
56   .GPIO3(GPIO3),
57   .GPIO4(GPIO4),
58   .S_AXI_ACLK(s00_axi_aclk),
59   .S_AXI_ARESETN(s00_axi_aresetn),
60   .S_AXI_AWADDR(s00_axi_awaddr),
61   .S_AXI_AWPROT(s00_axi_awprot),
62   .S_AXI_AWVALID(s00_axi_awvalid),
63   .S_AXI_AWREADY(s00_axi_awready),
64   .S_AXI_WDATA(s00_axi_wdata),
65   .S_AXI_WSTRB(s00_axi_wstrb),
66   .S_AXI_WVALID(s00_axi_wvalid),
67   .S_AXI_WREADY(s00_axi_wready),
68   .S_AXI_BRESP(s00_axi_bresp),
69   .S_AXI_BVALID(s00_axi_bvalid),
70   .S_AXI_BREADY(s00_axi_bready),
71   .S_AXI_ARADDR(s00_axi_araddr),
72   .S_AXI_ARPROT(s00_axi_arprot),
73   .S_AXI_ARVALID(s00_axi_arvalid),
74   .S_AXI_ARREADY(s00_axi_arready),
75   .S_AXI_RDATA(s00_axi_rdata),
76   .S_AXI_RRESP(s00_axi_rrresp),
77   .S_AXI_RVALID(s00_axi_rvalid),

```

File Edit Flow Tools Window Layout View Help

Default Layout

Flow Navigator

**Block Design system**

Sources

Design Sources (1)

- system\_wrapper (system\_wrapper)
  - system (system.b)
  - Constraints (1)
  - base.xdc (target)
- Constraints (1)
- Simulation Sources (1)

Cores Interfaces

Diagram Address Editor IP Catalog base.xdc @ Ship\_GPIO\_v1\_0.v

Name	AXI4	Status	License	VLNV
User Repository (/home/peluz/vivado/koltt-Ship/ip_repo/Ship_GPIO_1.0)				
AXI Peripheral				
Ship_GPIO_v1_0	AXI4	Pre-Production	Included	user.org:user:Ship_GPIO:1.0
Properties...				
IP Settings...				
Add Repository...				
Refresh All Repositories				
Customize ...				
<b>Edit in IP Packer</b>				
Ctrl+E				
User Repository (/home/peluz/vivado/koltt-Ship/ip_repo/Ship_PWM_1.0)				
AXI Peripheral				
Ship_PWM_v1_0	AXI4	Pre-Production	Included	user.org:user:Ship_PWM:1.0
Properties...				
IP Settings...				
Add Repository...				
Refresh All Repositories				
Customize ...				
<b>Edit in IP Packer</b>				
Ctrl+E				
User Repository (/home/peluz/vivado/koltt-Ship/ip_repo/Ship_clk4kHz_v1.0)				
AXI Peripheral				
Ship_clk4kHz_v1_0	AXI4	Pre-Production	Included	user.org:user:Ship_clk4kHz:1.0
Properties...				
IP Settings...				
Add Repository...				
Refresh All Repositories				
Customize ...				
<b>Edit in IP Packer</b>				
Ctrl+E				
Vivado Repository				
Alliance Partners				
Automotive & Industrial				
AXI Infrastructure				
BaselIP				
Basic Elements				
Communication & Networks				
Debug & Verification				
Digital Signal Processing				
Embedded Processing				
FPGA Features and Design				
Math Functions				
Memories & Storage Elements				
Partial Reconfiguration				
SDAccel DSA Infrastructure				
Standard Bus Interfaces				

Hierarchy IP Sources Libraries Sources Design Signals

IP Properties

Version: 1.0 (Rev. 2)  
Interfaces: AXI4  
Description: My new AXI IP  
Status: Pre-Production  
License: Included  
Change Log: View Change Log  
Vendor: user.org  
VLNV: user.org:user:Ship\_GPIO:1.0

Details

Name: Ship\_GPIO\_v1\_0  
Version: 1.0 (Rev. 2)  
Interfaces: AXI4  
Description: My new AXI IP  
Status: Pre-Production  
License: Included  
Vendor: user.org

Messages

4 errors 2 critical warnings 17 warnings 132 infos 245 statuses Show All

Synthesis (4 errors)

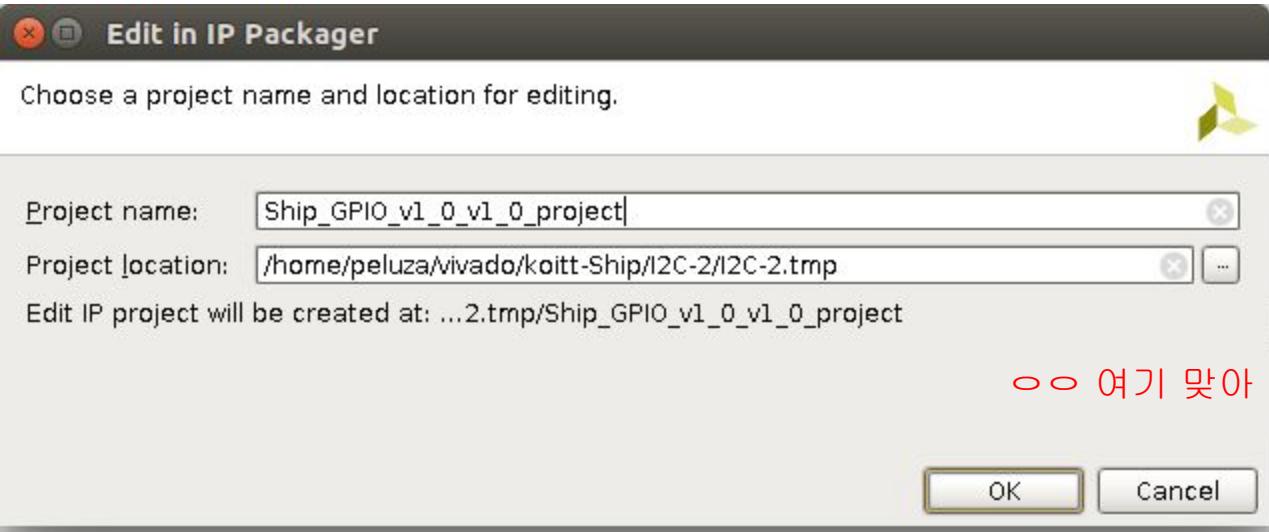
- Out-of-context Module Runs (4 errors)
  - system (4 errors)
    - system\_Ship\_GPIO\_0\_0\_synth\_1 (4 errors)
      - [Synth 8-448] named port connection 'GPIO4' does not exist for instance 'Ship\_GPIO\_v1\_0\_S00\_AXI\_inst' of module 'Ship\_GPIO\_v1\_0\_S00\_AXI' [Ship\_GPIO\_v1\_0.v:57]
      - [Synth 8-285] failed synthesizing module 'Ship\_GPIO\_v1\_0' [Ship\_GPIO\_v1\_0.v:4] (1 more like this)
      - [Common 17-69] Command failed: Synthesis failed - please see the console or run log file for details

Synthesized Design (2 critical warnings)

Tcl Console Messages Log IP Status Reports Design Runs

Un-package and edit IP in a new project

수정하는 방법을 가르쳐 주기 위한 예러였다!



53 ) Ship\_GPIO\_v1\_0\_S00\_AXI\_inst (  
54 .GPIO1(GPIO1),  
55 .GPIO2(GPIO2),  
56 .GPIO3(GPIO3),  
57 .GPIO4(GPIO4),

요기가 에러였네~

53 ) Ship\_GPIO\_v1\_0\_S00\_AXI\_inst ( - - -  
54 .GPIO0(GPIO0),  
55 .GPIO1(GPIO1),  
56 .GPIO2(GPIO2),  
57 .GPIO3(GPIO3),

요렇게

Σ Project Summary × Package IP

- Packaging Steps <<
- ✓ Identification
  - ✓ Compatibility
  - ✓ File Groups
  - Customization Parameters
  - Ports and Interfaces
  - ✓ Addressing and Memory
  - Customization GUI
  - ✓ Review and Package

다시 패키징 진행

Block Design - system

! '/Ship\_GPIO\_0' block in this design should be upgraded. [Show IP Status](#) [Upgrade Later](#)



블록 디자인에 보면 이렇게 IP 상태가  
바뀌었음을 감지하고 '네 상태를 좀 봐라!'라고  
친절히 그렇다면 응당 Show IP Status를

## IP Status - ip\_status

! Report is out of date because the status of one or more IPs have changed. [Rerun](#)

5 Up-to-dates

[Hide All](#)

Source File	IP Status	Recommendation	Change Log	IP Name	Current Version	Recommended Version	License	Current Part	
system (5)									
- /rst_ps7_0_100M	<input type="checkbox"/>	Up-to-date	No changes required	<a href="#">More info</a>	Processor System Reset	5.0 (Rev. 10)	5.0 (Rev. 10)	Included	xc7z010clg400-1
- /Ship_PWM_0	<input type="checkbox"/>	Up-to-date	No changes required	<a href="#">More info</a>	Ship_PWM_v1.0	1.0 (Rev. 14)	1.0 (Rev. 14)	Included	xc7z010clg400-1
- /processing_system7_0	<input type="checkbox"/>	Up-to-date	No changes required	<a href="#">More info</a>	ZYNQ7 Processing System	5.5 (Rev. 3)	5.5 (Rev. 3)	Included	xc7z010clg400-1
- /ps7_0_axi_periph	<input type="checkbox"/>	Up-to-date	No changes required	<a href="#">More info</a>	AXI Interconnect	2.1 (Rev. 12)	2.1 (Rev. 12)	Included	xc7z010clg400-1
- /Ship_GPIO_0	<input type="checkbox"/>	Up-to-date	No changes required	<a href="#">More info</a>	Ship_GPIO_v1.0	1.0 (Rev. 2)	1.0 (Rev. 2)	Included	xc7z010clg400-1

[Upgrade Selected](#)

만약 Show! 했는데 원가 Upgrade selected가  
안된다면!

## IP Status - ip\_status

1 Revision Change

4 Up-to-dates

[Hide All](#)

Source File	IP Status	Recommendation	Change Log	IP Name	Current Version	Recommended Version	License	
system (5)								
- /Ship_GPIO_0	<input checked="" type="checkbox"/>	<a href="#">IP revision change. IP definition 'Ship_GPIO_v1.0 (1.0)' changed on disk</a>	<a href="#">Upgrade IP</a>	Ship_GPIO_v1.0	1.0 (Rev. 2)	1.0 (Rev. 3)	Included	
- /rst_ps7_0_100M	<input type="checkbox"/>	Up-to-date	No changes required	<a href="#">More info</a>	Processor System Reset	5.0 (Rev. 10)	5.0 (Rev. 10)	Included
- /Ship_PWM_0	<input type="checkbox"/>	Up-to-date	No changes required	<a href="#">More info</a>	Ship_PWM_v1.0	1.0 (Rev. 14)	1.0 (Rev. 14)	Included
- /processing_system7_0	<input type="checkbox"/>	Up-to-date	No changes required	<a href="#">More info</a>	ZYNQ7 Processing System	5.5 (Rev. 3)	5.5 (Rev. 3)	Included
- /ps7_0_axi_periph	<input type="checkbox"/>	Up-to-date	No changes required	<a href="#">More info</a>	AXI Interconnect	2.1 (Rev. 12)	2.1 (Rev. 12)	Included

[Upgrade Selected](#)

Rerun 누르면 짜잔! 새로고침 됨.

Generate IP 'ps7\_0\_axi\_periph/s00\_couplers/auto\_pc'...

Cancel

Background

IP 업그레이드 하면 이렇게 Output product가  
자동으로 Generate 된다.

### Generate Output Products



Out-of-context module run was launched for generating output products.  
Cached synthesis data was used for 1 IP. See the Messages window for details

OK

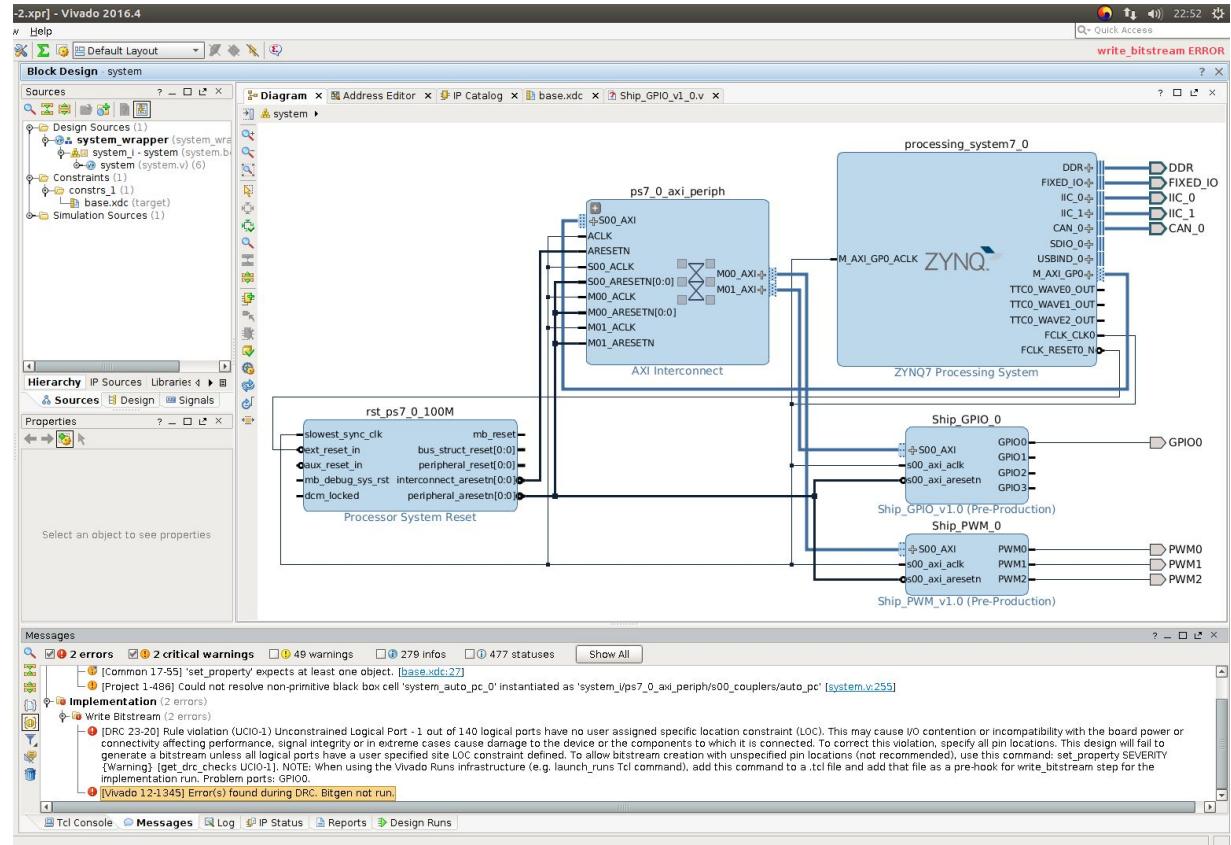
그리고 이렇게 알림이 뜬다.

## Program and Debug

- Bitstream Settings
- Generate Bitstream
- Open Hardware Manager

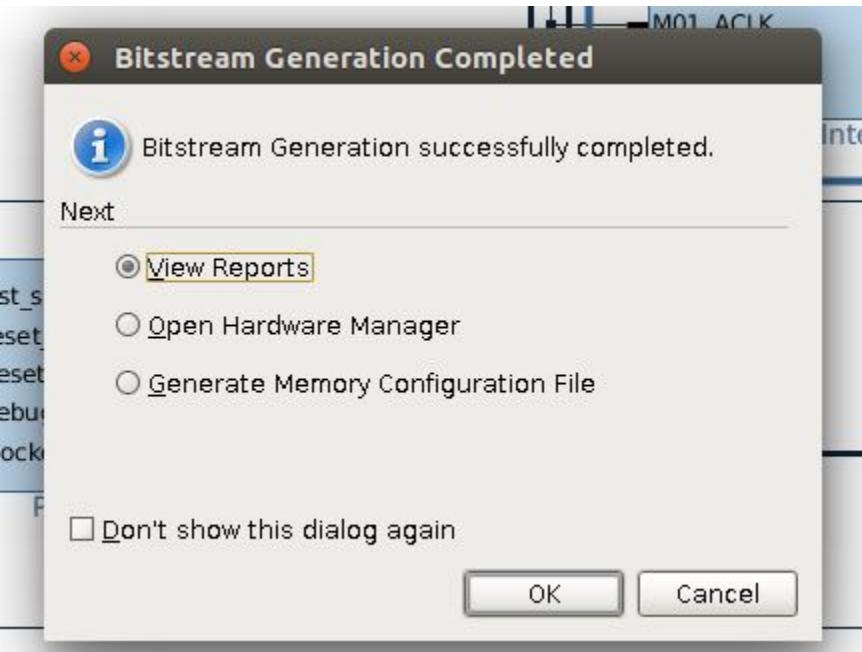
## 다시 한 번 비트스트림 제너레이트!

그런데 또 에러가 났다.

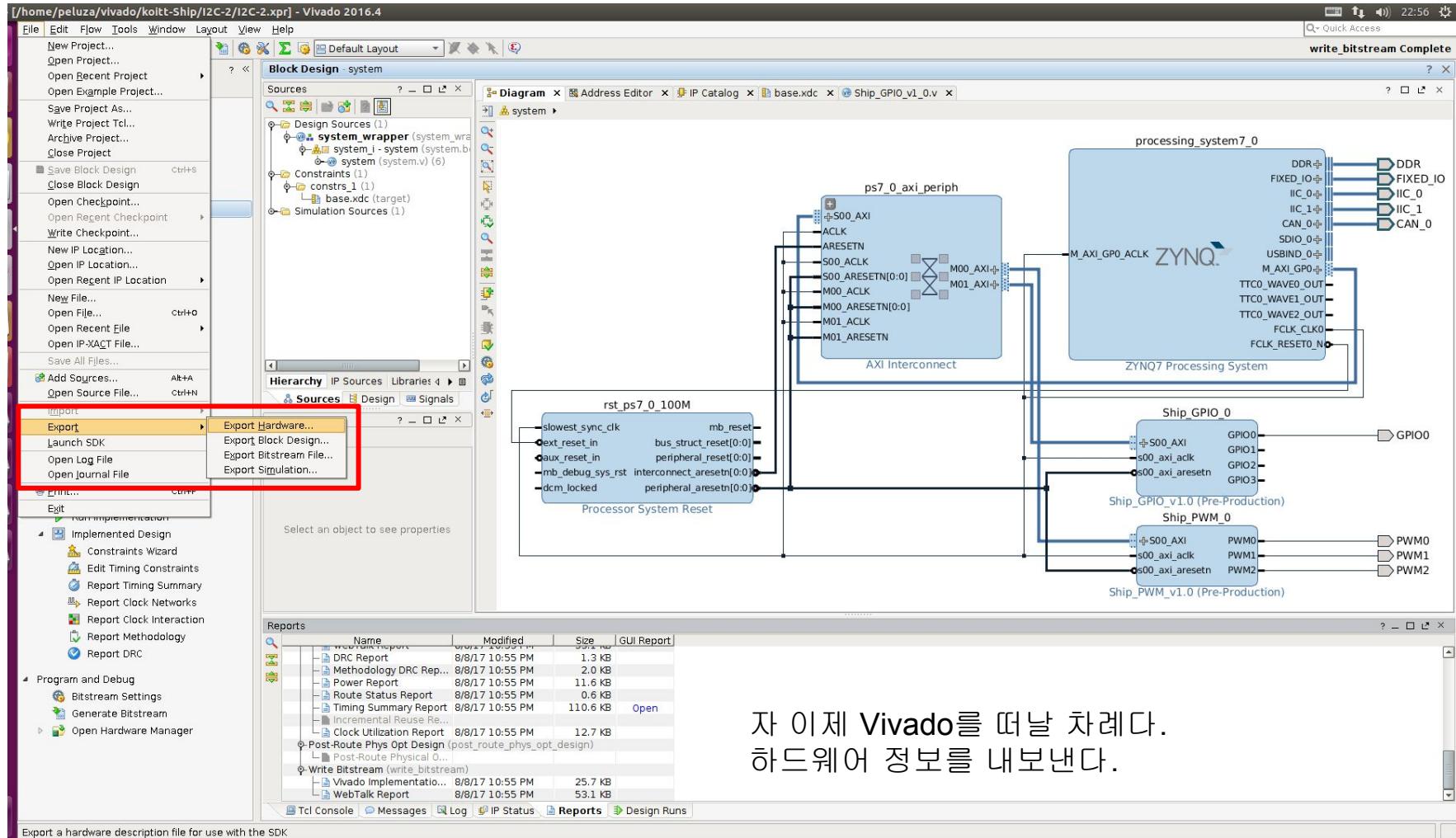


Scalar ports (4)																
↳ <input checked="" type="checkbox"/> GPIO0	OUT		U14	▼	<input checked="" type="checkbox"/>	34 LVCMOS33*	▼	3.300	12	▼	SLOW	▼	NONE	▼	FP_VTT_50	▼
↳ <input checked="" type="checkbox"/> PWM0	OUT		U15	▼	<input checked="" type="checkbox"/>	34 LVCMOS33*	▼	3.300	12	▼	SLOW	▼	NONE	▼	FP_VTT_50	▼
↳ <input checked="" type="checkbox"/> PWM1	OUT		V17	▼	<input checked="" type="checkbox"/>	34 LVCMOS33*	▼	3.300	12	▼	SLOW	▼	NONE	▼	FP_VTT_50	▼
↳ <input checked="" type="checkbox"/> PWM2	OUT		V18	▼	<input checked="" type="checkbox"/>	34 LVCMOS33*	▼	3.300	12	▼	SLOW	▼	NONE	▼	FP_VTT_50	▼

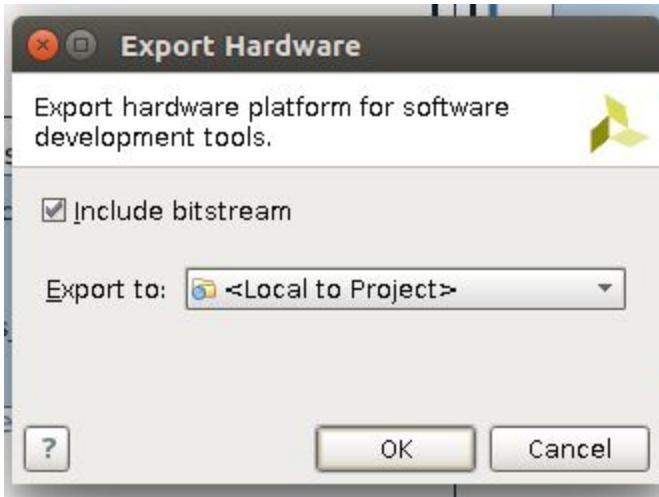
보아하니 제약설정 쪽에서 문제가 있는 고로 바꿔줬다.  
 (여긴 합성 설계 탭에서 I/O planning)



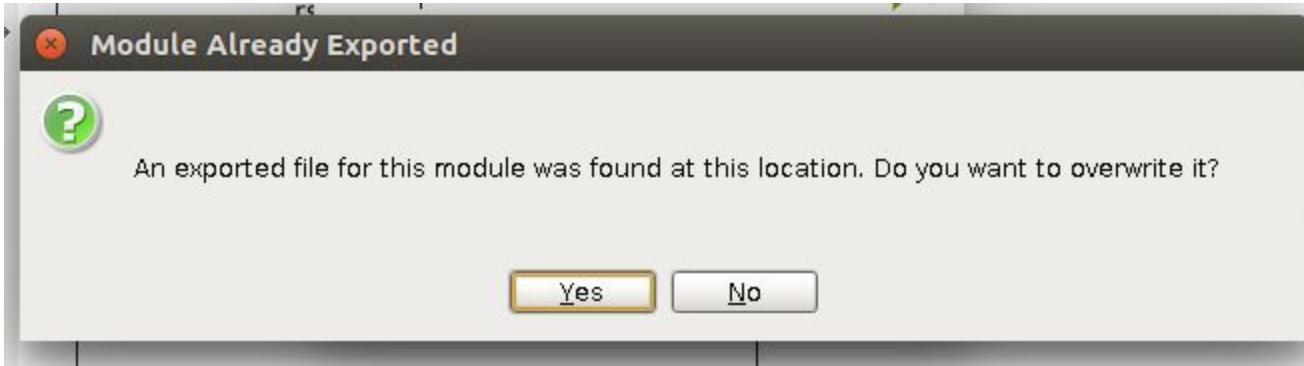
잘 완료 되었다.



자 이제 Vivado를 떠날 차례다.  
하드웨어 정보를 내보낸다.



비트스트림 정보 포함 안 하고 보내는  
똑백이는 없겠죠?



덮어써야 한다면 거리낌 없이!

# Petalinux로 포팅

```
file copy -force /home/peluza/vivado/koitt-Ship/I2C-2/I2C-2.runs/impl_1/system_wrapper.hdf
```

## 내보냈는지 확인

```
peluza@peluza-NH:~/petalinux/i2c-test/images/linux$ petalinux-config --get-hw-description=~/vivado/koitt-Ship/I2C-2/I2C-2.sdk/
INFO: Checking component...
INFO: Getting hardware description...
cp: omitting directory '/home/peluza/vivado/koitt-Ship/I2C-2/I2C-2.sdk/RemoteSystemsTempFiles'
cp: omitting directory '/home/peluza/vivado/koitt-Ship/I2C-2/I2C-2.sdk/system_wrapper_hw_platform_0'
cp: omitting directory '/home/peluza/vivado/koitt-Ship/I2C-2/I2C-2.sdk/webtalk'
INFO: Rename system_wrapper.hdf to system.hdf

***** hsi v2015.4 (64-bit)
**** SW Build 1412921 on Wed Nov 18 09:44:32 MST 2015
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.

source /home/peluza/petalinux/i2c-test/build/linux/hw-description/hw-description.tcl -notrace
INFO: [Common 17-206] Exiting hsi at Tue Aug  8 22:58:24 2017...
INFO: Config linux
[INFO ] oldconfig linux
[INFO ] generate DTS to /home/peluza/petalinux/i2c-test/subsystems/linux/configs/device-tree
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
WARNING: ps7_ethernet_0: No reset found
WARNING: ps7_i2c_0: No reset found
WARNING: ps7_i2c_1: No reset found
WARNING: ps7_usb_0: No reset found
INFO: [Common 17-206] Exiting hsi at Tue Aug  8 22:58:32 2017...
[INFO ] generate BSP for zynq_fsbl
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
INFO: [Common 17-206] Exiting hsi at Tue Aug  8 22:58:44 2017...
INFO: Config linux/kernel
[INFO ] oldconfig linux/kernel
INFO: Config linux/rootfs
[INFO ] oldconfig linux/rootfs
INFO: Config linux/u-boot
[INFO ] generate linux/u-boot configuration files
[INFO ] generate linux/u-boot board header files
INFO: [Hsi 55-1698] elapsed time for repository loading 0 seconds
INFO: [Common 17-206] Exiting hsi at Tue Aug  8 22:58:50 2017...
[INFO ] oldconfig linux/u-boot
```

자, 뭘 망설이는가 사용할 페타리눅스  
프로젝트에서 새로운 하드웨어 디스크립션  
파일을 받아들여라!

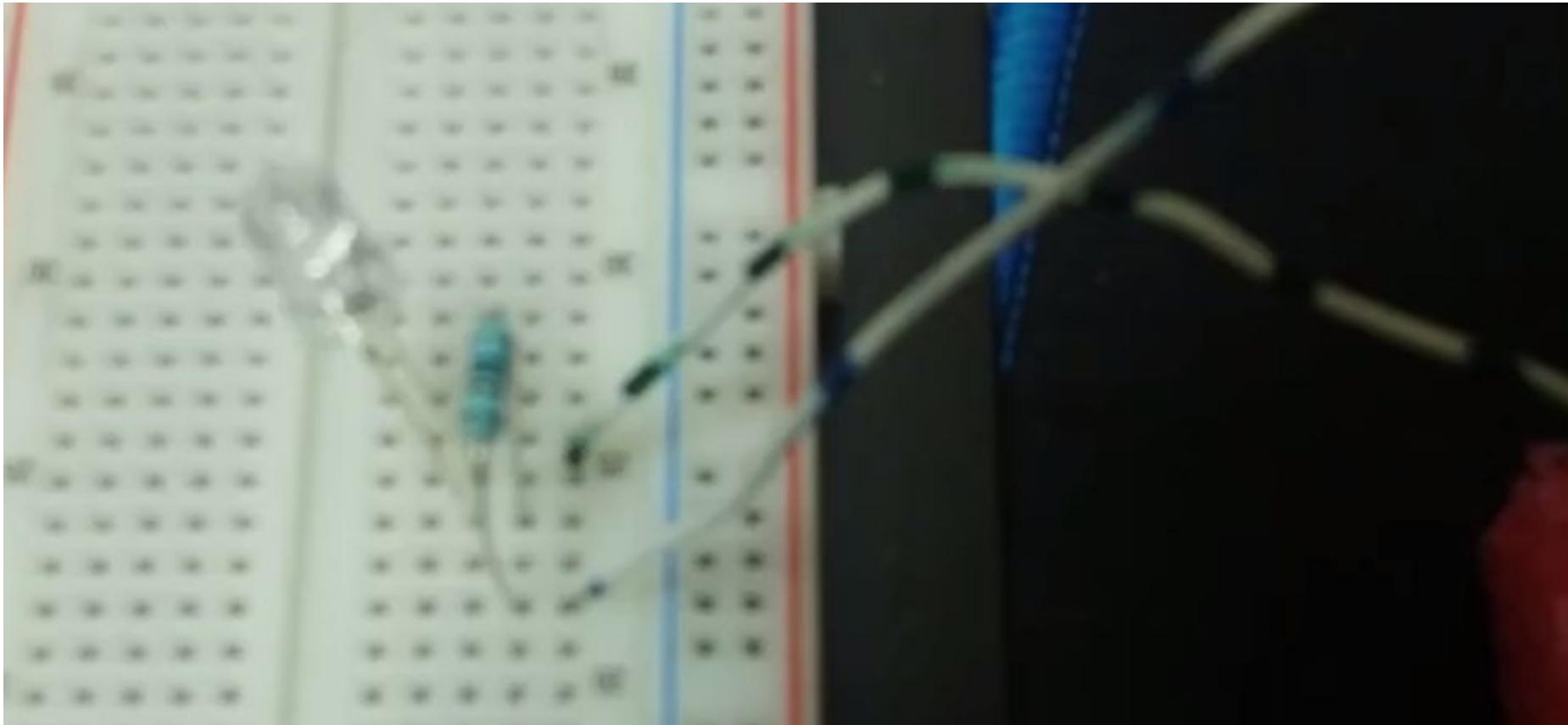
```
peluza@peluza-NH:~/petalinux/i2c-test/images/linux$ petalinux-build
INFO: Checking component...
INFO: Generating make files and build linux
INFO: Generating make files for the subcomponents of linux
INFO: Building linux
[INFO ] pre-build linux/rootfs/can-utils
[INFO ] pre-build linux/rootfs/gpio-dev-mem-test
[INFO ] pre-build linux/rootfs/test_can_receiver_1
[INFO ] pre-build linux/rootfs/test_can_sender_1
[INFO ] build system.dtb
[INFO ] build linux/kernel
[INFO ] generate linux/u-boot configuration files
[INFO ] update linux/u-boot source
[INFO ] build linux/u-boot
[INFO ] build zynq_fslb
[INFO ] build linux/rootfs/can-utils
[INFO ] build linux/rootfs/gpio-dev-mem-test
[INFO ] build linux/rootfs/test_can_receiver_1
[INFO ] build linux/rootfs/test_can_sender_1
[INFO ] build kernel in-tree modules
[INFO ] modules linux/kernel
[INFO ] post-build linux/rootfs/can-utils
[INFO ] post-build linux/rootfs/gpio-dev-mem-test
[INFO ] post-build linux/rootfs/test_can_receiver_1
[INFO ] post-build linux/rootfs/test_can_sender_1
[INFO ] pre-install linux/rootfs/can-utils
[INFO ] pre-install linux/rootfs/gpio-dev-mem-test
[INFO ] pre-install linux/rootfs/test_can_receiver_1
[INFO ] pre-install linux/rootfs/test_can_sender_1
[INFO ] install system.dtb
[INFO ] install linux/kernel
[INFO ] generate linux/u-boot configuration files
[INFO ] update linux/u-boot source
[INFO ] build linux/u-boot
[INFO ] install linux/u-boot
[INFO ] install sys_init
[INFO ] install linux/rootfs/can-utils
[INFO ] install linux/rootfs/gpio-dev-mem-test
[INFO ] install linux/rootfs/test_can_receiver_1
[INFO ] install linux/rootfs/test_can_sender_1
[INFO ] install kernel in-tree modules
[INFO ] modules_install linux/kernel
[INFO ] post-install linux/rootfs/can-utils
[INFO ] post-install linux/rootfs/gpio-dev-mem-test
[INFO ] post-install linux/rootfs/test_can_receiver_1
[INFO ] post-install linux/rootfs/test_can_sender_1
[INFO ] package rootfs.cpio to /home/peluza/petalinux/i2c-test/images/linux
[INFO ] Update and install vmlinux image
[INFO ] vmlinux linux/kernel
[INFO ] install linux/kernel
[INFO ] package zImage
[INFO ] zImage linux/kernel
[INFO ] install linux/kernel
[INFO ] Package HDF bitstream
[INFO ] Failed to copy images to TFTPBOOT /tftpboot
peluza@peluza-NH:~/petalinux/i2c-test/images/linux$
```

커업파일~!

```
peluza@peluza-NH:~/petalinux/i2c-test/images/linux$ petalinux-package --boot --fsbl zynq_fsbl.elf --fpga ./system_wrapper.bit --u-boot --force
INFO: File in BOOT BIN: "/home/peluza/petalinux/i2c-test/images/linux/zynq_fsbl.elf"
INFO: File in BOOT BIN: "/home/peluza/petalinux/i2c-test/images/linux/system_wrapper.bit"
INFO: File in BOOT BIN: "/home/peluza/petalinux/i2c-test/images/linux/u-boot.elf"
INFO: Generating zynq binary package BOOT.BIN...
INFO: Binary is ready.
WARNING: Unable to access the TFTPBOOT folder /tftpboot!!!
WARNING: Skip file copy to TFTPBOOT folder!!!
```

컴파일로 탄생한 새 파일들로 이미지 파일을 최신화합니다.

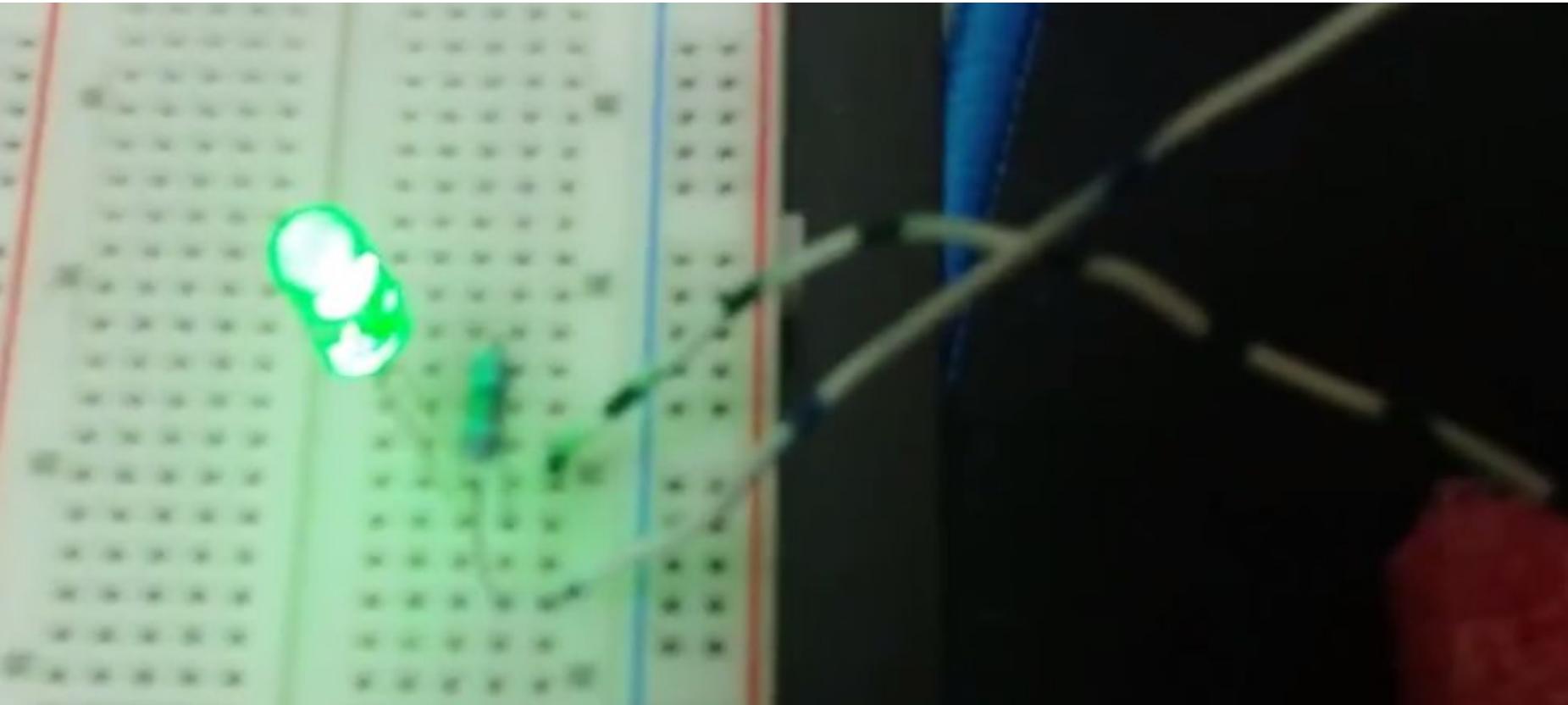
구동 테스트



꺼졌는데.

```
Built with Petalinux v2015.4 (Yocto 1.8) peluza /dev/ttyPS0
peluza login: root
login[894]: root login on 'ttyPS0'
root@peluza:-# gpio-dev-nen-test -g 0x43c10000 -i
GPIO access through /dev/nen.
gpio dev-nen test: input: 00000000
root@peluza:-# gpio-dev-nen-test -g 0x43c10000 -o 1
GPIO access through /dev/nen.
root@peluza:-# gpio-dev-nen-test -g 0x43c10000 -o 0
GPIO access through /dev/nen.
root@peluza:-# gpio-dev-nen-test -g 0x43c10000 -o 1
GPIO access through /dev/nen.
root@peluza:-#
```

레지스터 쓰니까.



켜졌다.

**PS**

전술기의 닦달로 구현 1시간 문서화 **50분**의 시간이 날아갔습니다.  
아아

**PS2** 오랫만에 열일