Building Generic Bus Properties

Gisselquist Technology, LLC

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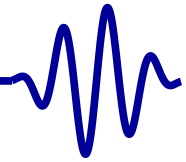
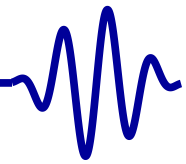


Bus Properties

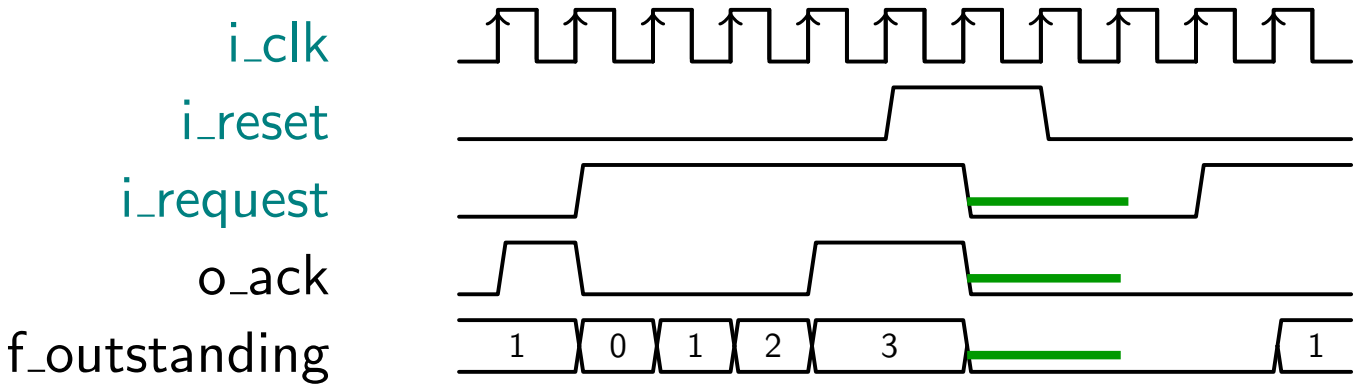
Four Properties



1. Everything gets cleared following a reset
2. Whenever the bus is stalled, the request doesn't change
3. There should be no acknowledgments without a prior request
4. All requests should (eventually) get a response

1. Reset

1. Everything gets cleared following a reset




```
assert property (@(posedge i_clk)
      i_reset |=> !o_ack);
```

1. Reset

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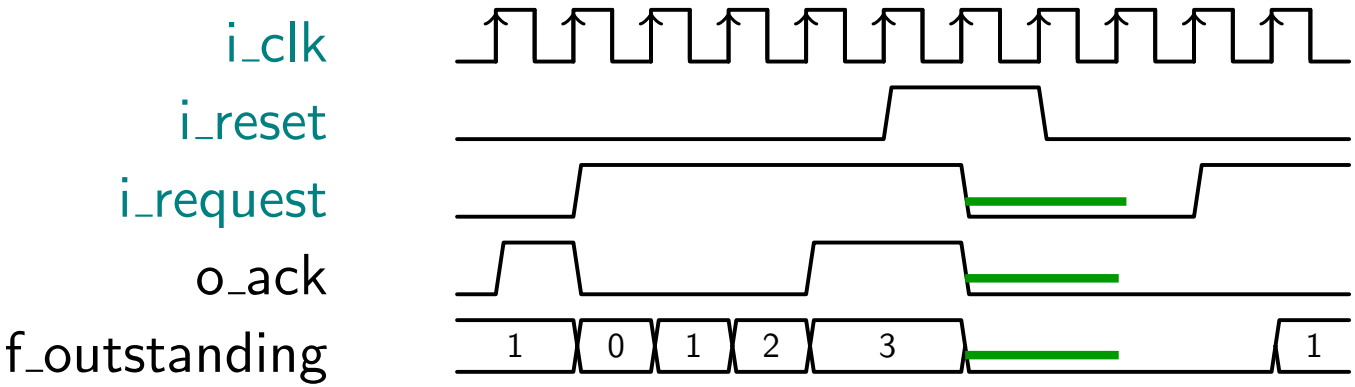
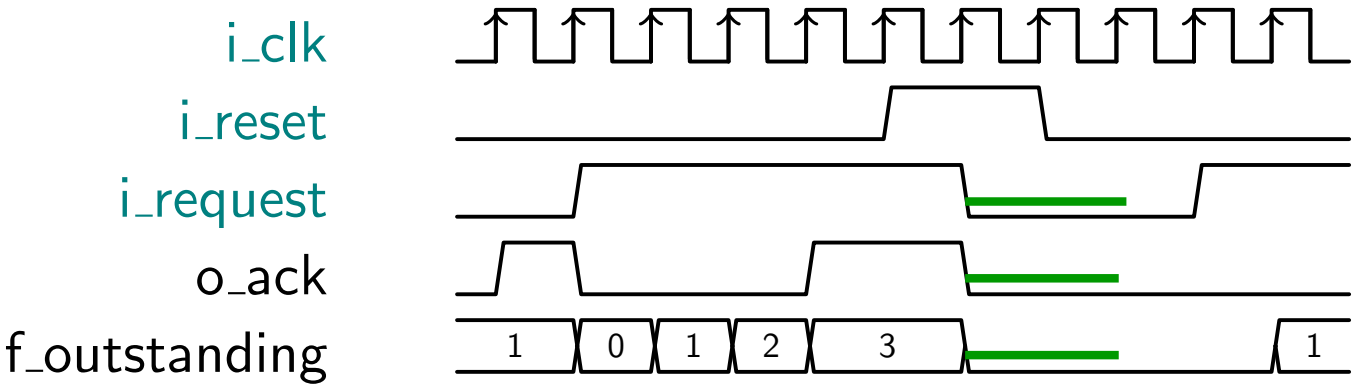



```
assert property (@(posedge i_clk)
      i_reset |=> !o_ack);
```

```
assume property (@(posedge i_clk)
      i_reset |=> !i_request);
```

1. Reset

1. Everything gets cleared following a reset



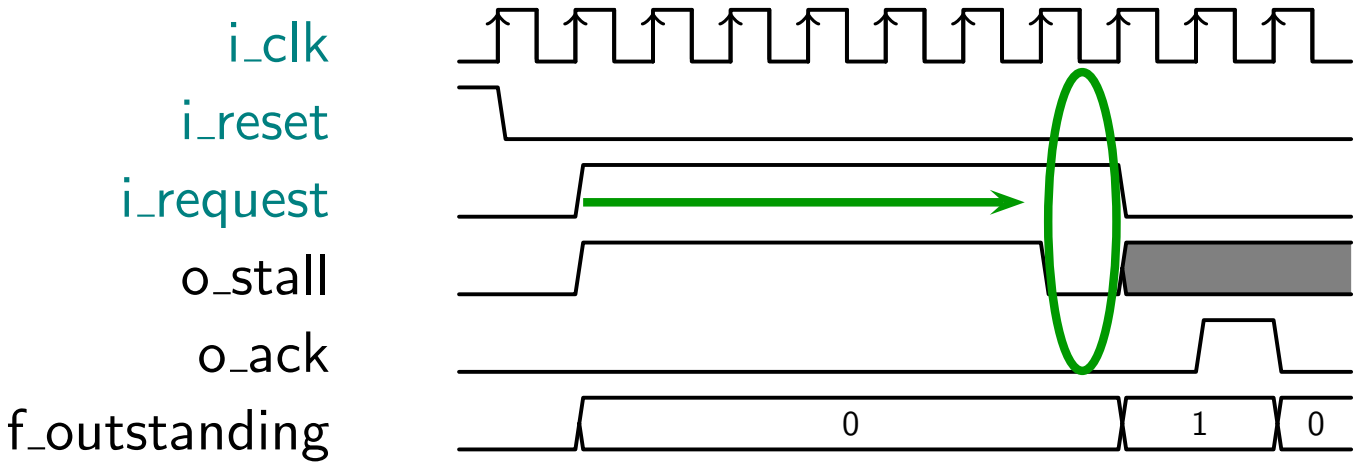

```
assert property (@(posedge i_clk)
      i_reset |=> !o_ack);
```

```
assume property (@(posedge i_clk)
      i_reset |=> !i_request);
```

```
assert property (@(posedge i_clk)
      i_reset |=> (f_outstanding == 0));
```

2. Stalls

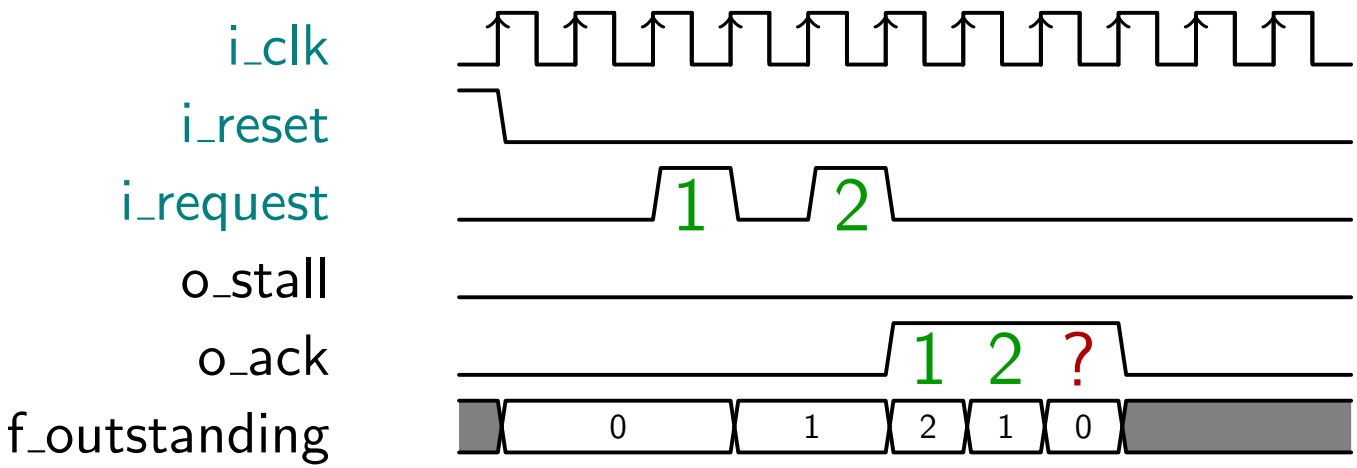
2. Whenever the bus is stalled, the request doesn't change




```
assert property (@(posedge i_clk)
        i_request && o_stall && (!i_reset)
        |=> i_request && $stable(request_details));
```

3. Extra Acks

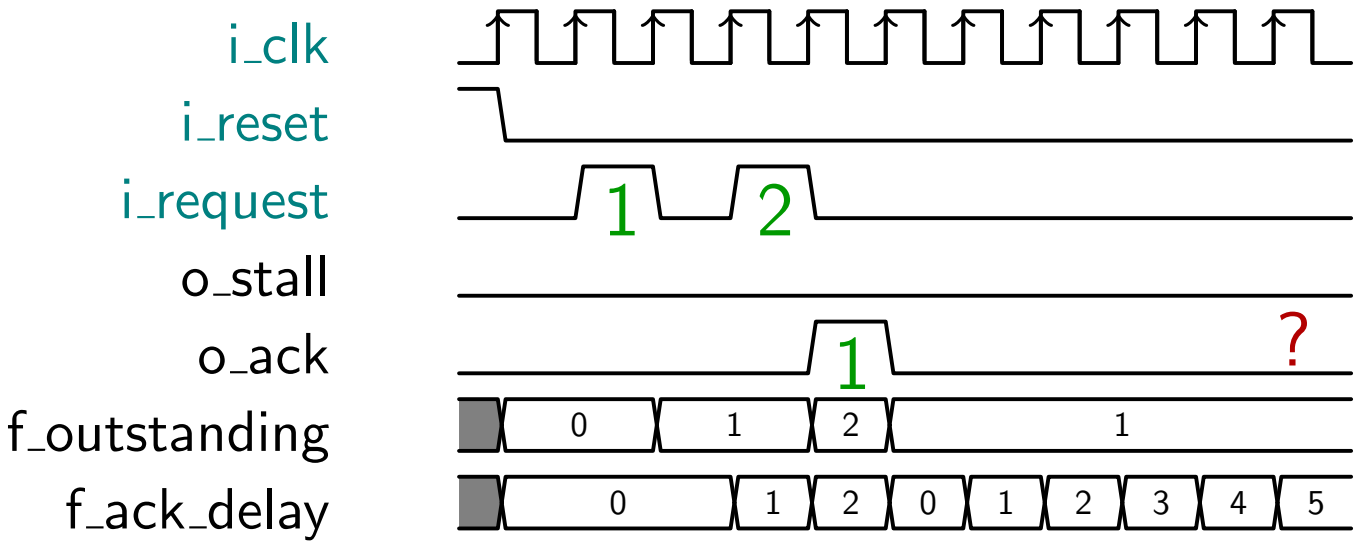
3. There should be no acknowledgments without a prior request



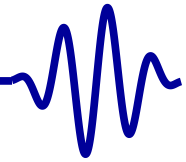

```
assert property (@(posedge i_clk)
        (f_outstanding == 0)
        |-> !o_ack);
```

4. No Lockups

4. All requests should (eventually) get a response




```
assert property (@(posedge i_clk)
        (f_outstanding > 0)&&(!o_ack)
        |-> (f_ack_delay < MAXIMUM_DELAY));
```



AXI Properties

AXI Signals

Global Signals	Write Address	Write Data	Write Return	Read Address	Read Return
ACLK ARESETN	AWVALID AWREADY	WVALID WREADY	BVALID BREADY	ARVALID ARREADY	RVALID RREADY
	AWADDR AWPROT	WDATA WSTRB	BRESP	ARADDR ARPROT	RRESP RDATA
	AWID AWLEN AWSIZE AWBURST AWLOCK AWCACHE	WLAST	BID	ARID ARLEN ARSIZE ARBURST ARLOCK ARCACHE	RID RLAST
	AWQOS			ARQOS	
	AWUSER	WUSER	BUSER	ARUSER	RUSER

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ACLK	AWVALID	WVALID	BVALID	ARVALID	RVALID
ARESETN	AWREADY	WREADY	BREADY	ARREADY	RREADY
	AWADDR	WDATA	BRESP	ARADDR	RRESP
	AWPROT	WSTRB		ARPROT	RDATA
					RID
					RLAST
	AWSIZE			ARSIZE	
	AWBURST			ARBURST	
	AWLOCK			ARLOCK	
	AWCACHE			ARCACHE	
	AWQOS			ARQOS	
	AWUSER	WUSER	BUSER	ARUSER	RUSER

AXI-lite doesn't quite require so many

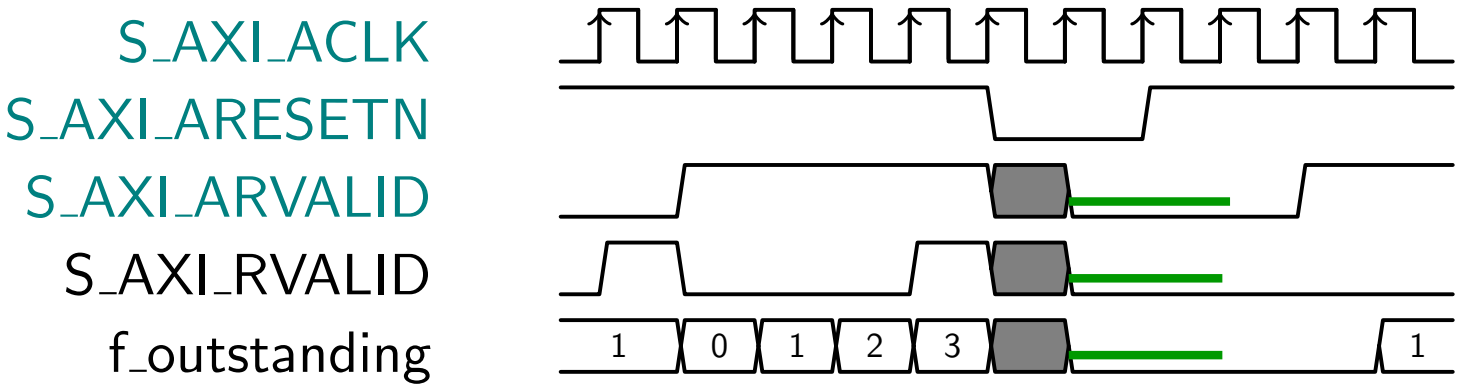
AXI Signals

Global Signals	Write Address	Write Data	Write Return	Read Address	Read Return
ACLK	AWVALID	WVALID	BVALID	ARVALID	RVALID
ARESETN	AWREADY	WREADY	BREADY	ARREADY	RREADY
	AWADDR	WDATA	BRESP	ARADDR	RRESP
	AWPROT	WSTRB		ARPROT	RDATA
	AWID		BID	ARID	RID
	AWLEN	WLAST		ARLEN	RLAST
				ARSIZE	
				ARBURST	
				ARLOCK	
	AWCACHE			ARCACHE	
	AWQOS			ARQOS	
	AWUSER	WUSER	BUSER	ARUSER	RUSER

We'll focus on the read channels for today's presentation

1. Reset

1. Everything gets cleared following a reset



How might you write the properties to describe this?

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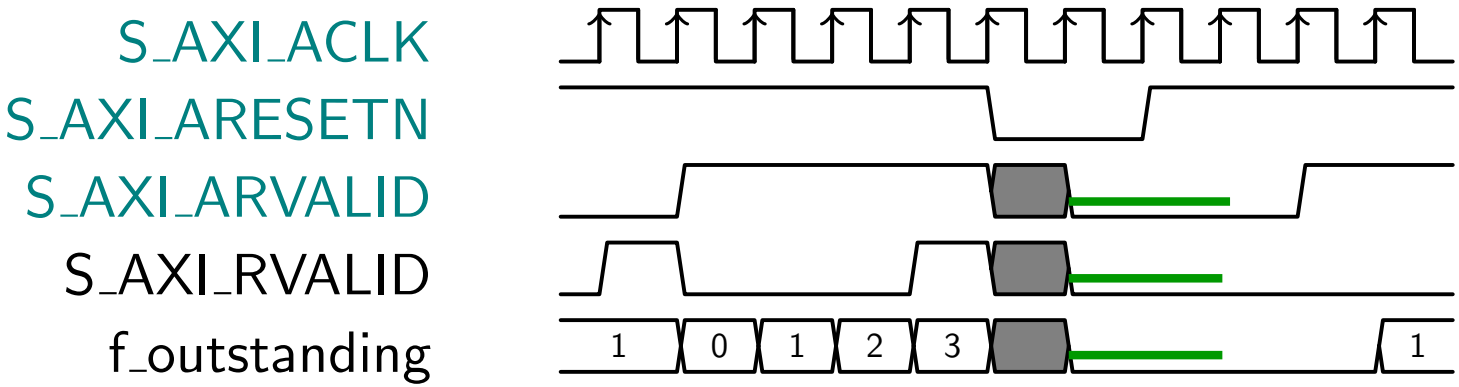


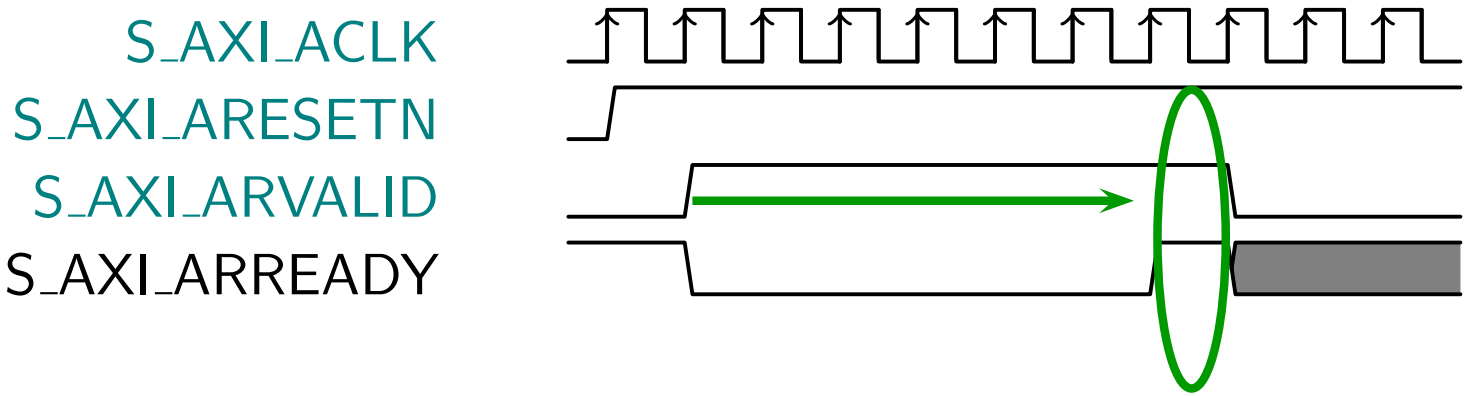
How might you write the properties to describe this?

```
// The slave assume master signals
assume property (@(posedge i_clk)
        !S_AXI_ARESETN |=> !S_AXI_ARVALID);

// Asserts its own outputs
assert property (@(posedge i_clk)
        !S_AXI_ARESETN |=> !S_AXI_RVALID);
```

2. Stalls

2. Whenever the bus is stalled, the request doesn't change



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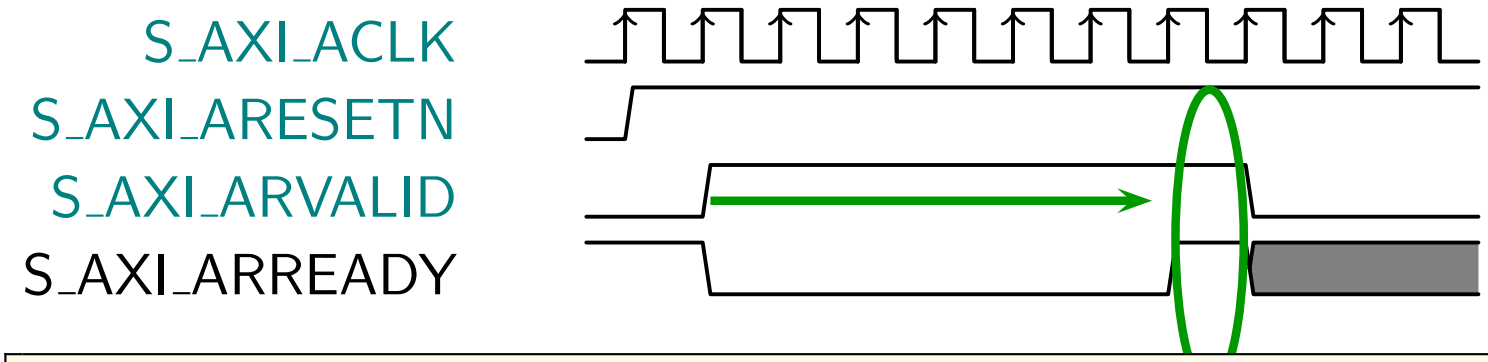
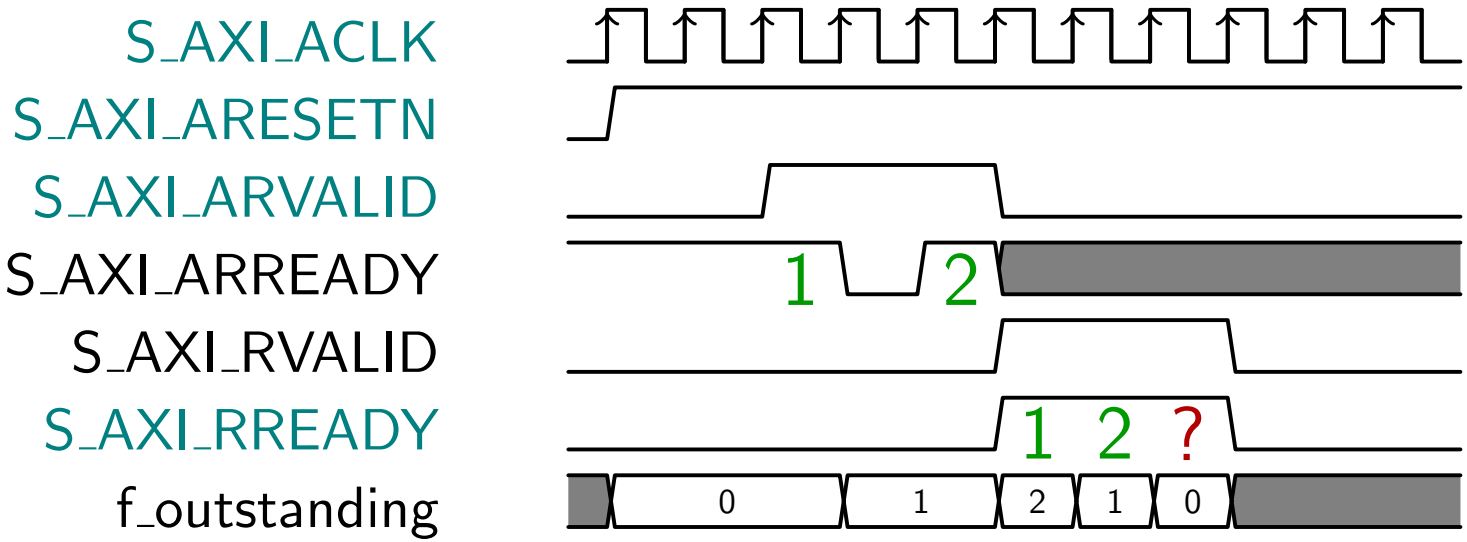



```
assume property (@(posedge i_clk)
        (S_AXI_ARESETN)
        && S_AXI_ARVALID && !S_AXI_ARREADY
        |=> S_AXI_ARVALID && $stable(S_AXI_ARADDR));

assert property (@(posedge i_clk)
        (S_AXI_ARESETN)
        && S_AXI_RVALID && !S_AXI_RREADY
        |=> S_AXI_RVALID && $stable(S_AXI_RDATA));
```

3. Extra Acks

3. There should be no acknowledgments without a prior request



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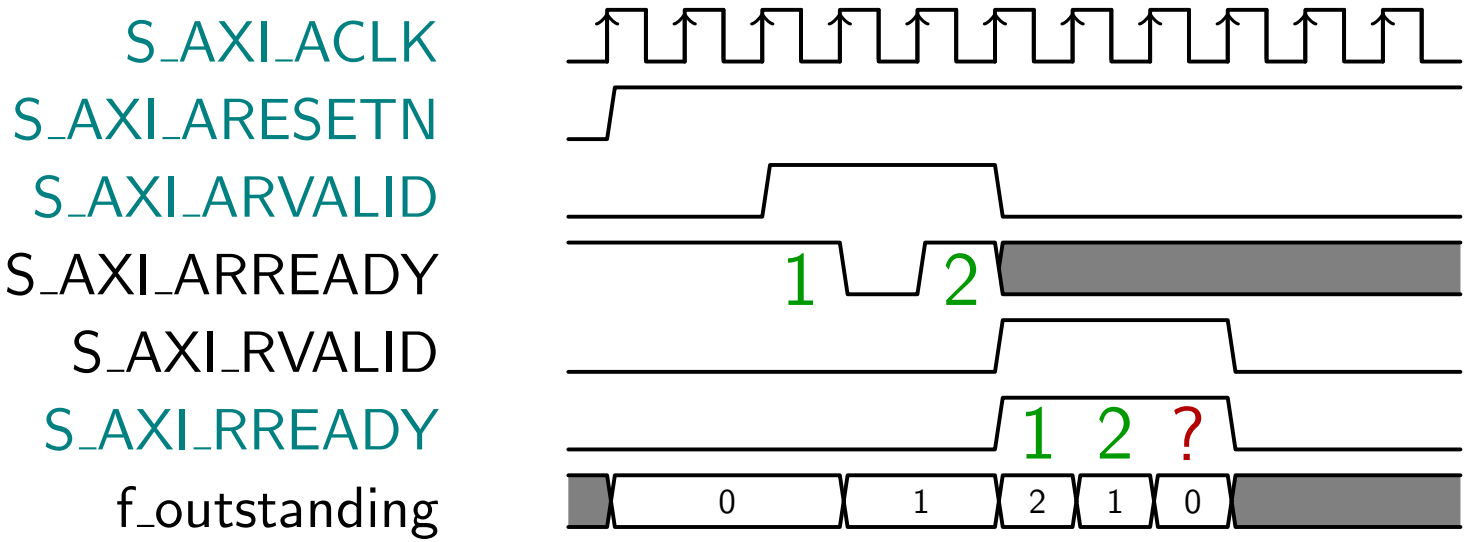
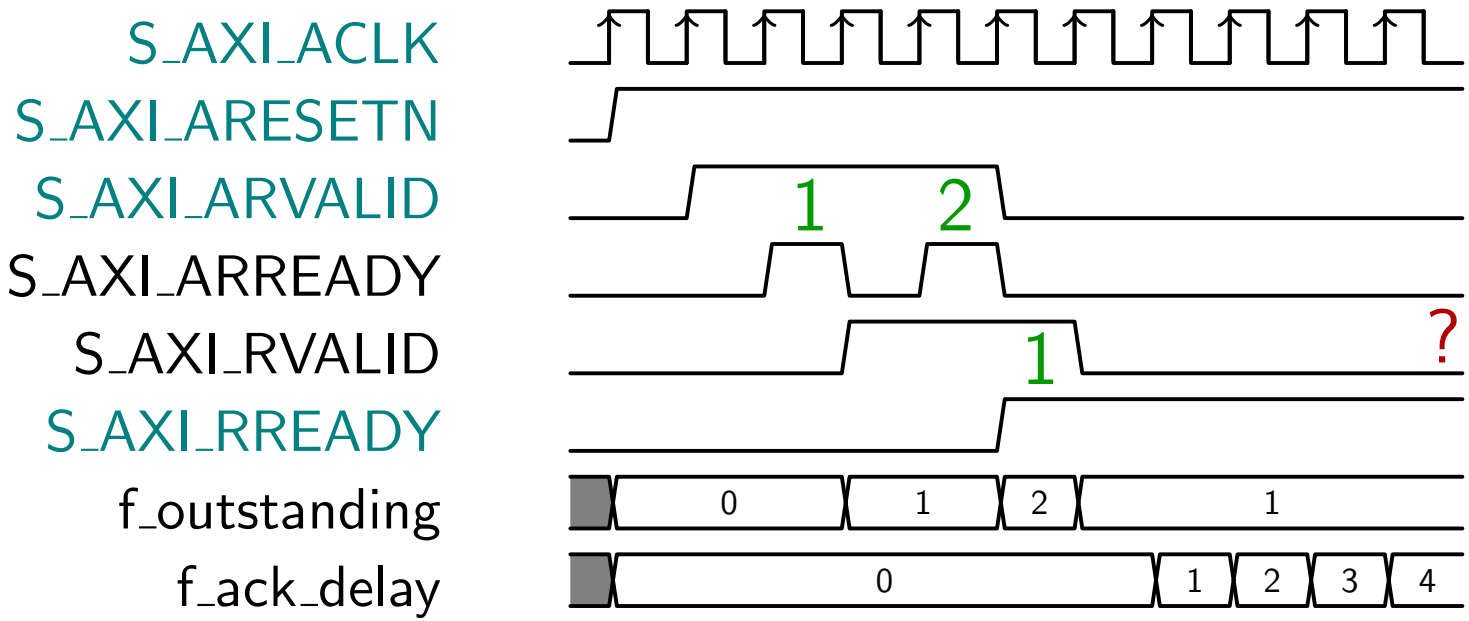



```
assert property (@(posedge i_clk)
        (f_outstanding == 0)
        |-> !S_AXI_RVALID);
```

4. No Lockups

4. All requests should (eventually) get a response



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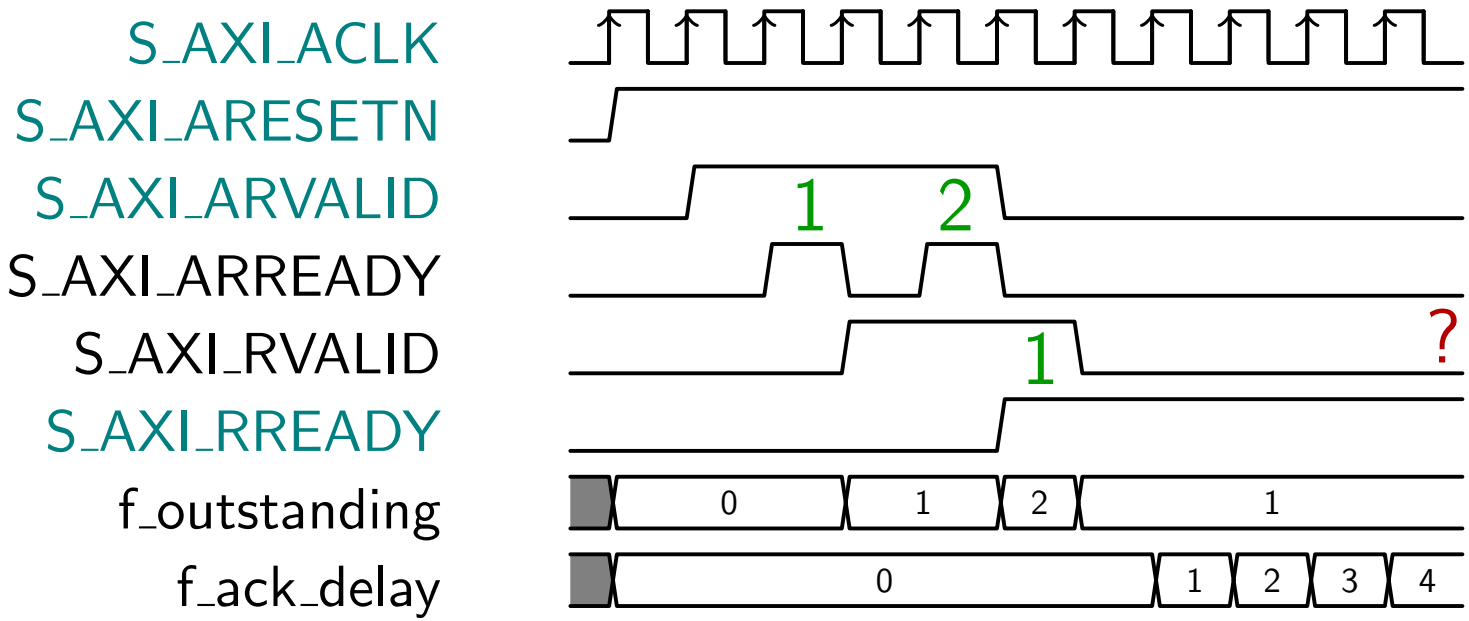


```
assert property (@(posedge i_clk)
      (f_outstanding > 0)&&(!S_AXI_RVALID)
      |-> (f_ack_delay < MAXIMUM_DELAY));
```