

Computer Architecture Experiment

Topic 1. Pipelined CPU supporting RISC-V RV32I Instructions

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Outline



- Experiment Purpose
- Experiment Task
- Basic Principle
- Operating Procedures
- Checkpoints



Experiment Purpose



- Understand RISC-V RV32I instructions
- Master the design methods of pipelined CPU executing RV32I instructions
- Master the method of Pipeline Forwarding Detection and bypass unit design
- Master the methods of 1-cycle stall of Predict-not-taken branch design
- master methods of program verification of Pipelined CPU executing RV32I instructions



Experiment Task



- Design of Pipelined CPU executing RV32I instructions.
 - Design datapath
 - Design Bypass Unit
 - Design CPU Controller

Verify the Pipelined CPU with program and observe the execution of program





31 30 25	24 21	20	19	15 14 12	2 11 8	7	6 0	
funct7	rs2		rs1	funct3	rd	l	opcode	R-type
imm[11	:0]		rs1	funct3	rd	l	opcode	I-type
4 000000000	1-2-5			yr 111 x 110		ryonan.		
imm[11:5]	rs2		rs1	funct3	imm[4:0]	opcode	S-type
imm[12] imm[10:5]	rs2		rs1	funct3	imm[4:1]	imm[11]	opcode	B-type
	imm[31:12]			rd		opcode	U-type
imm[20] imm[10):1] imi	m[11]	imm	[19:12]	rd	l	opcode	J-type





31	25	24 20	19	15 14 1	2 11 7	0	
		imm[31:12]			rd	0110111	U lui
		imm[31:12]			rd	0010111	U auipc
	imn	n[20 10:1 11 19:	12]		rd	1101111	J jal
	imm[11:0]		rs1	000	rd	1100111	I jalr
	imm[12 10:5]	rs2	rs1	000	imm[4:1 11]	1100011	B beq
	imm[12 10:5]	rs2	rs1	001	imm[4:1 11]	1100011	B bne
	imm[12 10:5]	rs2	rs1	100	imm[4:1 11]	1100011	B blt
	imm[12 10:5]	rs2	rs1	101	imm[4:1 11]	1100011	B bge
	imm[12 10:5]	rs2	rs1	110	imm[4:1 11]	1100011	B bltu
	imm[12 10:5]	rs2	rs1	111	imm[4:1 11]	1100011	B bgeu





31 2	5 24 2	0 19 1	5 14 12	11	7 6 0	_
imm[11:0]	rs1	000	rd	0000011	I lb
imm[11:0]	rs1	001	rd	0000011	I lh
imm[11:0]	rs1	010	rd	0000011	I lw
imm[11:0]	rs1	100	rd	0000011	I lbu
imm[11:0]	rs1	101	rd	0000011	I lhu
imm[11:5]	rs2	rs1	000	imm[4:0]	0100011	S sb
imm[11:5]	rs2	rs1	001	imm[4:0]	0100011	S sh
imm[11:5]	rs2	rs1	010	imm[4:0]	0100011	S sw





31 25	5 24 20	19 1	5 14 12	11 7	6 0	
imm[11:0]	· 	rs1	000	rd	0010011	I addi
imm[11:0]		rs1	010	rd	0010011	I slti
imm[11:0]		rs1	011	rd	0010011	I sltiu
imm[11:0]		rs1	100	rd	0010011	I xori
imm[11:0]		rs1	110	rd	0010011	I ori
imm[11:0]		rs1	111	rd	0010011	I andi
0000000	shamt	rs1	001	rd	0010011	I slli
0000000	shamt	rs1	101	rd	0010011	I srli
0100000	shamt	rs1	101	rd	0010011	I srai



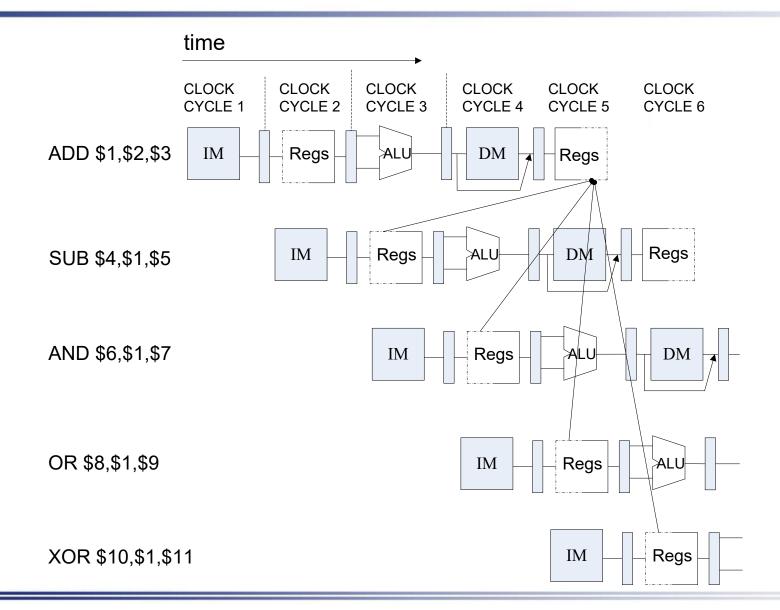
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	4
E S O O O O O O O O O O O O O O O O O O	

31	25 24 20	19 15	14 12	11 7	6 0	ı
0000000	rs2	rs1	000	rd	0110011	R add
0100000	rs2	rs1	000	rd	0110011	R sub
0000000	rs2	rs1	001	rd	0110011	R sll
0000000	rs2	rs1	010	rd	0110011	R slt
0000000	rs2	rs1	011	rd	0110011	Rsltu
0000000	rs2	rs1	100	rd	0110011	R xor
0000000	rs2	rs1	101	rd	0110011	R srl
0100000	rs2	rs1	101	rd	0110011	R sra
0000000	rs2	rs1	110	rd	0110011	R or
0000000	rs2	rs1	111	rd	0110011	R and



Instruction Demo

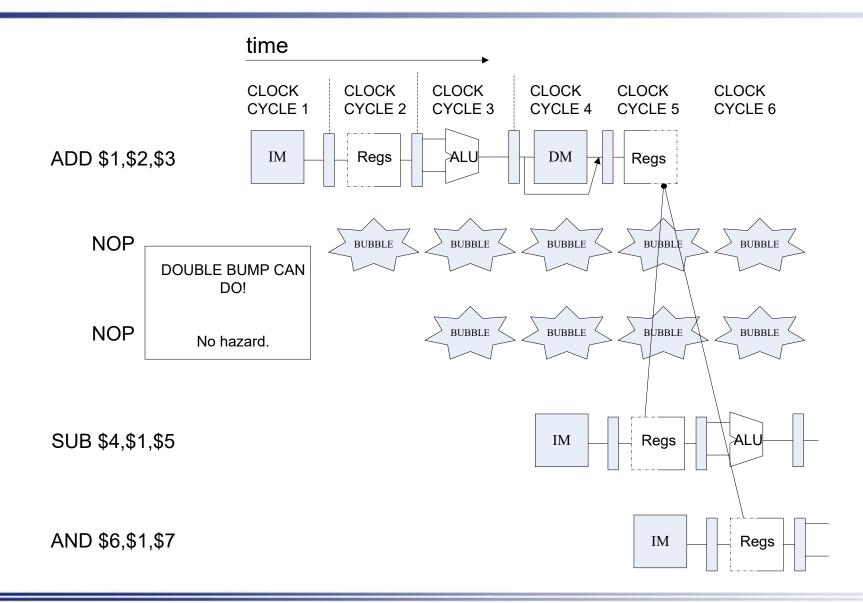






Data Hazard Causes Stalls

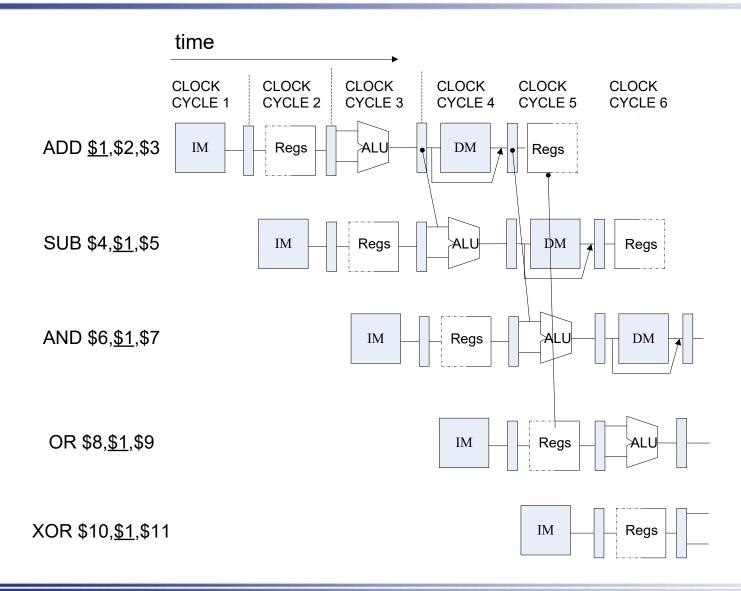








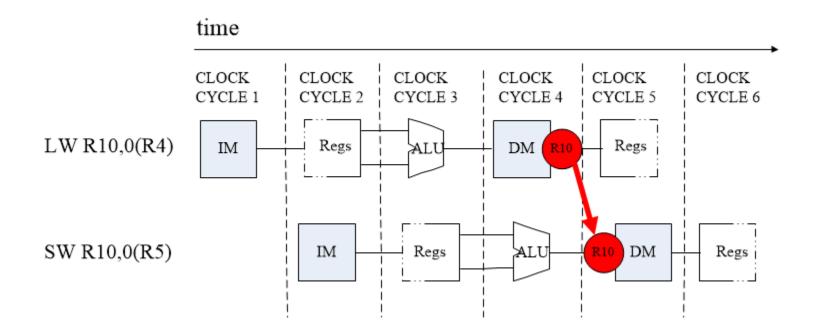






SW After LW

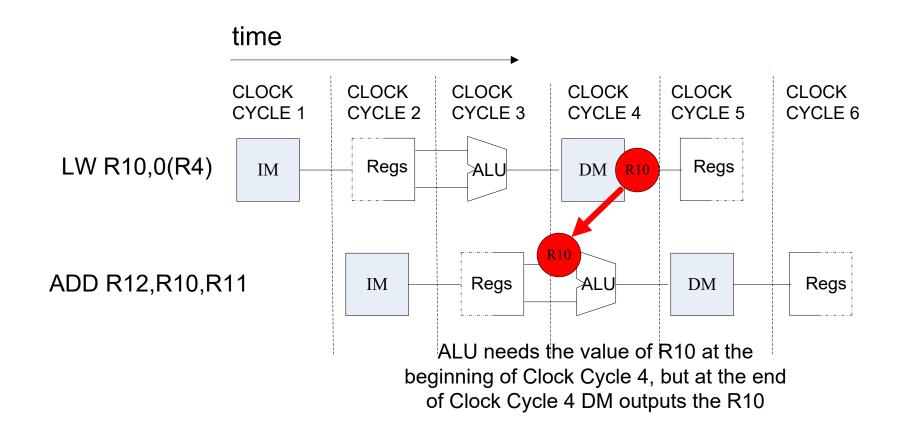








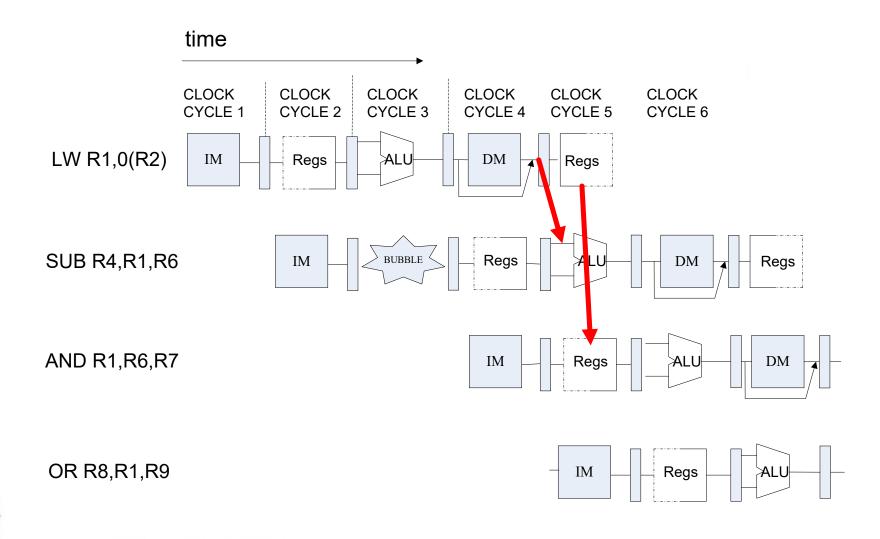
Condition in Which Bypass Unit doesn't work





Pipeline Stalls







Instruction Demo



	Address Instruction				
_		36	Nop		
		40	Add R30,R30,R30		
Branch to 72→		44	Beq R1,R3,24		
		48	And R12,R2,R5		
		52	Or R13,R6,R2		
if R1!=R3, it executes in sequence		56	And R14,R2,R2		
		60			
		64			
		68			
If D1=D2 it executes these		72	Lw R14,50(R7)		
If R1=R3, it executes these instruction		76			



Execution result



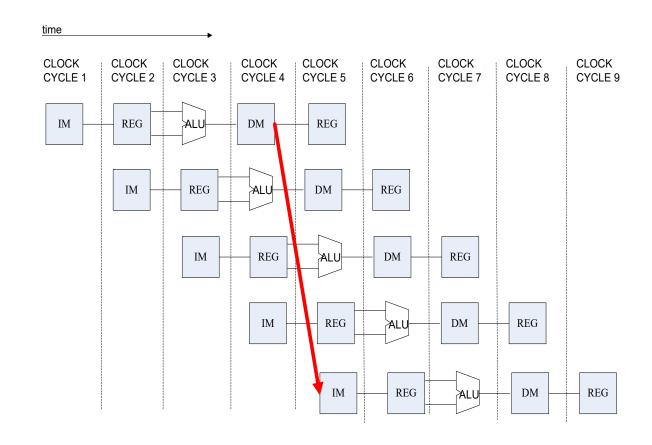
44 BEQ R1,R3,24

48 AND R12,R2,R5

52 OR R13,R6,R2

56 ADD R14,R2,R2

60 OR 72 (DEPENDING ON BRANCH)





Methods of resolving Control hazards



Freeze or flush the pipeline

Predict-not-taken

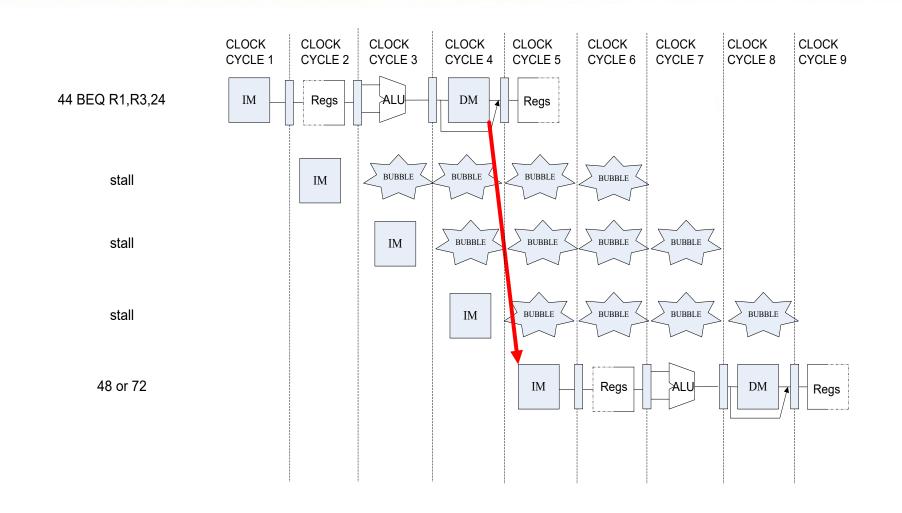
Predict-taken

Delayed branch



Freeze method

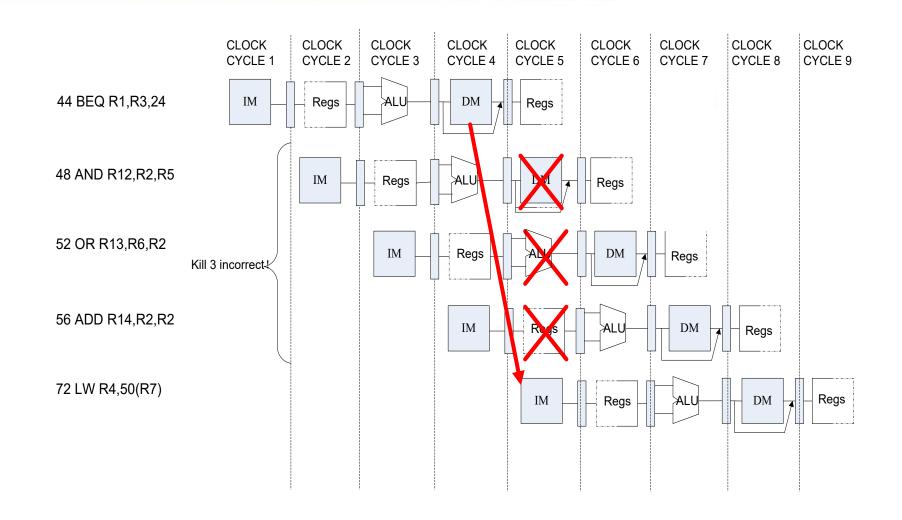














Predict-taken method



- 60% of branch result is taken
- Bring forward calculation of branch condition from MEM
 Stage to EX Stage, stall reduce from 3-cycle to 2-cycle.
- Then bring forward from EX to ID, stall reduce from 2-cycle to 1-cycle.
- 1-cycle stall may be used for 1 delay slot



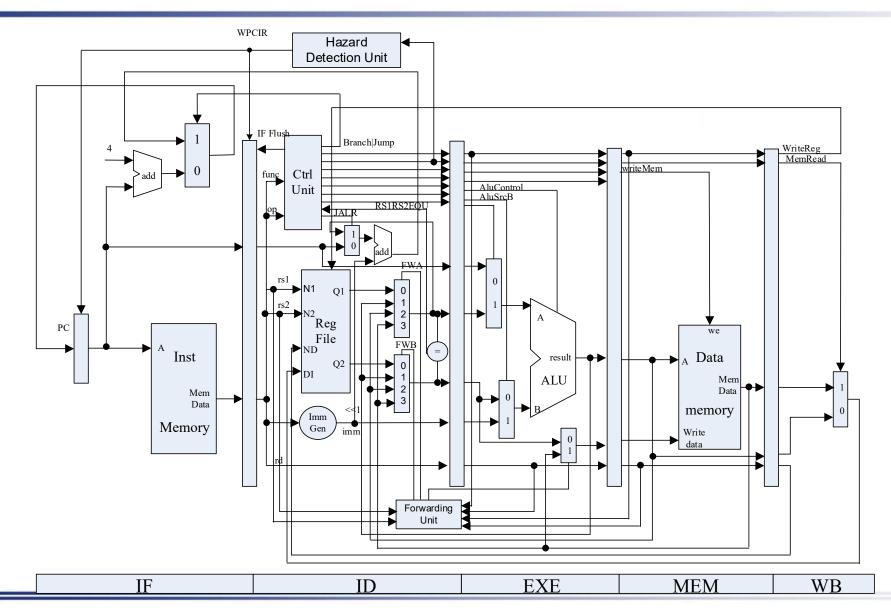




Predict Methods	Status	Original Datapath	Address Calculation Forward	Condition Comparison Forward	
Predict-taken	Hit (Need Branch)	3 stall	1 stall	1 stall	
Predict-taken	Miss (No Branch) 3 stall		3 stall	1 stall	
Predict-not- taken	Hit (No Branch)	go on	go on	go on	
Predict-not- taken	Miss (Need Branch)	3 stall	3 stall	1 stall	

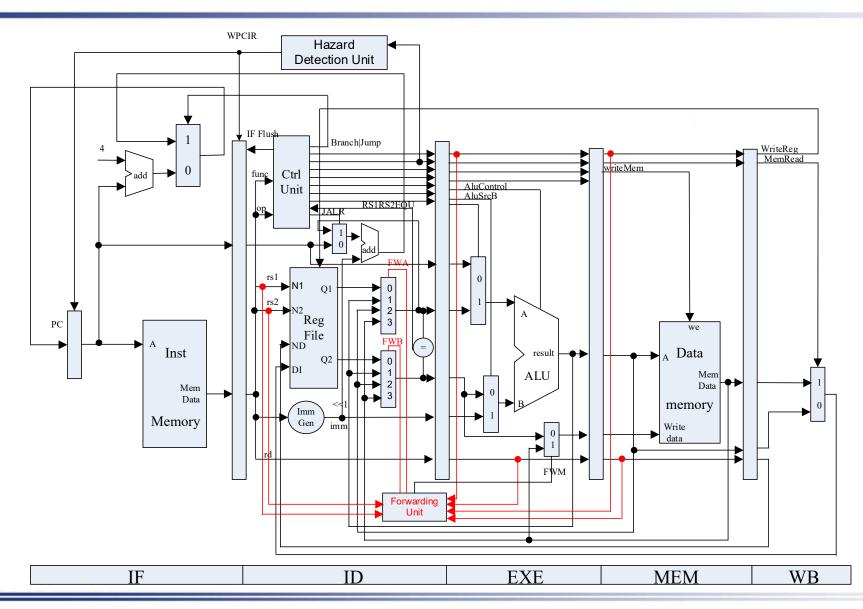






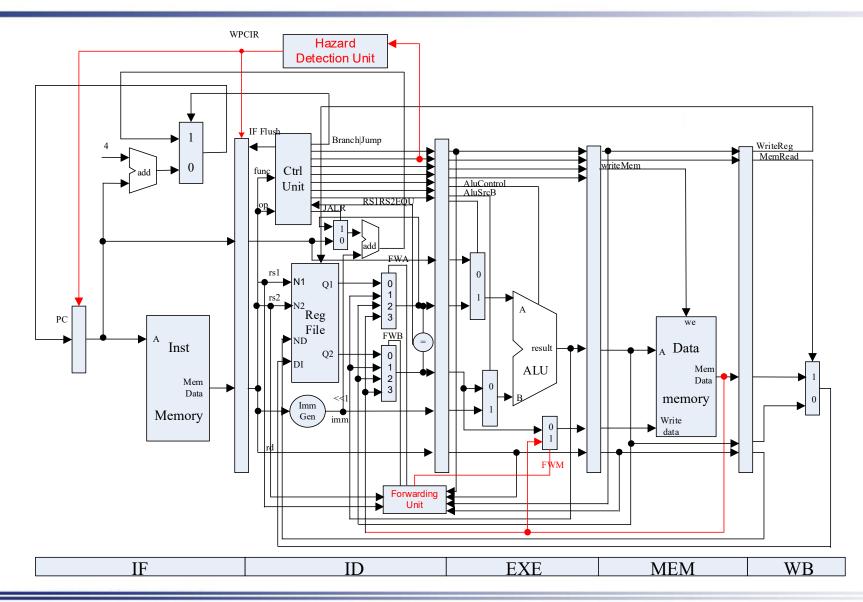






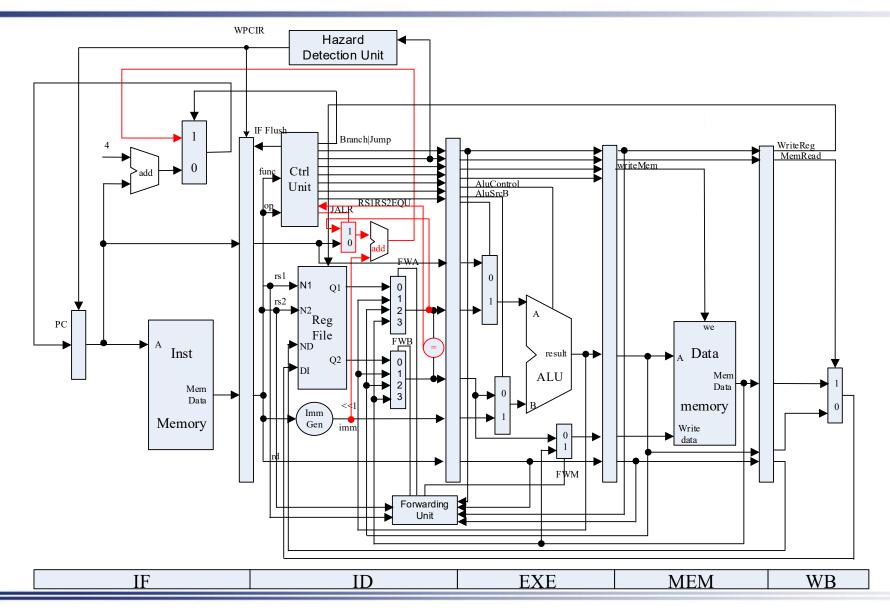
















Instr. Mem.(1)

004120b3

38

14



slt x1,x2,x4







NO.	Instruction	Addr.	Label	ASM	Comment
15	002350b3	3C		srl x1, x6, x2	
16	402350b3	40		sra x1, x6, x2	
17	4023d0b3	44		sra x1, x7, x2	
18	007330b3	48		sltu x1, x6, x7	
19	0063b0b3	4C		sltu x1, x7, x6	
20	00000033	50		add x0,x0,x0	
21	ffd50093	54		addi x1,x10,-3	
22	00f27093	58		andi x1,x4,15	
23	00f26093	5C		ori x1,x4,15	
24	00f24093	60		xori x1,x4,15	
25	00f22093	64		slti x1,x4,15	
26	00121093	68		slli x1,x4,1	
27	00225093	6C		srli x1,x4,2	
28	40c35093	70		srai x1, x6, 12	
29	fff33093	74		sltiu x1, x6, -1	





Instr. Mem.(3)

NO.	Instruction	Addr.	Label	ASM	Comment
30	fff3b093	78		beq x4,x5,label0	
31	00520863	7C		beq x4,x4,label0	
32	00420663	80		addi x0,x0,0	
33	0000013	84		addi x0,x0,0	
34	0000013	88	label0:	bne x4,x4,label1	
35	00421863	8C		bne x4,x5,label1	
36	00521663	90		addi x0,x0,0	
37	0000013	94		addi x0,x0,0	
38	0000013	98	label1:	blt x5,x4,label2	
39	0042c863	9C		blt x4,x5,label2	
40	00524663	A0		addi x0,x0,0	
41	0000013	A4		addi x0,x0,0	
42	0000013	A8	label2:	bltu x6,x7,label3	
43	00736863	AC		bltu x7,x6,label3	
44	0063e663	В0		addi x0,x0,0	







NO.	Instruction	Addr.	Label	ASM	Comment
45	0000013	B4		addi x0,x0,0	
46	0000013	B8	label3:	bge x4,x5,label4	
47	00525863	ВС		bge x5,x4,label4	
48	0042d663	CO		addi x0,x0,0	
49	0000013	C4		addi x0,x0,0	
50	0000013	C8	label4:	bgeu x7,x6,label5	
51	0063f863	CC		bgeu x6,x7,label5	
52	00737663	D0		addi x0,x0,0	
53	0000013	D4		addi x0,x0,0	
54	0000013	D8	label5:	bge x4,x4,label6	
55	00425663	DC		addi x0,x0,0	
56	0000013	EO		addi x0,x0,0	
57	0000013	E4	label6:	lui x1,4	
58	000040b7	E8		jal x1,12	
59	00c000ef	EC		addi x0,x0,0	







NO.	Instruction	Addr.	Label	ASM	Comment
60	0000013	FO		addi x0,x0,0	
61	0000013	F4		lw x8, 24(x0)	
62	01802403	F8		sw x8, 28(x0)	
63	00802e23	FC		lw x1, 28(x0)	
64	01c02083	100		sh x8, 32(x0)	
65	02801023	104		lw x1, 32(x0)	
66	02002083	108		sb x8, 36(x0)	
67	02800223	10C		lw x1, 36(x0)	
68	02402083	110		lh x1, 26(x0)	
69	01a01083	114		lhu x1, 26(x0)	
70	01a05083	118		lb x1, 27(x0)	
71	01b00083	11C		lbu x1, 27(x0)	
72	01b04083	120		auipc x1, 0xffff0	
73	ffff0097	124		jalr x1,0(x0)	
74	000000e7	128			







NO.	Data	Addr.	Comment	NO.	Instruction	Addr.	Comment
0	000080BF	0		16	00000000	40	
1	8000000	4		17	00000000	44	
2	0000010	8		18	00000000	48	
3	0000014	С		19	00000000	4C	
4	FFFF0000	10		20	A3000000	50	
5	0FFF0000	14		21	2700000	54	
6	FF000F0F	18		22	79000000	58	
7	F0F0F0F0	1C		23	15100000	5C	
8	00000000	20		24	00000000	60	
9	00000000	24		25	00000000	64	
10	00000000	28		26	00000000	68	
11	00000000	2C		27	00000000	6C	
12	00000000	30		28	00000000	70	
13	00000000	34		29	00000000	74	
14	00000000	38		30	00000000	78	
15	00000000	3C		31	00000000	7C	

Test Bench



```
RV32core core(
   .debug_en(1'b0),
   .debug_step(1'b0),
   .debug_addr(7'b0),
   .debug_data(),
   .clk(clk),
   .rst(rst),
   .interrupter(1'b0)
initial begin
   clk = 0;
   rst = 1;
   #2 rst = 0;
end
always #1 clk = ^{\sim}clk;
```



Simulation (1)



Name	Value	0 ns 2	, ns	4 ns	6 ns		ıs	10 ns	Livi	12 ns	14 n	<u> </u>	16 ns	18	ns	20 ns		2 ns
¼ dk	0																	
> W PC_IF[31:0]	00000000	00000000	00000	0004 000	80000	00000000	, X	000	00010		00000014	0000	00018	00000010	000	000020	0000000	24 00
> W inst_IF[31:0]	00000013	00000013	00402	2103 008	02203	004100Ъ3	X	fff	08093		00c02283	0100	2303	01402383	400	2200Ъ3	0022701	ьз 📈 00
> W PC_ID[31:0]	00000000	00	000000	000	000004	00000008	X	000	0000c		00000010	0000	00014	00000018	000	00001c	0000002	20 00
> W inst_ID[31:0]	00000000	00000000	00000	0013 004	102103	00802203	X	004	100Ъ3		fff08093	0000	2283	01002303	014	102383	4022001	ьз 00
> ₩ PC_EXE[31:0]	00000000		00000000			00000004		000008	X	00000)00c	0000	00010	00000014	000	000018	000000	10 00
> W inst_EXE[31:0]	00000000	00	000000	X 000	000013	00402103	; X 01	802203	0000	0000	004100ъ3	fff	8093	00:02283	010	002303	0140238	83 40
> ₩ PC_MEM[31:0]	00000000			0000000			X 01	000004	0000	8000		000000c		00000010	000	000014	000000	18 00
> W inst_MEM[31:0]	00000000		00000000			00000013	; X 0:	402103	0080	2203	00000000	004	100Ъ3	fff08093	000	02283	0100230	03 01
> W PC_WB[31:0]	00000000			0000000	0				0000	0004	8000000	X	00000	00c	000	000010	000000	14 00
> W inst_WB[31:0]	00000000			00000000			X 01	0000013	0040	2103	00802203	0000	0000	004100ъ3	ff	08093	0000228	83 01
Branch_ctrl	0																	
JALR	0																\longrightarrow	
RegWrite_ctrl	0																	
mem_w_ctrl	0																	
MIO_ctrl	0																	
ALUSrc_A_ctrl	0																	
ALUSrc_B_ctrl	0																	
□ DatatoReg_ctrl	0																	
¹⊌ rs1use_ctrl	0																	
rs2use_ctrl	0																	
> W hazard_orl[1:0	0	0	X	X	:	2	-x			1		X		2			Х	1
> W ImmSel_ctrl[2:0]	0	0	X		1		=X $=$		0				1				Χ	0
> W cmp_ctrl[2:0]	0								0							_		
> W ALUContrl[3:0]		0	X							1							X 2	Д 3
> V forwardA[1:0]	0			0			X	3	X	0	1	X			0			
> V forwardB[1:0]	0	(0					X	3				0				

Simulation (2)



Name	Value	20 ns	22 ns	24 ns	26 ns	28 ns	30 ns	32 ns	34 ns	36 ns	38 ns	40 ns	42 r
¼ dk	0												
> W PC_IF[31:0]	00000000	00000020	00000024	00000028	0000002c	00000030	00000034	00000038	00000030	00000040	00000044	00000048	0000004c
> W inst_IF[31:0]	00000013	402200ъ3	002270ъ3	002260Ъ3	002240ъ3	002210Ъ3	002220Ъ3	004120ъ3	002350ъ3	402350ъ3	4023d0b3	007330ь3	0063P0P3
> W PC_ID[31:0]	00000000	0000001c	00000020	00000024	00000028	0000002c	00000030	00000034	00000038	0000003e	00000040	00000044	00000048
> W inst_ID[31:0]	00000000	01402383	402200Ъ3	002270ъ3	002260ъ3	002240Ъ3	002210Ъ3	002220ъ3	004120ъ3	002350ъ3	402350ъ3	4023d0b3	007330ъ3
> W PC_EXE[31:0]	00000000	00000018	0000001c	00000020	00000024	00000028	00000020	00000030	00000034	00000038	00000030	00000040	00000044
> W inst_EXE[31:0]	00000000	01002303	01402383	402200Ь3	002270ь3	002260Ь3	002240Ь3	002210ъ3	002220ъ3	004120Ь3	002350ъ3	402350Ь3	402340ъ3
> ₩ PC_MEM[31:0]	00000000	00000014	00000018	0000001c	00000020	00000024	00000028	0000002c	00000030	00000034	00000038	0000003c	00000040
> W inst_MEM[31:0]	00000000	00e02283	01002303	01402383	402200b3	002270Ъ3	002260Ъ3	002240ъ3	002210ъ3	002220Ъ3	004120Ъ3	002350Ъ3	402350ъ3
> W PC_WB[31:0]	00000000	00000010	00000014	00000018	00000010	00000020	00000024	00000028	00000020	00000030	00000034	00000038	0000003c
> W inst_WB[31:0]	00000000	fff08093	00e02283	01002303	01402383	402200b3	002270Ь3	002260ъ3	002240ъ3	002210Ь3	002220Ъ3	004120Ь3	002350ъ3
Branch_ctrl	0								10.00				
JALR	0												
RegWrite_ctrl	0												
mem_w_ctrl	0												
MIO_ctrl	0												
ALUSrc_A_ctrl	0												
ALUSrc_B_ctrl	0												
DatatoReg_ctrl	0												
lars1use_ctrl	0												
lars2use_ctrl	0												
> W hazard_orl[1:	0	2	Χ					1					
> W ImmSel_ctrl[2:0	0 0	1	χ					0					
> W cmp_ctrl[2:0]	0							0					
> W ALUContrl[3:0	0	1	2	Х 3	X 4	X 5	X 6	X	8	χ 7	X	4	9
> W forwardA[1:0]	0							0					
> W forwardB[1:0]	0							0					

Simulation (3)



Name	Value	40	ns l	42 ns	44	ns	46 ns	1 48 ;	ns	50 ns	52 ns	54 ns	. 56 n	s 58 ns	60 ns	62
¼ clk	0															
> W PC_IF[31:0]	00000000	0000004	18	0000004c	00000050	000	00054	00000058	0000	005c X	00000060	00000064	00000068	00000060	00000070	00000074
> W inst_IF[31:0]	00000013	0073301	3	00635053	00000033	ffe	150093	00f27093	00f2	6093	00f24093	00f22093	00121093	00225093	40c35093	fff33093
> W PC_ID[31:0]	00000000	0000004	4	00000048	0000004c	000	00050	00000054	0000	0058 X	0000005c	00000060	00000064	83000000	0000006c	00000070
> W inst_ID[31:0]	00000000	4023401	3	007330Ъ3	0063Ъ0Ъ3	000	00033	ff450093	00f2	7093	00f26093	00f24093	00f22093	00121093	00225093	40c35093
> W PC_EXE[31:0]	00000000	0000004	10	00000044	00000048	000	0004c	00000050	0000	0054	00000058	00000050	00000060	00000064	00000068	00000060
> W inst_EXE[31:0]	00000000	4023501	3	4023d0b3	007330Ь3	000	35053	00000033	ffd5	0093	00f27093	00f26093	00f24093	00f22093	00121093	00225093
> W PC_MEM[31:0]	00000000	0000003	Sc X	00000040	00000044	000	00048	0000004c	0000	0050	00000054	00000058	0000005c	00000060	00000064	00000068
> W inst_MEM[31:0]	00000000	0023501	3	402350b3	402340ь3	007	330Ъ3	00634043	0000	0033	ffd50093	00f27093	00f26093	00f24093	00f22093	00121093
> W PC_WB[31:0]	00000000	0000003	38	0000003e	00000040	000	00044	00000048	0000	004c	00000050	00000054	00000058	00000050	00000060	00000064
> W inst_WB[31:0]	00000000	0041201	3	002350Ъ3	402350ъ3	40:	34023	007330ъ3	0063	ьоьз	00000033	ffd50093	00f27093	00f26093	00f24093	00f22093
Branch_ctrl	0															
JALR	0															
RegWrite_ctrl	0															
mem_w_ctrl	0															
MIO_ctrl	0															
ALUSrc_A_ctrl	0															
ALUSrc_B_ctrl	0															
DatatoReg_ctrl	0						_			0						
ไ₀ rs1use_ctrl	0															
lars2use_ctrl	0															
hazard_orl[1:0	0 0									1						
> W ImmSel_ctrl[2:0	0				0			Х					1			
> W cmp_ctrl[2:0]	0									0						
> W ALUContrl[3:0		a	X_		9	X		1	X	3	4	X 5	8	χ 6	χ_7	X a
> V forwardA[1:0]										0						
> W forwardB[1:0]	0									0						

Simulation (4)



Name	Value	60	ns	62 ns	64 ns	66 ns	68 ns	70 ns	72 ns	74 ns	76 ns	78 ns	80 ns	82
¼ dk	0				1									
> W PC_IF[31:0]	00000000	00000070	000	00074	00000078	00000070	00000080	00000084	00000080	00000090	00000094	00000090	00000040	0000004
> 💗 inst_IF[31:0]	00000013	40e35093	fff	33093	fff3b093	00520863	00420663	00000013	00421863	00521663	00000013	0042c863	00524663	00000013
> W PC_ID[31:0]	00000000	00000066	000	00070	00000074	00000078	0000007c	0000	0080	0000008c	X 000	00090	0000009c	0000000
> 💗 inst_ID[31:0]	00000000	00225093	40c	5093	fff33093	fff3b093	00520863	00420663	00000013	00421863	00521663	00000013	00420863	00524663
> W PC_EXE[31:0]	00000000	00000068	000	0006c	00000070	00000074	00000078	00000070	000	00080	00000080	X 0001	00090	0000009
> W inst_EXE[31:0]	00000000	00121093	002	25093	40c35093	fff33093	fff3b093	00520863	00420663	00000013	00421863	00521663	00000013	00420863
> W PC_MEM[31:0]	00000000	00000064	000	00068	0000006c	00000070	00000074	00000078	0000007c	000	00080	0000008e	0000	0090
> W inst_MEM[31:0]	00000000	00f22093	001	21093	00225093	40c35093	fff33093	fff3b093	00520863	00420663	00000013	00421863	00521663	0000001
> W PC_WB[31:0]	00000000	00000060	000	00064	00000068	00000060	00000070	00000074	00000078	00000070	000	00080	00000080	0000009
> W inst_WB[31:0]	00000000	00f24093	00f	22093	00121093	00225093	40c35093	fff33093	fff3b093	00520863	00420663	00000013	00421863	0052166
Branch_ctrl	0													
JALR	0													
RegWrite_ctrl	0													
mem_w_ctrl	0						0							
MIO_ctrl	0													
ALUSrc_A_ctrl	0													
ALUSrc_B_ctrl	0													
DatatoReg_ctrl	0													
a rs1use_ctrl	0													
lars2use_ctrl	0													
hazard_orl[1:0	0						X	0	X 1	X	0	X	X	0
> W ImmSel_ctrl[2:0	0							2	Ŷ	$\overline{}$	2	<u> </u>	$\langle \rangle$	2
> W cmp_ctrl[2:0]	0)		\langle	1	X .	$\hat{\vee}$	2	X .		3
> W ALUContrl[3:0]	0	7		9	<u></u>	9	\langle	0	Ý i	$\sqrt{}$	0	X i	()—	0
	0		/					<u> </u>				/		
> V forwardB[1:0]	0													

Simulation (5)



Name	Value	80 ns	82 ns	84 ns	86 ns		90 ns	92 ns	94 ns	96 ns	98 ns	100 ns	1 102
¼ clk	0												
> W PC_IF[31:0]	00000000	000000a0	000000a4	000000ac	000000ь0	000000ъ4	000000Ъс	00000000	00000004	00000000	00000040	00000044	000000de
> W inst_IF[31:0]	00000013	00524663	00000013	00736863	0063e663	00000013	00525863	00424663	00000013	0063f863	00737663	00000013	00425663
> W PC_ID[31:0]	00000000	0000009c	00000	00a0	000000ac	0000	0050	000000Ъс	0000	00c0	00000000	0000	0040
> W inst_ID[31:0]	00000000	00420863	00524663	00000013	00736863	0063e663	00000013	00525863	00424663	00000013	0063f863	00737663	00000013
> W PC_EXE[31:0]	00000000	00000090	00000090	0000	00a0	000000ac	0000	0050	000000Ъс	0000	00e0	00000000	00000040
> W inst_EXE[31:0]	00000000	00000013	0042c863	00524663	00000013	00736863	0063e663	00000013	00525863	00424663	00000013	0063f863	00737663
> ₩ PC_MEM[31:0]	00000000	00000	0090	0000009c	00000	00a0	000000ac	0000	0090	000000ъс	0000	0000	000000cc
> W inst_MEM[31:0]	00000000	00521663	00000013	00420863	00524663	00000013	00736863	0063e663	00000013	00525863	00424663	00000013	0063f863
> W PC_WB[31:0]	00000000	0000008c	00000	0090	00000090	0000	00a0	000000ac	0000	000Ъ0	000000ъс	0000	0000
> W inst_WB[31:0]	00000000	00421863	00521663	00000013	0042c863	00524663	00000013	00736863	0063e663	00000013	00525863	00424663	00000013
Branch_ctrl	0												
JALR	0												
RegWrite_ctrl	0												
mem_w_ctrl	0												
MIO_ctrl	0												
ALUSrc_A_ctrl	0												
ALUSrc_B_ctrl	0				L								
DatatoReg_ctrl	0												
¼ rs1use_ctrl	0												
lars2use_ctrl	0												
> 😽 hazard_orl[1:0	0)	1	Χ	0	1	X	0	X 1	Χ	0	1
> 😻 ImmSel_ctrl[2:0	0		2	1	Χ :	2	X i	X	2	X 1	X	2	X 1
> W cmp_ctrl[2:0]	0	(:	3	0	Χ	4	X 0	X	5	χ ο	X	6	χ ο
> W ALUContrl[3:0	0)	1	Χ	0	1	XX	0	X	Χ	0	X 1
> 💗 forwardA[1:0]	0						0						
> 😻 forwardB[1:0]	0						0						

Simulation (6)



Name	Value	100 ns	102 ns	104 ns	106 ns	108 ns	110 ns	112 ns	114 ns	116 ns	118 ns	120 ns	122 ns
¼ dk	0												
> W PC_IF[31:0]	00000000	00000044	00000040	000000e0	000000e8	000000ec	000000f0	000000f8	000000fc	00000100	00000104	00000108	00000100
> W inst_IF[31:0]	00000013	00000013	00425663	00000013	000040ъ7	00c000ef	00000013	01802403	00802e23	01c02083	02801023	02002083	02800223
> W PC_ID[31:0]	00000000	0000	0040	0000	00dc	000000e8	00000	00ec	000000f8	000000fc	00000100	00000104	00000108
> W inst_ID[31:0]	00000000	00737663	00000013	00425663	00000013	000040ъ7	00c000ef	00000013	01802403	00802e23	01c02083	02801023	02002083
> W PC_EXE[31:0]	00000000	00000000	0000	0040	00000	00dc	000000e8	0000	00ec	000000f8	000000fc	00000100	00000104
> W inst_EXE[31:0]	00000000	0063f863	00737663	00000013	00425663	00000013	000040ъ7	00c000ef	00000013	01802403	00802e23	01c02083	02801023
> W PC_MEM[31:0]	00000000	00000000	000000ec	0000	0040	00000	00de	000000e8	00000	00ec	000000f8	000000fc	00000100
> W inst_MEM[31:0]	00000000	00000013	0063f863	00737663	00000013	00425663	00000013	000040ъ7	00c000ef	00000013	01802403	00802e23	01c02083
> W PC_WB[31:0]	00000000	0000	0000	00000000	00000	0040	00000	00dc	000000e8	00000	00ec	000000f8	000000fc
> W inst_WB[31:0]	00000000	00424663	00000013	0063f863	00737663	00000013	00425663	00000013	000040ъ7	00c000ef	00000013	01802403	00802e23
1⊌ Branch_ctrl	0												
18 JALR	0												
I RegWrite_ctrl	0												
le mem_w_ctrl	0									1			
16 MIO_ctrl	0												
ALUSrc_A_ctrl	0												
ALUSrc_B_ctrl	0												
□ DatatoReg_ctrl	0												
lars1use_ctrl	0												
lars2use_ctrl	0						0						
> W hazard_orl[1:0	0	0	1	X 0	(1		2	3	2	3	2
> W ImmSel_ctrl[2:0]	0	2	1	2	1	5	3	χ	1	4	1	4	1
> W cmp_ctrl[2:0]	0	6	V 0	5	(<u> </u>				0				
> W ALUContrl[3:0]	0	0	X i	0	(1	•	Ъ	χ		1			
> 💗 forwardA[1:0]	0						0						
e√> ₩ forwardB[1:0]	0						0						

Simulation (7)



Name	Value	120 ns	122 ns	124 ns	126 ns	128 ns	130 ns	132 ns	134 ns	. 136 ns	138 ns	, 140 ns	142
¼ dk	0		77,77	1000	373, 334	77,77	33,43		313,45	33,43,		7,7,7	
> W PC_IF[31:0]	00000000	00000108	00000100	00000110	00000114	00000118	00000110	00000120	00000124	00000128	00000120	00000000	00000004
> W inst_IF[31:0]	00000013	02002083	02800223	02402083	01a01083	01a05083	01ь00083	01504083	ffff0097	000000e7	хихихих	00000013	00402103
> W PC_ID[31:0]	00000000	00000104	00000108	0000010c	00000110	00000114	00000118	0000011c	00000120	00000124	0000	0128	00000000
> W inst_ID[31:0]	00000000	02801023	02002083	02800223	02402083	01a01083	01a05083	01500083	01504083	ffff0097	000000e7	X 0000	0013
> W PC_EXE[31:0]	00000000	00000100	00000104	00000108	00000100	00000110	00000114	00000118	00000110	00000120	00000124	X 0000	0128
> W inst_EXE[31:0]	00000000	01c02083	02801023	02002083	02800223	02402083	01a01083	01a05083	01ь00083	01504083	ffff0097	000000e7	00000013
> W PC_MEM[31:0]	00000000	000000fc	00000100	00000104	00000108	0000010c	00000110	00000114	00000118	0000011c	00000120	00000124	00000128
> W inst_MEM[31:0]	00000000	00802e23	01002083	02801023	02002083	02800223	02402083	01a01083	01a05083	01500083	01504083	ffff0097	000000e7
> W PC_WB[31:0]	00000000	000000f8	000000fc	00000100	00000104	00000108	00000100	00000110	00000114	00000118	0000011c	00000120	00000124
> W inst_WB[31:0]	00000000	01802403	00802e23	01e02083	02801023	02002083	02800223	02402083	01a01083	01a05083	01500083	01Ъ04083	ffff0097
Branch_ctrl	0												
JALR	0												
RegWrite_ctrl	0												
mem_w_ctrl	0		\Box										
MIO_ctrl	0												
ALUSrc_A_ctrl	0												
ALUSrc_B_ctrl													
□ DatatoReg_ctri	0												
la rs1use_ctrl	0												
I rs2use_ctrl	0												
> W hazard_orl[1:	170	3	2	3	X		2			Χ		1	
> W ImmSel_ctrl[2:0	0 0	4	Xi	4	X		1			5	Χ	1	
> W cmp_ctrl[2:0]	0						0						
> W ALUContrl[3:0						1					Х ь	Χ	1
> 😻 forwardA[1:0]							0						
e. > 💔 forwardB[1:0]	0						0						

Checkpoints



• CP 1:

Waveform Simulation of the Pipelined CPU with the verification program

• CP 2:

FPGA Implementation of the Pipelined CPU with the verification program





Thanksl

