浙江大学
ZHEJIANG UNIVERSITY

Computer Architecture Experiment

Topic 5. Pipelined CPU supporting multi-cycle operations

浙江大学计算机学院

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Outline

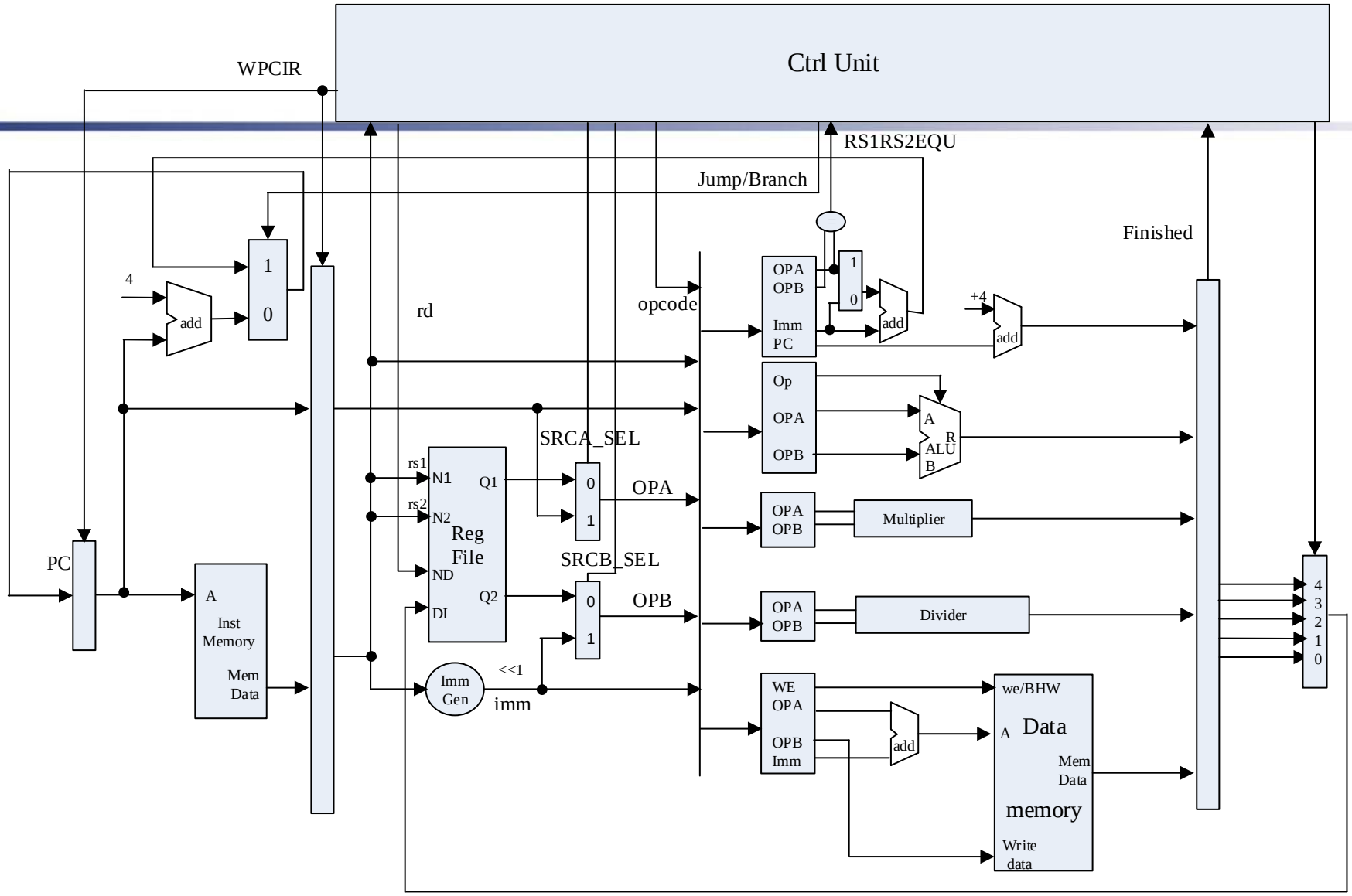
- Experiment Purpose
- Experiment Task
- Basic Principle
- Operating Procedures
- Checkpoints

Experiment Purpose

- **Understand the principle of piplines that support multicycle operations.**
- **Master the design methods of piplines that support multicycle operations.**
- **Master verification methods of pipelined CPU supporting multicycle operations.**

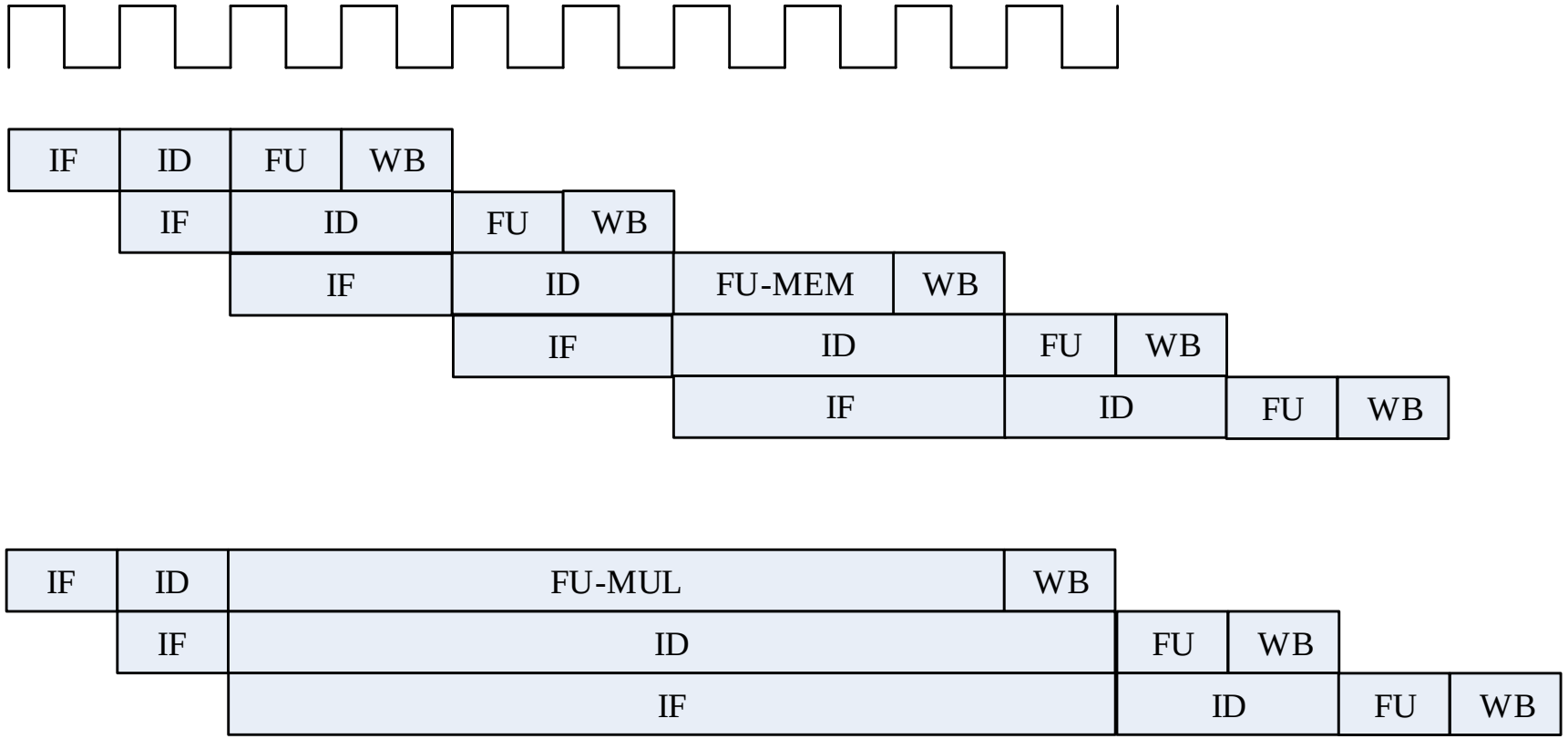
Experiment Task

- **Redesign the pipelines with IF/ID/FU/WB stages and FU stage supporting multicycle operations.**
- **Redesign of CPU Controller.**
- **Verify the Pipelined CPU with program and observe the execution of program.**


Ctrl Unit
WPCIR
RS1RS2EQU
Jump/Branch
Finished
4
add
1
0
rd
opcode
OPA
OPB
Imm
PC
=
+4
Op
ALU
SRCA_SEL
SRCB_SEL
OPA
OPB
rs1
rs2
N1
N2
ND
DI
Q1
Q2
Reg
File
PC
A
Inst
Memory
Mem
Data
Imm
Gen
<<1
imm
Multiplier
Divider
WE
we/BHW
Data
memory
Write
data
4
3
2
1
0

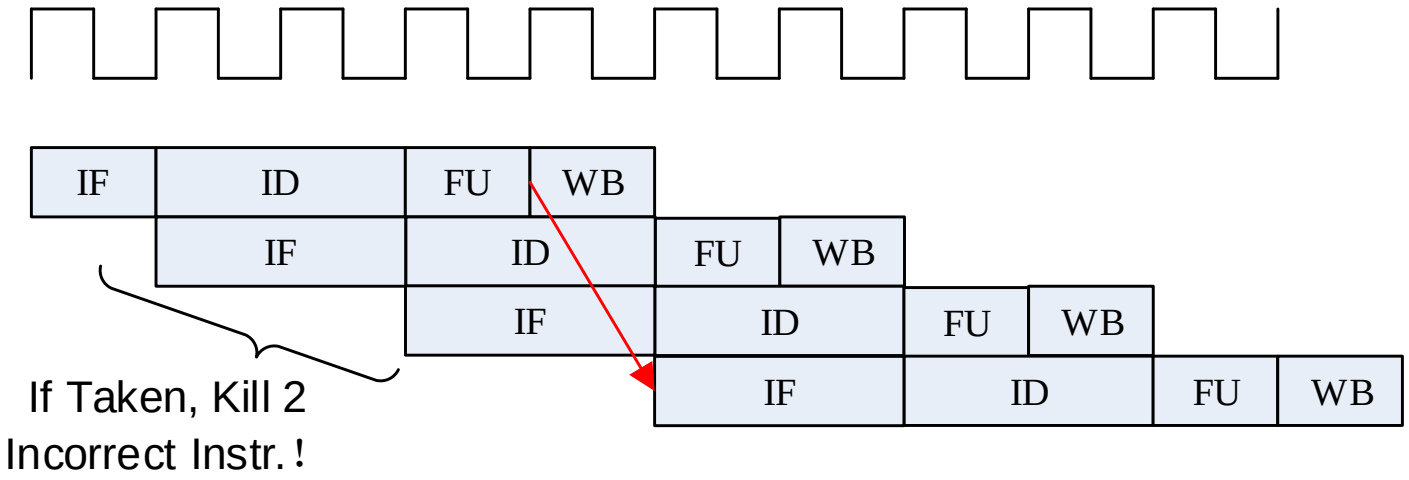
IF	ID	FU	WB

Pipelines resolving Data Hazards



Methods of resolving Control hazards

- **Predict-not-taken**
- **Condition and Addr. Calculation in FU**



Instr. Mem.(1)

NO.	Instruction	Addr.	Label	ASM	Comment
0	00000013	0	__start:	addi x0, x0, 0	
1	00402103	4		lw x2, 4(x0)	
2	00802203	8		lw x4, 8(x0)	
3	004100b3	C		add x1, x2, x4	
4	fff08193	10		addi x3, x1, -1	
5	00c02283	14		lw x5, 12(x0)	
6	01002303	18		lw x6, 16(x0)	
7	01402383	1C		lw x7, 20(x0)	
8	40220433	20		sub x8,x4,x2	
9	ffd50493	24		addi x9,x10,-3	
10	00520c63	28		beq x4,x5,label0	
11	00420a63	2C		beq x4,x4,label0	
12	03000a13	30		addi x20,x0,48	
13	03400a13	34		addi x20,x0,52	
14	03800a13	38		addi x20,x0,56	

Instr. Mem.(2)

NO.	Instruction	Addr.	Label	ASM	Comment
15	03c00a13	3C		addi x20,x0,60	
16	00004537	40	label0:	lui x10,4	
17	014005ef	44		jal x11,20	
18	04800a13	48		addi x20,x0,72	
19	04c00a13	4C		addi x20,x0,76	
20	05000a13	50		addi x20,x0,80	
21	05400a13	54		addi x20,x0,84	
22	ffff0617	58		auipc x12, 0xffff0	
23	0223c6b3	5C		div x13, x7, x2	
24	02520733	60		mul x14, x4, x5	
25	022687b3	64		mul x15, x13, x2	
26	00400813	68		addi x16, x0, 4	
27	000008e7	6C		jalr x17,0(x0)	

Data Mem.

NO.	Data	Addr.	Comment
0	000080BF	0	
1	00000008	4	
2	00000010	8	
3	00000014	C	
4	FFFF0000	10	
5	0FFF0000	14	
6	FF000F0F	18	
7	F0F0F0F0	1C	
8	00000000	20	
9	00000000	24	
10	00000000	28	
11	00000000	2C	
12	00000000	30	
13	00000000	34	
14	00000000	38	
15	00000000	3C	

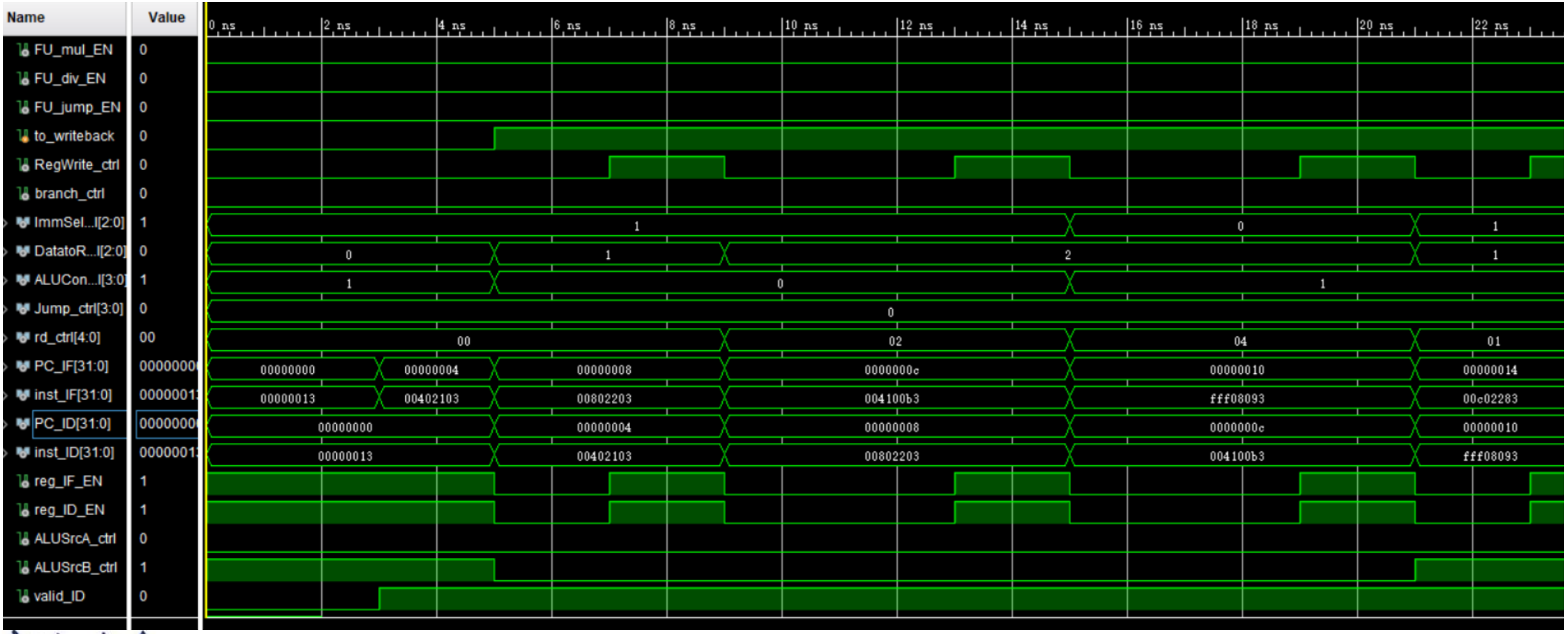
NO.	Instruction	Addr.	Comment
16	00000000	40	
17	00000000	44	
18	00000000	48	
19	00000000	4C	
20	A3000000	50	
21	27000000	54	
22	79000000	58	
23	15100000	5C	
24	00000000	60	
25	00000000	64	
26	00000000	68	
27	00000000	6C	
28	00000000	70	
29	00000000	74	
30	00000000	78	
31	00000000	7C	

Test Bench

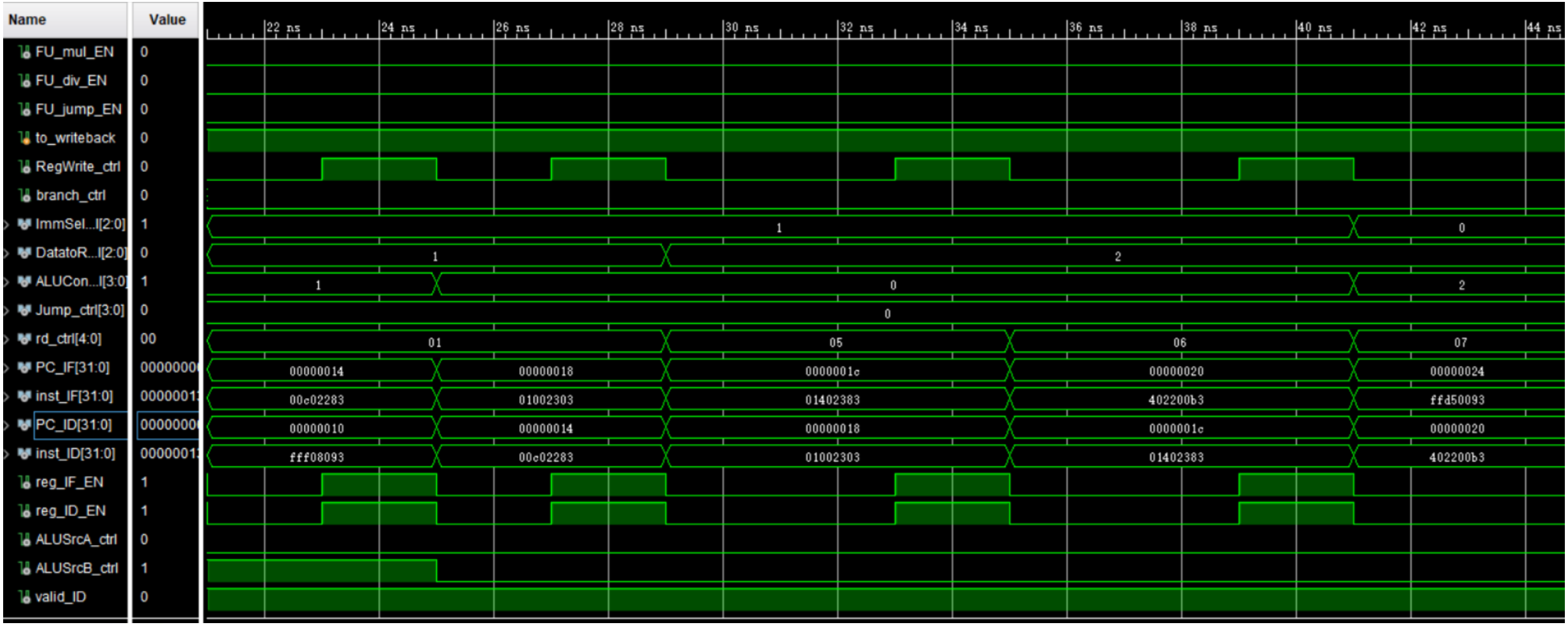
```
RV32core core(
    .debug_en(1'b0),
    .debug_step(1'b0),
    .debug_addr(7'b0),
    .debug_data(),
    .clk(clk),
    .rst(rst),
    .interrupter(1'b0)
);

initial begin
    clk = 0;
    rst = 1;
    #2 rst = 0;
end
always #1 clk = ~clk;
```

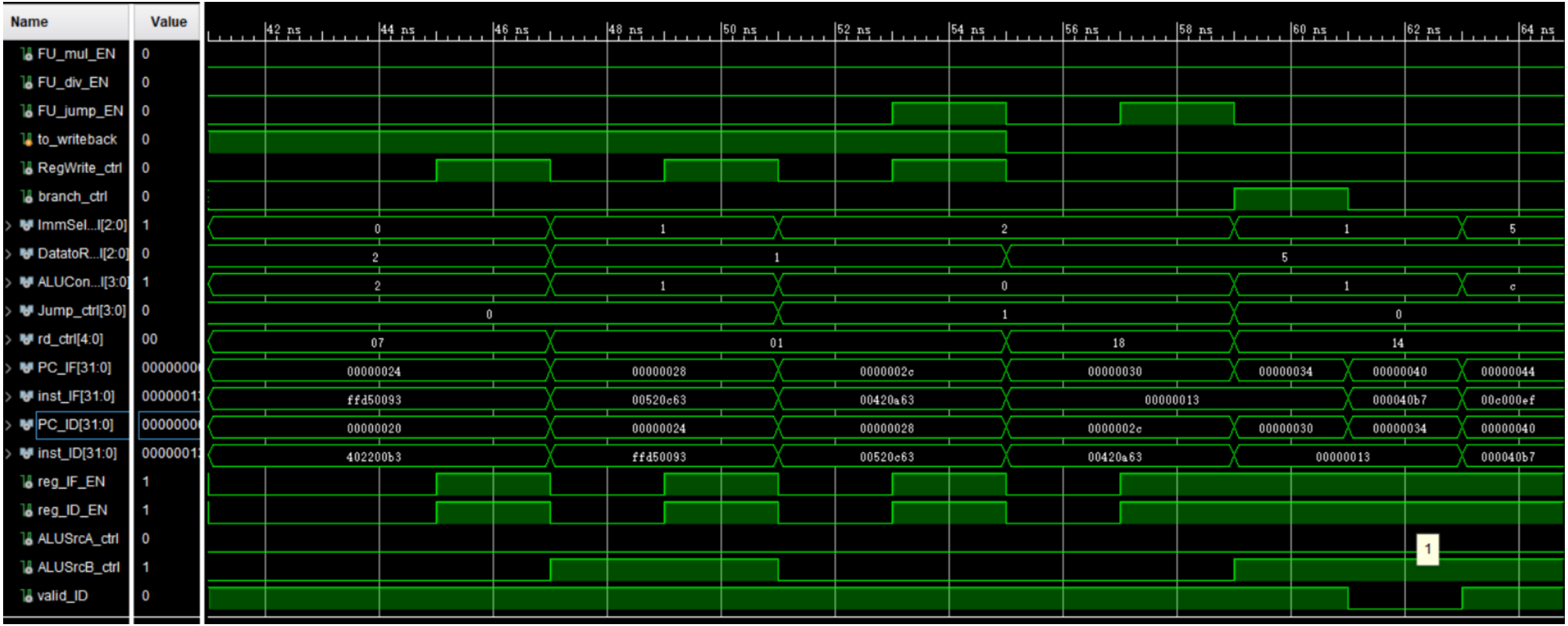
Simulation (1)



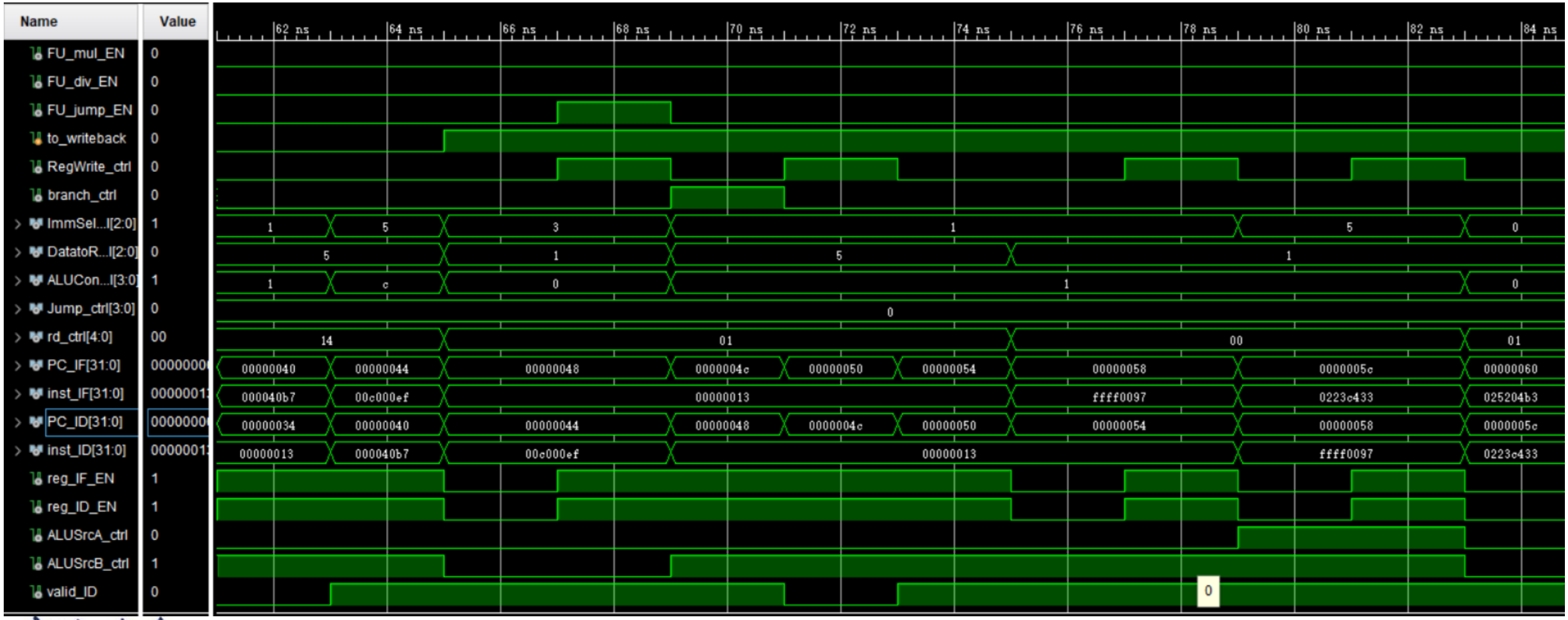
Simulation (2)



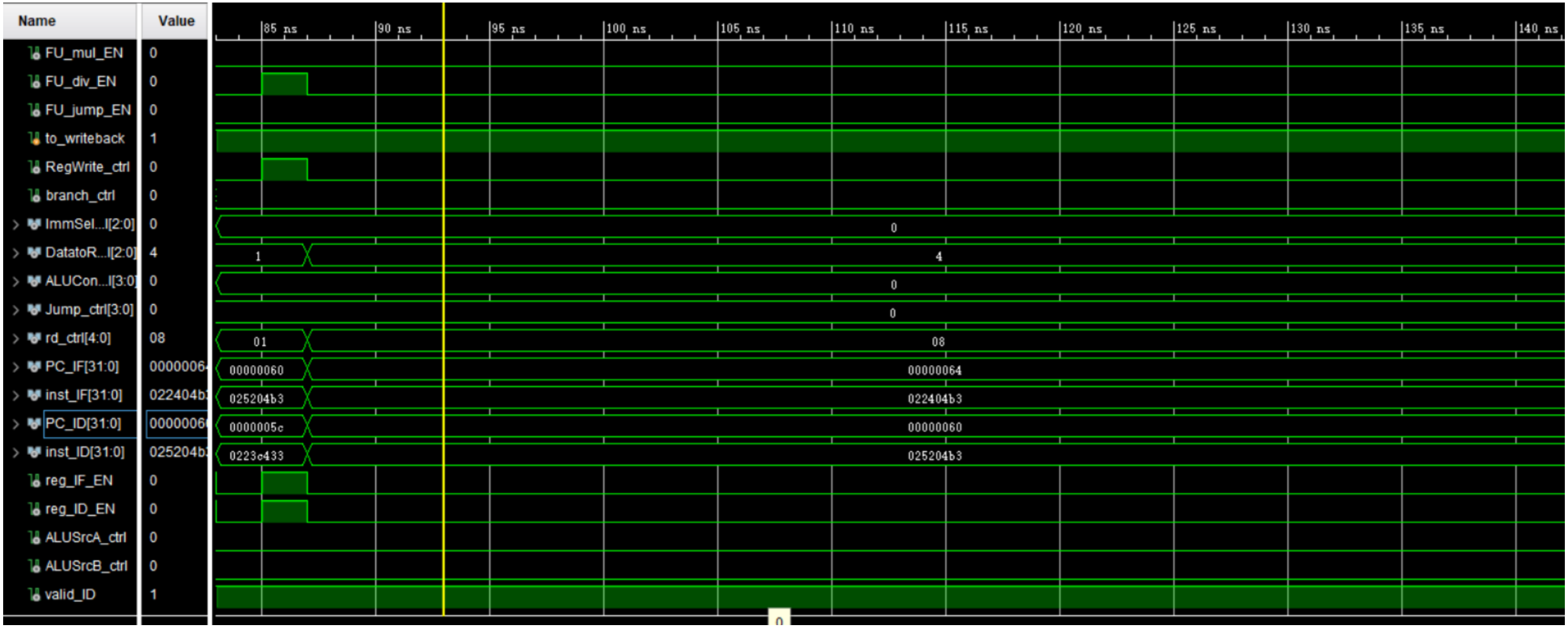
Simulation (3)



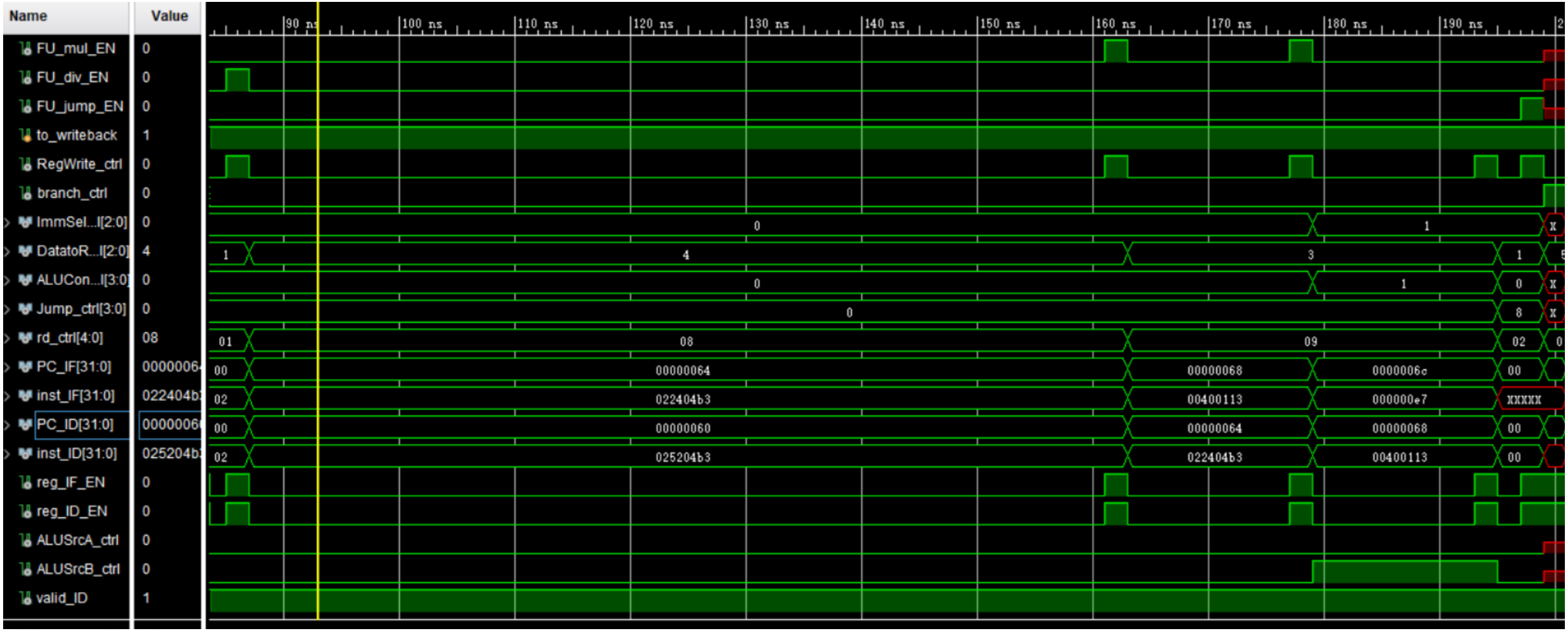
Simulation (4)



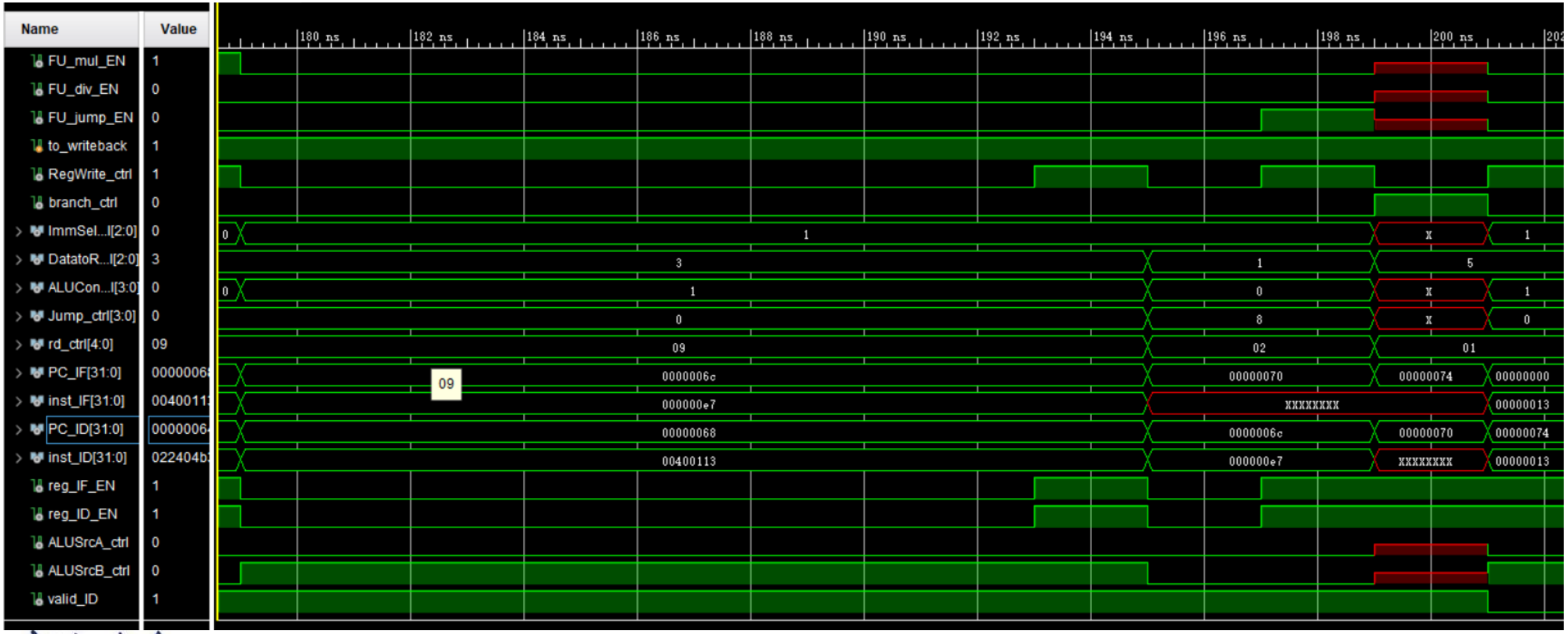
Simulation (5)



Simulation (6)



Simulation (7)



Checkpoints

- **CP 1:**

  Waveform Simulation of the Pipelined CPU with the verification program

- **CP 2:**

  FPGA Implementation of the Pipelined CPU with the verification program

Thanks!