3.2 Memory Map

ARM has a well-defined memory map for devices based on the ARM v7-M Architecture. The M4 further refines this map in the area of the Peripheral and System address ranges. Below is the system memory map as defined by ARM:

Table 3: ARM Cortex-M4 Memory Map

Address	Name	Executable	Description
0x00000000 – 0x1FFFFFFF	Code	Y	ROM or Flash Memory
0x20000000 – 0x3FFFFFFF	Reserved	N	Reserved
0x40000000 – 0x5FFFFFFF	Peripheral	N	On-chip peripheral address space
0x60000000 – 0x9FFFFFFF	External RAM	Y	External / Off-chip Memory
0xA0000000 – 0xDFFFFFFF	External Device	N	External device memory
0xE0000000 – 0xE00FFFFF	Private Peripheral Bus	N	NVIC, System timers, System Control Block
0xE0100000 – 0xFFFFFFFF	Vendor	N	Vendor Defined

The MCU-specific implementation of this memory map is as follows:

Table 4: MCU System Memory Map

Address	Name	Executable	Description
0x00000000 – 0x000FFFFF	Flash	Y	Flash Memory
0x00100000 - 0x03FFFFFF	Reserved	X	No device at this address range
0x04000000 – 0x07FFFFFF	External MSPI Flash	Y	XIP Read-Only External MSPI Flash
0x08000000 – 0x08000FFF	Boot Loader ROM	Y	Execute Only Boot Loader and Flash Helper Functions.
0x08001000 – 0x0FFFFFFF	Reserved	X	No device at this address range
0x10000000 – 0x1000FFFF	SRAM (TCM)	Y	Low-power / Low Latency SRAM (TCM)
0x10010000 – 0x1005FFFF	SRAM	Y	Main SRAM
0x10040000 – 0x3FFFFFFF	Reserved	X	No device at this address range
0x40000000 – 0x50FFFFFF	Peripheral	N	Peripheral devices
0x51000000 – 0x51FFFFFF	External Memory	X	Read/Write External Memory (MSPI) *[Chip Rev B Only]*
0x52000000 – 0xDFFFFFFF	Reserved	X	No device at this address range
0xE0000000 – 0xE00FFFFF	PPB	N	NVIC, System timers, System Control Block
0xE0100000 – 0xFFFFFFFF	Reserved	X	No device at this address range

Peripheral devices within the memory map are allocated on 4 KB boundaries, allowing each device up to 1024 32-bit control and status registers. Peripherals will return undefined read data when an attempt to access a register which does not exist occurs. Peripherals, whether accessed via the APB or the AHB, will always accept any write data sent to their registers without attempting to return an ERROR response. Specifically, a write to a read-only register would just become a don’t-care write.