SHRI RAMSWAROOP MEMORIAL GROUP OF PROFESSIONAL COLLEGES

E

QUIZ TEST-1

(Session: 2021-22)

MCA [Semester I]

KCA-105: Computer Organization and Architecture

Duration: 01 Hour | Maximum Marks: 30

Roll No. | | | | | | | |

(To be filled by Students)

Note: Attempt all questions

Part – A

(Questions from Tutorial Sheet I)

[10 Marks] CO BL

Q1) Differentiate between centralized and distributed arbitration. (Q. No. 7) (5) CO1 2

Q2) What are the main functions and components of CPU? (Q. No.2) (5) CO1 2

Part – B

[20 Marks] [1x5=5] CO BL

Q3) Briefly answer the following parts (a) – (e).

a) What do you mean by EA? CO1 1

b) Define Register Indirect Mode. CO1 1

c) How will you write the expression A*B+C*D in reverse polish notation? CO1 1

d) What is Cache Memory? CO1 1

e) What is an instruction? CO1 1

Q4) Discuss about Memory Transfer and Explain its process with the help of 4*1 multiplexer. (4+4) CO1 2

Q5) What is Memory Stack? Explain its operation with the help of an example. (3+4) CO1 2

X

No of Students : 50
Date of Quiz Test: 31/12/2021
KCA-105: Er. Shivam Awasthi

SHRI RAMSWAROOP MEMORIAL COLLEGE OF ENGINEERING & MANAGEMENT

PRE END SEMESTER EXAMINATION

(Session: 2021-22)

MCA I Sem.

KCA-105: Computer Organization & Architecture

Duration: 03 Hours **Maximum Marks: 100**

Note: (a) This paper is divided into three sections. Attempt all Sections
(b) Section A contains 10 Questions carrying 02 mark each.
(c) Section B contains 05 Questions carrying 10 marks each.
(d) Section C contains 05 Questions carrying 10 marks each.

Section-A

Q 1: Attempt all parts. All parts carry equal marks. Be precise in your answers. [2 X 10 = 20 Marks]		Marks	CO	BL
(a)	Explain the block structure of computer briefly.	[2]	CO1	1
(b)	Define Bus Architecture.	[2]	CO1	1
(c)	Find 2's complement of the number 5 and -13.	[1+1]	CO2	1
(d)	What is IEEE standard for floating point number?	[2]	CO2	1
(e)	Differentiate between RISC and CISC architecture.	[2]	CO3	1
(f)	Explain all the phases of instruction cycle briefly.	[2]	CO3	1
(g)	What is meant by cache mapping?	[2]	CO4	1
(h)	What do you understand by Virtual Memory?	[2]	CO4	1
(i)	What is I/O control method?	[2]	CO5	1
(j)	What is memory management unit?	[2]	CO5	1

Section-B

Q2: Attempt any *three* Questions from this section. [10 X 3 = 30 Marks]		Marks	CO	BL
(a)	What is Bus Arbitration? Explain its types.	[3+7]	CO1	4
(b)	Design a 4-bit carry look ahead adder and explain its operation with an example.	[5+5]	CO2	4
(c)	Explain the data flow during an interrupt cycle with the help of diagram.	[10]	CO3	3
(d)	Explain 2D & $2^{1/2}$ D memory organization.	[5+5]	CO4	4
(e)	What do you mean by serial communication? What are the transmission modes of serial communication?	[3+7]	CO5	3

Section-C

Q3: Attempt any *one* part of the following. [10 X 1 =10 Marks]		Marks	CO	BL
(a)	Describe in detail the different kinds of addressing modes with an example.	[10]	CO1	2
(b)	What is Memory Stack? Explain its operation with the help of an example.	[2+8]	CO1	3

Number of Students: 48
Date of Pre-End Sem Exam: 02/02/2022
KCA-105_Er. Shivam Awasthi

Q4: Attempt any *one* part of the following. [10 X 1 =10 Marks]	Marks	CO	BL
(a) Show step by step the multiplication process using Booth's algorithm when (+ 15) and (– 13) numbers are multiplied. Assume 5-bit registers that hold signed numbers.	[10]	CO2	4
(b) Perform restoring division operation on following dividend & divisor. Dividend = 1010 and Divisor = 0011.	[10]	CO2	5

Q5: Attempt any *one* part of the following. [10 X 1 =10 Marks]	Marks	CO	BL
(a) Describe the types of instructions on the basis of address fields used in the instruction with example.	[10]	CO3	3
(b) What is pipeline? Explain it's types with example.	[2+8]	CO3	3

Q6: Attempt any *one* part of the following. [10 X 1 =10 Marks]	Marks	CO	BL
(a) Explain semiconductor RAM. Enlist the types of semiconductor memory.	[5+5]	CO4	3
(b) A ROM chip of 1024*8 has four select inputs and operates from a 5-volt power supply. How many pins are needed for the IC package? Draw a diagram and label all input and output terminals in the ROM.	[5+5]	CO4	5

Q7: Attempt any *one* part of the following. [10 X 1 =10 Marks]	Marks	CO	BL
(a) Discuss the various types of address mapping used in cache memory.	[10]	CO5	3
(b) Explain auxiliary memory. What are the commonly used auxiliary memory?	[3+7]	CO5	3

X

PAPER ID-411334

Roll No: [ ]

MCA
(SEM I) THEORY EXAMINATION 2021-22
COMPUTER ORGANIZATION & ARCHITECTURE

Time: 3 Hours *Total Marks: 100*

Notes:

- *Attempt all Sections and assume any missing data.*
- *Appropriate marks are allotted to each question, answer accordingly.*

SECTION-A	Attempt All of the following Questions in brief	Marks(10X2=20)	CO
Q1(a)	What are the various facts related to bus and bus system?		
Q1(b)	What is arithmetic and logic circuit?		
Q1(c)	Describe the micro-programming sequencing.		
Q1(d)	What do you mean by programming of ROM?		
Q1(e)	What is the function of I/O interface?		
Q1(f)	Discuss the basic component of register transfer logic.		
Q1(g)	What is the main advantage of RTL?		
Q1(h)	Define the goal of CISC architecture.		
Q1(i)	Define the goal of RISC architecture.		
Q1(j)	What are the modes of data transfer?		

SECTION-B	Attempt ANY THREE of the following Questions	Marks(3X10=30)	CO
Q2(a)	What is programmable logic device? List various techniques to program PLD. Explain any one technique with example.		
Q2(b)	Write Short Notes on any two of the following: i) Central Processing Unit (CPU). iii) Input/output Interface. ii) Input/output Ports.		
Q2(c)	Show step by step the multiplication process using booth's algorithm when (+15) and (-13) numbers are multiplied.		
Q2(d)	Assume 5 – bit registers that hold signed numbers.		
Q2(e)	Explain various types of processor organization.		

SECTION-C	Attempt ANY ONE following Question	Marks (1X10=10)	CO
Q3(a)	Explain General-purpose register based organization.		
Q3(b)	What is the Stack organization? Compare register stack and memory stack.		

SECTION-C	Attempt ANY ONE following Question	Marks (1X10=10)	CO
Q4(a)	Explain the Booth's algorithm in depth with the help of flowchart. Give an example for multiplication using Booth's algorithm.		
Q4(b)	Perform the division process of 00001111 by 0011 (use a dividend of 8 bits).		

SECTION-C	Attempt ANY ONE following Question	Marks (1X10=10)	CO
Q5(a)	Evaluate the arithmetic statements X=(A+B)*(C+D) using a general register computer with three address, two address and one address instruction format a program to evaluate the expression.		
Q5(b)	Explain hardwired control unit. What are the methods to design hardwired controllers?		

SECTION-C	Attempt ANY ONE following Question	Marks (1X10=10)	CO
Q6(a)	A ROM chip of 1024*8 has four select inputs and operates from a 5volt power supply. How many pins are needed for the IC package? Draw a block diagram and label all input and output terminals in the ROM.		
Q6(b)	Explain 2D, 2 ½D memory organizations.		

SECTION-C	Attempt ANY ONE following Question	Marks (1X10=10)	CO
Q7(a)	Give the block diagram of DMA controller. Why are the read and write control lines in a DMA controller bidirectional?		
Q7(b)	What do you mean by serial communication? What are the transmission modes of serial communication?		