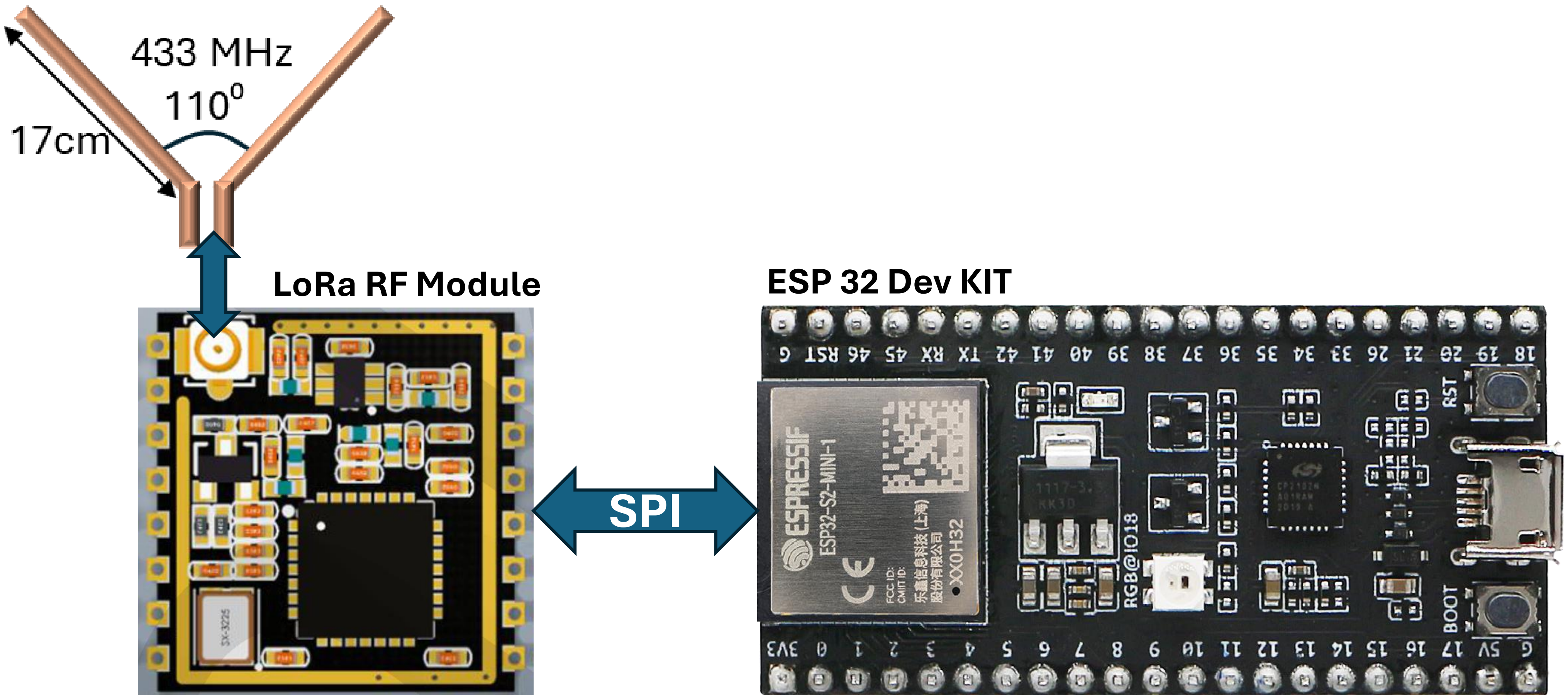
SI-2024 Introduction to CubeSat and Satellite Communication

LoRa Basics

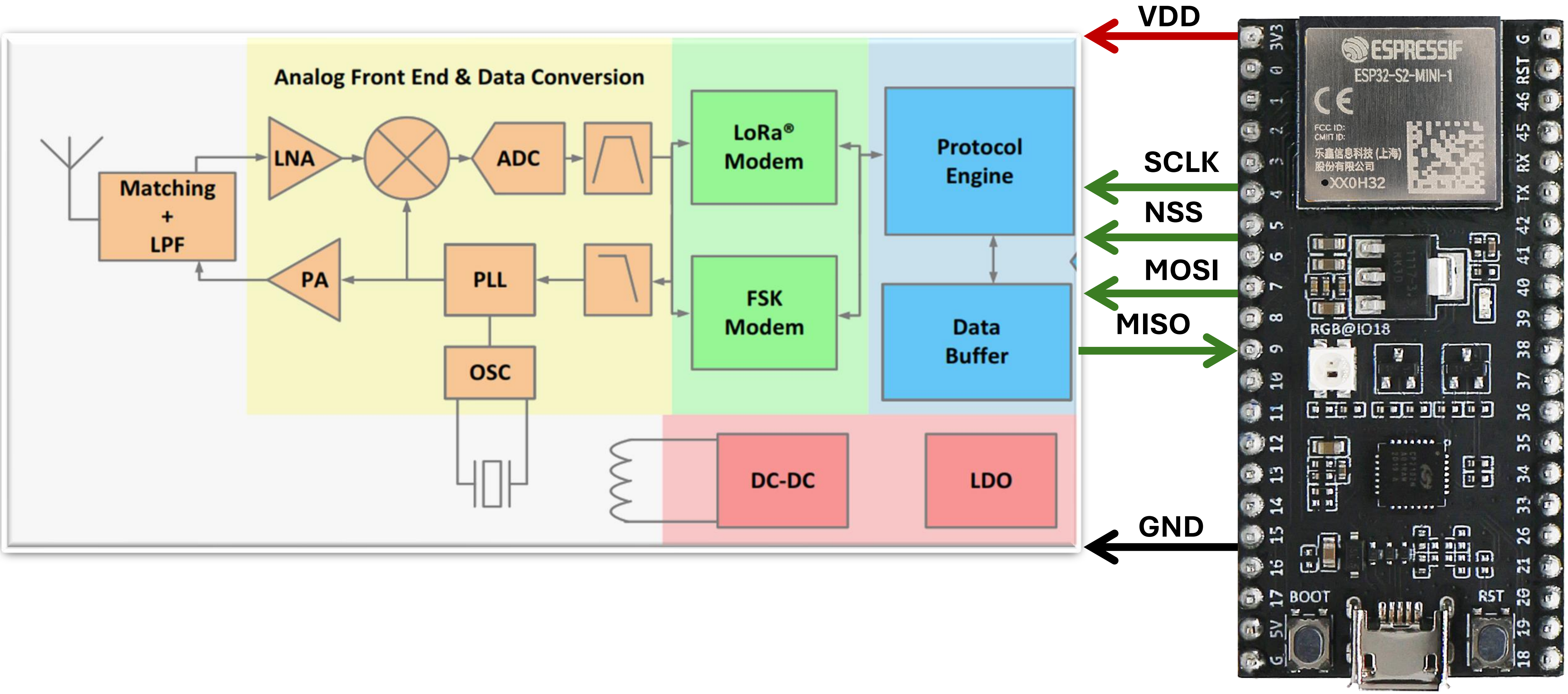
2nd July 2024

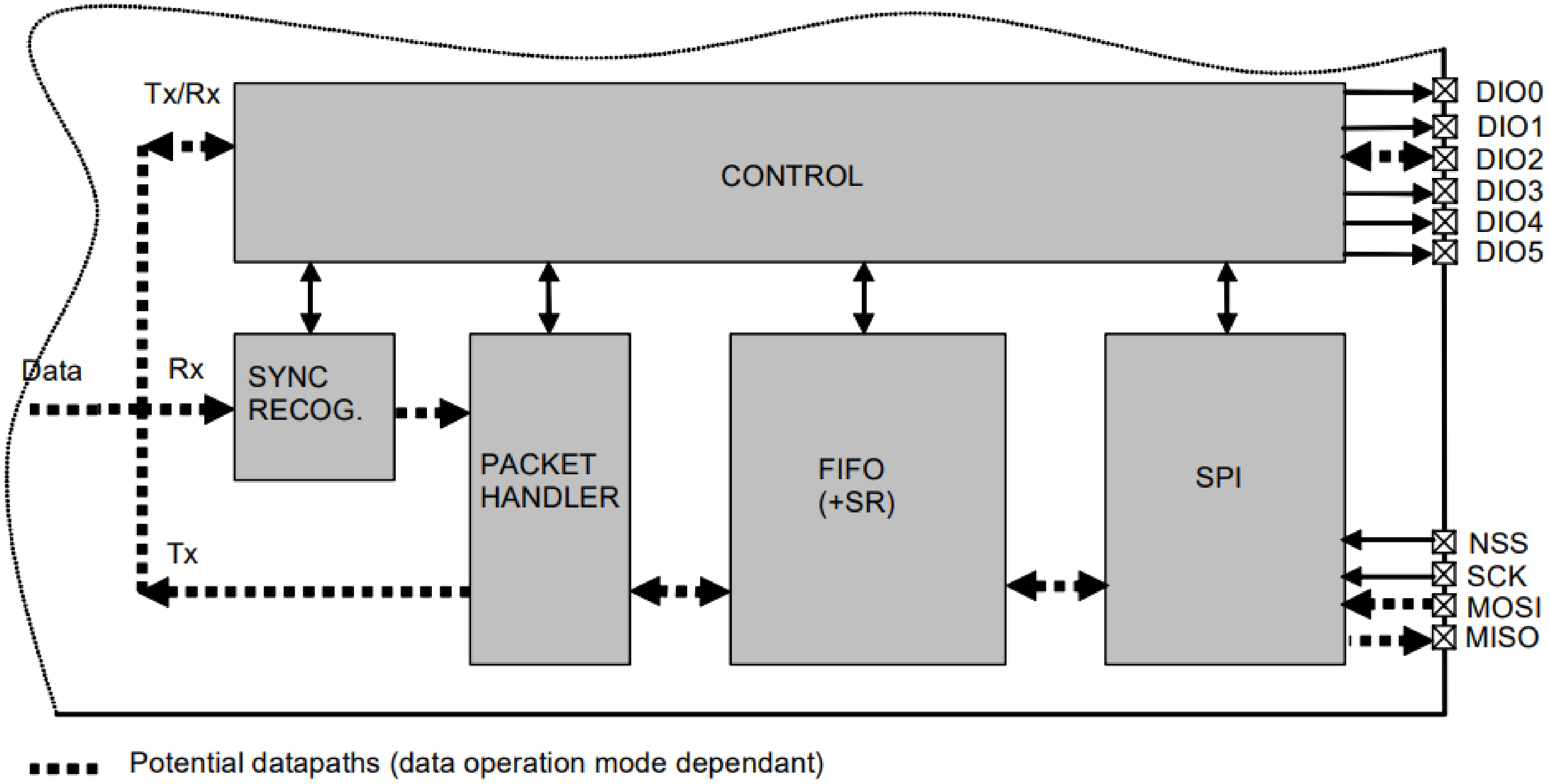
SiliconTech

LoRa + ESP32



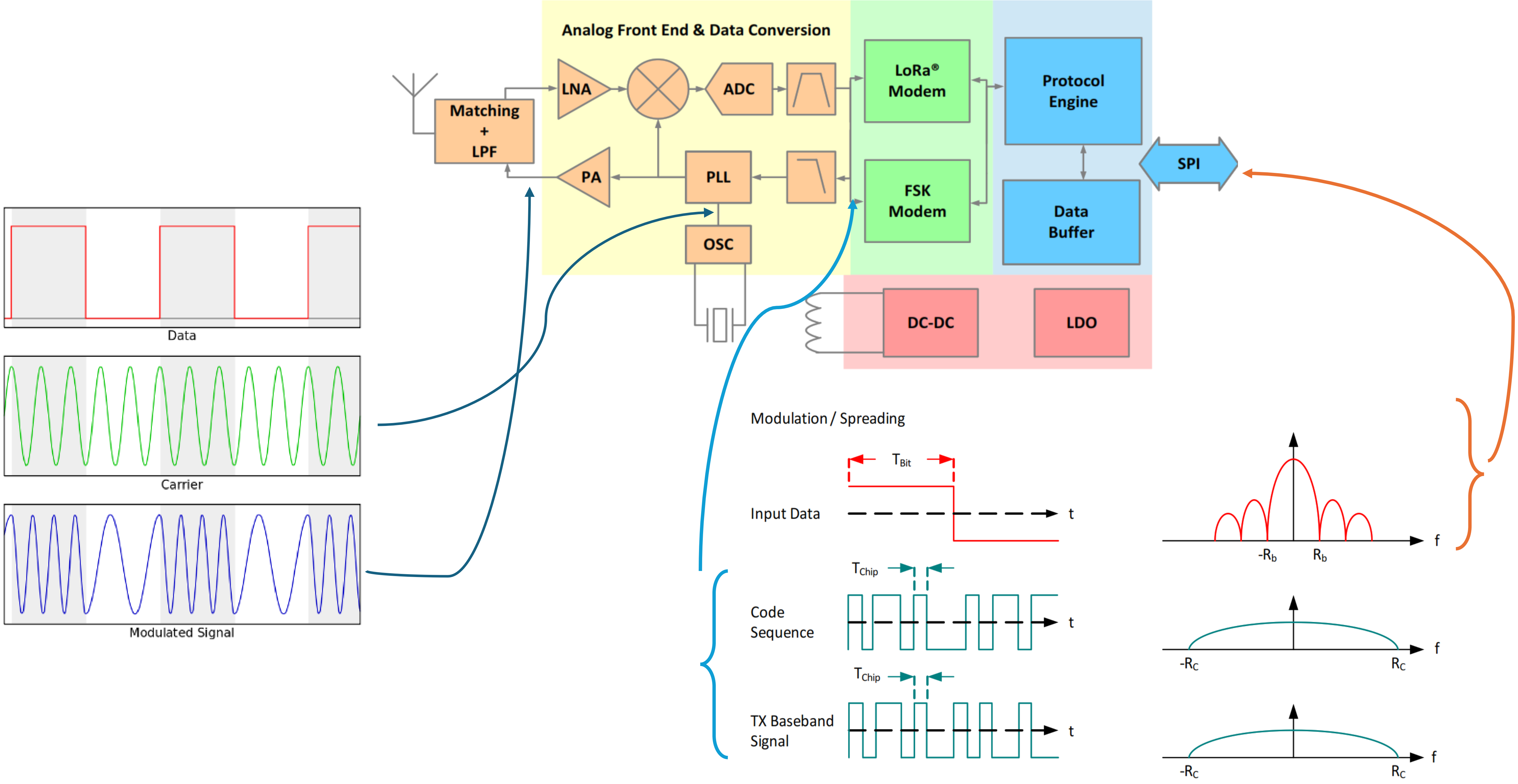
LoRa + ESP32


Analog Front End & Data Conversion
Matching
+
LPF
LNA
ADC
PA
PLL
OSC
LoRa®
Modem
FSK
Modem
Protocol
Engine
Data
Buffer
DC-DC
LDO
VDD
SCLK
NSS
MOSI
MISO
GND
ESPRESSIF
ESP32-S2-MINI-1
RGB@IO18
BOOT
RST



Continuous mode: each bit transmitted or received is accessed in real time at the DIO2/DATA pin. This mode may be used if adequate external signal processing is available.
Packet mode (recommended): user only provides/retrieves payload bytes to/from the FIFO. The packet is automatically built with preamble, Sync word, and optional CRC and DC-free encoding schemes The reverse operation is performed in reception. The uC processing overhead is hence significantly reduced compared to Continuous mode. Depending on the optional features activated (CRC, etc) the maximum payload length is limited to 255, 2047 bytes or unlimited.

LoRa Transceiver (Radio) Architecture



LoRa Basics: Shannon-Hartley Theorem

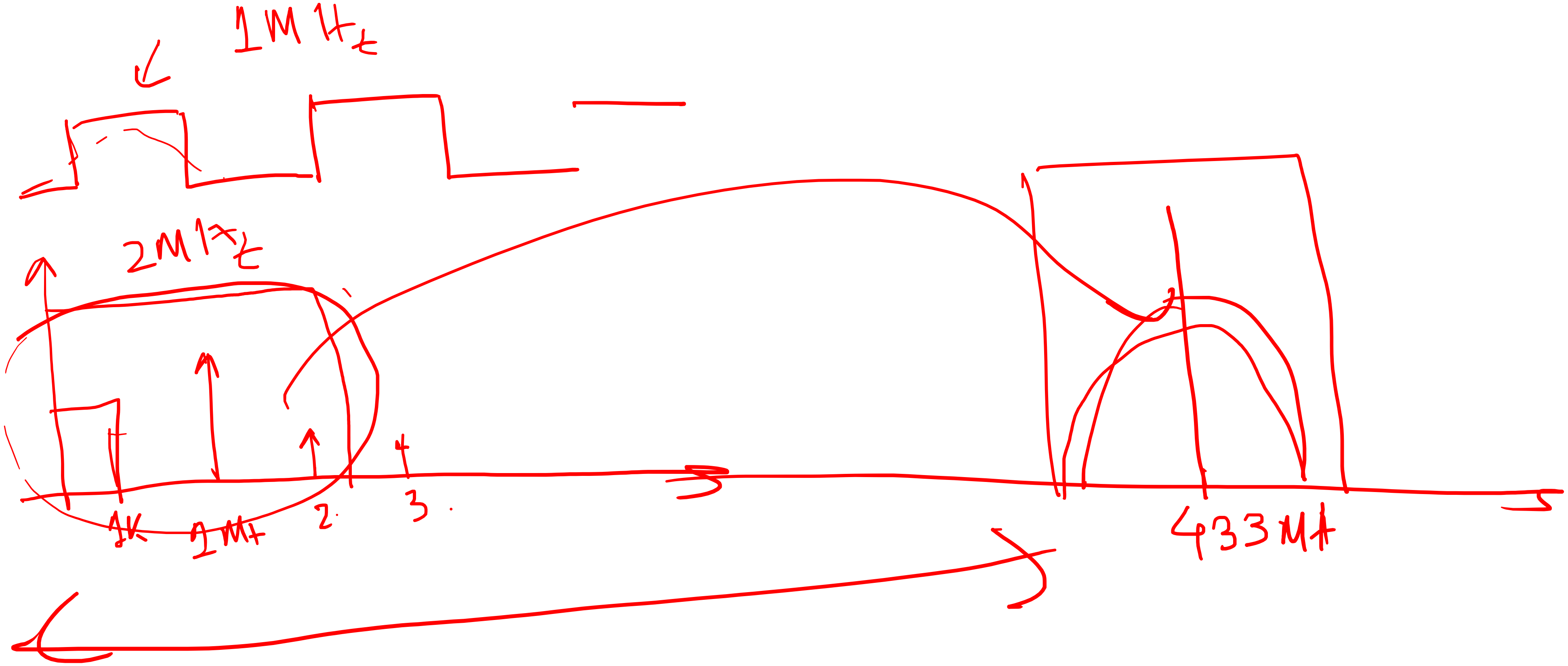
$$Channel\ Capacity\ (C) = B \cdot \log_2\left(1 + \frac{S}{N}\right)\ bits/sec$$

$$where:$$
$$B\ is\ the\ channel\ bandwidth\ (B),$$
$$S\ is\ the\ average\ signal\ power\ (Watts),$$
$$N: average\ noise\ power\ (watts)$$

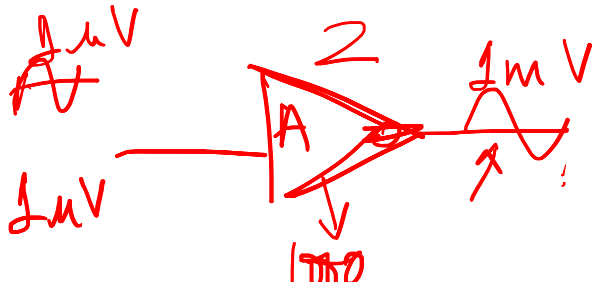
With some algebra and assuming S/N << 1 :

$$Channel\ Capacity\ (C) \approx B \cdot \frac{S}{N}\ bits/sec$$

Therefore, for a give S/N ratio, the channel capacity can be increased by merely increasing the bandwidth of the transmitted signal.



1MHz
2MHz
1K
1MHz
2
3
433MHz



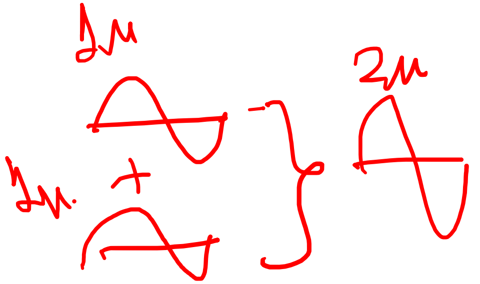
$$20\log\left(\frac{1mV}{1\mu V}\right) = 60\,dB$$

A 3

6

$\log(A_1 \cdot A_2)$

$\log(A_1) + \log(A_2)$



$1\mu \sin\omega t + 1\mu \sin\omega t$

$2\mu \sin\omega t \times \boxed{1000}$

$2mV \sin\omega t$

Noise : uncorrelated

$v_1 = 1\mu V$

$$20\log\left(\frac{1mV}{1mV}\right)$$

$$\boxed{SNR = 60\,dB}$$

$1mV + 1mV = 2mV$

$v_1 = 1\mu V, \quad v_2 = 1\mu V$

$$\cancel{SNR = 20\log\left(\frac{2mV}{2\mu V}\right) = 60\,dB}$$

$$V_{tot} = \sqrt{V_1^2 + V_2^2} = \sqrt{1\mu^2 + 1\mu V^2}$$

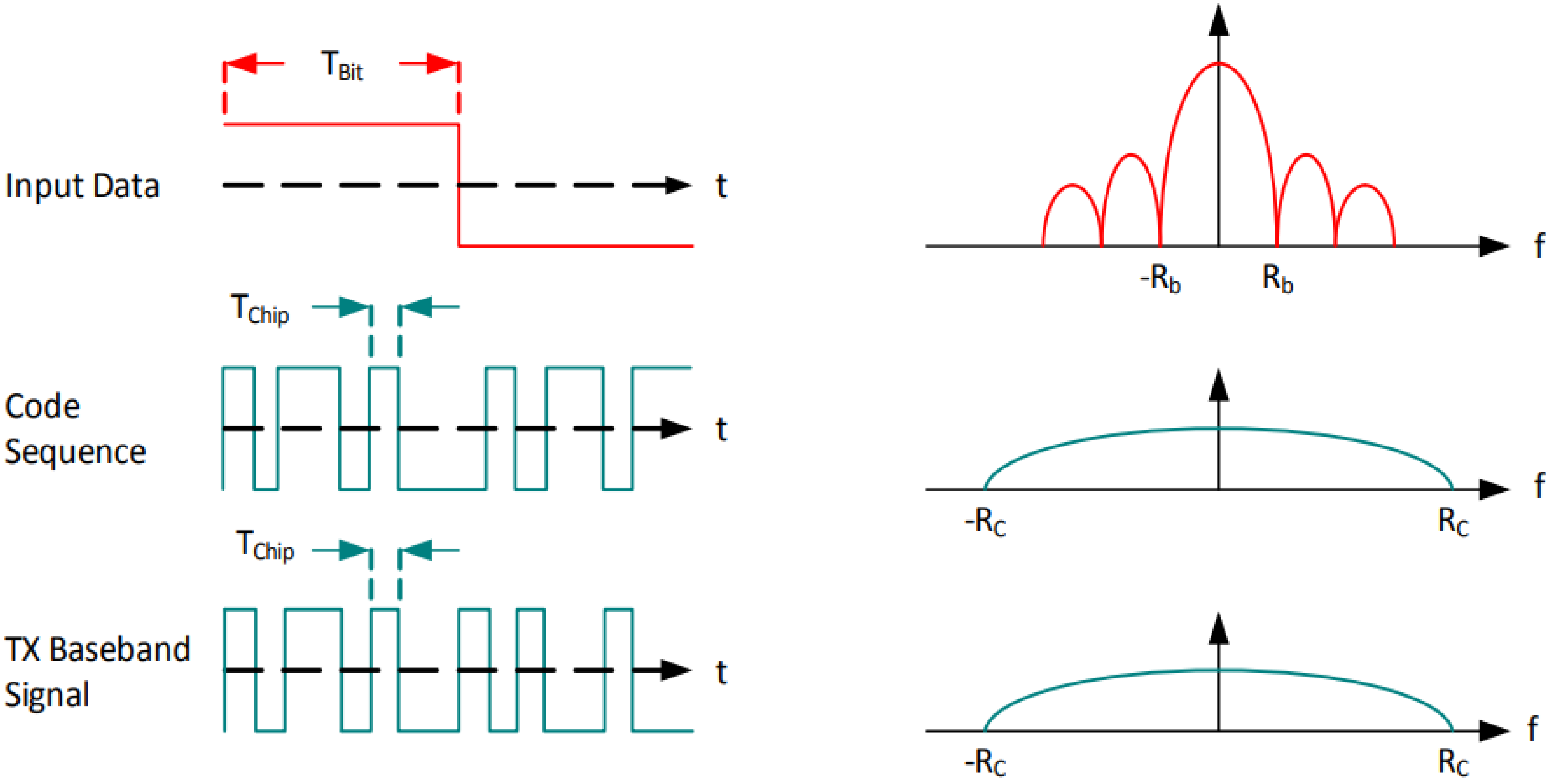
$$= \sqrt{2} \cdot 1\mu V$$

$$SNR = 20\log\left(\frac{2mV}{\sqrt{2} \cdot 1\mu}\right)$$

$$20\log\left(\frac{2000}{\sqrt{2}}\right)$$

$$\sqrt{2\mu^2 V} = \sqrt{2}\,\mu V$$

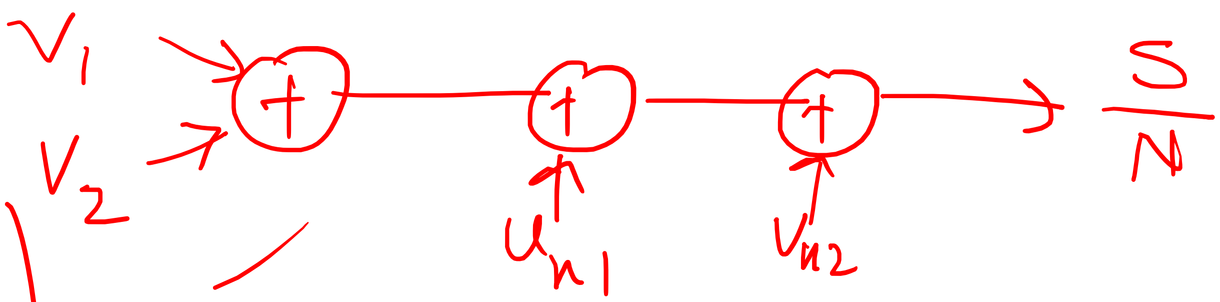
Spread-Spectrum Principles: Modulation/Spreading



Processing Gain $(G_P) = 10\log\left(\frac{R_C}{R_B}\right)$

where, $R_C: chip\ rate, R_B: bit\ rate$

$$20\log\left(\frac{V_1+V_2+V_3\cdots V_n}{\sqrt{V_{n1}^2+V_{n2}^2+\cdots V_n^2}}\right)$$



$$\frac{36.5\,dB}{73\,dB}$$

$$10\log\left(\frac{(V_1+V_2+V_3+\cdots V_n)^2}{V_{n1}^2+V_{n2}^2+\cdots V_{nn}^2}\right)$$

$$20\log\left(\frac{\sqrt{2}\times 20\,mV}{\sqrt{2^2\mu V+4^2\mu V}}\right)\rightarrow \text{rms}$$

$V_1 = 10\,mV\sin\omega t$

$V_2 = 10\,mV\sin\omega t$

$V_{n1} = 2\,\mu V_{rms}$

$V_{n2} = 4\,\mu V_{rms}$

$\underline{SNR} = ?$

$$=20\log\left(\frac{\sqrt{2}\times 20\,\mu V}{\sqrt{20}\,\mu V}\right)$$

$$=20\log(\sqrt{40}\times 1000)$$

$$=\underbrace{20\log(\#)}_{18\,dB}+\underbrace{20\log(1000)}_{60}$$

$\underline{73\,dB}$

~ 78

dBm $\quad \underline{10\log\left(\frac{P_{out}(W)}{1mW}\right)}$

$\frac{V^2}{R}$

Tx $\rightarrow$ +20 dBm $\rightarrow$

Rx $\rightarrow$ -148 dBm

$$\frac{-148}{10} = 10^{-14.8} = \underline{\underline{10^{-15} \times 1mW}}$$

$$= 10^{-9}\ \mu W$$

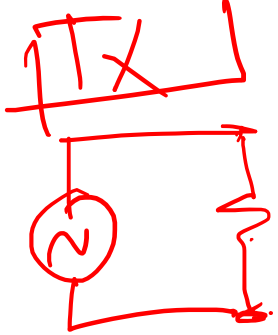
$$10\log\left(\frac{P_{out}}{1mV}\right) = 20\ \text{dBm} \qquad \frac{20}{3}\times 7$$

$$\log\left(\frac{P_{out}}{1m}\right) = 2$$

$$P_{out} = 100\ mV \qquad 2^7 = \underline{64} - 12$$

$$10\log\left(\frac{2mW}{1mV}\right) = 3\text{dBm}.$$

$$10\log(2\times2\times2\times$$



+20 dB

100 mV

$50\,\Omega$

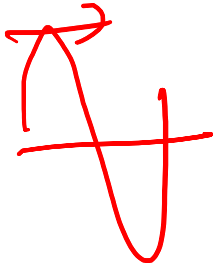
$V_{Tx} =$

$$\frac{V_{Tx}^2}{50\,\Omega} = 100\,mW$$

$$V_{Tx} = \sqrt{100 \times 10^{-3} \times 50}$$

$$= \sqrt{5} = 2.\ldots V$$

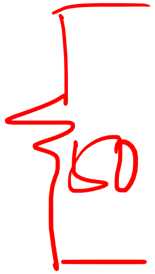
$$\sqrt{2} \times \sqrt{5}$$



$\leftarrow 3V \cdot \sin(\omega t)$

400 MHz

-158 dB



$50\,\Omega$

V_{Rx}

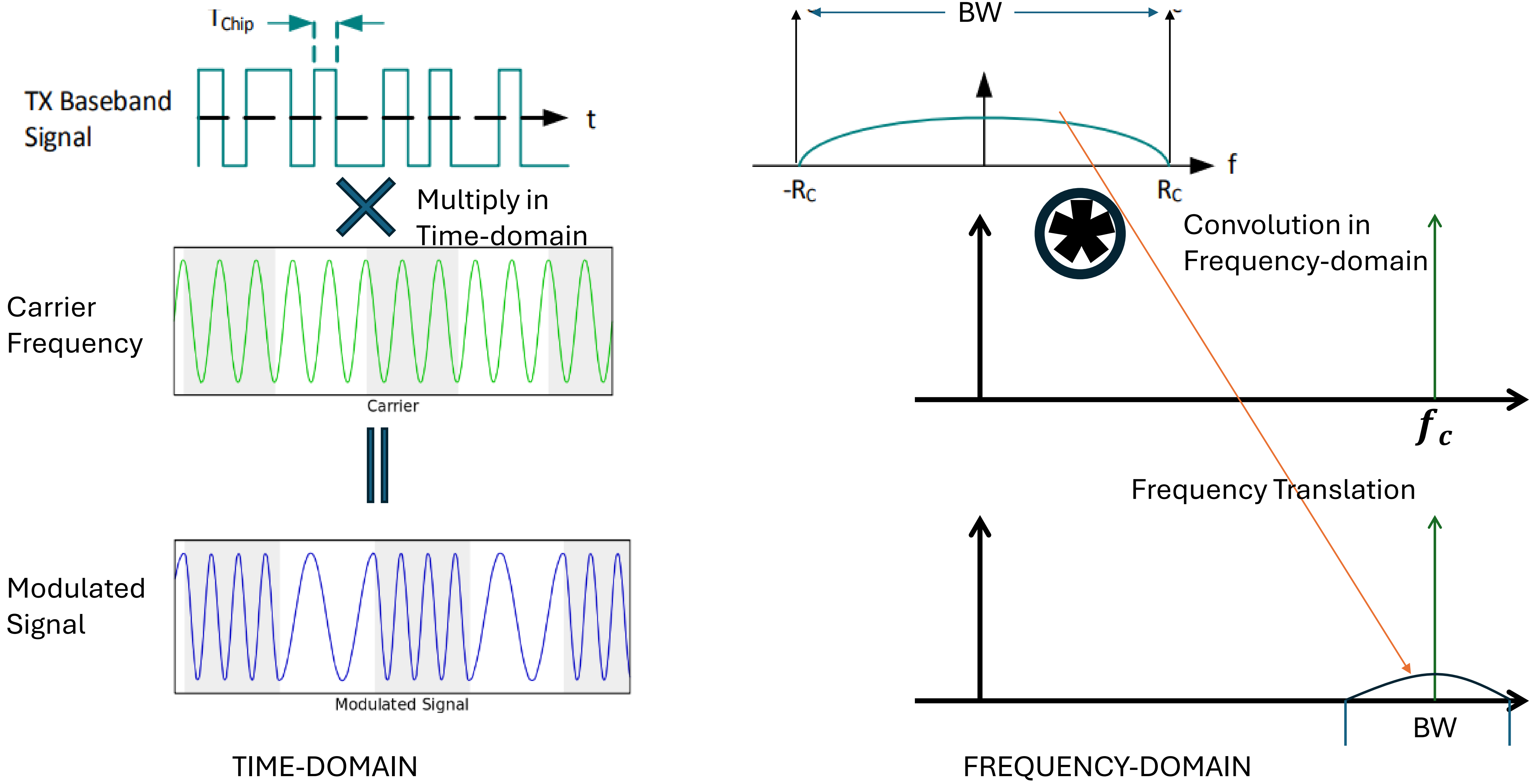
$$\frac{V_{Rx}^2}{50\,\Omega} = 10^{-15} \times 1\,mW$$

$$V_{Rx} = \sqrt{50 \times 10^{-18}}$$

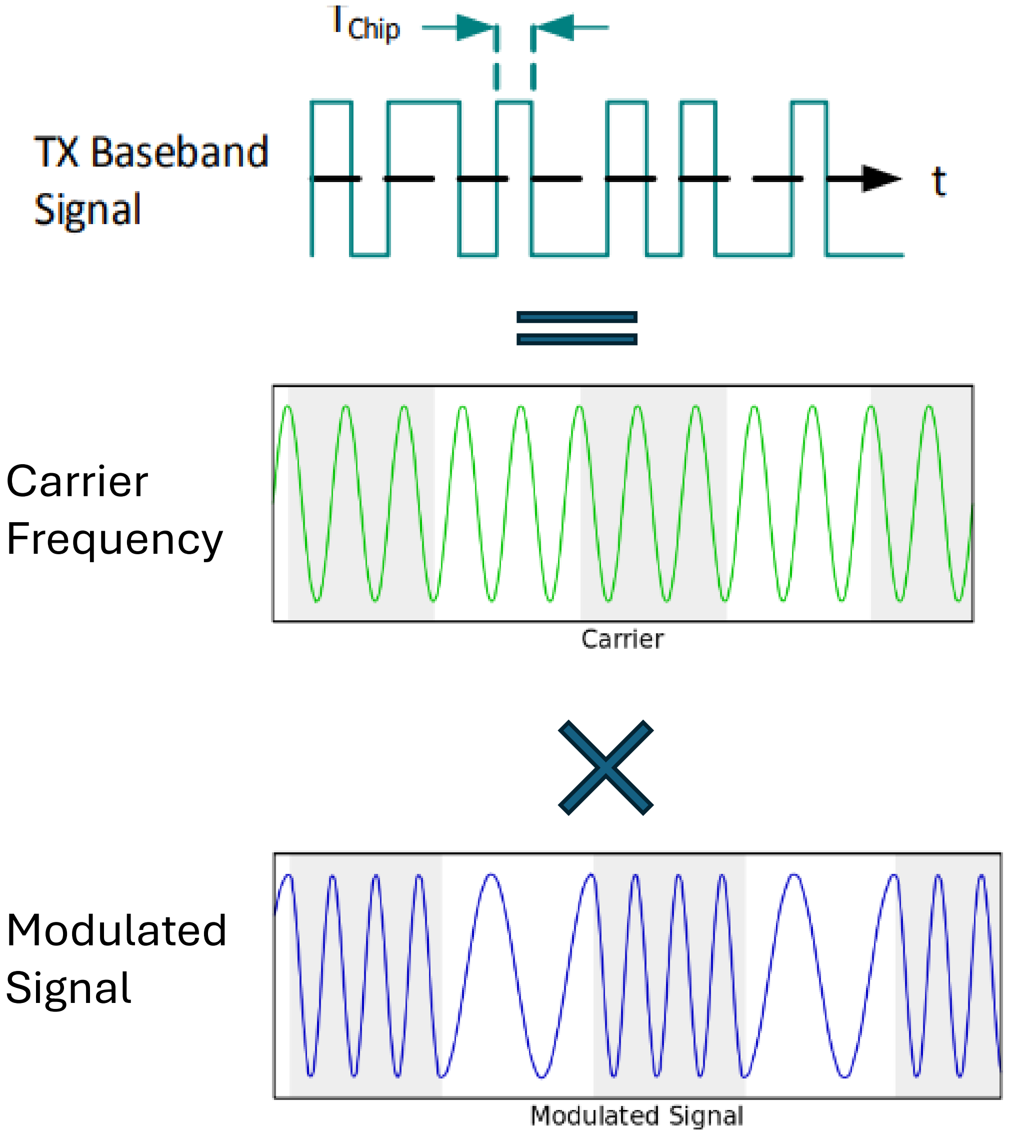
$$= \sqrt{50} \times 10^{-9}\ V$$

$$\boxed{V_{Rx} \doteq 7\,nV}$$

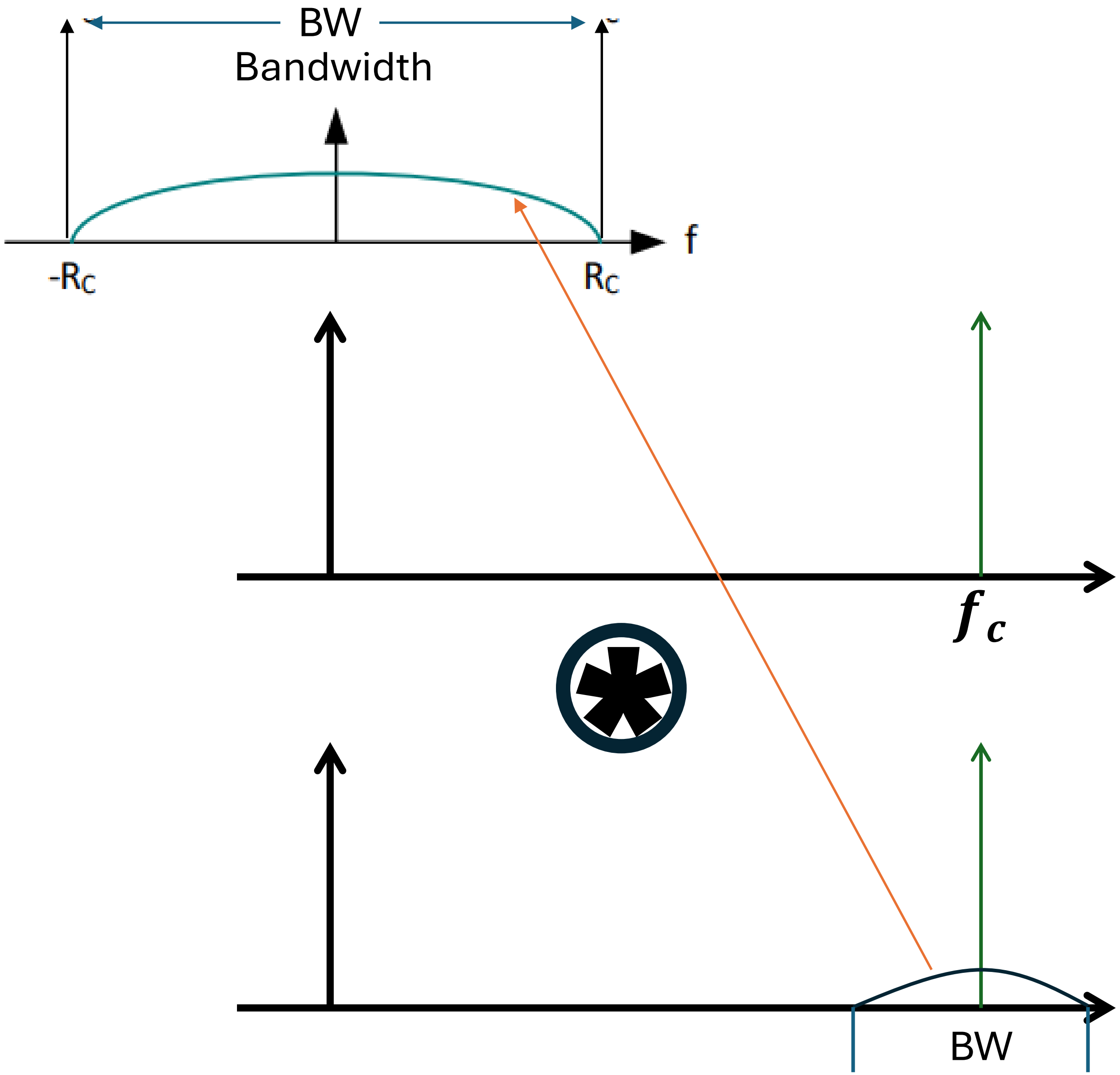
Spread-Spectrum Principles: Modulation/Spreading



Spread-Spectrum Principles: Demodulation/De-spreading



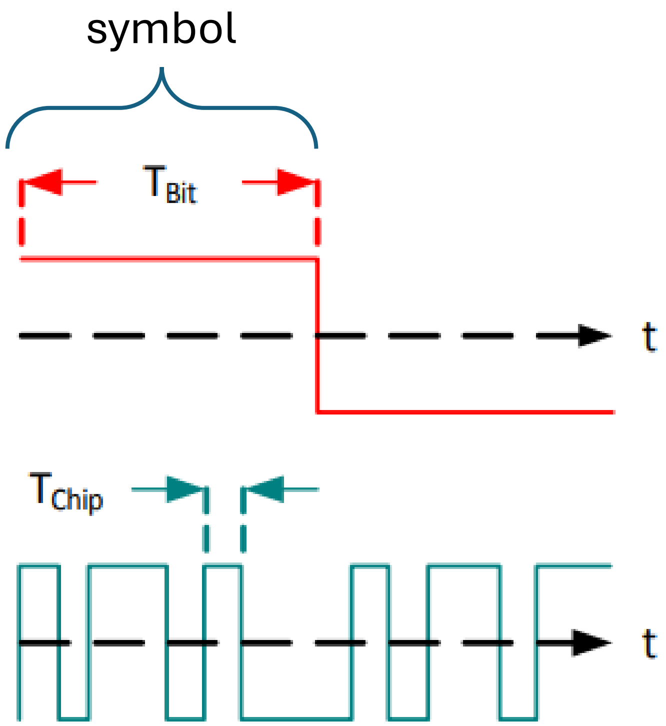
TIME-DOMAIN



FREQUENCY-DOMAIN

LoRa Spread-Spectrum: Spreading Factor

SpreadingFactor (RegModulationCfg)	Spreading Factor (Chips / symbol)	LoRa Demodulator SNR
6	64	-5 dB
7	128	-7.5 dB
8	256	-10 dB
9	512	-12.5 dB
10	1024	-15 dB
11	2048	-17.5 dB
12	4096	-20 dB



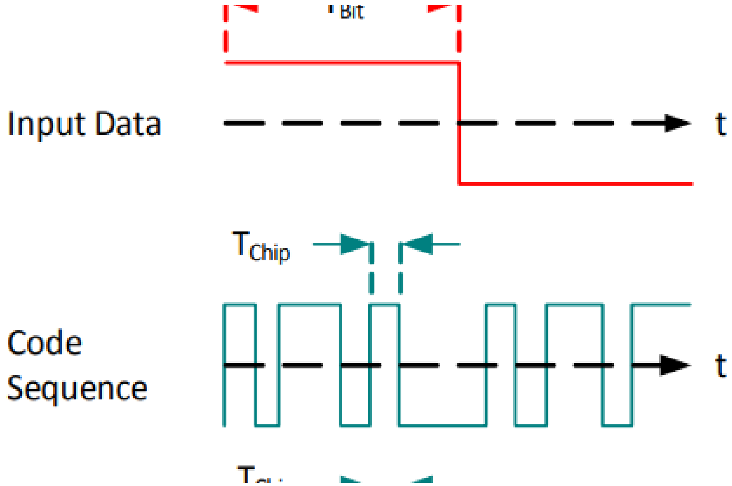
$$Spreading\ Factor\ (SF) = 2^{SF}\, chips/sym$$

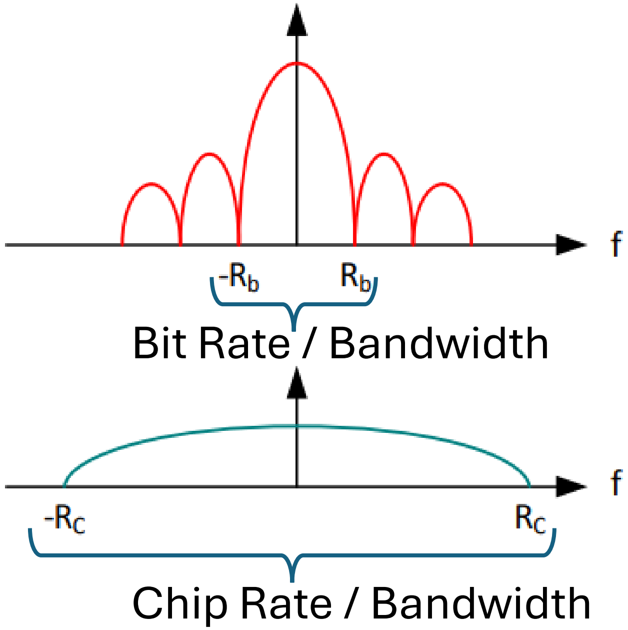
LoRa Spread-Spectrum: Modulation Bandwidth

Bandwidth (kHz)	Spreading Factor	Coding rate	Nominal Rb (bps)
7.8	12	4/5	18
10.4	12	4/5	24
15.6	12	4/5	37
20.8	12	4/5	49
31.2	12	4/5	73
41.7	12	4/5	98
62.5	12	4/5	146
125	12	4/5	293
250	12	4/5	586
500	12	4/5	1172

$$R_B = SF \frac{1}{2^{SF}/BW} \text{bits/sec}$$

$$R_C = R_B 2^{SF} \text{ chips/sec}$$





LoRa Sensitivity and Rate Calculation

RX Sensitivity at 433 MHz

Spread Factor	SNR (dB)	Sensitivity (dBm)
7	-7	-125
10	-15	-134
12	-20	-141

LoRa™ Rate Calculation Guide

SrNo	BW\SF	6	7	8	9	10	11	12
0	7.8khz	585 bps	**341**	195	109	60	52	18
1	10.4khz	780	455	**260**	146	81	69	24
2	15.6khz	1170	682	390	219	121	104	36
3	20.8khz	1562	910	520	**292**	162	139	49
4	31.2khz	2340	1365	780	438	**243**	209	73
5	41.6khz	3120	1820	1040	585	325	**279**	97
6	62.5khz	4688	2734	1562	878	488	419	146
7	125khz	9380	5468	3125	1757	976	839	**293**
8	250khz	18750	10937	6250	3515	1953	1678	585
9	500khz	37500	21875	12500	7031	3906	3356	1171

RSSI and SNR LoRa Mode in LF Mode (433MHz)

$RSSI = 64\,dB$ $\quad RSSI\ pck\ (dBm) = -164 + 64 = -100\ dBm.$

10^{-10} $\quad 1mV$ $\quad \boxed{10^{-10}\,mW} \leftarrow \quad \rightarrow \quad \frac{V^2}{50} = 10^{-10} \times 10^{-3}$

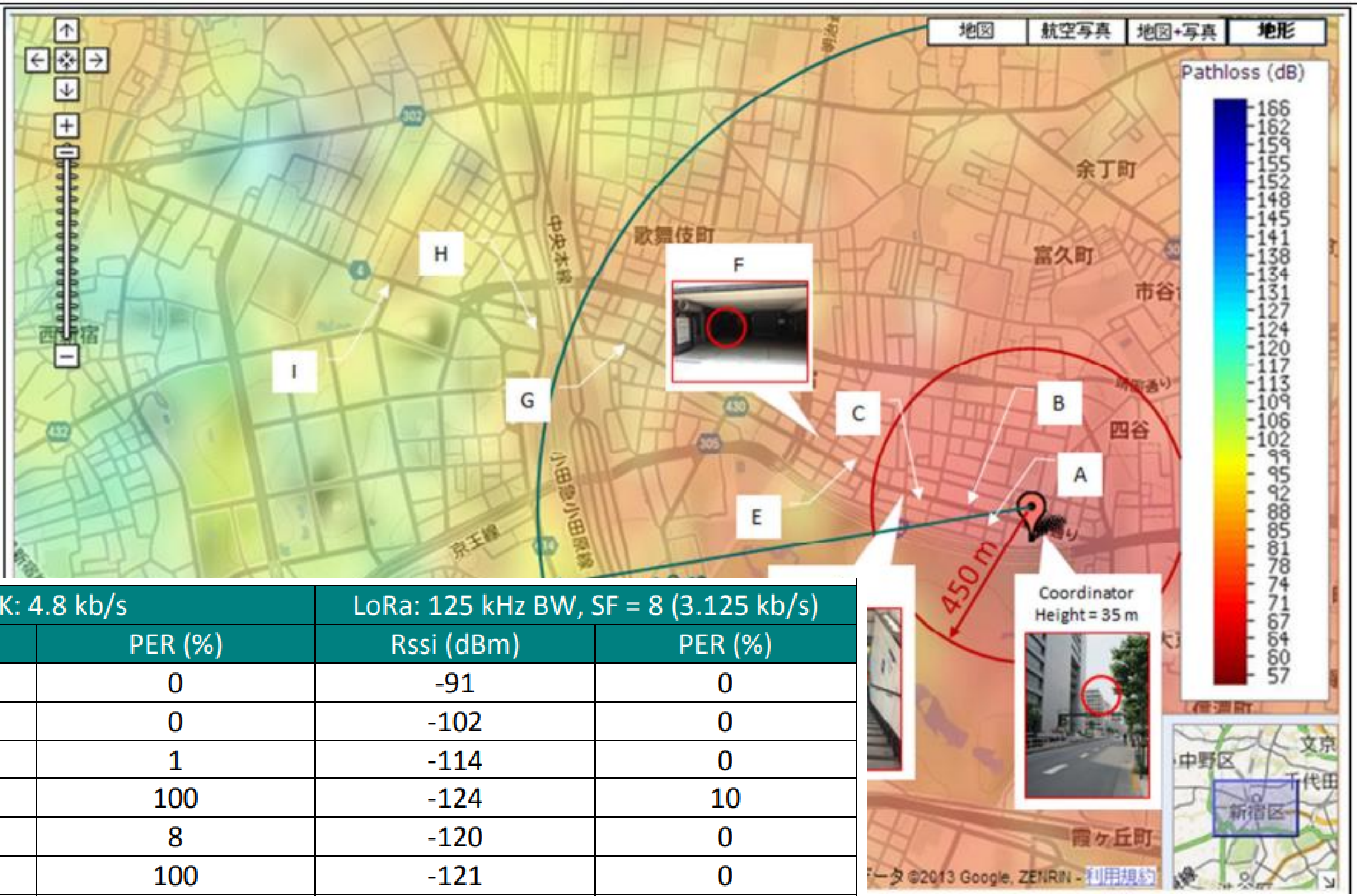
$V = \sqrt{50 \times 10^{-13}} = \sqrt{5} \times 10^{-6} = \underline{\underline{2.\ \mu V}}$

- **<u>For SNR > 0:</u>**
  - RSSI or Packet Strength (dBm) = -164 + RSSI
- **<u>For SNR < 0:</u>**
  - RSSI or Packet Strength (dBm) = -164 + PacketRSSI + 0.25*PacketSNR

Key Properties of LoRa

- **Scalable bandwidth:** LoRa modulation is both bandwidth and frequency scalable. It can be used for both narrowband frequency hopping and wideband direct sequence applications.
- **Constant Envelope / Low-Power** : Similar to FSK, LoRa is a constant envelope modulation scheme which means that the same low-cost and low-power high-efficiency PA stages can be re-used without modification.
- **High Robustness**: Asynchronous nature a LoRa signal is very resistant to both in-band and out-of-band interference mechanisms.
- **Multipath / fading resistant** : The chirp pulse is relatively broadband and thus LoRa offers immunity to multipath and fading, making it ideal for use in urban and suburban environments, where both mechanisms dominate.
- **Doppler Resistant** : Doppler shift causes a small frequency shift in the LoRa pulse which introduces a relatively negligible shift in the time axis of the baseband signal. This frequency offset tolerance mitigates the requirement for tight tolerance reference clock sources. *Ideally suited for satellite communication*.
- **Long Range Capability** : For a fixed output power and throughput, the link budget of LoRa exceeds that of conventional FSK

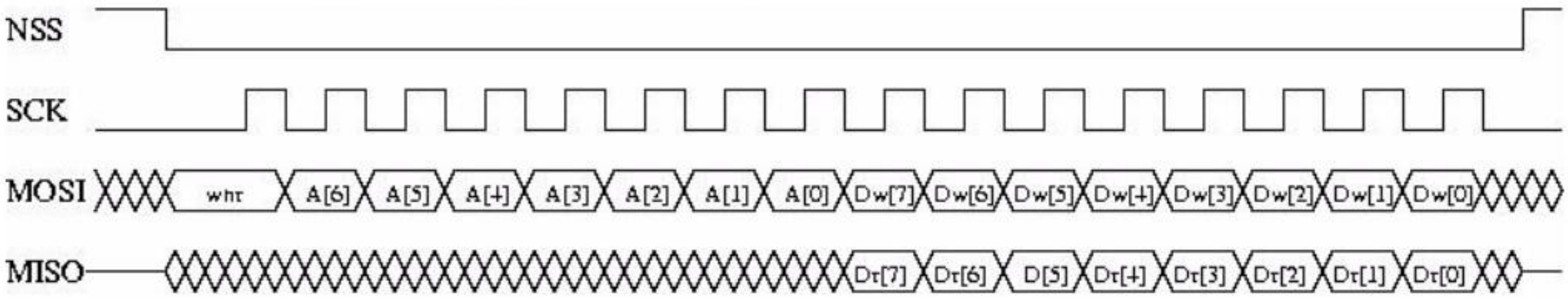
Network Trial



Ref. #	Distance (m)	2-FSK: 4.8 kb/s		LoRa: 125 kHz BW, SF = 8 (3.125 kb/s)	
		Rssi (dBm)	PER (%)	Rssi (dBm)	PER (%)
A	80	-97	0	-91	0
B	150	-100	0	-102	0
C	280	-112	1	-114	0
D	330	-	100	-124	10
E	480	-118	8	-120	0
F	560	-	100	-121	0
G	1180	-	100	-112	0
H	1350	-	100	-126	10
I	1750	-	100	-127	100

Figure 9: Shinjuku Urban Range Test

SPI Access



The SPI interface gives access to the configuration register via a synchronous full-duplex protocol corresponding to CPOL = 0 and CPHA = 0 in Motorola/Freescale nomenclature. Only the slave side is implementation.

- SINGLE access: an address byte followed by a data byte is sent for a write access whereas an address byte is sent and a read byte is received for the read access. The NSS pin goes low at the beginning of the frame and goes high after the data byte.
- BURST access: the address byte is followed by several data bytes. The address is automatically incremented internally between each data byte. This mode is available for both read and write accesses. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.
- FIFO access: if the address byte corresponds to the address of the FIFO, then succeeding data byte will address the FIFO. The address is not automatically incremented but is memorized and does not need to be sent between each data byte. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer