

SI-2024

Intro to CubeSat & Satellite Communication



Introduction to CMOS VLSI Design

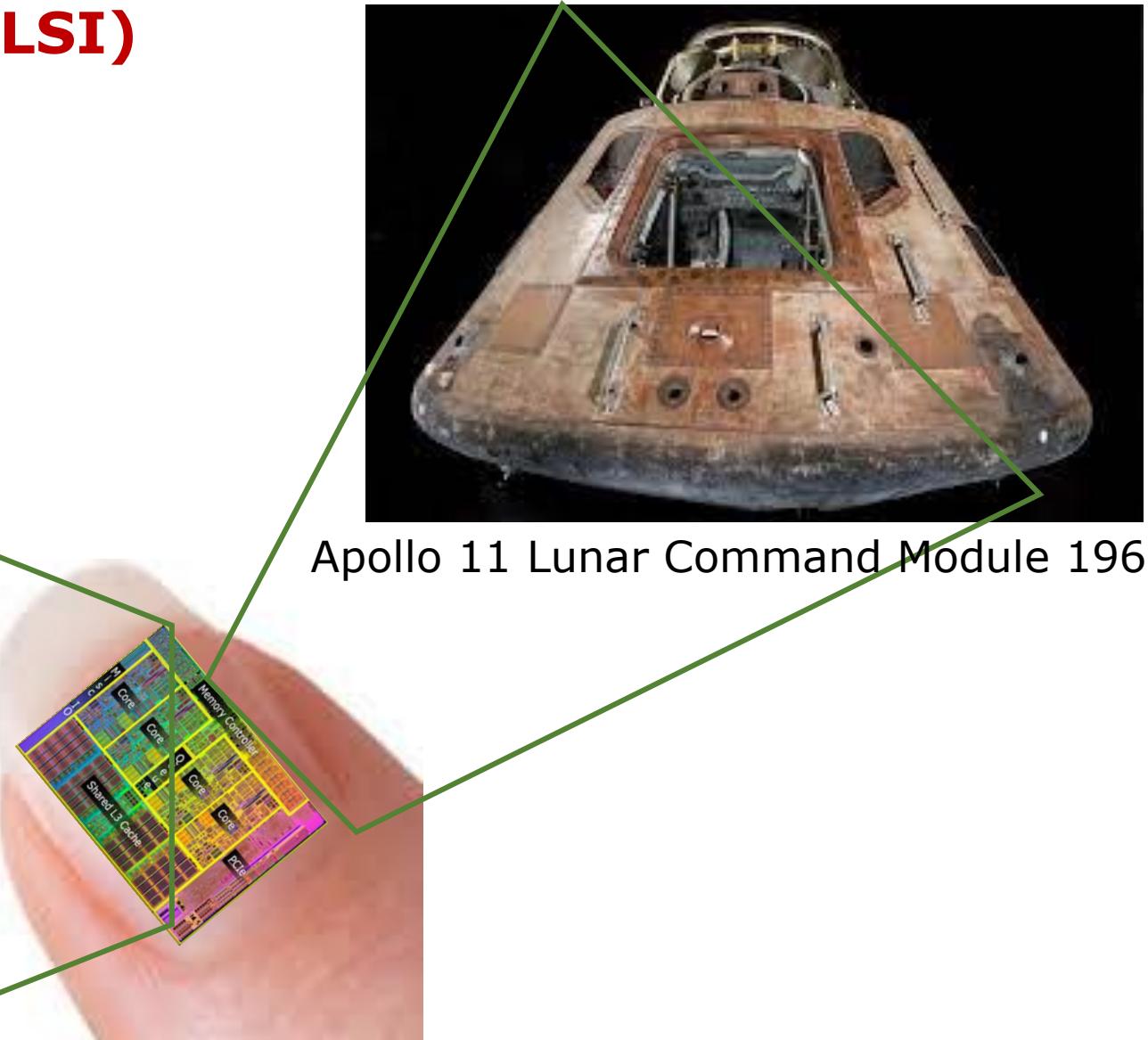
Saroj Rout

Summer Internship
July 1, 2024

► Very Large Scale Integration (VLSI)

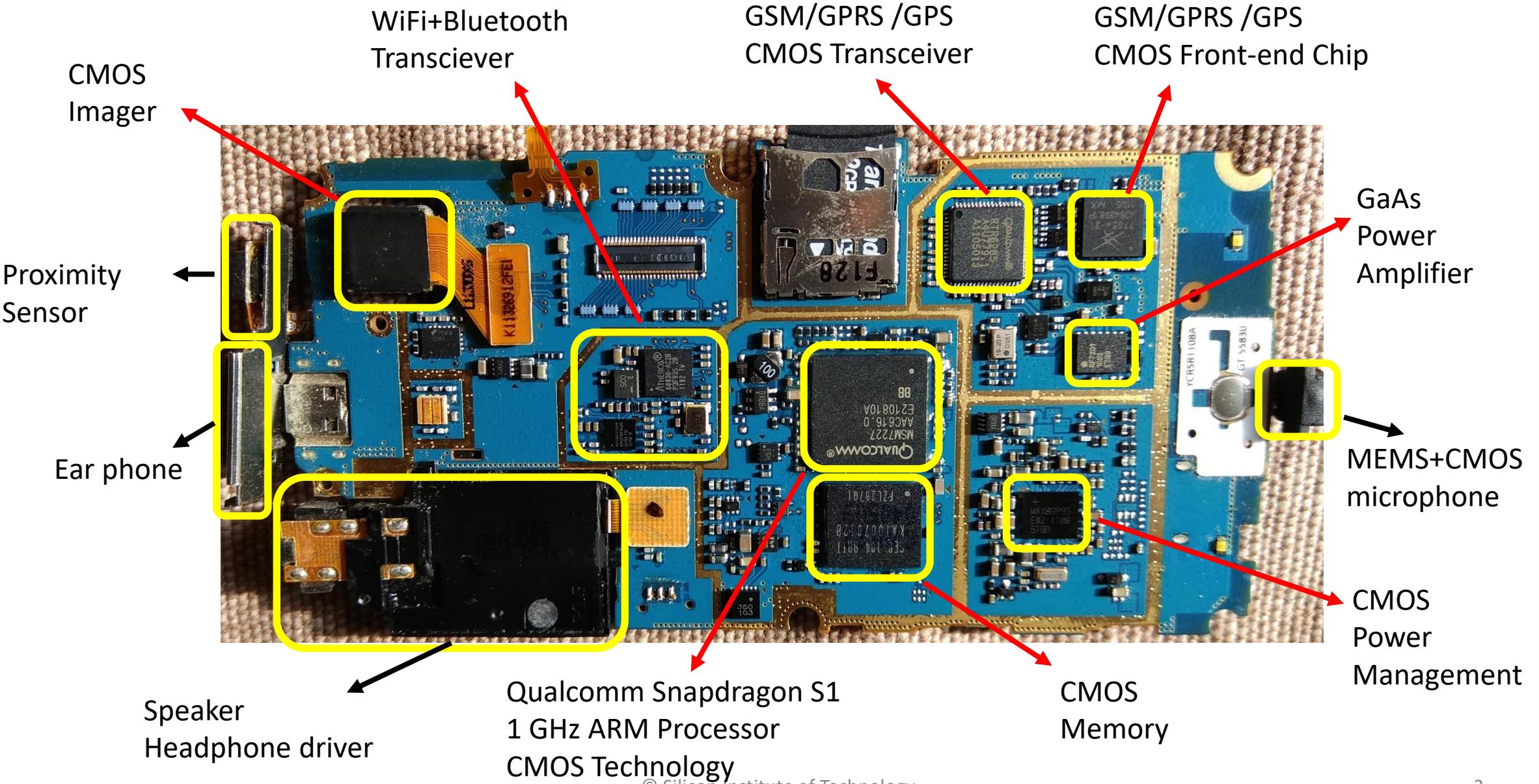


Mainframe computer of the 70s

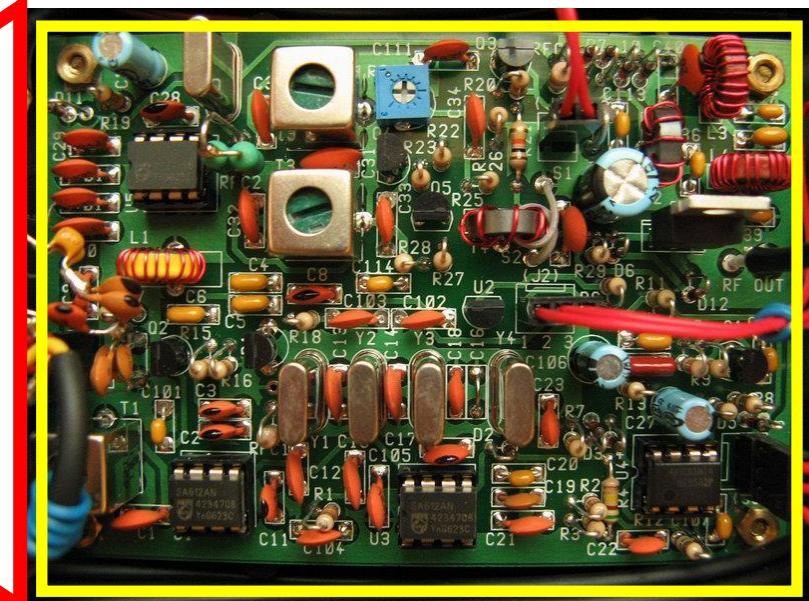
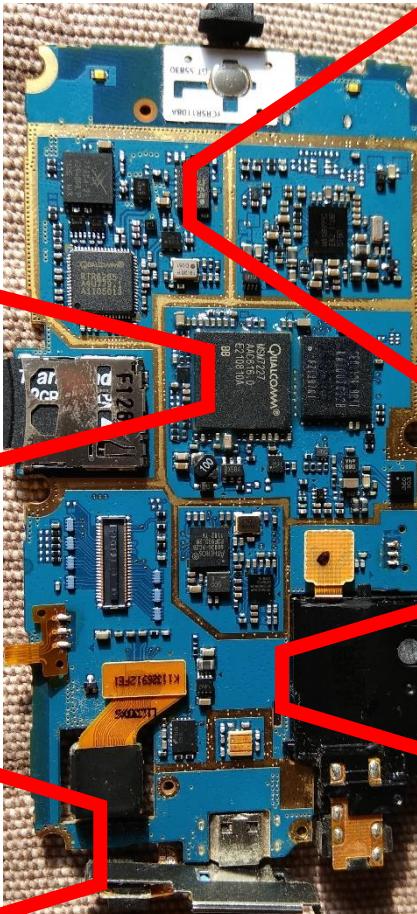
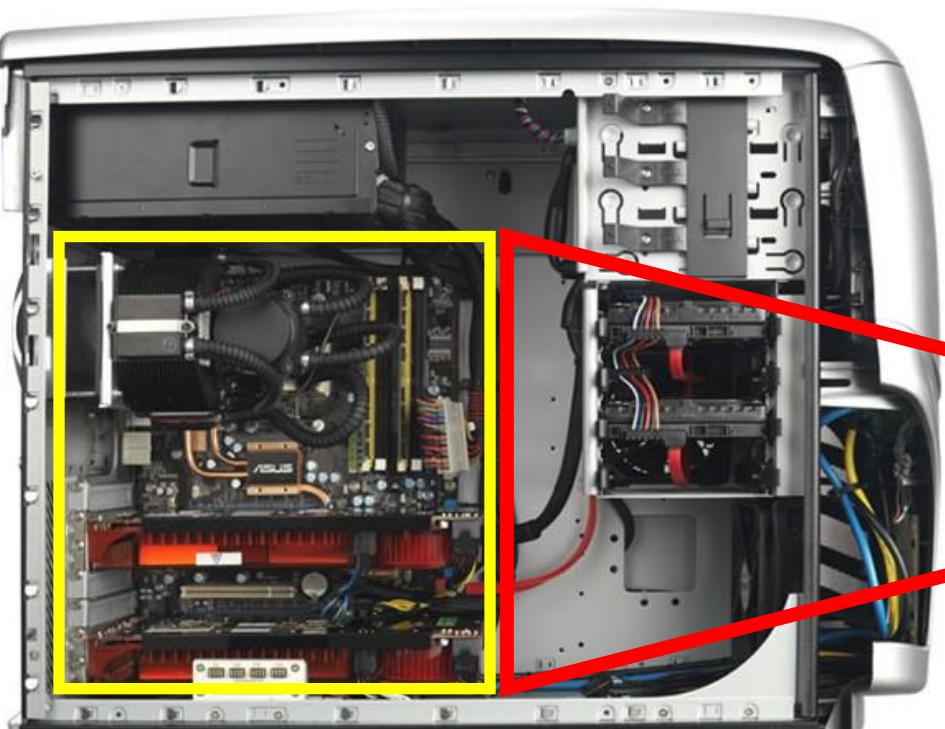


Today

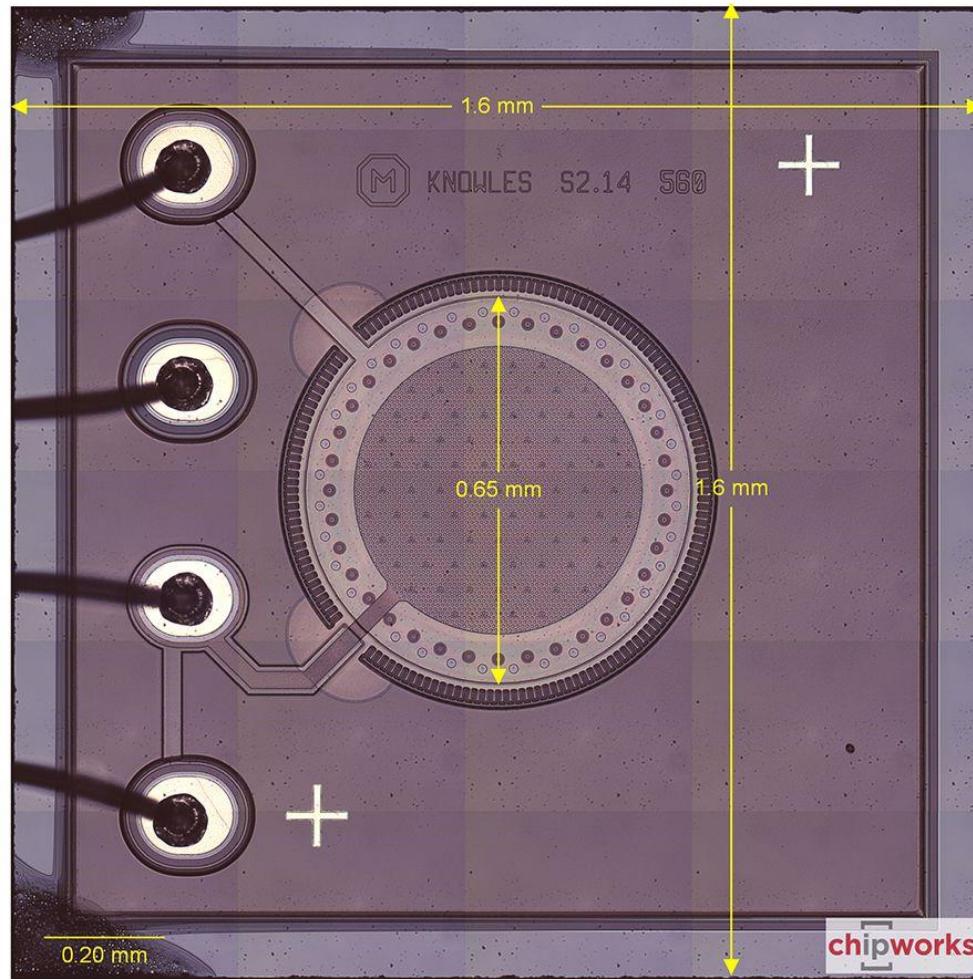
► Anatomy of an Electronic System: Mobile Phone



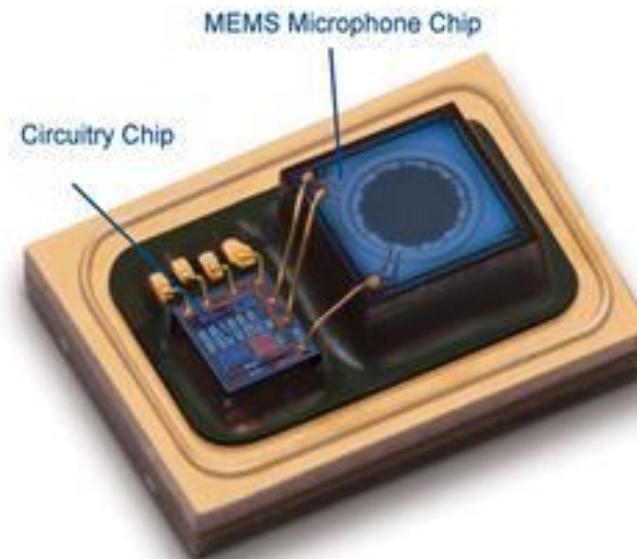
► Very Large Scale Integration (VLSI)



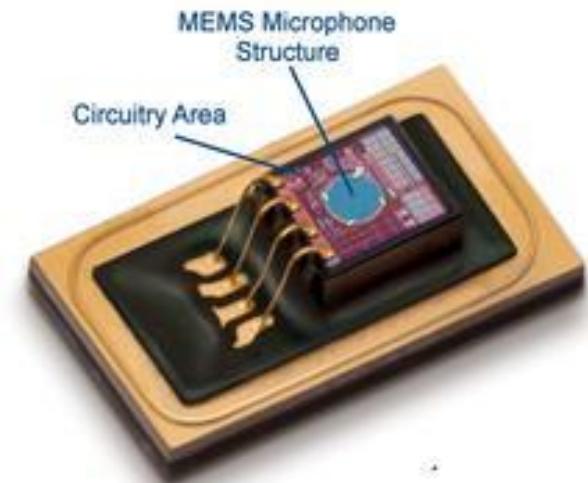
► Capacitive MEMS Microphone



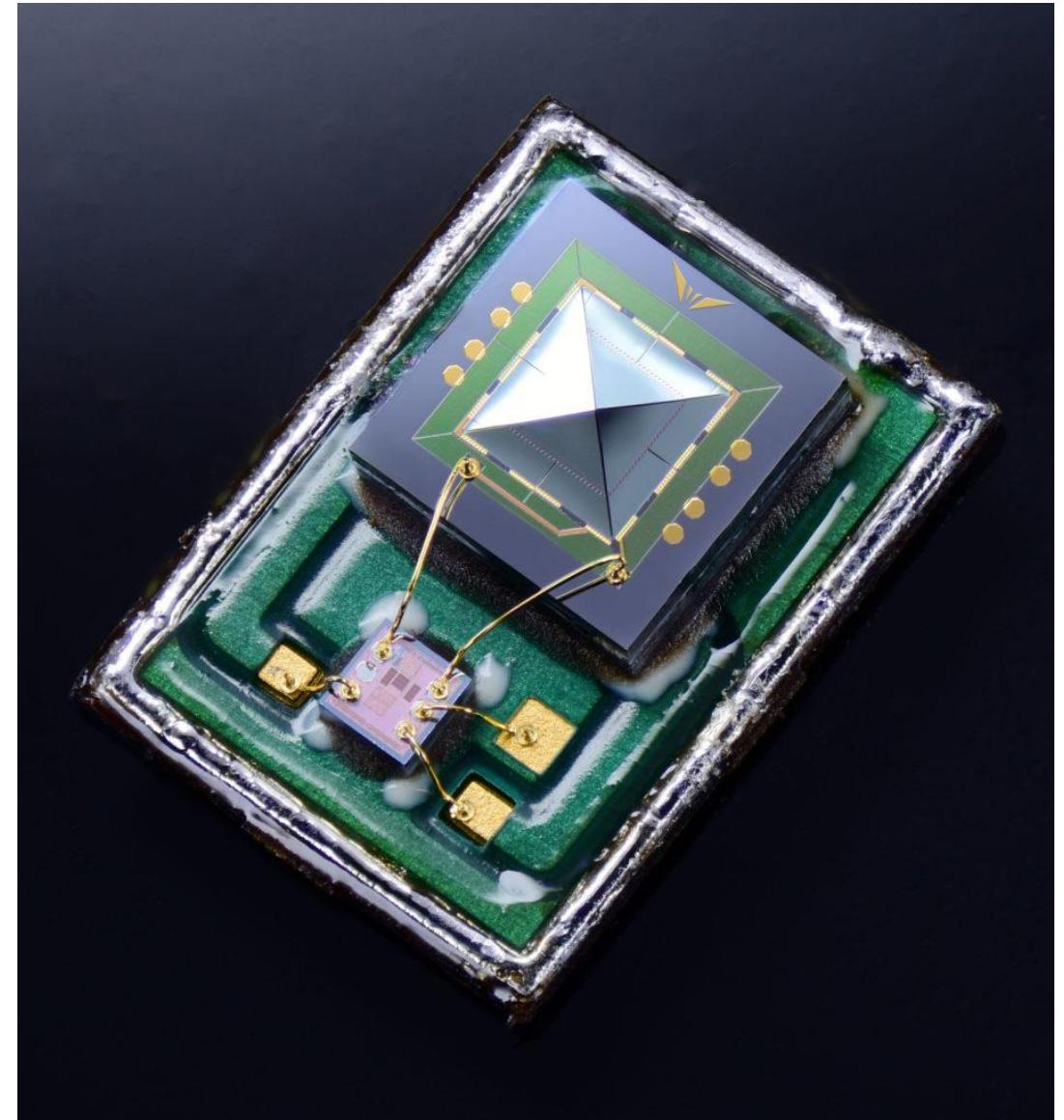
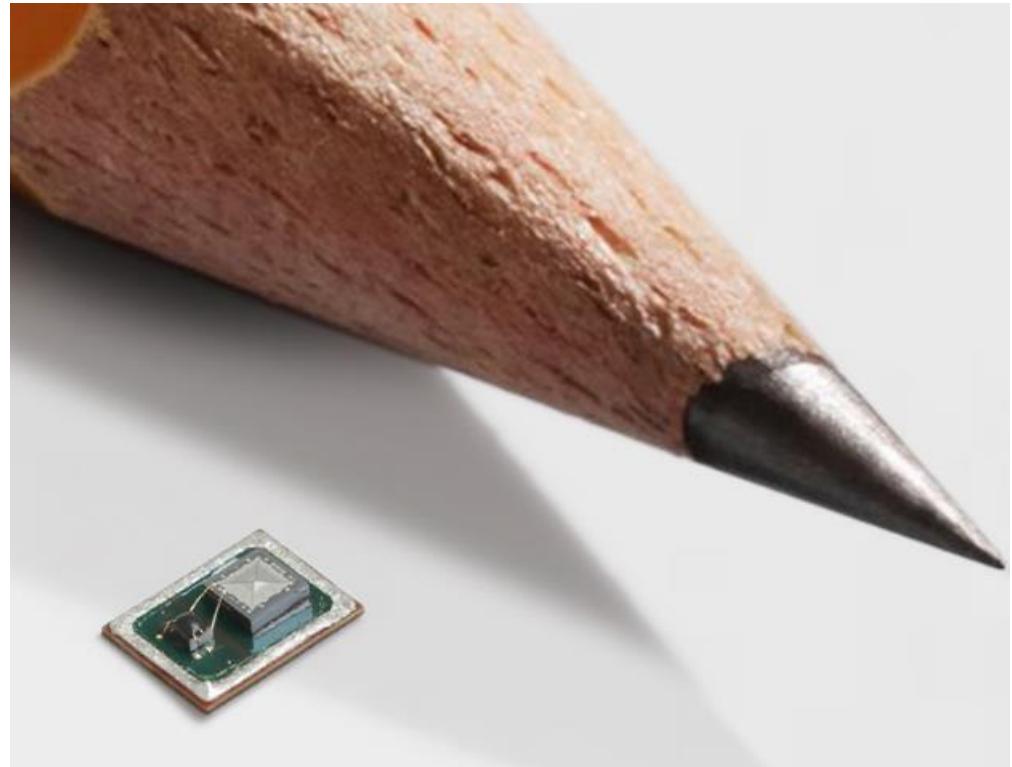
Akustica 2-chip MEMS Microphone



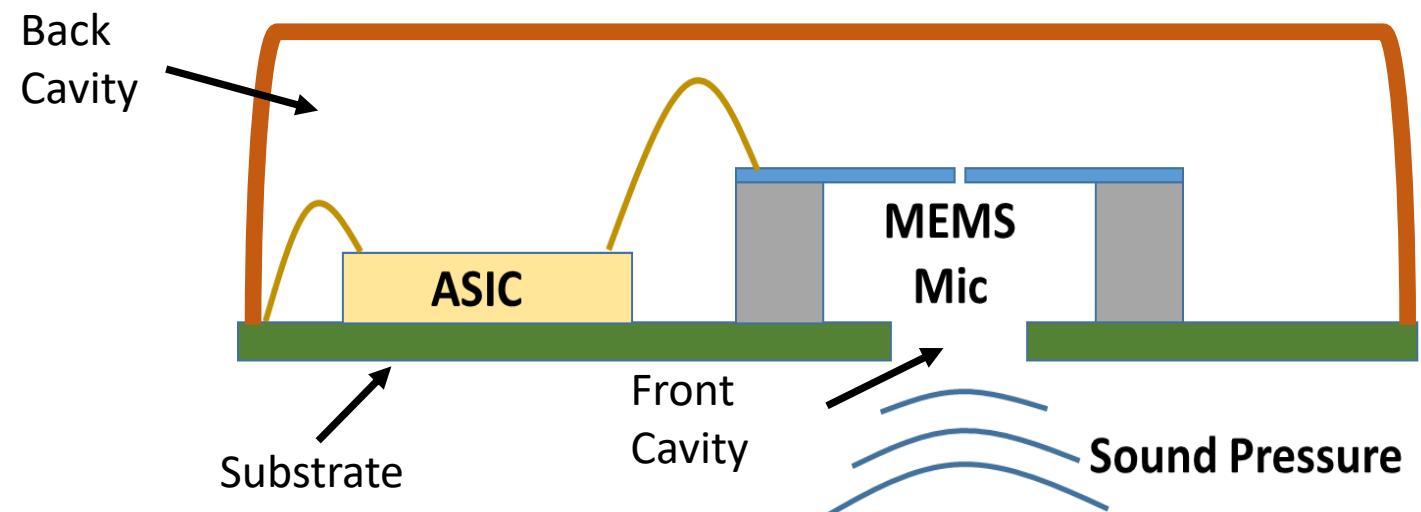
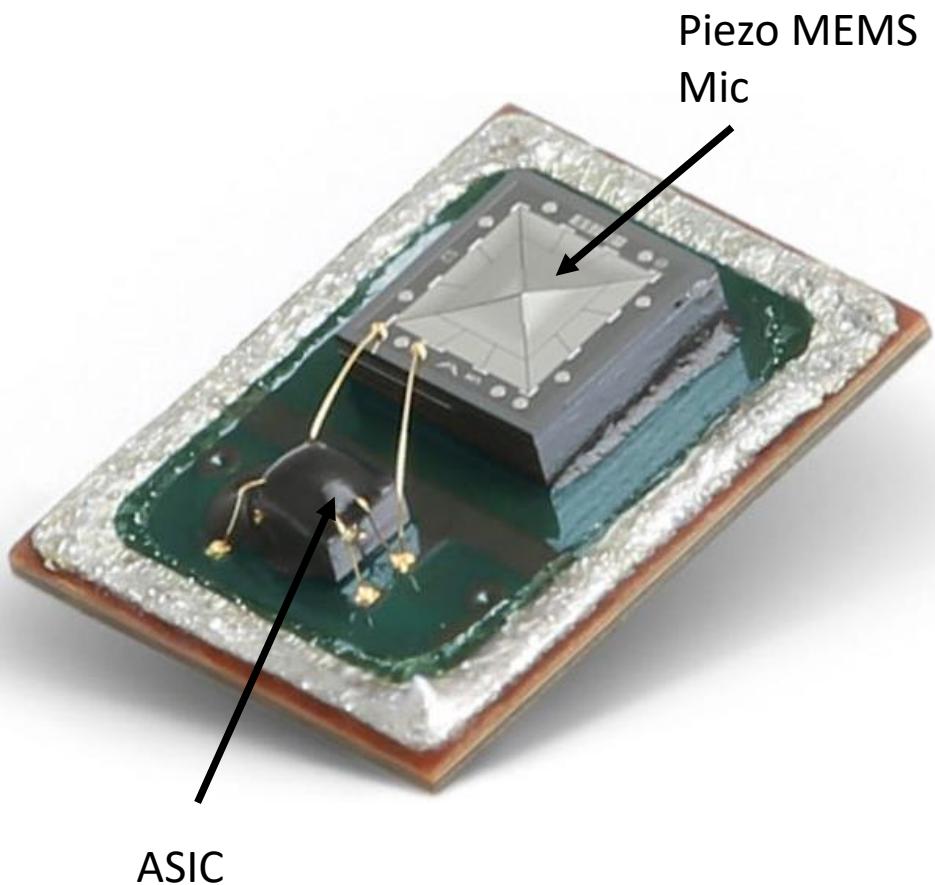
Akustica Monolithic MEMS Microphone



► Piezoelectric MEMS Microphone



► Cross-section



► Inertial Measurement Unit (IMU)/ Gyroscope

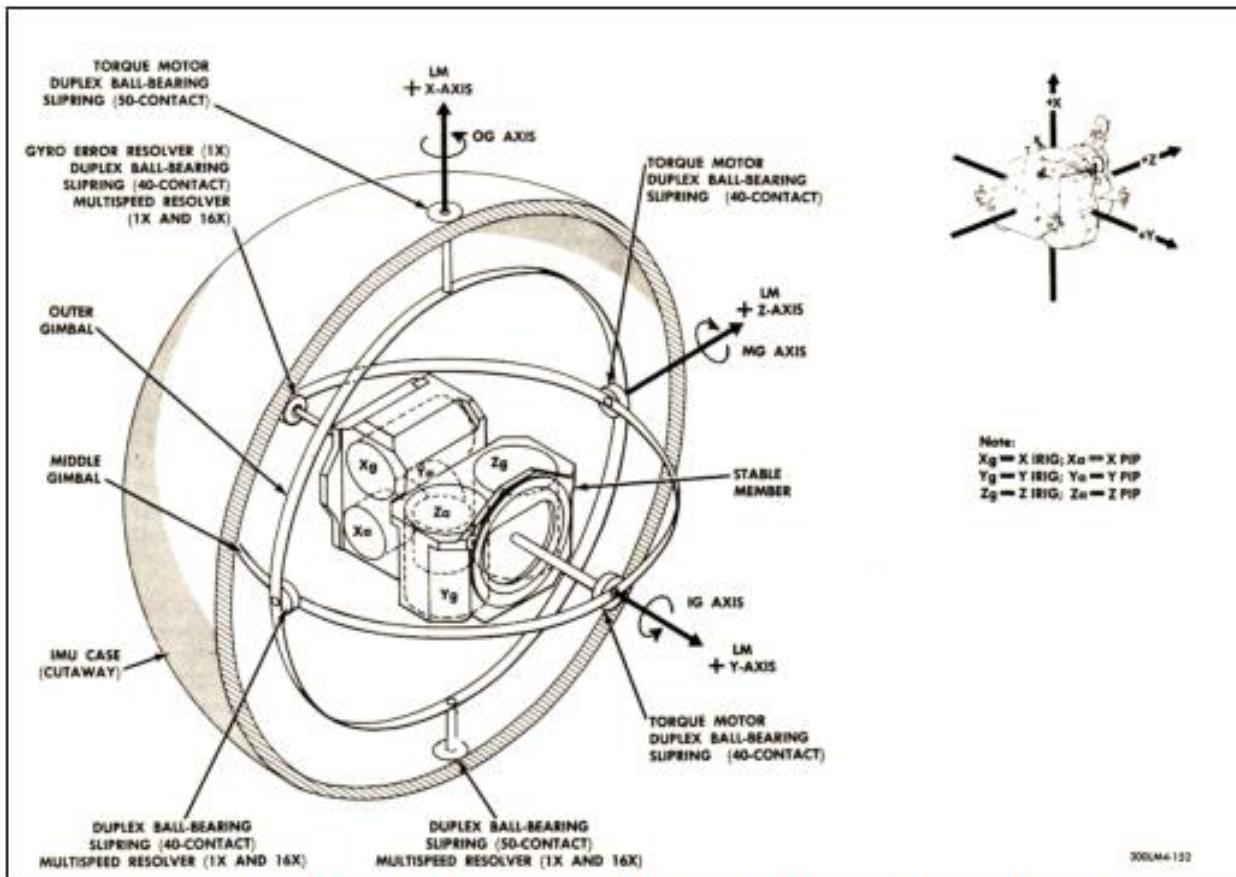


Figure 1.2: (left) Platform-type IMU utilized in the lunar module flight control during the Apollo missions. Three orthogonal accelerometers and three orthogonal gyroscopes are placed in a platform stabilized by a gimbal structure [10]. (right) IMU utilized in the LGM-118 peacemaker intercontinental ballistic missile [11].

► MEMS/CMOS Gyroscope

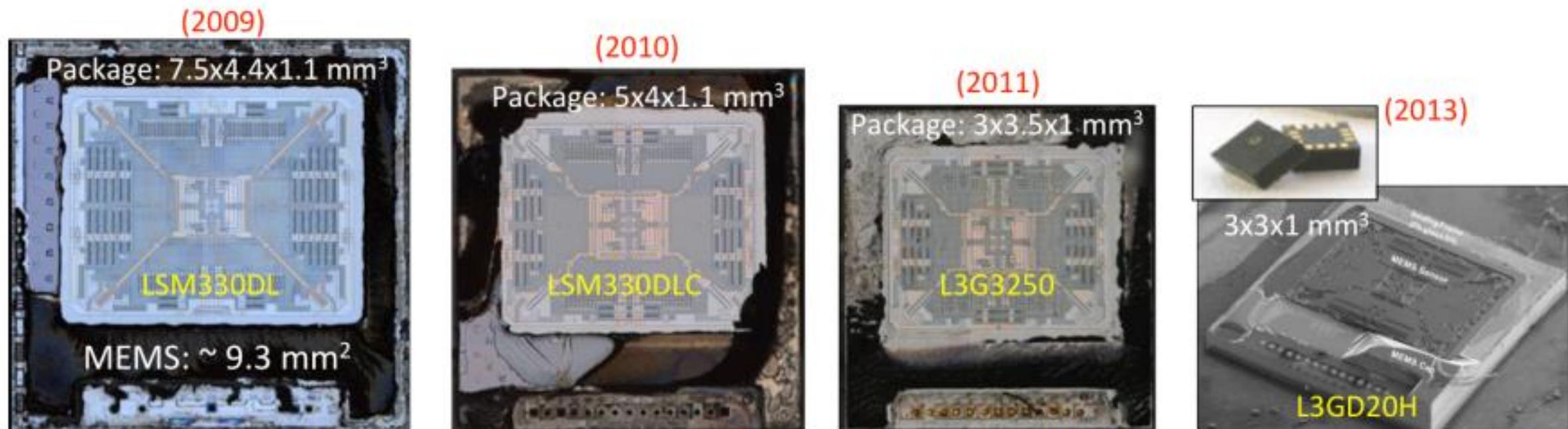


Figure 1.6: Evolution of STmicroelectronics tri-axial gyroscopes. Package size volume reduced by 4X in 4 years.

► MEMS/CMOS Gyroscope

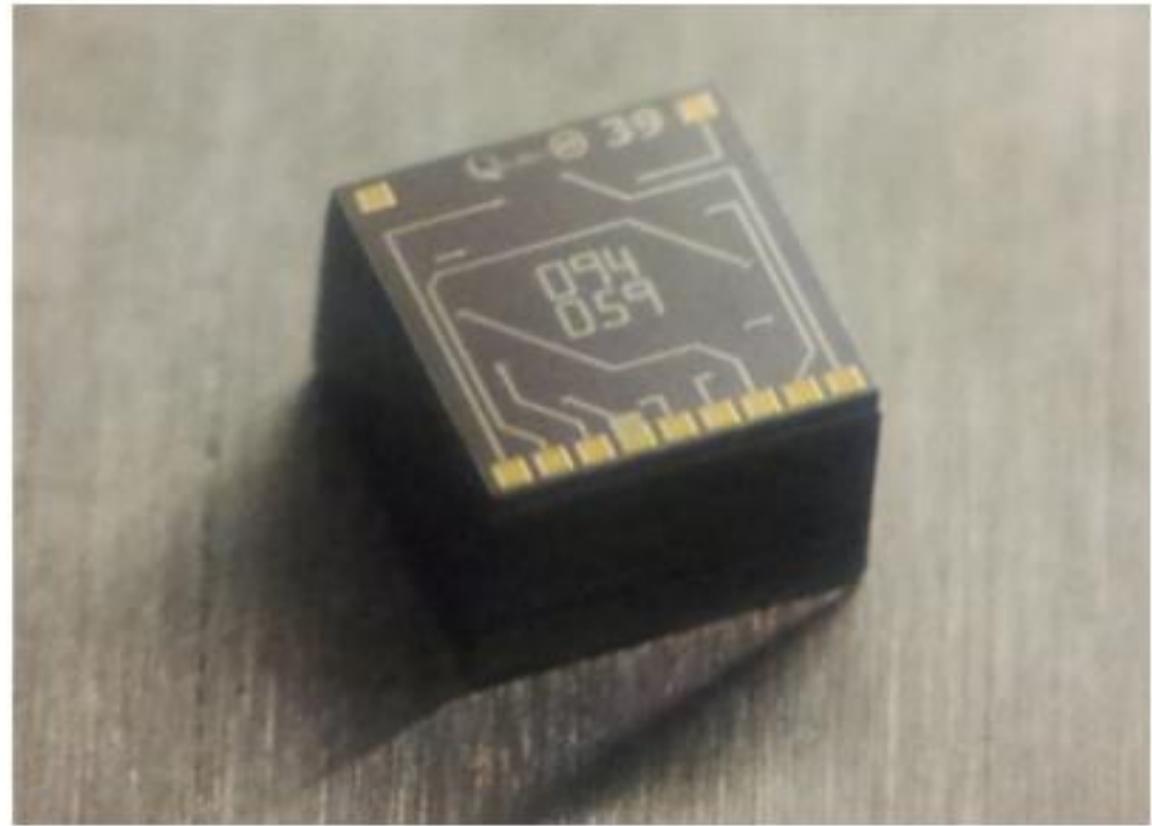
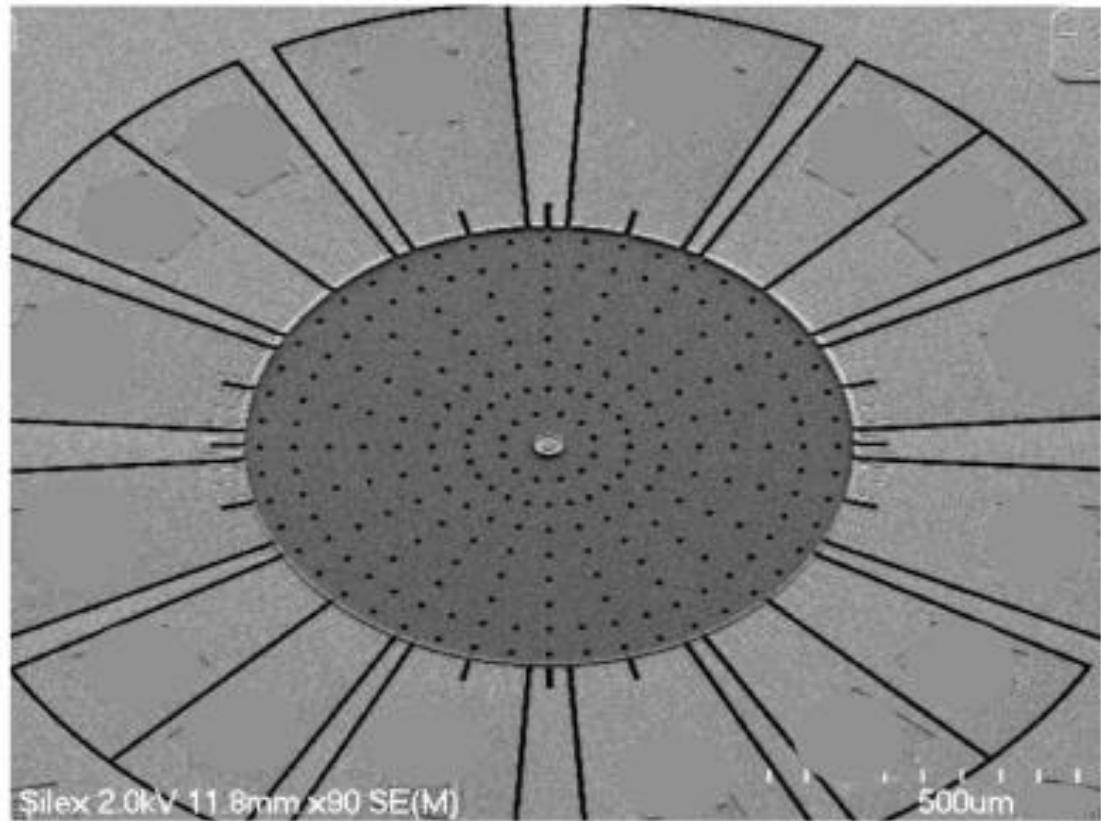
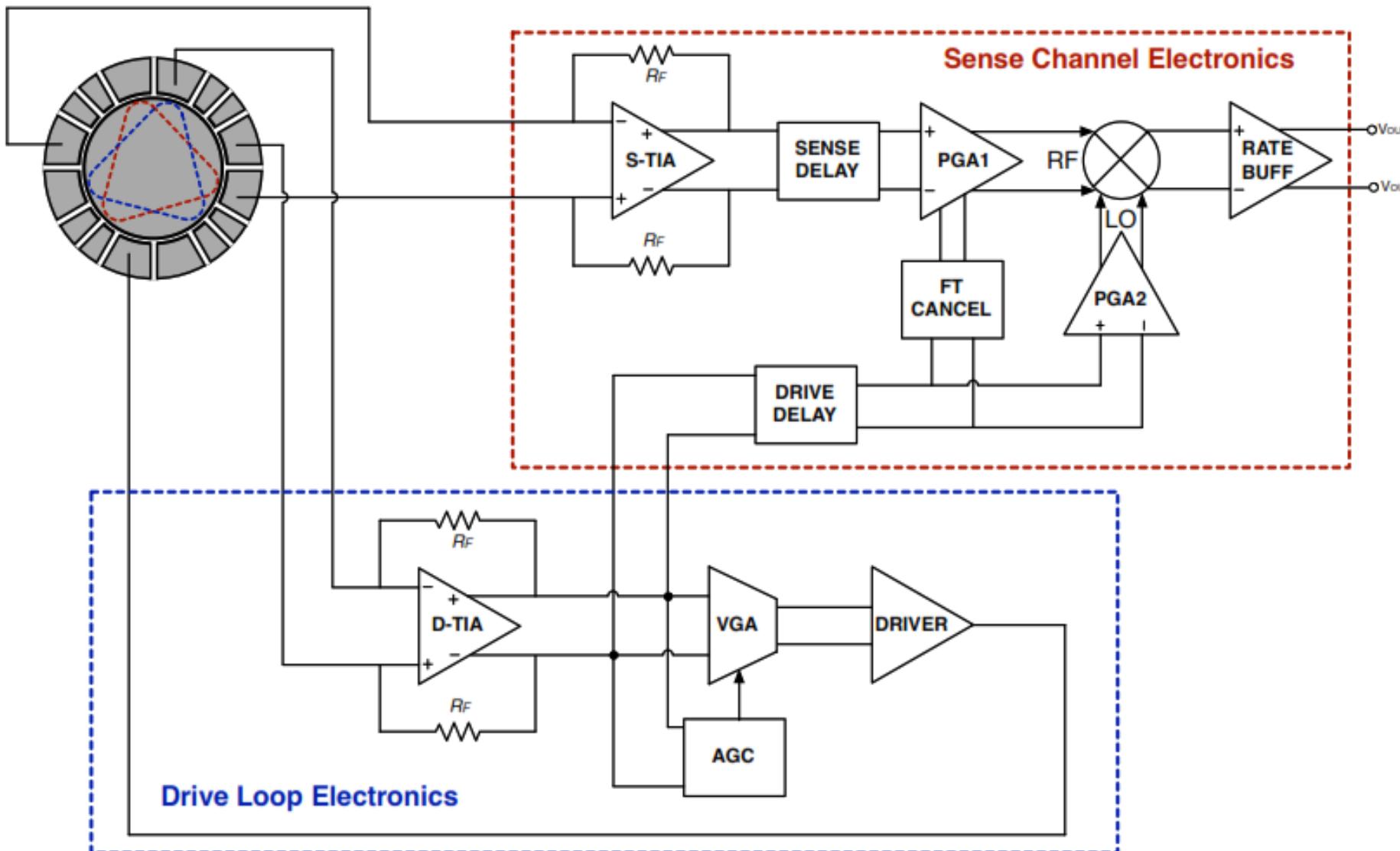
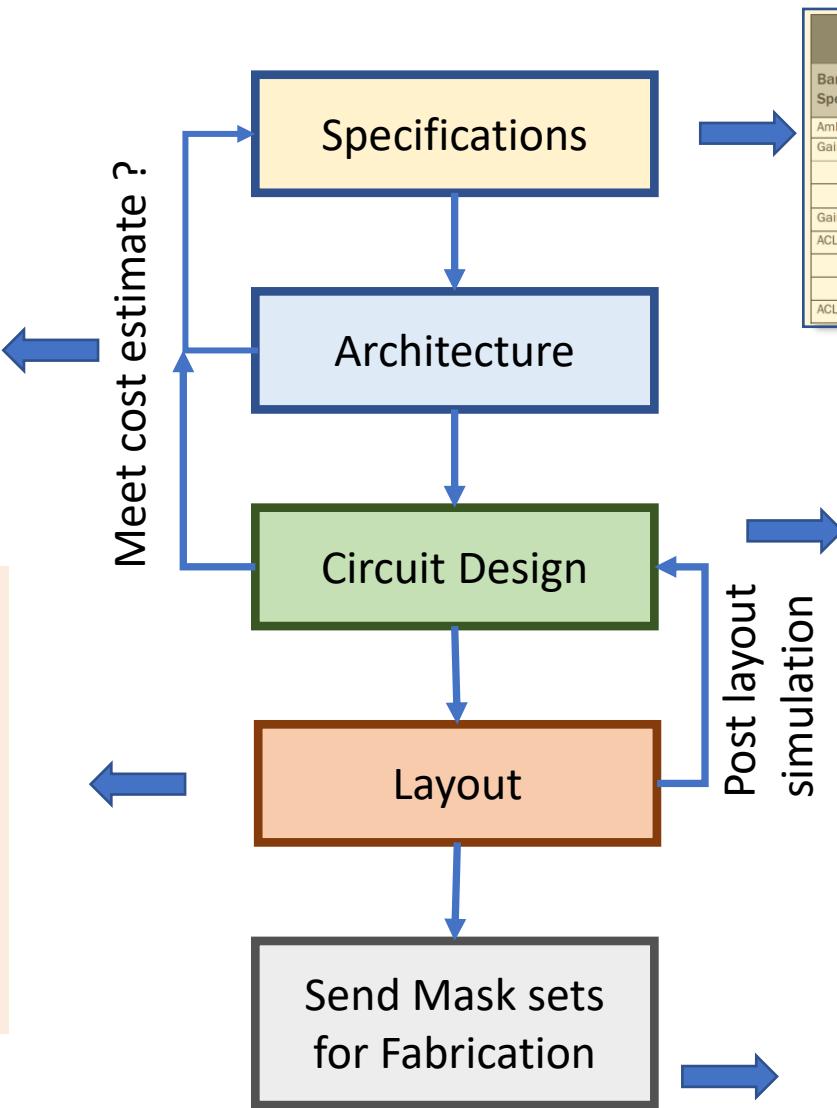
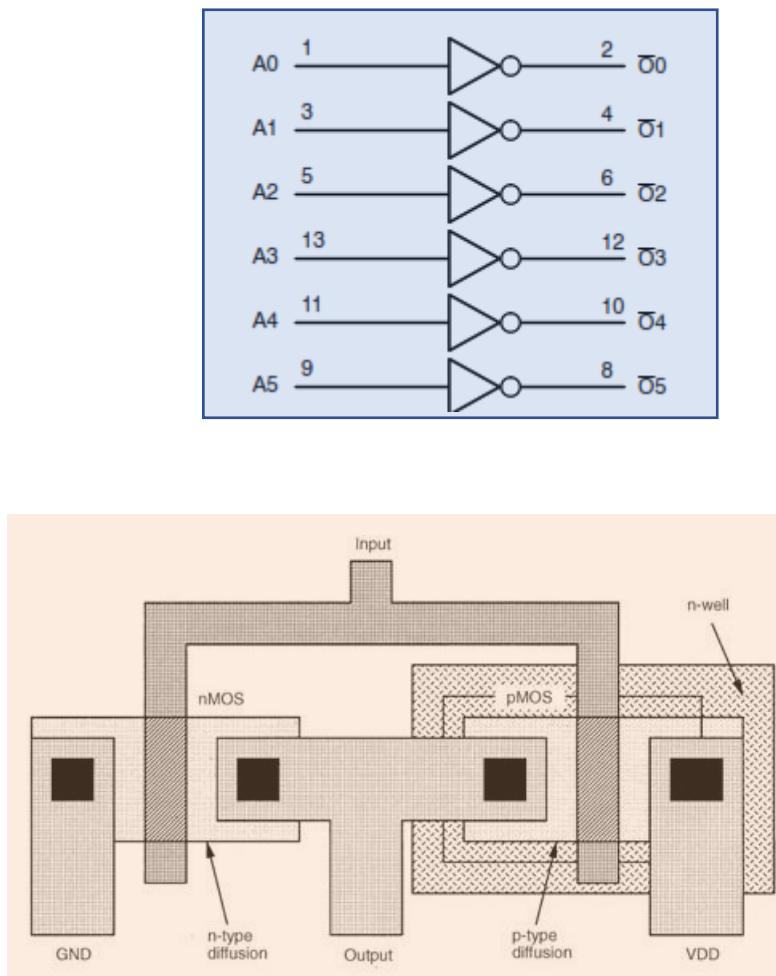


Figure 4.22: (left) SEM view of 800 μm BAW disk gyroscope implemented with the HARPSS™ process in a 40 μm -thick substrate. (right) Vacuum-packaged BAW disk gyroscope singulated die.

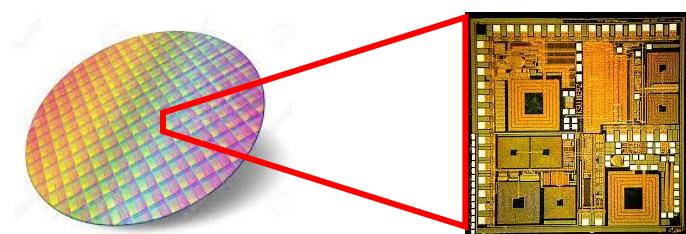
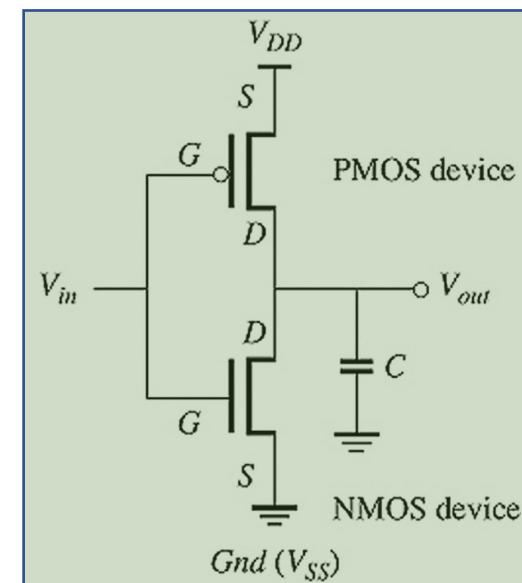
► Analog Front-End (AFE)



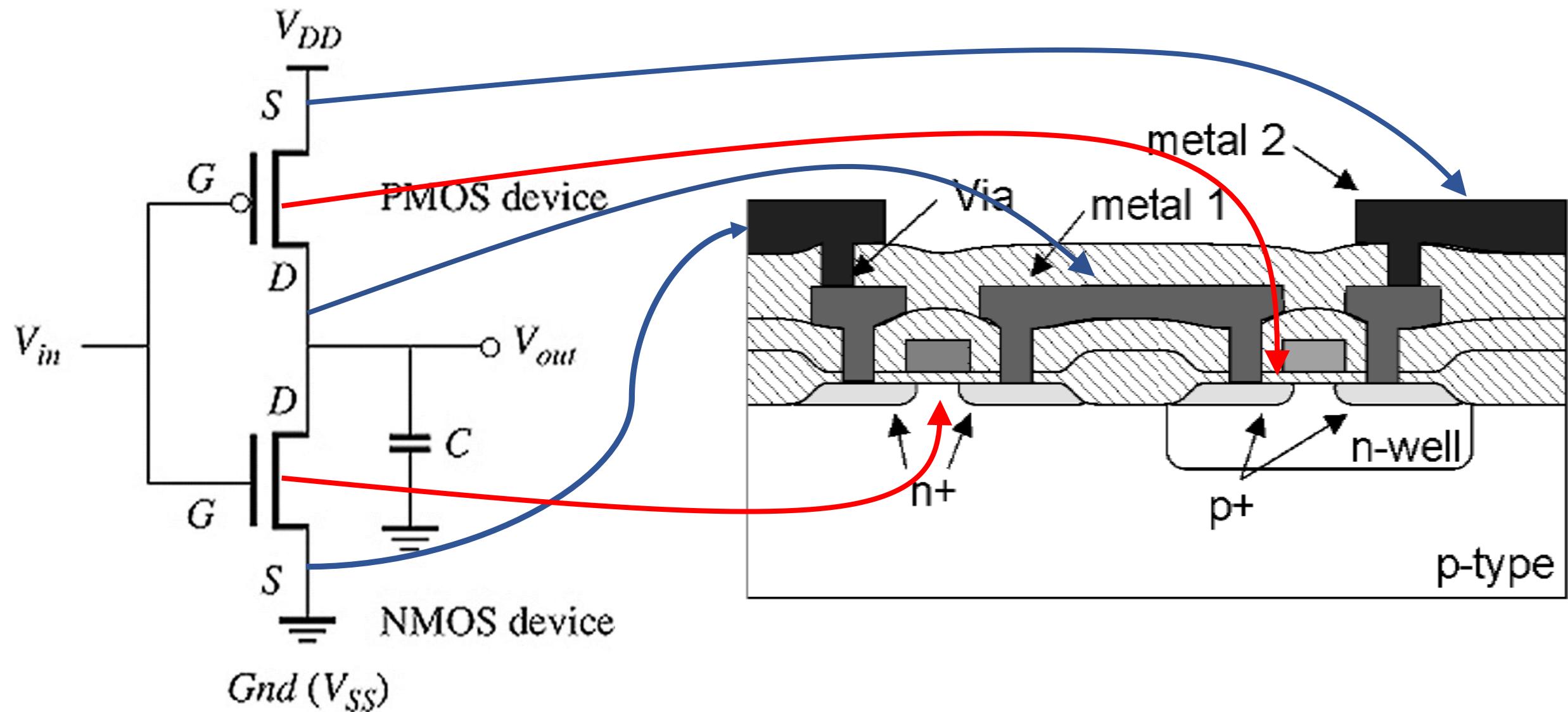
► Custom (Analog/Digital) Integrated Circuit (IC) Design Flow



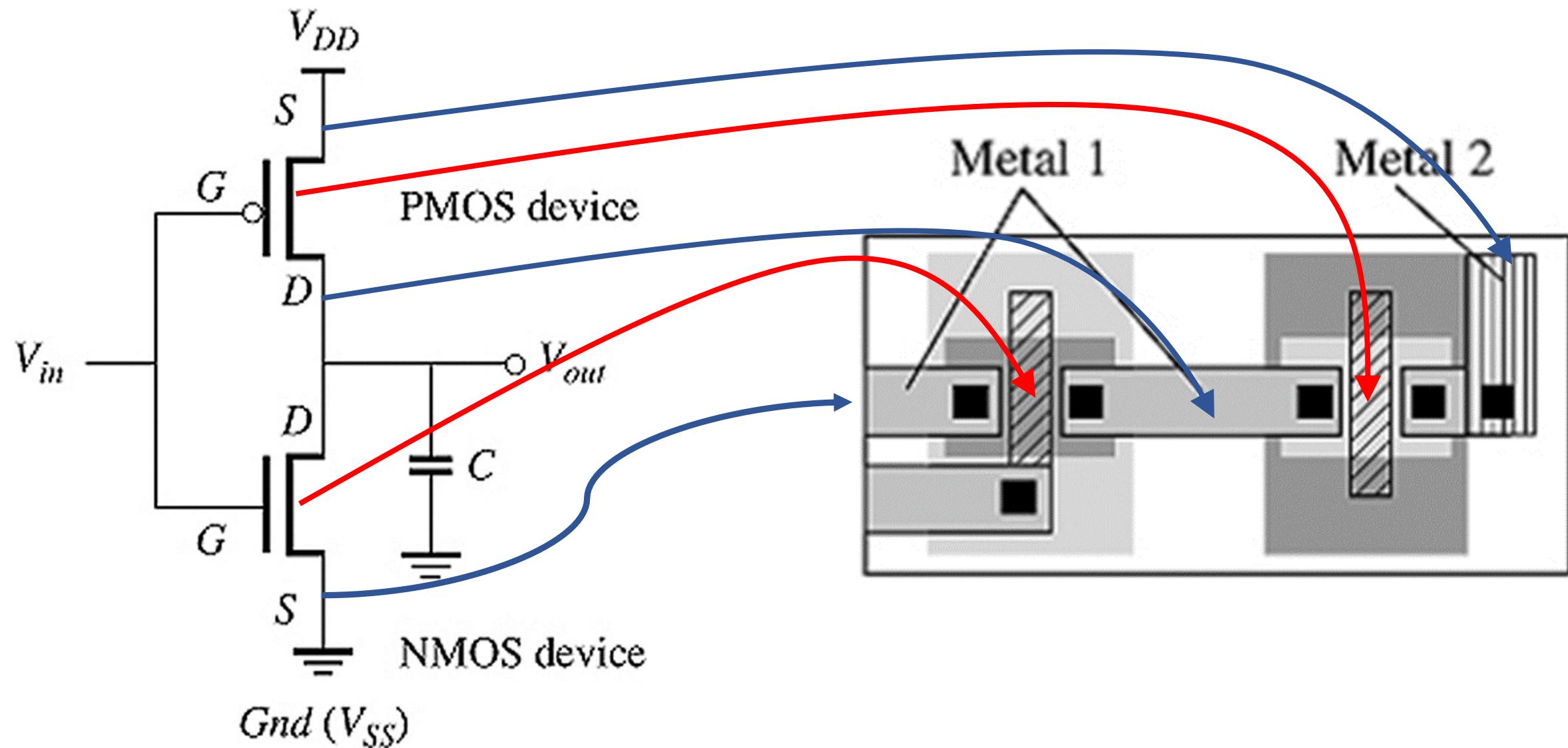
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Band 1 Electrical Specifications					
Ambient Temperature	-30	+25	+85	°C	T=+25°C, V _{CC} =V _{BAT} =+3.4V, V _{EN} =+1.8V, Rel 99 Modulation, and 50Ω system, unless otherwise specified.
Gain	25	27		dB	HPM, P _{OUT} =28.0dBm
	15	19		dB	MPM, P _{OUT} ≤19.0dBm
	13 ¹	16		dB	LPM, P _{OUT} ≤8.0dBm
Gain Linearity	±1.0			dB	HPM, 19.0dBm≤P _{OUT} ≤28.0dBm
ACLR - 5MHz Offset	-40			dBc	HPM, P _{OUT} =28.0dBm
	-42			dBc	MPM, P _{OUT} =19.0dBm
	-42			dBc	LPM, P _{OUT} =8.0dBm
ACLR - 10MHz Offset	-53			dBc	HPM, P _{OUT} =28.0dBm



► Schematic to Physical Devices

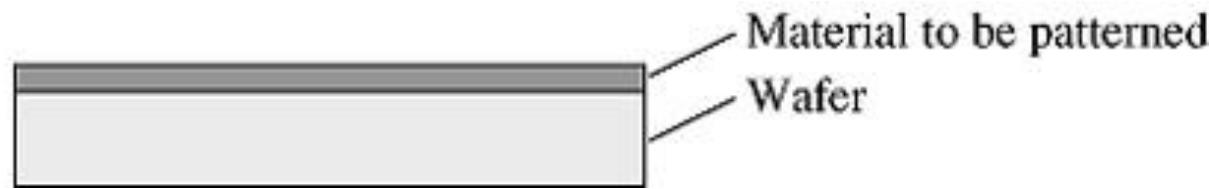


► Circuit to Foundry Masks (Layout)

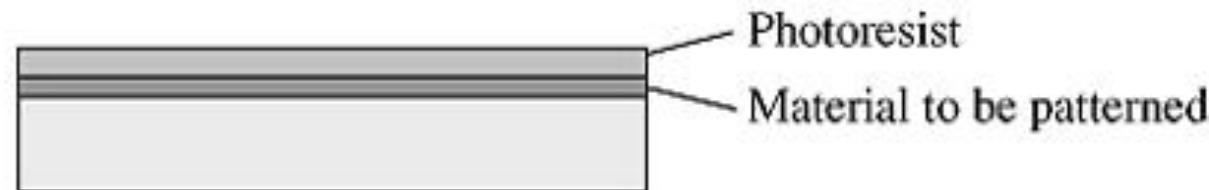


► Material Patterning Steps (1)

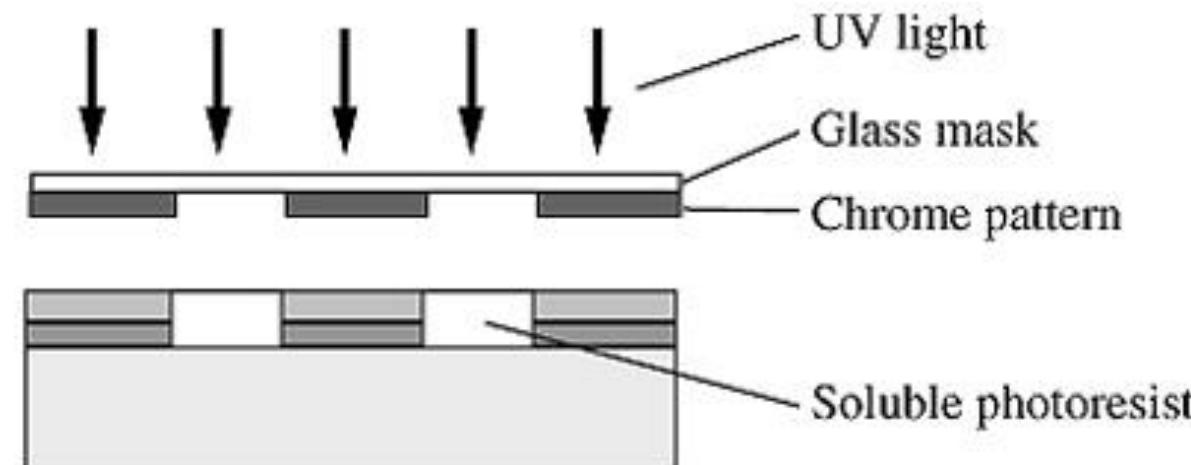
Step 1: Apply material to water



Step 2: Spin on a photoresistive material

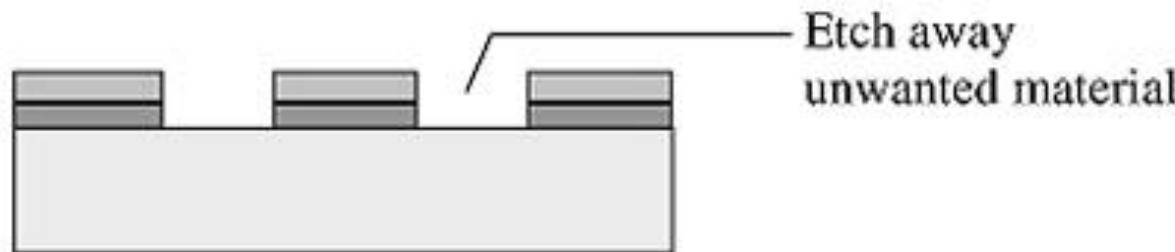


Step 3: Pattern photoresist with UV light through glass mask



► Material Patterning Steps (2)

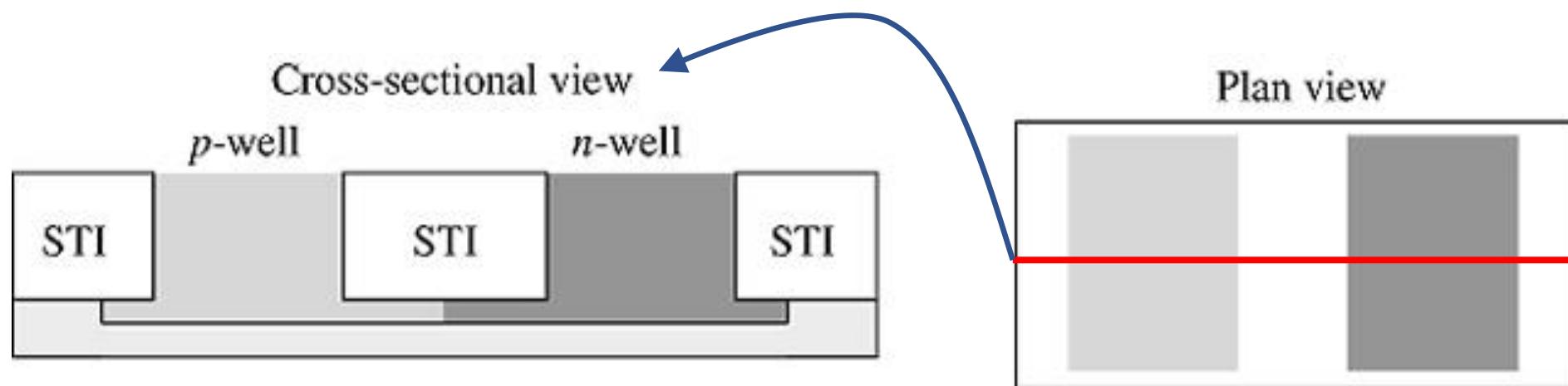
Step 4: Apply specific processing step such as etch, implant, oxidation, after removing soluble photoresist



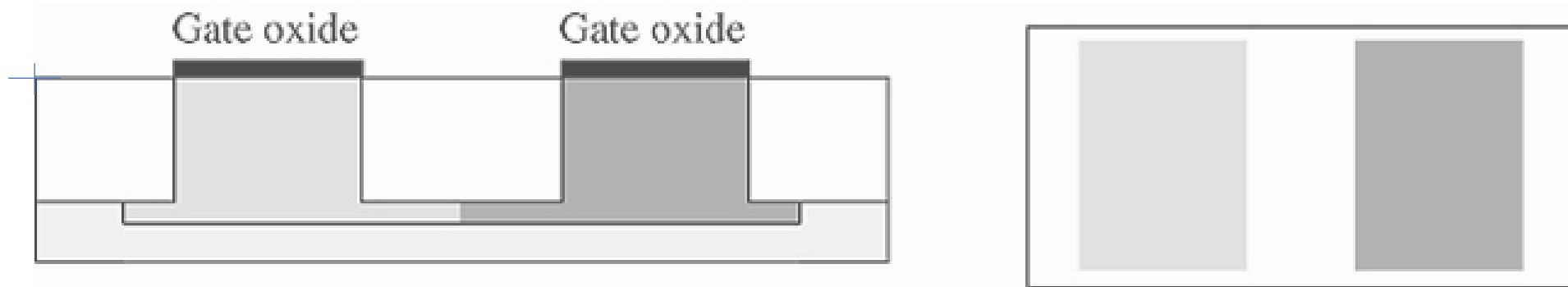
Step 5: Wash off resist



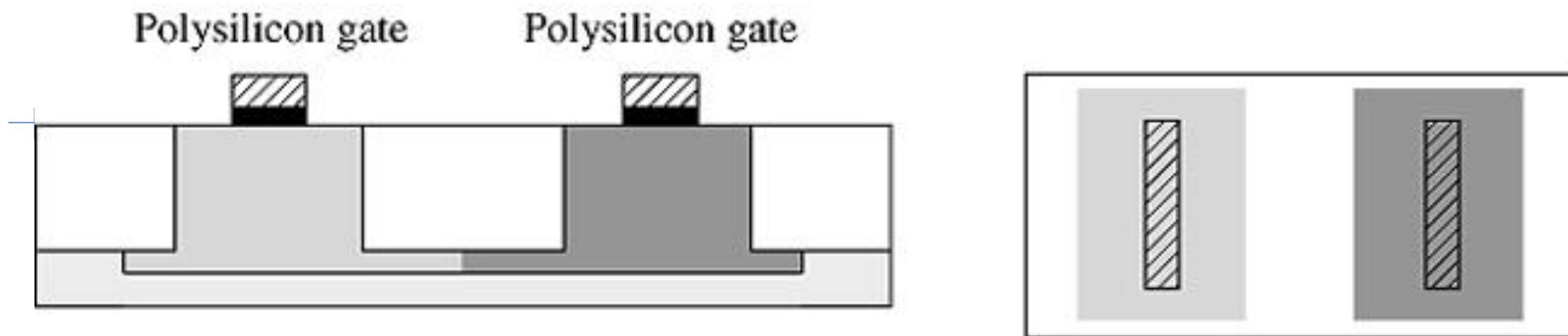
► Foundry Masks (Layout) to Physical Devices



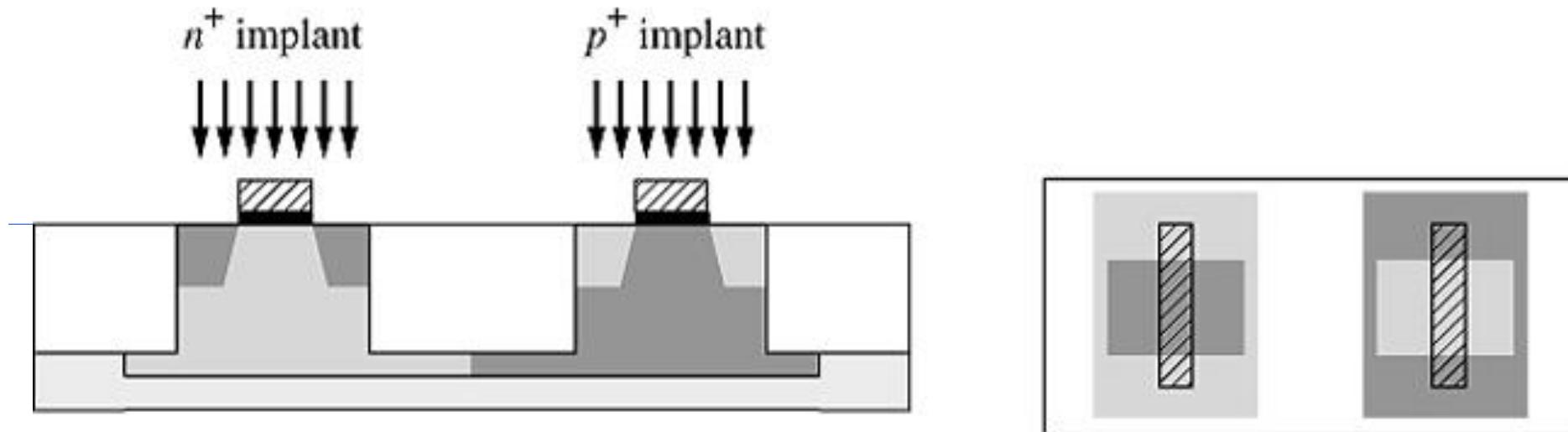
► Foundry Masks (Layout) to Physical Devices (2)



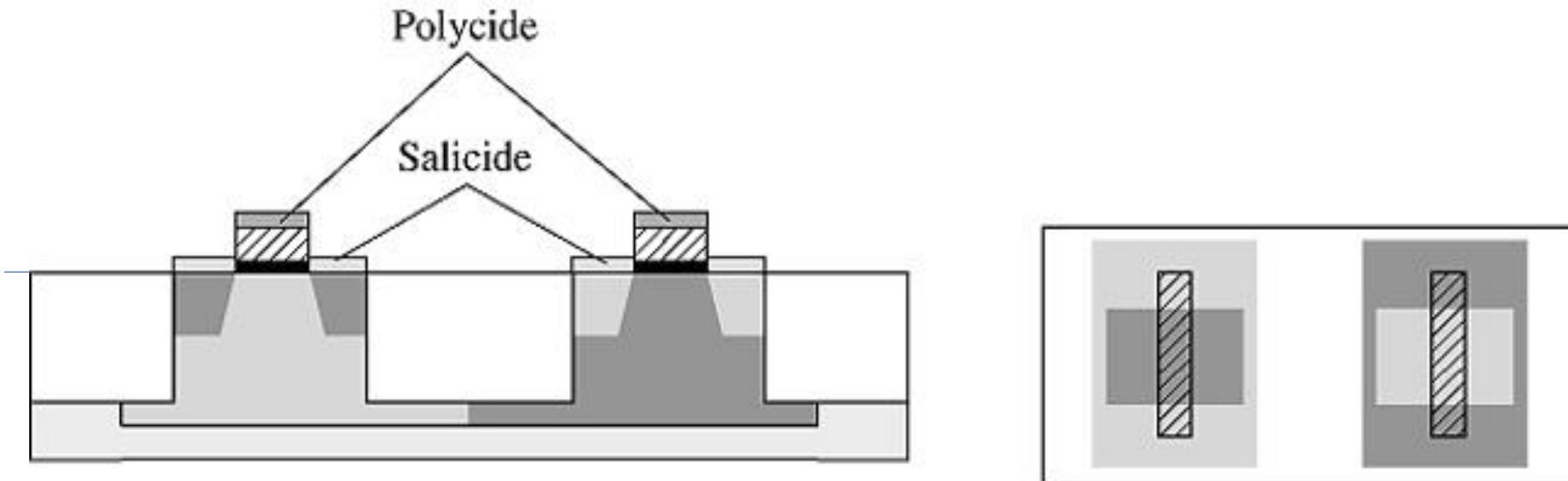
► Foundry Masks (Layout) to Physical Devices (3)



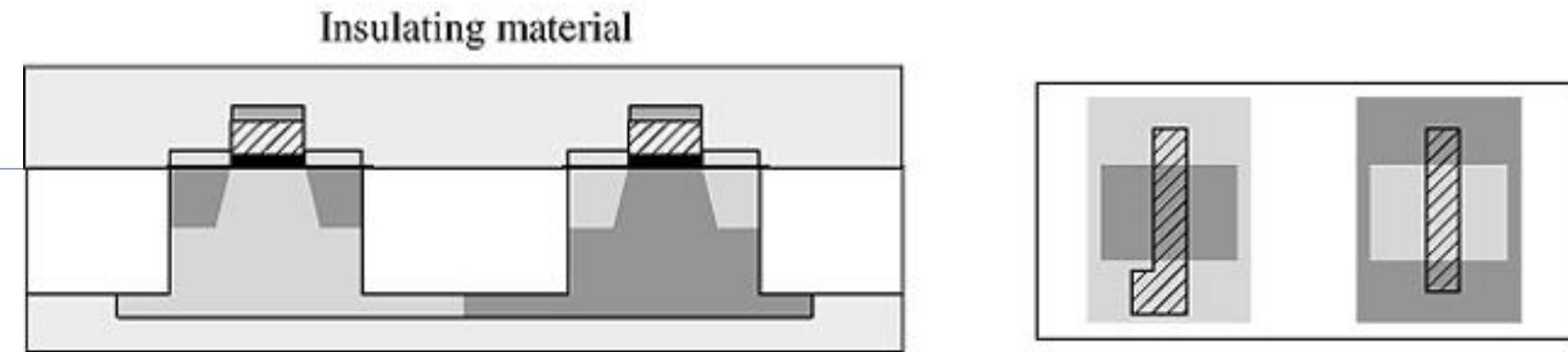
► Foundry Masks (Layout) to Physical Devices (4)



► Foundry Masks (Layout) to Physical Devices (5)

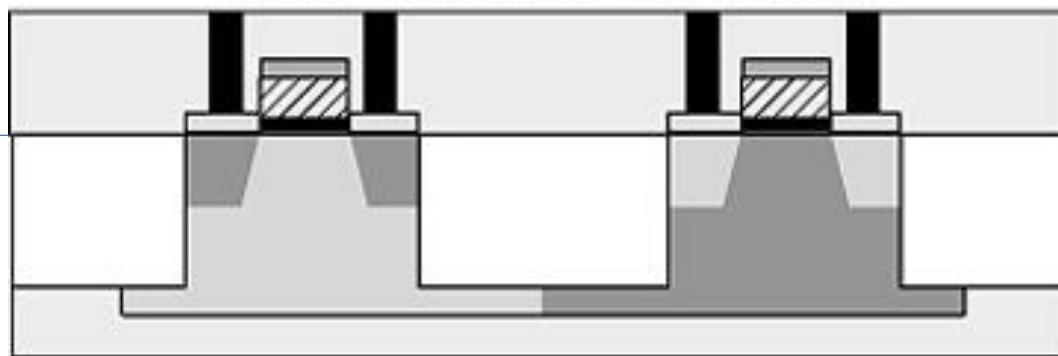


► Foundry Masks (Layout) to Physical Devices (6)

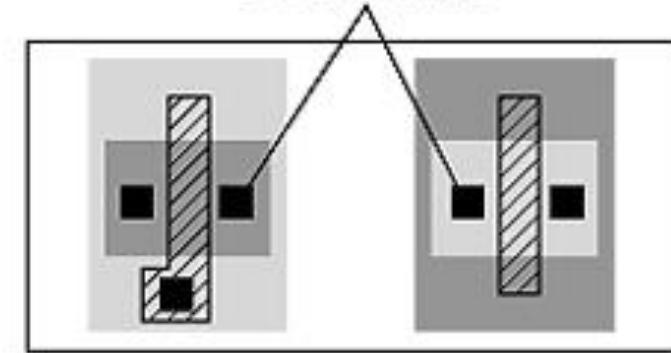


► Foundry Masks (Layout) to Physical Devices (7)

Contact cuts filled with tungsten

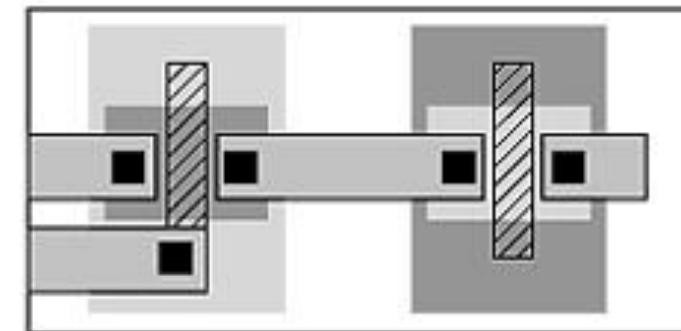
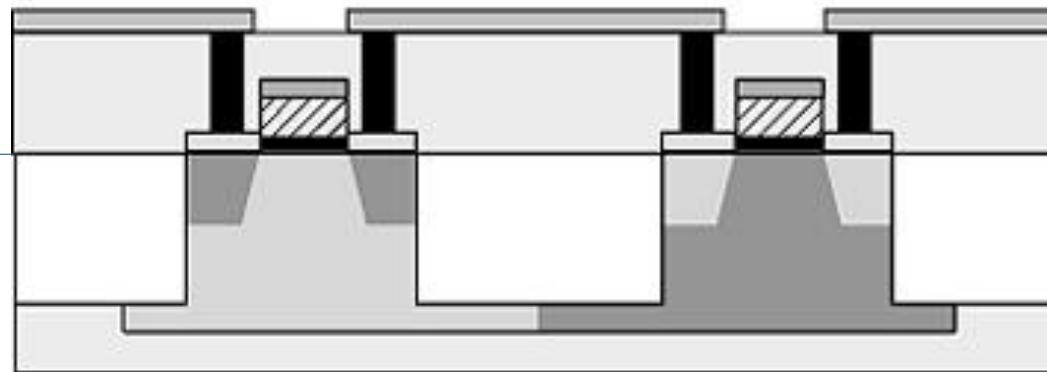


Contact cuts



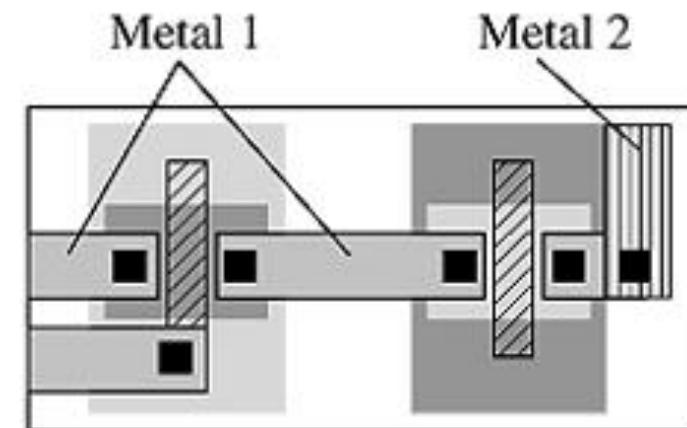
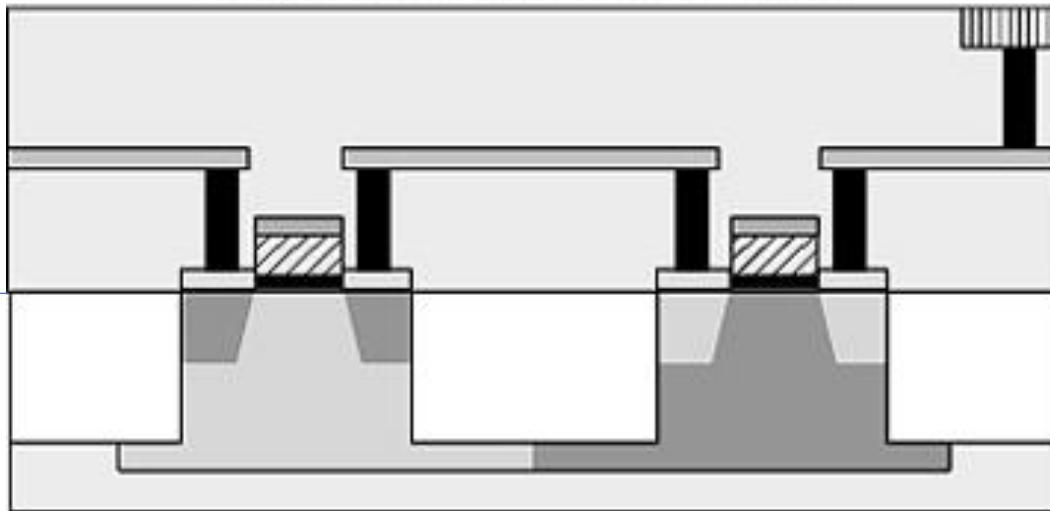
► Foundry Masks (Layout) to Physical Devices (8)

Deposited and patterned metal 1

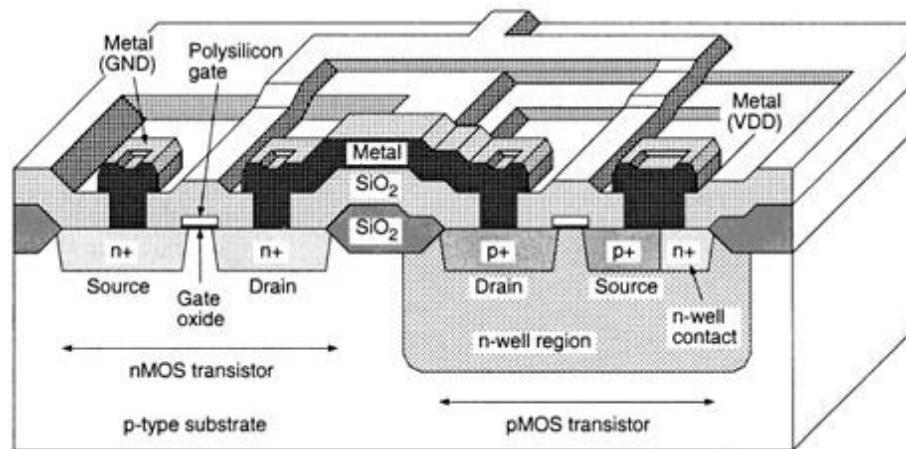
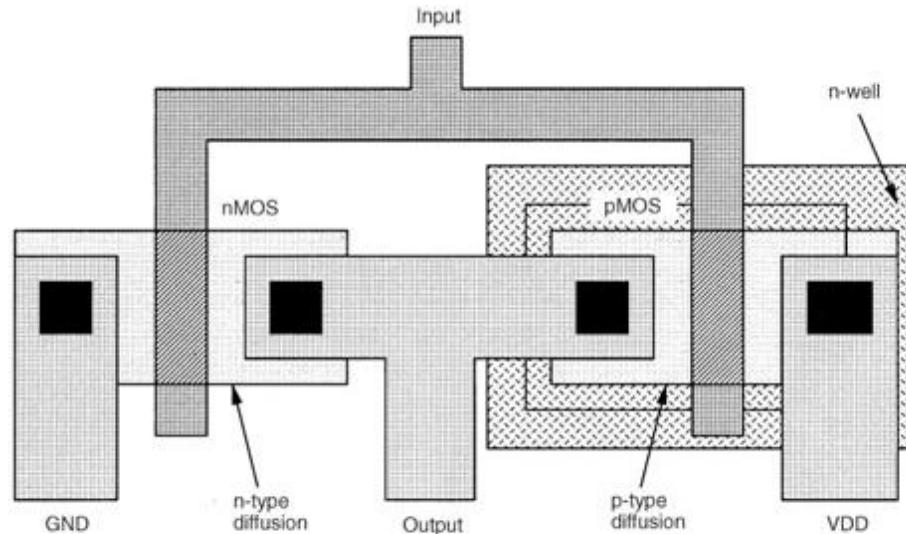


► Foundry Masks (Layout) to Physical Devices (9)

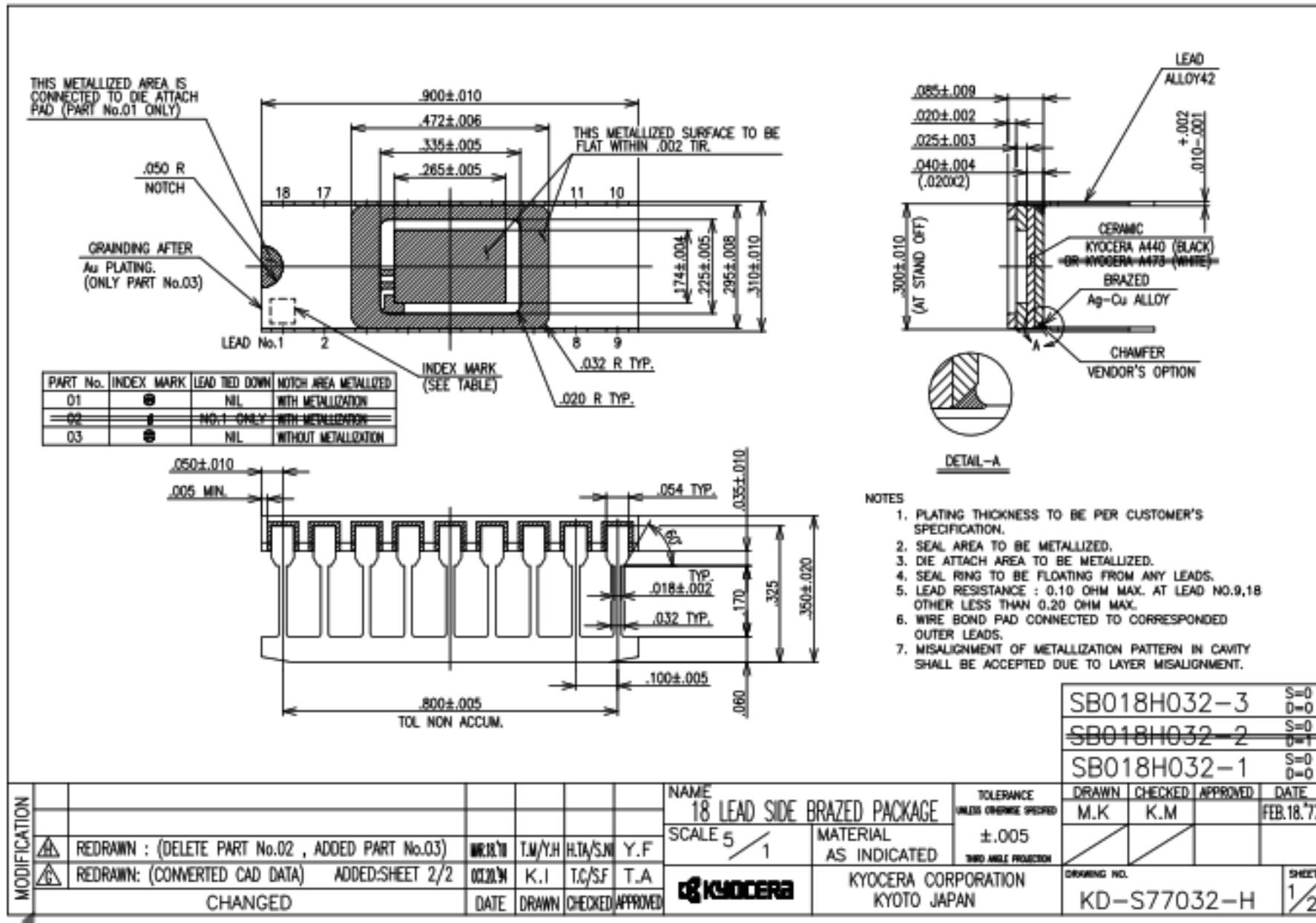
Deposited and patterned metal 2



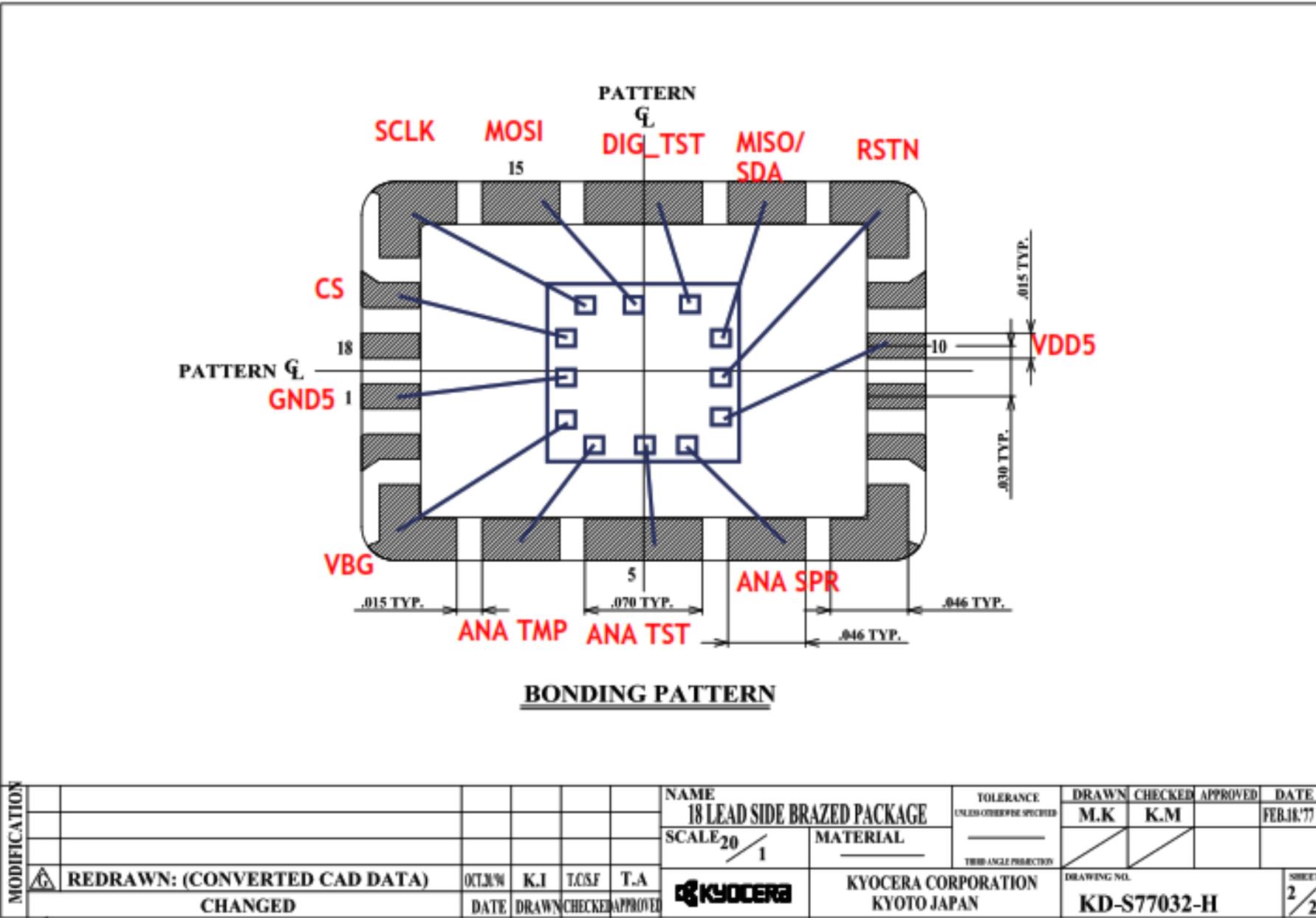
► An Older Fabrication Technique: LOCOS



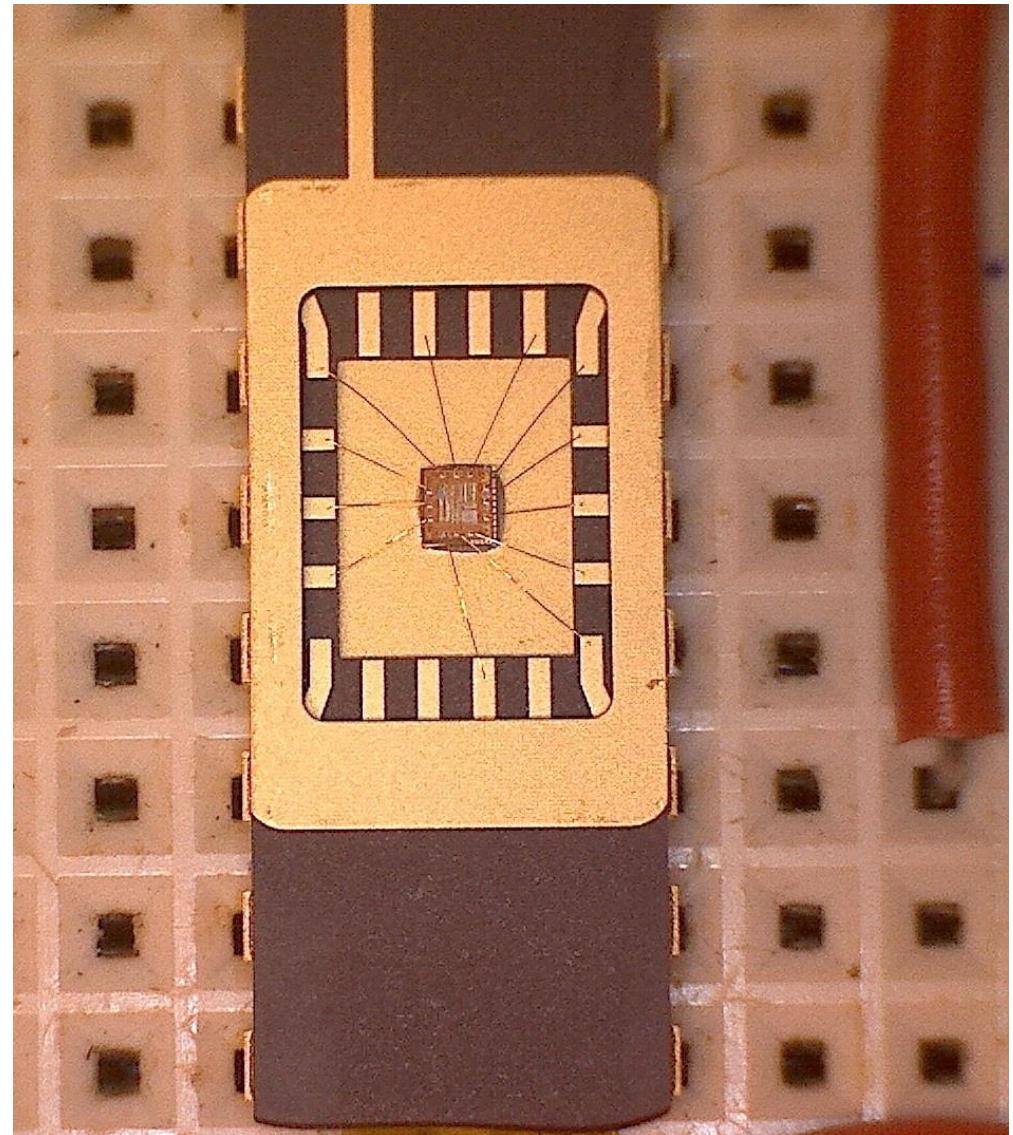
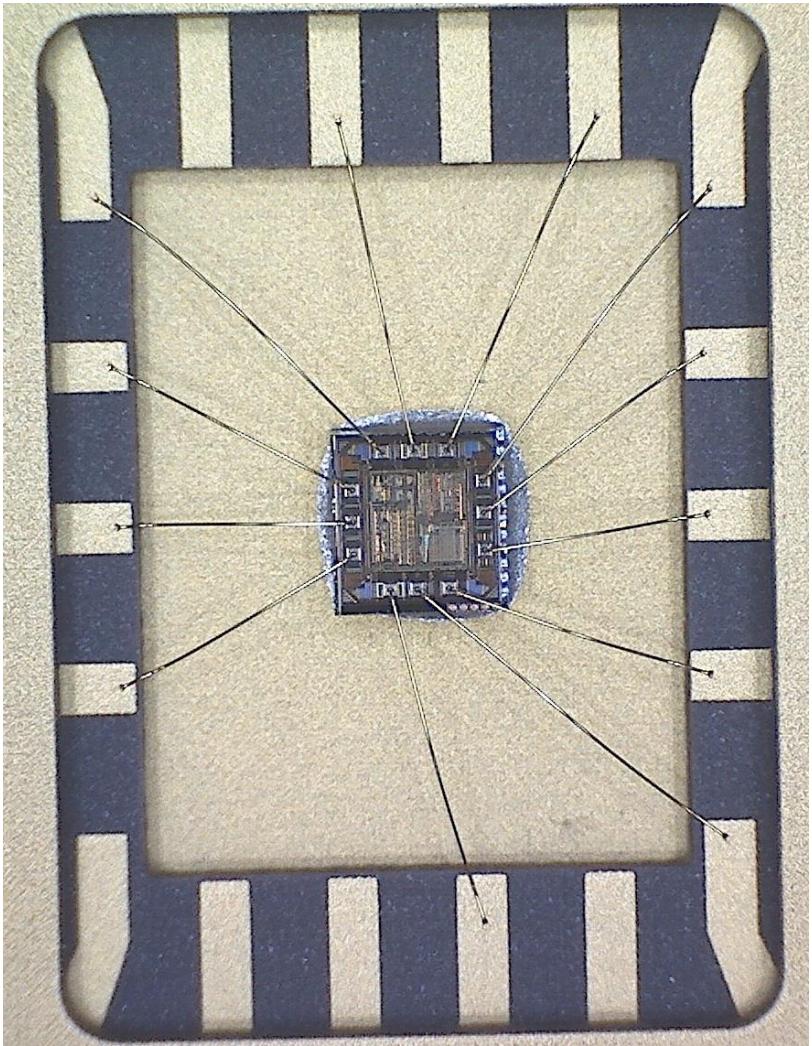
► 18-PIN CDIP CAD Drawing



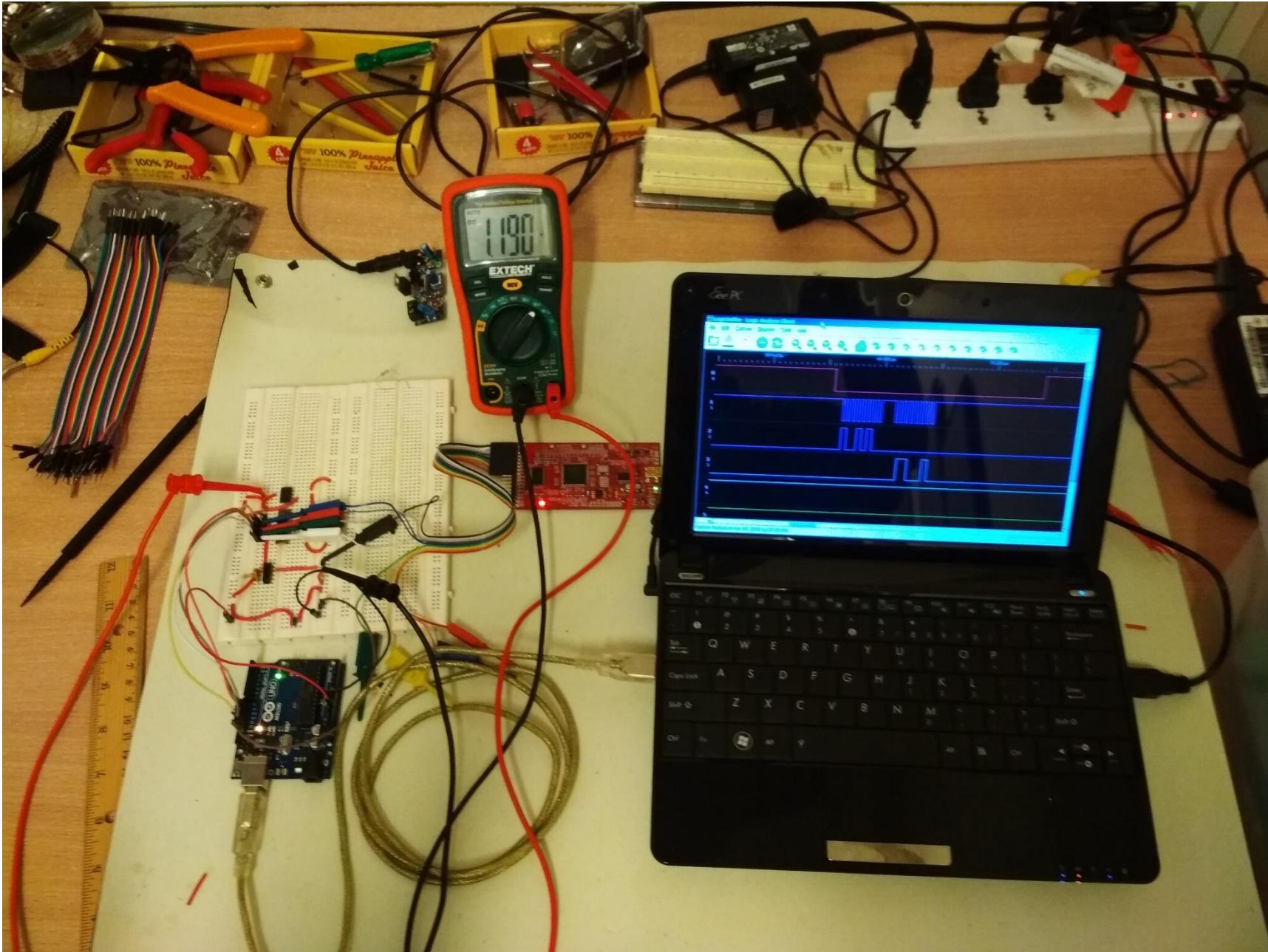
Bonding Diagram



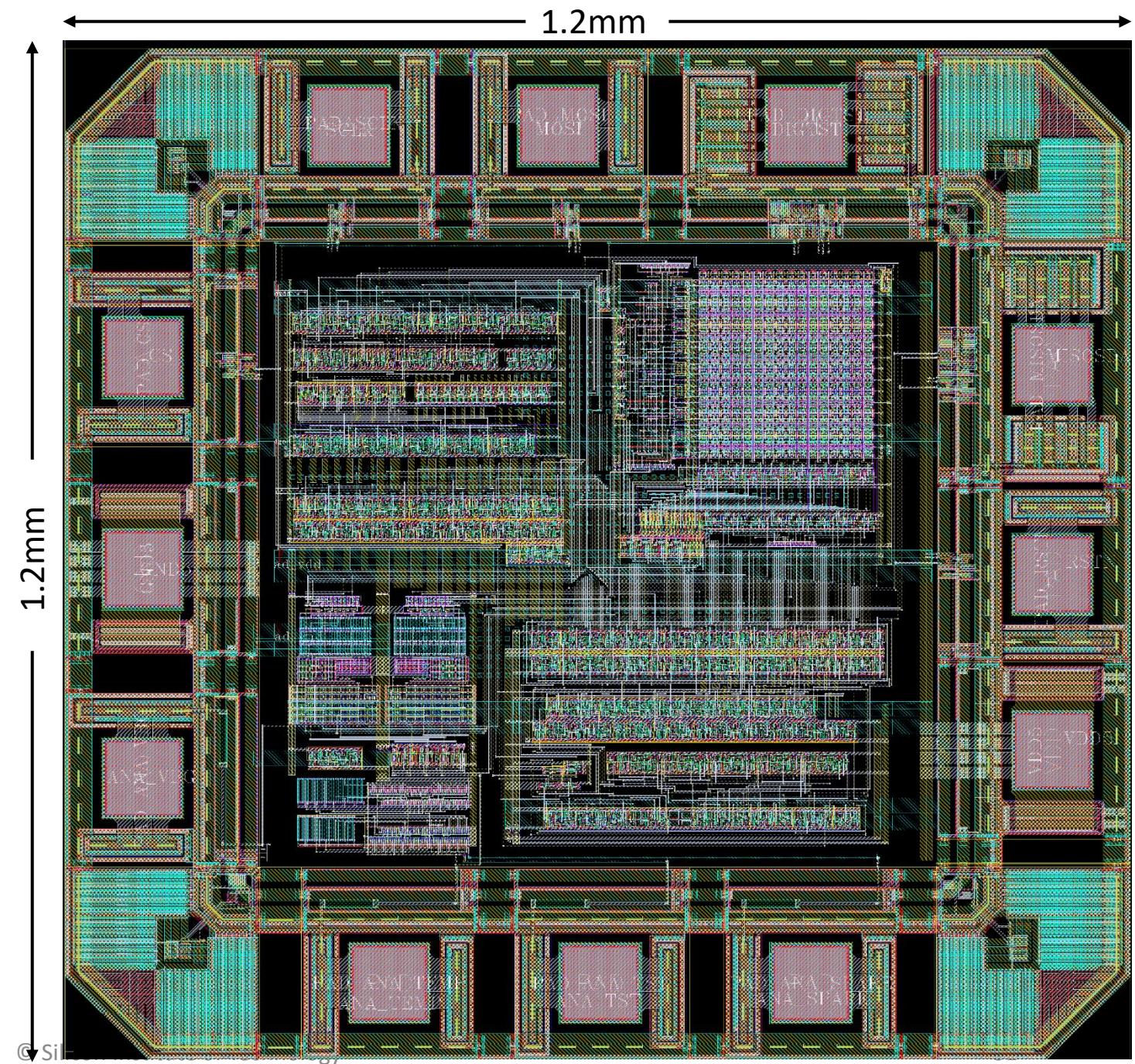
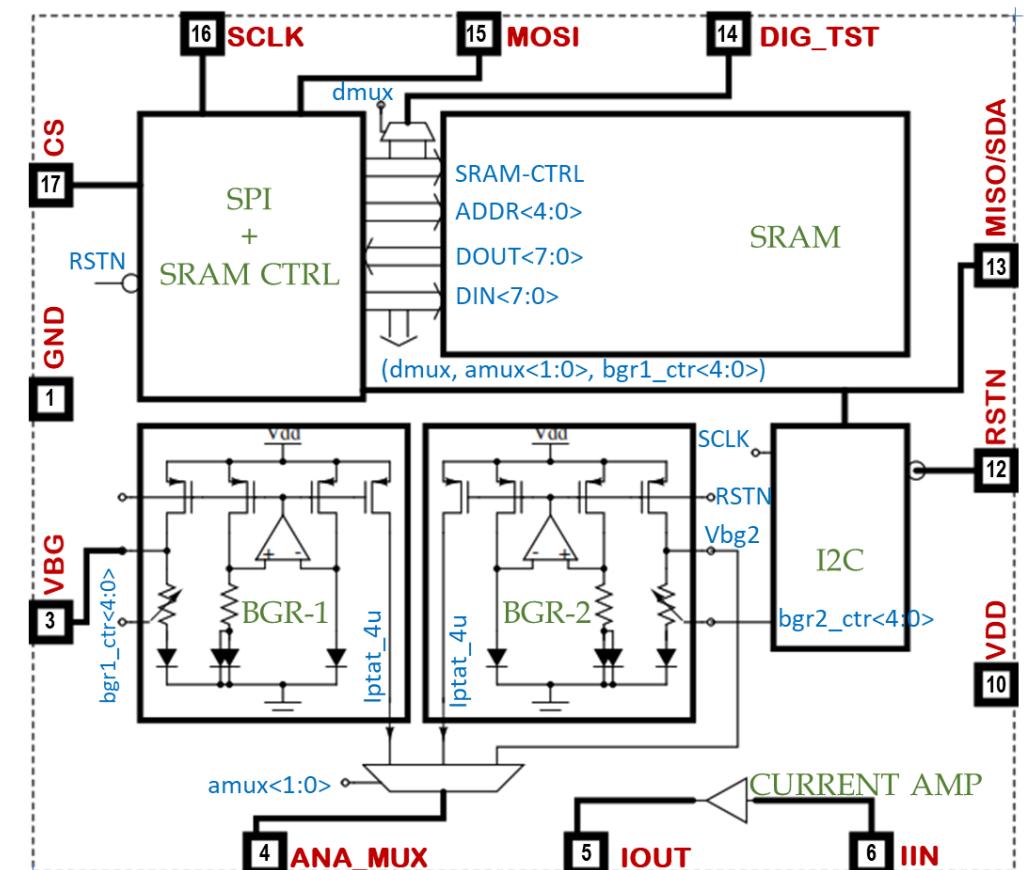
► Packaged Part

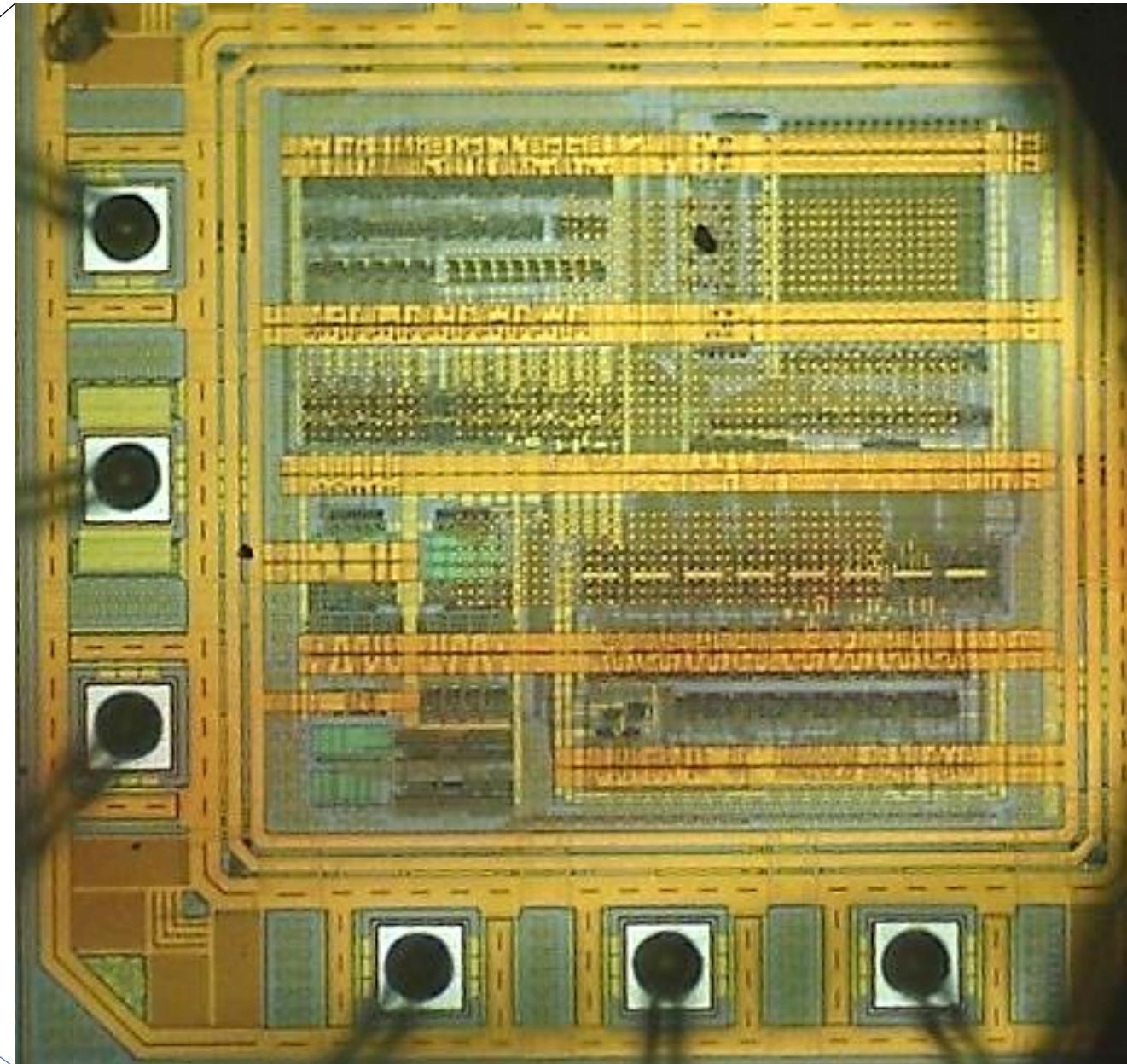
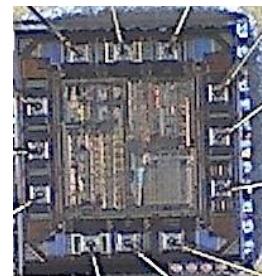


► Testing



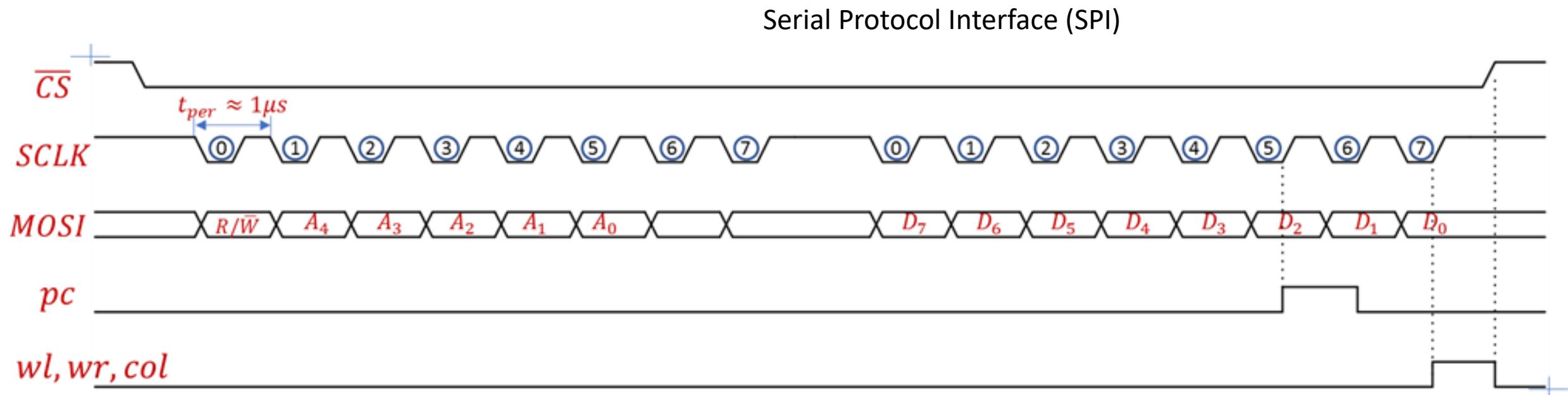
► Project Volta



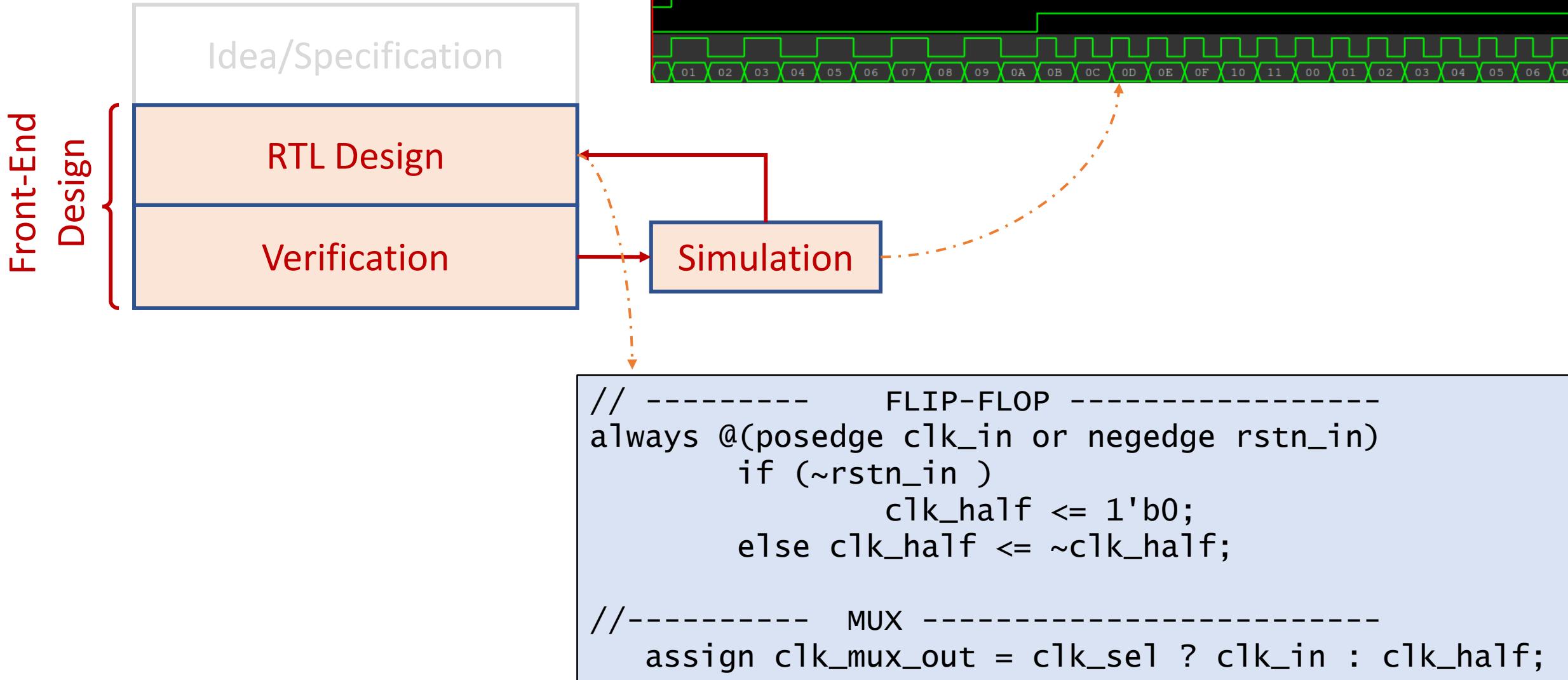


► Digital IC Design Flow

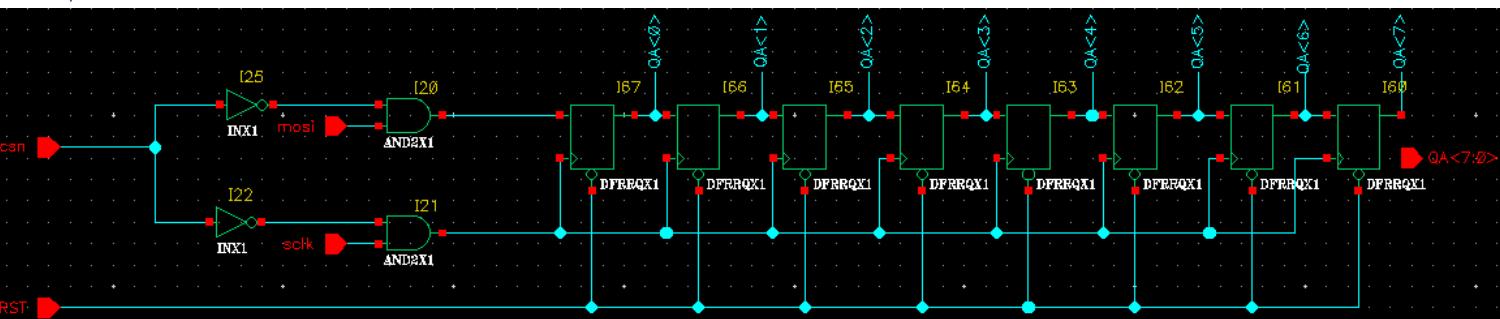
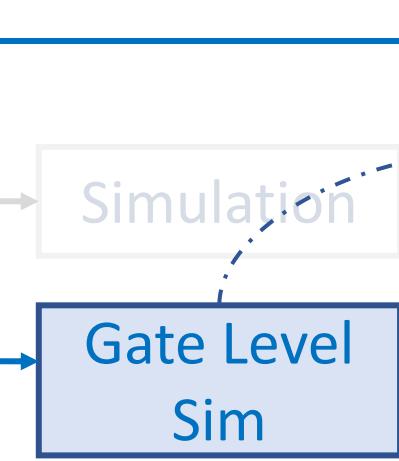
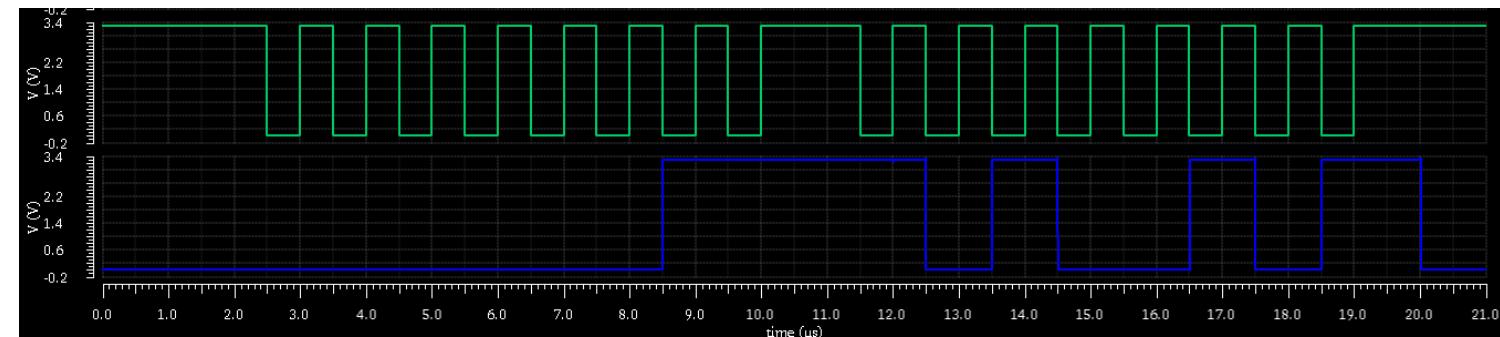
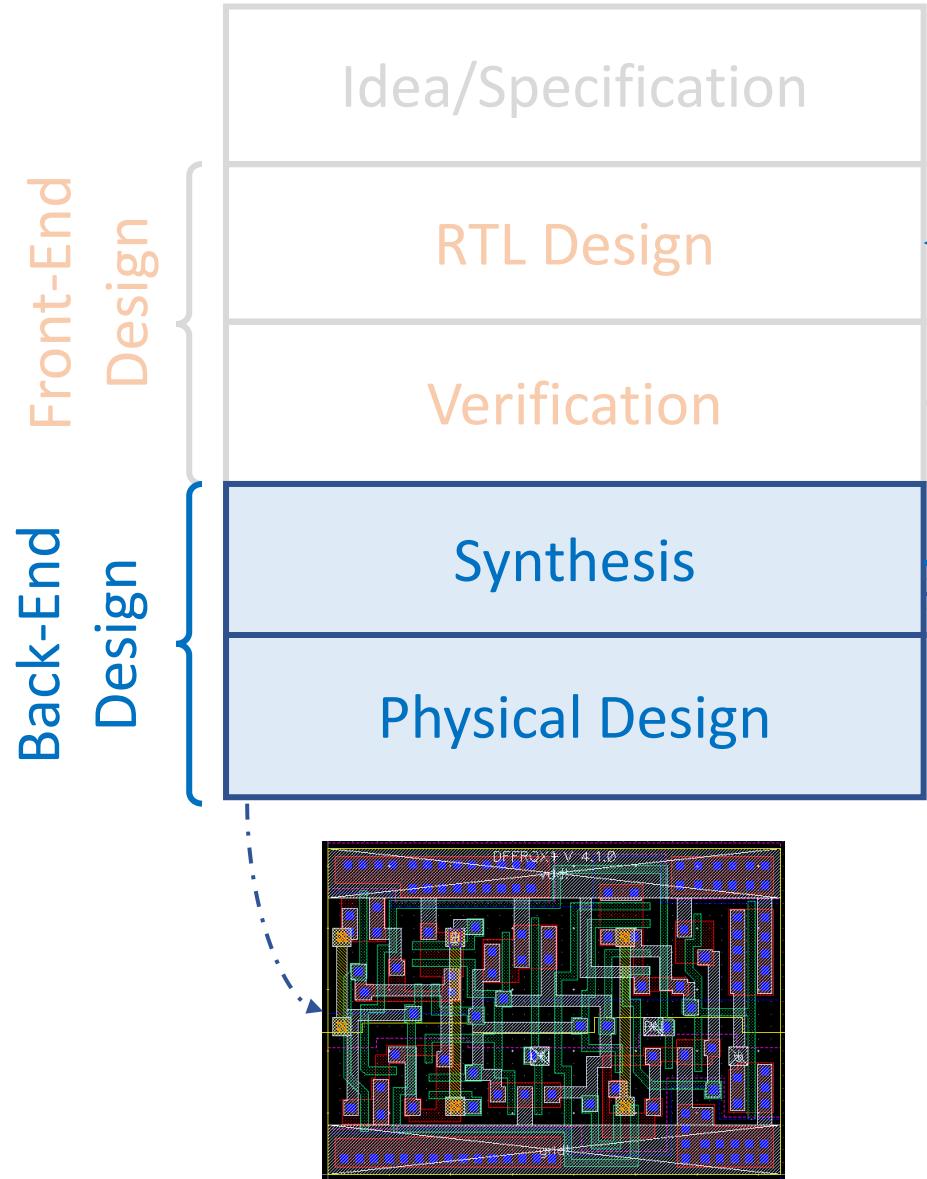
Idea/Specification



► Digital IC Design Flow



► Digital IC Design Flow



► Digital IC Design Flow

Front-End Design

Idea/Specification

RTL Design

Verification

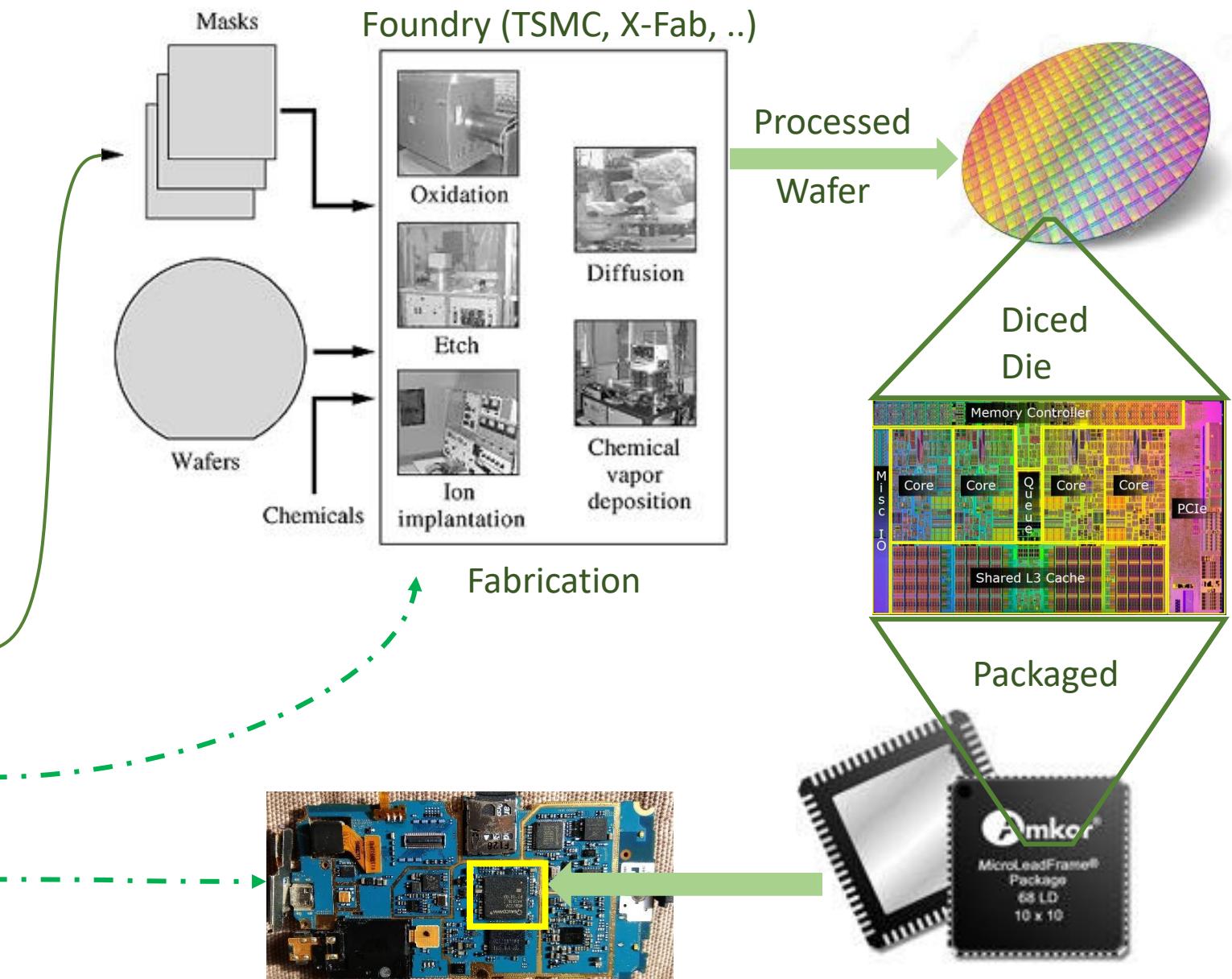
Synthesis

Physical Design

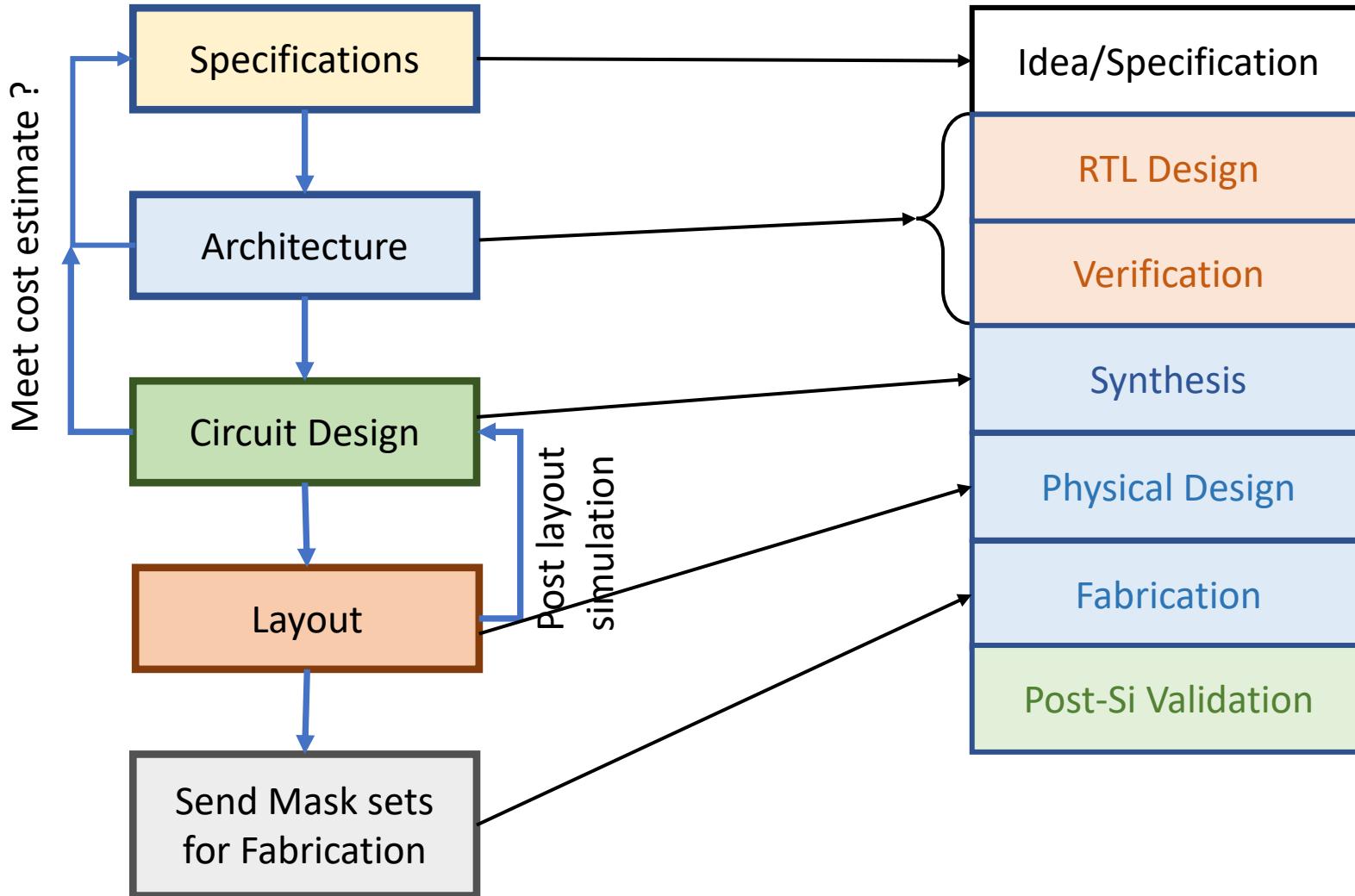
Fabrication

Post Si Validation

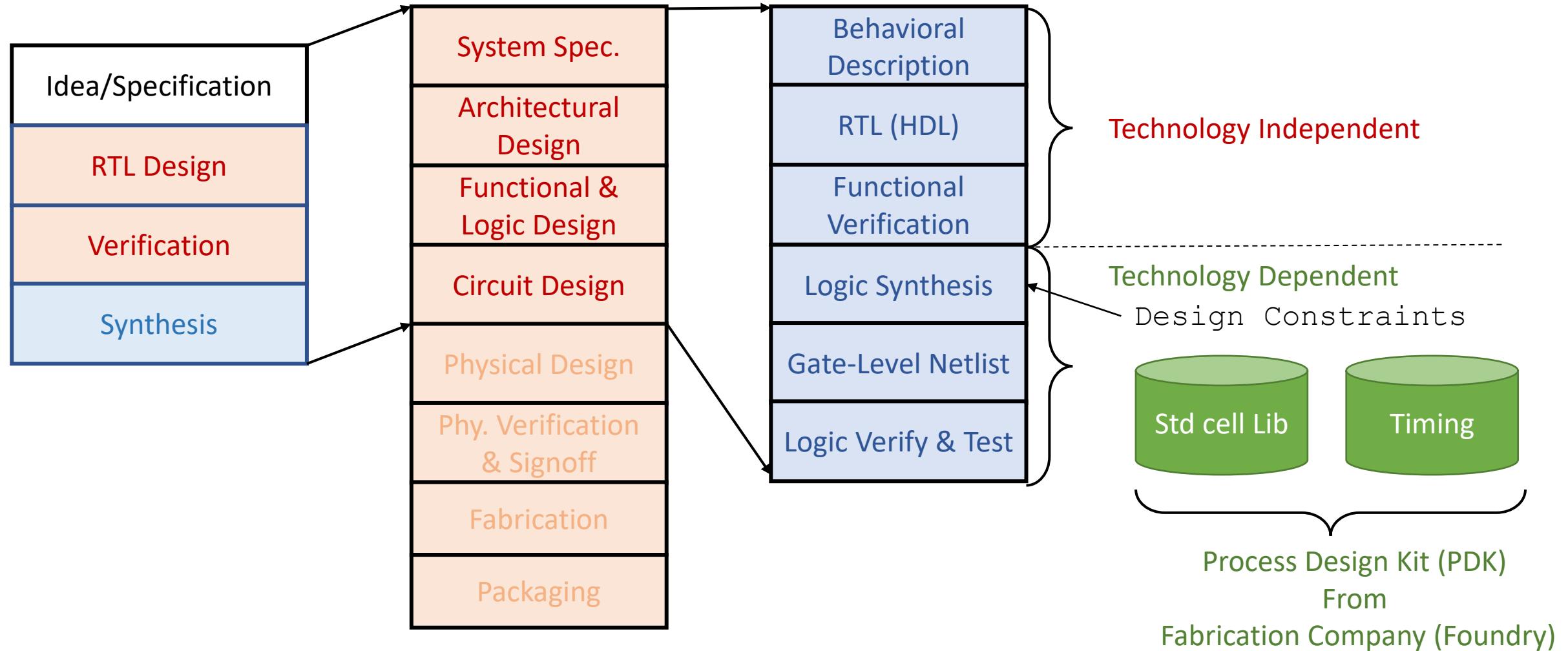
Back-End Design



► **Full Custom vs. Semi-Custom Design Flow**



► Digital IC Design Flow



► Digital IC Design Flow

