An 80-MHz 8-bit CMOS D/A Converter

TAKAHIRO MIKI, YASUYUKI NAKAMURA, MASAO NAKAYA, SOTOJU ASAI, YOICHI AKASAKA, AND YASUTAKA HORIBA

Abstract—**A high-speed 8-bit D/A converter has been fabricated in a 2-μm CMOS technology. In order to achieve high accuracy, a current-cell matrix configuration and a switching sequence named "symmetrical switching" have been introduced. The mismatch problem of small-size transistors has been relaxed by this matrix configuration. The linearity error caused by an undesirable current distribution of the current sources has been reduced by the symmetrical switching. This switching sequence has been developed on the basis of an analysis of the influence of ground-line resistance. In order to realize high-speed operation, a high-speed decoding circuit and a fast-settling current source have been developed. High-speed low-power decoding has been realized by a decoding circuit with one stage of latches. Fast settling time has been attained by designing a current source considering the relationship between the settling time and output impedance. The experimental results have shown that the maximum conversion rate is 80 MHz, a typical dc integral linearity error is 0.38 LSB, a typical dc differential linearity error is 0.22 LSB, and the maximum power consumption is 145 mW. The chip size is 1.85×2.05 mm².**

I. Introduction

ONE OF THE main applications of high-speed D/A converters is in display systems which include consumer video systems such as digital TV and high-definition TV. In these systems, the CMOS D/A converter has advantages of low power, low cost, and I/O compatibility with both TTL and external CMOS circuitry. Another important advantage of a CMOS D/A converter is its capability of being integrated with memories and digital processing IC's for video applications [1]. High-resolution display systems such as high-definition TV, however, need very high-speed converters which are clocked at more than 65 MHz and have resolution of more than 8 bits. The CMOS D/A converters produced up to now [2], [4] have had a low conversion rate, or, if the speed is satisfactory, a high power consumption.

This paper will describe an 80-MHz, 145-mW, 8-bit D/A converter fabricated in a 2-μm CMOS process [3]. A current-cell matrix has been introduced as a basic architecture to achieve high differential linearity and monotonicity. A decoding circuit with a minimum gate delay has been developed to achieve the two-dimensional decoding with neither degradation of speed nor increase of power consumption. Current sources and current switches have been optimally designed by considering the relationship between the settling time and output compliance characteristics. The linearity error caused by a voltage drop along the analog ground line has been reduced by "symmetrical switching."

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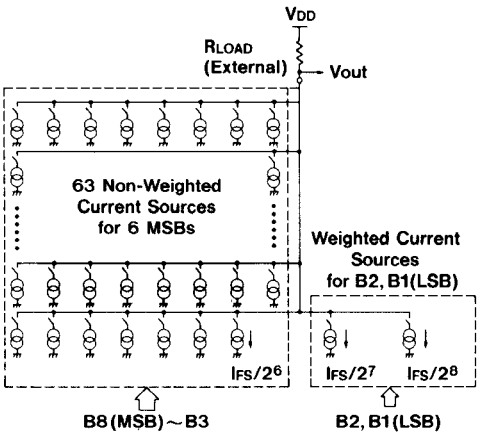

Fig. 1. Basic architecture of the DAC.

II. Basic Architecture

Small transistors which have less than 5-μm gate length are required to realize the fast settling of the current sources (the details will be discussed in Section IV). However, as the device size decreases, the mismatch among transistors increases. This mismatch degrades differential linearity and monotonicity which are necessary in video applications. In order to improve these characteristics, the current for the six MSB's has been generated by 63 non-weighted current sources arranged in a matrix. Fig. 1 shows the basic architecture of the D/A converter. For example, if the digital inputs for the six MSB's correspond to the decimal number of 30, 30 current sources in the matrix are turned on and these outputs are summed up with the outputs of weighted current sources. The output is obtained in the form of the voltage drop across the external load resistor. Since the output of the largest current sources is only 4 LSB, even a 12.5-percent relative mismatch is allowable for retaining a differential linearity error of 0.5 LSB.

III. Matrix Decoding

To decode the matrix, a region like the shadowed portion in Fig. 2 should be selected. Since this portion is neither a point nor a rectangular, a simple combination of

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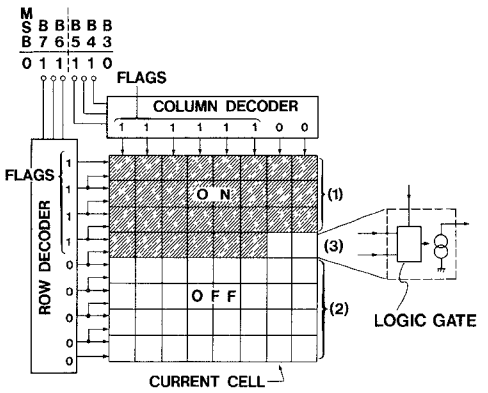

Fig. 2. Two-step decoding.

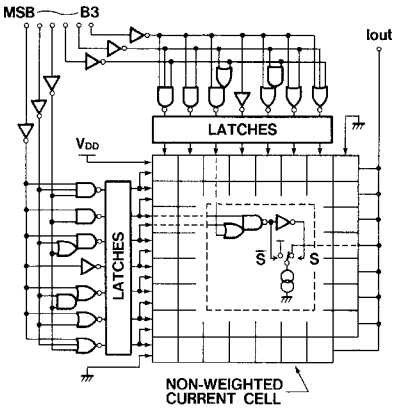

Fig. 3. High-speed decoding circuit.

NOR gates and/or NAND gates cannot attain the decoding. Decoding circuits that realize this complex decoding at speeds less than 20 MHz have already been developed [5], [6]. One solution for the 80-MHz decoding may be to introduce several stages of pipelined latches into these decoding circuits. The inserted latches, however, increase the power consumption. In order to obtain a high-speed decoding circuit with low power consumption, the decoding should be achieved with a minimum number of pipeline stages. In order to reduce the pipelining stages required for 80-MHz decoding, the following decoding circuit of minimum delay has been developed.

Fig. 2 shows the decoding logic achieved by using the minimum number of logic stages. The matrix consists of three types of rows. They are: 1) rows in which all of the current cells are turned on; 2) rows in which all of the current cells are turned off; and 3) a certain row in which current cells are turned on depending upon the column decoder signal. In consideration of these three types of rows, a decoding logic which is carried out in two steps has been developed. The details of the decoding are as follows. In the first step, digital inputs are decoded in the row decoder and column decoder. The number of flags in the columns corresponds to the input value of the column decoder. The number of flags in the rows corresponds to the input value of the row decoder plus one. In the next step, each logic gate in the current cell identifies the row type described above by comparing one row signal with the one next to it. If both of the row signals are at a high level, then the current source is turned on regardless of column signal. If the two row signals are different, then the current source is turned on depending upon the column signal.

Fig. 3 shows the actual decoding circuit. The above-described decoding logic has been achieved by using peripheral decoders and OR–NAND gates in the current cells, i.e., by two logic stages. The inverters at the input node and the inverter inside the current cell are used for buffering and generation of complementary signals. One stage of latches has been inserted between the peripheral decoders and the matrix to suppress the glitch and to enhance the decoding speed. However, since the decoding and the other required functions have been realized by the above-described four gate stages fabricated with 2-μm design rules, no more stages of latches have been necessary for 80-MHz decoding. This decoding circuit consumes approximately 70 mW and contributes to attaining the high-speed low-power characteristics of this D/A converter.

IV. Design of Current Source

Fig. 4 shows a circuit diagram of the LSB current source. In the MSB current cell of the matrix and in the current source for $B2$, each of Q_1, Q_2, and Q_3 is formed by four paralleled transistors and two paralleled transistors, respectively. The primary bias voltage V_{G1} is directly applied to the current source transistor Q_1 and determines the full-scale current. The secondary bias voltage V_{G2} is applied through transmission gates. The current source transistor Q_1 and the current switch transistors Q_2 or Q_3 are operated in saturation. The discharge transmission gates TG_3 and TG_4 are formed by single NMOS transistors to realize low-resistance switches with low stray capacitance.

The current source transistor Q_1 has been designed to have a low transconductance in order to enhance the immunity against voltage fluctuation along the ground line (discussed in Section V), and also, against noise at the node of the primary bias voltage V_{G1}. For the same purpose, the cascode-connected configuration for the current source Q_1 as is shown in Fig. 5(b) has not been used. In the cascode configuration, Q_4 and Q_5 are operated in saturation, whereas Q_1 and Q_2 are operated in saturation in the single transistor configuration shown in Fig. 5(a). Since the voltage V_x across Q_4 and Q_5 is lower than the voltage V_{out} across Q_1 and Q_2, Q_4 and Q_5 should be designed to have relatively high transconductance. This high transconductance can cause a low immunity against the voltage fluctuation at the ground line and the bias node.

In order to realize a fast settling time, the stray capacitance at the output node should be small. The stray capacitance at the common source node should also be small to minimize the recovery time of the voltage at this node during the switching transition. This can be achieved by using small-sized transistors for the current source and the current switch. However, short-channel devices de-

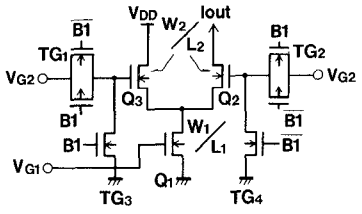

Fig. 4. Circuit diagram of the LSB current source.

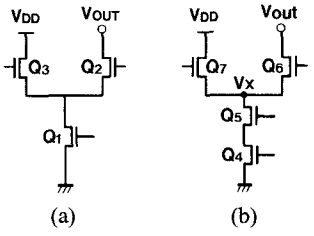

Fig. 5. Configuration of current source. (a) Single-transistor configuration. (b) Cascode configuration.

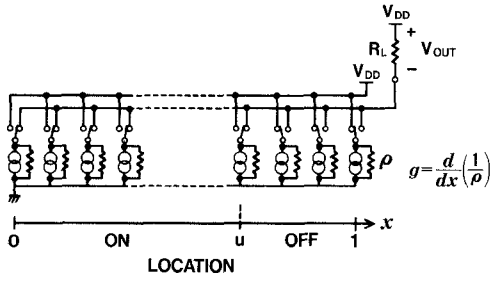

Fig. 6. Model for analyzing influence of output impedance of current sources.

crease the output impedance, and consequently, the linearity is degraded.

Fig. 6 shows a model for analyzing the influence of the output impedance. A one-dimensional current source array is assumed here. The current sources are uniformly arranged from $x=0$ to $x=1$. Assuming i is the output current per unit length of the current source array and a constant g is the output conductance of a unit length of the current source array, then the relationship between i and output voltage V_{out} is as follows:

$$i = i_0 - gV_{\text{out}} \tag{1}$$

where i_0 is an output current per unit length of the current source array when $V_{\text{out}}=0$. Assuming u is a ratio of input value to the full scale, the total output current when the input value corresponds to u is given by integrating i from 0 to u. Since i is not a function of x, the output voltage V_{out} is given as

$$V_{\text{out}}(u) = R_L \int_0^u i\,dx = R_L iu \tag{2}$$

where R_L is a load resistance. V_{out} is obtained from (1) and (2) as

$$V_{\text{out}}(u) = R_L i_0 \frac{u}{1+gR_L u}. \tag{3}$$

Assuming the ideal output $V'_{\text{out}}(u)$ is given by a straight

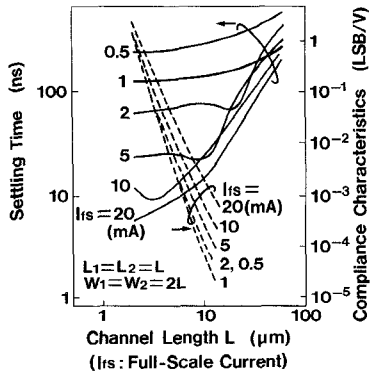

Fig. 7. Simulation result for settling time and compliance characteristics as a function of channel length.

line between zero and full-scale output, that is,

$$V'_{\text{out}}(u) = V_{\text{out}}(1)u \tag{4}$$

the deviation of the actual output from the ideal output normalized by the full-scale output is obtained as follows:

$$E(u) = \frac{V_{\text{out}}(u) - V'_{\text{out}}(u)}{V_{\text{out}}(1)} = gR_L \frac{u(1-u)}{1+gR_L u}. \tag{5}$$

The maximum of $E(u)$ gives an integral linearity error. Since all current sources are arranged along the unit length, g is equal to the total output conductance when all current sources are connected in parallel. Assuming C_p is a compliance of the full-scale current defined as a normalized fluctuation of the full-scale current caused by a unit voltage change of output node, the relationship between g and C_p is given by

$$C_p \triangleq \frac{(\Delta I_{fs}/I_{fs})}{\Delta V_{\text{out}}} = \frac{g}{I_{fs}} \tag{6}$$

where I_{fs} is a full-scale current. Consequently, the integral linearity error E is approximated as

$$E = \frac{1}{4} gR_L = \frac{1}{4} C_p V_{fs} \tag{7}$$

where V_{fs} is a full-scale voltage swing. For example, when the full-scale voltage swing is 1 V, an output compliance of 0.4 LSB/V is required in order to suppress the integral linearity error within 0.1 LSB.

The relation of the settling time and the output compliance as a function of channel length has been simulated. The results are shown in Fig. 7. It is assumed that the current source transistor and current switch transistors have the same size and that the channel width is twice the channel length. A load resistance which produces a full-scale swing of 1 V for each full-scale current, and a load capacitance of 20 pF are also assumed. A gate length of less than 5 μm and a full-scale current of more than 10 mA are necessary to achieve a settling time of 12.5 ns. On the other hand, the minimum gate length of 2 μm has a compliance of 1 LSB/V which causes an integral linearity error of 0.25 LSB. The gate length of 2.5 μm has been chosen for L_1 and L_2 to have a margin in both settling

time and linearity. Owing to this optimization and the small stray capacitances in the 2-μm design-rule geometries, the fast settling time has been achieved without a serious degradation in the linearity.

V. Symmetrical Switching

As discussed in the previous section, an output current of 10–20 mA is necessary to achieve fast settling time. However, this large current also causes a linearity error. The voltage drop along the ground line caused by the current changes the bias voltage of the current sources, producing a tapered error distribution in the output value of each current source. In a conventional switching sequence of the current source, the tapered distribution results in a significant linearity error. In order to avoid this problem, a switching sequence named "symmetrical switching" has been introduced.

The top of Fig. 8 shows a model for the analysis of this problem. Although a matrix configuration is used in the D/A converter, the current sources are assumed to be arranged in a one-dimensional way for simplicity. The influence of the output impedance discussed in the previous section has been neglected. Nonweighted current sources are uniformly arranged along a ground line from $x=0$ to $x=1$. Assuming that $j(x)$ is the output current per unit length of current source array, this current is related to the ground line voltage $v(x)$ as

$$j(x) = j_0 - G_m v(x) \tag{8}$$

where j_0 is the output current per unit length of the current source array when $v=0$ and the constant G_m is a transconductance between the bias voltage and $j(x)$. Since all current sources are arranged along the unit length, j_0 and G_m are equal to the full-scale current in the case that no voltage drop occurs along the ground line and equal to the transconductance between the full-scale current and the bias voltage, respectively. The voltage drop along the ground line between x_0 and $x_0-\Delta x$ is given by Ohm's law, that is [7]

$$v(x_0) - v(x_0-\Delta x) = \Delta x R \int_{x_0}^{1} j(x)\,dx \tag{9}$$

where R is the total resistance of the ground line. From (8) and (9), the following differential equation and boundary conditions are derived:

$$v(x) - \frac{1}{G_m R}\frac{d^2}{dx^2}v(x) = \frac{1}{G_m}j_0 \tag{10}$$

$$v(0) = 0 \tag{11}$$

$$\left.\frac{dv}{dx}\right|_{x=1} = 0. \tag{12}$$

The boundary condition (12) is confirmed by substituting $x_0=1$ into (9). The current distribution normalized by an average current is calculated by substituting the solution of

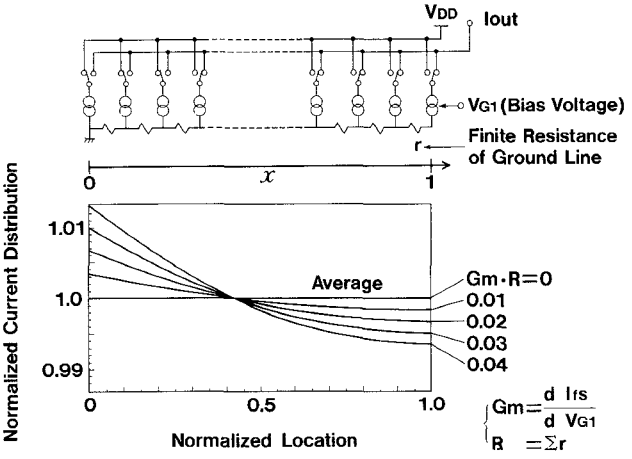

Fig. 8. Current distribution of current sources.

this differential equation into (8), that is

$$j_{nom}(x) = \sqrt{G_m R}\,\frac{\cosh\left\{\sqrt{G_m R}\,(1-x)\right\}}{\sinh\sqrt{G_m R}}. \tag{13}$$

This normalized current distribution is shown in the bottom of Fig. 8. The outputs of the current sources have a tapered distribution. This tapered distribution produces a significant linearity error in a conventional switching sequence.

Fig. 9 shows an example of a conventional switching sequence and the proposed new switching sequence. If the current sources are connected to the output node sequentially from the left to the right as input value increases, each deviation from the average is accumulated and produces a significant integral linearity error. This error is obtained as the maximum value of the integration of the deviation, that is [7]

$$E_{sq} = \frac{G_m R}{9\sqrt{3}}. \tag{14}$$

For example, assuming that the bias voltage is 2.5 V, the threshold voltage is 0.7 V, the full-scale current is 13.3 mA, and the resistance of the ground line is 2 Ω, the error amounts to 0.2 percent.

In order to avoid this problem, the symmetrical switching shown in Fig. 9 has been introduced. In the symmetrical switching, the current sources are connected symmetrically about the center as the input value increases. The integral linearity error has been reduced by this switching sequence because a deviation from the average of the output current is immediately canceled in the next step. The error caused by this switching sequence is approximated as [7]

$$E_{sy} = \frac{G_m R}{36\sqrt{3}} \tag{15}$$

which is 25 percent of the error caused by the sequential switching. Assuming the same condition as in the sequential switching, the integral linearity error is reduced to 0.05

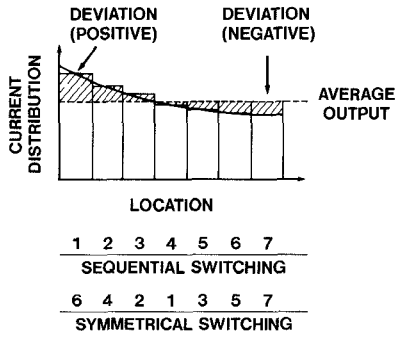

Fig. 9. Symmetrical switching.

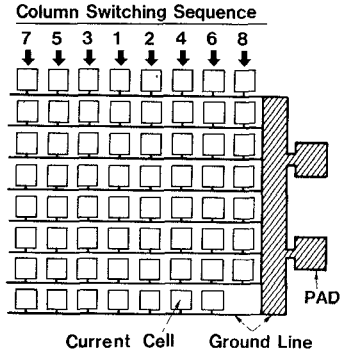

Fig. 10. Switching sequence of matrix.

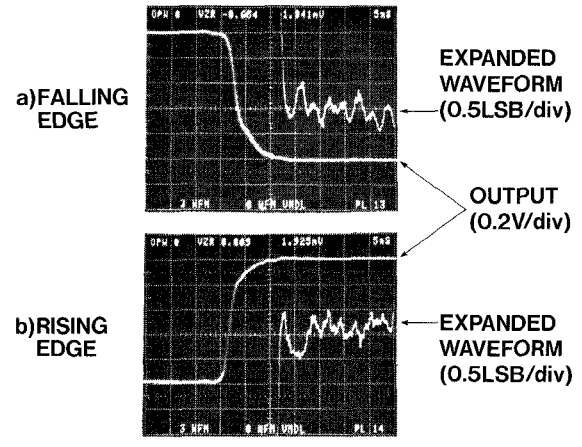

Fig. 11. Settling waveform of DAC.

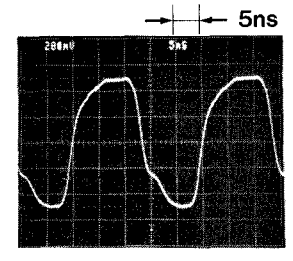

Fig. 12. Full-scale swing at 80-MHz data update rate.

percent by using this switching sequence. On the other hand, the differential linearity error is increased by this sequence. This error is given by the difference between the output at $x = 0$ and at $x = 1$. It is 1.5 percent of the output of the unit current sources in a typical condition. However, this value corresponds to a differential linearity error of only 0.06 LSB in this D/A converter in which current sources of 4 LSB are used in the matrix.

Fig. 10 shows the switching order used in the current-cell matrix. A comb-shaped ground line has been used. The resistances of the backbone and the tooth of the comb are 0.4 and 5 Ω, respectively. Two bonding pads have been allocated to reduce the resistance of the backbone of the comb. The symmetrical switching is introduced into the column switching order by simply rearranging the logic gates in the column decoder shown in Fig. 3. This switching sequence is not used for the row switching order, because the resistance of the backbone is small enough to minimize the voltage drop along itself. However, if the backbone is narrow, it is more effective to introduce this technique into the row switching order also.

VI. Process

This D/A converter has been implemented in a 2-μm double-polysilicon CMOS technology. The first polysilicon forms gate electrodes and interconnection. The second polysilicon has been used only for interconnection. A double-aluminum process would seem to be more flexible in terms of the layout of some interconnections, such as analog ground lines, current output lines, and power supply lines, in which it is necessary to have small resistances. However, the double-polysilicon process has been adopted because of its advantage of feasible integration of the other analog circuits such as a flash A/D converter which contains capacitors and resistors.

VII. Experimental Results

Fig. 11 shows the full-scale transition of the output, where the full-scale current is 13.3 mA and the external load is 75 Ω. The expanded waveform shows that the settling time to 0.5 LSB is approximately 12.5 ns at both rising and falling edges. The 10–90-percent rise/fall time is less than 5.5 ns. The amplitude of the full-scale swing is constant up to 80 MHz. Fig. 12 shows the output waveform of the full-scale swing at the data-update rate of 80 MHz. This waveform also shows that the decoder is successfully operated at the same frequency because all gates in the decoding circuit alternate their outputs in every swing. The maximum speed of the decoding circuit is approximately 95 MHz. This speed has been measured by observing a sudden change of the waveform and the amplitude. Fig. 13 shows a result of linearity measurement at dc. In this example, an integral linearity error of 0.19 LSB and a differential linearity error of 0.17 LSB have been obtained without trimming. It has been observed that the glitch consists of a single pulse. Its height is 40 mV and its duration is 4.5 ns. The glitch energy is 100 ps·V. This glitch is caused by an internal skew between the row decoder outputs and column decoder outputs. A chip photomicrograph is shown in Fig. 14. Current cells have

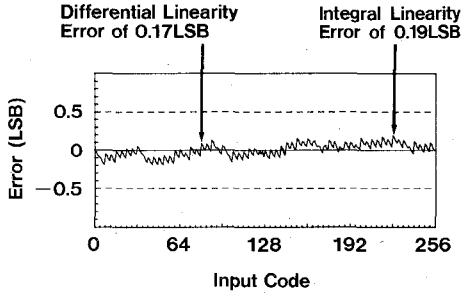

Fig. 13. Linearity of DAC.

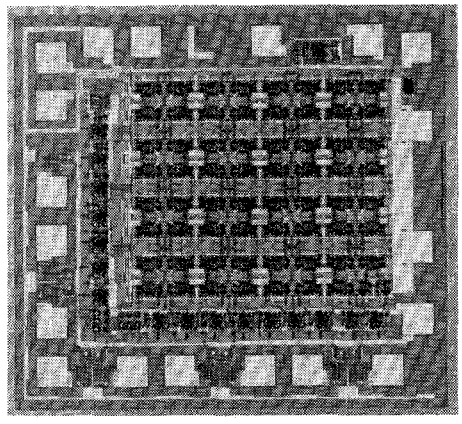

Fig. 14. Photomicrograph of DAC.

TABLE I
CHARACTERISTICS OF THE DAC

Resolution	8 bit
Settling Time	12.5 ns
Rise/Fall Time	5.5 ns
Integral Linearity Error (DC)	0.38 LSB (Typ.)
Differential Linearity Error (DC)	0.22 LSB (Typ.)
Glitch Energy	100 ps·V
Power Consumption	145 mW
Chip Size	1.85 mm x 2.05 mm

been arranged in an 8×8 matrix. The chip size is 2.05×1.85 mm^2 and the active area is 1.6×1.3 mm^2. The power consumption is 145 mW at a power supply of 5 V. The characteristics of this D/A converter are summarized in Table I.

VIII. Conclusion

An 80-MHz, 145-mW, 8-bit D/A converter has been fabricated in a 2-μm double-polysilicon process. High accuracy has been achieved by adopting a current-cell matrix configuration and introducing a switching sequence named "symmetrical switching." High-speed and low-power decoding is achieved by a decoding circuit with minimum gate delay. Fast-settling and high-impedance current sources have been realized by an optimization of the current source geometry based on an analysis of the relationship between a linearity error and output impedance of the current source.

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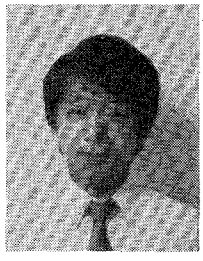

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Sotoju Asai, for photograph and biography please see this issue, p. 982.

Yoichi Akasaka, for photograph and biography please see this issue, p. 982.

Yasutaka Horiba, for photograph and biography please see this issue, p. 982.