A 26 μW 8 bit 10 MS/s Asynchronous SAR ADC for Low Energy Radios

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***Abstract*—This paper presents an asynchronous SAR ADC for flexible, low energy radios. To achieve excellent power efficiency for a relatively moderate resolution, various techniques are introduced to reduce the power consumption: custom-designed 0.5 fF unit capacitors minimize the analog power consumption while asynchronous dynamic logic minimizes the digital power consumption. The variability of the custom-designed capacitors is estimated by a specialized CAD tool and verified by chip measurements. An implemented 8-bit prototype in a 90 nm CMOS technology occupies 228 μm $\times$ 240 μm including decoupling capacitors, and achieves an ENOB of 7.77 bit at a sampling frequency of 10.24 MS/s. The power consumption equals 26.3 μW from a 1 V supply, thus resulting in an energy efficiency of 12 fJ/conversion-step. Moreover, the fully dynamic design, which is optimized for low-leakage, leads to a standby power consumption of 6 nW. In that way, the energy efficiency of this converter can be maintained down to very low sampling rates.**

***Index Terms*—ADC, analog-to-digital conversion, asynchronous, CMOS, successive approximation.**

I. Introduction

UPCOMING low energy radios in the ISM (industrial, scientific and medical) radio bands such as low-energy Bluetooth or IEEE 802.15.6 for body-area networks require power-efficient ADCs. Because of the use of simple modulation schemes like OOK, moderate resolutions (e.g. 4 bit up to 8 bit) are sufficient. Data rates are strongly application dependent, but are typically expected in the range of several kS/s (e.g. medical sensor applications like ECG monitoring) up to several MS/s (e.g. audio streaming). To provide a single solution that can cover a wide range of applications, the data rate needs to be scalable in a power-efficient way to adapt to different scenarios. Thus, ultra-low-power moderate-resolution ADCs with a relatively low, but efficiently scalable sample rate are required. This work proposes an architecture that achieves excellent power-efficiency for an 8 bit ADC using sample rates from 1 kS/s up to 10 MS/s.

The successive approximation architecture (SAR) is selected in this work because of the excellent power efficiency. Fig. 1 presents the overall architecture of the proposed 8 bit asynchronous SAR ADC: the switched capacitor network implements the Sample&Hold (S&H), the feedback DAC and the summation node. Based on the output of the comparator, the feedback loop performs an 8-bit binary-search algorithm to determine the digital output code.

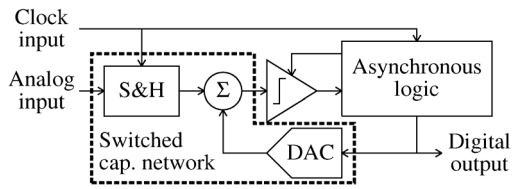

Fig. 1. Asynchronous SAR ADC architecture.

Several key techniques are presented in this work to enable power efficiency for moderate-resolution, flexible-speed AD converters: custom-designed 0.5 fF capacitors to reduce analog power consumption, asynchronous dynamic logic to reduce digital power consumption and a low-leakage fully dynamic design to achieve a widely scalable sample rate. Moreover, a reduced power supply (1 V) further minimizes the power consumption.

This paper is organized as follows. Section II discusses the design and implementation of the switched capacitor network, the 0.5 fF unit capacitors and the comparator. Section III introduces asynchronous dynamic logic as a power-efficient implementation for digital logic. The overall ADC is presented in Section IV and measurement results are discussed in Section V. Finally, conclusions are drawn in Section VI.

II. Switched Capacitor Network and Comparator

A. Switched Capacitor Network

The switched-capacitor network of the ADC, shown in Fig. 2, implements the Sample&Hold, feedback DAC and summation node. The transistor sizes of the sampling switch and DAC drivers are indicated in the figure. A complementary switch samples the differential analog input signal on the capacitor array. Despite the reduced power supply of 1 V and the relatively high threshold voltage of the low-V_{th} transistors in the used 90 nm process, the simple complementary switch achieves sufficient linearity and bandwidth for the design target. According to simulations, a linearity of over 60 dB is achieved for a full-scale input tone around Nyquist while sampling at 10 MS/s. Because of the absence of bottom-plate sampling, charge injection from the sampling switch results in a signal-dependent common-mode step in the order of 4

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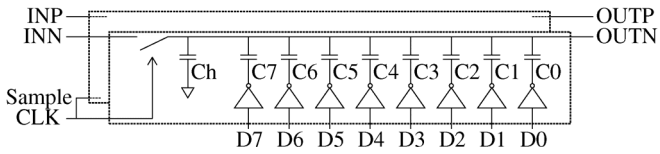

Switch: PMOS 20u/0.1u, NMOS 10u/0.1u
DAC drivers (all identical size): PMOS 1u/0.1u, NMOS 0.4u/0.1u

Fig. 2. Switched capacitor core of the ADC.

to 12 mV. However, even with 10% size mismatch in the transistors of the sampling switch, apart from a 0.7 mV output offset, the linearity of 60 dB is still maintained.

The sampling capacitance C_s of the proposed architecture is composed of two parts:

$$C_s = C_h + C_{dac} \tag{1}$$

where C_h is the attenuation capacitance, and C_{dac} the overall DAC capacitance, which is given by:

$$C_{dac} = \sum_{i=0}^{7} C_i \tag{2}$$

The kT/C noise due to sampling depends on the total sampling capacitor C_s as follows:

$$P_{ns} = 2kT/C_s \tag{3}$$

where P_{ns} is the effective differential noise power due to sampling, while the factor of two arises from the differential implementation.

The DAC is implemented with an 8-bit binary-scaled charge-redistribution topology [1]. The digital bits $D_{7\ldots0}$ drive the bottom plates of the binary-scaled capacitors $C_{7\ldots0}$ through a set of inverters. Since the inverters switch between GND and VDD (1 V), the output swing $V_{\mathrm{DAC,pp}}$ of the differential DAC is 2 V (peak-to-peak, differential). Capacitor C_h attenuates the DAC output with a factor H_{dac}:

$$H_{dac} = \frac{C_{dac}}{C_{dac} + C_h} = \frac{C_{dac}}{C_s} \tag{4}$$

thus reducing the effective differential swing of the DAC to:

$$V_{\mathrm{fs,pp}} = V_{\mathrm{DAC,pp}} \cdot H_{dac} = 2\frac{C_{dac}}{C_s} \quad [\mathrm{V}] \tag{5}$$

In this way, the effective peak-to-peak differential input range of the ADC also becomes $V_{\mathrm{fs,pp}}$. Even though a large signal swing can improve the power efficiency of the ADC, from a system point of view, a smaller swing can be more practical. For example, in the intended application, the ADC will be preceded by a baseband amplifier, which will benefit from a smaller swing because of linearity and gain requirements. In this case, the range reduction is implemented by including attenuation capacitor C_h, such that the reference voltage of the DAC can be made equal to the supply of 1 V. Alternatively, the reference voltage can be scaled down, such that C_h can be omitted. However, in that case an additional voltage-domain would be needed, which adds complexity and power consumption outside the ADC. Moreover, to maintain the same noise-level, (3) implies that C_s needs to remain constant, thus when omitting C_h, C_{dac} has to be increased (1). The increase of C_{dac} counteracts the expected advantage of reducing the reference voltage. Since the power consumption of the DAC is relatively small compared to the overall power consumption, while none of the approaches is obviously more power efficient, the approach with an attenuation capacitor is preferred here since it simplifies the system design and prevents the need for an additional external voltage regulator.

The kT/C noise from the DAC is characterized by the effective capacitance which loads the DAC drivers (i.e. capacitors C_{dac} and C_h in series), and taking into account the attenuation effect (4):

$$P_{nd} = \frac{2kT(C_{dac} + C_h)}{C_{dac}C_h} \cdot H_{dac}^2 = \frac{2kTC_{dac}}{(C_{dac} + C_h)C_h} \tag{6}$$

where P_{nd} is the effective differential noise power from the DAC, while the factor of two arises from the differential implementation.

The settling time of the DAC is determined by the transistors composing the DAC drivers and their capacitive load. The comparator, optimized for low-power and not for high-speed, limits the speed of the ADC. While the comparator is being reset, which takes about 3 ns, the DAC is switched and starts settling to the next level. As long as the DAC settles within 3 ns, it will be ready before the next comparison starts. This requirement can be achieved easily, thus the DAC uses rather small devices while still being able to settle within 0.5 LSB in less than 2.5 ns according to post-layout simulations. Also, since the reference voltages of the DAC are equal to GND and VDD, the switches are driven by a V_{gs} equal to VDD, which is beneficial for the settling time.

For the proposed circuit, the effective differential signal power (assuming a full-scale sinusoid) can be expressed as follows, using (5):

$$P_s = \frac{1}{2}\left(\frac{V_{\mathrm{fs,pp}}}{2}\right)^2 = \frac{C_{dac}^2}{2C_s^2} \quad [\mathrm{V}^2] \tag{7}$$

Since the power consumption of a switched capacitor circuit is proportional to the capacitor values, C_s has to be minimized for a low-power design. For $C_s = 308$ fF and $C_{dac} = 128$ fF, a signal power $P_s = 86\mathrm{e}{-3}\mathrm{V}^2$ is obtained, while P_{ns} and P_{nd} are $28\mathrm{e}-9\mathrm{V}^2$ and $21\mathrm{e}-9\mathrm{V}^2$, respectively. Since both noise levels are 65 dB below the signal level, the performance is sufficient for an 8 bit ADC. At the same time, the signal-range becomes $V_{\mathrm{fs,pp}} = 0.83$ V with an LSB of 3.2 mV, which is a practical range for the intended receiver application. Since C_{dac} is composed of 8 binary scaled capacitors, the implication of choosing C_{dac} equal to 128 fF is that the unit element (C_0) has to be as small as 0.5 fF. From standard libraries, such small capacitors are not available. However, the sizing is key to minimize the power consumption of the switched-capacitor circuit. For that reason, custom-designed capacitors are proposed, which will be introduced in the following section.

B. Capacitor Implementation

The implementation of capacitors with small values is crucial to achieve a high power efficiency and a high accuracy. Because of the need for small but precisely-matched capacitor

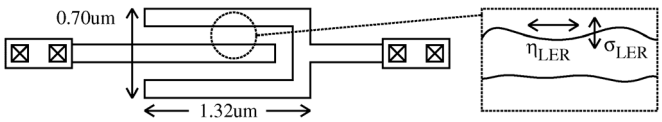

Fig. 3. 0.5 fF unit capacitor implementation, with a zoom-in window for indicating the LER effect.

elements, this work proposes a custom-designed metal–metal capacitor with a small value of 0.5 fF as shown in Fig. 3. The proposed structure uses metal layers 6 and 7 stacked together with minimum metal width and minimum metal spacing (both 0.14 μm). The structure results in three parasitic components: the intended parasitic capacitance between the two nodes of the structure, which is designed to be 0.5 fF based on standard parasitic extraction tools. Next to that, two additional unintended parasitics are present, namely from each node to GND. By choosing metal layers 6 and 7 instead of the lower metal layers, and by choosing minimum width and spacing, the unintended parasitics are minimized. Note that these unintended parasitics do not reduce the accuracy since they are either in parallel to the DAC driver or in parallel to C_h. In the first case, they increase the power consumption and settling time of the DAC, but they do not change the charge-redistribution function. In the second case, they contribute to C_h, and can be taken into account during the design. Since the proposed capacitor uses only standard metal layers, it can be implemented in any standard digital CMOS process. Moreover, with scaling of technology, it can be made even smaller in physical size.

Fig. 4 shows a small part of the layout of one side of the differential capacitor array: two rows of 265 capacitors are implemented: the first row consists of the 255 unit elements for the DAC and 10 elements for C_h, while the second row implements the remaining elements for C_h. Note that the area-penalty to implement C_h is only 4.5 μm out of 18 μm total height, thus about 25% of the total size. Mismatch between C_h and C_{dac} results in gain variations of this ADC. For C_h, only a small part (43 fF) is determined by indirect parasitics: 21 fF from the layout interconnect, and another 22 fF from the comparator. The largest part (136 fF) is implemented by the same unit capacitors which are also used to compose C_{dac}. Therefore, C_h can be matched reasonably well to C_{dac} considering PVT variations. E.g., for 10% variation in the 43 fF-value, only 1.5% gain-variation is observed, which can be neglected for the intended application scenario.

The DAC drivers are connected by the 8 horizontal wires, while the elements are combined using a common-centroid approach. Because of the narrow shape of the capacitors, all elements can be laid out on a single row instead of using a 2-dimensional array, as is typically the case for a MIM capacitor based implementation. Being only one-dimensional, the top-level connectivity is relatively simple. The total size of the differential capacitor array, including DAC drivers and sampling switches is 160 μm $\times$ 45 μm. A top-level parasitic extraction is done on the structure to verify the parasitics and to confirm proper binary scaling of the array. Table I shows the relevant results: proper binary scaling is achieved, the small deviations are caused by numerical truncation from the extraction tool. The

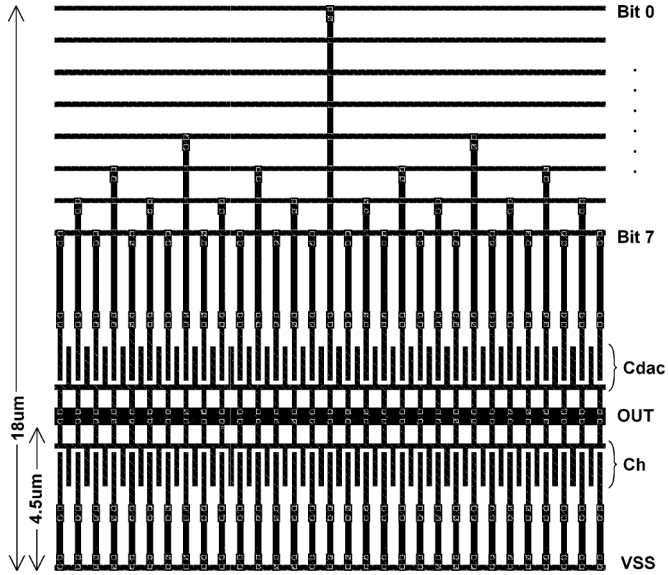

Fig. 4. Partial layout of the capacitor array.

TABLE I
EXTRACTED CAPACITORS AND THEIR NORMALIZED VALUE

Capacitor	Value (fF)	Normalized value
C_0	0.4932	1.00
C_1	0.9868	2.00
C_2	1.973	4.00
C_3	3.947	8.00
C_4	7.893	16.00
C_5	15.78	31.98
C_6	31.57	63.99
C_7	63.15	128.00
C_h	157	

157 fF capacitance of C_h is based on 275 unit capacitors (136 fF), while the remaining 21 fF is present because of the interconnect and capacitor parasitics. Note that the comparator will add an additional component to C_h. The total DAC capacitance equals 126 fF. However, mainly due to the common-centroid layout, there are relatively large interconnect parasitics present, resulting in a total load of 377 fF for the DAC (of which 251 fF is redundant). Thus, with the current layout, further down-scaling of the unit elements is not advantageous to reduce the power consumption. Instead, improving the interconnect or grouping the elements differently will have more impact.

C. Capacitor Variability

For the linearity performance of the ADC, the mismatch of the unit capacitors of the DAC has to be low enough. Since the mismatch of custom-build metal structures is not known beforehand, a variability study has been carried out. In this section, the matching requirements are discussed first. Then, a comparison to technology-provided MIM capacitors is used to come to a first estimate of the precision of the proposed structure. Finally, based on dedicated CAD tools, the capacitor variability of the

proposed structure is estimated. Later on, in Section V, measurement results are used to verify the matching performance.

For the requirement for capacitor matching, the mid-code transition is considered as the worst-case, since at this transition, all the capacitors in a binary-scaled design are active. The requirement is set to a maximum DNL error of 0.5 LSB, for a 3σ deviation:

$$3\sigma_{\mathrm{DNL,mid}} < \frac{1}{2}\mathrm{LSB} \tag{8}$$

The unit capacitors are modeled with a nominal value of C_u and a standard deviation of σ_u. A differential 8-bit binary-scaled DAC is composed of 510 C_u-elements ($2\cdot(2^8-1)$), with an LSB step of $2C_u$ (note that the factor of two arises from the differential implementation). At the MSB code transition (from code 01111111 to code 10000000) all 510 capacitors are switched, thus leading to a σ of

$$\sigma_{\mathrm{DNL,mid}} = \frac{\sqrt{510}\sigma_u}{2C_u} \tag{9}$$

Combining (8) and (9) results in a requirement of 1.5% capacitor matching in order to achieve 8 bit accuracy performance:

$$3\frac{\sqrt{510}\sigma_u}{2C_u} < \frac{1}{2} \Rightarrow \frac{\sigma_u}{C_u} < 1.5\% \tag{10}$$

To give a first indication of the matching performance of the proposed structure, a capacitor provided by the technology is considered for comparison. Since no data on MOM capacitors was available, data from a MIM capacitor is used instead. Since the MIM capacitor is a plate capacitor, the proposed structure from Fig. 3 is also considered as a (folded) plate capacitor with area A and plate-distance d: the distance d corresponds to the metal spacing (0.14 μm), while the area is given by the stacked height of the used metals ($2 \cdot 0.31$ μm) times the length of the outline of the fork (≈ 2.78 μm), resulting in an area A of 1.7 μm^2. Since the plate capacitance is given by

$$C = \frac{\epsilon_0\epsilon_r A}{d} \tag{11}$$

assuming $\epsilon_r = 4$, this correctly estimates the capacitance to be around 0.43 fF. This calculation reveals that, despite the small capacitor value, the occupied area (1.7 μm^2) is actually large. A typical MIM capacitor in this technology node can have a density of 2 fF/μm^2 and a matching of 1%. This value is defined as the matching between two random capacitors, while the definition of σ_u in this work considers the standard deviation of a single capacitor compared to the mean value. Thus, to match to the definition in this work, the 1% MIM capacitor matching reduces by $\sqrt{2}$ to 0.7%. Then, to estimate the matching performance for the same area (1.7 μm^2), the result is further divided by $\sqrt{1.7}$, since the matching is inverse proportional to the square-root of the area. Thus, a MIM capacitor with the same area as the proposed structure achieves a matching of 0.54%. However, since its plate-distance d is about 6 times less than the proposed design, it is expected that the proposed design can achieve a matching which is even a factor better than 0.54%. Though this calculation indicates that it is possible to achieve the required precision for such small components, it has to be emphasized that, since this comparison is based on different structures with different processing, it does not provide a precise result.

A more advanced estimate of the variability is done using a dedicated CAD tool in combination with process modeling: the mismatch comes from various random fluctuations during the manufacturing process. In case of a metal-metal capacitor, the sidewalls of two metals facing each other are the main contributions to the intended capacitance. In other words, the distance between the sidewalls is a crucial parameter. Hence the line-edge roughness (LER) is considered to be the main cause of the mismatch (see Fig. 3). The LER of metals originates from the photo-resist LER generated during the lithography process and is further affected in the subsequent etching process.

Since there is unfortunately no commercial layout parasitic extraction (LPE) tool available to take into account the LER, a Monte Carlo simulation has been conducted, using a customized static solver [2], to evaluate the mismatch of the intended parasitic capacitance caused by the LER. To do so, 1000 groups of random line patterns (for 1000 MC samples), as inputs of the extraction tool, are generated based on the physical model of LER. The LER is usually characterized with two parameters, namely the standard deviation (σ_{LER}), representing the absolute roughness amplitude orthogonal to the line-edge, and the correlation length (η_{LER}) along the line-edge, as indicated in Fig. 3. These two parameters largely depend on the materials and the manufacturing process and thus should be carefully chosen. While not being able to get the estimation of σ_{LER} and η_{LER} from the technology based on which the chip has been fabricated, the two parameters are chosen according to the measurement data of copper-wires in meander-fork structures, provided by IMEC [3]: $\sigma_{LER} = 3.5$ nm and $\eta_{LER} = 16$ nm, as this is the closest data available on a similar scale technology. The random lines are then obtained from the inverse Fourier transform of the power spectrum for the corresponding spatial autocorrelation function [4], characterized by σ_{LER} and η_{LER}. Then, every sample structure with the generated random line pattern is solved using the customized extraction tool [2], obtaining 1000 capacitance samples. The relative standard deviation of the capacitance (σ_u/C_u) can therefore be estimated. According to the MC simulation results, the relative standard deviation of the 0.5 fF unit capacitor is approximately 0.25%. Although there are various random variations during the manufacturing process, considering LER is the primary contributor, this design using minimum metal spacing should have enough margin to achieve 8-bit performance.

D. Dynamic Comparator

The comparator is crucial for the overall power consumption. As shown in Fig. 5, a two-stage dynamic comparator is used [5]. Since this design has no static biasing, the average power consumption scales proportional to the sampling rate. In each current-path of the comparator, at least one high-V_t device is used to limit the leakage, while sufficient voltage-headroom and speed is maintained by the remaining low-V_t devices. This ensures good power efficiency for a wide range of sample rates. Furthermore, to minimize the active power consumption,

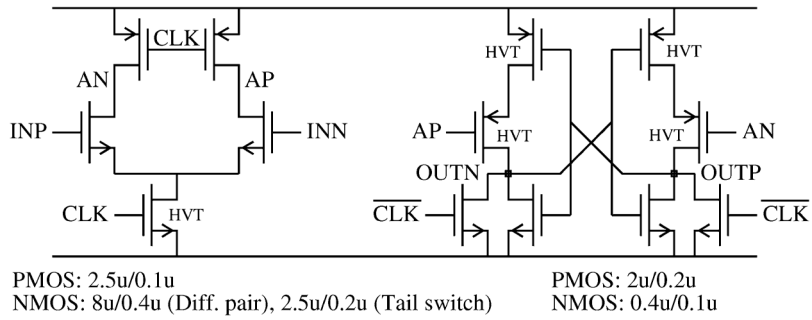

Fig. 5. High-speed, low-leakage dynamic comparator.

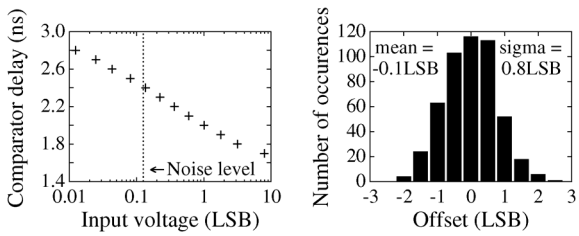

Fig. 6. Simulated comparator delay and offset (500 MC runs).

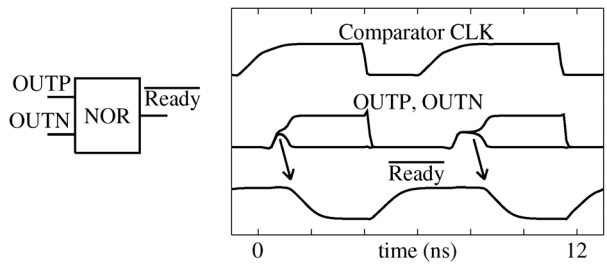

Fig. 7. Ready-indication of the comparator.

the layout of only 10×30 μm^2 is optimized for low parasitics and dynamic offset matching, the latter being achieved by using dummy transistors and dummy metal wiring. The simulated gain of the first stage is around 6, and the noise level of the total comparator equals $P_{nc} = 90\text{e}-9\text{V}^2$, corresponding to $\sqrt{90\text{e}-9}/3.2\text{e}-3 = 0.09$ LSB. Thus, the total noise including contributions from the sampler, DAC and comparator becomes P_n:

$$P_n = P_{ns} + P_{nd} + P_{nc} = 140\text{e}-9\ \text{V}^2 \qquad (12)$$

which corresponds to 0.12 LSB and is confirmed by noise simulations on the complete analog circuit. Fig. 6 shows the simulated delay of the comparator, and the offset performance using MC simulations on schematic level. With a noise level around 0.1 LSB, the delay will be 2.4 ns at most. For the intended sample rate, this relatively short delay prevents metastability issues. The offset of a few LSB can be ignored for the ADC target application. While an additional post-layout offset simulation estimates a systematic 0.4 LSB offset due to capacitive mismatch, this might be inaccurate as it is not confirmed by measurements.

Since the implemented logic in this ADC is asynchronous, a *ready*-indication from the comparator is used to control the timing of the state-machine. As shown in Fig. 5, the two outputs of the latch (OUTP and OUTN) are pre-charged low. As soon as the comparator has taken a decision, one of the two outputs will go high. A logical NOR operation detects this low-to-high transition and generates an active-low *ready*-indication as shown in Fig. 7. A combination of high-V_t and low-V_t transistors is used in the NOR-gate to ensure that the output is valid before the ready-signal.

III. Asynchronous Dynamic Logic

While the analog power consumption is minimized by reducing the size of the capacitors, also the digital power consumption needs to be minimized to achieve a low overall power consumption. This is especially important because of the relatively low resolution of the ADC: for analog components, the size is often exponentially related to the number of bits N, e.g. in case of a noise-limited or matching-limited design. Thus, the related power consumption is also exponentially related to N. On the other hand, the digital logic in a SAR converter is linear proportional to the resolution N. As a result, for a relatively low resolution design (8 bit), in which the analog power consumption is optimized, the digital power consumption can become dominant. For that reason, asynchronous dynamic logic is introduced which reduces the complexity of the digital logic, and thus reduces the power consumption compared to a standard CMOS implementation. By using dynamic logic instead of complementary logic, less transistors are needed to implement the same functionality. Next to that, since the logic is asynchronous, it requires only a low-speed sample-rate clock instead of an oversampled clock, thereby saving power in the clock structure and simplifying the required scalability in the data rate.

A. Logic Implementation for One-Bit Cycle

The logic of the SAR ADC performs a binary search algorithm in eight identical cycles. In this section, the design of the asynchronous dynamic logic for one bit cycle will be discussed. Fig. 8 shows a conceptual state diagram for one bit cycle: first, a new bit in the DAC will be set. A comparison is performed and the result determines which final value will be stored in the DAC register. In a synchronous system, these three steps are executed in succession by making use of an oversampled

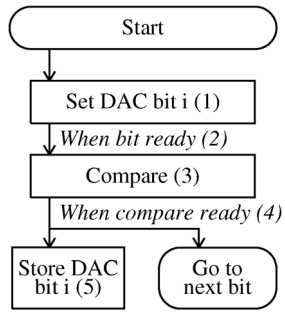

Fig. 8. State machine for one bit cycle.

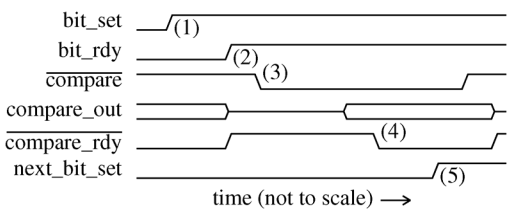

Fig. 9. Timing diagram for one bit cycle.

clock. To achieve consecutive operation of these three steps in an asynchronous system, self-synchronization is used. For each state-transition, a specific condition will be tested to make sure that the previous step is finished before starting with the next step: the comparison will only start after the DAC bit is properly set, while the result is only stored after the comparison is finished. In this way, the steps are executed consecutively without the help of an oversampled clock for synchronization. An illustration of the behavior in time is shown in Fig. 9: first, the bit is set (indicated with (1) in the figure). As soon as it is ready (2), the comparison will be initiated (3). After some time, the output of the comparator is valid which will be indicated by a ready signal (4), based on which the result is stored and the next cycle will be initiated (5).

The logic to implement the diagram from Fig. 8 is split in two parts, as shown in Fig. 10: the main control implements the flow of the SAR algorithm and the DAC control implements the SAR register. The output signals ($\overline{\text{compare}}$, next_bit_set, DACP and DACN) correspond directly to the state bits, while the conditions for each transition are indicated next to the state-transition arrows. The main control starts in state '10'. When the DAC bit is set and ready, the state changes to '00' in which the $\overline{\text{compare}}$ output goes low to request a comparison. Note that one additional condition is tested ($\overline{\text{compare\_rdy}} = 1$) to make sure the comparator is ready to start a new comparison. Then, as soon as the comparator is ready ($\overline{\text{compare\_rdy}} = 0$), the state advances to '01' and the operation is handed over to the next bit iteration by enabling the next_bit_set output. In parallel to the main control, the DAC control starts in state '1', in which the DAC bit is turned off. When a bit-set is requested while no comparison is active, the state changes to '0', in which the bit is set. The positive output DACP generates the bit_rdy signal as required by the main control. When the comparison is valid ($\overline{\text{compare\_rdy}} = 0$), the DAC control either remains in the present state or changes back to state '1', dependent on the comparator result (compare_out). The condition $\text{next\_bit\_set} = 0$ is also checked since it indicates which of the eight bit cycles is active.

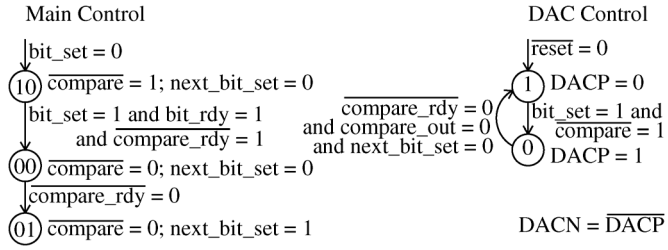

Fig. 10. State machine of the main control and the DAC control.

Fig. 11 shows the dynamic logic implementation that corresponds directly to the diagrams from Fig. 10. Capacitances C_1 up to C_3 are used as memory elements to store the state while dynamic logic is used to implement the state transitions. C_1 up to C_3 are exclusively based on the parasitics of the connected transistors. By proper sizing of the these transistors, it has been verified that the stored logic levels remain reliable during operation. The direct relation between the state-diagram and the logic is illustrated for the DAC control. For example, corresponding to Fig. 10, Fig. 11 shows that the state changes to '1' if either $\overline{\text{reset}} = 0$ or $\overline{\text{compare\_rdy}} = \text{compare\_out} = \text{next\_bit\_set} = 0$, while the state changes to '0' if $\text{bit\_set} = 1$ and $\overline{\text{compare}} = 1$. Note that bit_rdy, generated by DACP, only indicates that the DAC control bit is set properly, it does not imply that the analog DAC output level is settled. Proper DAC settling is thus not ensured by the logic itself, but it is ensured by the fact that the comparator reset-phase (which is done in parallel to the DAC settling) takes more time (3 ns) than the DAC settling (2.5 ns).

B. Overall Logic Overview

Fig. 12 shows the overall architecture of the logic for the SAR ADC. Next to the eight slices of the main control and DAC control, a comparator control and a standby control are implemented. The comparator control has to generate a high-level on the comparator clock input when one of the slices of the main control is in the *compare*-state, encoded by $C_1C_2 =$ '00' as shown in Fig. 10. Thus, the comparator control is a simple logic operation on the states of the 8 slices, and is implemented with a complementary logic function:

$$\text{comparator\_clk} = \sum_{\text{slice } i=0}^{7} \overline{C}_{1,i}\overline{C}_{2,i} \tag{13}$$

A standby control is implemented to minimize the power consumption at low sampling rates, thereby extending the power efficiency to a wider range of sampling rates. At low sampling rates, the power consumption of the ADC is dominated by leakage currents. It should be noted that the leakage currents are strongly dependent on the logic state of the implemented state-machine. In this design, the leakage current is minimized for only one specific state, namely the *standby state*. Furthermore, the standby control block guarantees that the ADC will remain in this state as long as possible: as shown by the timing diagram (Fig. 13), the standby control turns on the internal clock as soon as a conversion is requested by a rising edge of

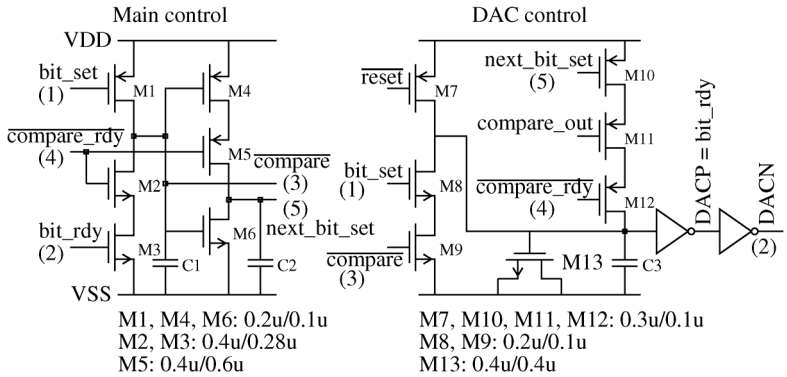

Fig. 11. Implementation of the main control and the DAC control.

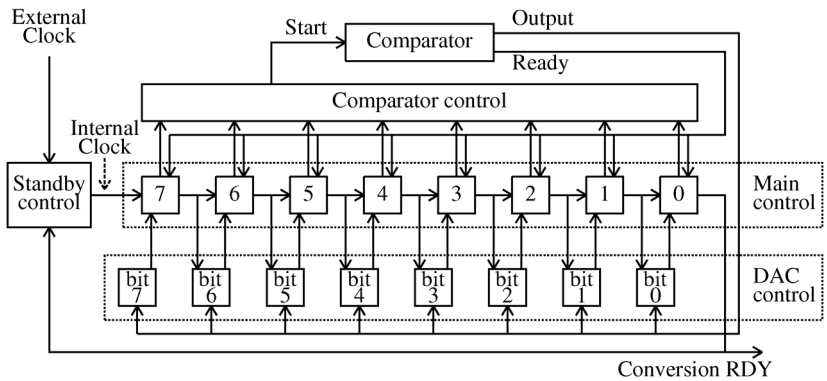

Fig. 12. Simplified overview of the asynchronous control logic.

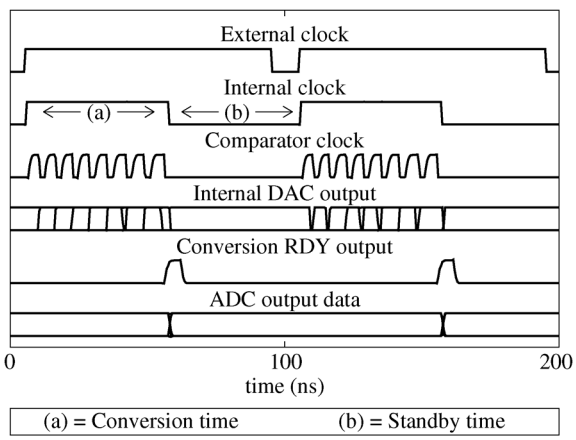

Fig. 13. Simplified timing diagram of the control logic.

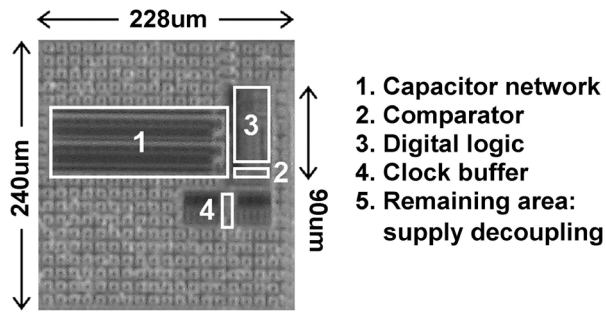

Fig. 14. Die photo of the ADC including decoupling capacitors.

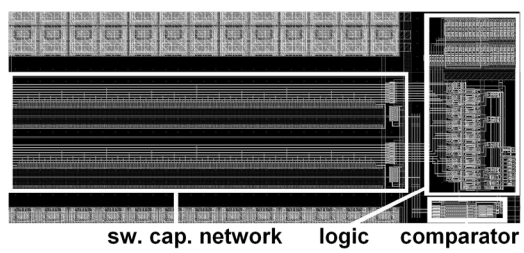

Fig. 15. ADC layout.

the external clock. As soon as the conversion is finished, the standby control disables the internal clock. Thus, regardless of the duty cycle or frequency of the external clock, the standby control minimizes the conversion time (indicated by *(a)* in the figure), while it maximizes the standby time (indicated by *(b)* in the figure). By automatically maximizing the standby time and by minimizing the leakage currents for the standby state, the average power consumption at low speed operation is minimized.

IV. Chip Implementation

Fig. 14 shows a die photo of the realized ADC in a 90 nm CMOS technology. The core occupies 90×228 μm^2, while the remaining area in the figure is used for supply decoupling (26 pF for the DAC, 32 pF for the logic and 18 pF for the clock buffer). For clarity, Fig. 15 shows the layout including the switched capacitor network, the digital logic and the comparator. Note that the manually designed logic is not yet optimized for small area. The ADC is packaged (with several other designs) in a QFN80 package for testing.

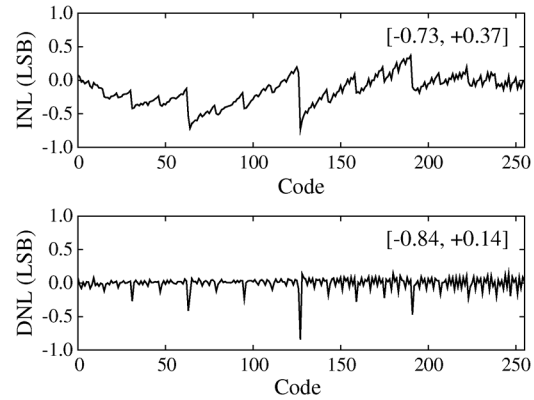

Fig. 16. Measured INL and DNL at 10.24 MS/s.

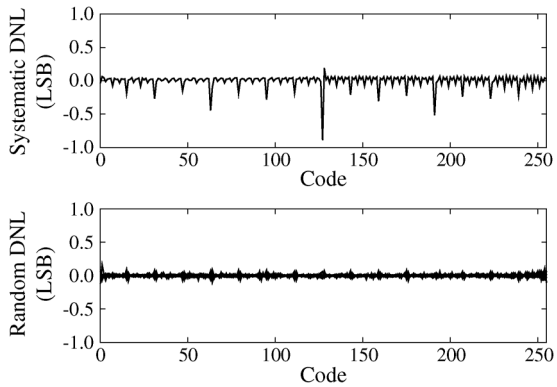

Fig. 17. Measured systematic and random DNL for nine chips.

V. Measurement Results and Analysis

The performance of the ADC was measured at 1 V supply and 10.24 MS/s. Fig. 16 shows that the measured INL and DNL are within 0.73 LSB and 0.84 LSB, respectively. The average sigma of the DNL over all 256 codes equals $\overline{\sigma_{\mathrm{DNL}}} = 0.1$ LSB. Summing (in the power domain) this $\overline{\sigma_{\mathrm{DNL}}}$-term, the simulated noise P_n of 0.12 LSB, and ideal quantization noise of $1/\sqrt{12} = 0.289$ LSB, this leads to a total of 0.33 LSB, thus estimating a static ENOB of 7.8 bit. For a more detailed analysis of the matching of the unit capacitors, the DNL was measured for nine test-chips. The worst-case $\mathrm{INL}_{\max}/\mathrm{DNL}_{\max}$ on nine measured samples equals 0.9 LSB. To distinguish systematic and random errors, the DNL is split into two parts: systematic DNL and random DNL. The systematic DNL is obtained by averaging the nine measured DNL curves. Then, the random DNL curves are obtained for each measured sample by subtracting the systematic DNL from the DNL. Thus, Fig. 17 shows the measured systematic DNL and random DNL for all chips. As can be observed, the systematic DNL is dominant for the overall DNL, which suggests that a systematic layout issue, which is not detected by the extraction tool, is causing DNL performance loss. From the random DNL component, the matching performance of the unit capacitors can be analyzed. Using (9), an estimate for σ_u/C_u can be calculated based on the measured $\sigma_{\mathrm{DNL,mid}}$ at the MSB transition. More generally, for each bit i (where the MSB corresponds to $i = 7$), the related code transition can estimate σ_u/C_u according to

$$\frac{\sigma_u}{C_u} = \frac{2\sigma_{\mathrm{DNL}_i}}{\sqrt{2 \cdot (2^{i+1} - 1)}} \tag{14}$$

where DNL_i is the DNL at the code transition of bit i, while the term $2 \cdot (2^{i+1} - 1)$ accounts for the number of active capacitors at this transition. Fig. 18 shows the estimated capacitor matching for each bit transition, averaged over the nine measured samples. For comparison and confirmation of (14), the results of a simulation are also shown. The MC simulation takes capacitor mismatch (0.5% or 1%) and random noise into account, calculates the DNL plots, and uses (14) to estimate the capacitor matching. For the LSB transitions, the estimation is inaccurate due to noise. From the figure, the capacitor matching is estimated to be better than 1%, possibly in the order of 0.5% or less, which corresponds to the estimate from Section II.

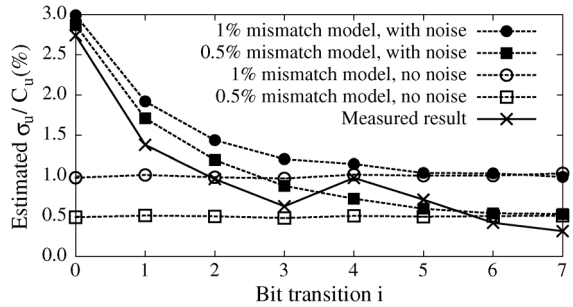

Fig. 18. Estimated capacitor matching based on DNL measurements.

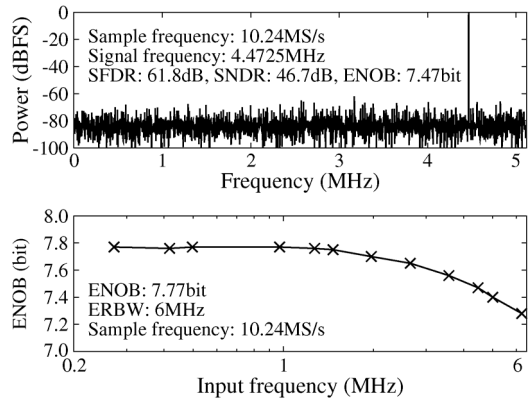

Fig. 19. Measured spectrum (4096-point FFT) and ENOB at 10.24 MS/s.

Fig. 19 shows an output spectrum for a near-Nyquist tone and the ENOB as function of the input frequency. The ENOB equals 7.77 bit, while the ERBW (6 MHz) is slightly beyond Nyquist. The ENOB-loss at higher frequencies is due to a 2.4 fF capacitive coupling across the sampling switch, causing a frequency-dependent fluctuation of the sampled voltage during the conversion process. This is confirmed by a DNL-plot for a near-Nyquist tone, which is shown in Fig. 20. This DNL-plot was calculated according to well-established histogram measurements [6] and, since it uses a near-Nyquist input tone, includes both static and dynamic effects. A MATLAB simulation which models the capacitive coupling is also shown

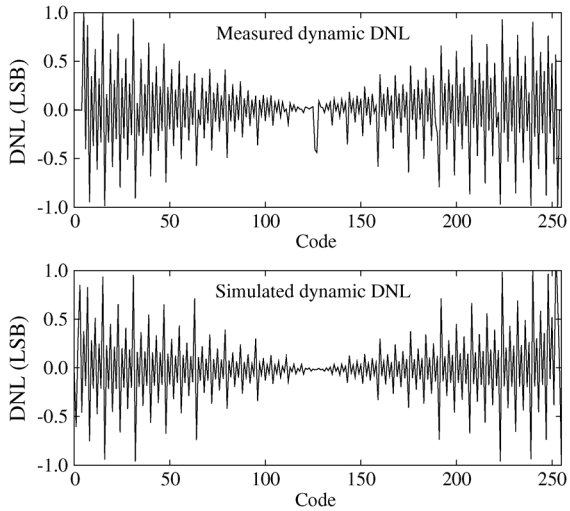

Fig. 20. Measured and simulated dynamic DNL, using $f_{in} = 4.49989$ MHz and $f_{sample} = 10.48576$ MHz.

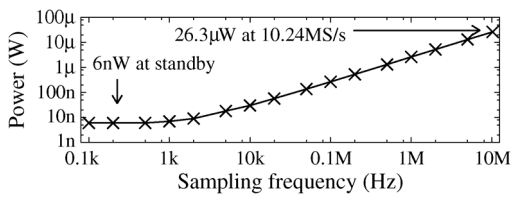

Fig. 21. Measured power consumption as a function of the sampling frequency.

TABLE II
SIMULATED ENERGY CONSUMPTION PER CONVERSION

	Schematic	**Parasitics**	**Post-layout**
Clock driver	134fJ (5%)	46fJ (2%)	180fJ (7%)
DAC	198fJ (8%)	438fJ (17%)	636fJ (25%)
Comparator	565fJ (22%)	303fJ (12%)	868fJ (34%)
Logic	477fJ (19%)	382fJ (15%)	859fJ (34%)
Overall	1374fJ (54%)	1169fJ (46%)	2543fJ (100%)

and exhibits the same signature as the measured result. This issue can be resolved by a more careful layout of the sampling switch, as demonstrated by a similar version of this chip [7], which does not exhibit significant ENOB-loss.

Fig. 21 reveals that the power consumption scales linearly with the sampling rate, reaching 26.3 μW at 10.24 MS/s and 6 nW below 0.5 kS/s. The presented numbers are measured when a full-scale sine is applied as input signal. For a PRBS input signal or a zero-DC input level, the power consumption changes with $+2\%$ and -5%, respectively. Table II shows the distribution of the power consumption according to simulations, where the parasitics consumption is estimated by subtracting the schematic-based result from the post-layout result. Obviously, unintended parasitics consume a large part of the total power (46%). This can be improved by optimizing the layout, but is partially also inherent from a low-speed, low-accuracy design, in which transistor dimensions are relatively small and hence the interconnect is more significant. According to simulations, the current peaks drawn from the supply can be as high as 0.4 mA and 1.6 mA for the DAC reference supply and the ADC supply, respectively. Since these peaks are short (<2 ns) and sufficient on-chip decoupling capacitors are implemented, they can be reduced by adding series resistors in the supply. Measurements confirm that with 1 kΩ series resistors in DAC reference and ADC supply, the resulting ENOB reduction is less than 0.1 bit, while simulations estimate that these resistors reduce the peak currents to less than 20 μA. For a further peak-reduction, external decoupling capacitors could be added. At the same time, the supply filtering and the DAC attenuation (4) reduce the impact of external supply noise.

TABLE III
MEASURED PERFORMANCE SUMMARY

Technology	90nm CMOS
Chip area	228μm$\times$240μm
Power supply	1V
Power consumption	26.3μW at 10.24MS/s
Power consumption standby	6nW
Common-mode level	0.5V
Signal range (peak-peak, diff.)	0.83V
ERBW	6MHz
ENOB	7.77bit
FoM	12fJ/conversion-step
Maximum INL, DNL *	0.9LSB
Offset *	max.: 1.4LSB, σ: 0.9LSB, mean: 0.01LSB
Gain variation (amongst samples) *	max.: 1.1%, σ: 0.5%

* for nine measured samples

Because of the asynchronous operation, the conversion time remains constant regardless of the sampling rate (Fig. 13). As the operation and timing of the conversion process are fixed, the accuracy is maintained for reduced sampling rates since e.g. leakage effects will not increase at lower speeds. Using the FoM definition originating from [8]

$$\mathrm{FoM} = \frac{\mathrm{Power}}{2^{\mathrm{ENOB}} \cdot \min(\mathrm{f_s}, 2\mathrm{ERBW})}, \qquad (15)$$

an efficiency of 12 fJ/conversion-step is achieved at 10.24 MS/s. Since the power consumption of the implemented dynamic circuitry scales proportional to VDD^2, the FoM improves to 9 fJ/conversion-step at 0.9 V supply but degrades to 16 fJ/conversion-step at 1.1 V supply. A summary of the measured performance is given in Table III, while Table IV shows a comparison to existing SAR ADCs with similar speed and resolution, based on [9]. Compared to other 8-bit ENOB-designs ([7] and [10]), this design achieves the best power-efficiency. When compared to a wider range of SAR converters, this design still achieves a good efficiency.

VI. CONCLUSION

In this work, an ultra-low-power 8-bit SAR ADC with an efficiently scalable sample rate for wireless sensor nodes was presented. By using dedicated 0.5 fF capacitors, asynchronous dynamic logic and a low-complexity design, an energy efficiency

TABLE IV
PERFORMANCE COMPARISON

	[7]	[10]	[11]	[12]	[13]	[5]	This work
Technology	90nm	90nm	90nm	65nm	180nm	65nm	90nm
Power supply	1V	1V	1V	1.2V	1V	1V	1V
Power	69μW	290μW	0.75mW	1.13mW	98μW	1.9μW	26.3μW
Sampling rate	10.24MS/s	20MS/s	100MS/s	100MS/s	10MS/s	1MS/s	10.24MS/s
Resolution	8bit	9bit	9bit	10bit	10bit	10bit	8bit
ENOB	7.8bit	7.8bit	8.72bit	9.51bit	9.84bit	8.75bit	7.77bit
FoM	30fJ/step	65fJ/step	18fJ/step	15.5fJ/step	11fJ/step	4.4fJ/step	12fJ/step

of 12 fJ/conversion-step could be achieved at 10 MS/s. Because of the fully dynamic design and a low leakage level of only 6 nW, the excellent efficiency is maintained down to the kS/s range.

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