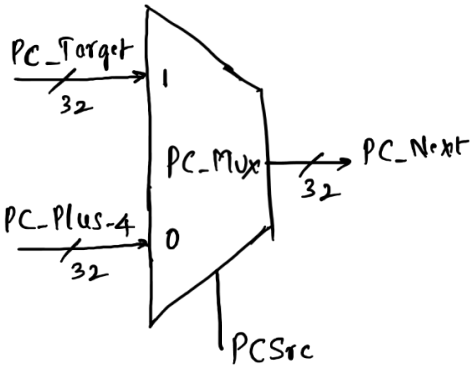
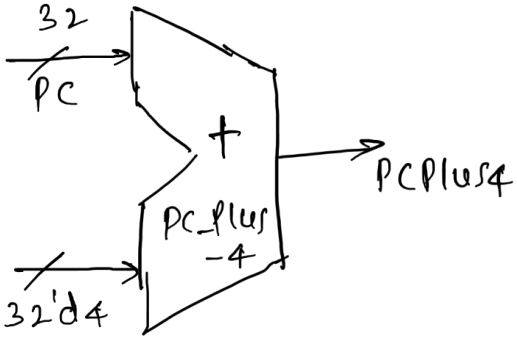
Digital Design with Verilog

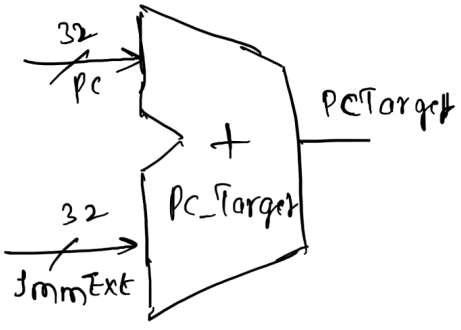
Date: June 12, 2025

Designing of a few Simple Blocks

1. In this tutorial, we shall design some simple blocks. Please stick to the input and output signals







End of Problem Set