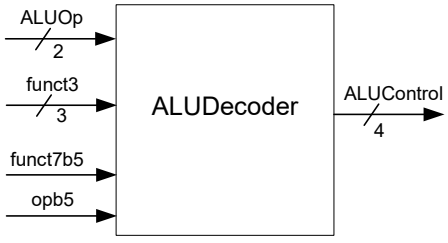
Digital Design with Verilog

Date: June 12, 2025

Designing of an ALU Decoder

1. In this tutorial, we shall design an ALU Decoder such that the our ALU which is designed in the previous tutorial will get proper ALUControl signals.
   (a) Please stick to the input and output signals names as shown in the block diagram below.



   (b) Following is the relation between the two inputs and output.

ALUOp	funct3	funct7b5	opb5	ALUControl
2'b00				4'b0000
2'b01				4'b0001
2'b10	3'b000			4'b0000
	3'b000	1'b1	1'b1	4'b0001
	3'b001			4'b1010
	3'b010			4'b0101
	3'b011			4'b0110
	3'b100			4'b0100
	3'b101	1'b1		4'b1011
	3'b101			4'b1100
	3'b110			4'b0011
	3'b111			4'b0010
	any other			4'bxxxx
2'b11	3'b000			4'b1000
	3'b001			4'b1001
	any other			4'bxxxx
anyother				4'bxxxx

End of Problem Set