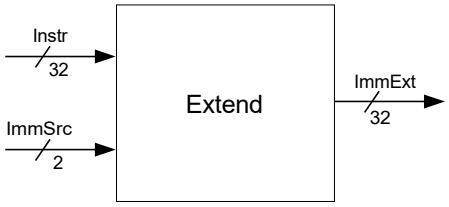
Digital Design with Verilog

Date: June 13, 2025

Designing of Extender

1. In this tutorial, we shall design a sign extender module, whcih will be used later on in some other designs.
   (a) Please stick to the input and output signals names as shown in the block diagram below.



   (b) Following is the relation between the input and outputs.

ImmSrc	ImmExtReg
2'b00	{{20{Instr[31]}},Instr[31:20]}
2'b01	{{20{Instr[31]}},Instr[31:25],Instr[11:7]}
2'b10	{{20{Instr[31]}},Instr[7],Instr[30:25],Instr[11:8],1'b0}
2'b11	{{12{Instr[31]}},Instr[19:12],Instr[20],Instr[30:21],1'b0}
another	32'bx

End of Problem Set