We shall be covering the concepts/ideas in the morning session and in the afternoon session mostly we shall code examples, simulate and port the designs to FPGA. Following is the tentative day-wise plan for the course.

Day	Toipc to be covered		
Day 1	Introduction and Course Outline, Logistics		Verilog: Design and Sumualtion
	Overview of Digital IC Design Flow		
	Review of Combinational Logic Design		
	Fundamentals of Sequential Logic Design	Assigment 1: Problems related to combinational and Sequentail Logic Design	
Day 2	Introduction to Verilog: Design Methodologies, Levels of abstraction, modules, instances		
	Verilog Basics : Lexical Conventions, data types, useful system tasks, compiler directives		
	Testbenches and Simulation	Lab/ Programming Excercises/ Hands-on	
Day 3	Modules and Ports: Anatomy of a module, declarin ports, port connection rules.		
	Gate-level-modelling: Logic gate primitives, construct a Verilog description from logic diagram		
	Data flow modelling: Continuous assignments, Expressions, Operators, and Operands	Lab/ Programming Excercises/ Hands-on	
Day 4	Behavioural Modelling: initail and always blocks, blocking and non-blocking procedural assignments, conditional statements		
	Behavioural Modelling of Sequential Logic: Latches, flip-flops, counters, registers, shift-registers		
	Modeling Memory: Read-only/ Read-Write Memories	Lab/ Programming Excercises/ Hands-on	
Day 5	User Defined Primitives: Defintion and rules, sequential and combinationational UDPs		
	Modelling of Combinational Logic: Decoders, Encoders, multiplexers, De-multiplexers, half-adder, full-adder, binary adder, comparators, partity generators, checkers		
	Usefel Modelling Techniques: force, release, parameters, conditional compilation, some more useful system tasks		
Day 6	Datapath Controller Design: Separating control and data paths, design of both control and data paths	Lab/ Programming Excercises/ Hands-on	
Day 7	Introduction to Verilog Synthesis: Benefits, synthesizable constructs,netlist		Verilog Synthesis
	Mapping of few Verilog HDL types and constants to hardware		
	Value Holders doe Hardware Modeling		
	Synthesis of Verillog Constructs : Logical, Arithmetic, Shift, and Case Operators	Lab/ Programming Excercises/ Hands-on	
Day 8	Synthesis of Conditional Expressions		
	Always constructs		
	Inferring Latches		
	Full Case/ Parallel Case	Lab/ Programming Excercises/ Hands-on	
Day 8	Latch with Asychronous Preset/Clear		
	Loop Statements		
	Modeling Flip-Flops		
	Use of local variables	Lab/ Programming Excercises/ Hands-on	
Day 9	Clock Rules		
	Flip-Flops with Asynchronus Preset/Clear		
	Blocking Vs Non-Blocking	Lab/ Programming Excercises/ Hands-on	

Day 10	Gate-level modelling		
	Parameterized Designs		
	Memory modelling		
			FPGA Architecture
Day 11	FPGA Design Flow : Architecture and mapping		
			RISC-V
Day 12 -15	Introduction to RISC-V		
	RISC-V single cycle and pipelined processor design	Lab/ Programming Excercises/ Hands-on	