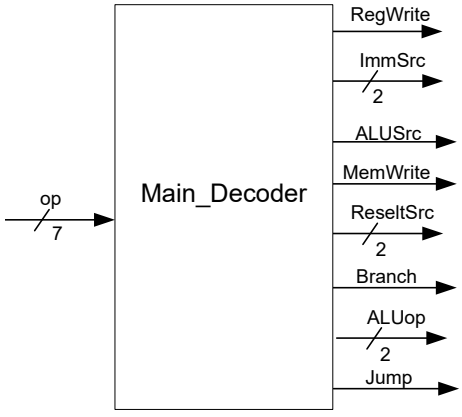
Digital Design with Verilog

Date: June 13, 2025

Designing of Main Decoder

1. In this tutorial, we shall design a Main Decoder, whcih will be used later on in some other designs.
   (a) Please stick to the input and output signals names as shown in the block diagram below.



   (b) Following is the relation between the input and outputs.

op	RegWrite	ImmSrc	ALUSrc	MemWrite	ResultSrc	Branch	ALUop	Jump
7'b0000000	1'b0	2'b00	1'b0	1'b0	2'b00	1'b0	2'b00	1'b0
7'b0000011	1'b1	2'b00	1'b1	1'b0	2'b01	1'b0	2'b00	1'b0
7'b0100011	1'b0	2'b01	1'b1	1'b1	2'b00	1'b0	2'b00	1'b0
7'b0110011	1'b1	2'bxx	1'b0	1'b0	2'b00	1'b0	2'b10	1'b0
7'b0010011	1'b1	2'b00	1'b1	1'b0	2'b00	1'b0	2'b10	1'b0
7'b1100011	1'b0	2'b10	1'b0	1'b0	2'b00	1'b1	2'b01	1'b0
7'b1101111	1'b1	2'b11	1'b0	1'b0	2'b10	1'b0	2'b00	1'b1
7'b1100111	1'b1	2'b00	1'b1	1'b0	2'b10	1'b0	2'b00	1'b1
7'b0110111	1'b1	2'b00	1'b1	1'b0	2'b00	1'b0	2'b11	1'b0
7'b0010111	1'b1	2'b00	1'b1	1'b0	2'b00	1'b0	2'b01	1'b0

End of Problem Set