# Introduction to Standard Cell Design

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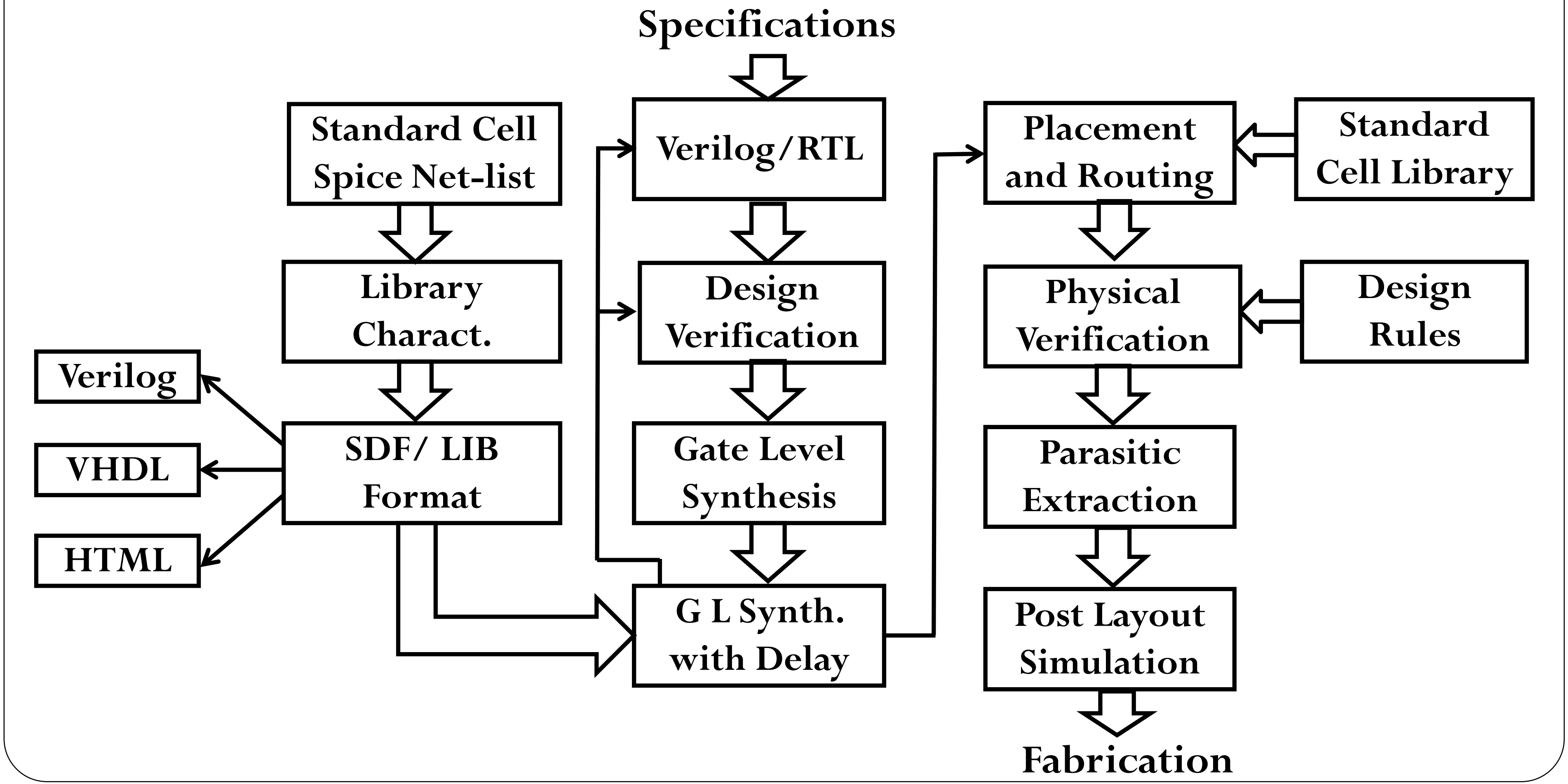
# Overview

- Digital Design Flow
- Standard-Cell vs Full-Custom Design
- Standard Cell Library
- Standard Cell
    - Layers
    - Dimensions
    - Template
    - Track and Grid
    - Pin and Via
    - Design Rules and Constraints
    - Library and Cell Types
    - Liberty file
    - Library Exchange Formant file

# Digital Design Flow



# Standard-Cell vs Full-Custom Design

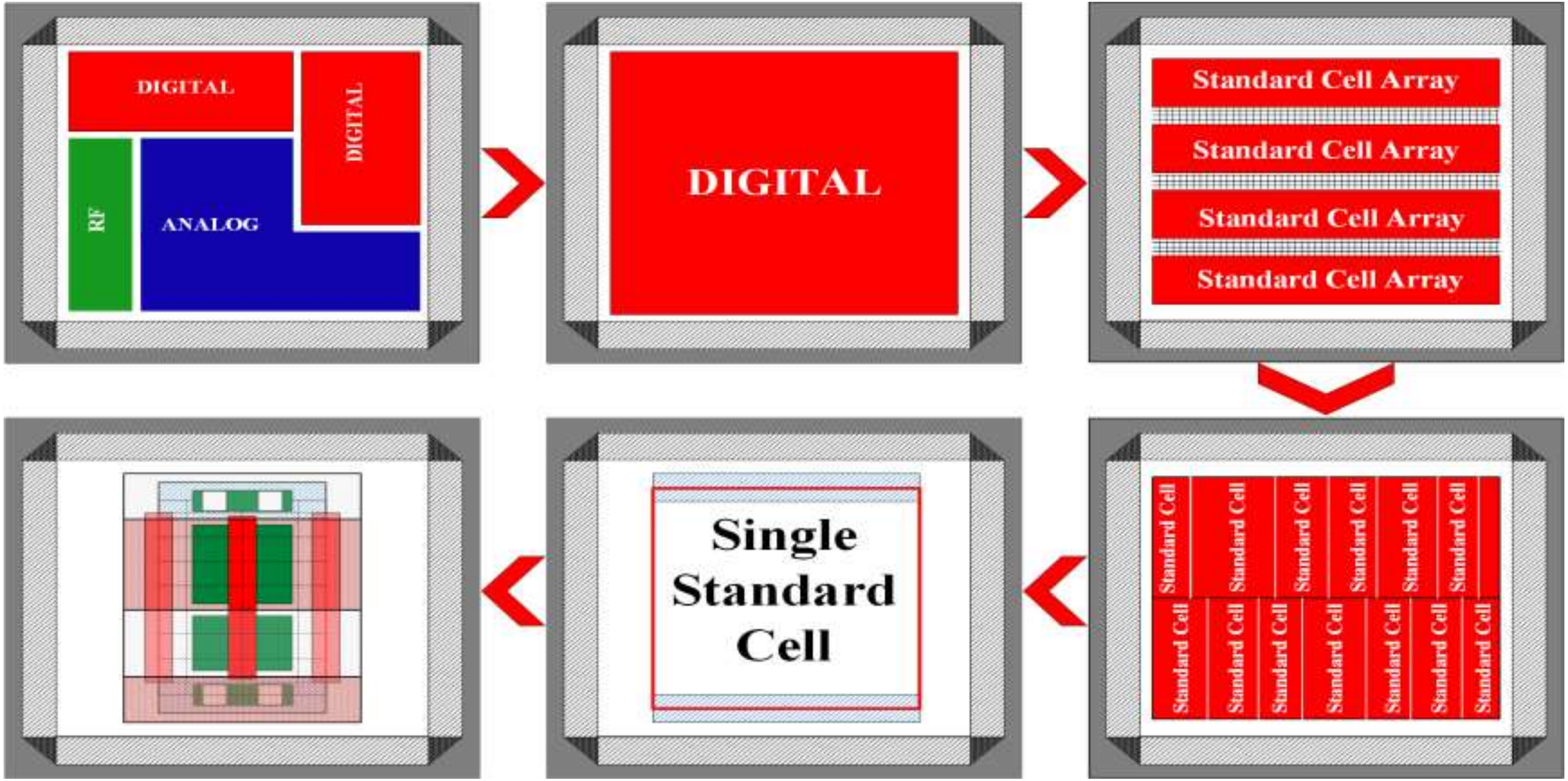
## Standard Cell Based Design

- Pre-designed cells in a library are used for chip Design
- Choosing of cell, placement and routing is done by the automated tool
- Same standard cells are used for any type of digital design
- Little scope on power/performance improvement
- Highly productive
- Developmental cost is low

## Full Custom Based Design

- Entire mask design is done without using any Library
- Geometry, Orientation and placement of every component is manual
- A simple changes in the spec forces the redesign of the layout.
- These is a scope of power/performance enhancement
- Very less productive
- Developmental cost is very high

# Standard Cells inside Chip



# Standard Cell Library

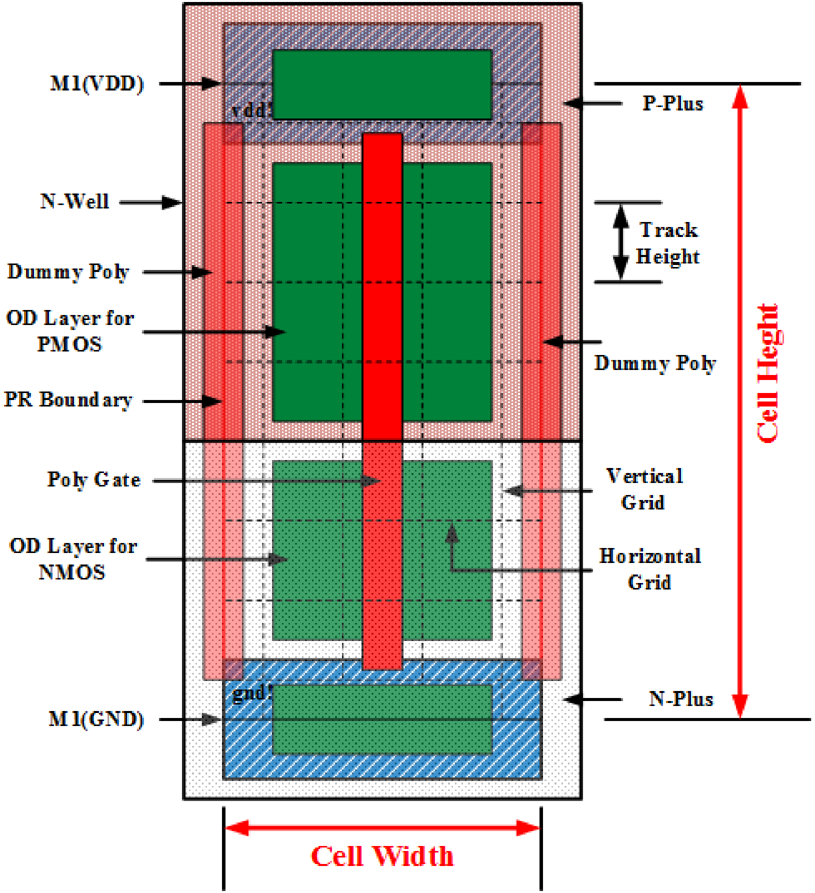
- A standard cell library is a collection of **well defined** and **appropriately characterized** logic gates that can be used to implement a digital design.
- A standard cell library is a collection of electronic logic functions such as AND, OR, INVERT, flip-flops, latches, and buffers. These cells are realized as **fixed-height, variable-width** and **full-custom** cells.
- A standard cell library contains two main components:
  - Library database (in **LEF** format or **Milky-way** format: abstract, layout, schematic, symbol and other logical and simulation views)
  - Timing information (in **Liberty** (.lib) format: function, timing, power and noise information)
- Additionally, a standard cell library also contain a full layout of the cell, SPICE model of the cell, Verilog or VHDL model, parasitic extraction model and DRC rule deck.

# Standard Cell Advantages

## Advantages:

- Save design time and money
- Well suited for automated design tools
- Less risky than full-custom design
- High Productivity
- More efficient Space
- Flexibility to perform implementation trade-off
  - Speed vs Power vs Area

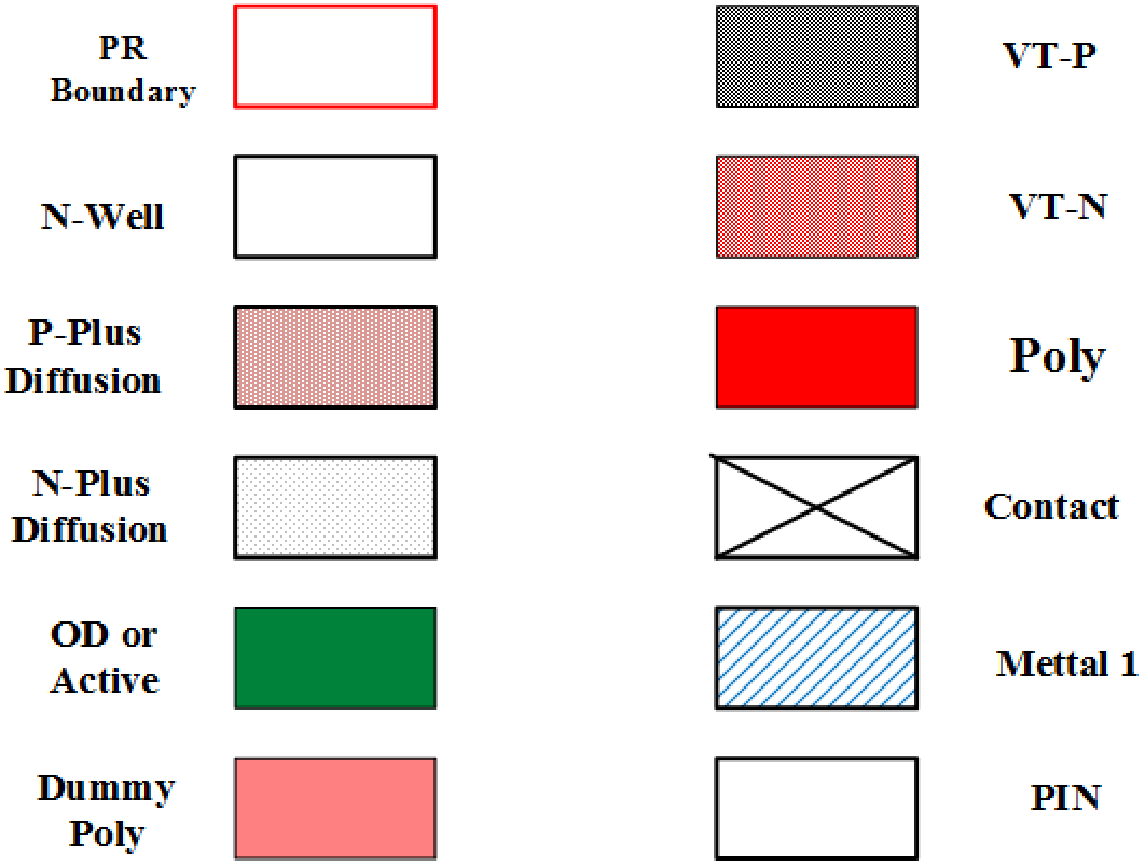
# Standard Cell Template



## STD Cell Template:

- ➢ Track
- ➢ Grid
- ➢ PR Boundary
- ➢ N-Well
- ➢ PP (P-Plus diffusion)
- ➢ NP (N-Plus diffusion)
- ➢ Vtp and Vtn
- ➢ Poly-Silicon Drawing
- ➢ Poly-Silicon Tile
- ➢ Metal-1 drawing
- ➢ Metal-1 Pin

# Standard Cell Layers



PR Boundary

N-Well

P-Plus Diffusion

N-Plus Diffusion

OD or Active

Dummy Poly

VT-P

VT-N

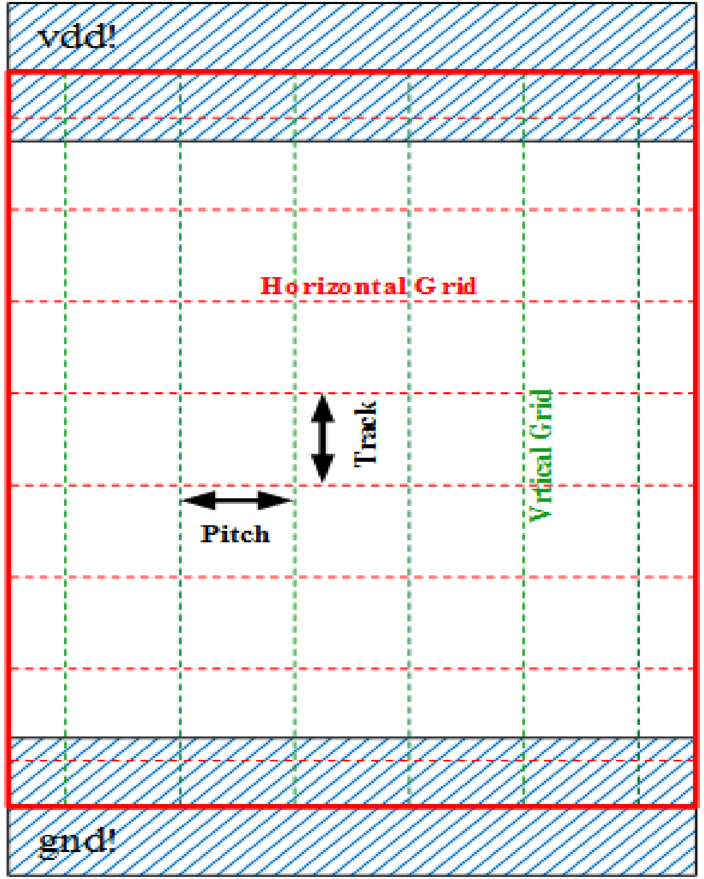
Poly

Contact

Mettal 1

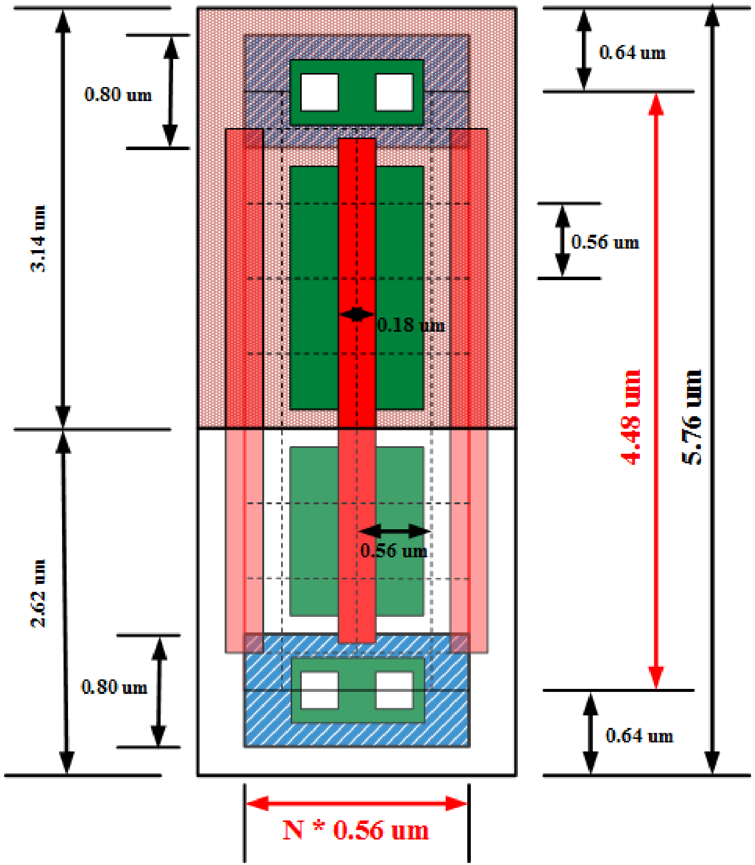
PIN

# Track and Grids



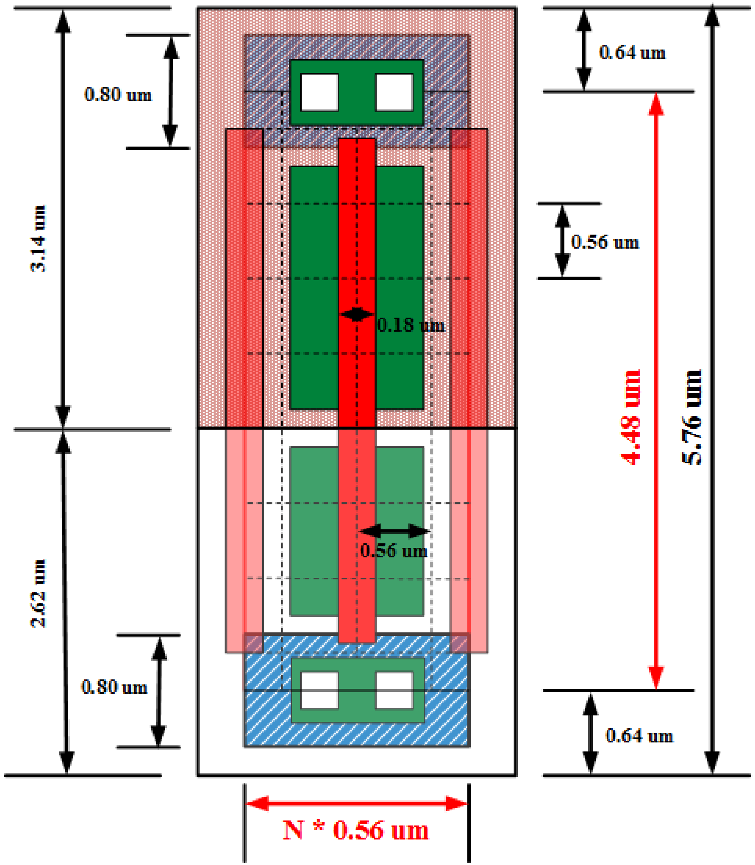
- ➢ This is a 8-track standard cell template
- ➢ The cross dashed lines are the grids
- ➢ Red dashed lines are horizontal grids
- ➢ Green dashed lines are vertical grids
- ➢ Distance between two horizontal grids are equal to one track
- ➢ The distance between two vertical grid is called one pitch
- ➢ The PRB height is nothing but the standard cell height
- ➢ Top metals are routed only on grids
- ➢ Pin access point given on grids interconnection point

# Standard Cell Dimensions: 180 nm node



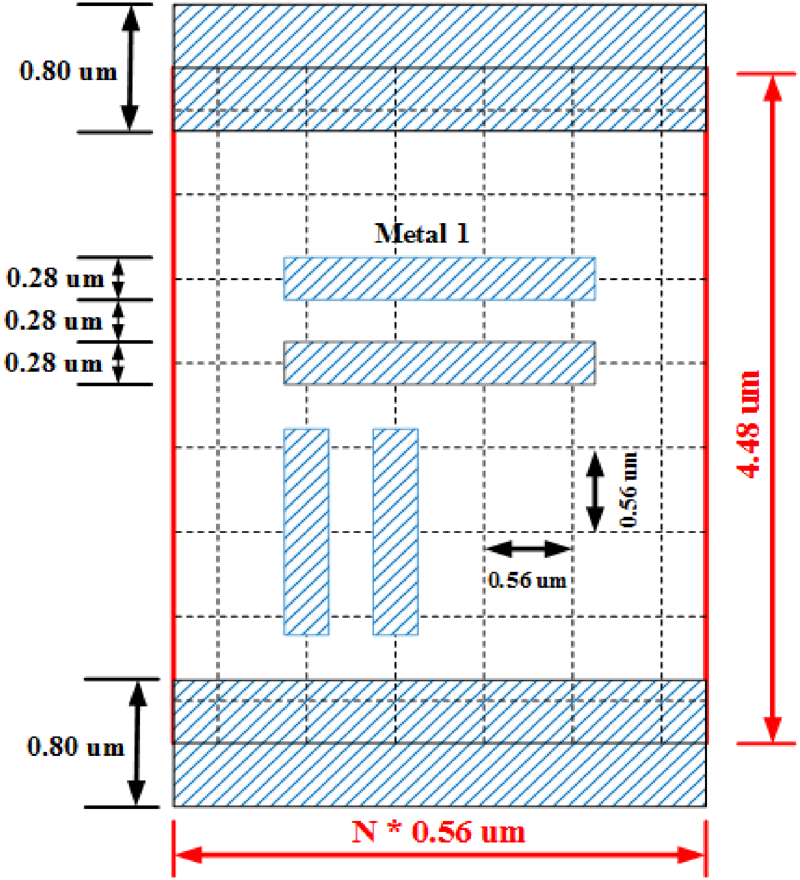
- No of Track: 8
- Track Height: 0.56 um
- Pitch Width: 0.56 um
- Metal-1 Height: 0.80 um
- Channel Length: 0.18 um
- N-Well Height: 3.14 um
- N-Well Ext. from PRB: 0.64 um (top)
- N-Well ext. from PRB: 0.43 um (both side)
- Cell Height: 4.84 um
- Template Height: 5.76 um
- Cell Width: N* 0.56 um
  - N= no. of pitch

# Standard Cell Performance: Based on Tracks



- Cell height measured in tracks
- A track height is one M1 pitch
- The more tracks, the wider the transistor , the faster the cells
- 7-8 low track libraries for area efficiency
- 11-12 tall track libraries for better performance
- 9-10 standard track libraries for a  reasonable area performance trade-off

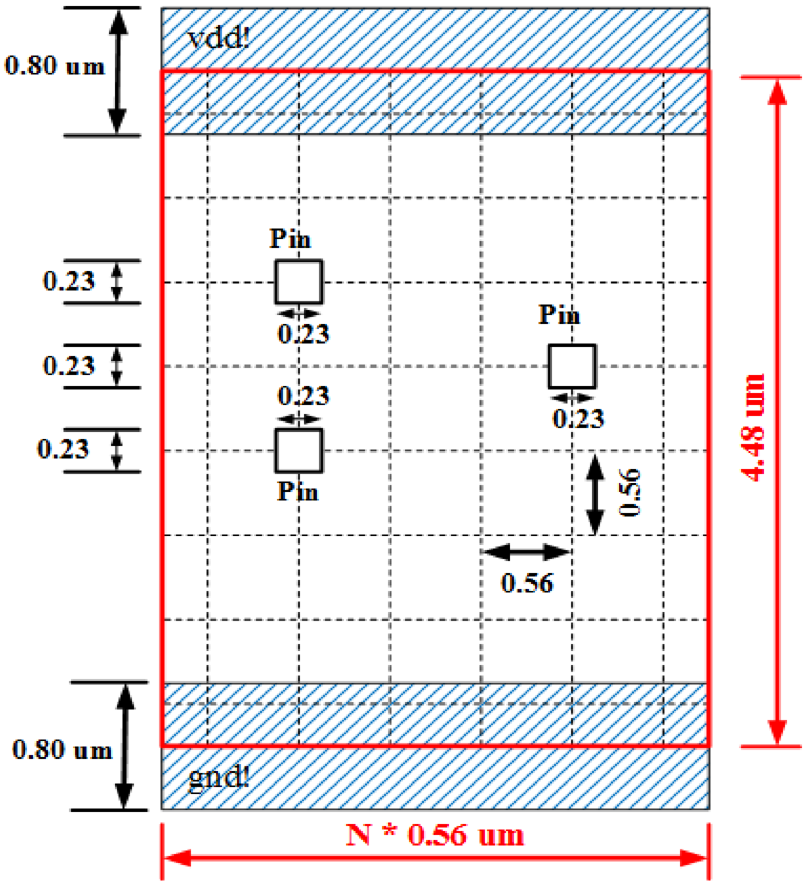
# Metal Width and Metal Spacing



- ➢ Minimum Metal width generally half of the track height (0.28 um) but it is not true for every technology node

- ➢ Minimum Metal spacing is generally half of the track height (0.28 um), but it is not mandatory.

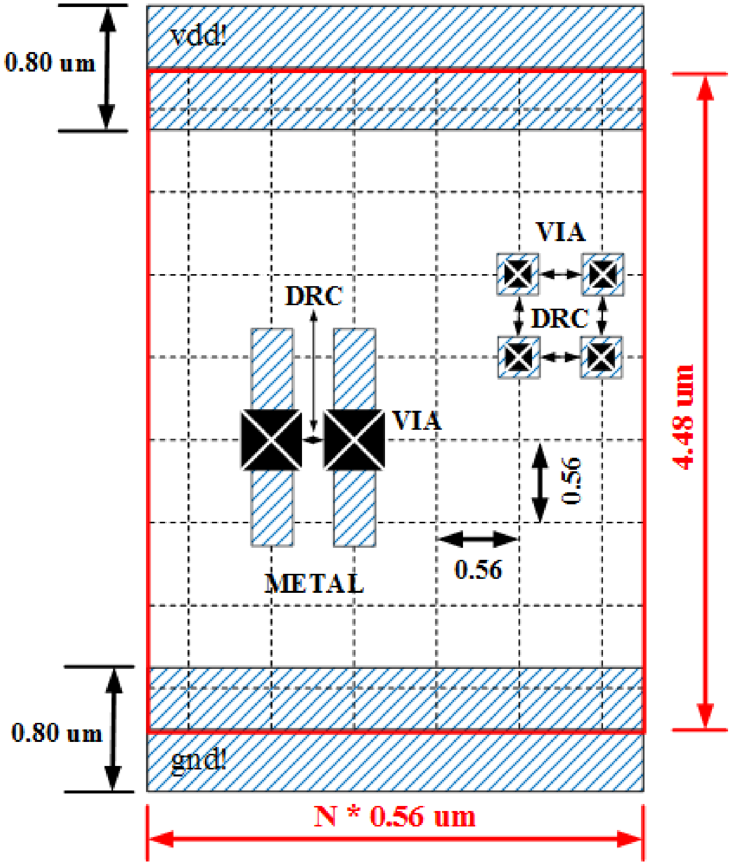
# Pin Position and Dimension



- ➢ Pin position always on the crossing points of grids

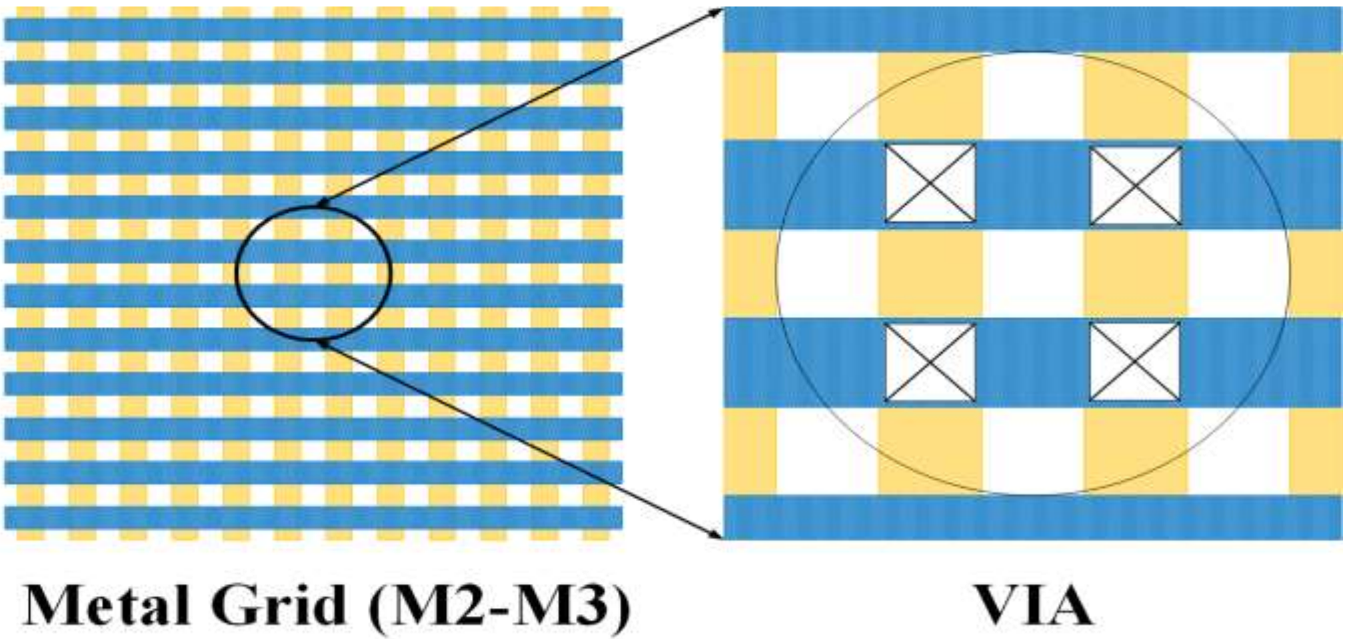
- ➢ Pin dimension depends upon the technology node, but it is always a square in shape

# Minimum Grid-to-Grid Calculation



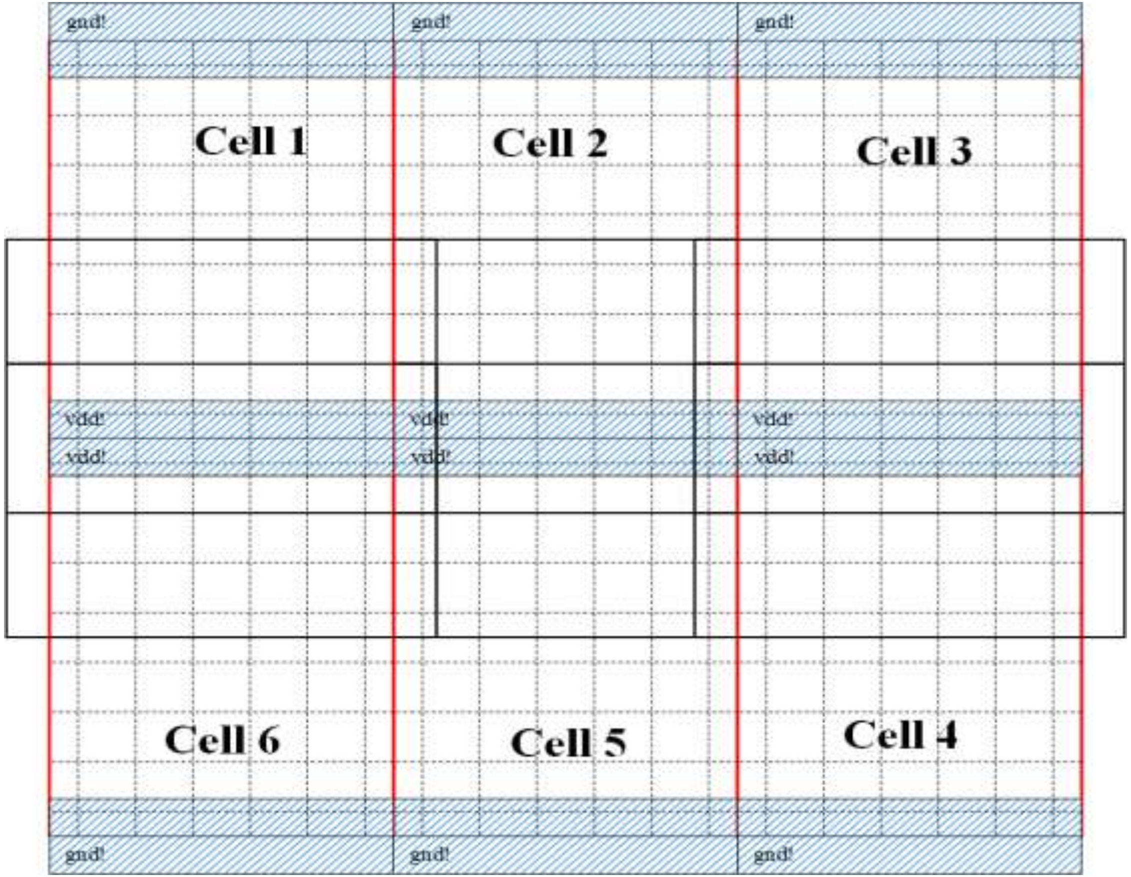
- ➢ Via position always on the crossing points of grids
- ➢ Via required minimum metal extension
- ➢ Minimum grid size depends on the minimum spacing between two vias at which no DRC violation occurs (via dimension > minimum metal width)
- ➢ Depends upon the minimum spacing between two metals (Via dimension < minimum metal width)

# Higher Metal Grid and H-V Routing



- Even metal in vertical direction and Odd metal in horizontal direction
- Yellow: Metal-2, Blue: Metal-3
- Via placement only over grid interconnections

# Standard Cell Abutment



- DRC violation should not come during cell abutment
- Cell abutment can be done horizontally or vertically or both
- Horizontal abutment touches PRB of two adjacent cells
- Vertical abutment merges either supply rail or ground rail of two adjacent cells
- During abutment N-well will overlap between two cells

# Frequently Used Design Rules

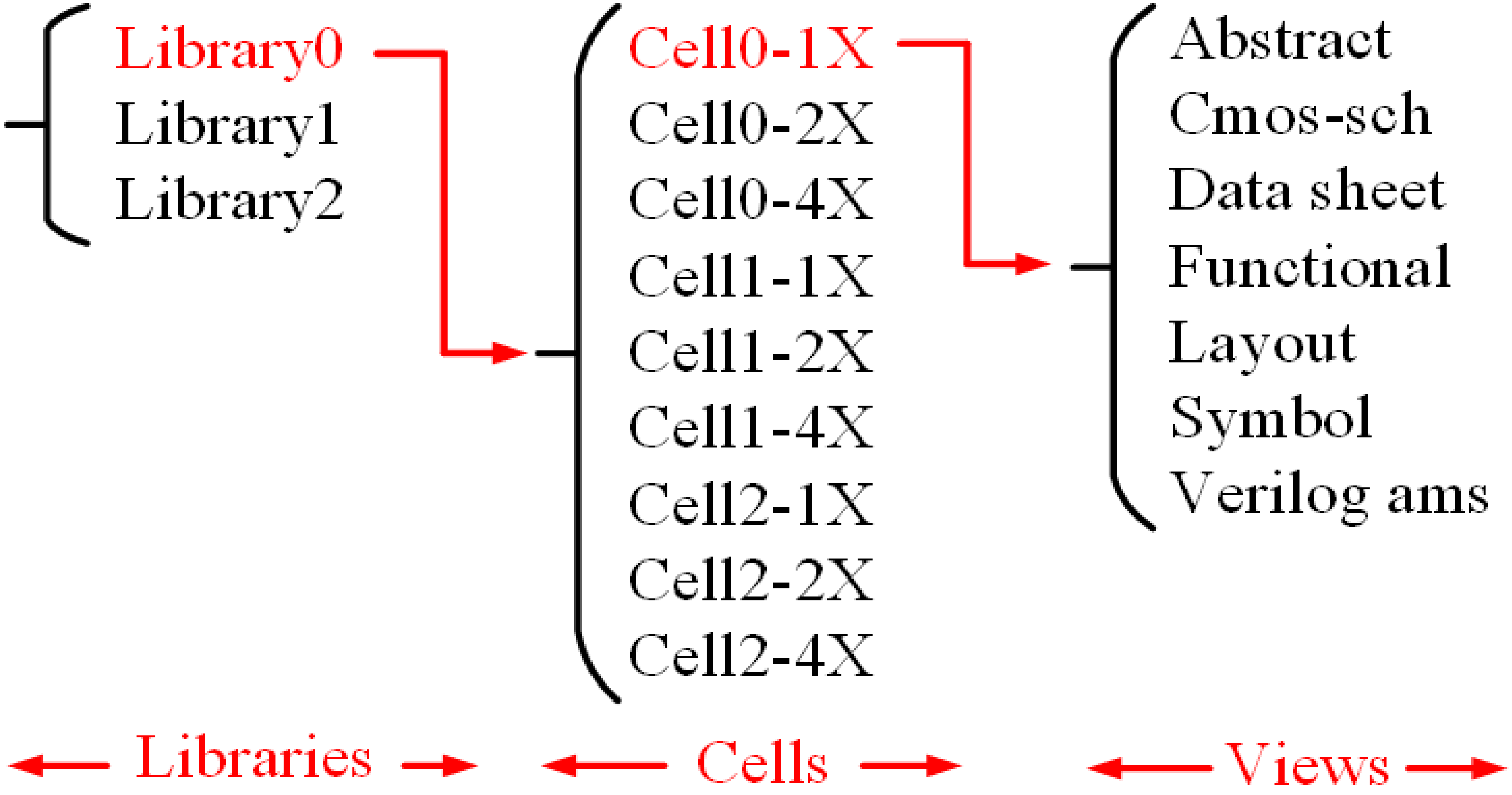
- Contact enclosure rules:
  - With metal
  - With poly
  - With OD
- Pin enclosure rules:
  - With metal
  - With poly
  - With OD
- Spacing Rules:
  - Metal-to-metal
  - Poly-to-poly
  - OD-to-OD
  - Contact-to-contact
  - Poly-to-OD
  - OD-to-NW

- Extension Rules:
  - Poly on OD
- Abutment (Half-DRC) Rules:
  - PRB-to-Metal
  - PRB-to-Poly
  - PRB-to-OD
  - PRB-to-Contact

Layout Constraints:

- Standard Cell Height
- Fixed Poly-to-poly pitch
- Limited to Metal 1
- Two access point

# Standard Cell Library Database



Library0
Library1
Library2

Cell0-1X
Cell0-2X
Cell0-4X
Cell1-1X
Cell1-2X
Cell1-4X
Cell2-1X
Cell2-2X
Cell2-4X

Abstract
Cmos-sch
Data sheet
Functional
Layout
Symbol
Verilog ams

Libraries

Cells

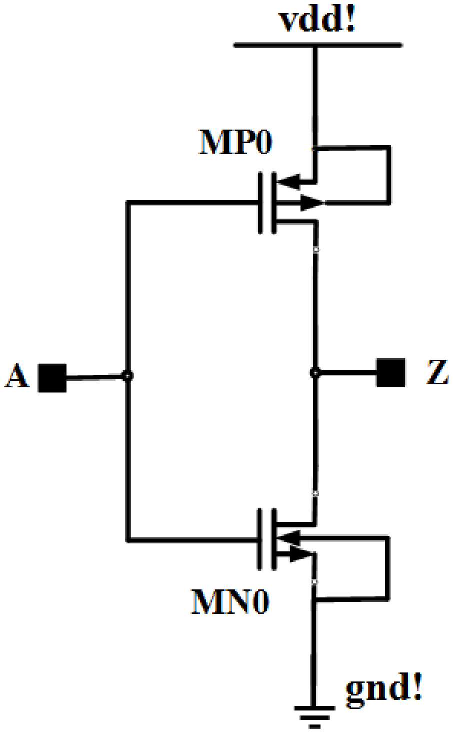
Views

# Library and Cell Types

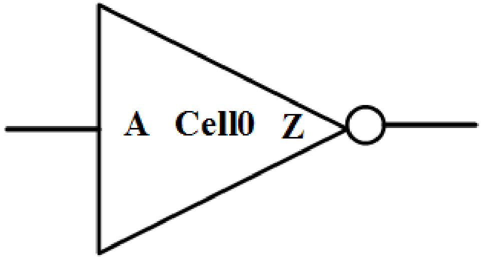
- **Libraries:**
  - HD – High Density
  - LL – Low Leakage
  - HDLL – High Density Low Leakage
  - HDMT – High Density Multi Threshold
  - HDMV – High Density Multi Threshold
  - JI – Junction Insulated
  - JIHD – Junction Insulated High Density
  - JIHDMT – Junction Insulated High Density Multi Threshold
- **Cells:**
  - Drive Strength (1X, 2X, 4X, 8X …..)
  - Threshold Voltage (LVT, SVT, HVT, ULVT, UHVT)
  - Gate length (Standard and +10%) (For Ex. 40 nm, 44 nm)

# Cell View

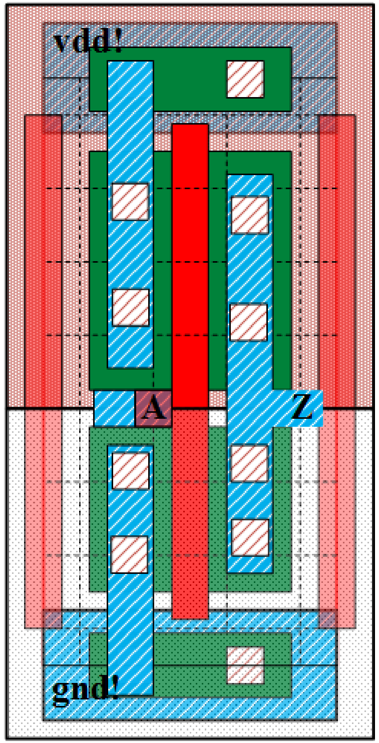
## Schematic



## Symbol



## Layout



# Good Layout Practice-1

- Avoid more poly routing until and unless it is required
- Avoid unnecessary poly end cap
- Avoid small U shape in metal routing
- Avoid unnecessary notches in OD
- Avoid small JOGs in metal, poly and OD
- Avoid small JOGs in NWELL, PP, NP, VTLP and VTLN Layers
- Avoid stare-case structure in OD until and unless it is required
- Avoid stare-case routing of Poly and Metal
- Avoid metal and poly bending in the routing
- Avoid poly feed-through
- Avoid unnecessary metal extension near the left side and right side of the PR boundary

# Good Layout Practice-2

- Try always to route all the pin connected metals on the grid
- Put appropriate amount of  contacts in metal-to-OD and metal-to-poly.
- Put wider metal in bending lines
- Put appropriate no. of contacts in metal-to-OD and metal-to-contact
- Output path should be little wide than other routings
- Contact-to-contact spacing should not be very close very far. Contacts should be appropriately spread within the available area
- Give sufficient enclosure to all the contacts

# Good Layout Practice-3

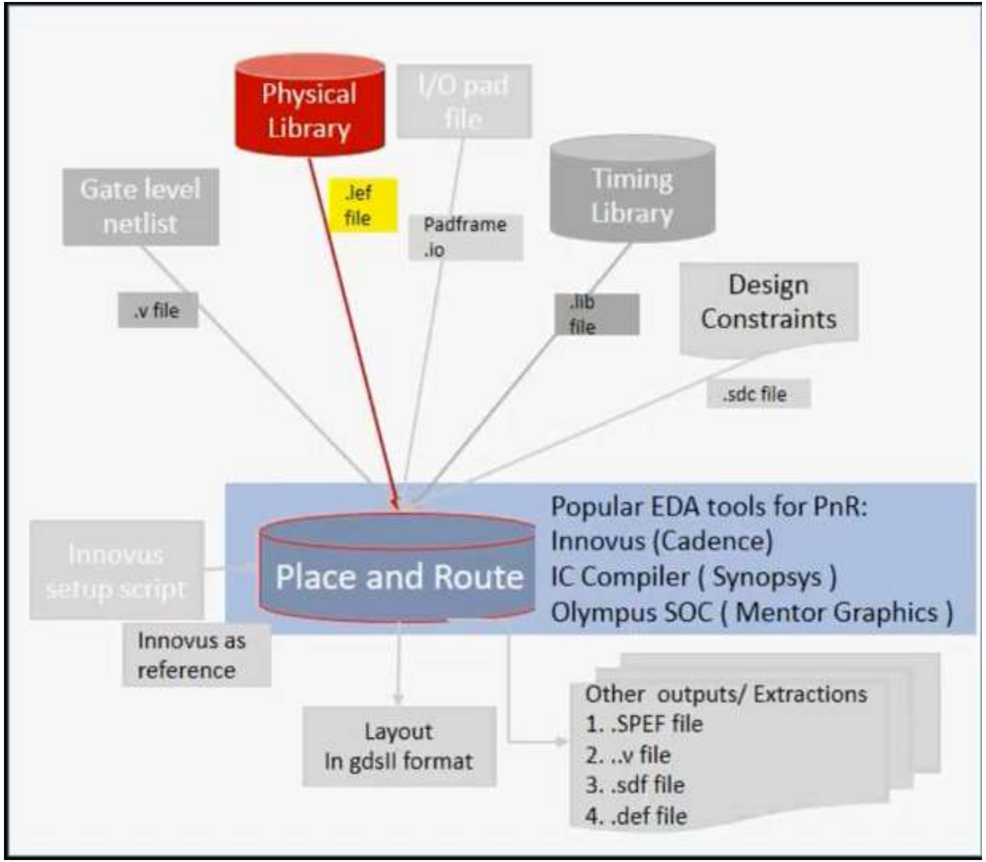
- Use staggered contacts
- Leave Metal1 routing horizontal grids for direct M1 access
- Prefer to move pins towards boundary
- Take advantages by pulling vdd/gnd using RX notches for improving
- More coverage of PC when very long for large number of fingers
- Cut any dummy poly from main gate if possible
- Fat metal in Vdd/Gnd will create DRC on abutment. Break the Vdd/Gnd in two small combs.
- Remove unnecessary Loop, U-shape and L-shape in metals
- Try to give as much as access points to the pins
- Try to give both horizontal and vertical access points
- Use Euler’s path theory for simplifying layout design

# Different files needed in Physical Design

- .v file
- .vhd file
- .lib file
- .db file
- .lef file
- .tf file
- .mw file
- .def file
- .sdc file
- .tlu file
- .saif file
- .spef file
- .sbpf file
- .sdf file
- .map file
- .itf file
- .io file
- .tcl file
- .rspf file
- .simv file
- .gds file

# LEF File

- ➢ LEF stands for **Library Exchange Format** file
- ➢ LEF file is a readable ASSCI format file
- ➢ LEF basically divided into parts;
  - Technology file
  - Cell file
- ➢ Technology LEF contains the information of available metal layers, via information, design rules.
- ➢ Cell LFE contains the information related to geometry of each cell's in abstract view



# LEF File

Technology LEF

- Technology LEF contains:
  - LEF Versions
  - Units: time, resistance, capacitance etc…
  - Manufacturing grid
  - Design rules and other details for each BEOL layers

- Layer name: poly, contact, metal, via1 etc
- Type: Master slice, routing, cut etc
- Direction: Vertical or Horizontal
- Pitch
- Width
- Spacing
- Resistance per sq. unit

# LEF File

Cell LEF

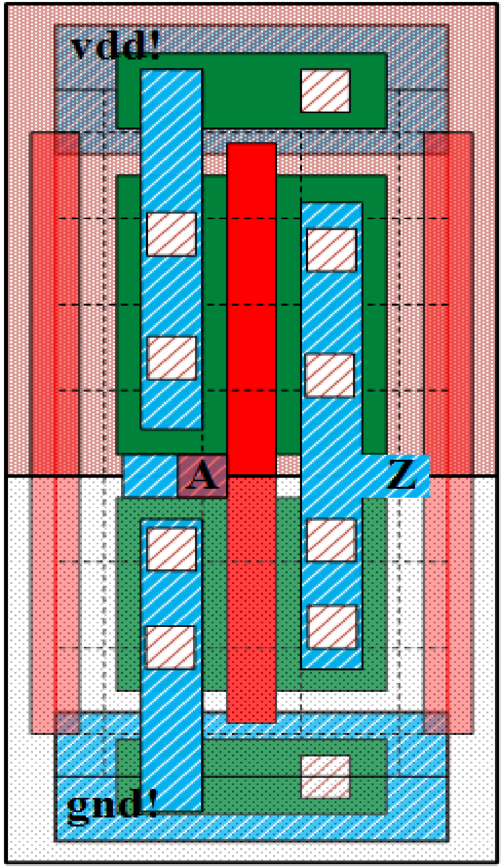
- Cell LEF contains:
  - Cell name: inv1x, nand21x, buf1x, aoi211x
  - Class: Core or Pad
  - Origin: 0 0
  - Size: width by height of cell
  - Symmetry: X, Y, XY
  - Site: Core Site or Pad

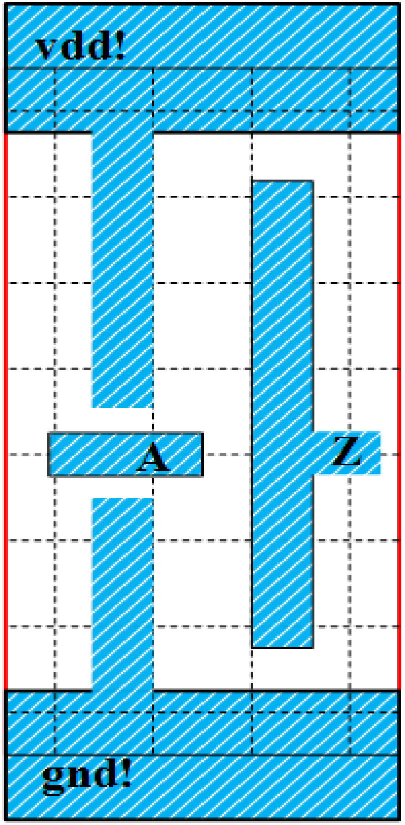
- Details of each pin
  - Pin name: A, B, C, Z
  - Direction: input, output, inout
  - Use: Signal, Clock, power, ground
  - Shape: Abutment in case of power and ground
  - Layer: Metal1 , Metal2
  - Rectangle coordinates: llX, llY, urX, urY

# LEF File

Abstract description of the layout for of PnR

- Readable ASSCI format
- Contains detailed pin information for connection
- Does not include front-end of the line layers poly, diffusion
- Contains the blockages of DRC
- LEF is an important file which is required at the time of design import in PnR tool
- LEF is also called physical library as it contains layout information of a cell in abstract view
- LEF file comes with standard cell library. But in case you want to do PnR of your own costumed designed cell, you would required to generate its lib file, LEF file, verilog file and gds file

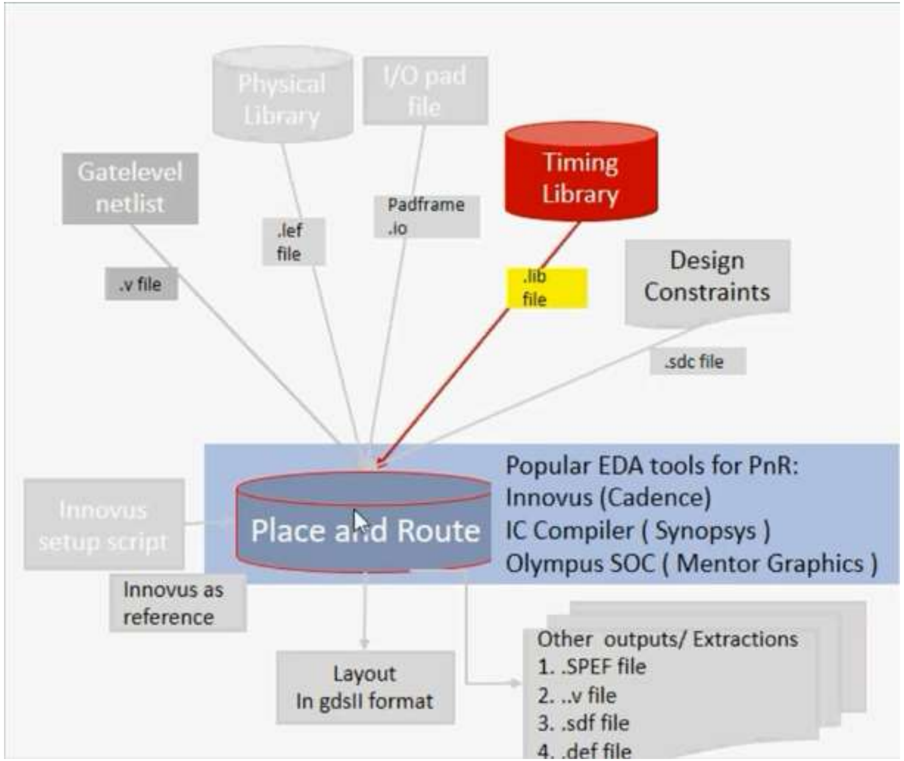




# Liberty File (.lib)

### .lib File

- .lib file stands for Liberty Timing File
- .lib file is an ASCII representation of timing and power parameters associated with any cells in a particular technology node
- This is basically a timing model file which contains cell delay, cell transition, setup and hold time requirements foe a cell
- .lib file contains timing and electrical characteristics of gate and macro library
- These file are provided by your gate library vendor or the foundry if they supply gate library



# Liberty File (.lib)

**.lib** File basically contains following information's

- General information common for all cells
  - Library name and technology
  - Units (time, power, voltage, current, resistance and capacitance
  - Value of process, voltage and temperature (Max, min, typical)
- Cell specific information
  - Cell name
  - Global pin
  - Leakage power
  - Area
- Pin specific information
  - Pin mane
  - Pin direction
  - Power
  - Capacitance
  - Fan-out load
  - Rise capacitance
  - Fall capacitance
  - Function

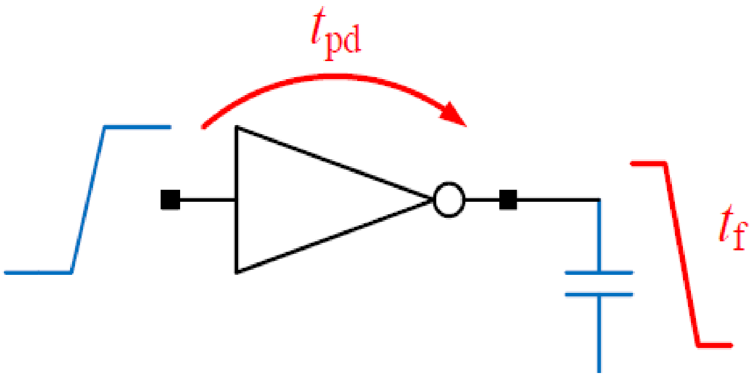
# Characterization of Cell

- Timing and power parameters of a cell is obtained by simulating the cell in variety of conditions and data is represented in **.lib file**
- There are two techniques to characterize a cell and generate **.lib file**
  - Composite current source (CCS)
  - Non linear delay model (NLDM)
- In CCS technique, current source is used whereas in NLDM technique voltage source is used to model and derive the **.lib file**
- CCS technique has more controlling parameters than NLDM, so **.lib file** generated using CCS is more accurate
- Run time of CCS .lib file is more than the NLDM .lib file
- File size of CCS .lib file is also larger than NLDM .lib file
- There is a cadence tool called, **liberate** which is used to generate .lib file for custom cells

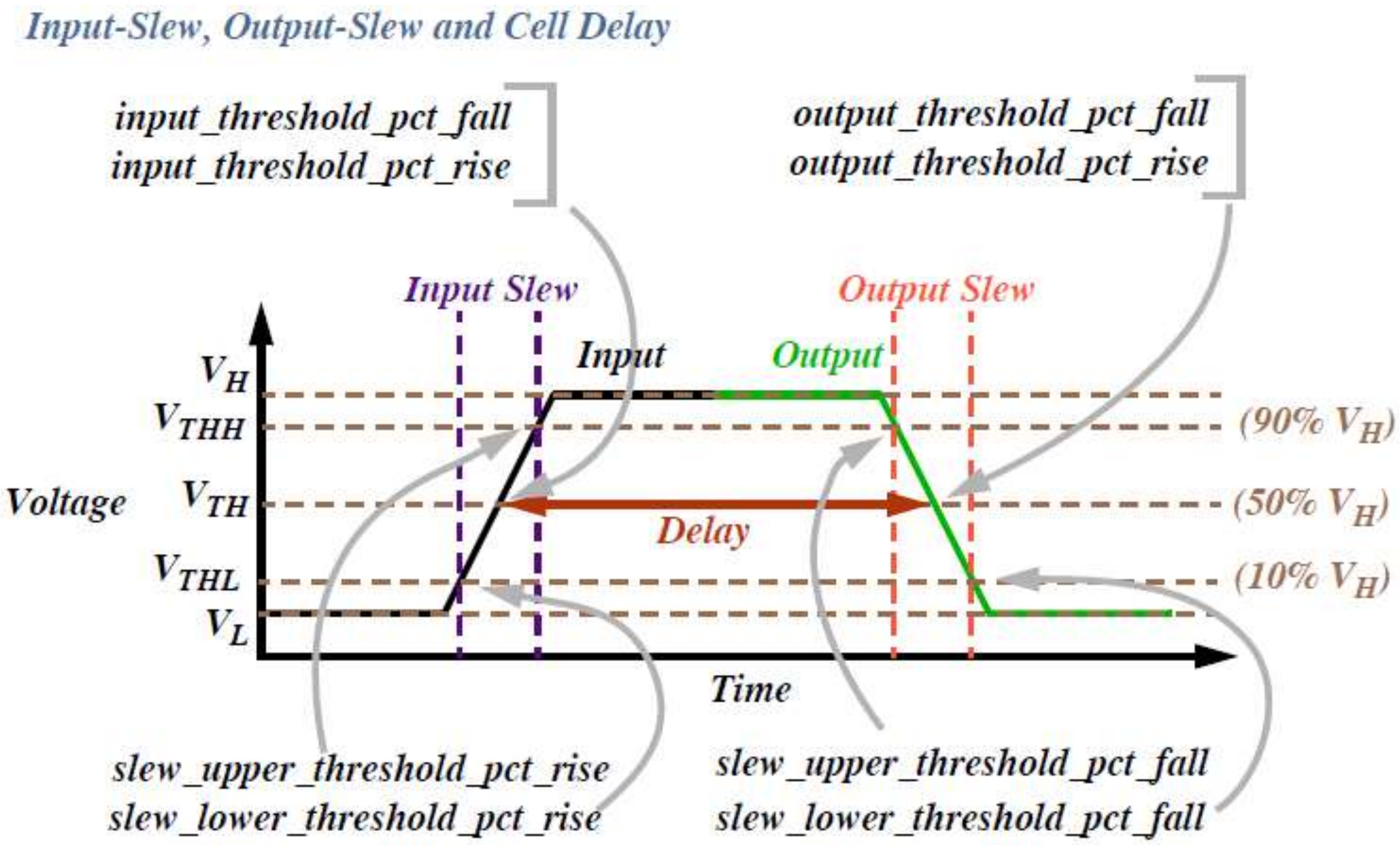
# Characterization of Cell

- How do we know the delay through a gate in a logic path
  - Running SPICE is too much complex
  - Instead, create a timing model that will simplify the calculation

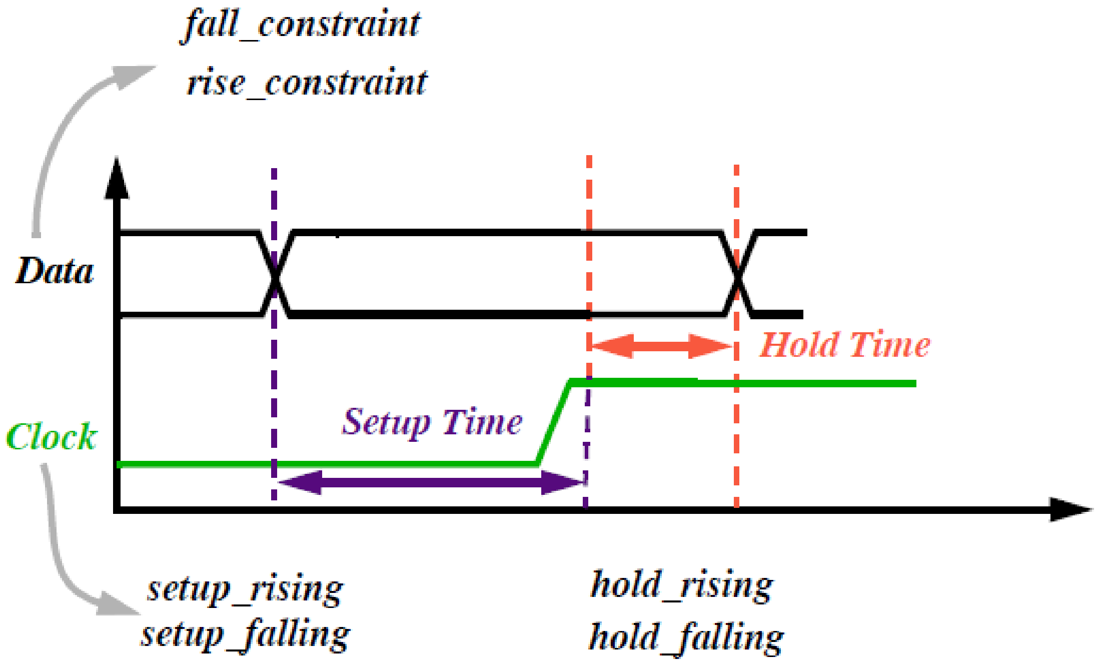
- For every timing arc calculate
  - Propagation delay
  - Output transition (t-rise, t-fall)
- Based on
  - Input net transition
  - Output load capacitance



# Timing Check: Delay

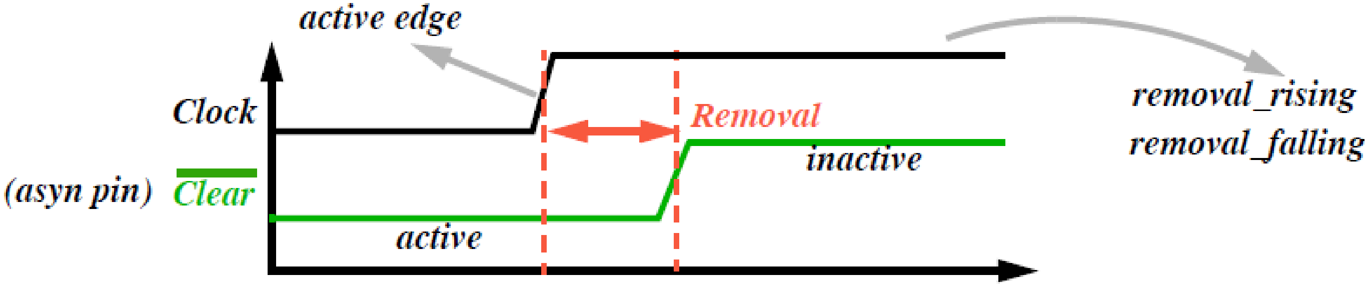

Input-Slew, Output-Slew and Cell Delay
input_threshold_pct_fall
input_threshold_pct_rise
output_threshold_pct_fall
output_threshold_pct_rise
Input Slew
Output Slew
Input
Output
$V_H$
$V_{THH}$
(90% $V_H$)
Voltage
$V_{TH}$
(50% $V_H$)
Delay
$V_{THL}$
(10% $V_H$)
$V_L$
Time
slew_upper_threshold_pct_rise
slew_lower_threshold_pct_rise
slew_upper_threshold_pct_fall
slew_lower_threshold_pct_fall

# Timing: Setup and Hold

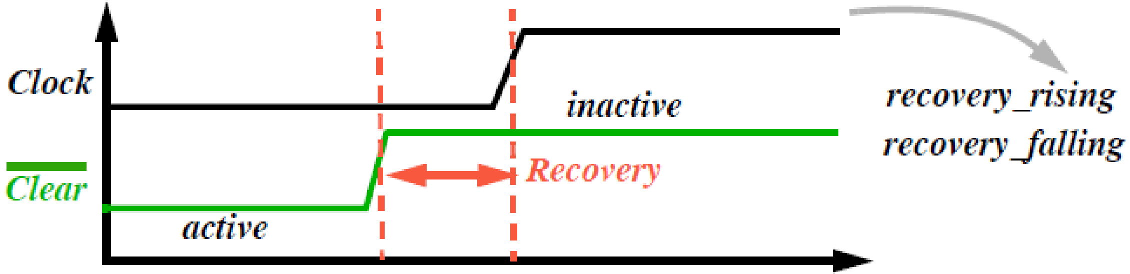


# Timing: Removal and Recovery

Removal:



Recovery



Thank you …