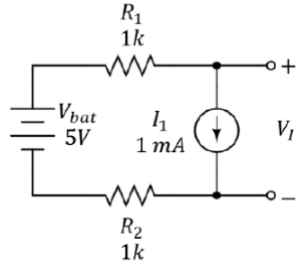
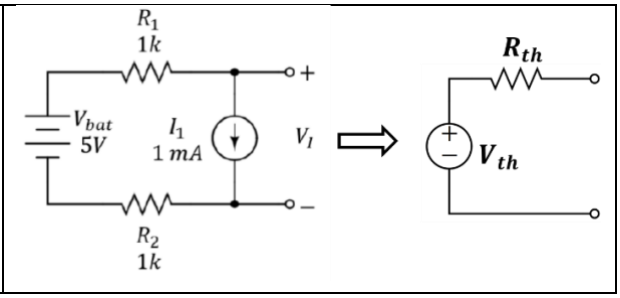
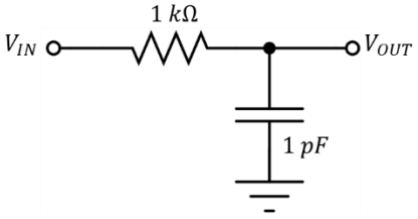
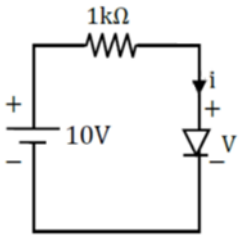
Question-1 The voltage across current source I_1 (V_I) is:	

Question-2 The Thevenin equivalent (V_{th}, R_{th}) of the network:	

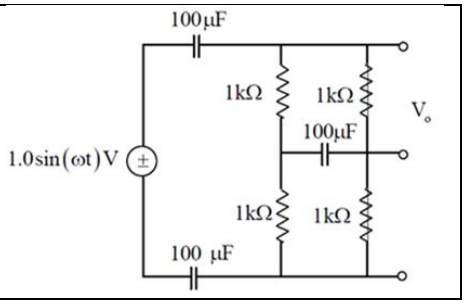
Question-3 Two capacitors of value C and 2C, are charged to 1V and 2V respectively and then connected in parallel with same polarity. The voltage across the parallel capacitors is:	

Question-4 $1\mu s$ after a step input of $1V$, the output voltage V_{OUT} is (1/e=0.368):	

Question-5
Forward bias voltage of the diode is 0.7V. The current in the circuit is:

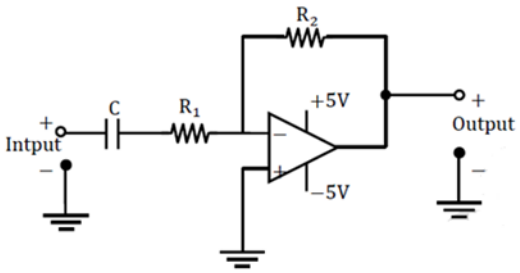


Question-6
At very high frequencies the peak output voltage V_0:

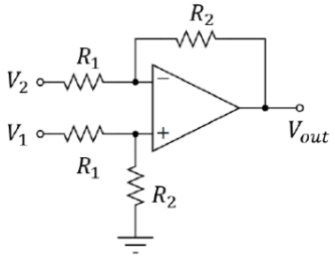


Question-7
The circuit shown is a filter of type:

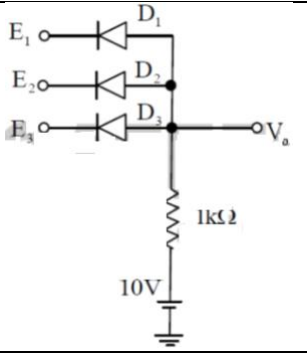
_____ with $f_{3dB} =$ rad/sec



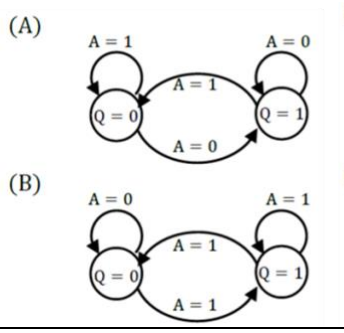
Question-8
Using principle of superposition, the expression for V_{out} is:

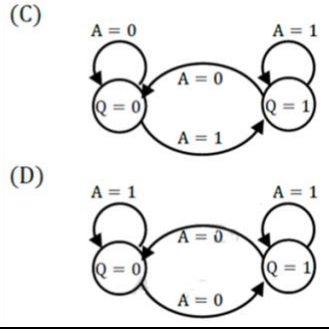


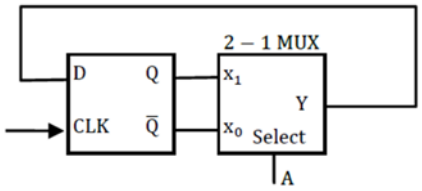
Question-9
In the circuit shown, D1, D2, D3 are identical, and inputs E1, E2 and E3 are '0' V for logic '0' and '10' V for logic '1'what logic gate does the circuit represents:



Question-10
The state-diagram shown for the logic circuit is:



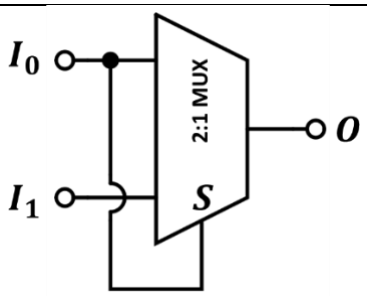




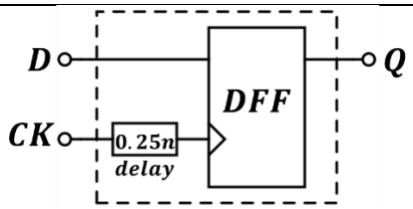
Question-11
The state-diagram in Question-10 is a:

(a) Moore Machine
(b) Mealy Machine
(c) Moore-Mealy Machine
(d) None of the above

Question-12
A 2:1 MUX is connected as shown in figure. The resultant logic gate is a:

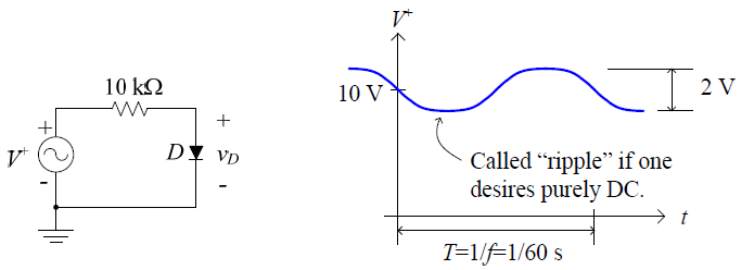


Question-13
A D-FlipFlop (DFF) has an inherent setup time of 0.5ns and when a delay on 0.25ns is added in the clock path, the resultant setup time is:



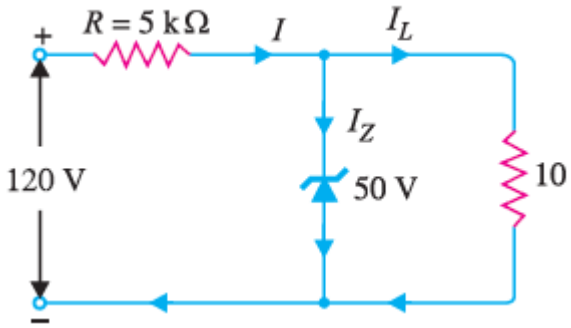
Question-14

For the circuit shown, find out $v_{D,}$ when V^{+}=10+1*cos (2*pi*60*t) V



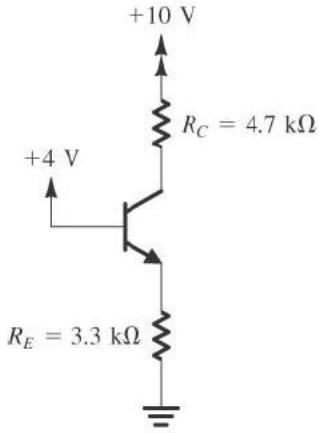
Question-15

For the circuit shown in the figure find out the output voltage, voltage across the resistor R and current through the zener diode.



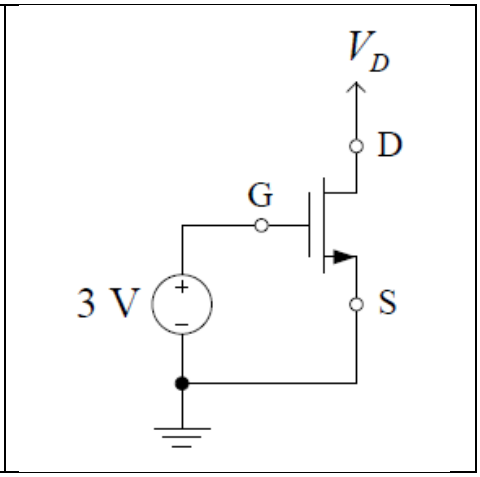
Question-16

Calculate the node voltages and currents in the circuit assuming β=100.



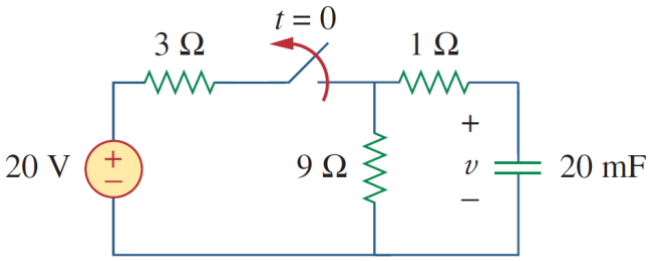
Question-17

For the circuit in the enhancement type NMOS threshold voltage V_T=2V, find the region of operation for V_D of 0.5V, 1V and 5V.



Question-18

The switch in the circuit has been closed for a long time and it is opened at t=0. Find v(t) for t>=0



Question-19

What is the logic function implemented by the CMOS transistor network.