KEI PALABASAN

Digital Design Engineer

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ABOUT ME

Digital designer in Verilog with Linux driver experience and educational background in MEMS design and fabrication.

EXPERIENCE

May 2022 - now **Smartfox Data Solutions, Inc.**
Hardware Engineer; Full-time Remote
- Underwent training in digital design and verification with Verilog and UVM, contributing to internal AXI-related IP.
- Designed and tested FPGA-based chip testing equipment for various applications.
- Adopted Agile methodologies and Gitflow, improving communication within the team and to product owners and stakeholders.
- Developed Linux drivers for custom graphics hardware, enabling rendering and high-level testing of hardware designs on Xilinx FPGAs using industry-compatible APIs and benchmarks.

ORGANIZATIONS

Oct 2021 - Oct 2022 **UP Competitive Robotics Club**
Chief Executive Officer
Led the organization's post-pandemic transition from online to physical activities.
- Managed UFM booth, driving a significant increase in recruitment, showing importance of F2F activities and interactive demos.
- Handled first F2F robotics workshops, improving applicant and member retention.
- Implemented necessary constitutional amendments and managed leadership elections to ensure organizational sustainability.

SKILLS

Teamwork/Communication: Scrum, Agile, Team Management, LaTeX, Markdown
Languages: C/C++, Verilog, SystemVerilog/UVM, GLSL, Python
OS/Applications: Linux (systemd), Tensorflow, Vulkan, LTSpice, JAMStack

EDUCATION

Aug 2019 - Aug 2023 **BS Electronics Engineering**
University of the Philippines Diliman - Quezon City, NCR
Graduated *summa cum laude* (1.12 GWA, equiv. 3.8 GPA)
Affiliated with UP Microlab for capstone project.

PUBLICATIONS

2023 **FPGA-targeted optimization approaches for SVM and CNN human activity recognition models using the HARTH and HAR70+ datasetss**
Palabasan, K.R., Rajagopalan, R.S., Manzano, J.M., Rosales, M.D., De Leon, M.T., Hizon, J.R.E.
Conference paper for PrimeASIA 2023.
doi:10.1109/PRIMEAsia60757.2023.00009

2023 **Comparison of hardware-optimized CNN and SVM models for human activity recognition using the HARTH and HAR 70 + datasets**
Palabasan, K.R., Rajagopalan, R.S., Manzano, J.M., Rosales, M.D., De Leon, M.T., Hizon, J.R.E.
Submitted as Undergraduate Project. Conference paper for ISOCC 2023. Furiosa AI Award.
doi:10.1109/isocc59558.2023.10396338

LANGUAGES

English - native
Filipino - proficient
Japanese - proficient

INTERESTS

Music - JPop/Vocaloid/Alt (Yorushika, Nakiso, Kanaria); Singing, Guitar.
Subculture - Anime/Manga, Cosplay, VTubers.
Tech - Custom Keyboards, AI model training/tweaking, Amateur Radio.
Games - ARMA 3, Minecraft, GMod