Principled foundations for microarchitectural security

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IMDEA Software Institute

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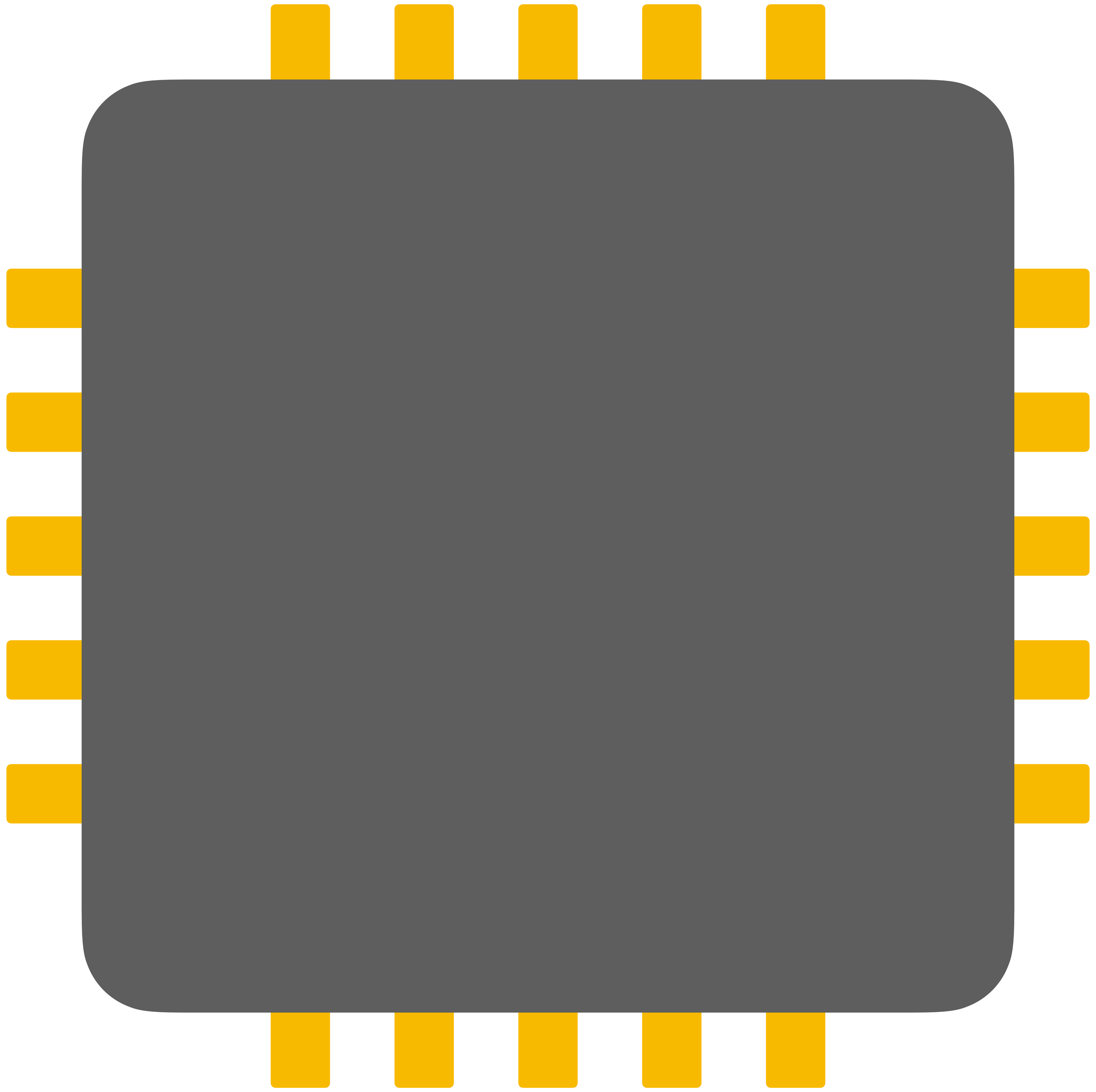
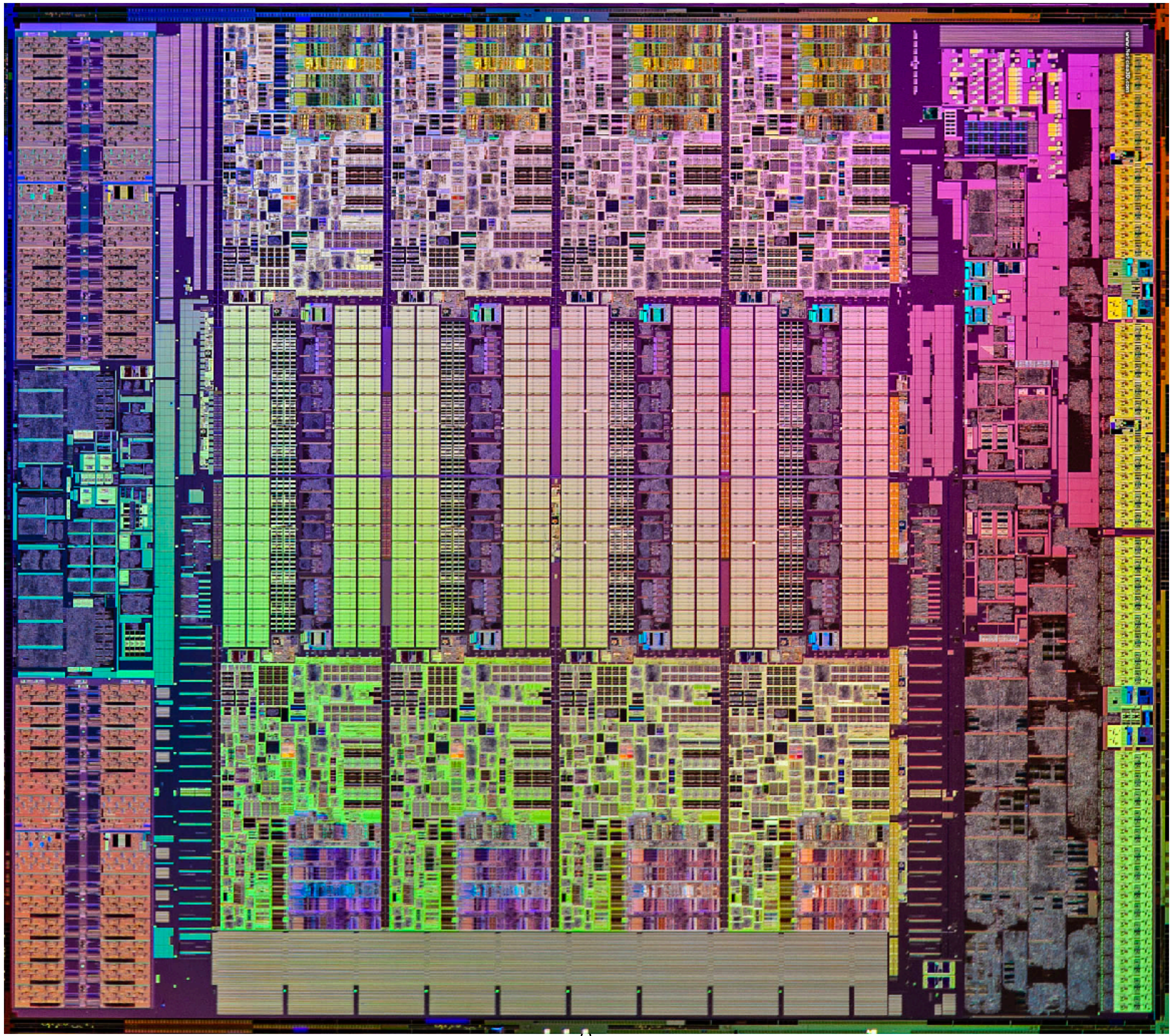
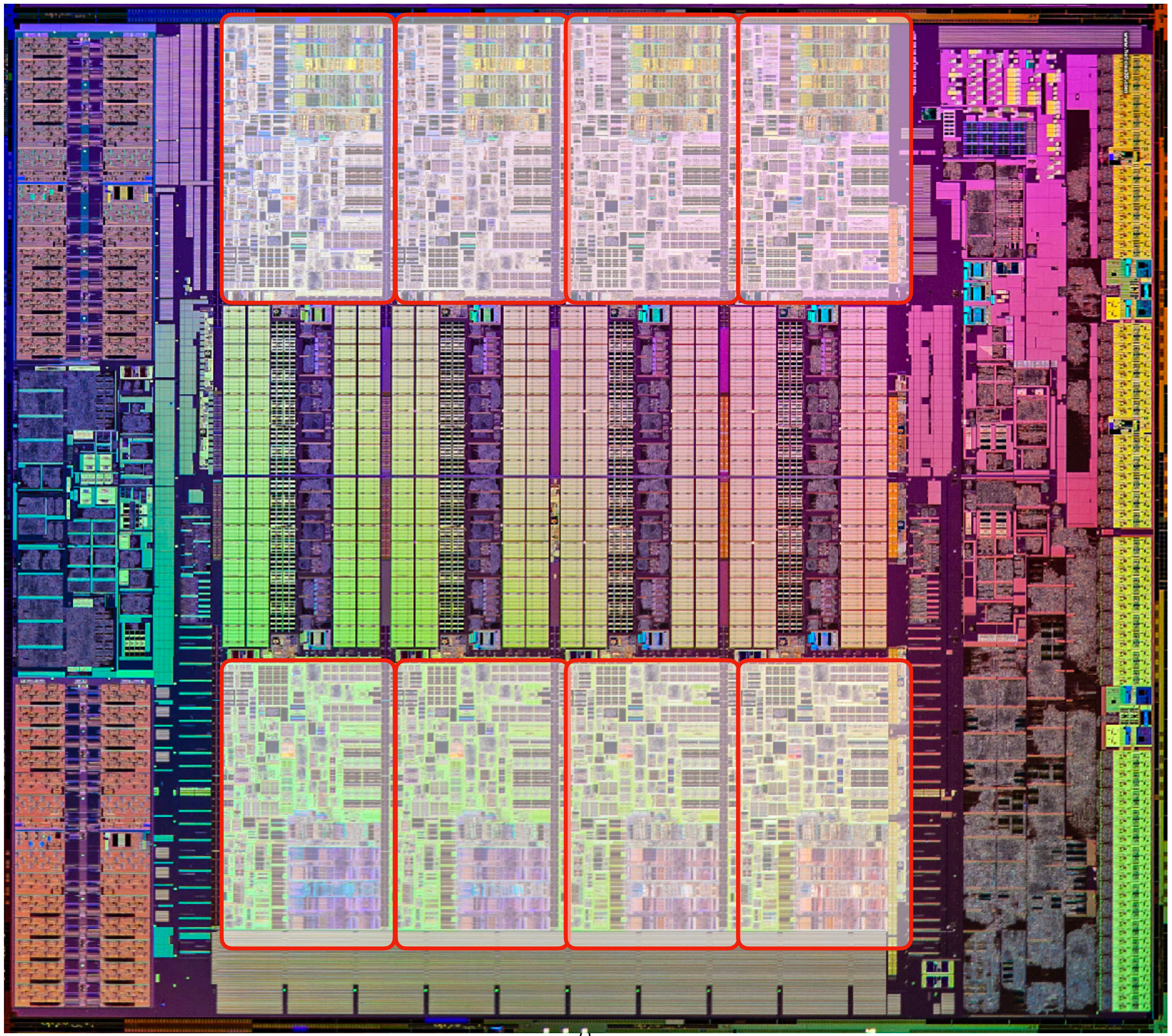




Picture of Intel “Haswell-E” Eight Core CPU



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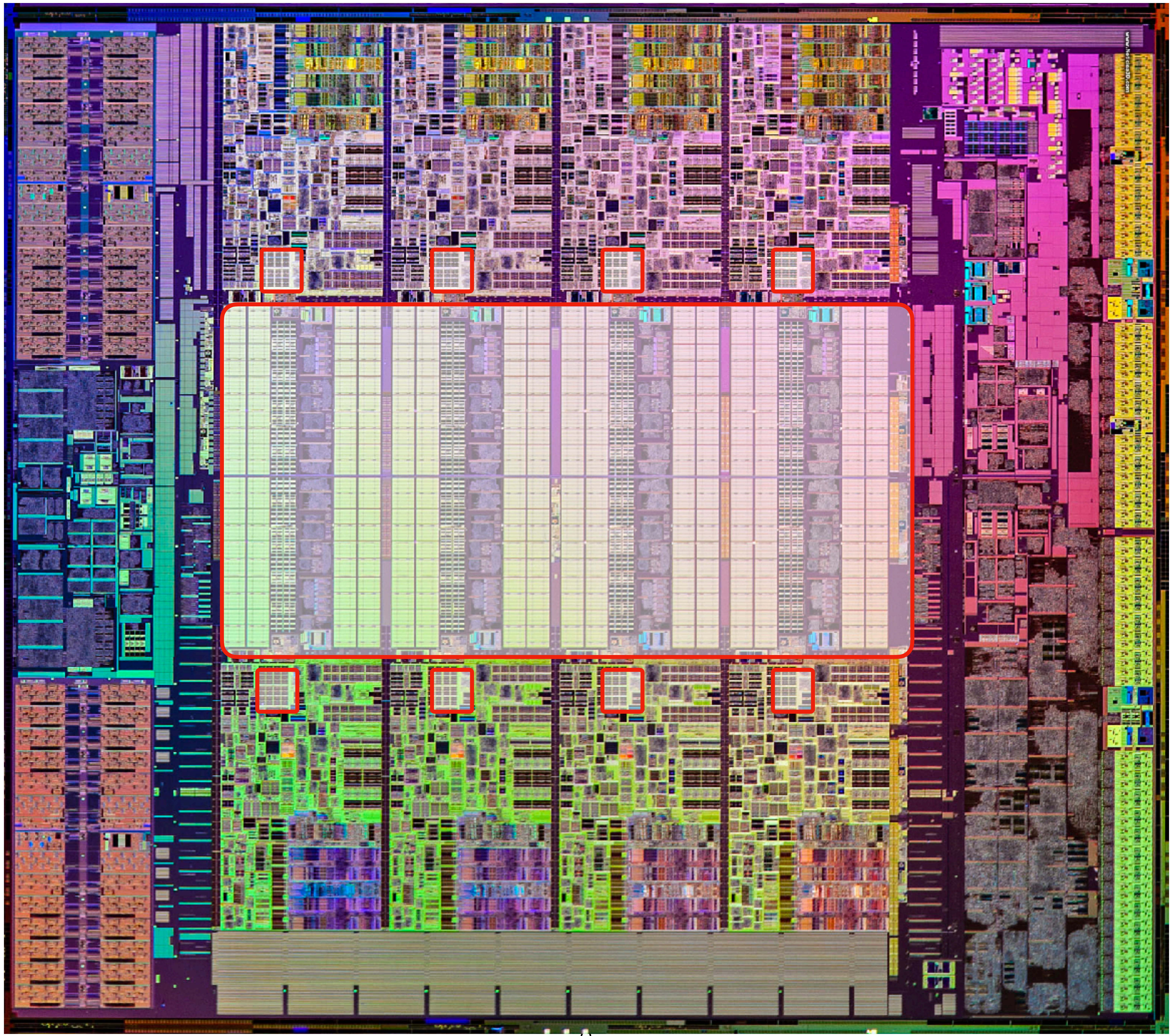

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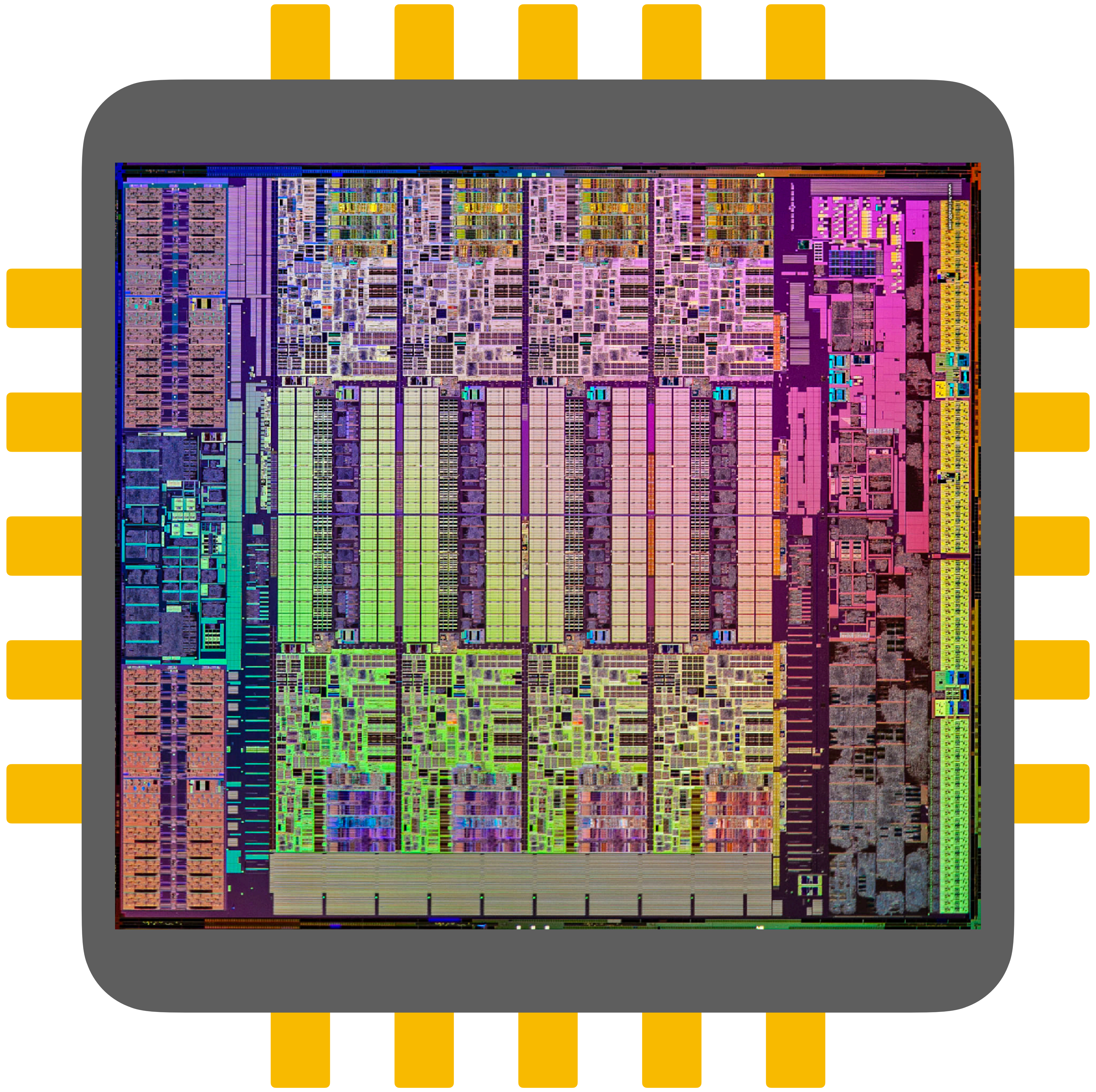
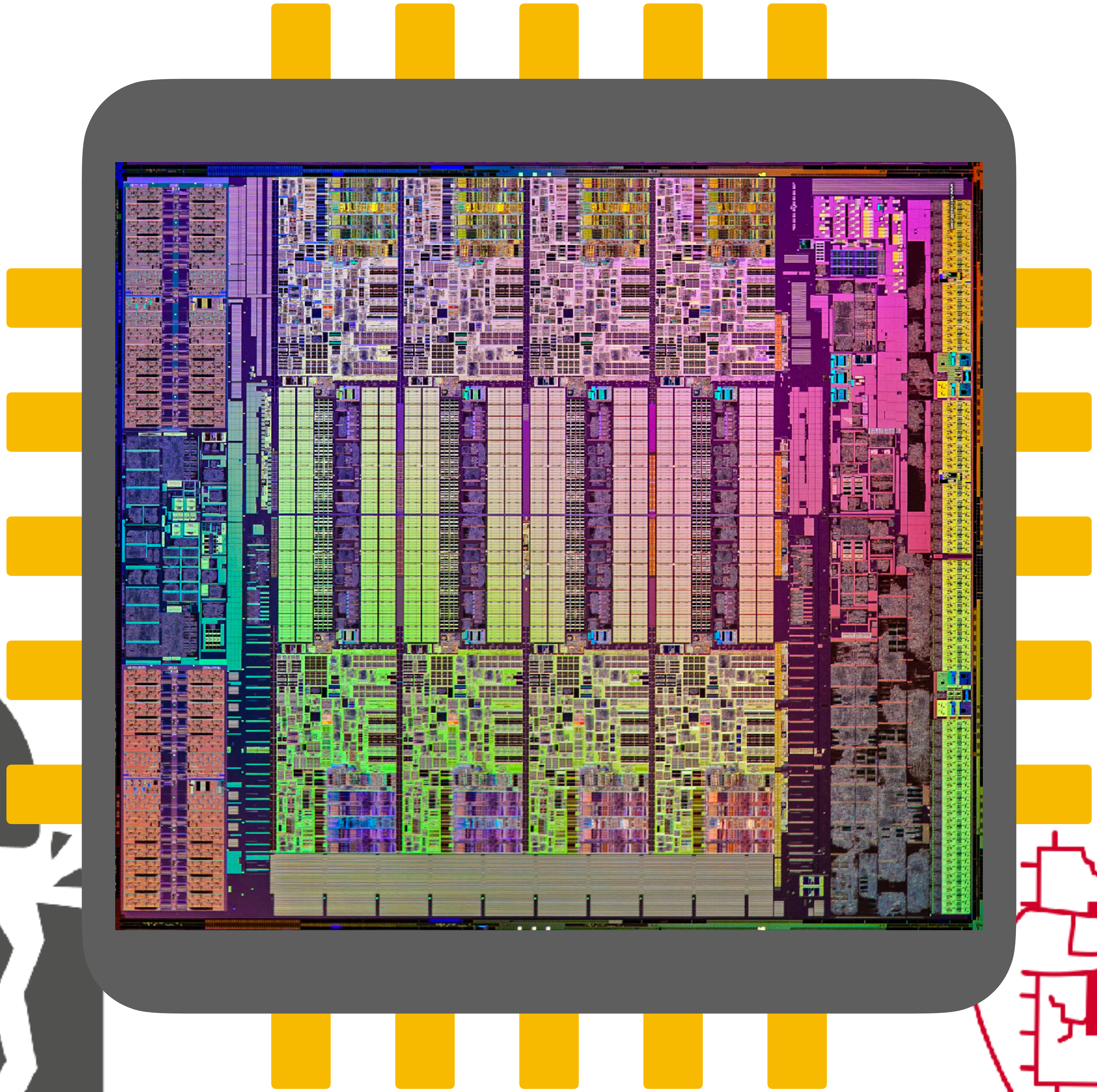


Picture of Intel “Haswell-E” Eight Core CPU

SPECTRE

MELTDOWN



FORESHADOW

MDS

Picture of Intel “Haswell-E” Eight Core CPU

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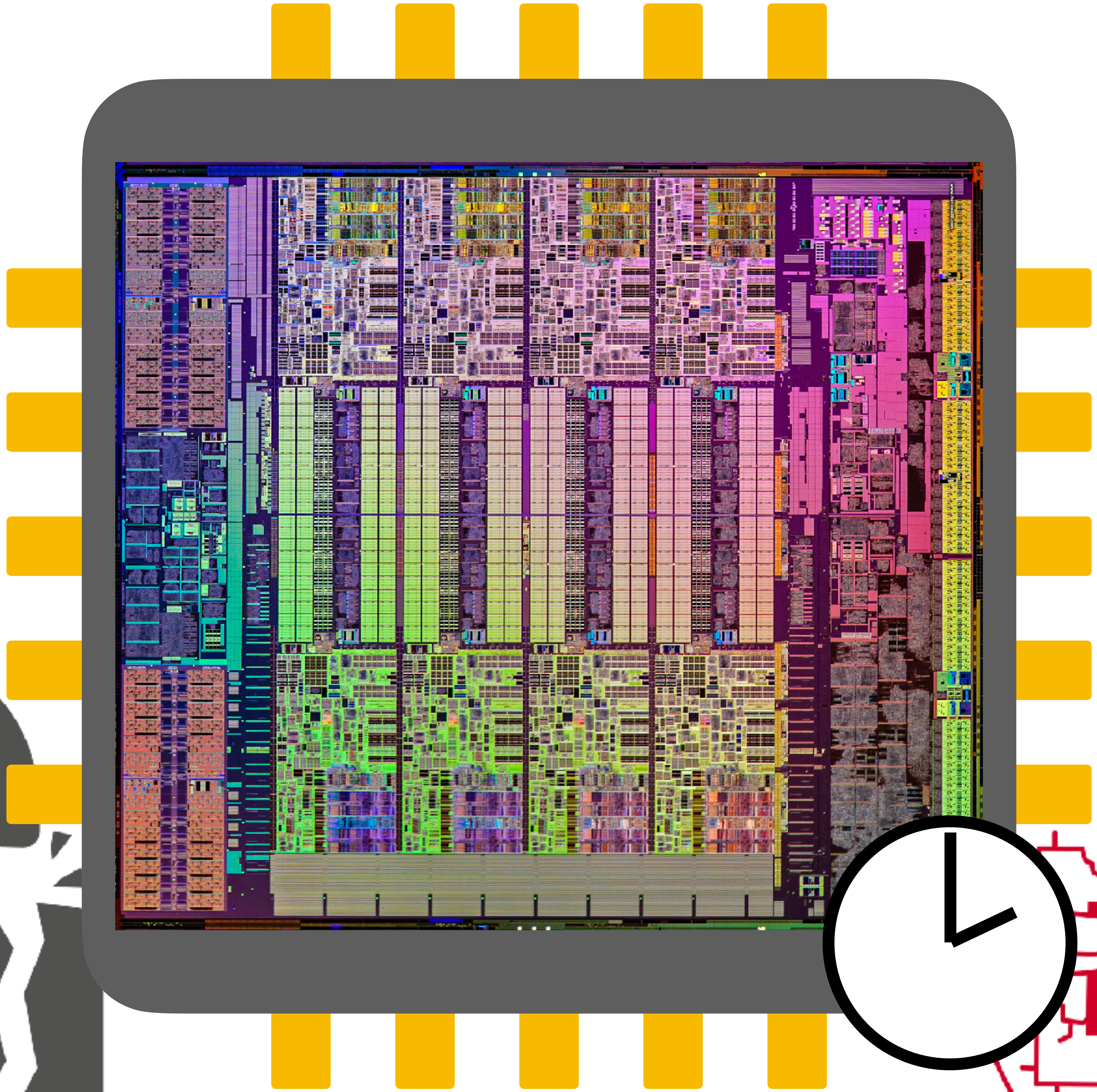

FORESHADOW

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Picture of Intel “Haswell-E” Eight Core CPU

Attacks exploit microarchitectural side-effects to compromise security!

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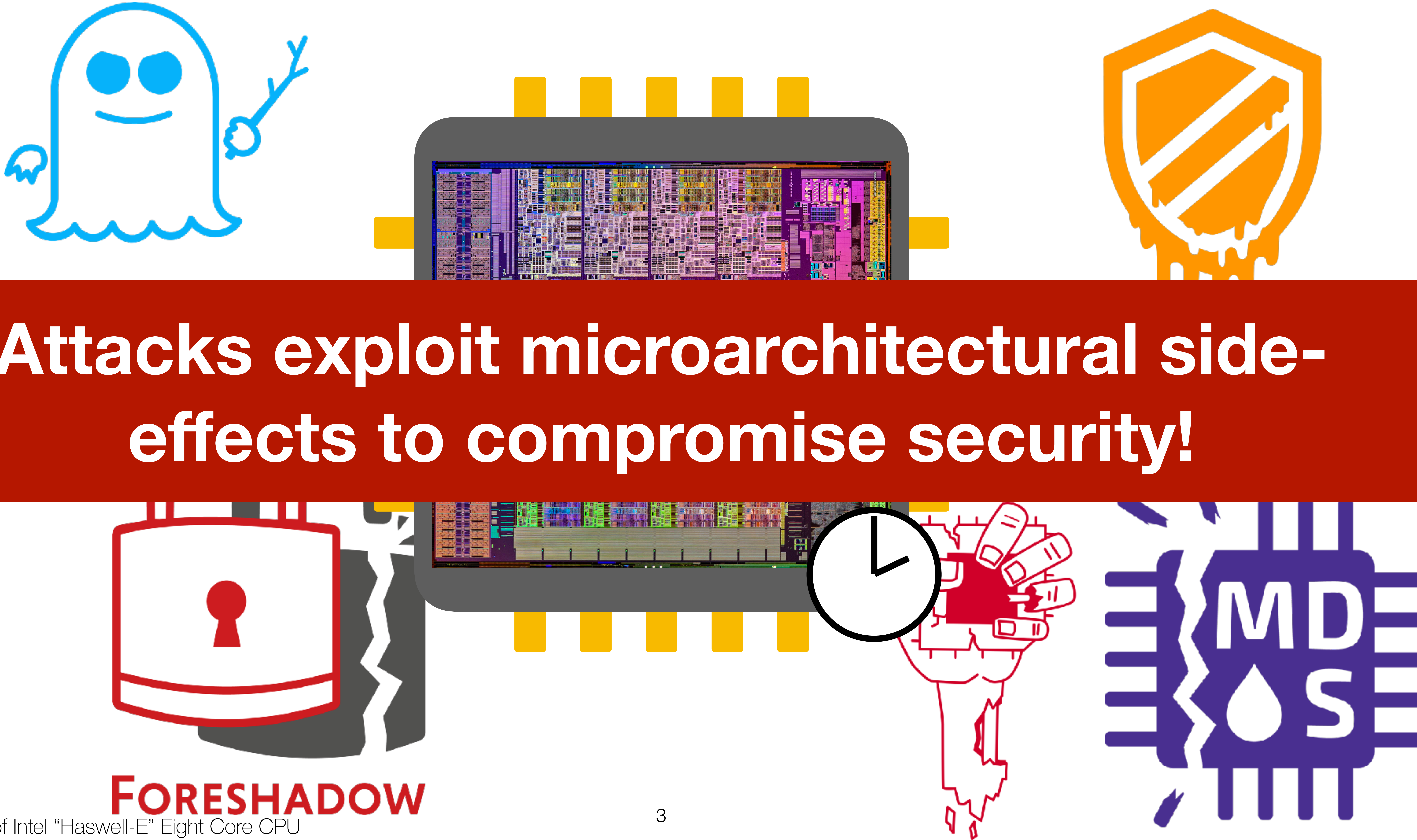

Attacks exploit microarchitectural side-effects to compromise security!

Picture of Intel “Haswell-E” Eight Core CPU

it microarchitect[...] side-compromise s[...]ity!

The New York Times
Researchers Discover Two Major Flaws in the World's Computers

The New York Times
Intel Fixes a Security Flaw It S[...] Repaired 6 Months Ago

BBC
Intel Zombieload bug fix to slow data centre computers

BBC
Meltdown fix can make some machines slower - Intel
Intel has admitted that patches to fix the Spectre and Meltdown chip flaws could slow machines "in some cases"

FOX BUSINESS
WASHINGTON, D.C.
NEWS ALERT
INTEL REVEALS DESIGN FLAW THAT COULD ALLOW HACKERS TO ACCESS DATA
WINTER STORM
@FOXB
DEVELOPING STORY
COMPUTER CHIP FLAWS IMPACT BILLIONS OF DEVICES
LIVE
CNN
DAX ▲164.69
NEWS STREAM
MDS

Picture c

The New York Times

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NEWS ALERT

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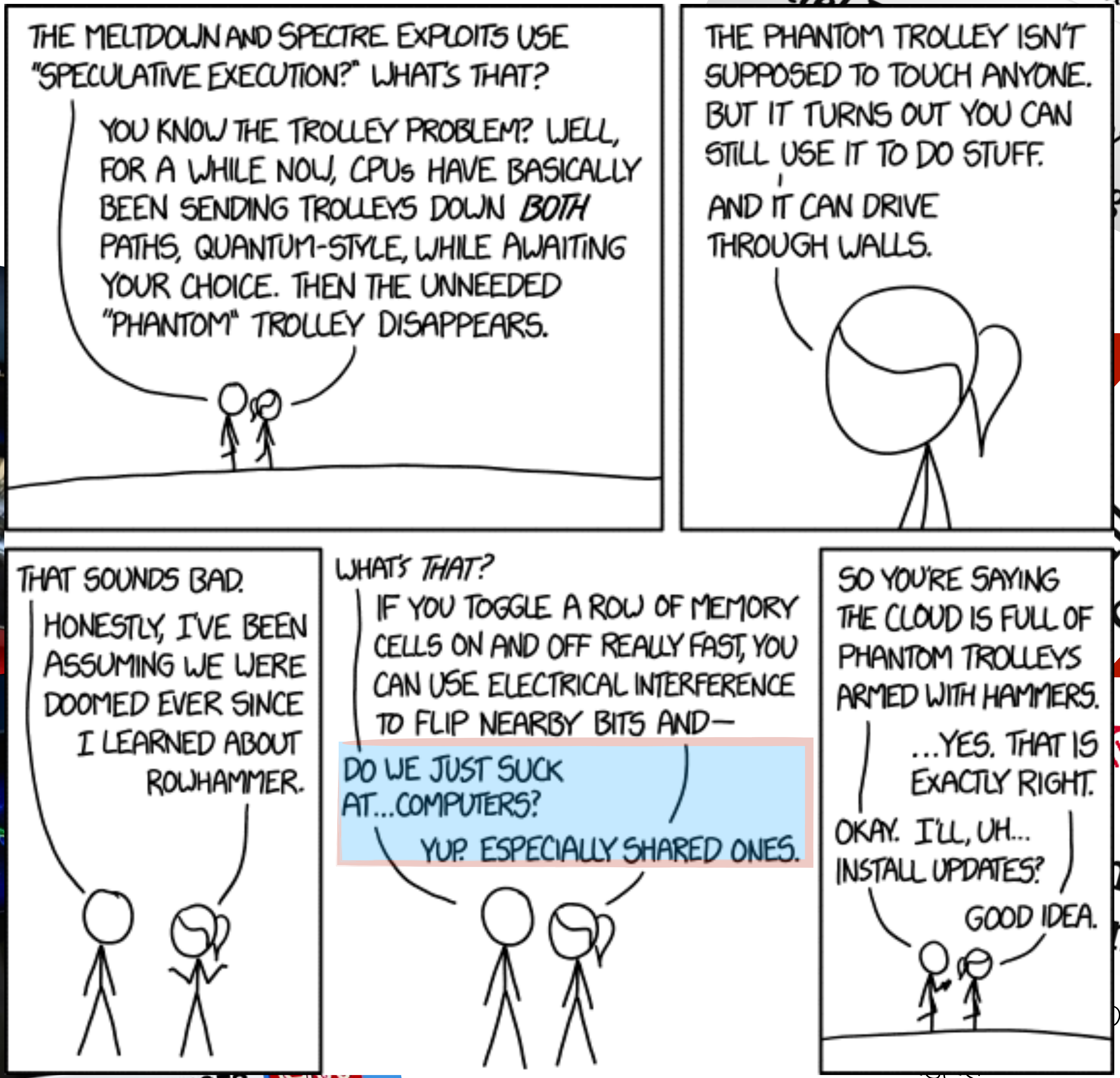
DEVELOPING STORY

COMPUTER CHIP FLAWS IMPACT BILLIONS OF DEVICES

DAX ▲164.69

NEWS STREAM


THE MELTDOWN AND SPECTRE EXPLOITS USE "SPECULATIVE EXECUTION?" WHAT'S THAT?
YOU KNOW THE TROLLEY PROBLEM? WELL, FOR A WHILE NOW, CPUs HAVE BASICALLY BEEN SENDING TROLLEYS DOWN BOTH PATHS, QUANTUM-STYLE, WHILE AWAITING YOUR CHOICE. THEN THE UNNEEDED "PHANTOM" TROLLEY DISAPPEARS.
THE PHANTOM TROLLEY ISN'T SUPPOSED TO TOUCH ANYONE. BUT IT TURNS OUT YOU CAN STILL USE IT TO DO STUFF.
AND IT CAN DRIVE THROUGH WALLS.
THAT SOUNDS BAD.
HONESTLY, I'VE BEEN ASSUMING WE WERE DOOMED EVER SINCE I LEARNED ABOUT ROWHAMMER.
WHAT'S THAT?
IF YOU TOGGLE A ROW OF MEMORY CELLS ON AND OFF REALLY FAST, YOU CAN USE ELECTRICAL INTERFERENCE TO FLIP NEARBY BITS AND—
DO WE JUST SUCK AT...COMPUTERS?
YUP. ESPECIALLY SHARED ONES.
SO YOU'RE SAYING THE CLOUD IS FULL OF PHANTOM TROLLEYS ARMED WITH HAMMERS.
...YES. THAT IS EXACTLY RIGHT.
OKAY. I'LL, UH... INSTALL UPDATES?
GOOD IDEA.

The New York Times

Intel

Flaw It

bieload bug fix to slow data computers

ake some ntel

fix the could slow

MDS

side-

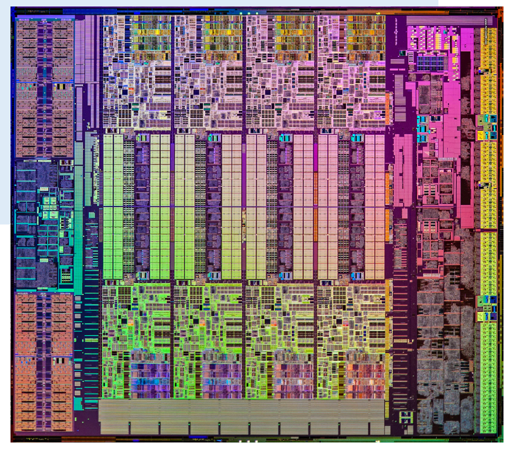
ity!

Picture c

What is the problem?

What is the problem?

Microarchitectural leakage depends on ***specific hardware details***



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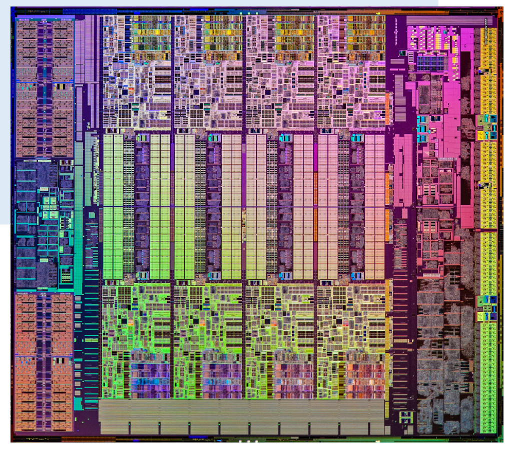

No ***faithful***, ***precise*** models capturing ***microarchitectural leakage***

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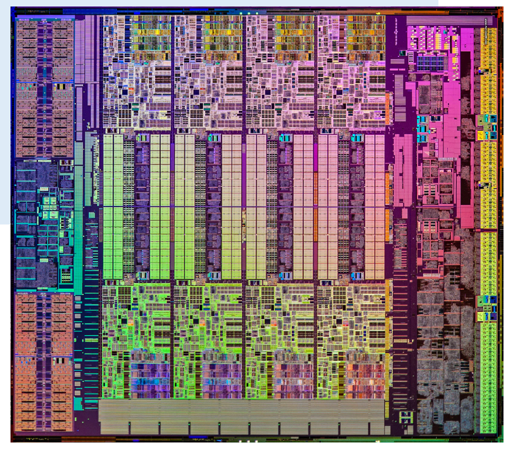

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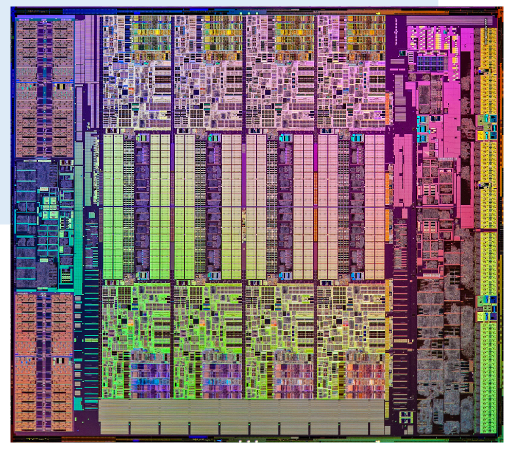
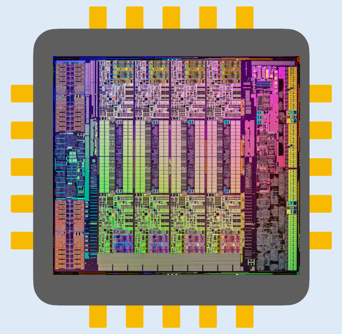
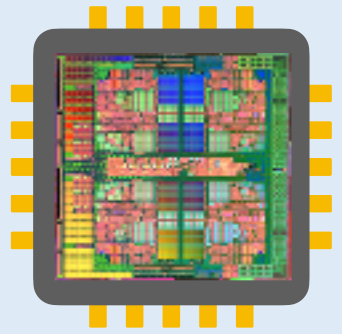


No ***faithful***, ***precise*** models capturing ***microarchitectural leakage***

Writing secure code is almost **impossible**

P +  = **Secure**

P +  = **Insecure**

A problem of (missing) abstractions

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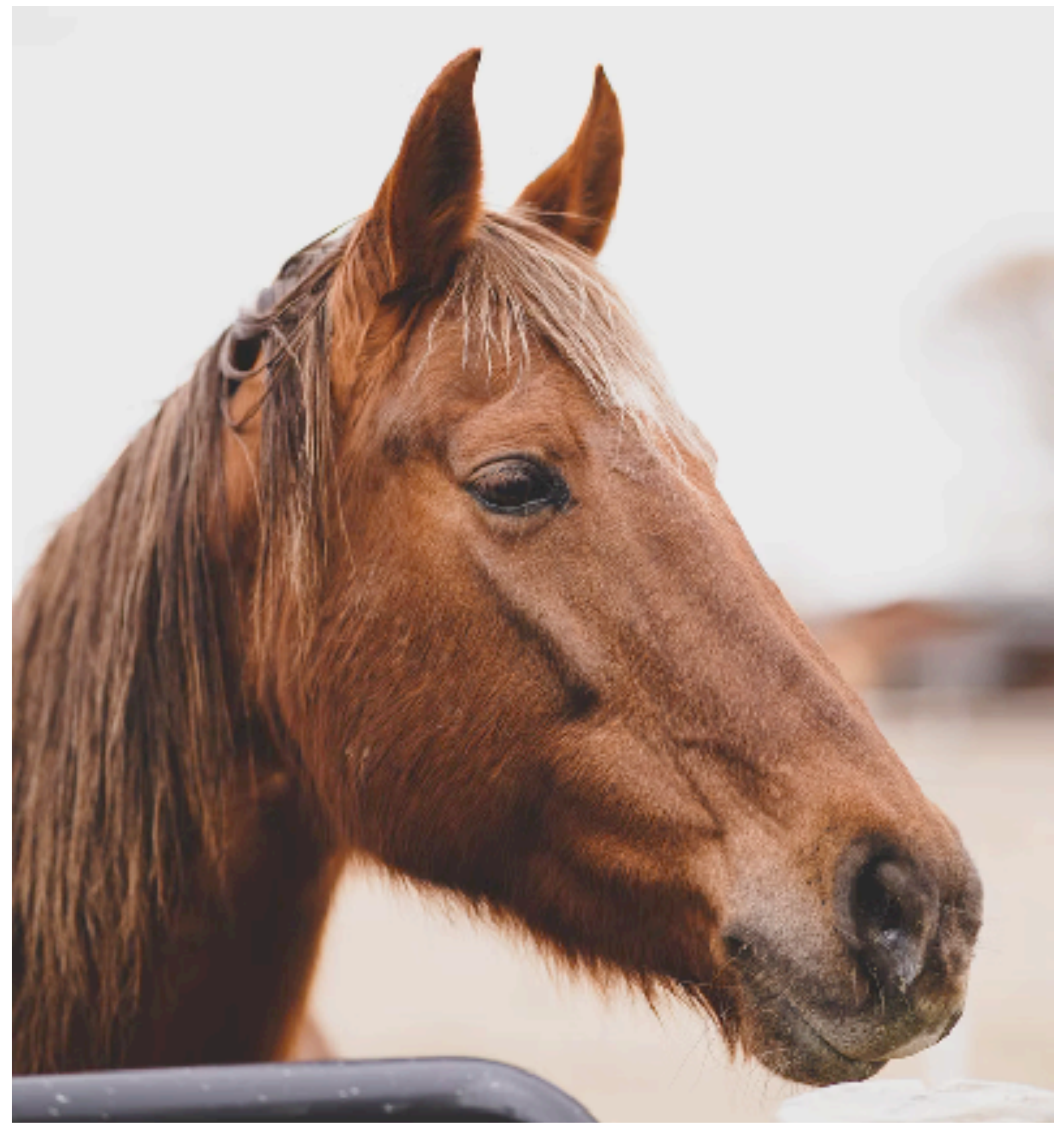

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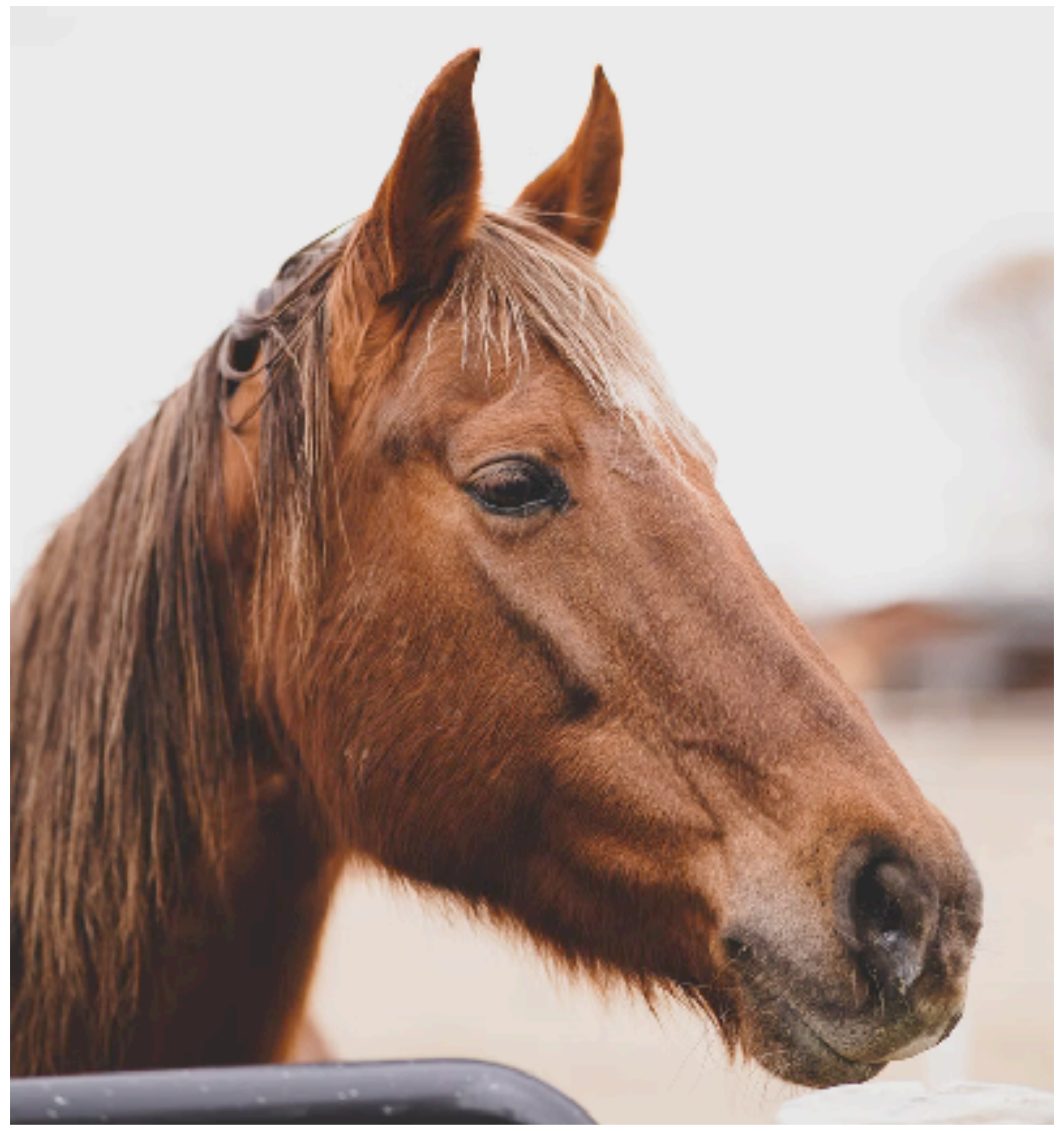
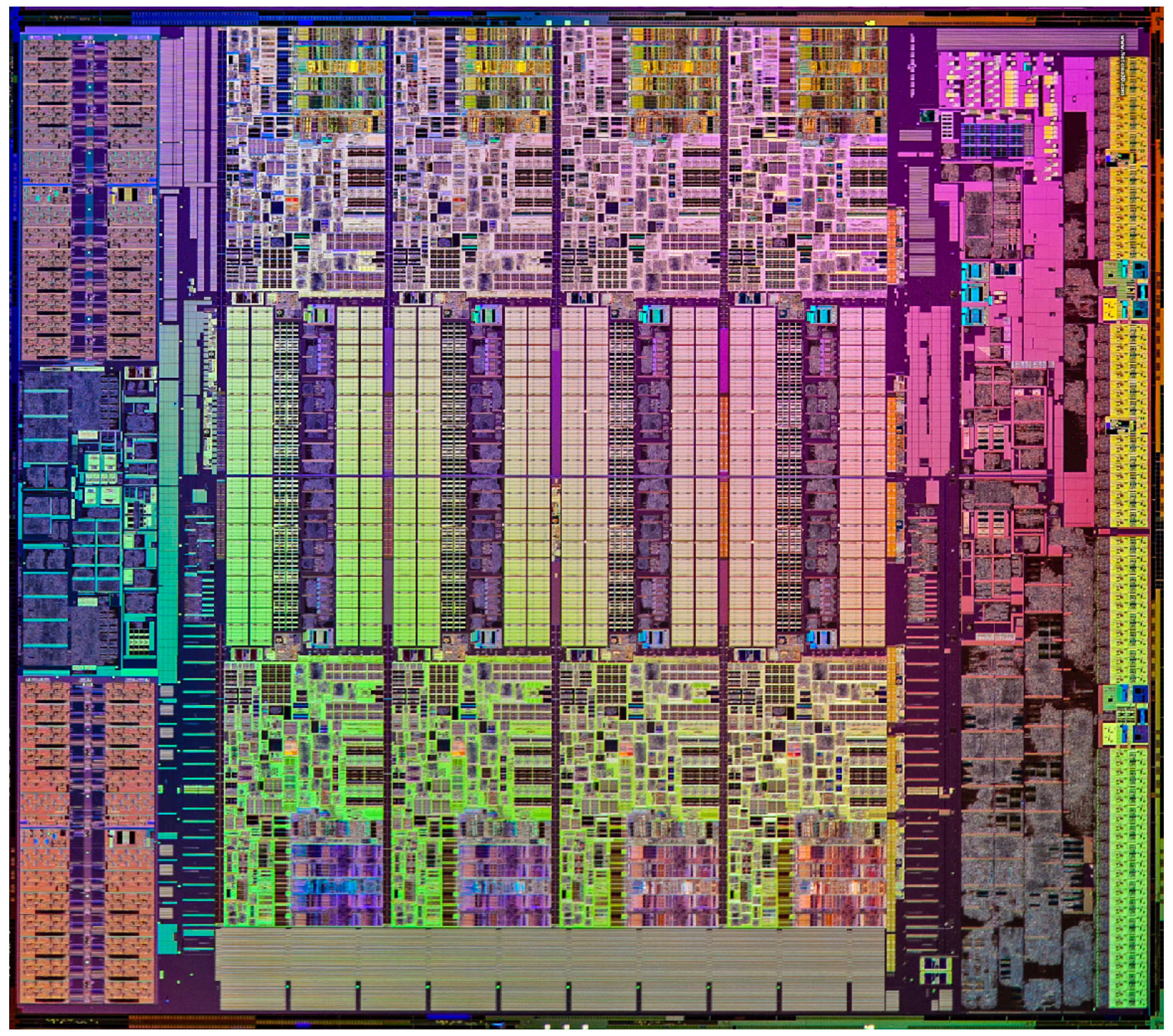
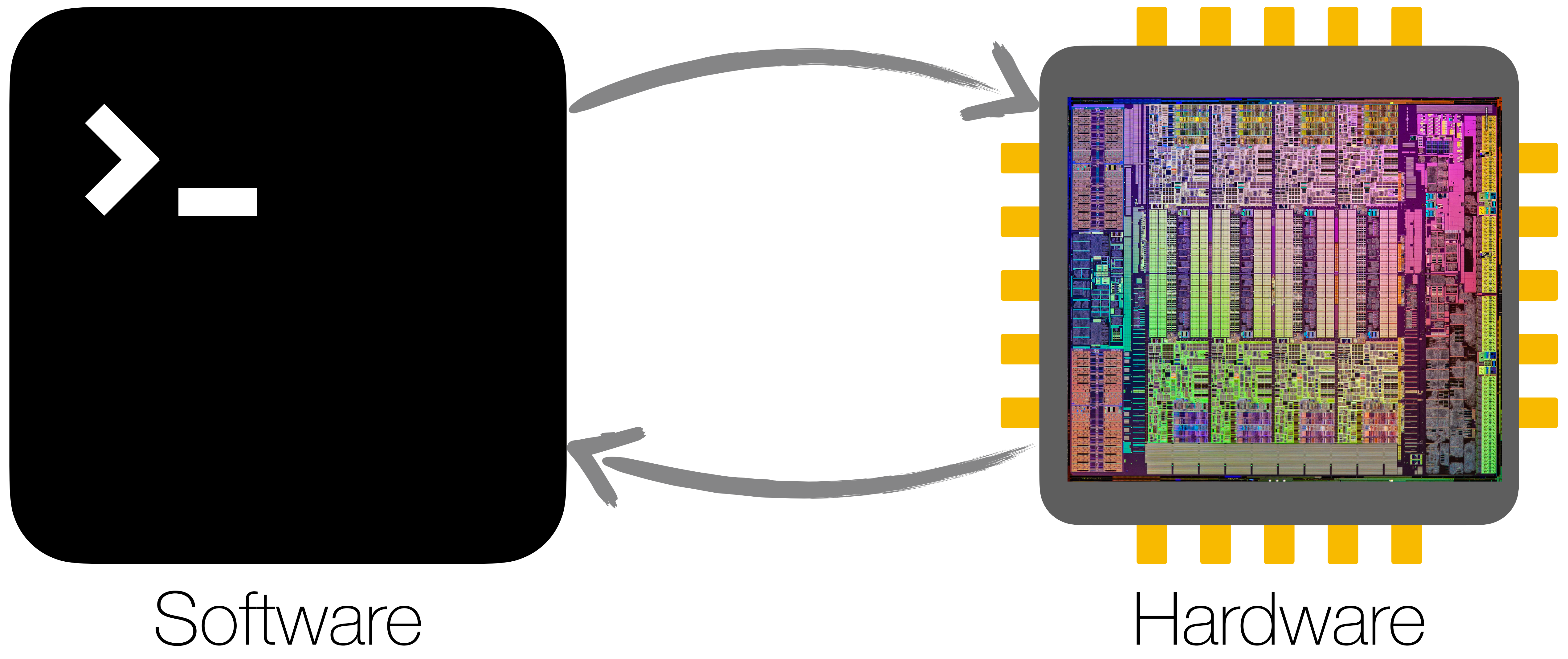




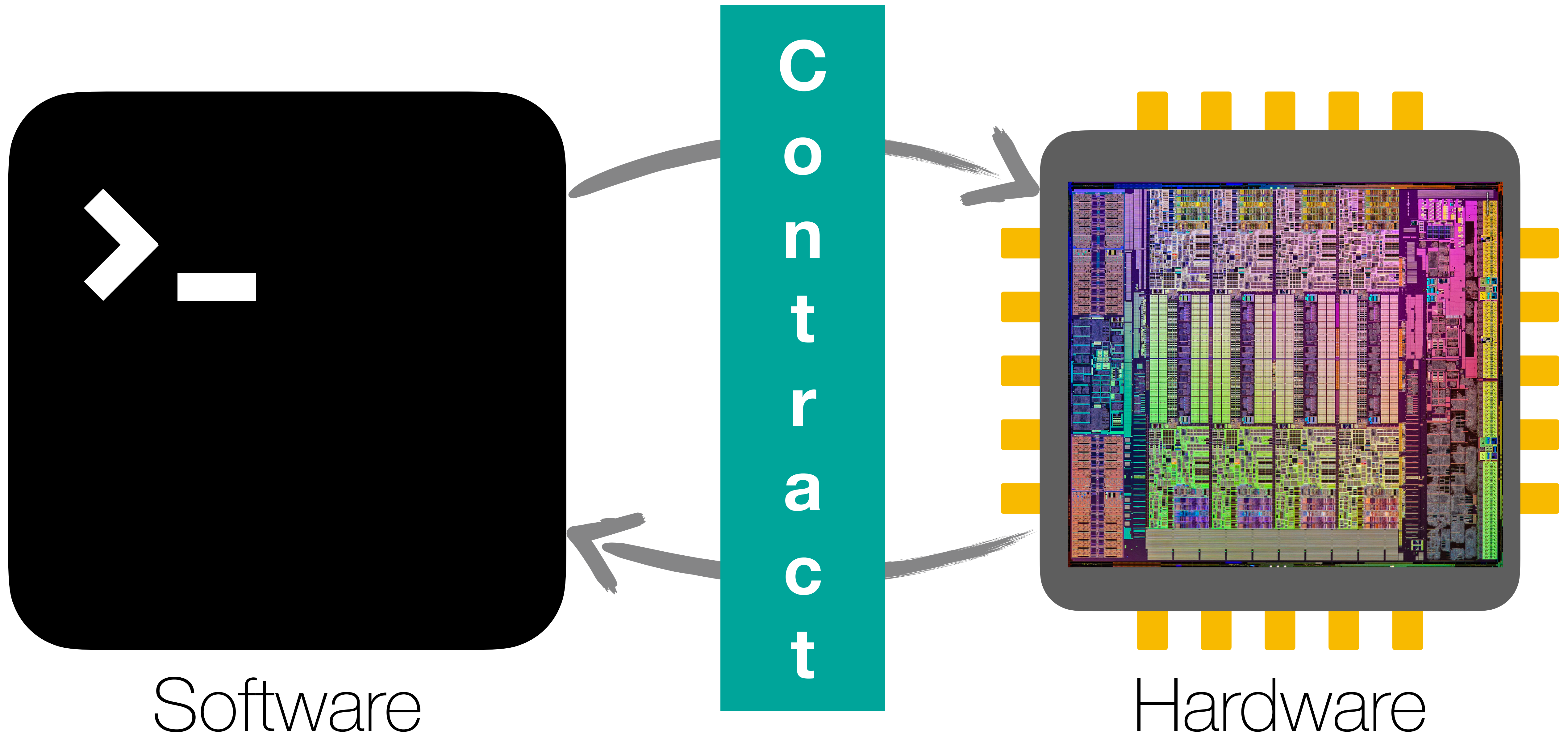
🧐???

What is a good abstraction?



What is a good abstraction?

Hardware-software **contracts** for ***security***



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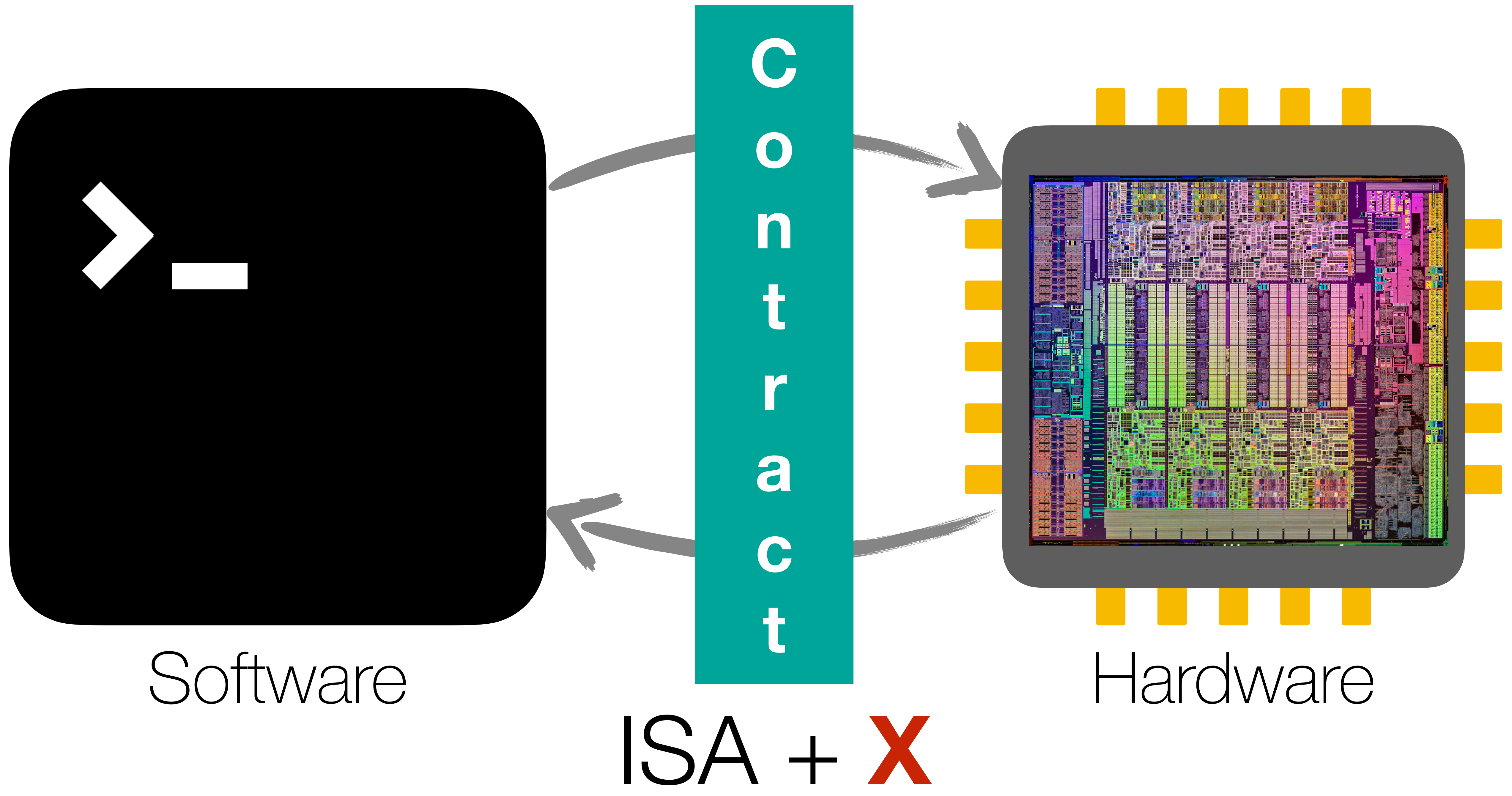
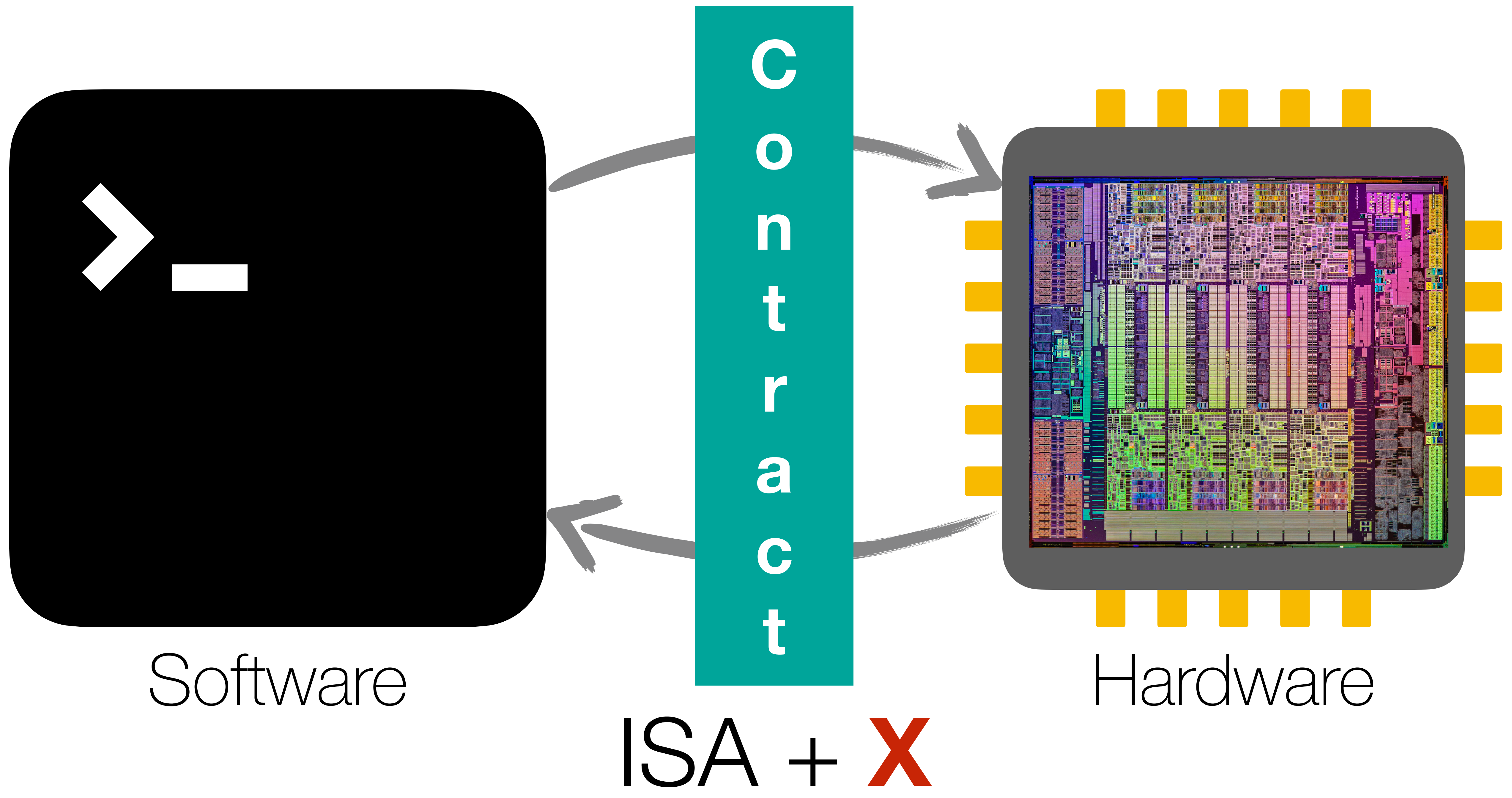


What is a good abstraction?

Hardware-software **contracts** for ***security***

Capture all possible ***microarchitectural leaks***!



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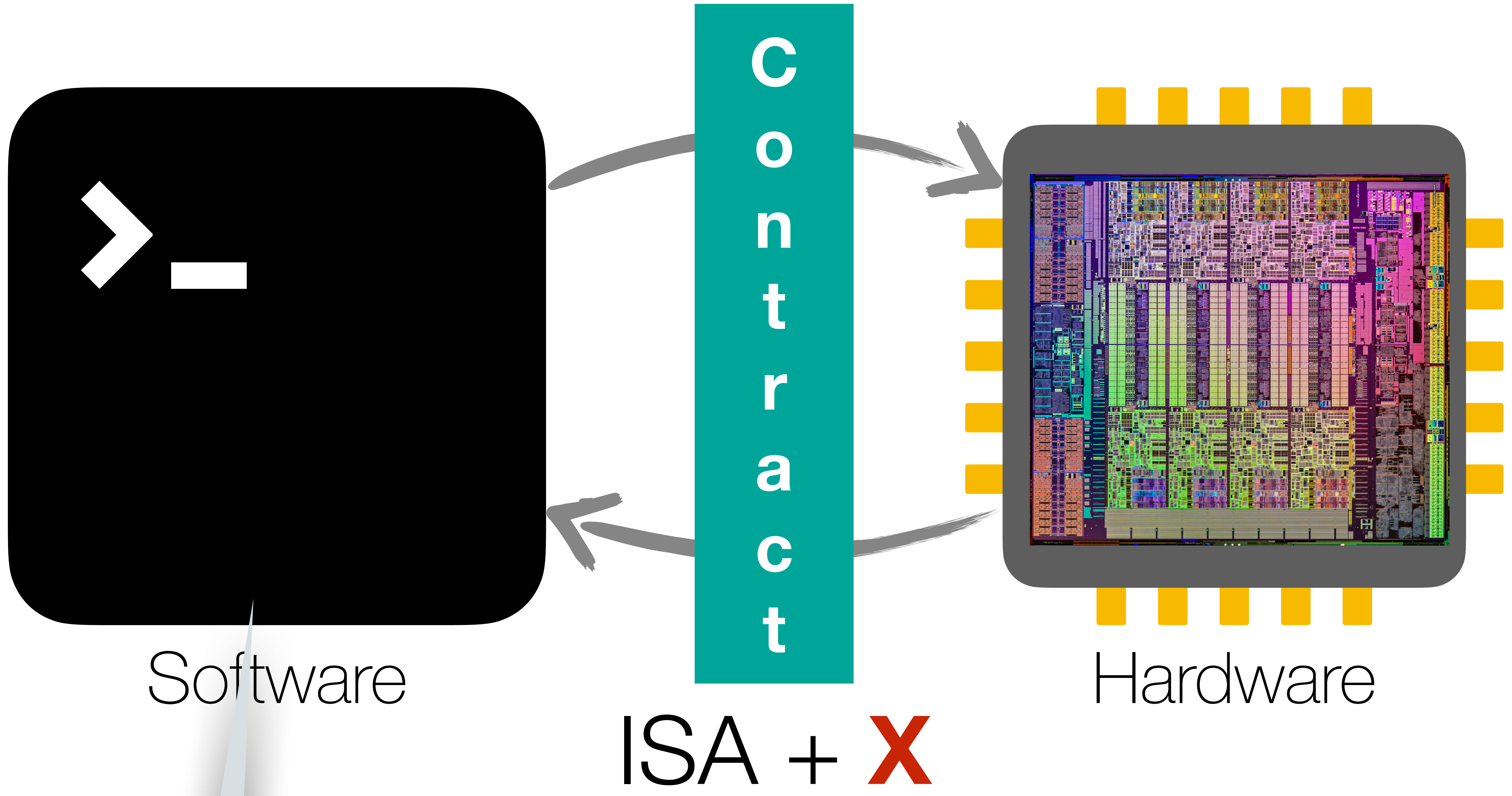

Secure programming **independently** of specific microarchitecture

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Hardware-software **contracts** for ***security***

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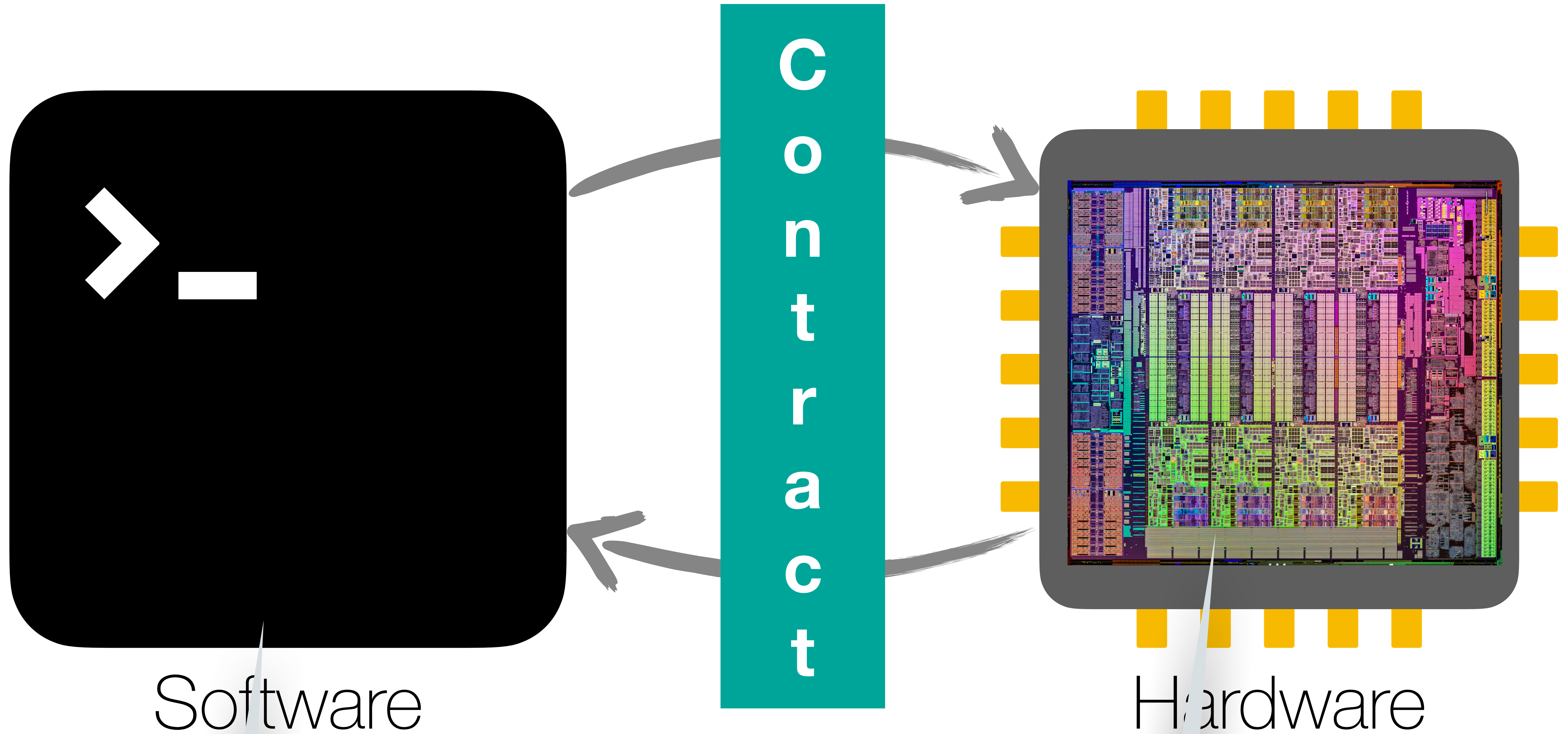

ISA + **X**

Secure programming **independently** of specific microarchitecture

Implement ***optimizations*** **compliant** with contract

In this talk

In this talk

HW/SW contracts for ***secure speculation***

In this talk

HW/SW contracts for ***secure speculation***

Contracts + ***Hardware***

In this talk

HW/SW contracts for ***secure speculation***

Contracts + ***Hardware***

Contracts + ***Software***

Outline

1. Speculative execution attacks
2. Modeling speculative leaks
3. Hardware-software contracts for secure speculation
4. What about hardware?
5. What about software?
6. Conclusions

Outline

Exploits ***speculative execution***

Almost ***all*** modern ***CPUs*** are ***affected***

P. Kocher, J. Horn, A. Fogh, D. Genkin, D. Gruss, W. Haas, M. Hamburg, M. Lipp, S. Mangard, T. Prescher, M. Schwarz, Y. Yarom — Spectre Attacks: Exploiting Speculative Execution — S&P 2019

Speculative execution + branch prediction

Size of array **A**

```
if (x < A_size)
    y = B[A[x]]
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HELP

Branch predictor

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Prediction based on ***branch history*** & ***program structure***

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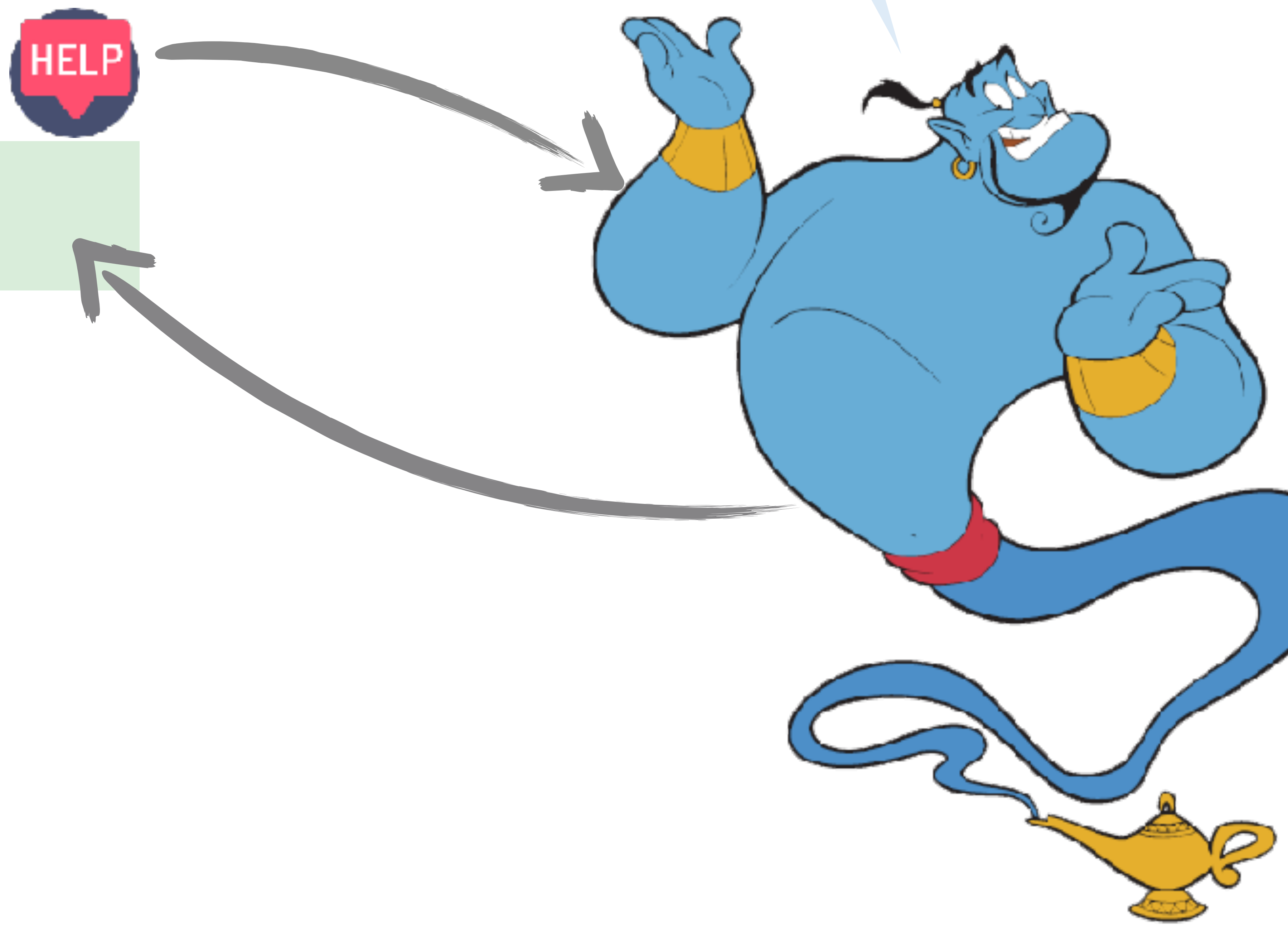

Branch predictor

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HELP

Branch predictor

Wrong predicton? ***Rollback changes***!

✓ Architectural (ISA) state

✗ Microarchitectural state

Spectre v1

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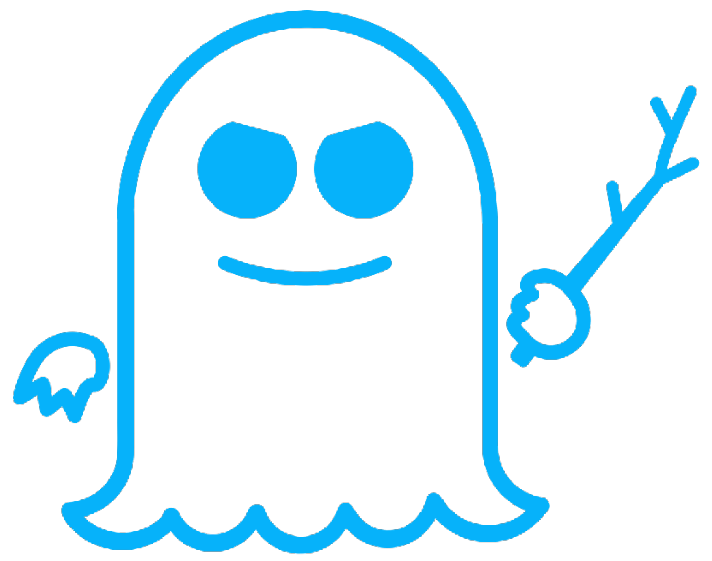

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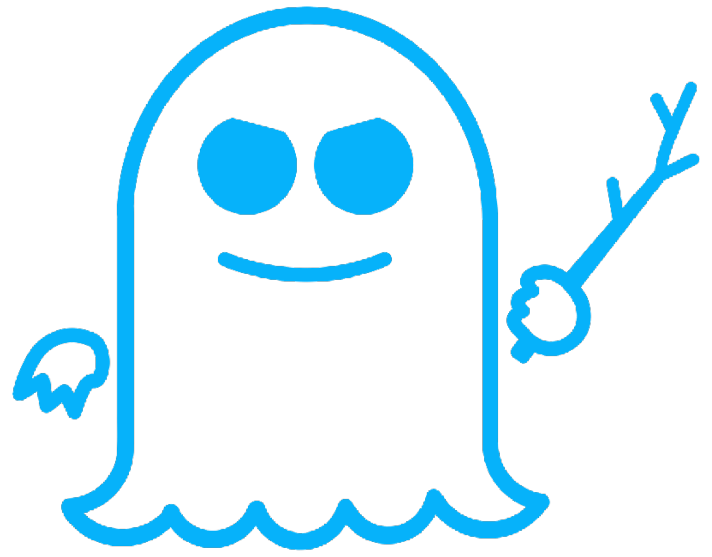

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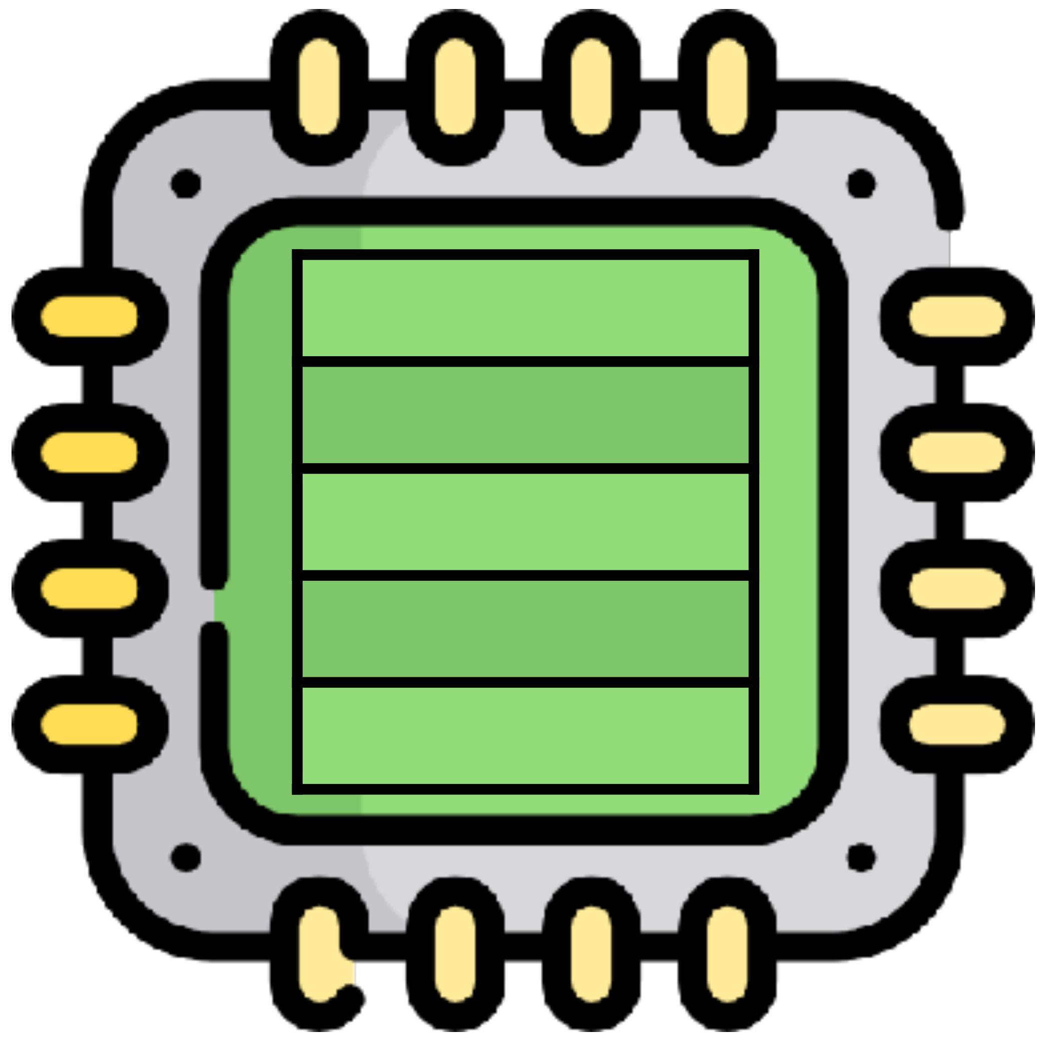

Spectre v1

```
void f(int x)
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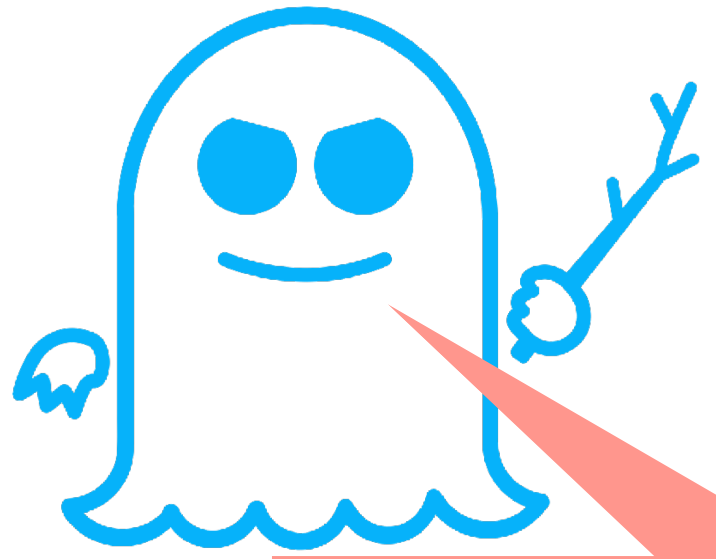
```

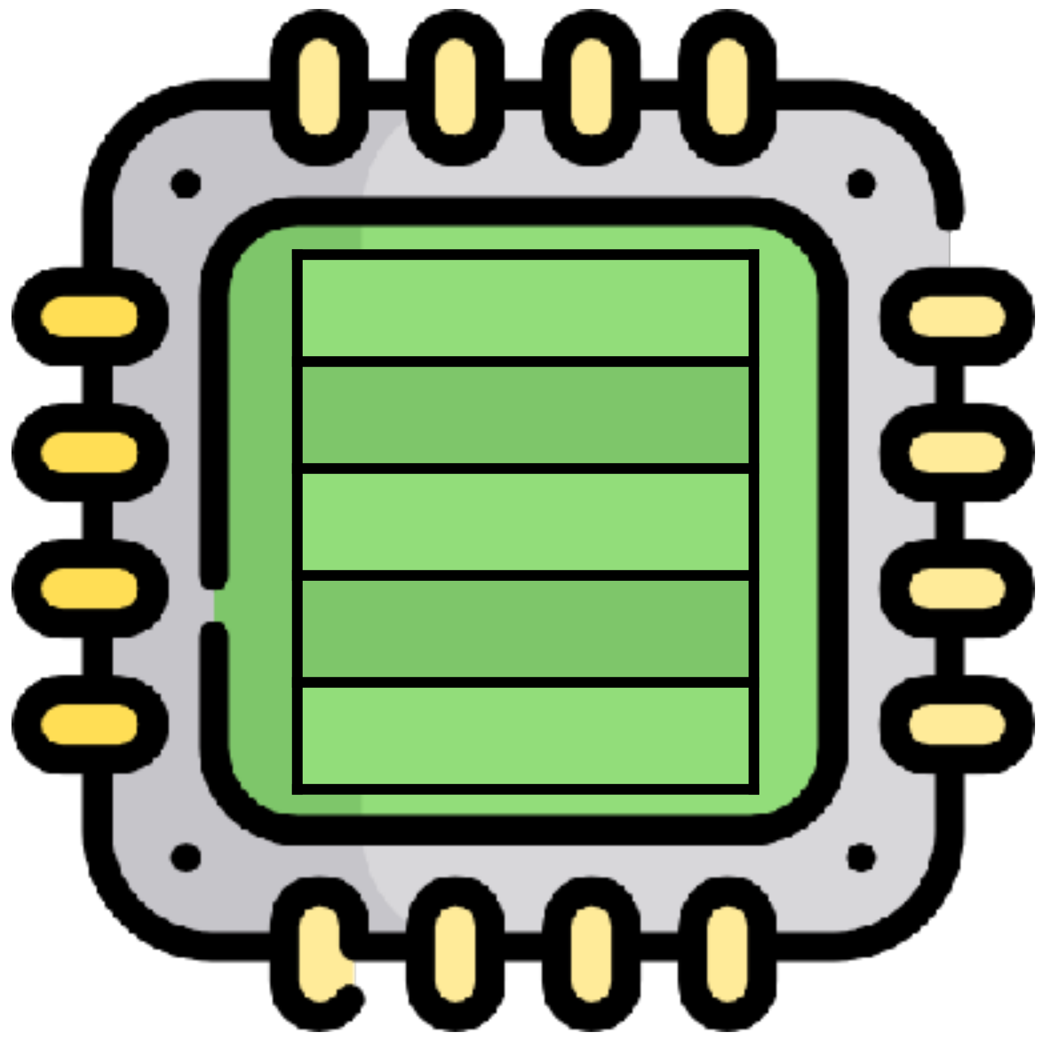
A_size=16

B	B[0]	B[1]	...



Secret data

What is in A[128]?



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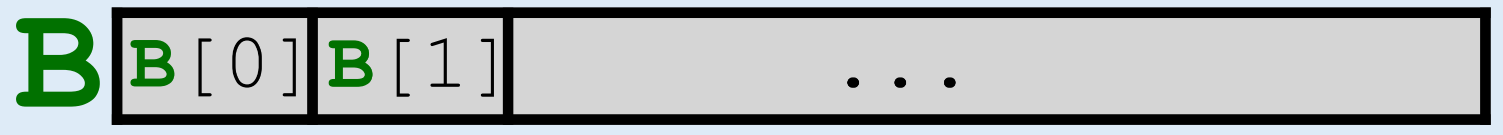

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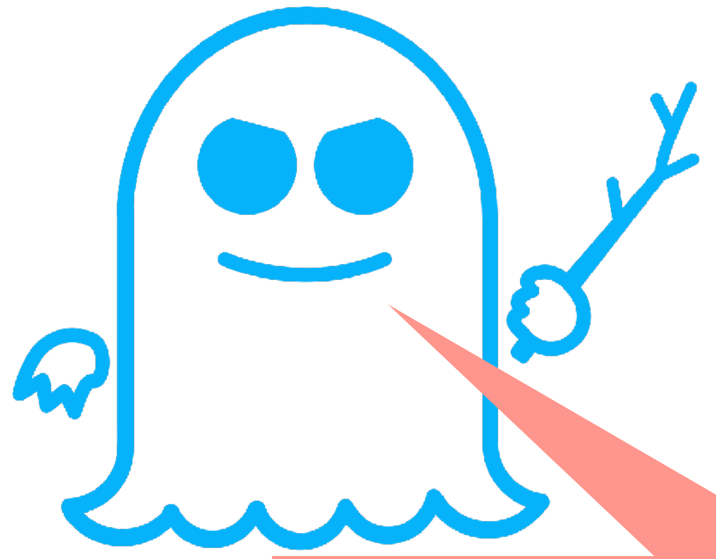

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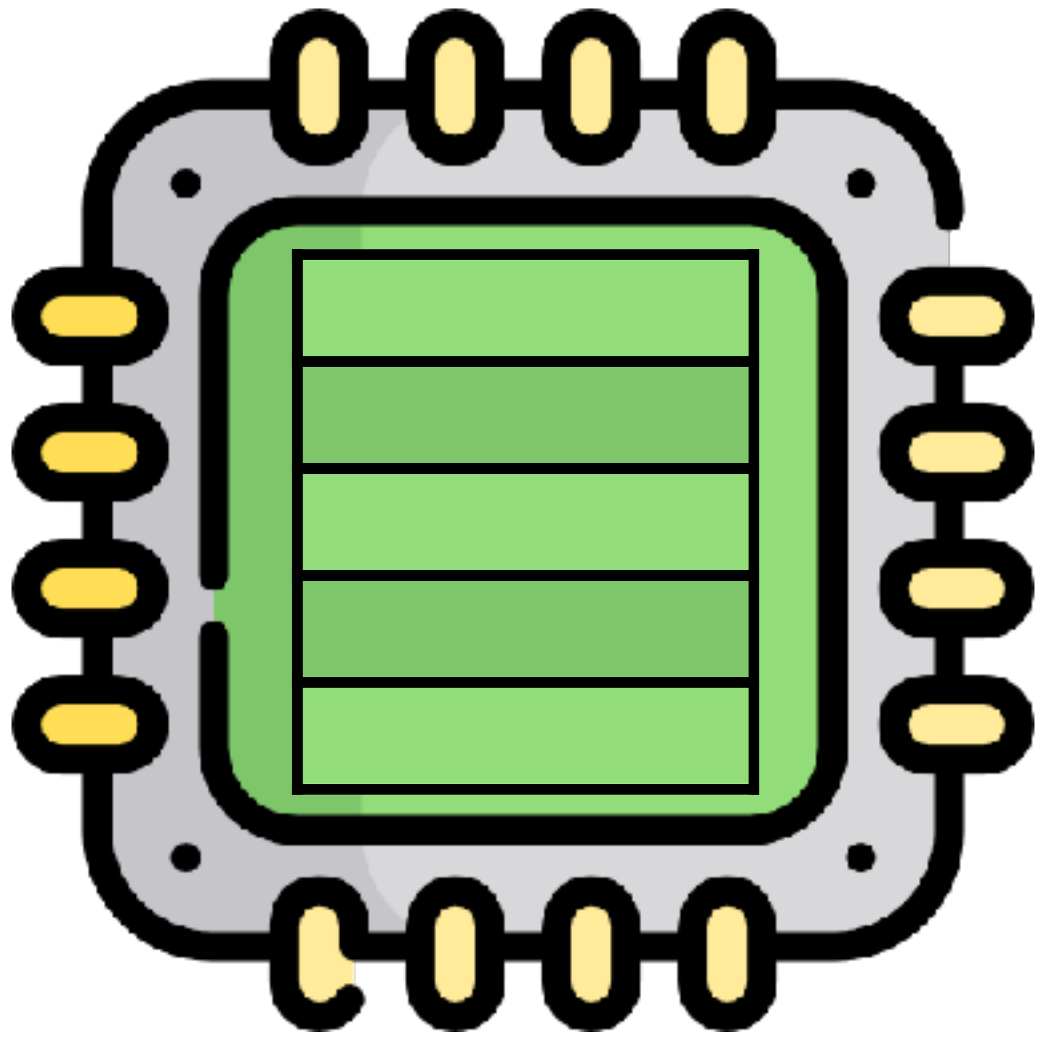
What is in A[128]?

1) Train branch predictor



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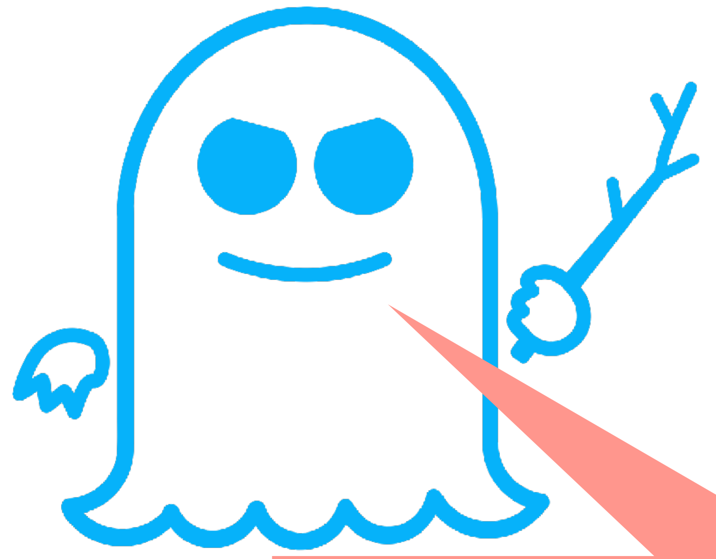

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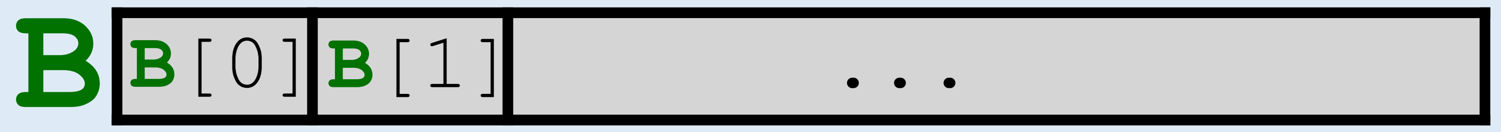

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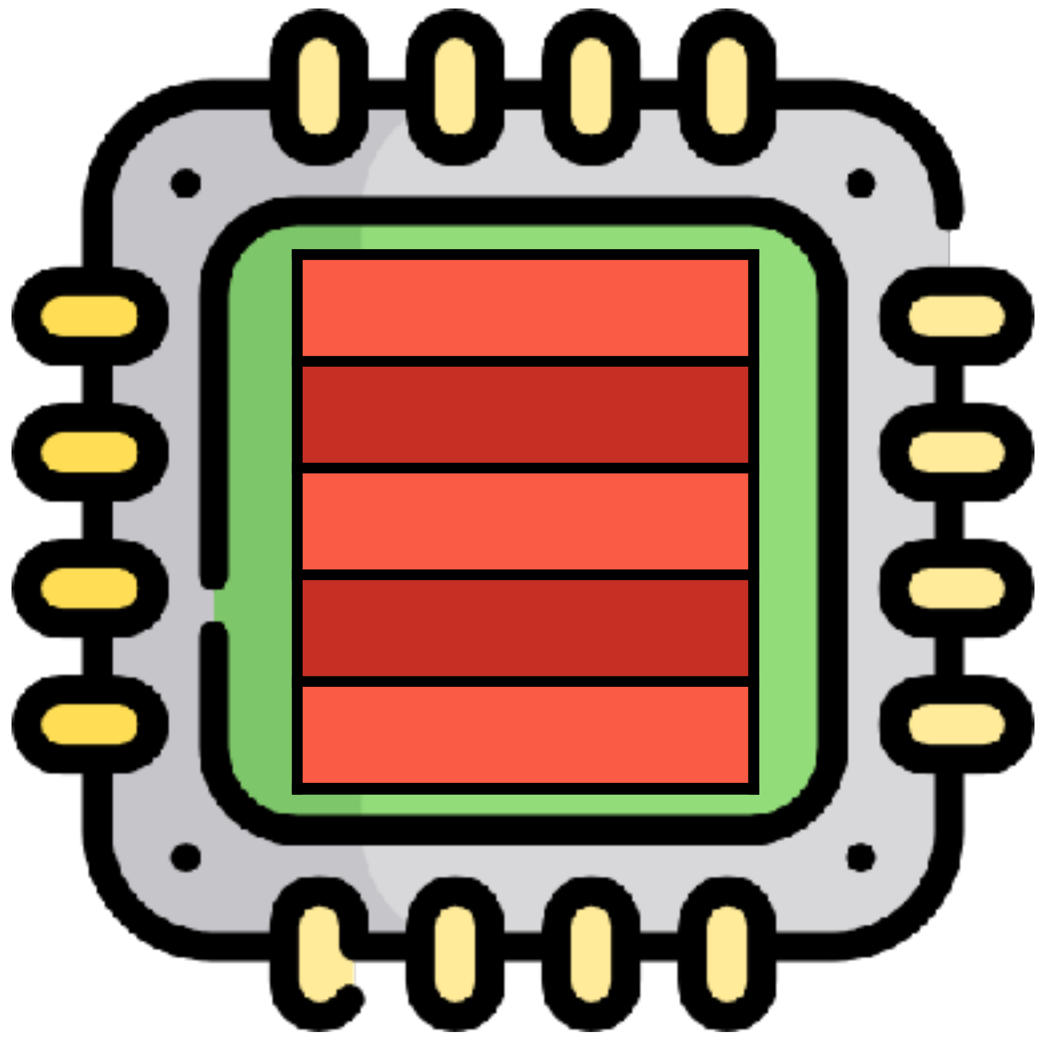

1) Train branch predictor

2) Prepare cache

Spectre v1

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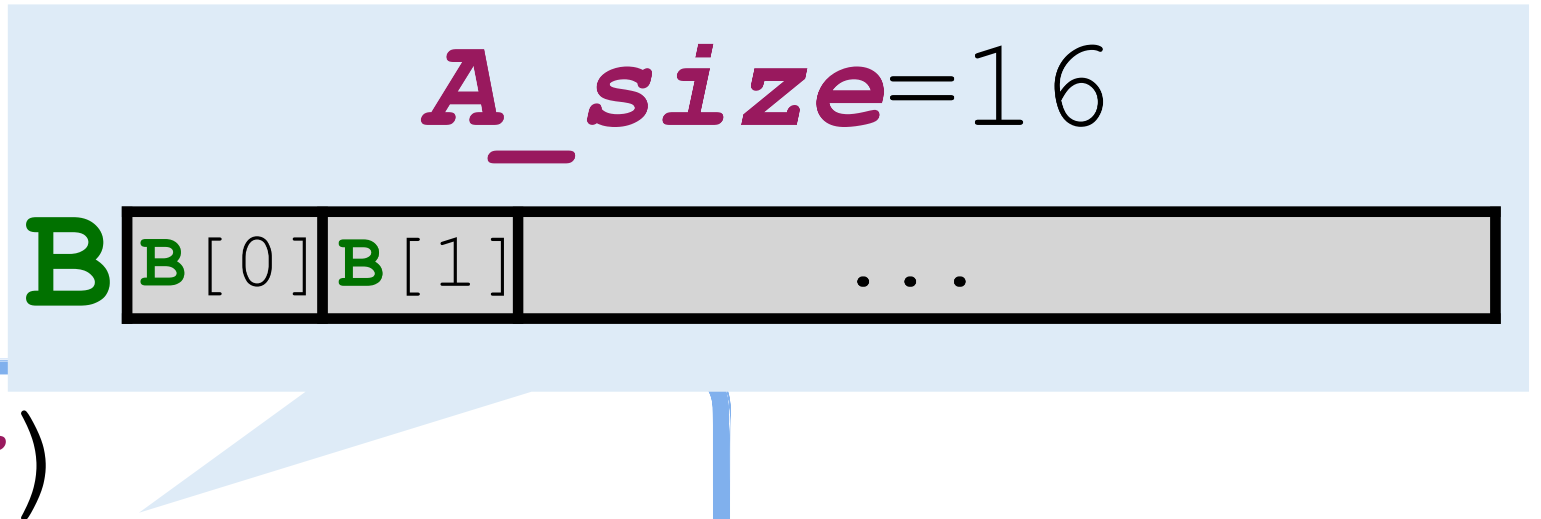

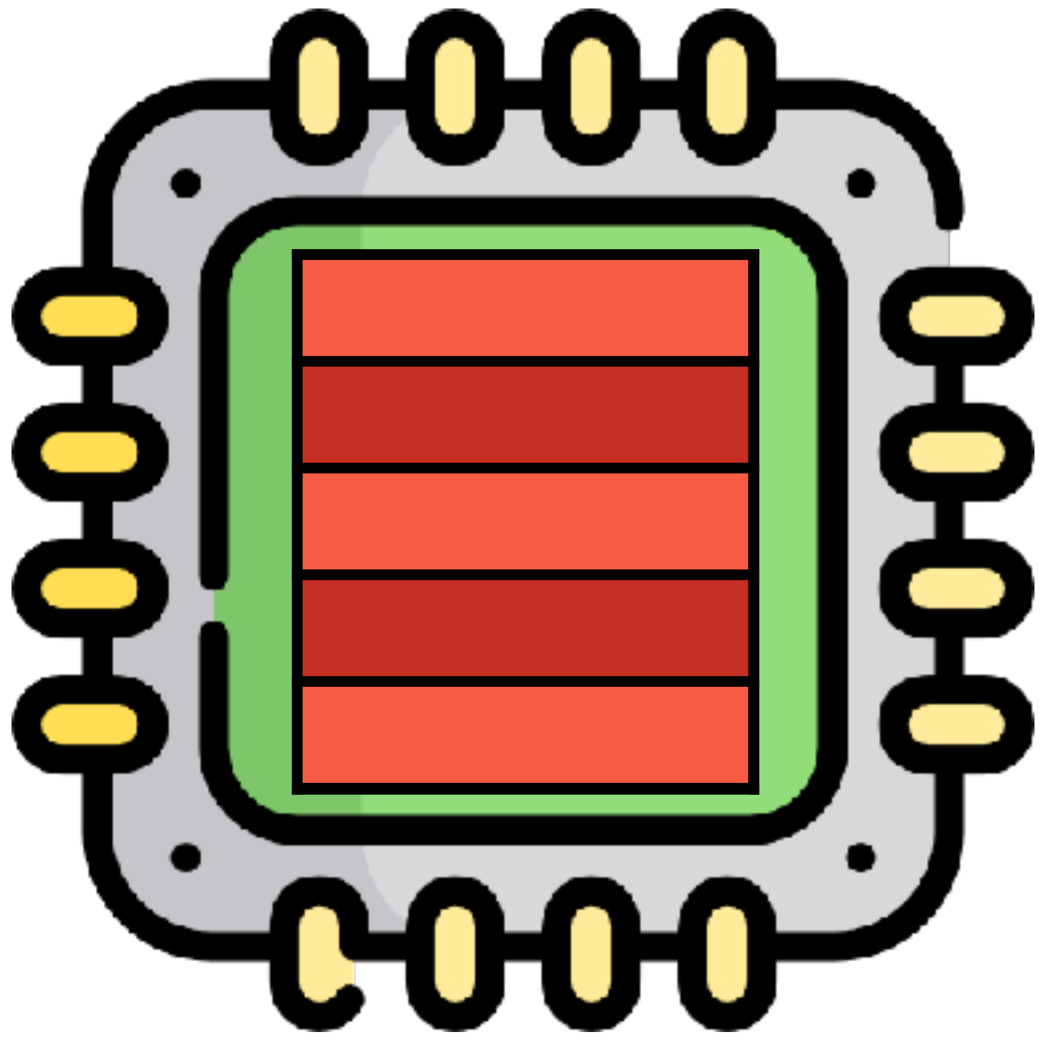

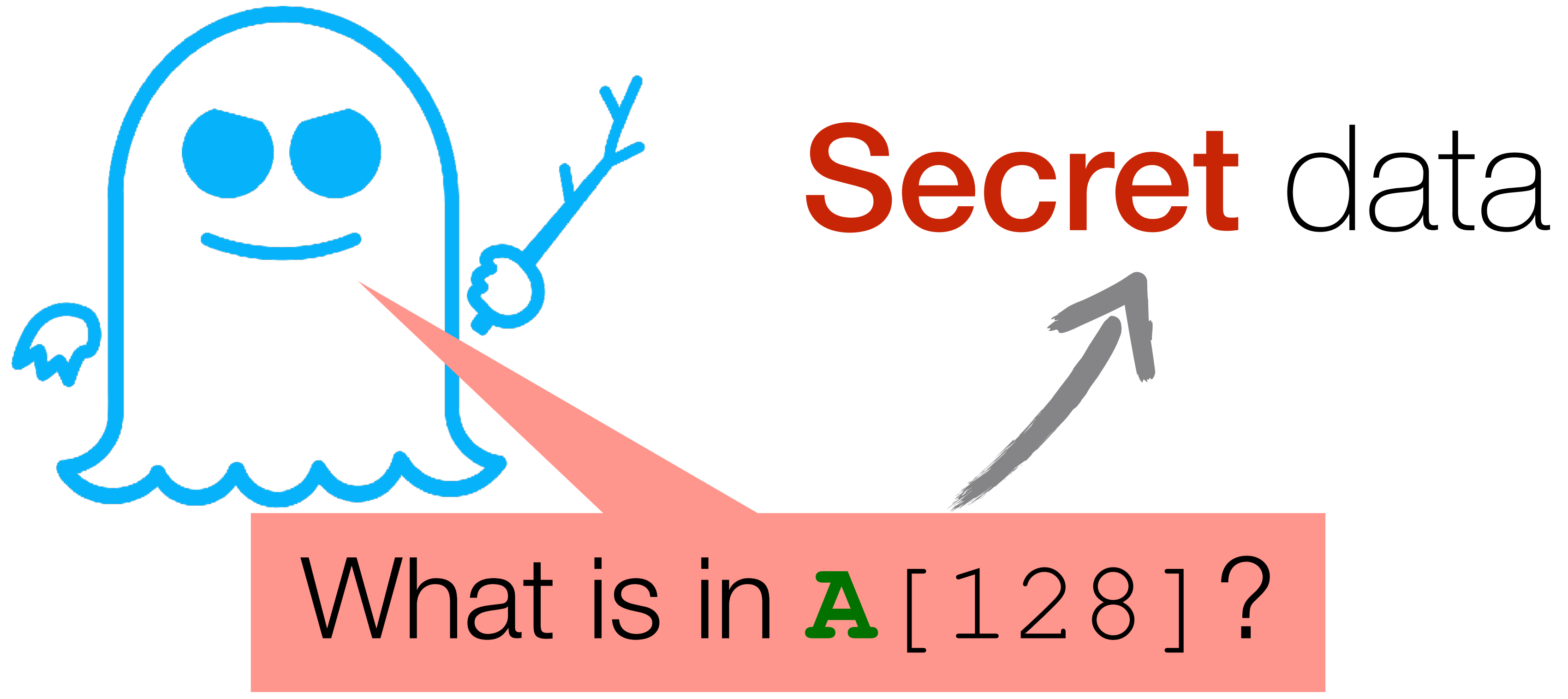

1) Train branch predictor

2) Prepare cache

3) Run with x = 128

Spectre v1

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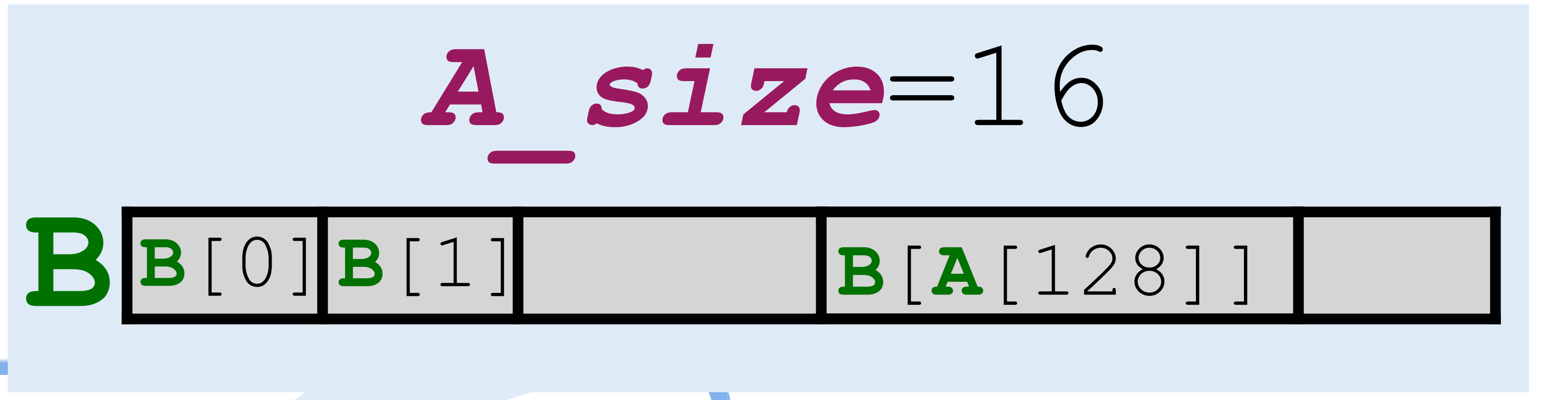

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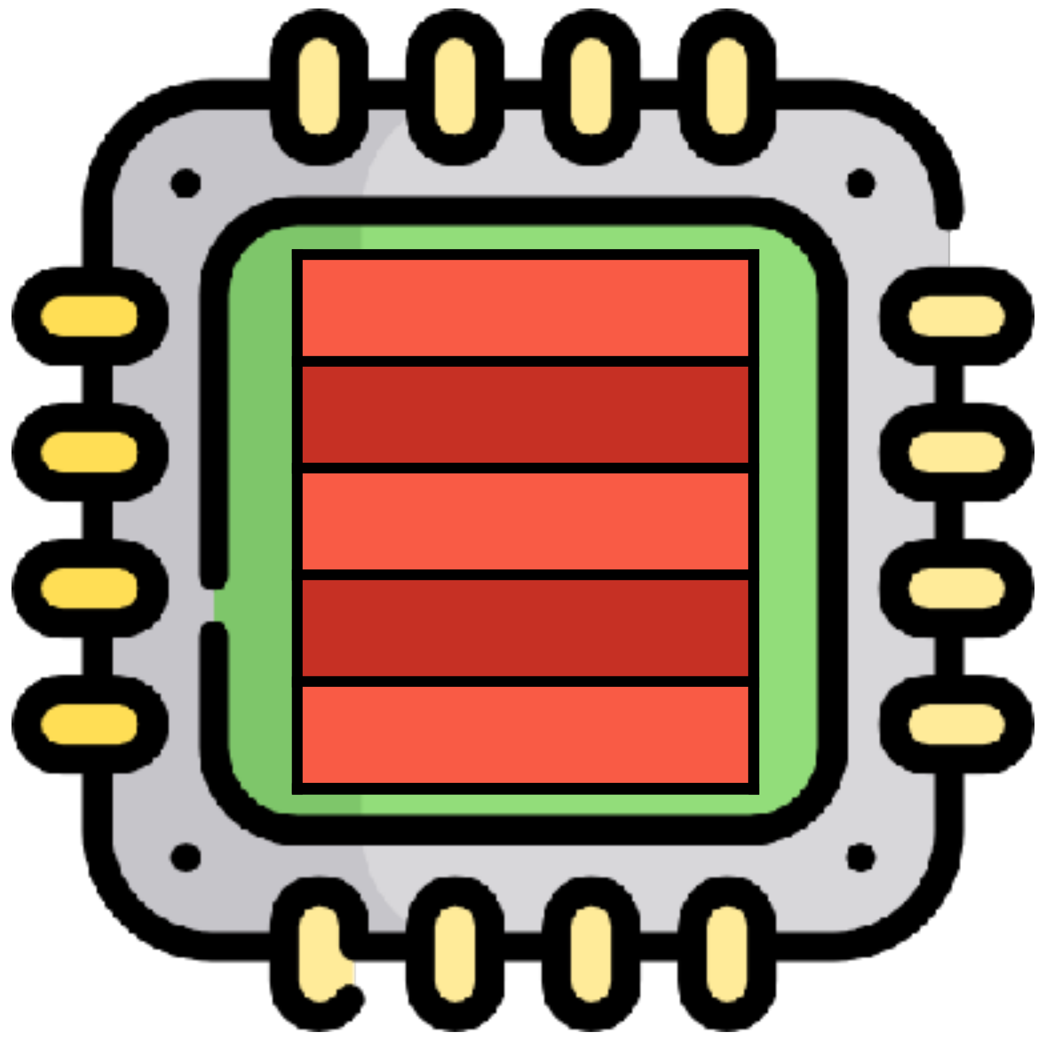

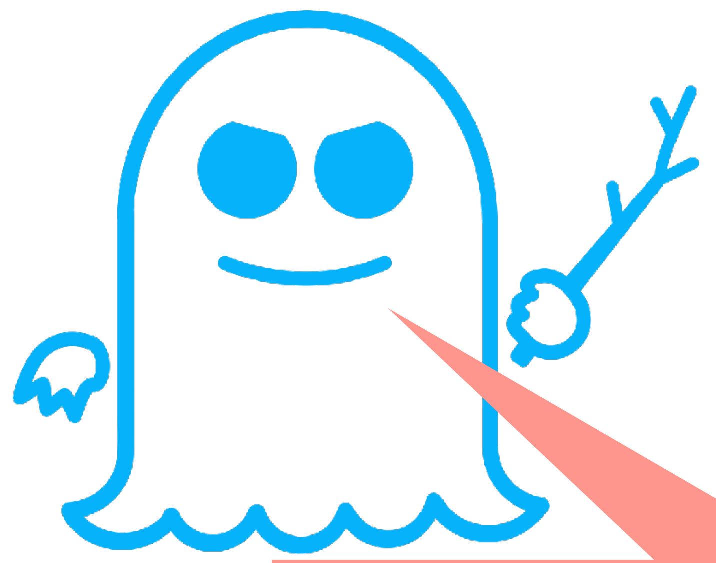

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Spectre v1

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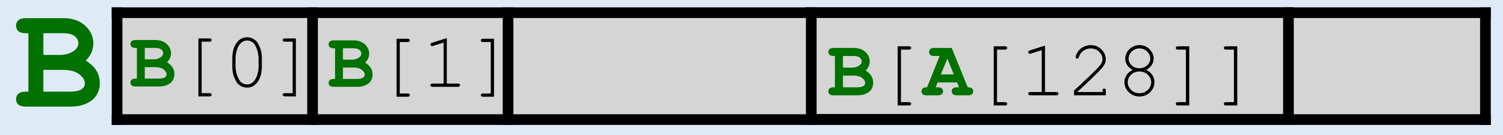

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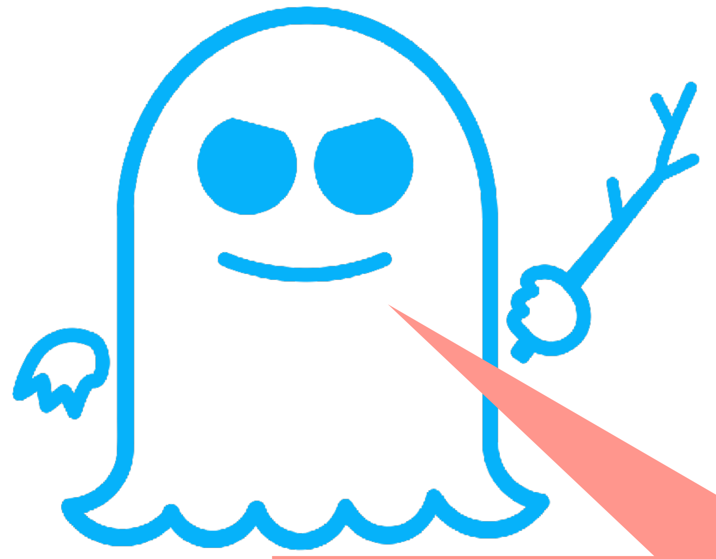

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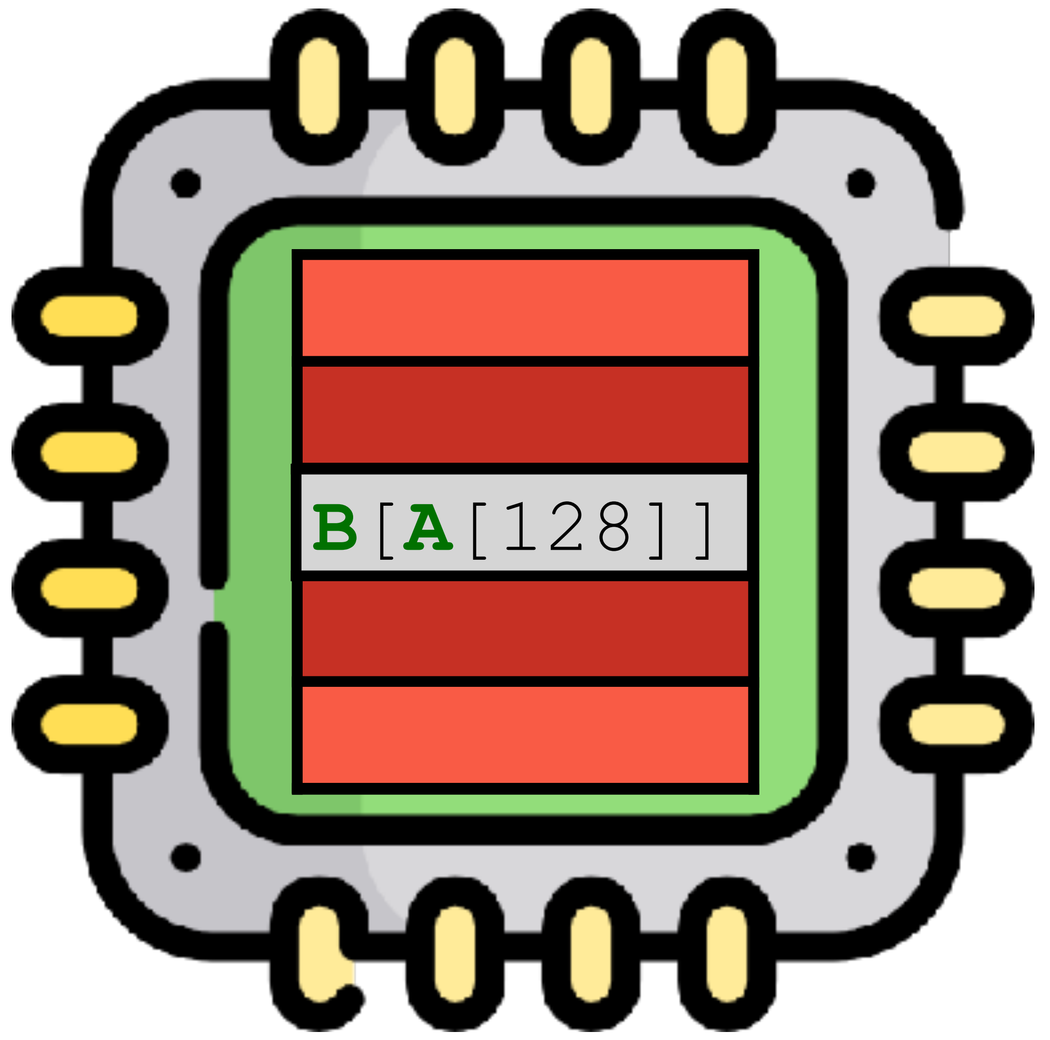

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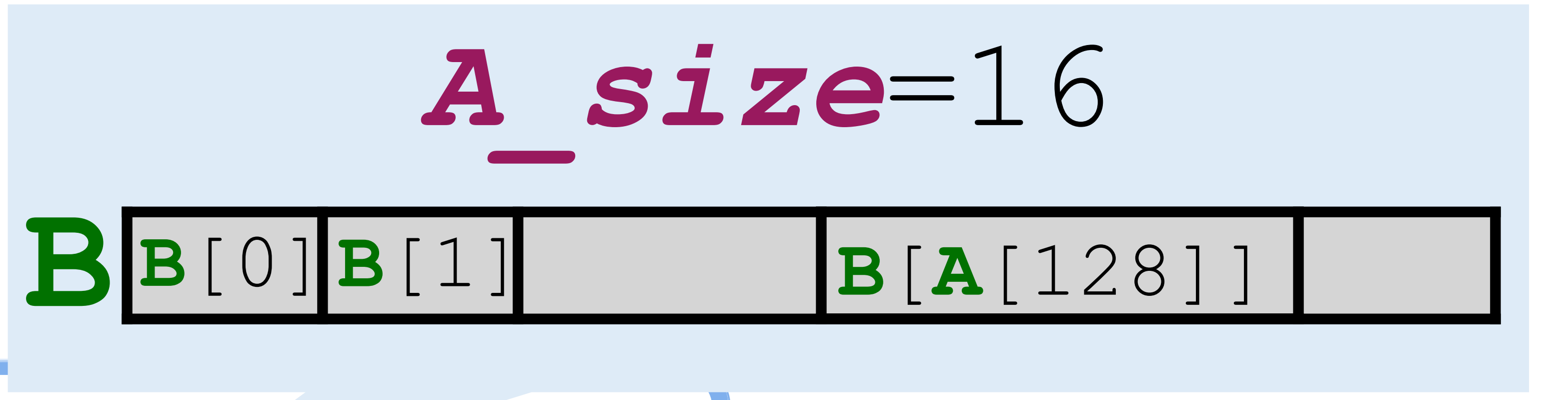

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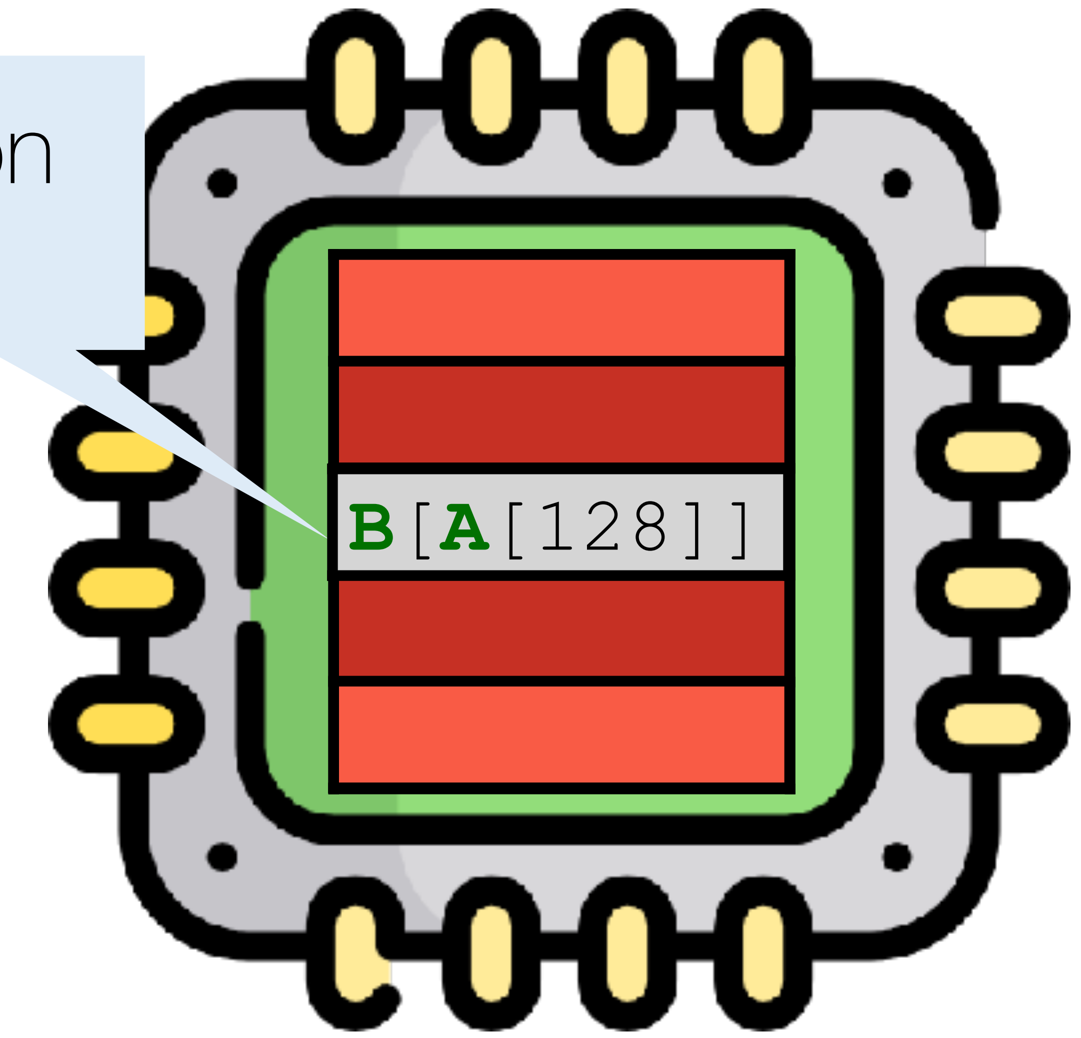
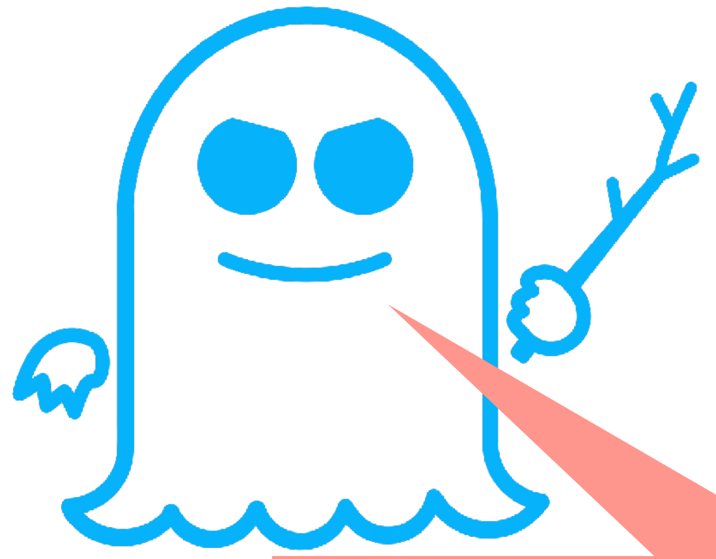
3) Run with x = 128

Depends on A[128]



Spectre v1



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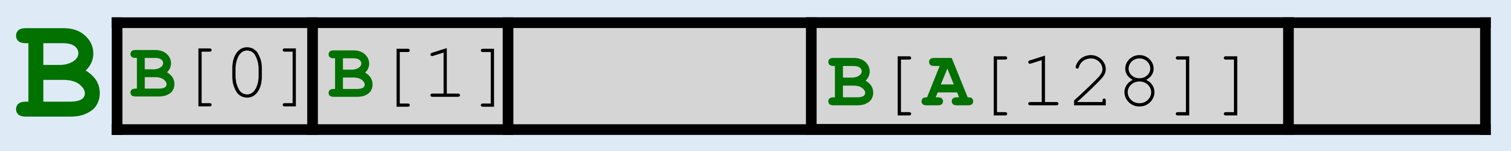

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1) **Train branch predictor**

2) **Prepare cache**

3) **Run with x = 128**

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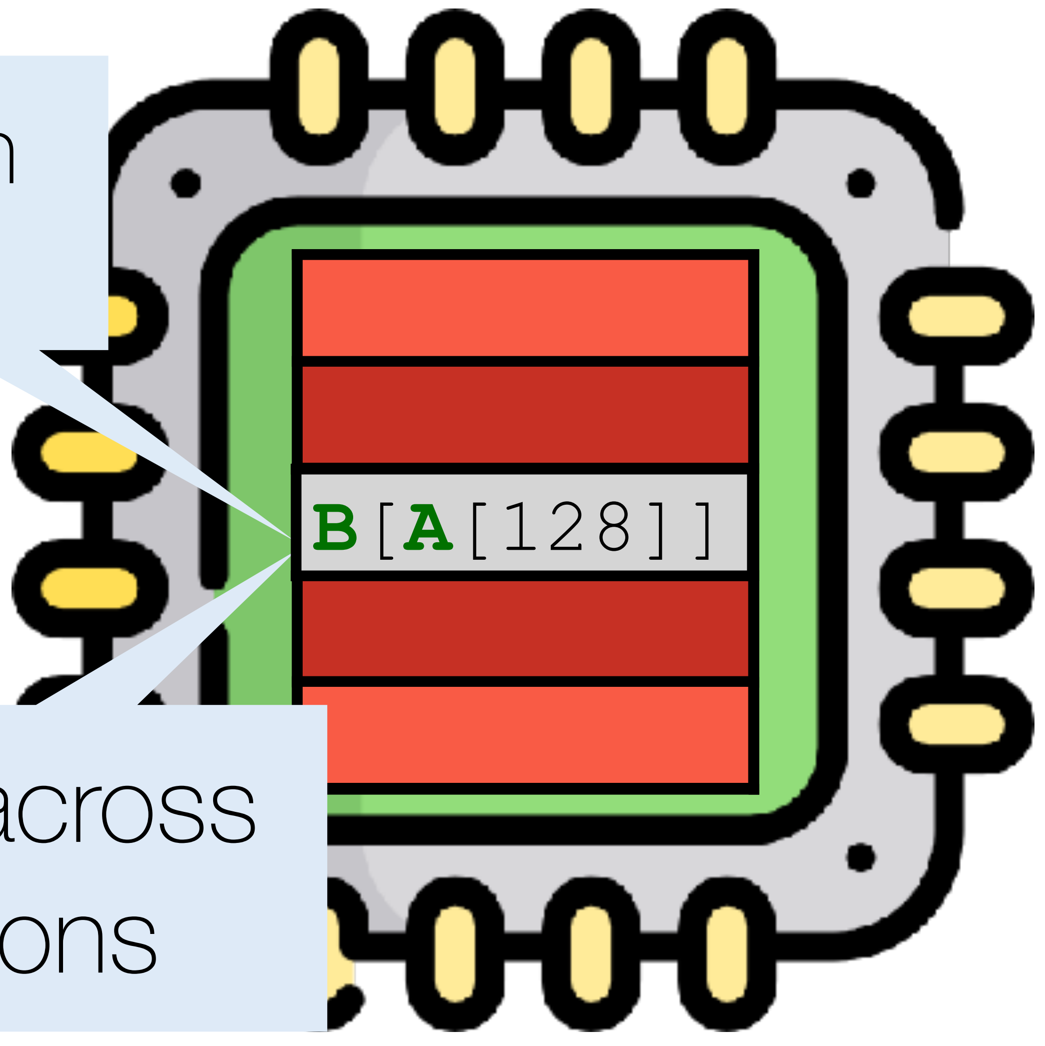

Persistent across speculations

Spectre v1

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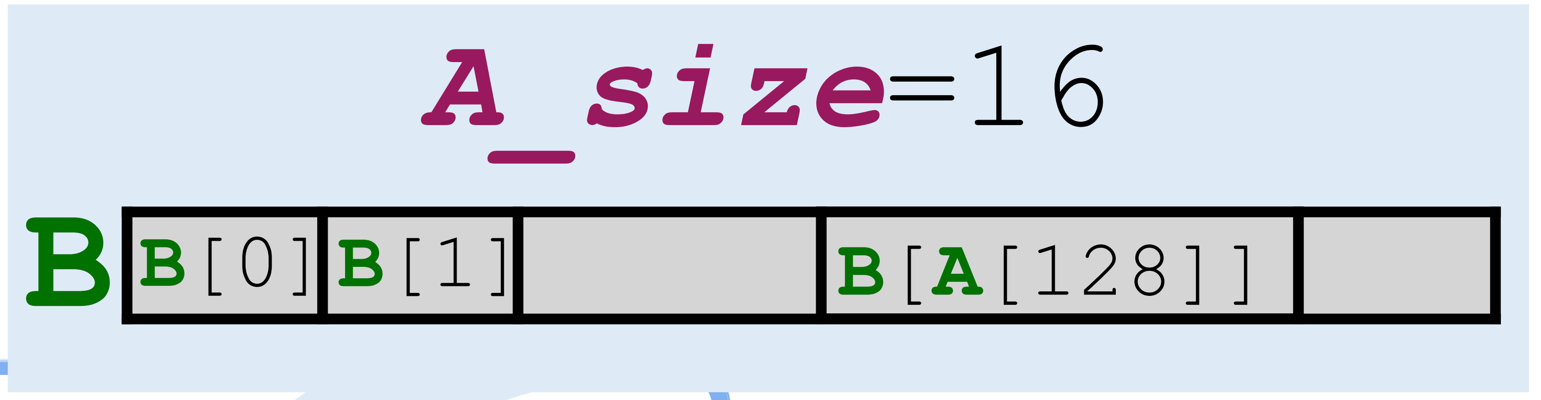
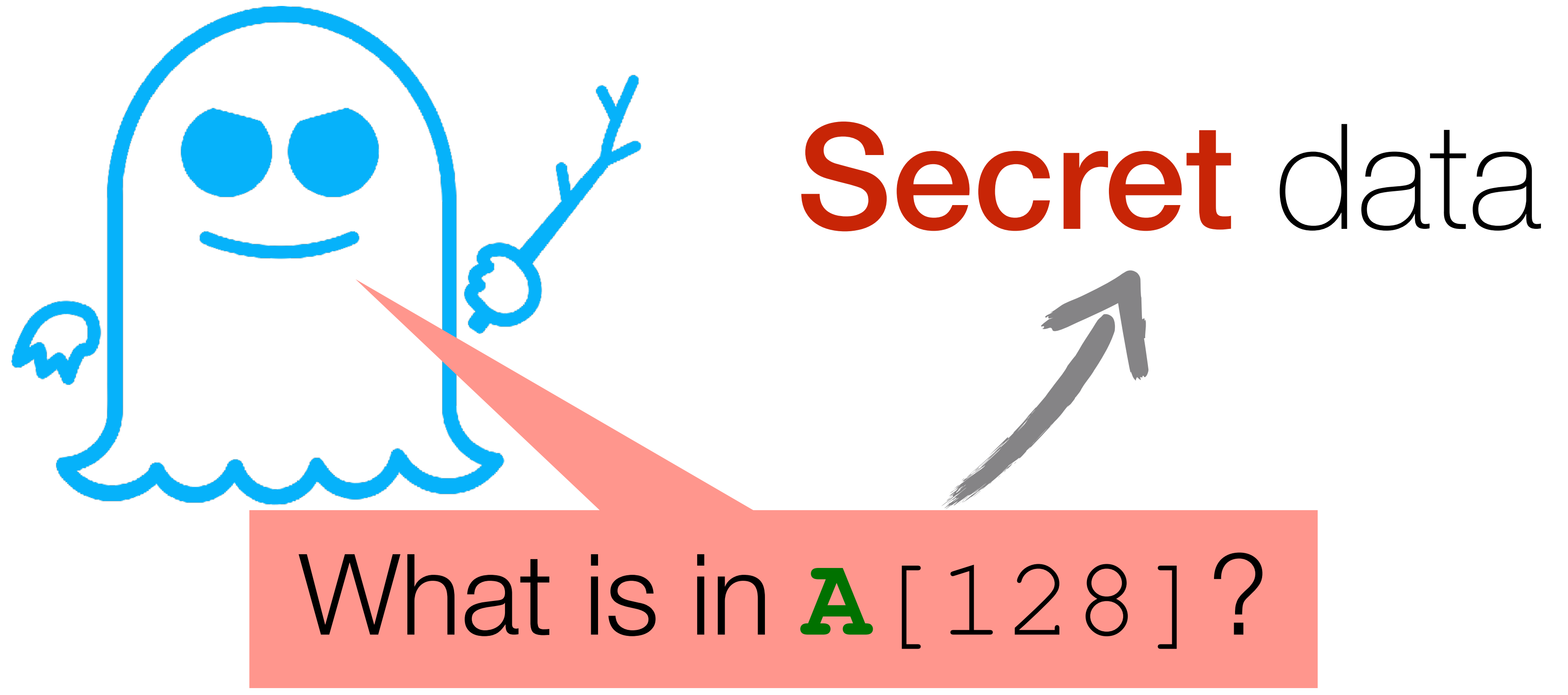
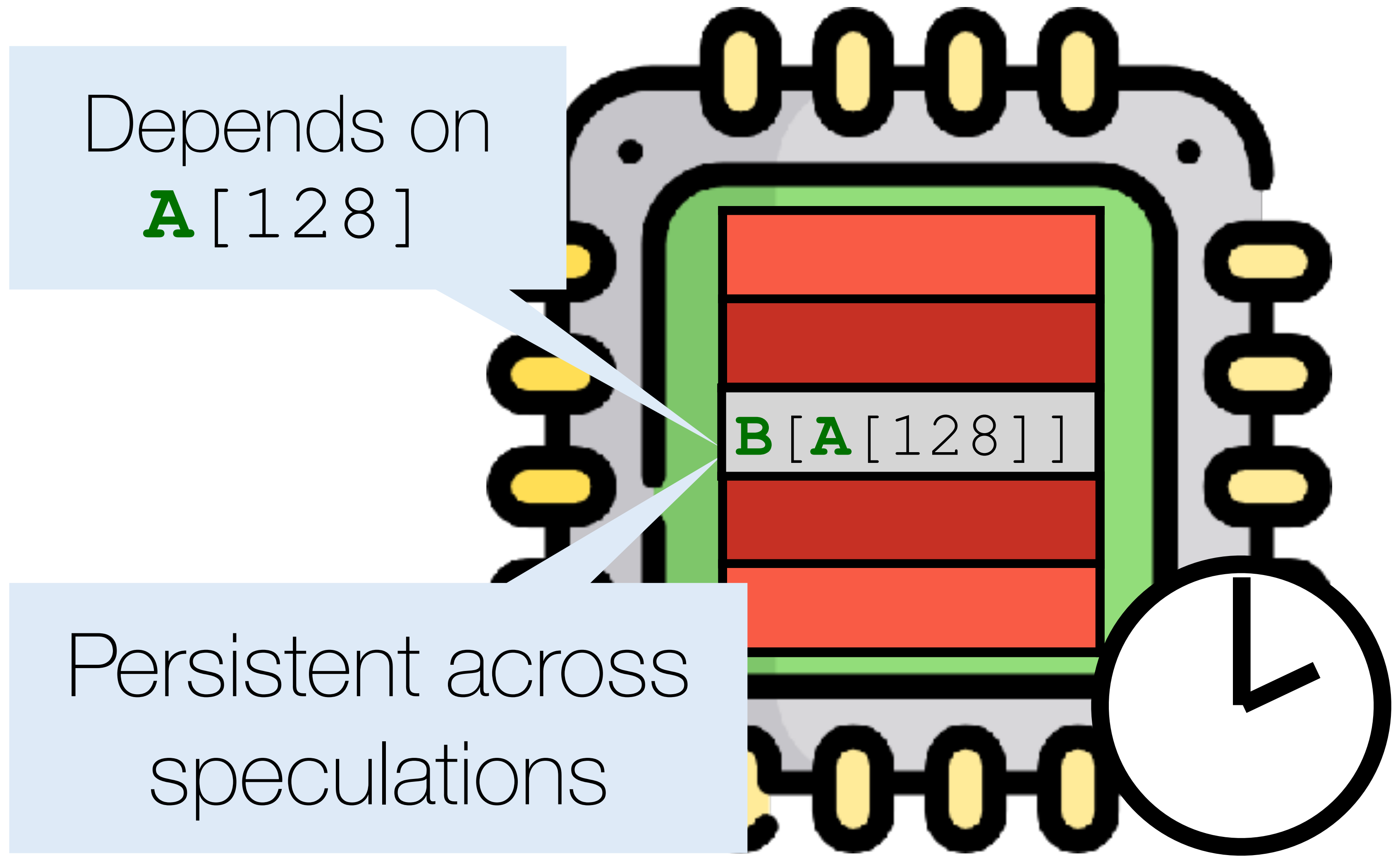






1) Train branch predictor

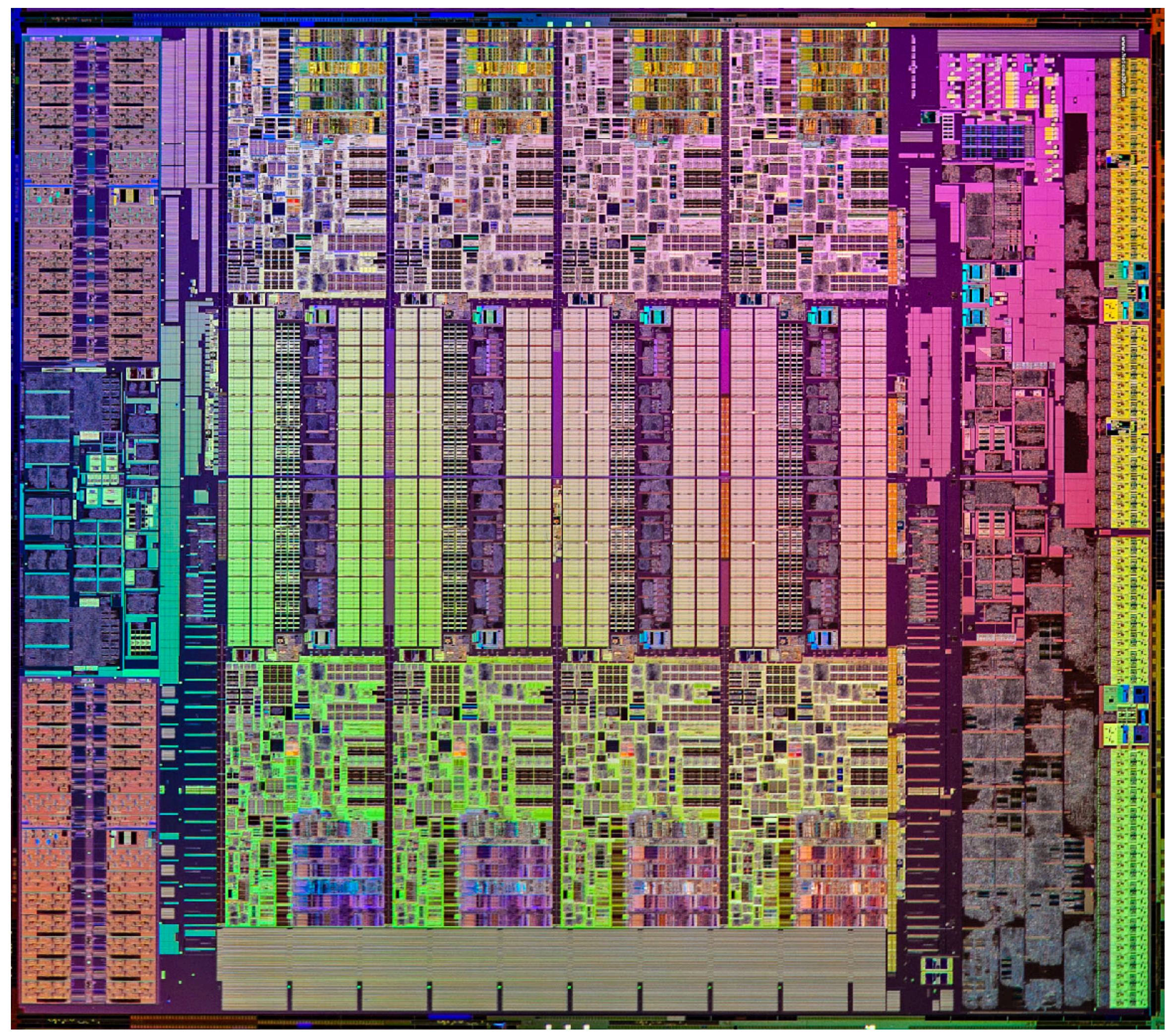
2) Prepare cache

3) Run with x = 128

4) Extract from cache

Outline

Speculative leaks at program level



Guarnieri, Köpf, Morales, Reineke, Sánchez — Spectector: Principled detection for speculative leaks — IEEE S&P 2020 — https://arxiv.org/abs/1812.08639

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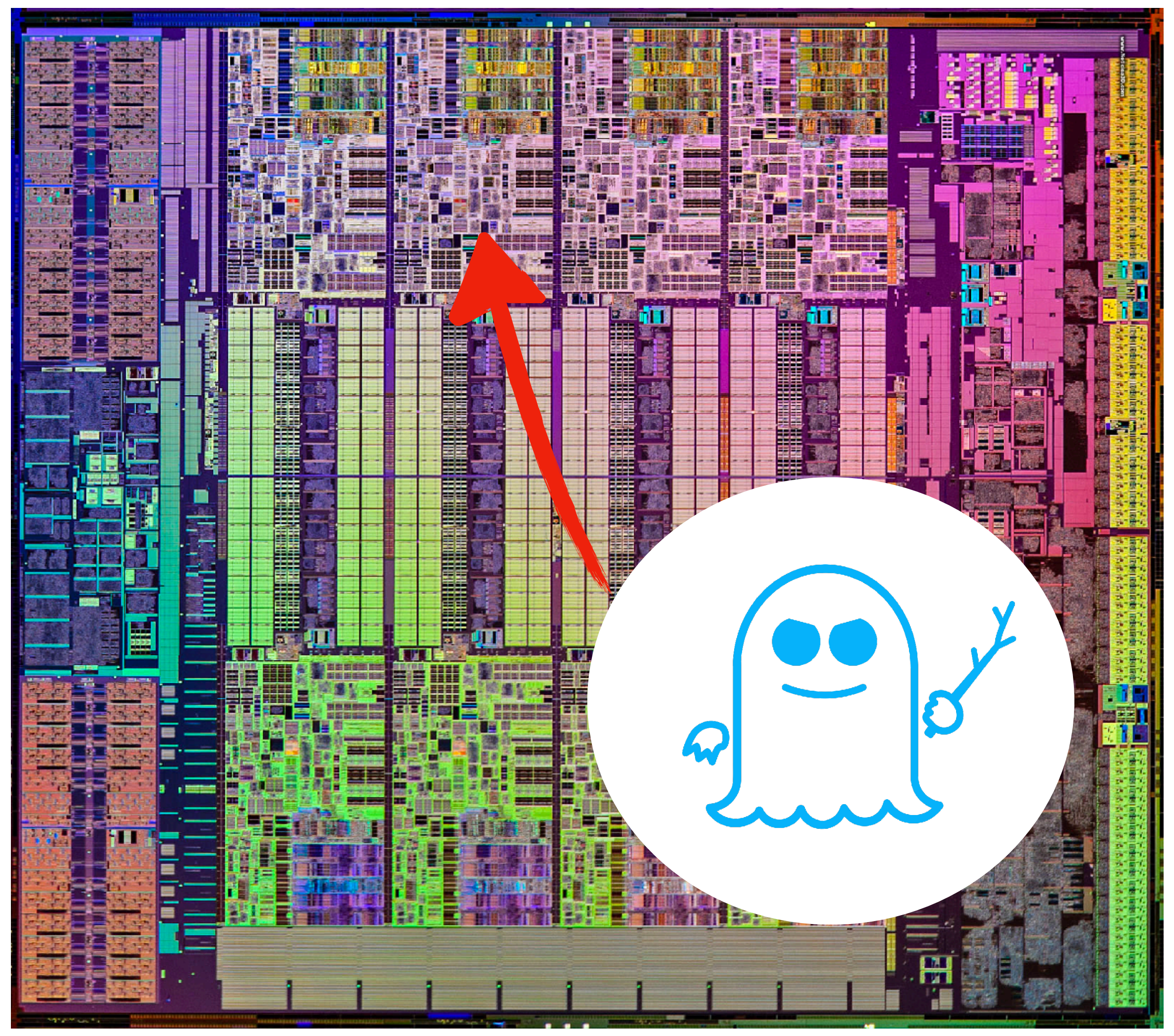

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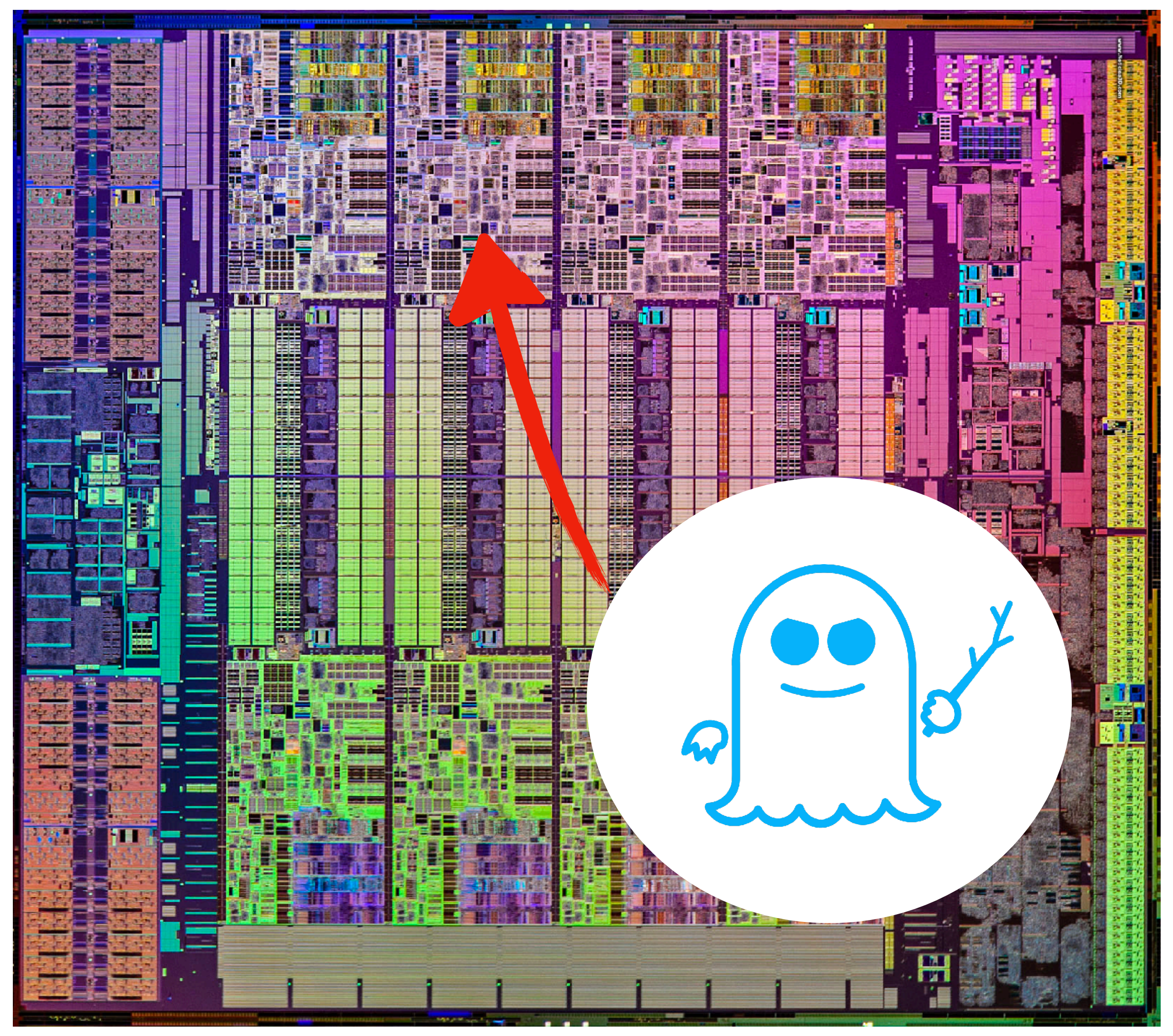
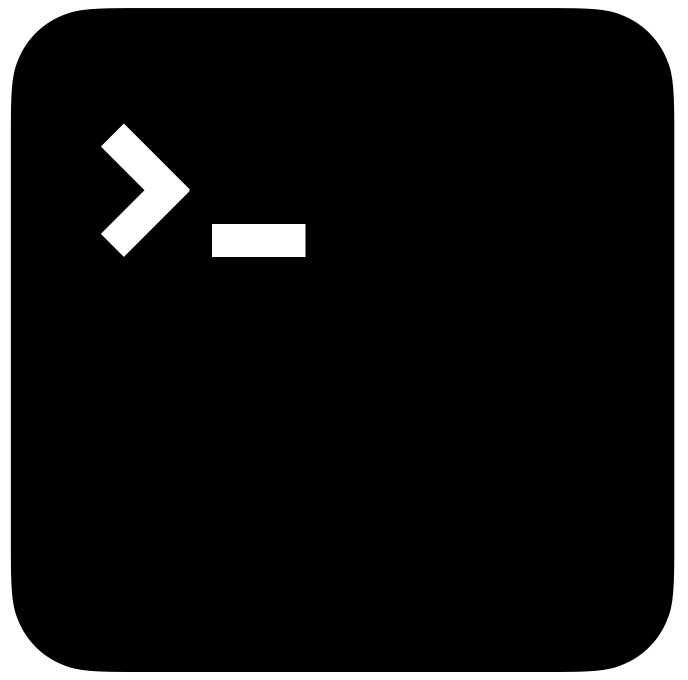
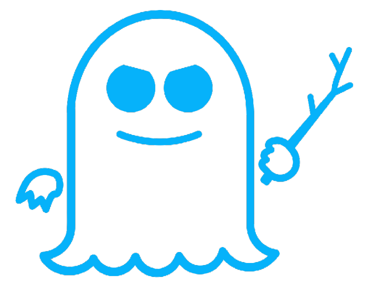


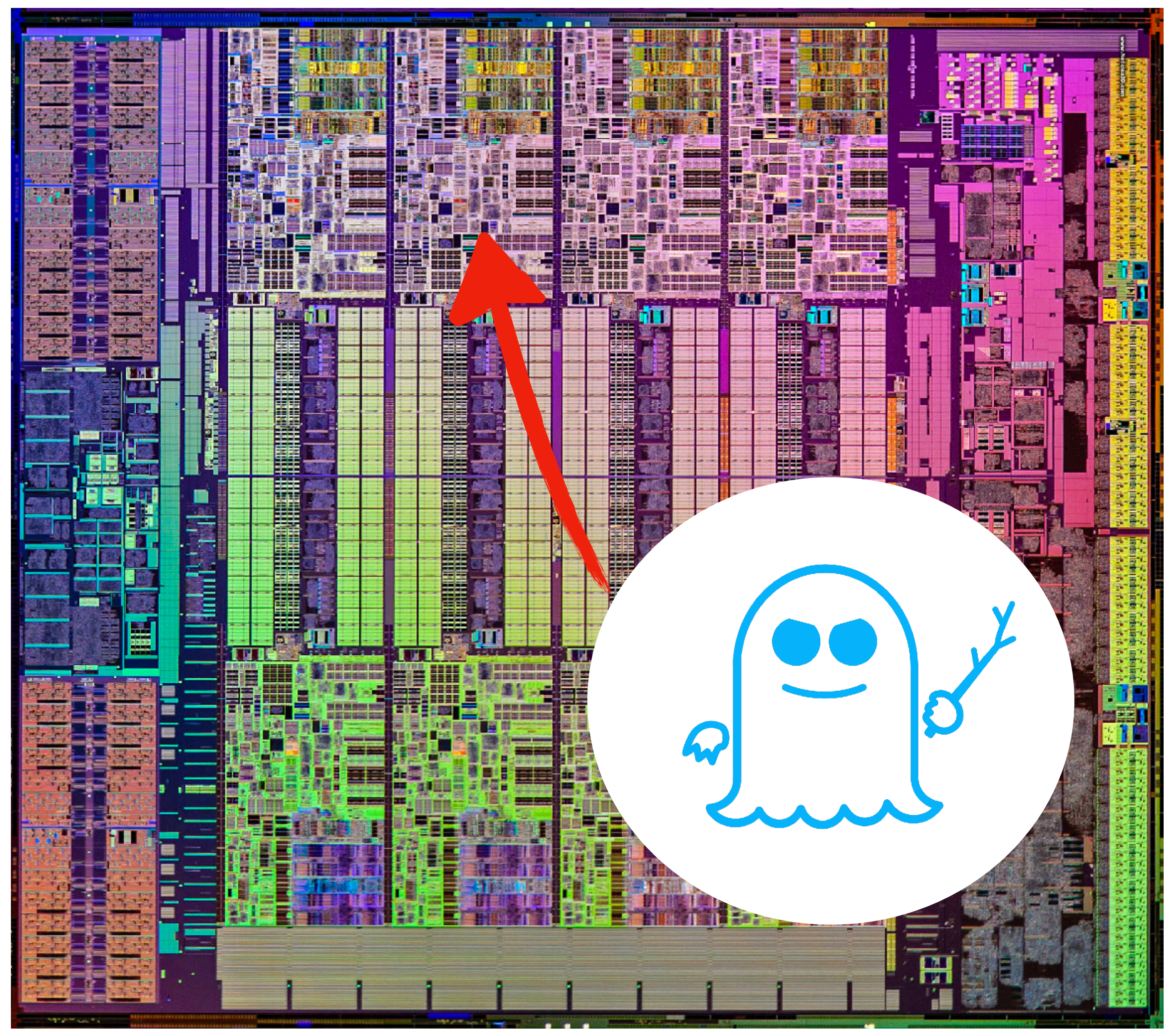


+



Speculative semantics

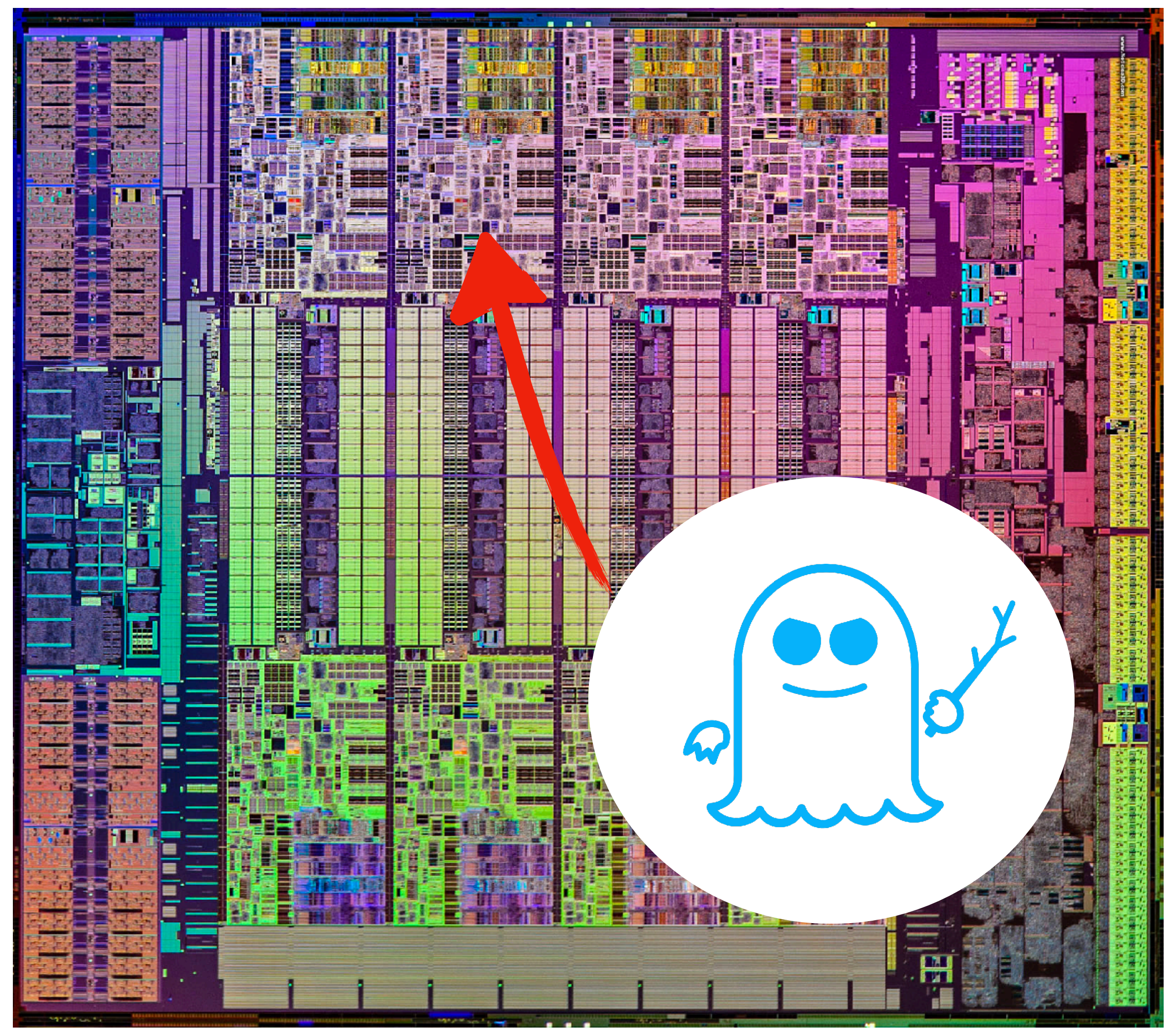
Speculative leaks at program level

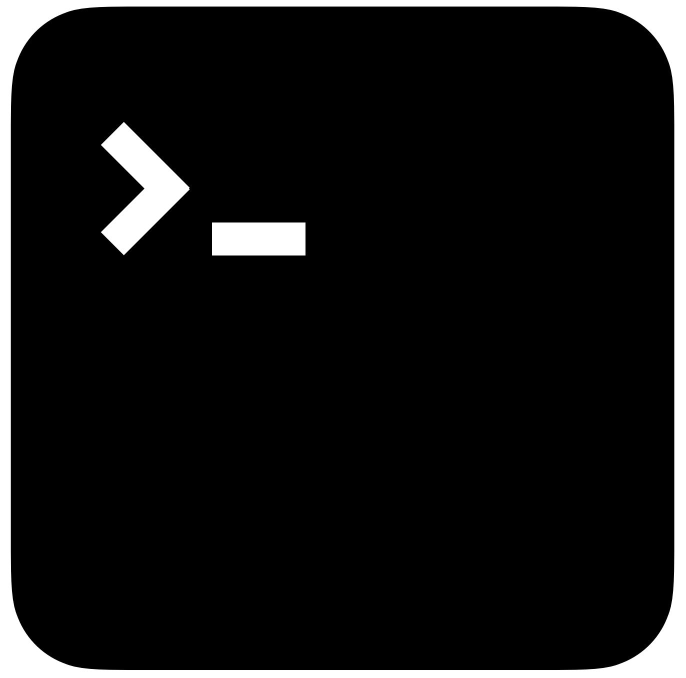


+ Speculative semantics

Execution mode + *Observer mode*

Speculative leaks at program level





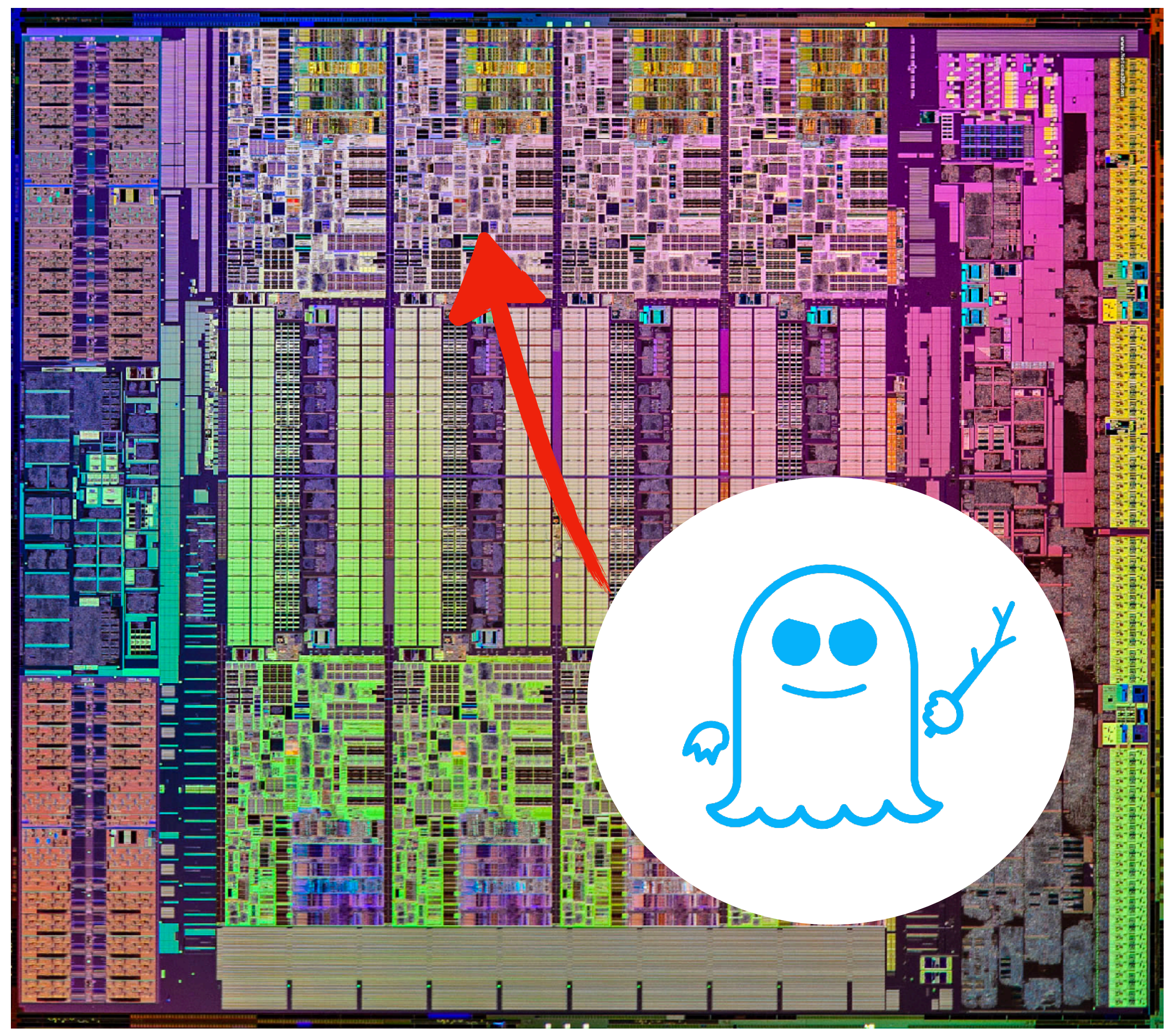
+

Speculative semantics

Execution mode **+** ***Observer mode***

Models how instructions are executed

Speculative leaks at program level



+ Speculative semantics

Execution mode + *Observer mode*

Models how instructions are executed

Capture attacker's observational power

Modeling speculation

```
if (x < A_size)
    y = A[x]
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end
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Modeling speculation

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Save ***program state*** before executing ***branch*** instructions

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🟩 Non-speculative

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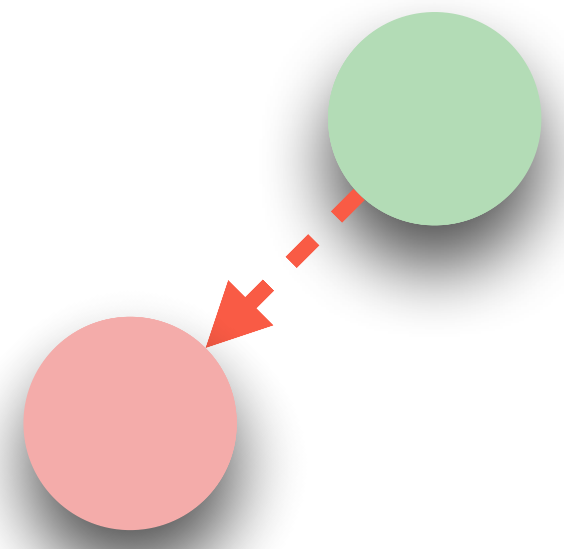

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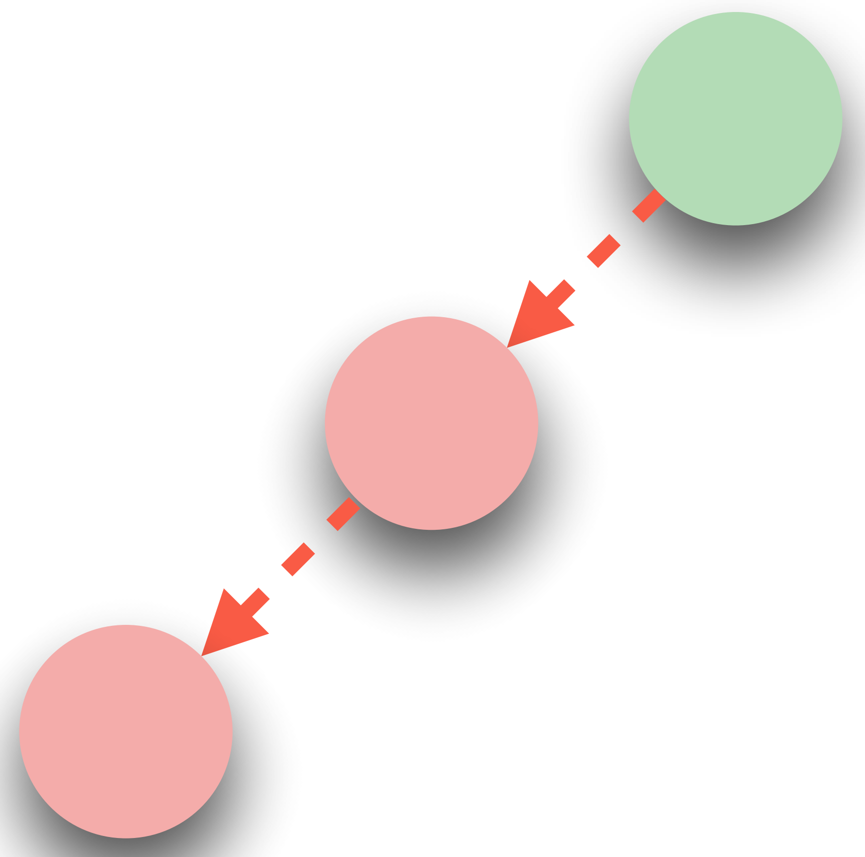

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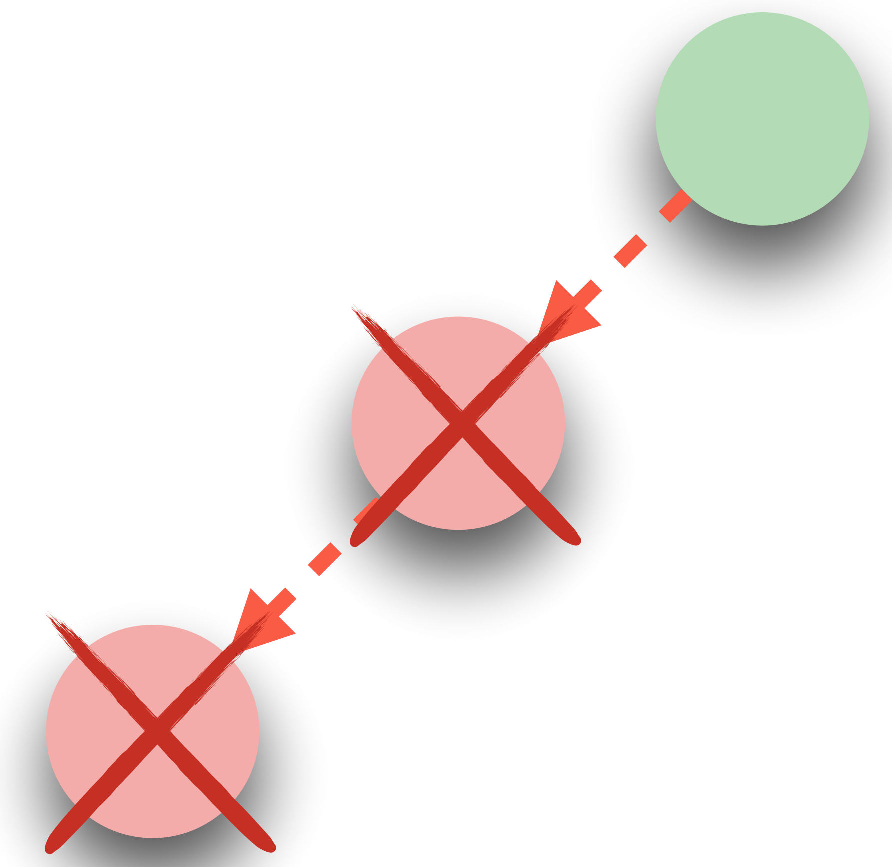

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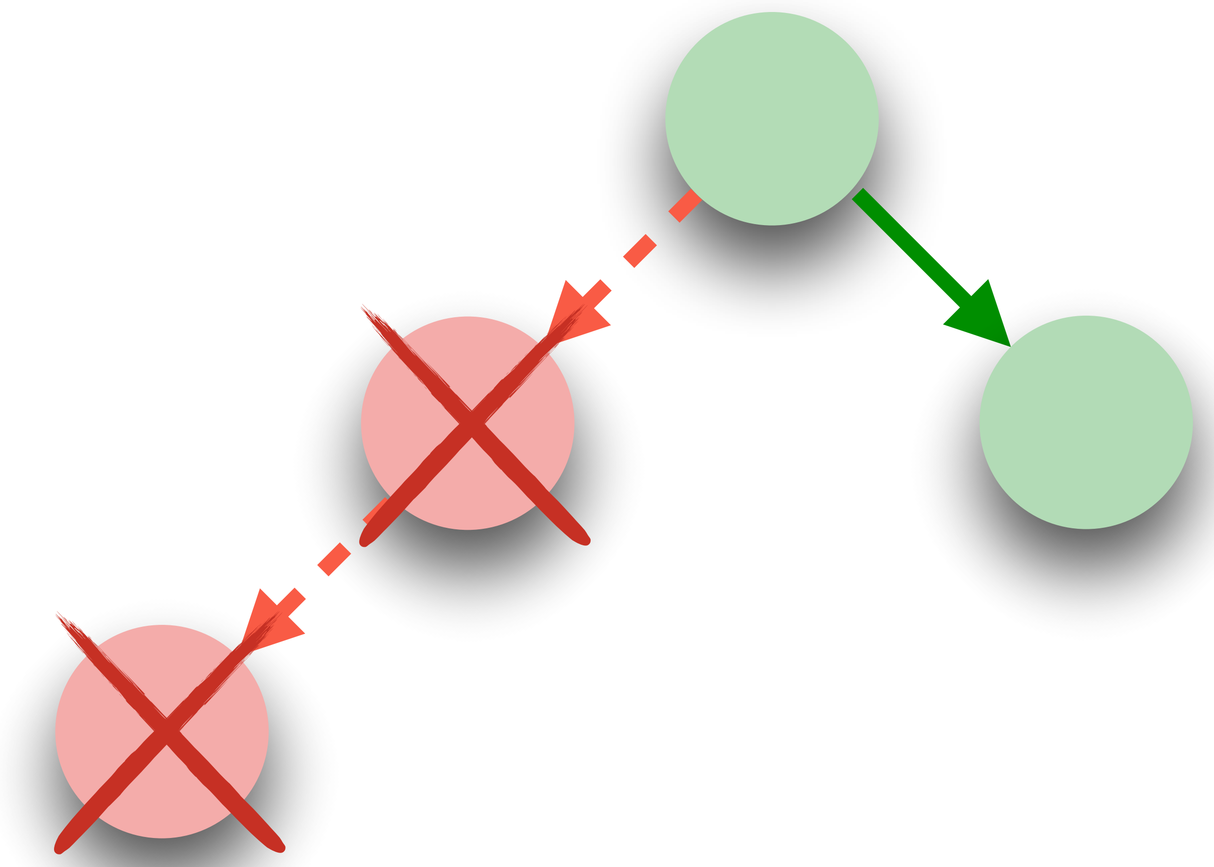

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Leakage into microarchitecture

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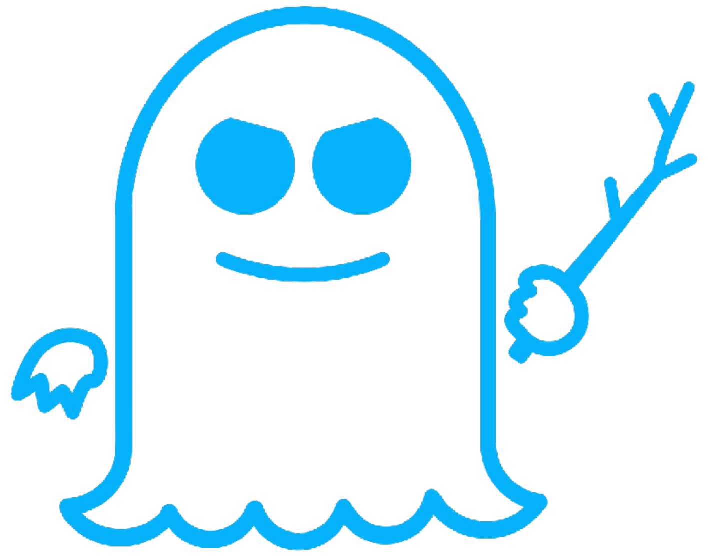

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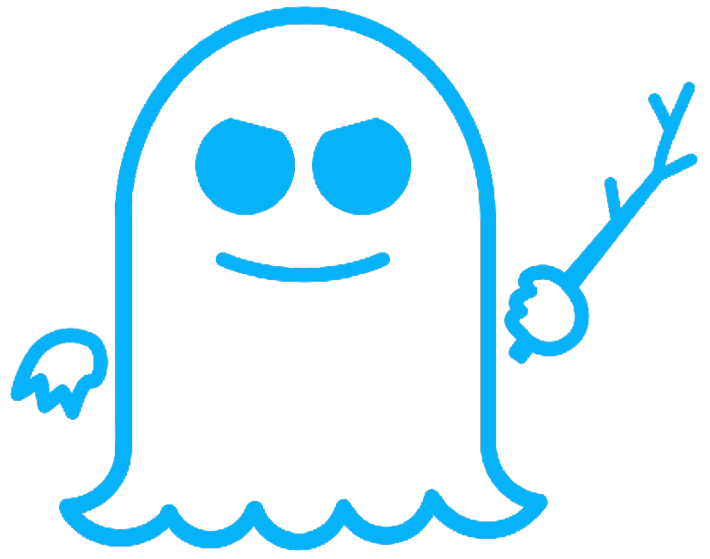

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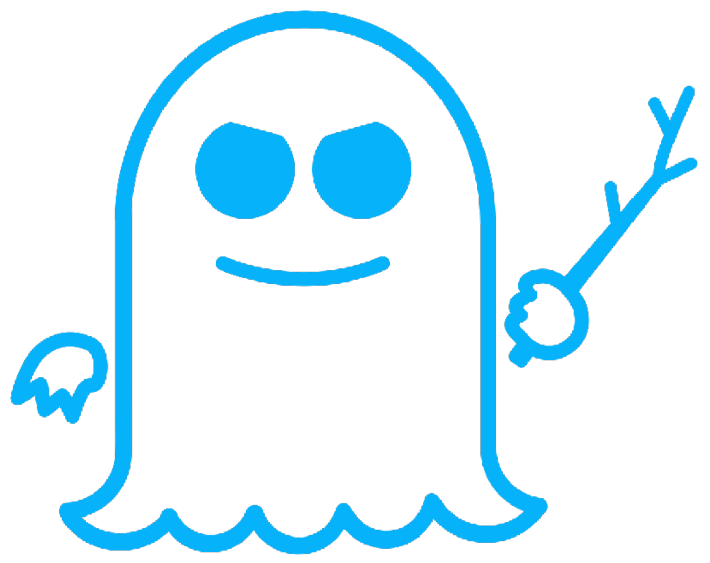

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Inspired by "constant-time" requirements

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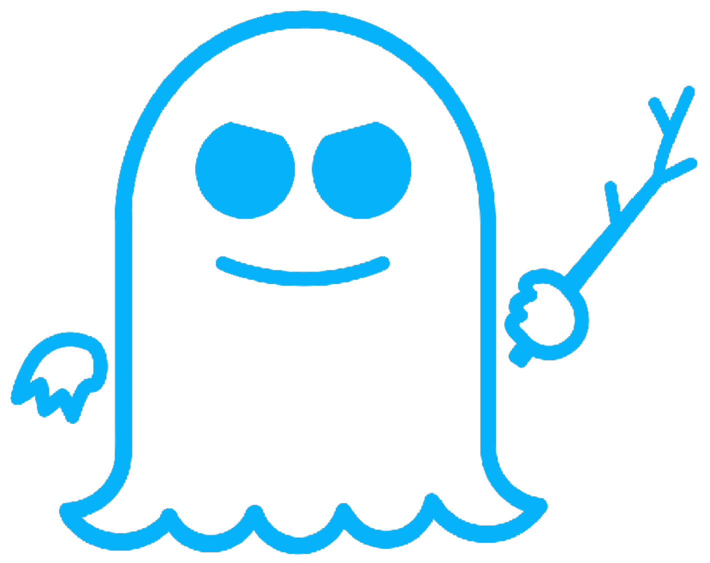

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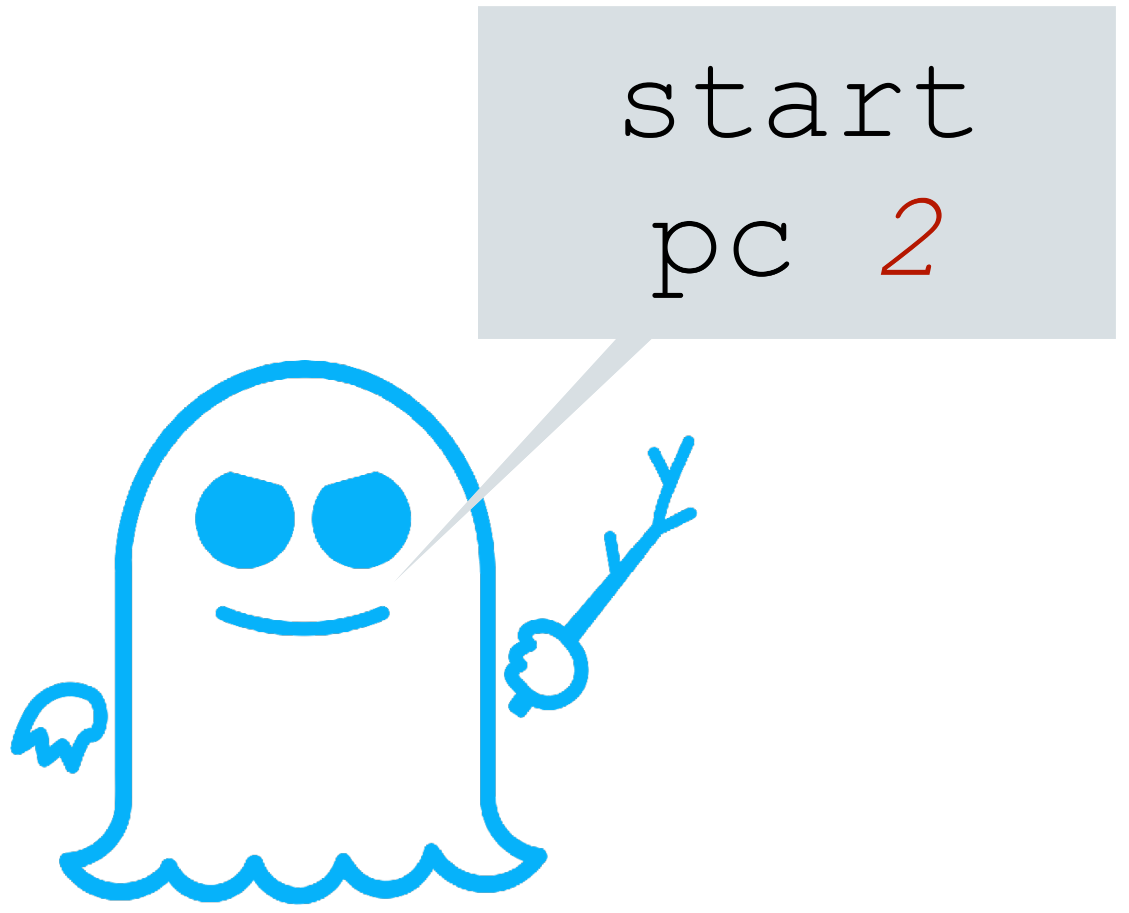

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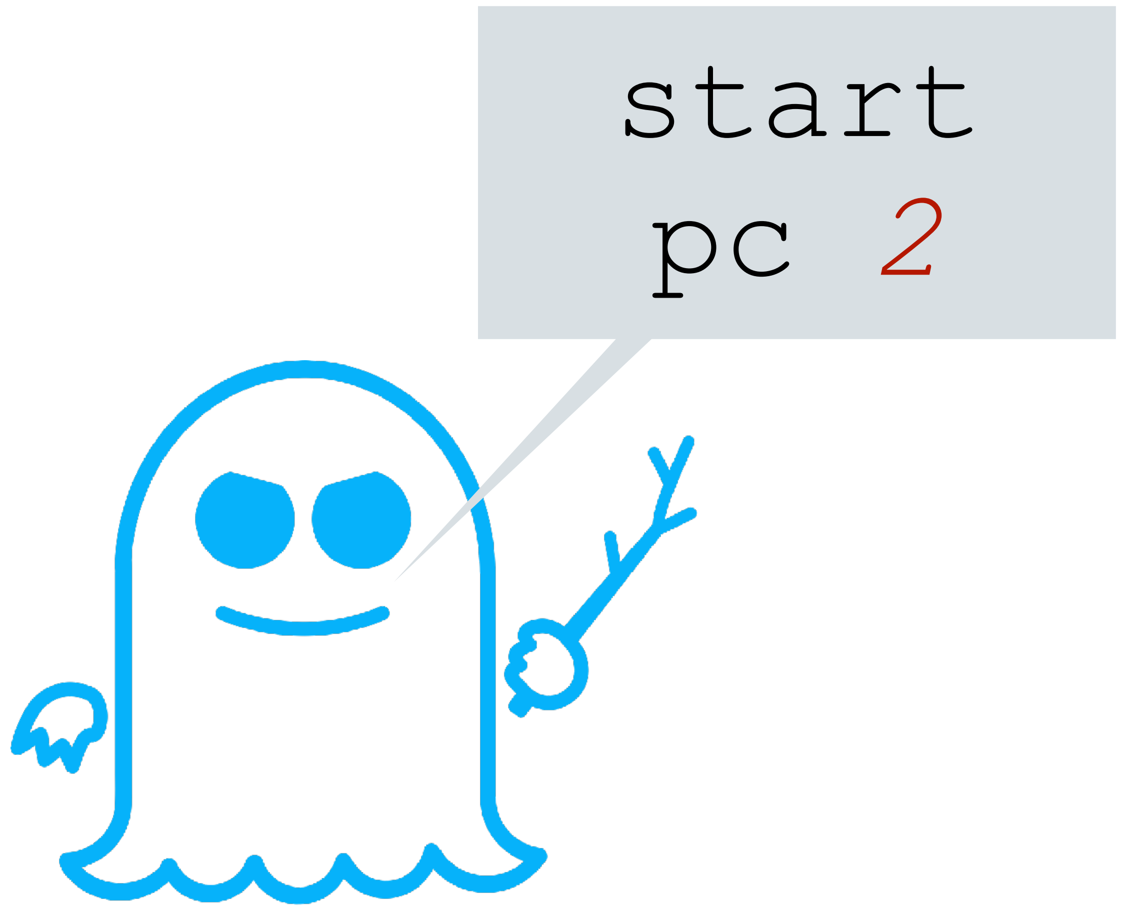

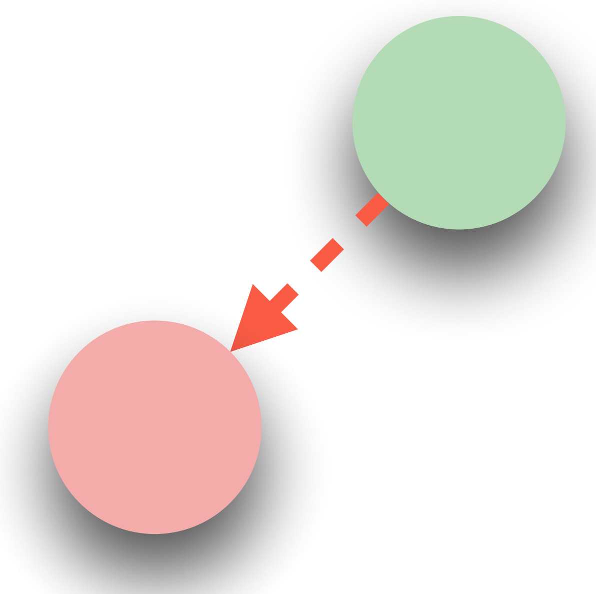

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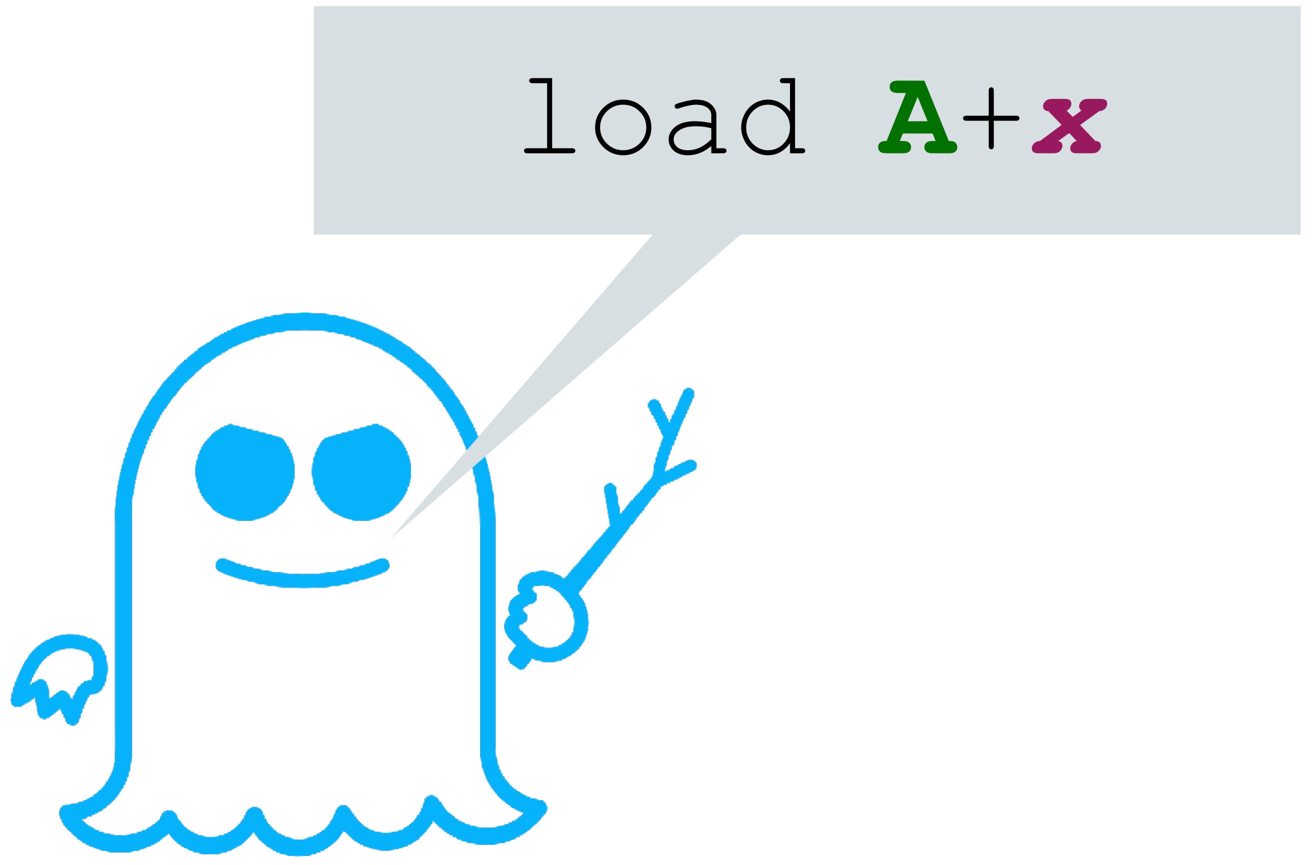

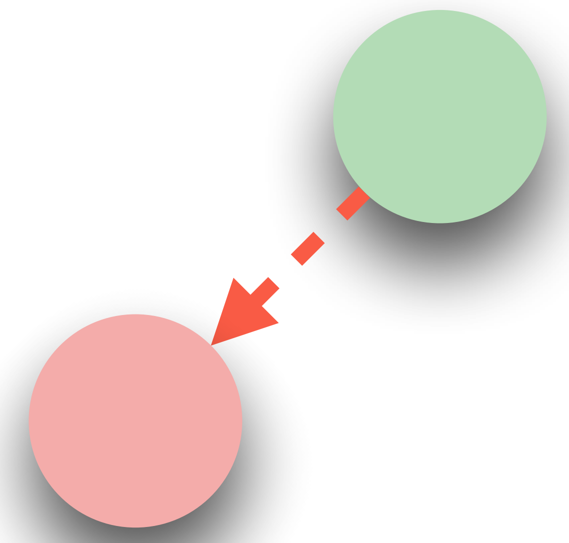

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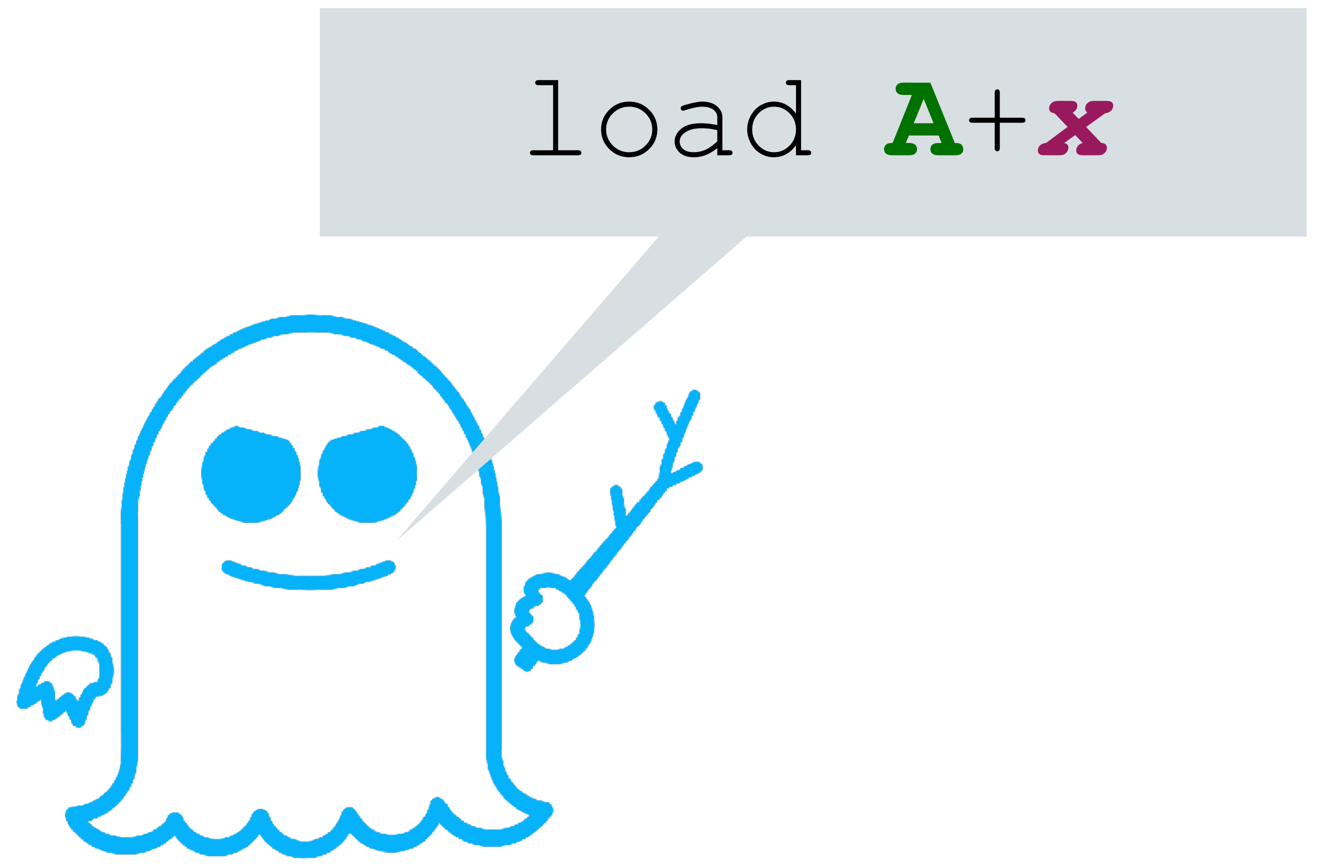

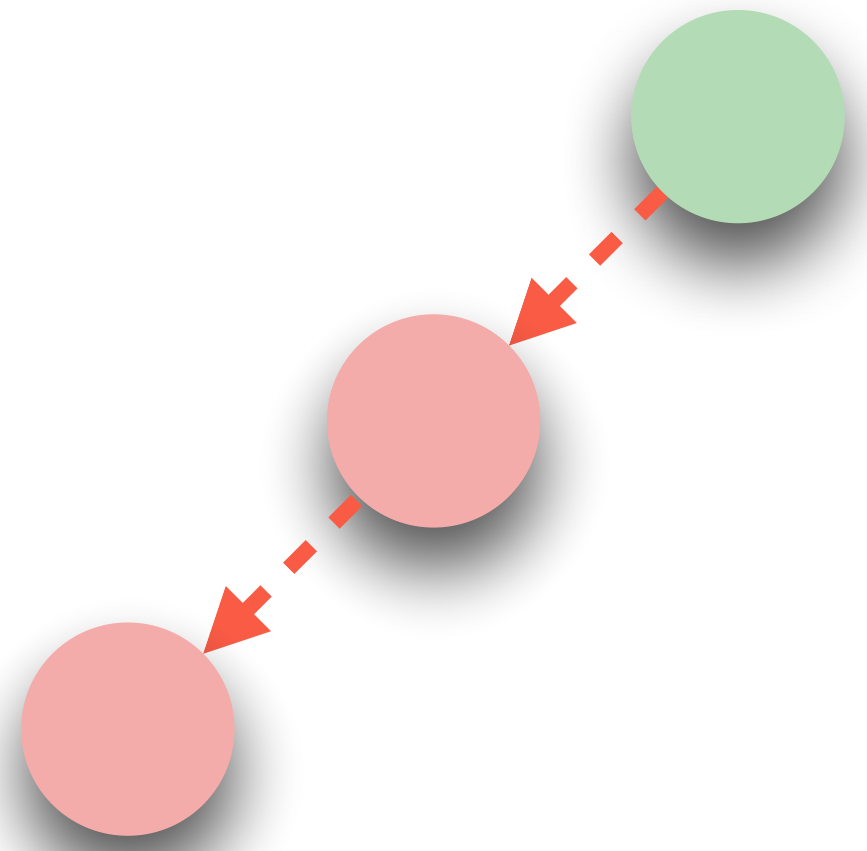

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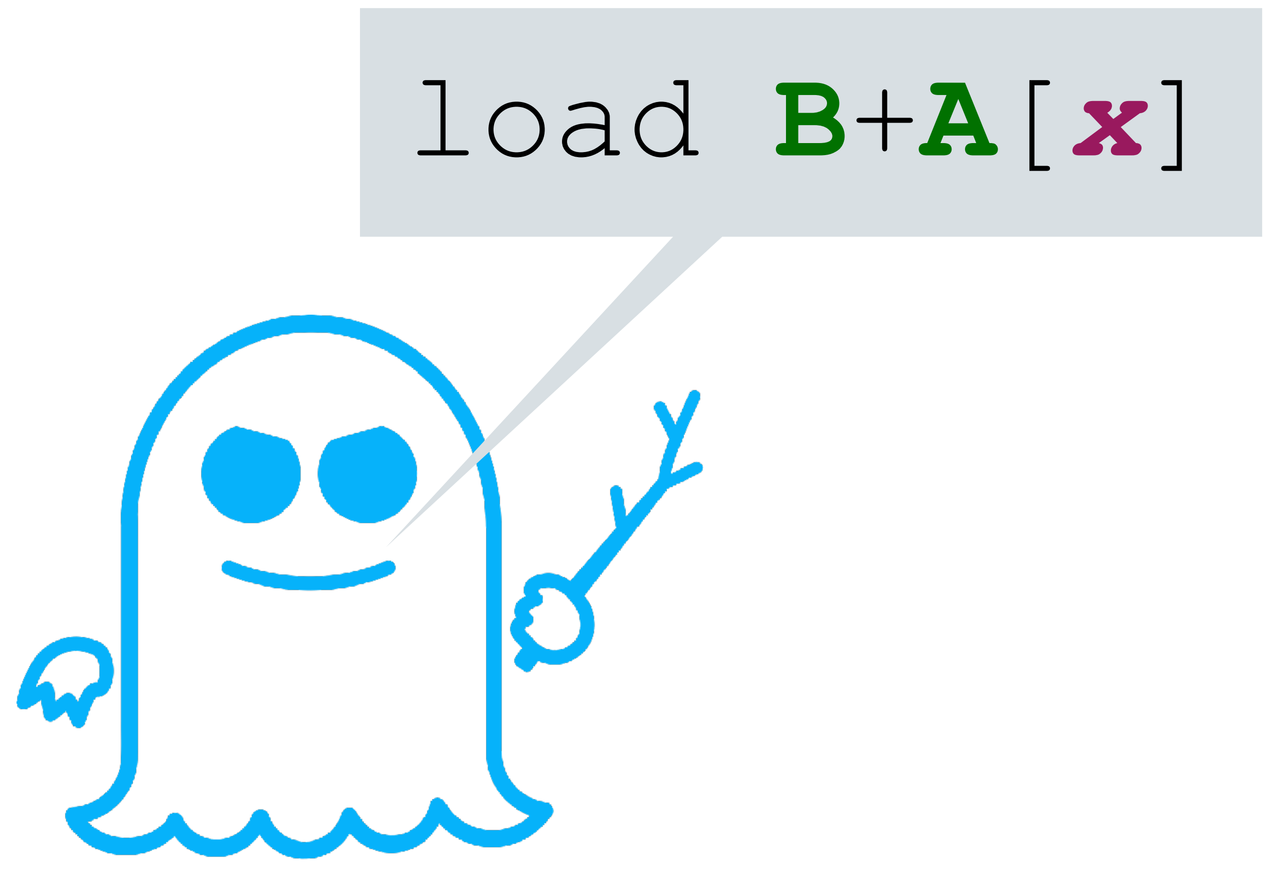

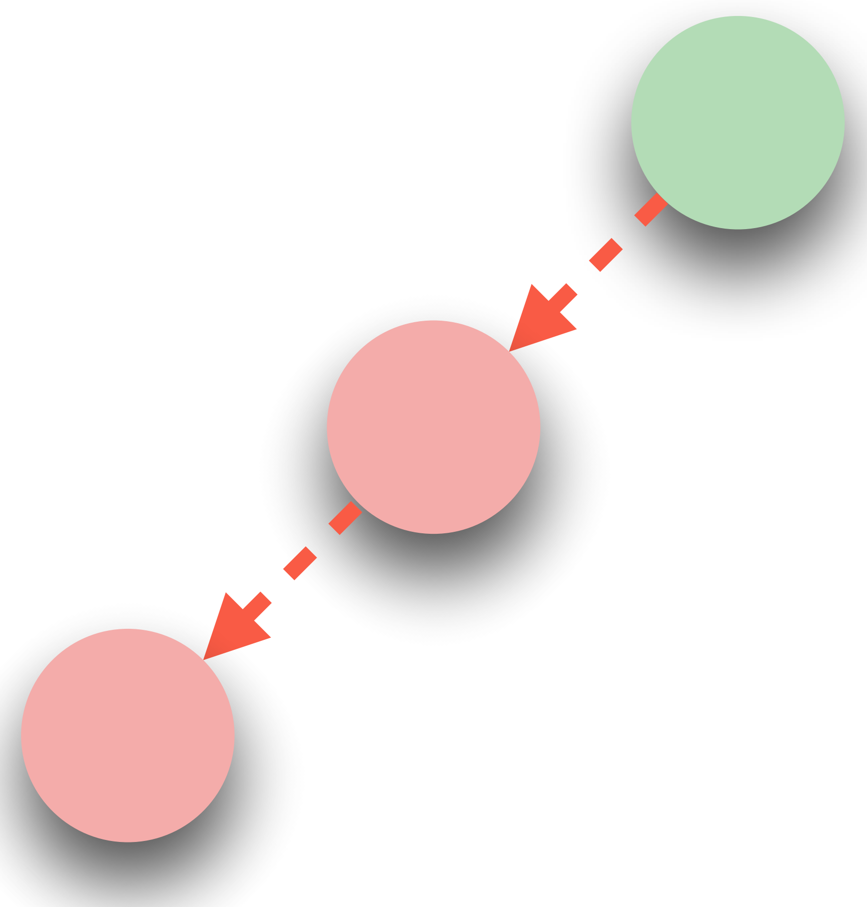

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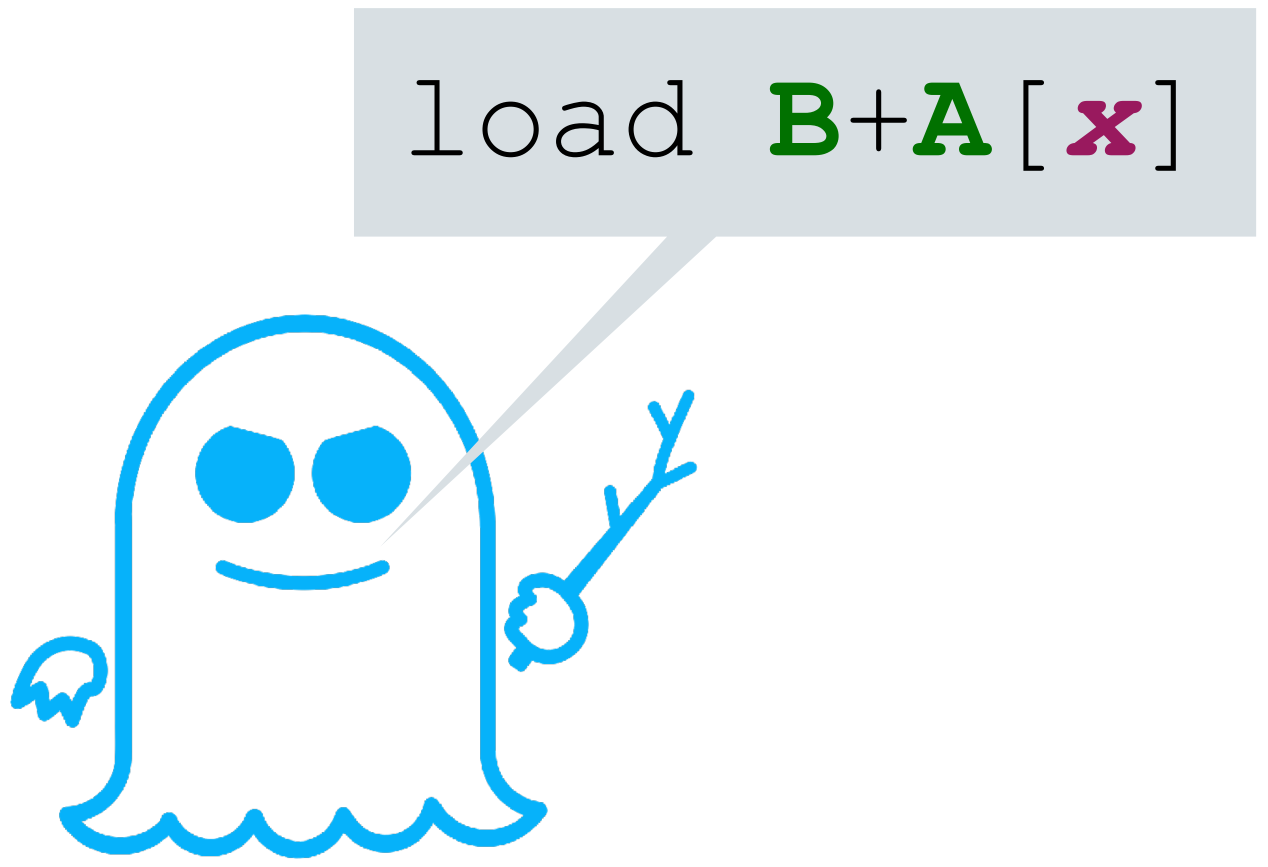

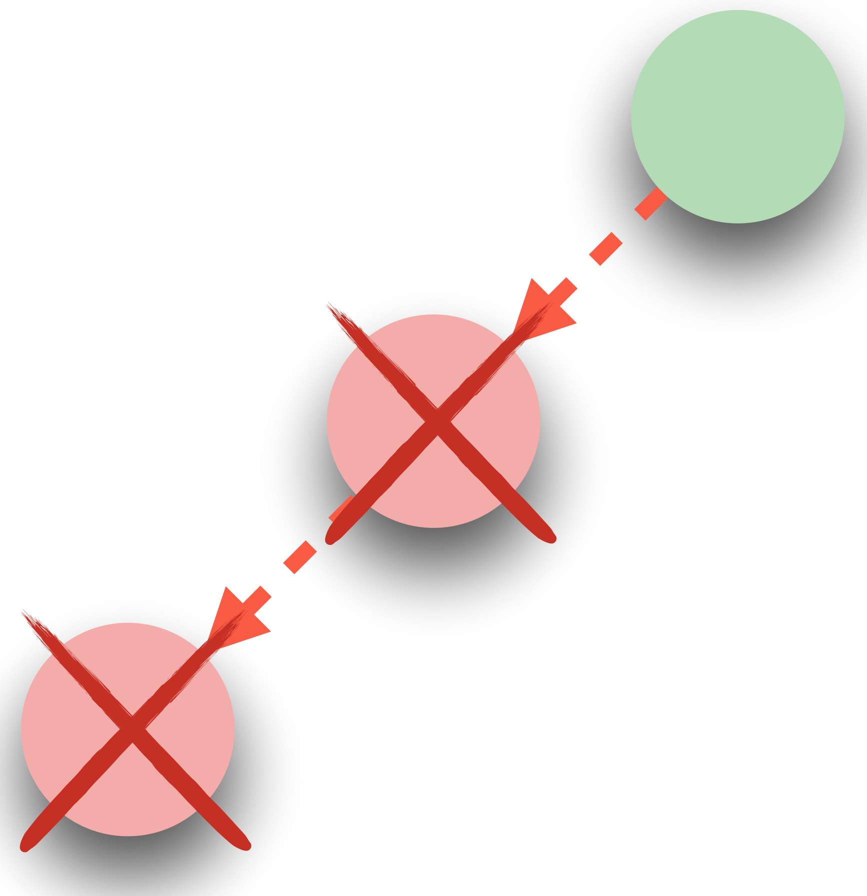

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4.  end
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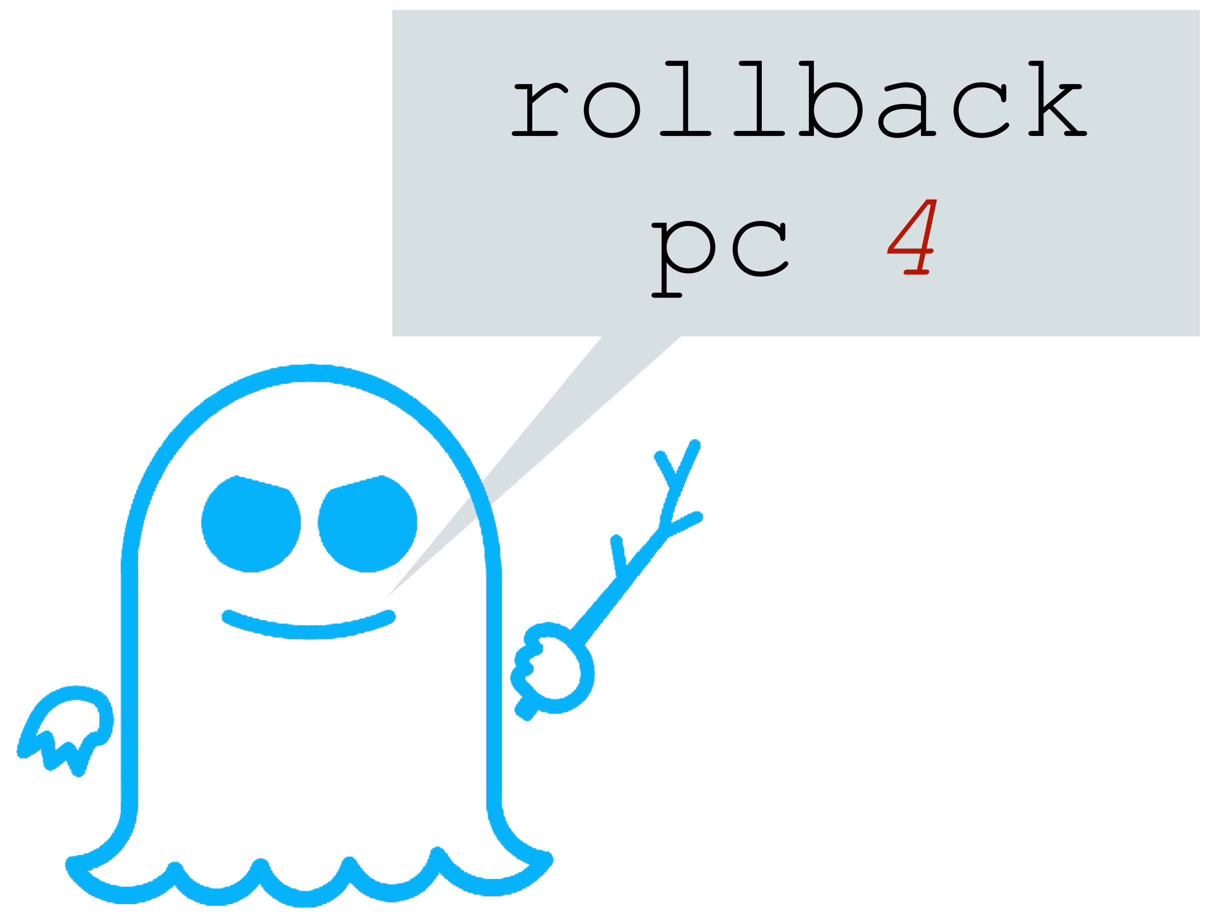

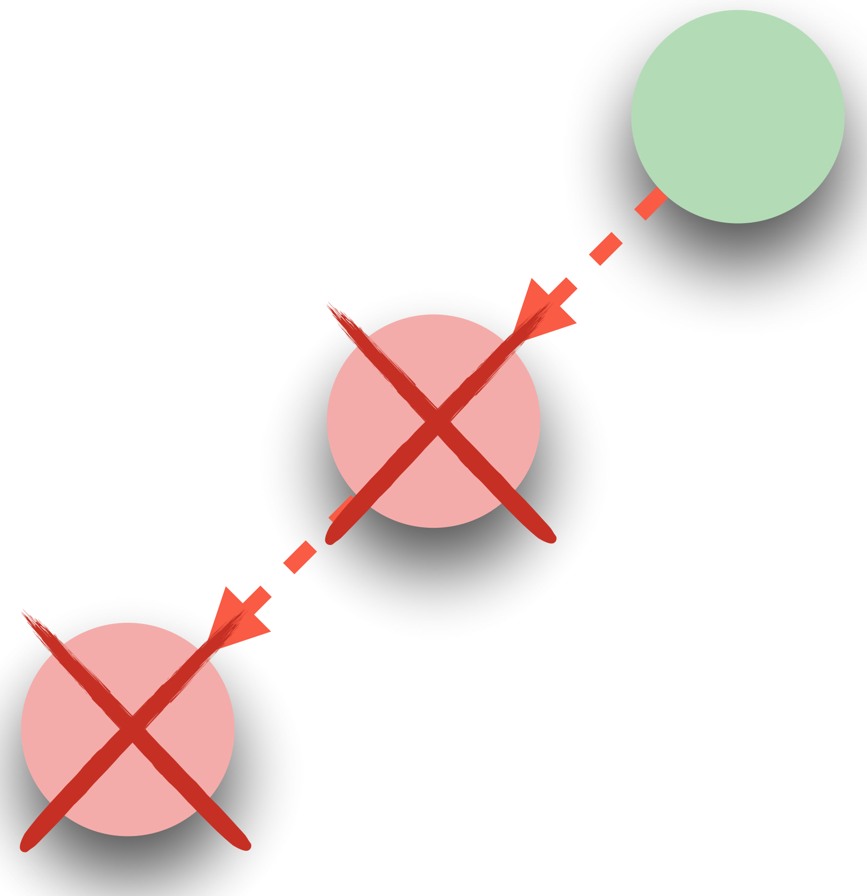

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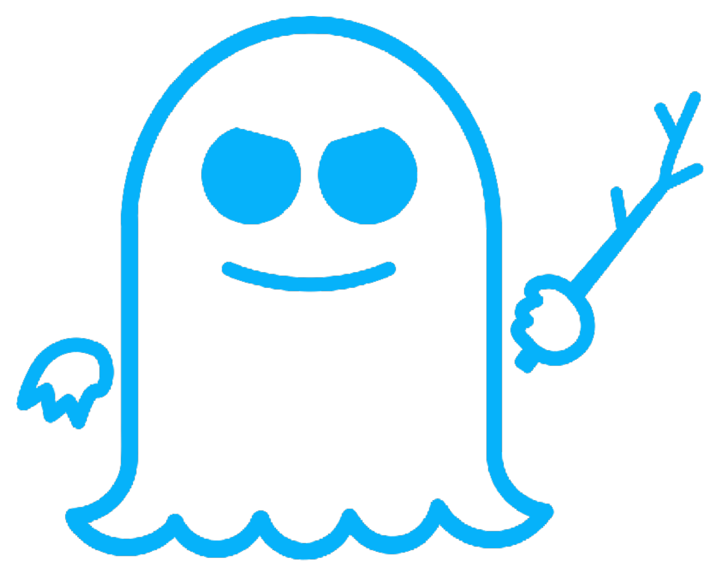

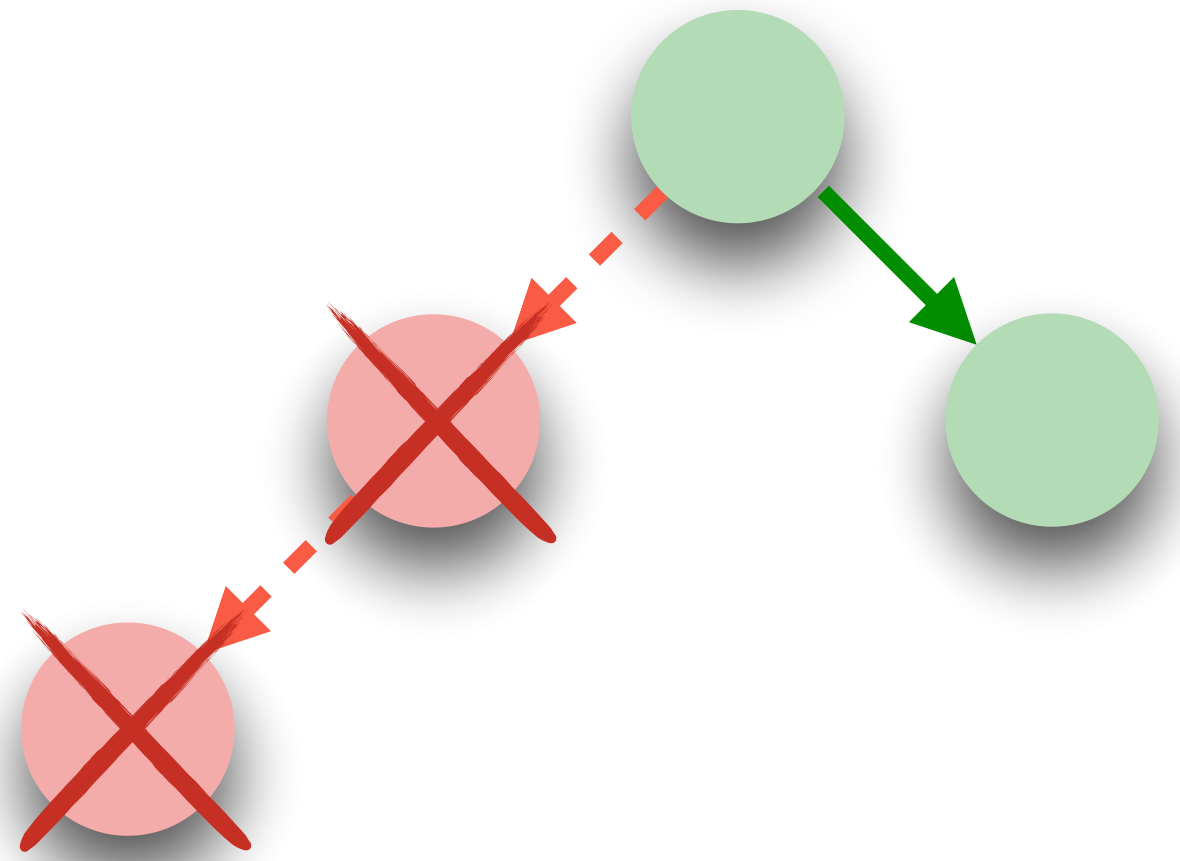

🟩 Non-speculative

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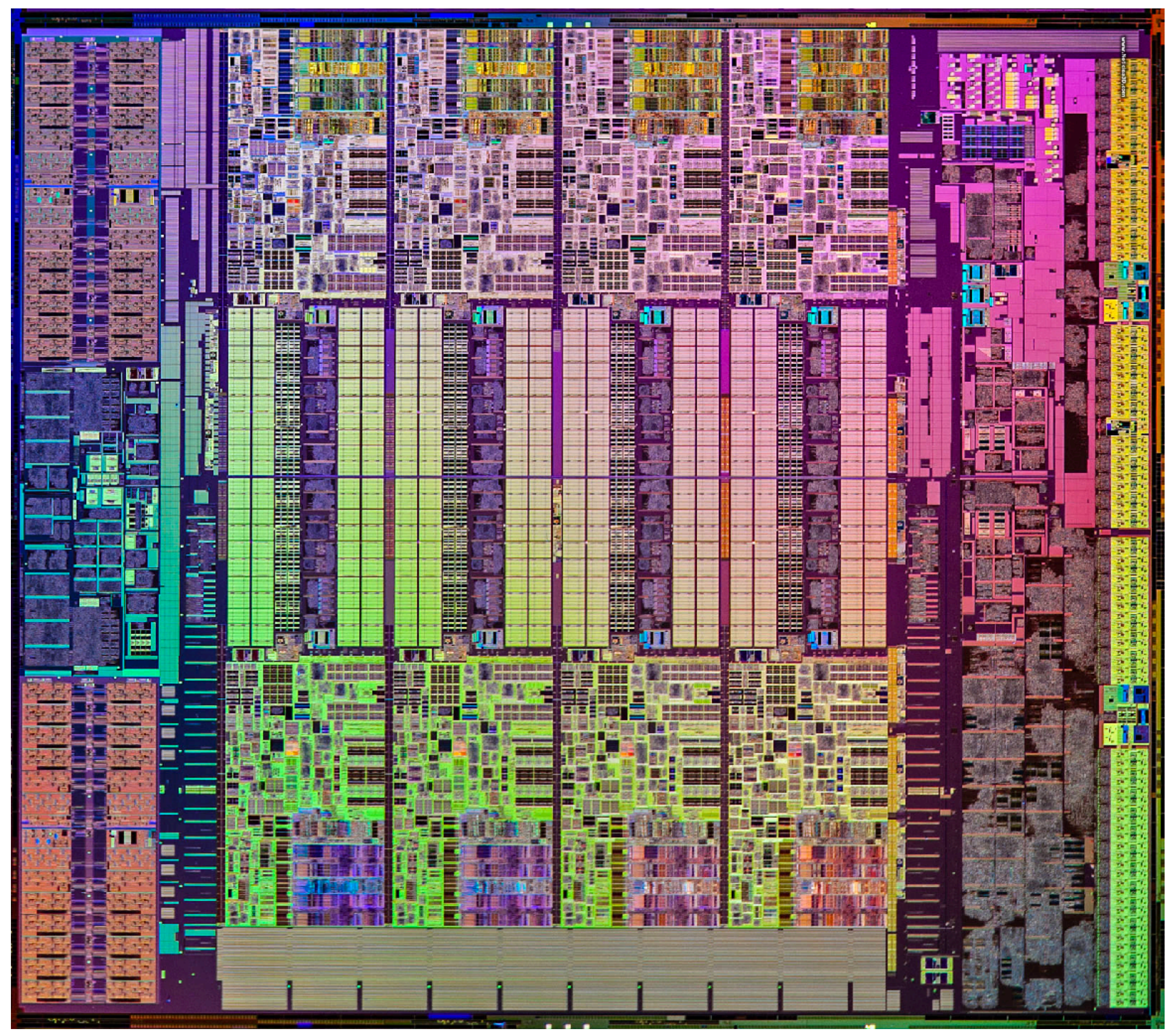
Outline

1. Speculative execution attacks
2. Modeling speculative leaks
3. Hardware-software contracts for secure speculation
4. What about hardware?
5. What about software?
6. Conclusions

Building sound leakage abstractions



Guarnieri, Köpf, Reineke, Vila — Hardware-software contracts for secure speculation — IEEE S&P 2021
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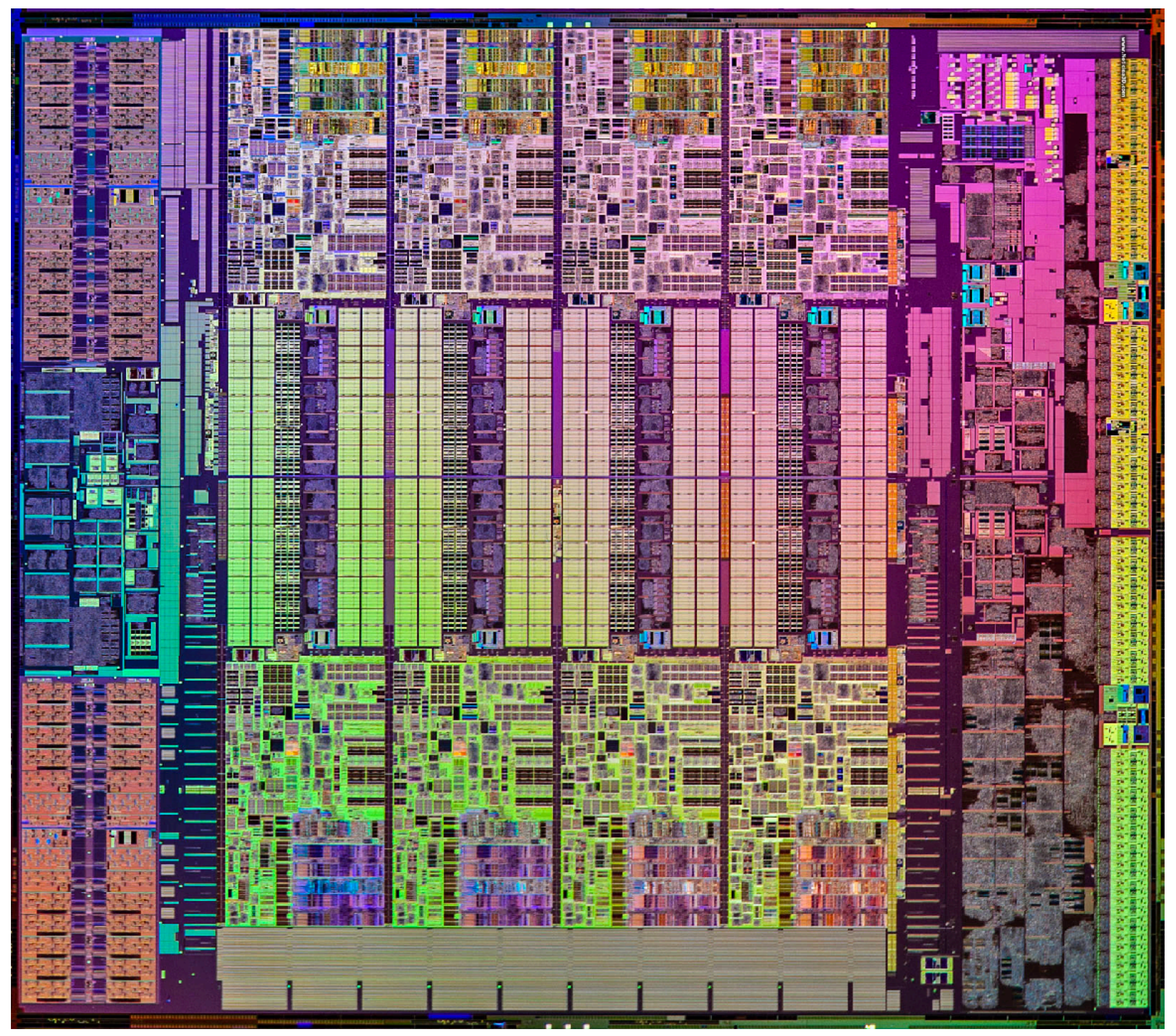
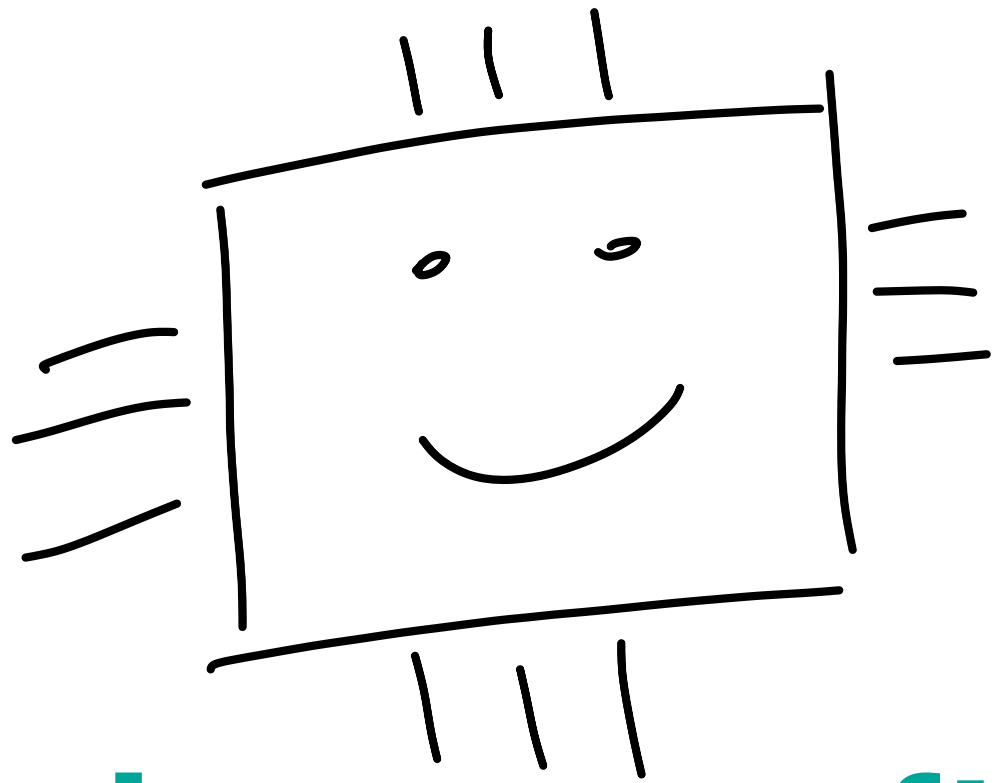
Building sound leakage abstractions





Hardware-software contract

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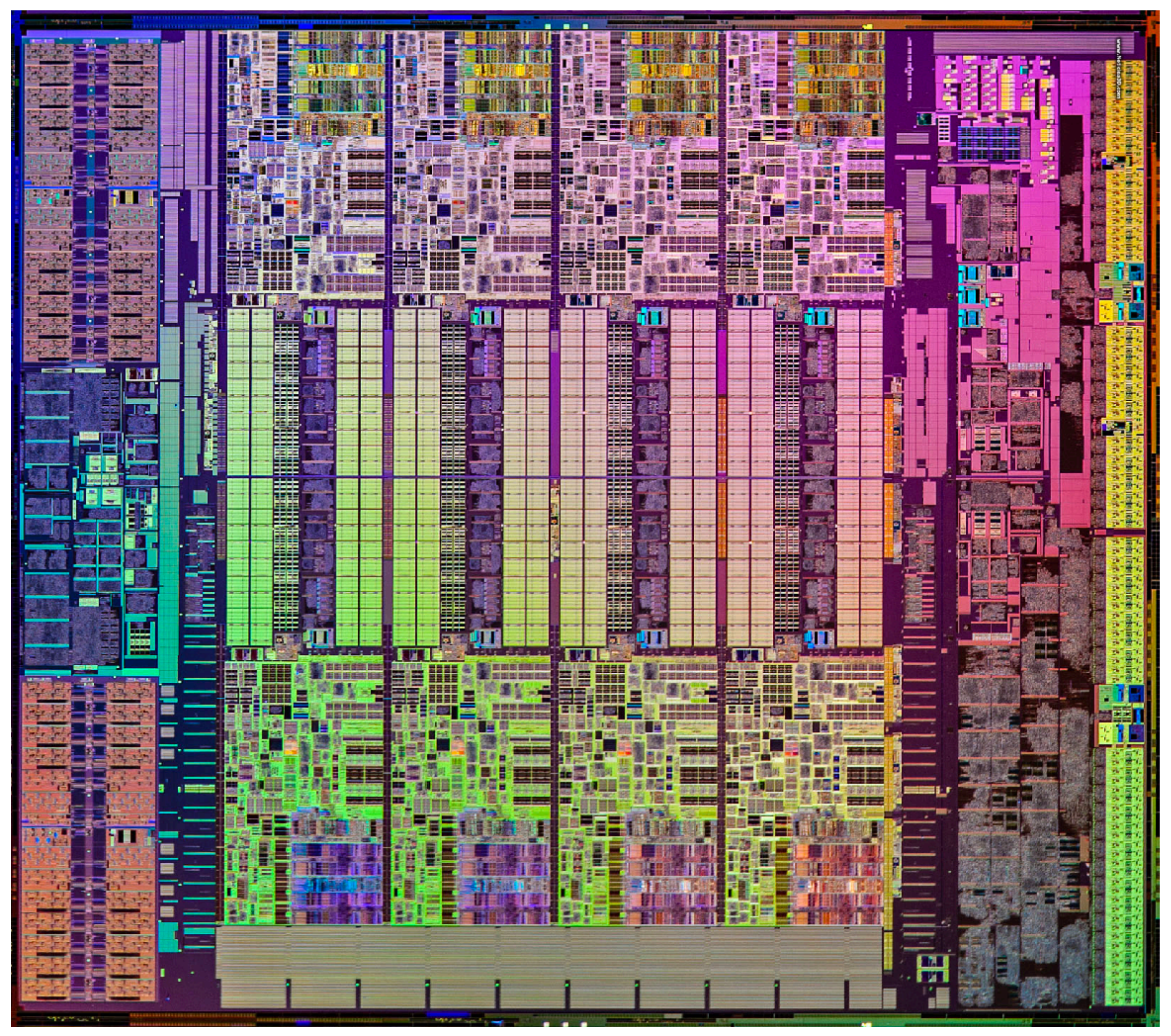

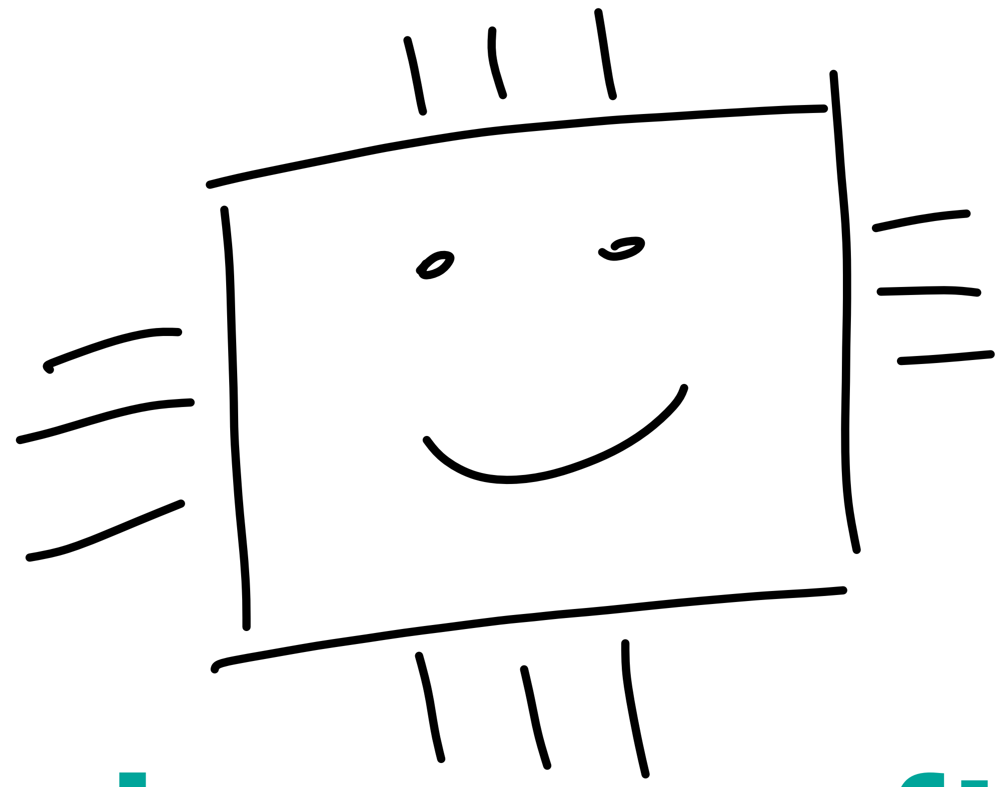

Hardware-software contract

Contracts specify which ***program executions*** a microarchitectural ***adversary can distinguish***

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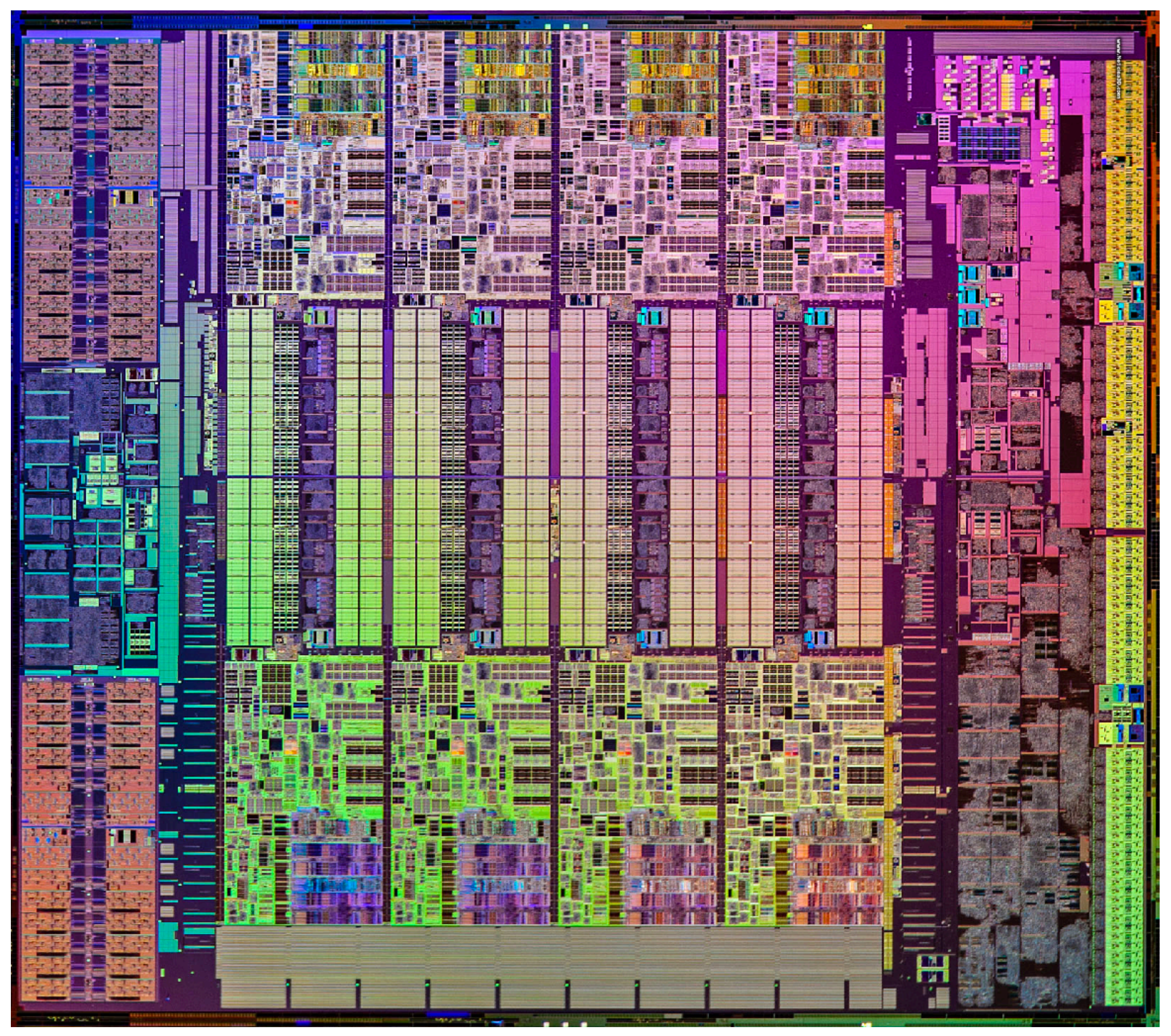

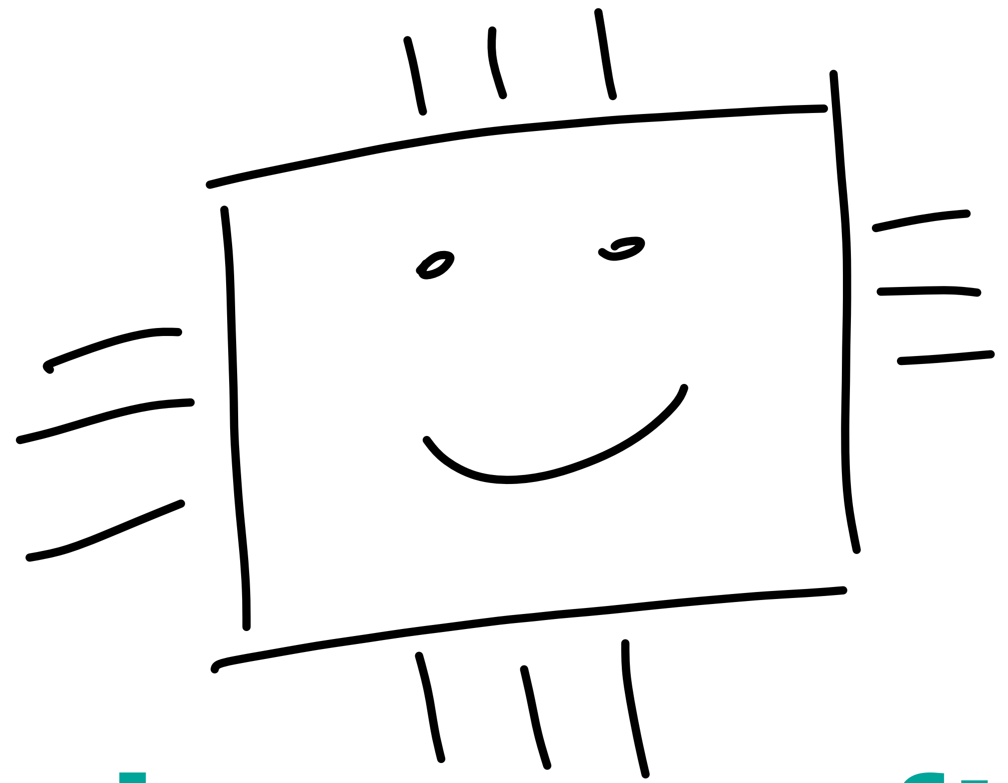

Hardware-software contract

Contracts specify which ***program executions*** a microarchitectural ***adversary can distinguish***

Goals

- Capture ***HW*** security ***guarantees***
- ***Basis*** for ***secure programming***

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Contracts

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Contract

ISA extended with observations

Contracts

Observations expose security-relevant ***events***

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ISA extended with observations

Contract traces: ▤(p, σ)

Contracts

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Contract satisfaction

Hardware ■ satisfies contract ≣ if for all programs p and arch. states σ, σ': if ≣(p, σ)=≣(p, σ') then ■(p, σ) =■(p, σ')

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Contracts for secure speculation

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Contract =

Execution Mode · Observer Mode

Contracts for secure speculation

At ISA level

Contract =

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Contracts for secure speculation

At ISA level

Contract = $\boxed{\text{Execution Mode}} \cdot$ Observer Mode

How are programs executed?

Contracts for secure speculation

At ISA level

Contract =

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How are programs executed?

What is visible about the execution?

Contracts for secure speculation

Contract =
$\boxed{\text{Execution Mode}}$ · Observer Mode

seq — sequential execution
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Contracts for secure speculation

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pc — only program counter

ct — **pc** + address of loads/stores

arch — **ct** + loaded values

Contracts for secure speculation

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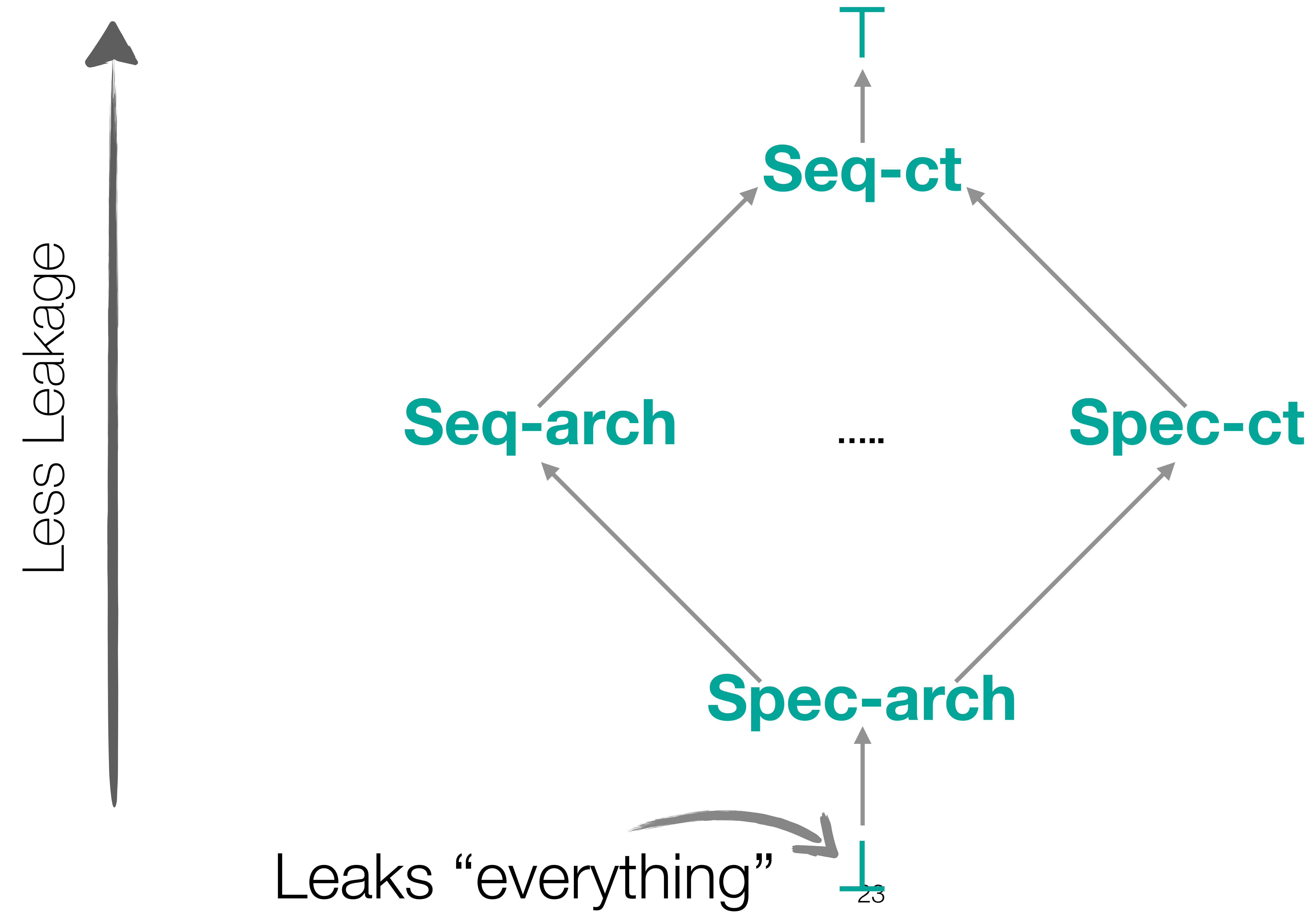
A lattice of contracts

Less Leakage

$$\begin{tikzcd}
& \top & \\
& \textbf{Seq-ct} \arrow[u] & \\
\textbf{Seq-arch} \arrow[ur] & \text{.....} & \textbf{Spec-ct} \arrow[ul] \\
& \textbf{Spec-arch} \arrow[ul] \arrow[ur] & \\
& \bot \arrow[u] &
\end{tikzcd}$$

A lattice of contracts



$$\begin{tikzcd}
 & \top & \\
 & \text{Seq-ct} \arrow[u] & \\
\text{Seq-arch} \arrow[ur] & \ldots & \text{Spec-ct} \arrow[ul] \\
 & \text{Spec-arch} \arrow[ul] \arrow[ur] & \\
 & \bot \arrow[u] &
\end{tikzcd}$$

A lattice of contracts

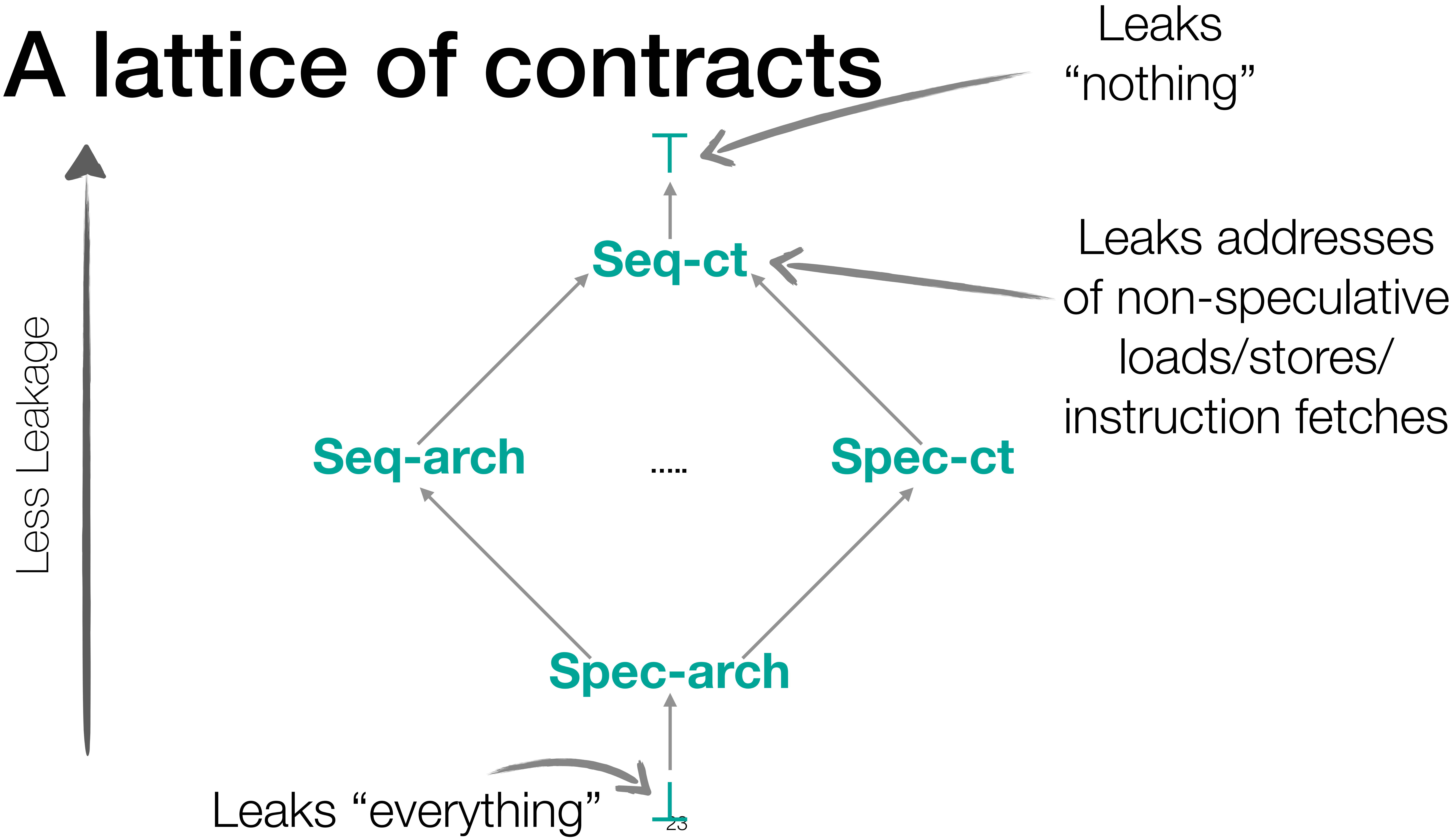
Leaks “nothing”

$$\begin{tikzcd}
 & \top & \\
 & \textbf{Seq-ct} \arrow[u] & \\
\textbf{Seq-arch} \arrow[ur] & \ldots\ldots & \textbf{Spec-ct} \arrow[ul] \\
 & \textbf{Spec-arch} \arrow[ul] \arrow[ur] & \\
 & \bot \arrow[u] &
\end{tikzcd}$$

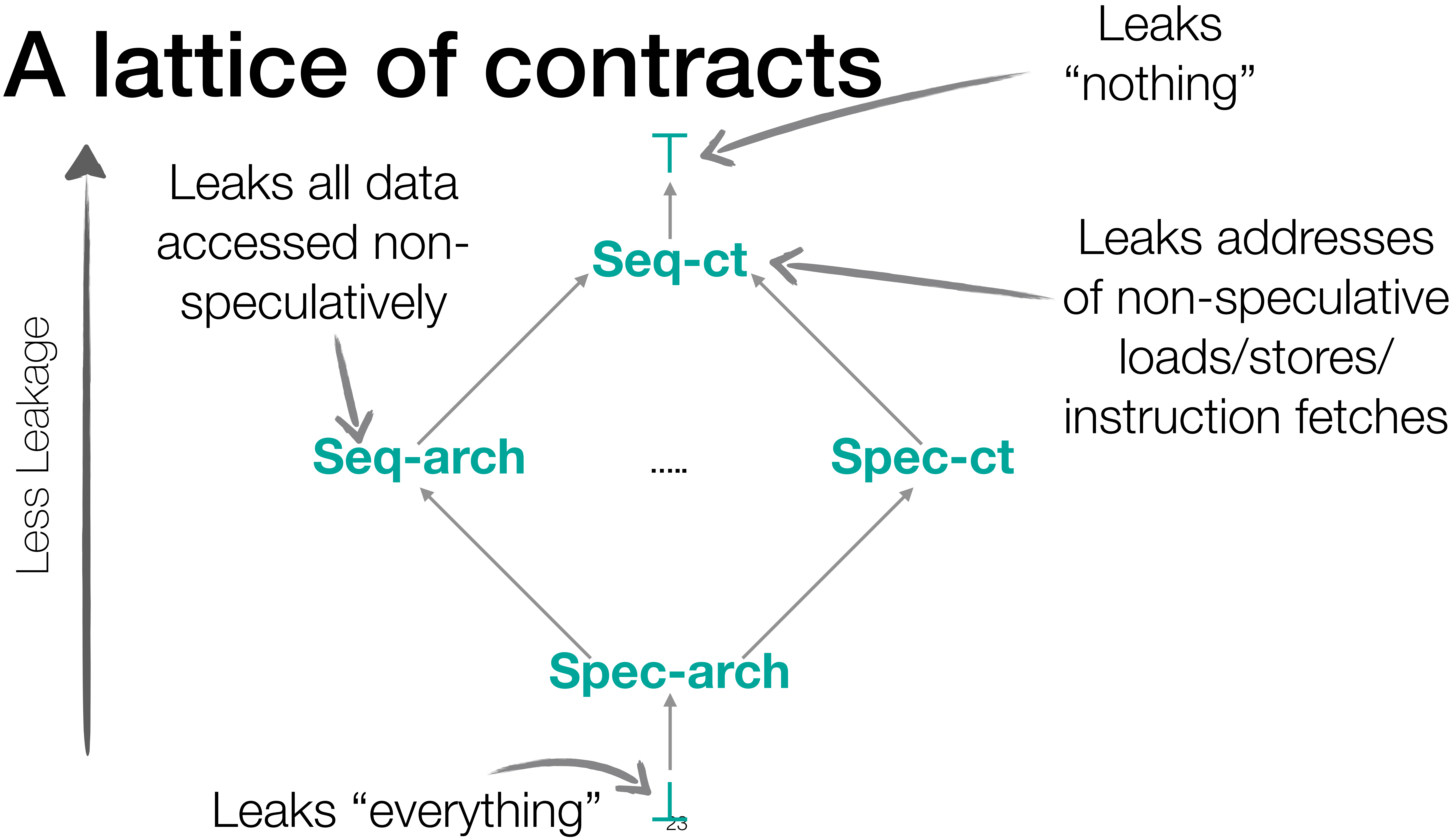
Less Leakage

Leaks “everything”

A lattice of contracts



A lattice of contracts


Leaks "nothing"
⊤
Leaks all data accessed non-speculatively
Seq-ct
Leaks addresses of non-speculative loads/stores/ instruction fetches
Less Leakage
Seq-arch
.....
Spec-ct
Spec-arch
Leaks "everything"
⊥

A lattice of contracts

Less Leakage

$$\begin{tikzcd}
 & \top & \\
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 & \bot \arrow[u] &
\end{tikzcd}$$

Leaks "nothing"

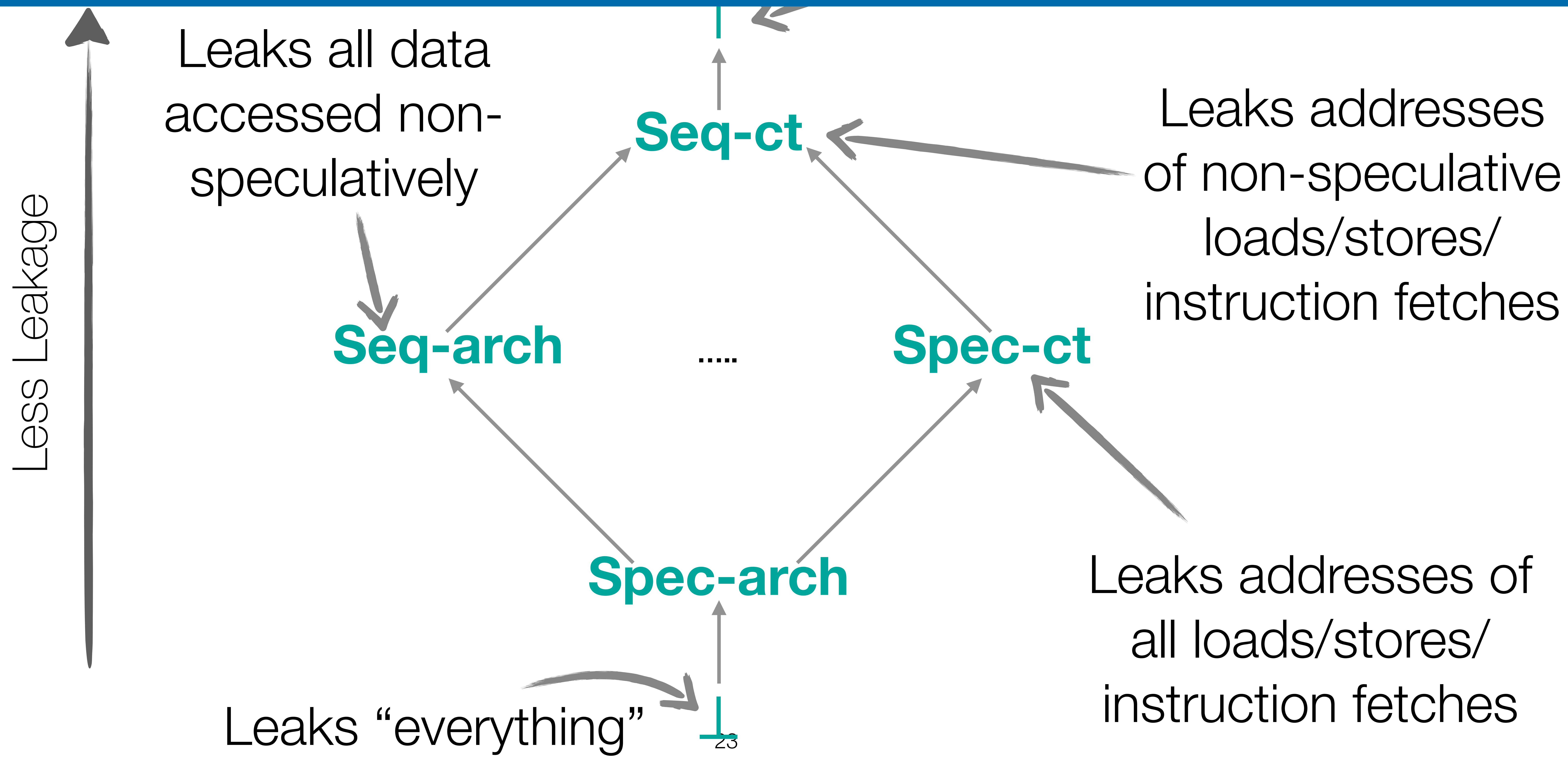
Leaks all data accessed non-speculatively

Leaks addresses of non-speculative loads/stores/ instruction fetches

Leaks addresses of all loads/stores/ instruction fetches

Leaks "everything"

Model different security guarantees! 🥳



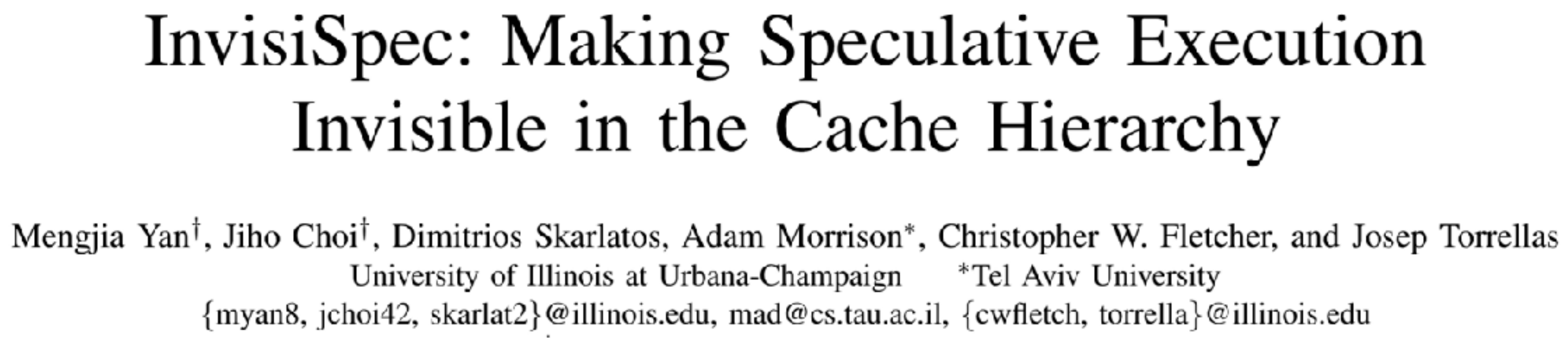
Less Leakage
Leaks all data accessed non-speculatively
Leaks addresses of non-speculative loads/stores/ instruction fetches
Seq-ct
Seq-arch
.....
Spec-ct
Spec-arch
Leaks addresses of all loads/stores/ instruction fetches
Leaks “everything”
⊥

Outline

1. Speculative execution attacks
2. Modeling speculative leaks
3. Hardware-software contracts for secure speculation
4. What about hardware?
5. What about software?
6. Conclusions

Hardware countermeasures

Hardware countermeasures



InvisiSpec: Making Speculative Execution Invisible in the Cache Hierarchy

Mengjia Yan[†], Jiho Choi[†], Dimitrios Skarlatos, Adam Morrison[*], Christopher W. Fletcher, and Josep Torrellas
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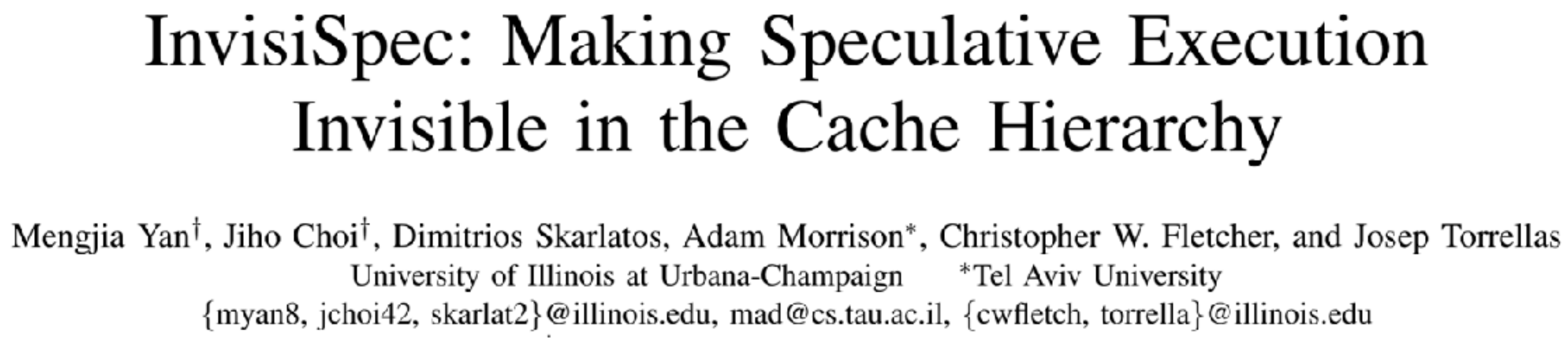
Hardware countermeasures



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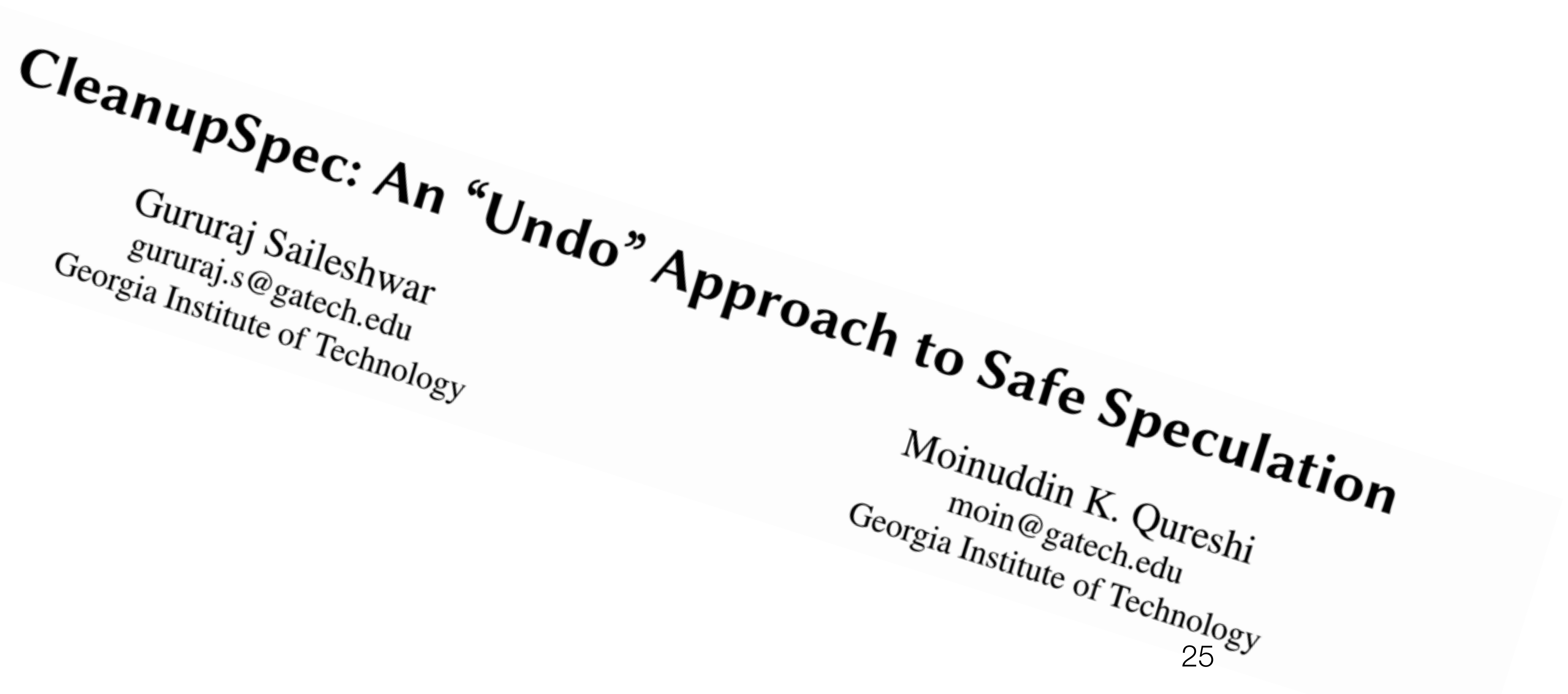

CleanupSpec: An “Undo” Approach to Safe Speculation

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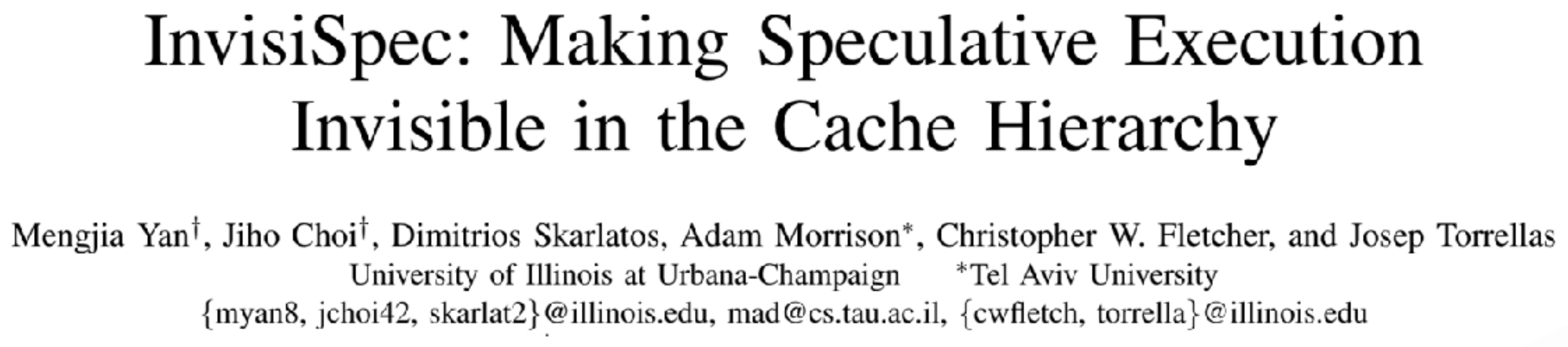
Hardware countermeasures



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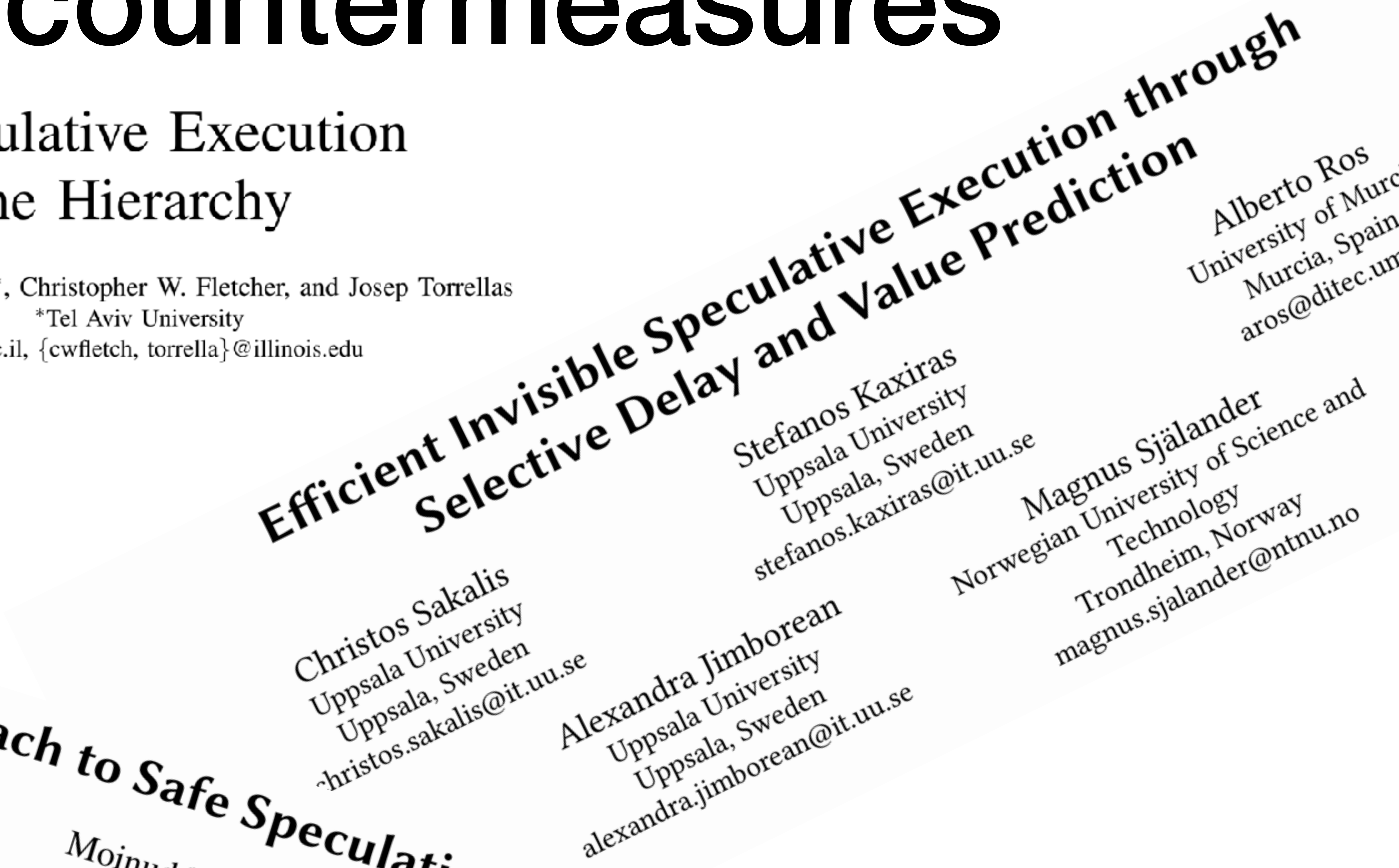

Efficient Invisible Speculative Execution through Selective Delay and Value Prediction

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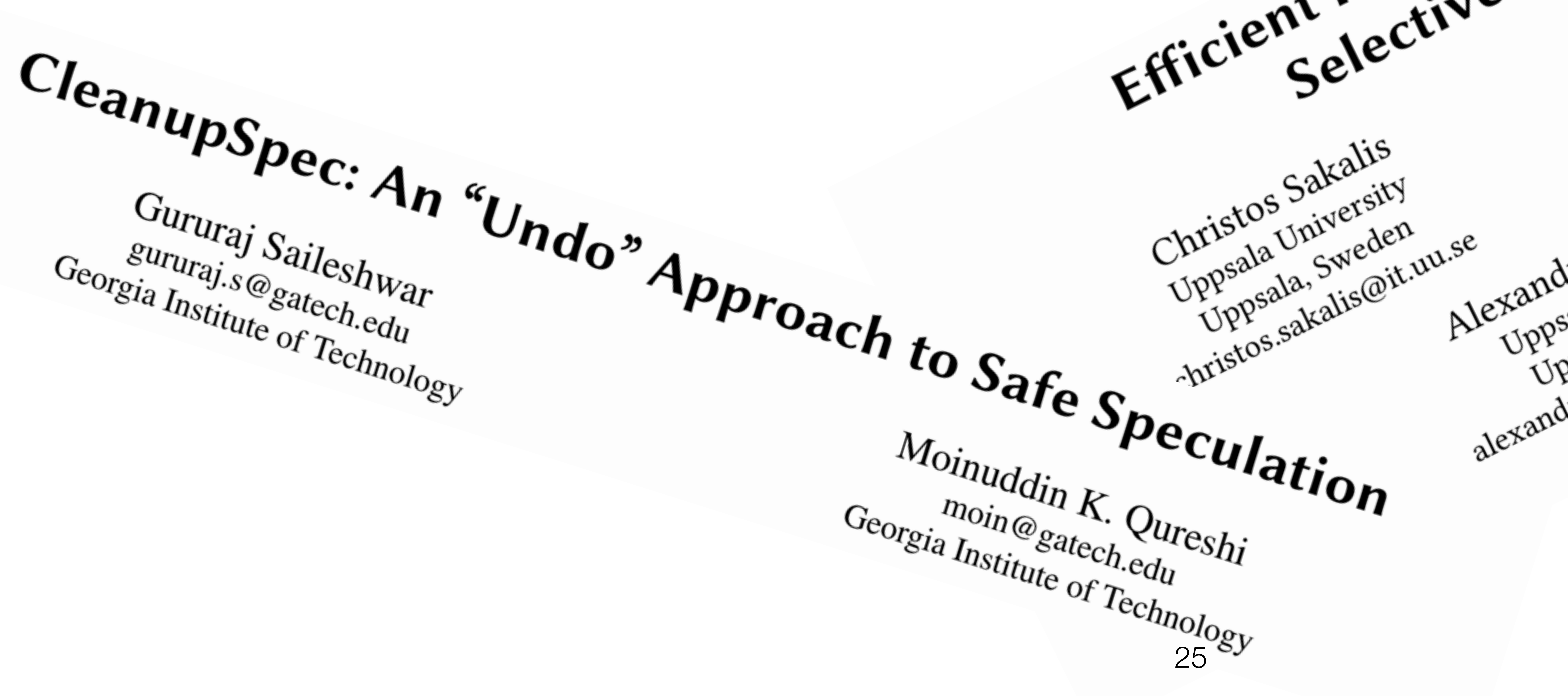

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Hardware countermeasures

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NDA: Preventing Speculative Execution Attacks at Their Source

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CleanupSpec: A

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Approach to Safe Speculation

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Hardware countermeasures

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Speculative Taint Tracking (STT): A Comprehensive Protectio
for Speculatively Accessed Data

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Security guarantees?

Hardware countermeasures

```
if (x < A_size)
   y = A[x]
   z = B[y]
end
```

Hardware countermeasures

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🟩 Non-speculative

🟥 Speculative

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Delay loads until they are no longer speculative
[Sakalis et al., ISCA'19]

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Taint speculatively loaded data + delay tainted loads
[STT and NDA, MICRO'19]

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Delay loads until they are no longer speculative
[Sakalis et al., ISCA'19]

Countermeasures block different leaks!

Taint speculatively loaded data + delay tainted loads
[STT and NDA, MICRO'19]

🟩 Non-speculative

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Guarantees

$$\begin{tikzcd}
 & \text{Seq-ct} \\
\text{Seq-arch} \arrow[ur] & \\
 & \text{Seq/spec-ct/pc} \arrow[uu] \\
 & \text{Spec-ct} \arrow[u] \\
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\end{tikzcd}$$

OoO	Vanilla out-of-order (OoO) CPU
NS	In-order CPU (no speculative execution)
LD	OoO CPU+load delay
TT	OoO CPU+taint tracking

Guarnieri, Köpf, Reineke, Vila — Hardware-software contracts for secure speculation — IEEE S&P 2021
https://arxiv.org/abs/2006.03841

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3-stage pipeline with ***speculative*** and ***out-of-order*** (OoO) execution

Formalized as ***operational semantics***

Attacker observes part of ***microarchitectural state***

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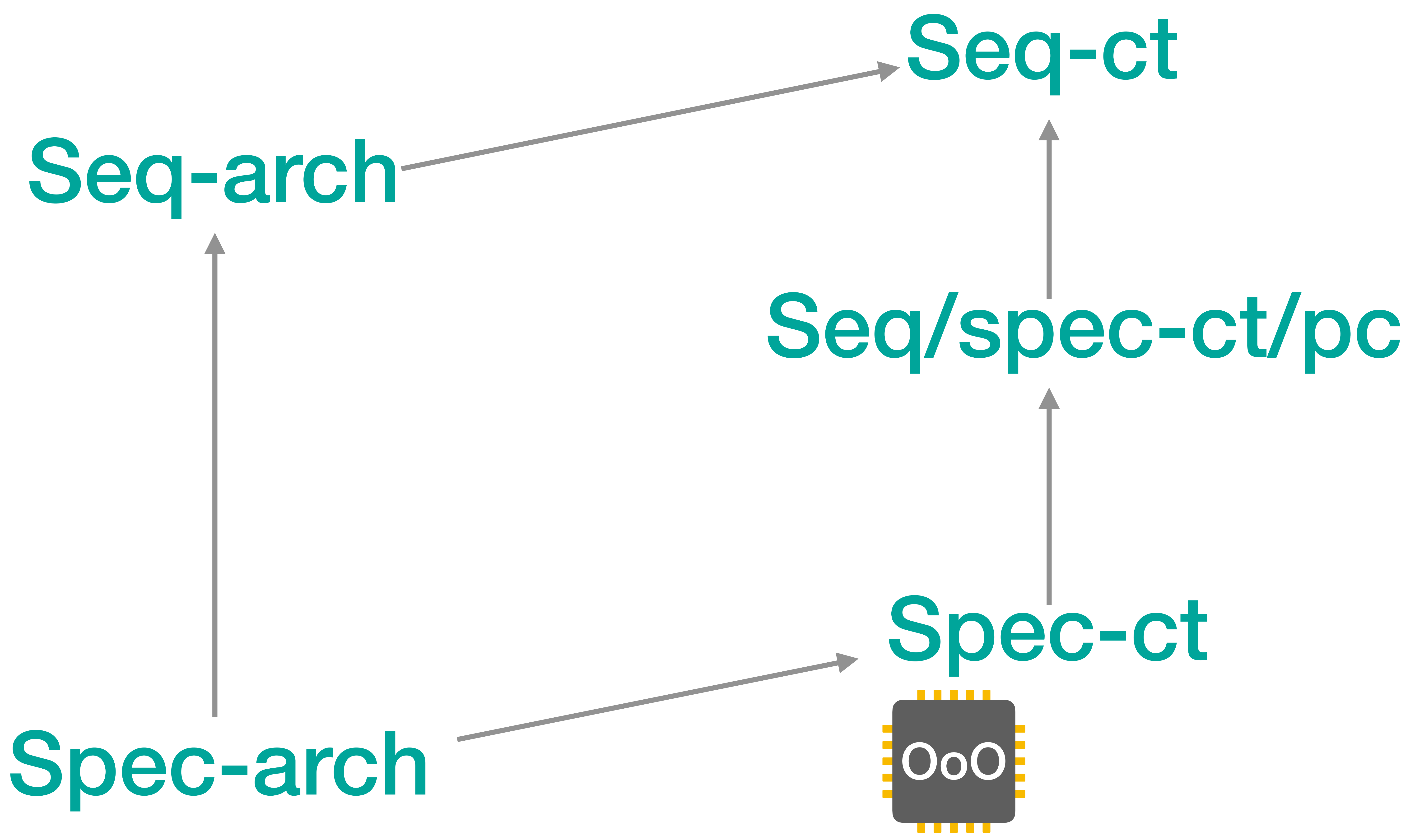

No speculative and out-of-order execution

Instructions executed ***in-order***

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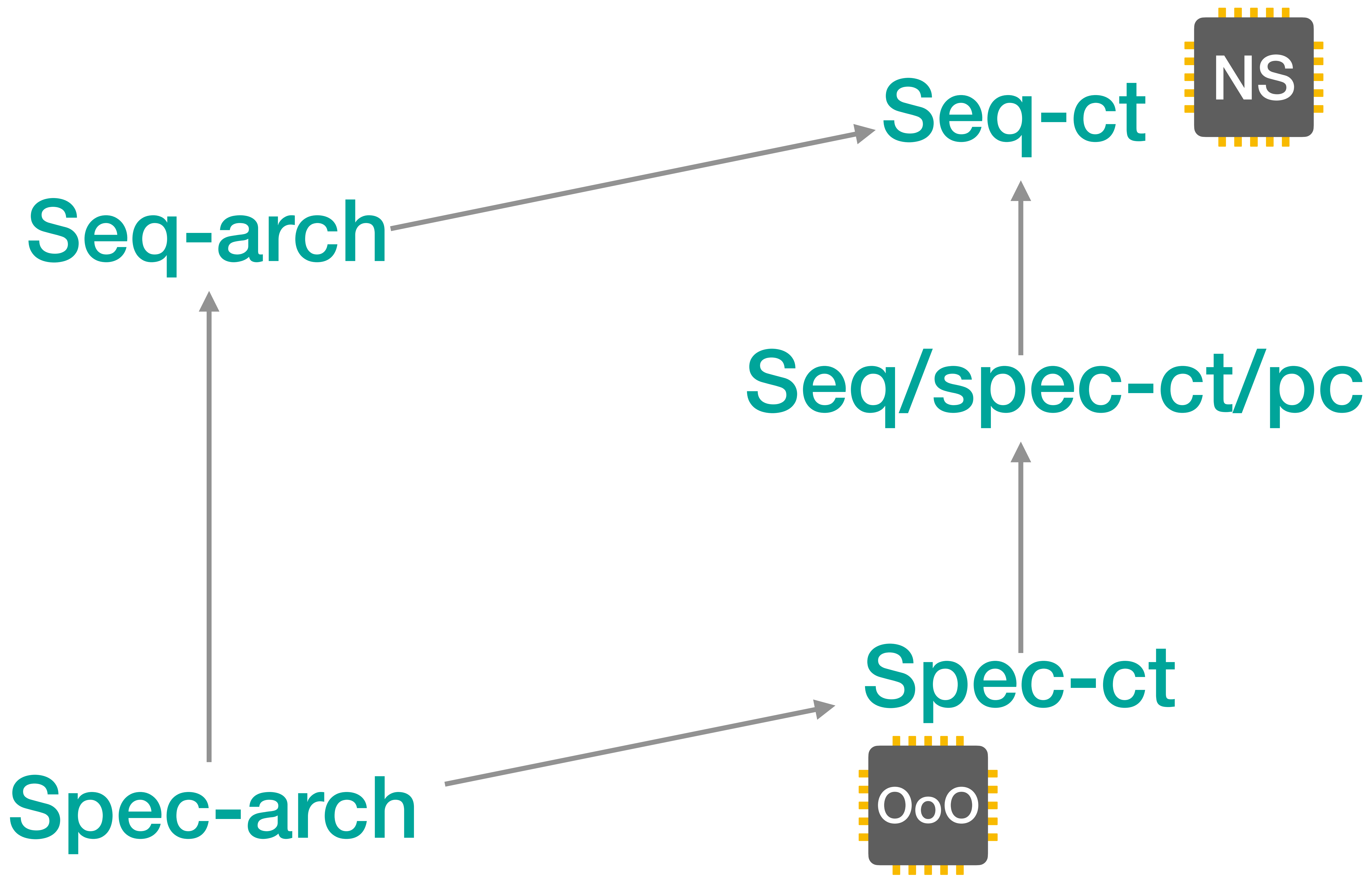

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Instructions executed ***in-order***

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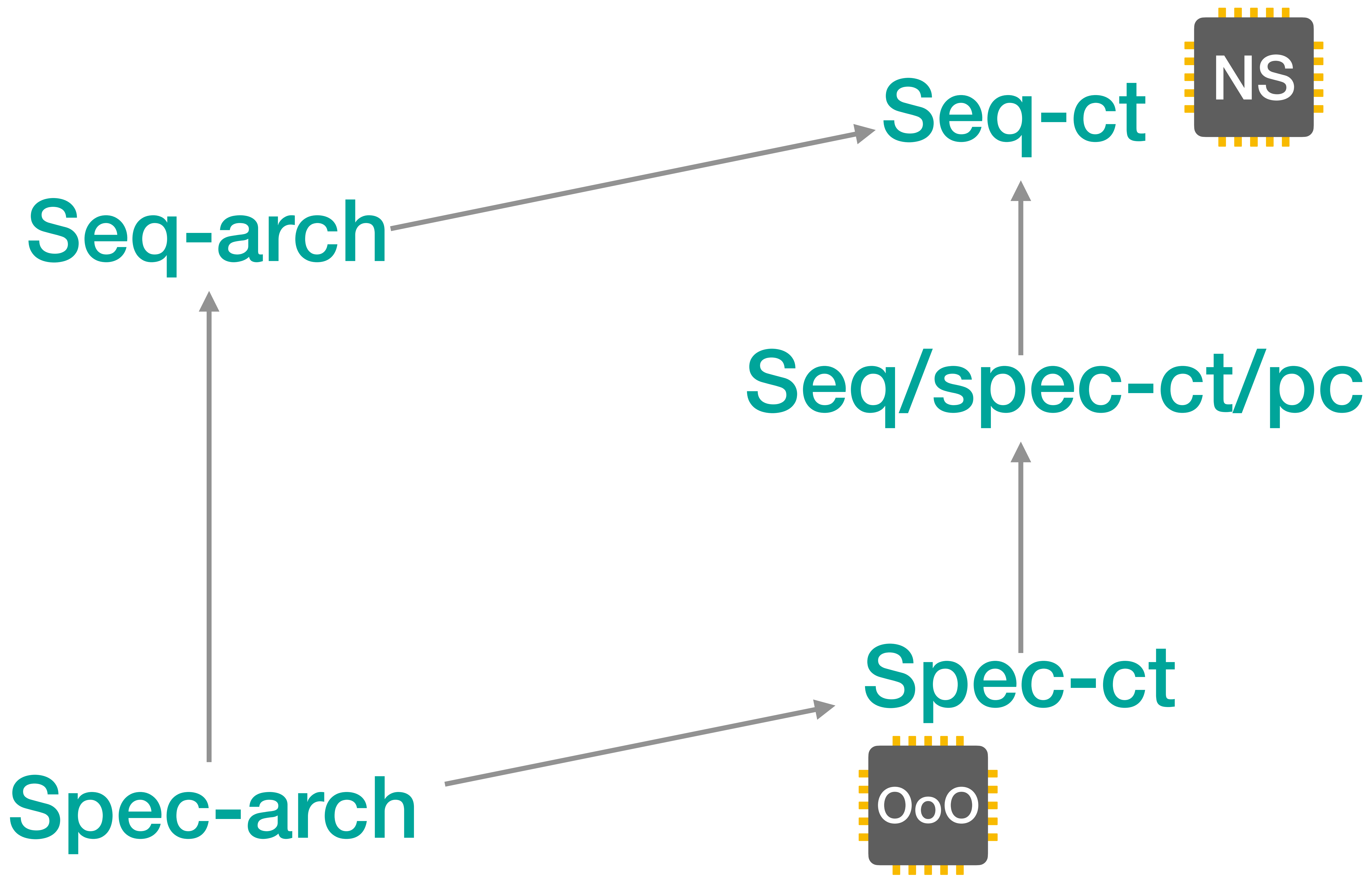

Delaying loads until all sources of ***speculation are resolved***

Sakalis et al., ISCA'19

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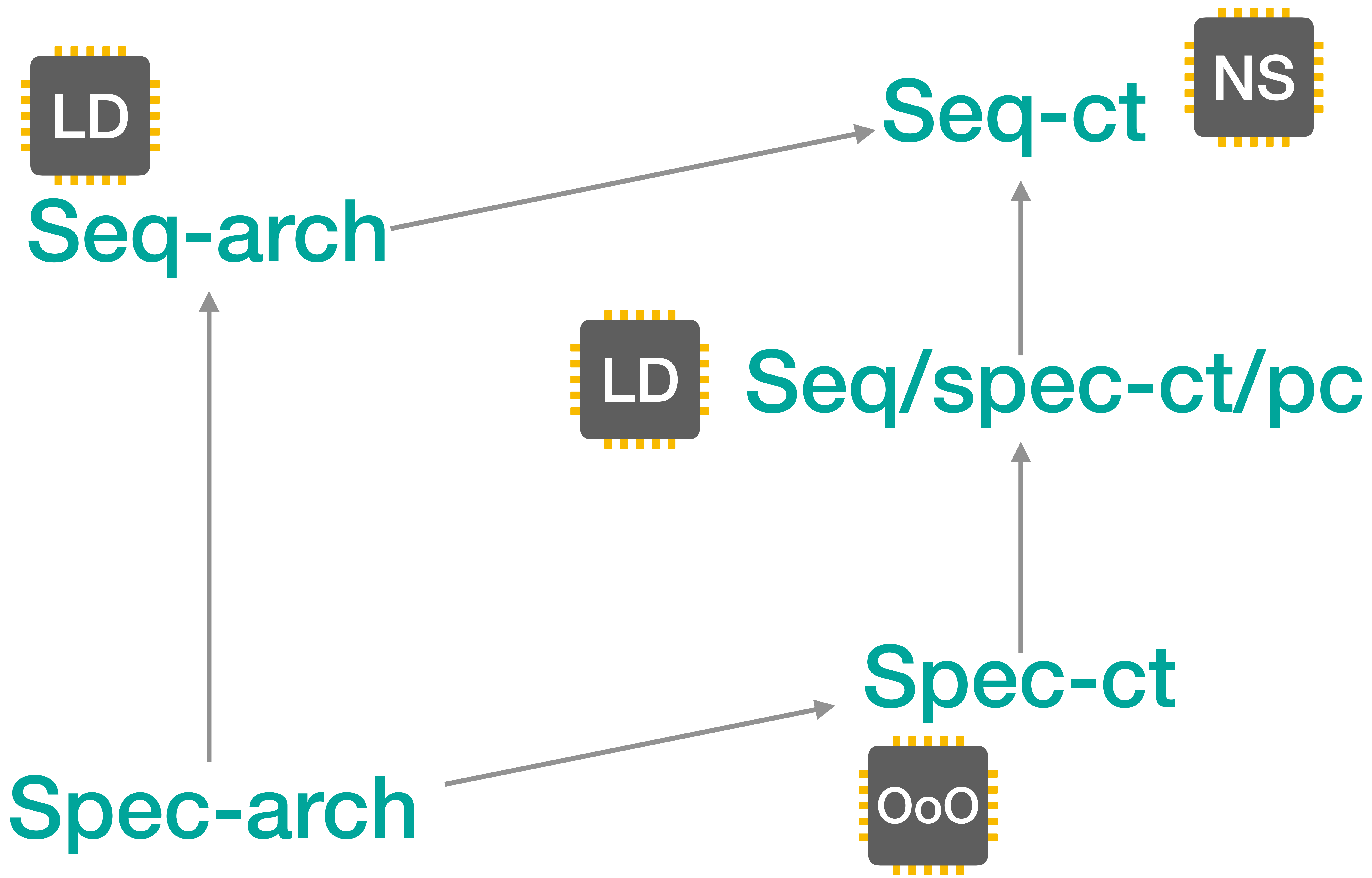

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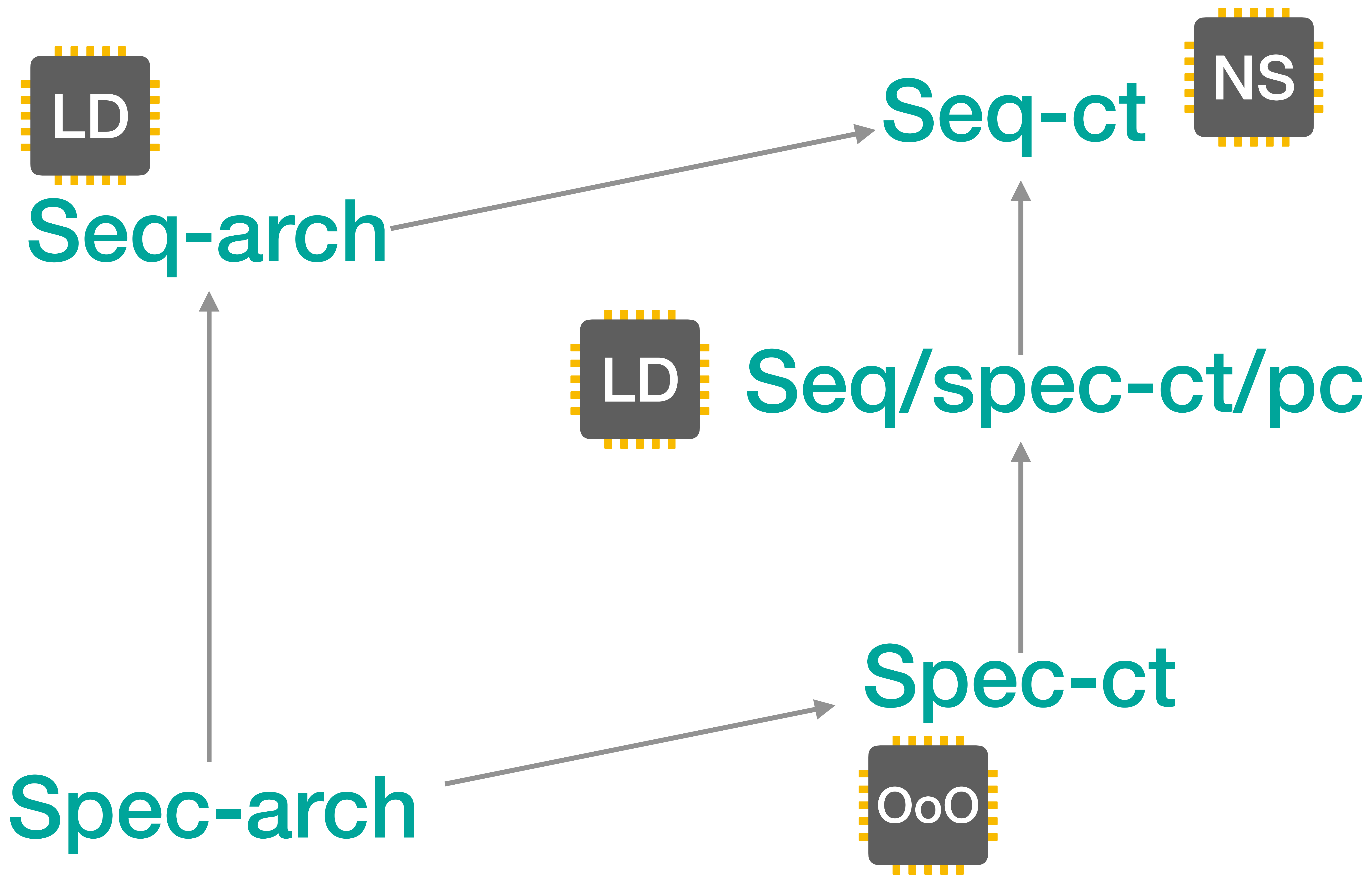

Taint speculative data

Propagate taint through computation

Delay tainted operations

STT and NDA, MICRO'19

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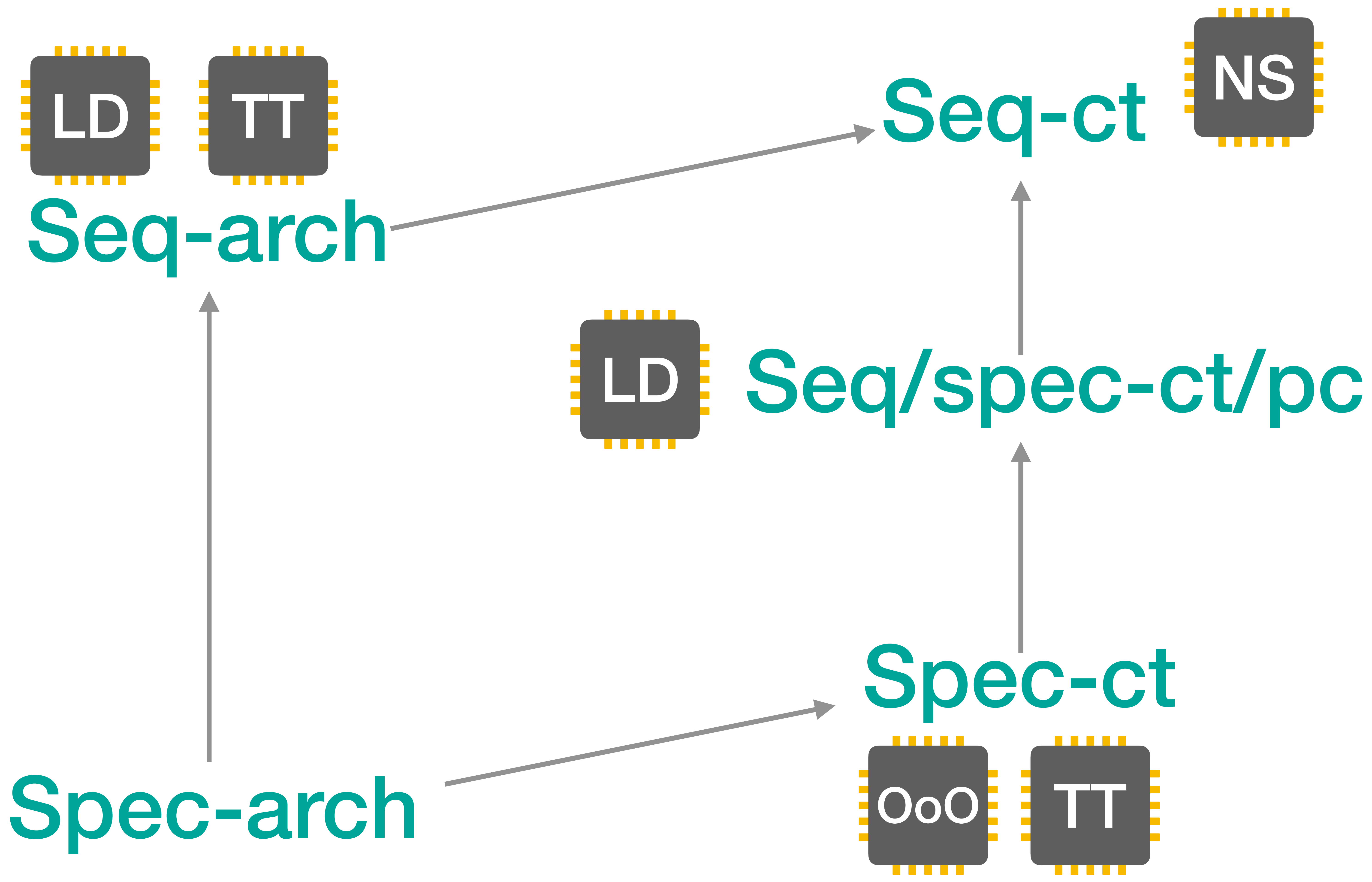

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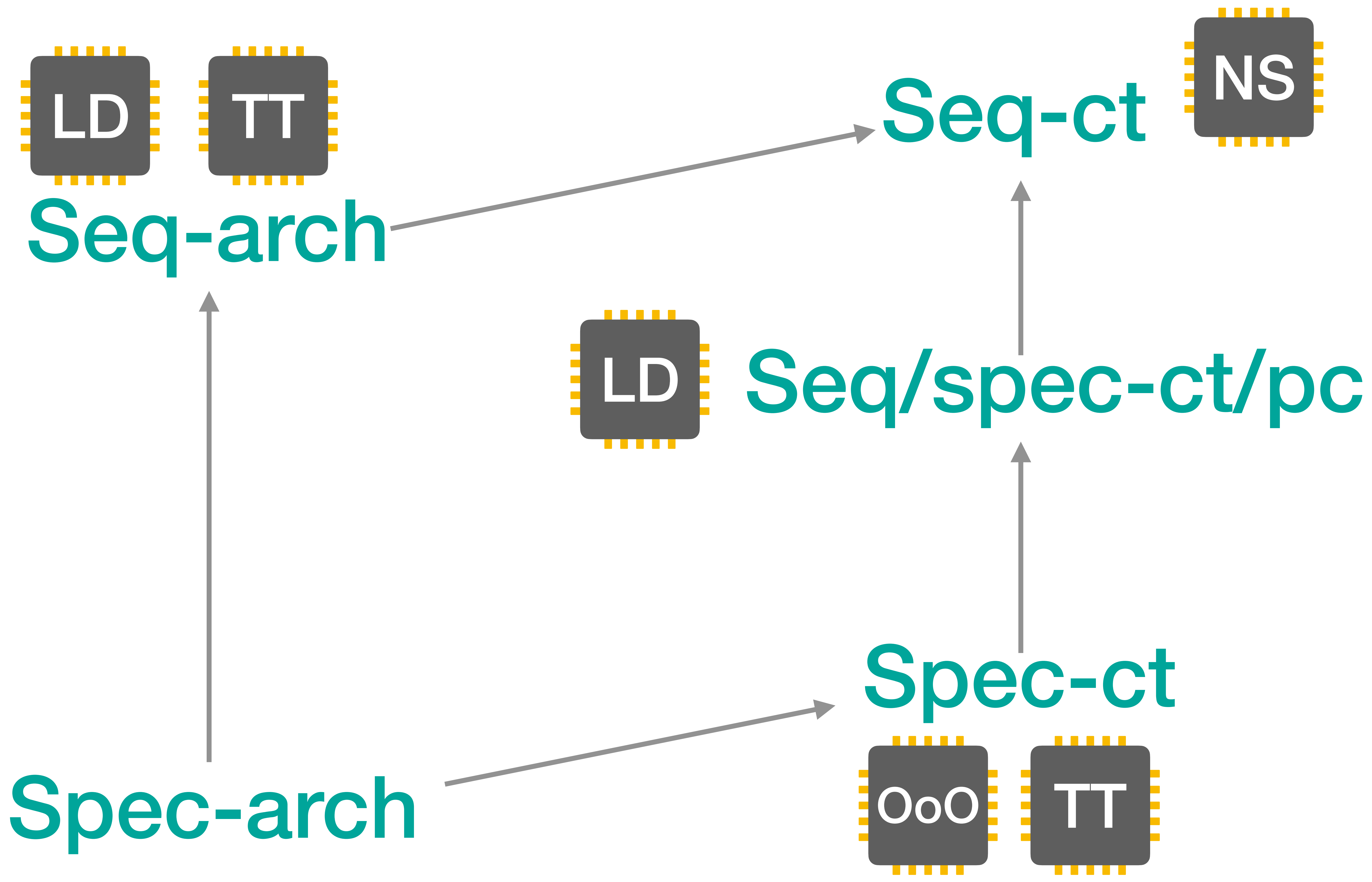
Characterize and compare security guarantees! 🥳



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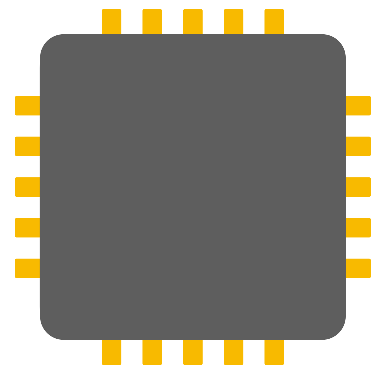
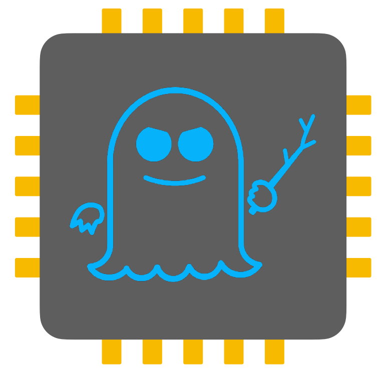
Speculative leaks in programs

Program + CPU with ***speculative execution*** = Secure?

Guarnieri, Köpf, Morales, Reineke, Sánchez — Spectector: Principled detection for speculative leaks — IEEE S&P 2020 — https://arxiv.org/abs/1812.08639

Speculative non-interference

Program **P** is **speculatively non-interferent** if

Leakage(**P**, ) = Leakage(**P**, )

Information leaked by executing **P** ***without*** speculative execution

Information leaked by executing **P** ***with*** speculative execution

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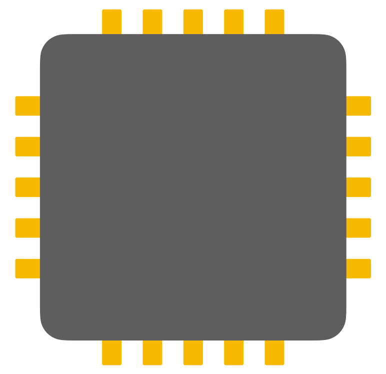
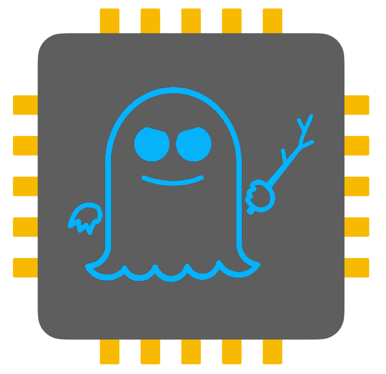
Leakage(**P**, ) = Leakage(**P**, )

Executed under **seq-ct**

Speculative non-interference

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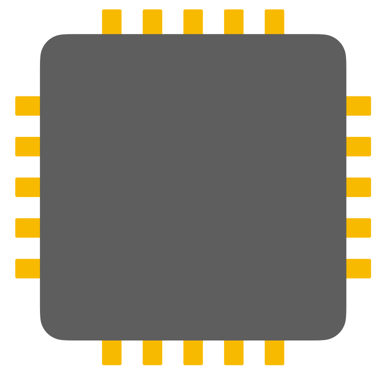
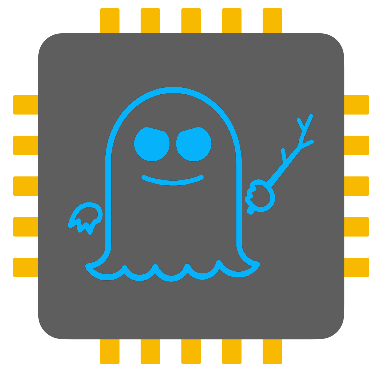
Leakage(**`P`**, ) = Leakage(**`P`**, )

Executed under **seq-ct**

Executed under **spec-ct**

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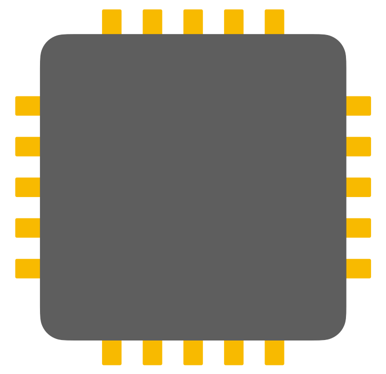
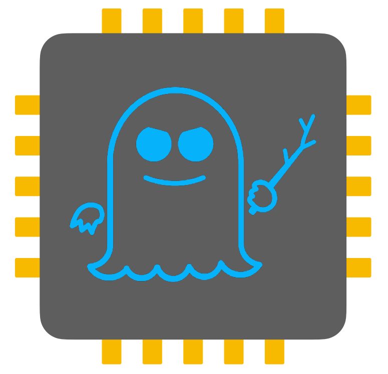
Leakage(**P**, ) = Leakage(**P**, )

For all program states σ and σ':

Speculative non-interference

Program **P** is **speculatively non-interferent** if

Leakage(**P**,) = Leakage(**P**,)

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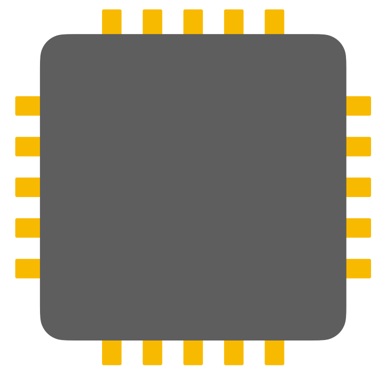
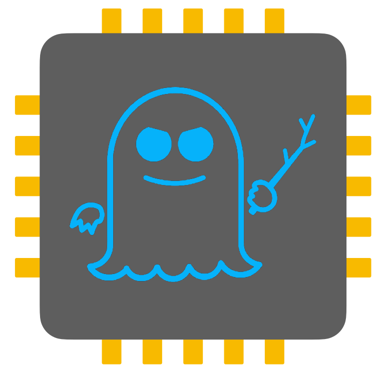
seq-ct(**P**,σ) = **seq-ct**(**P**,σ')

Speculative non-interference

Program **P** is **speculatively non-interferent** if

Leakage(**P**, ) = Leakage(**P**, )

For all program states σ and σ':

seq-ct(**P**,σ) = **seq-ct**(**P**,σ')

$\Longrightarrow$ **spec-ct**(**P**,σ) = **spec-ct**(**P**,σ')

Speculative non-interference

```
if (x < A_size)
   y = A[x]
   z = B[y]
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```

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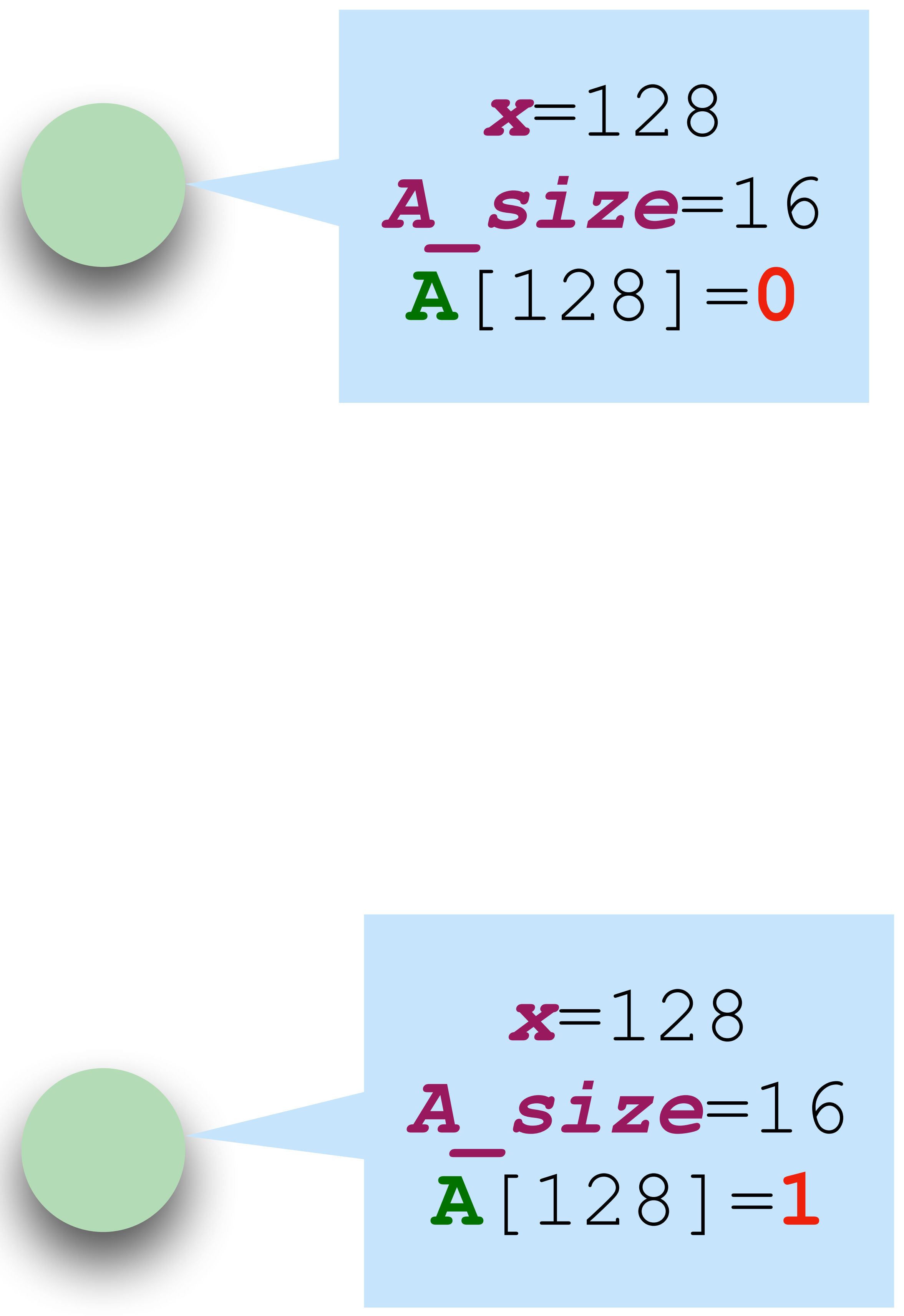

🟩 Non-speculative

🟥 Speculative

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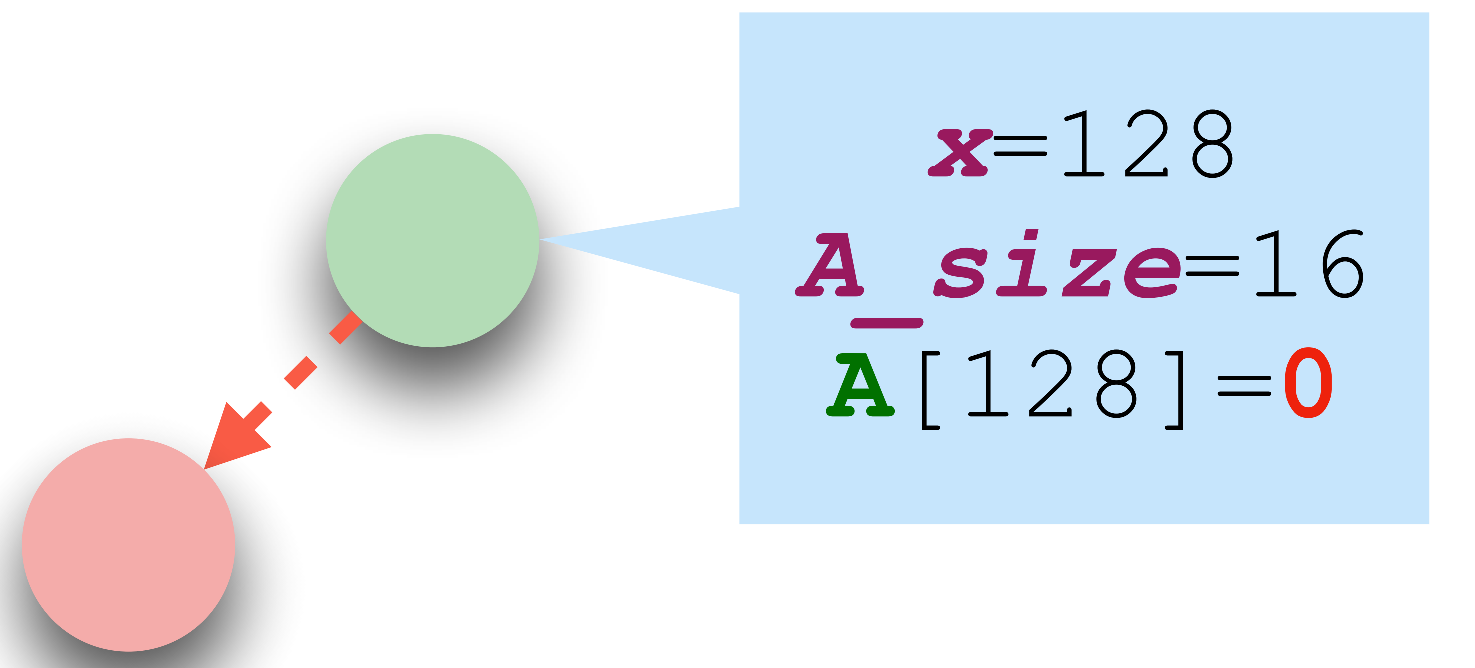

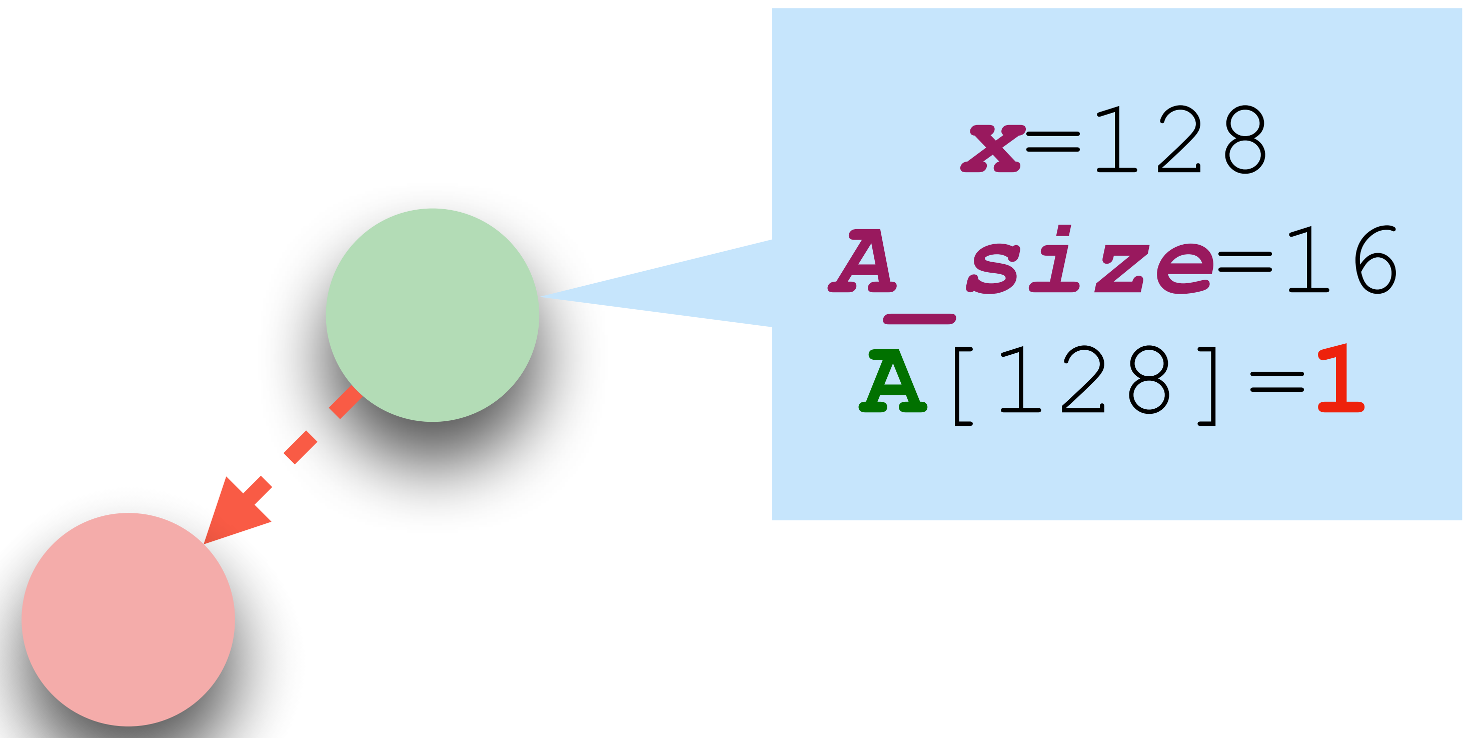

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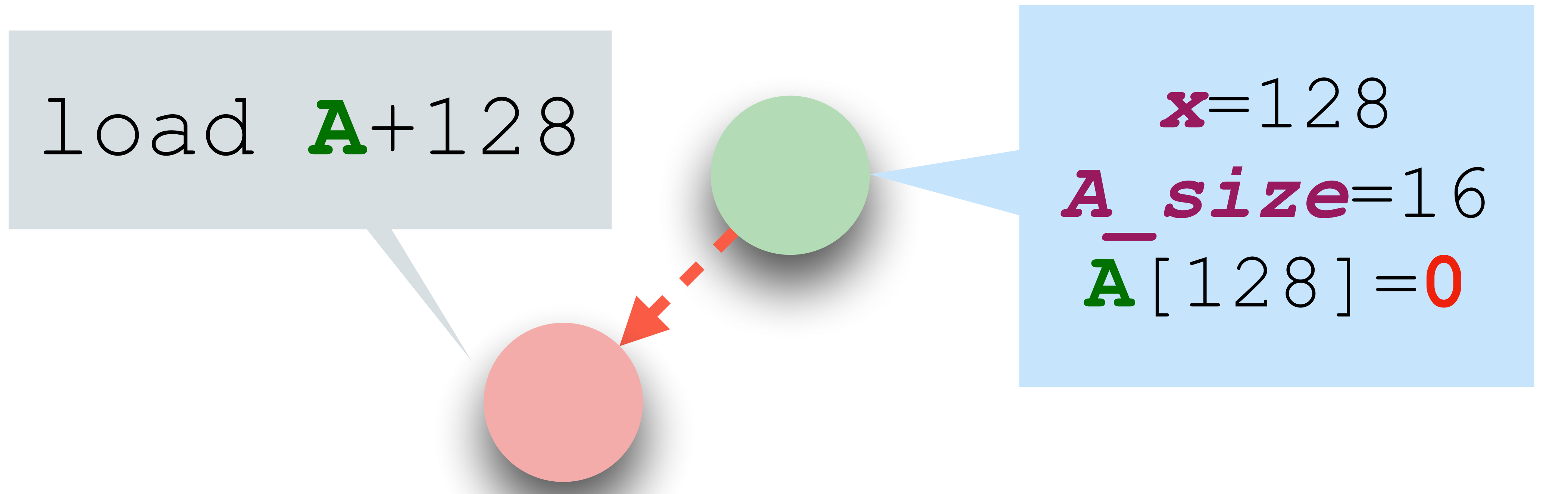

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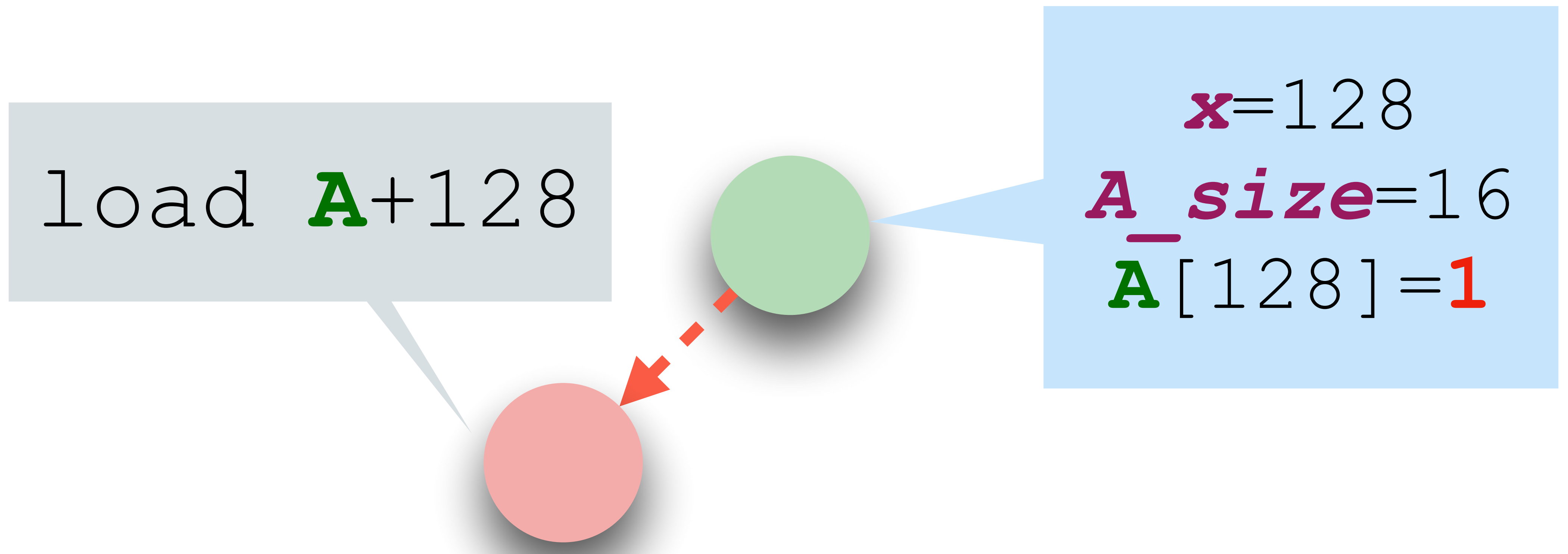

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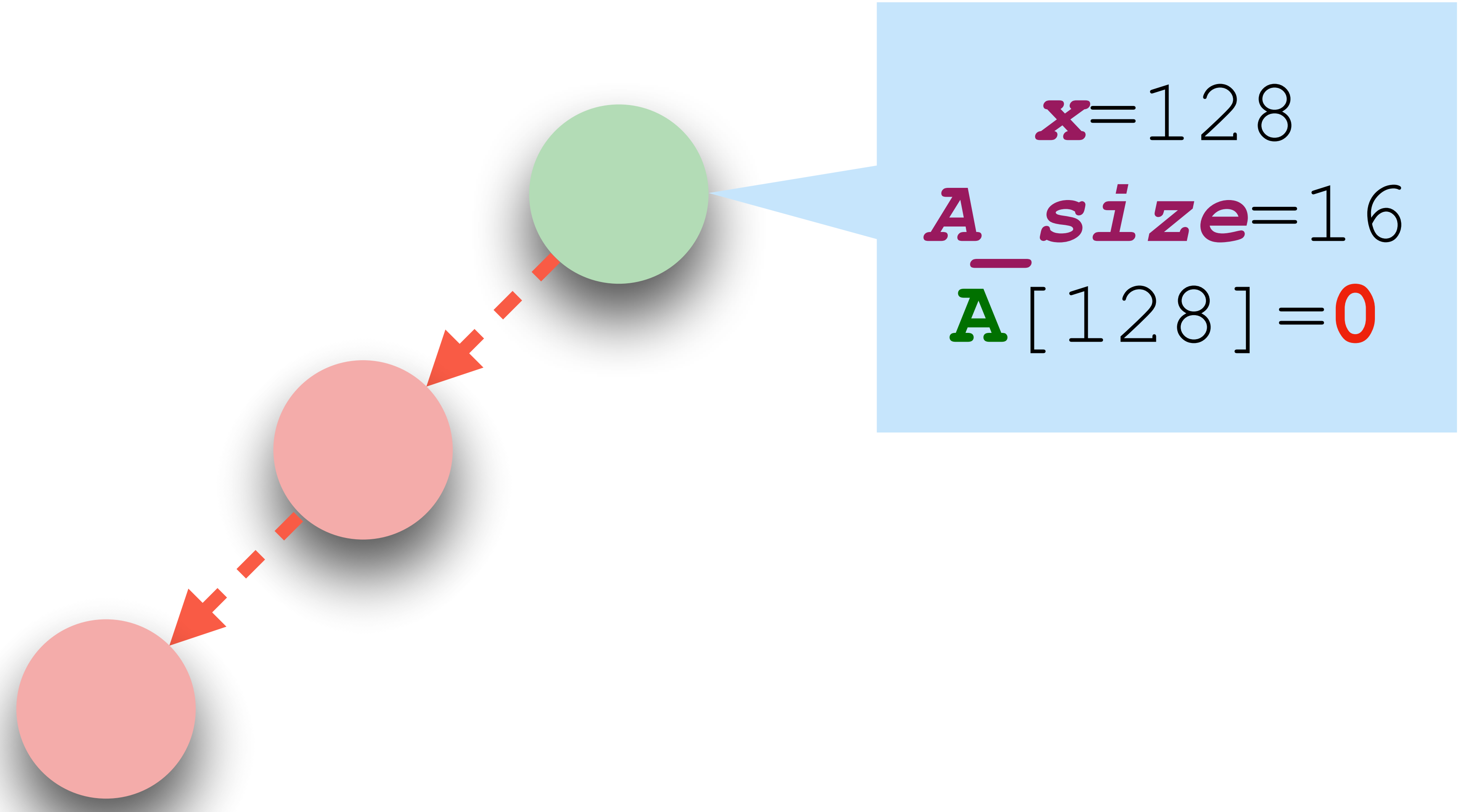

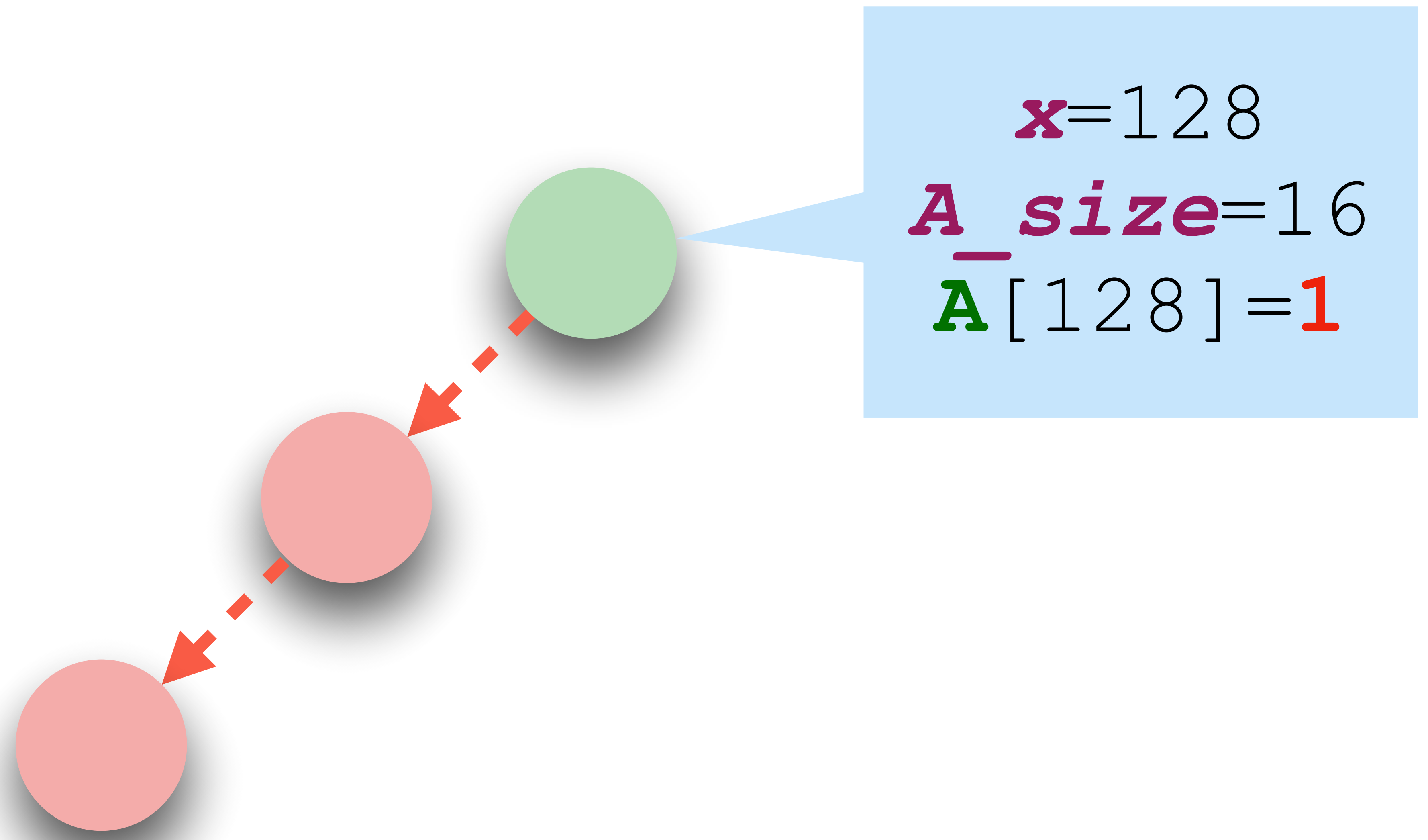

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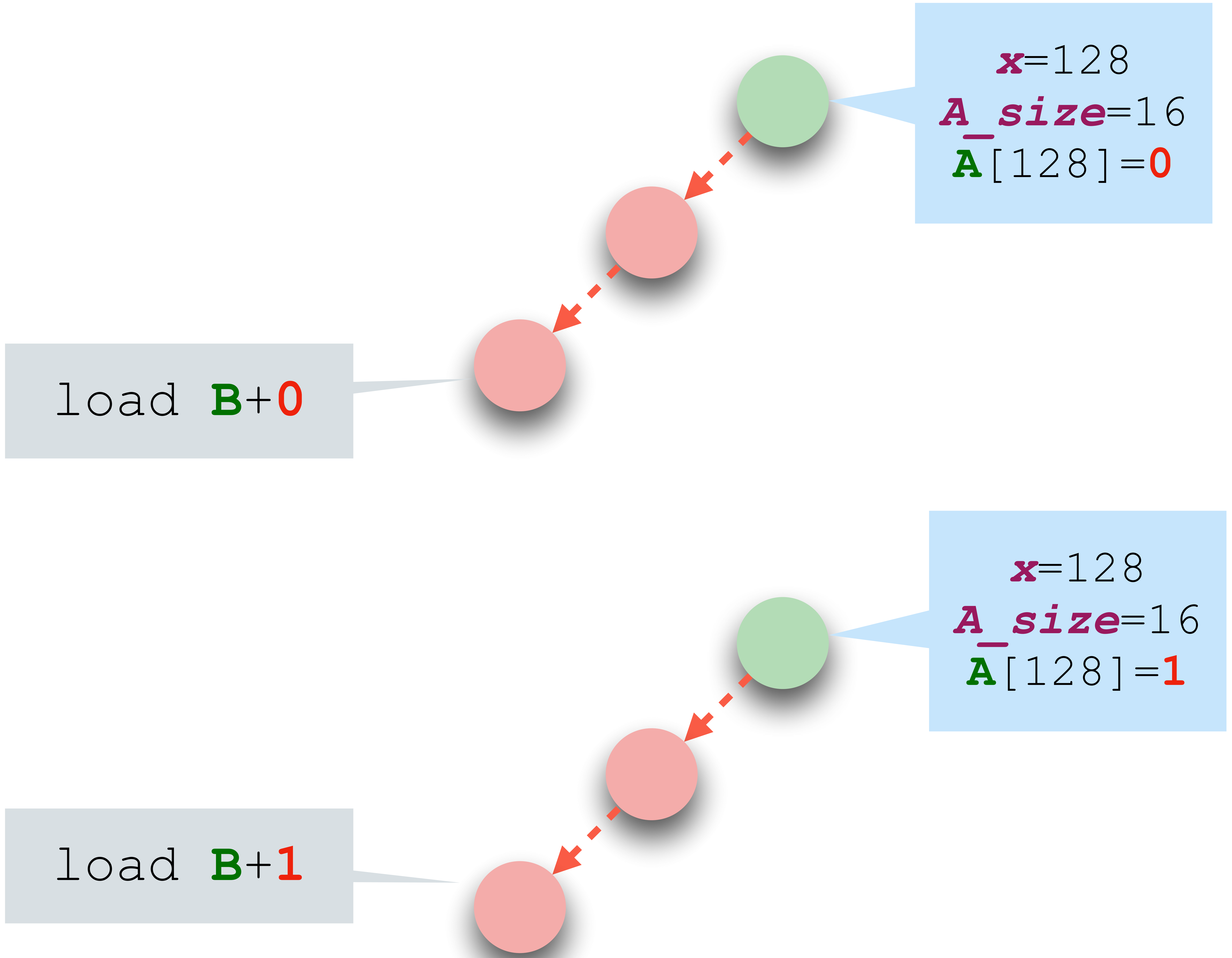

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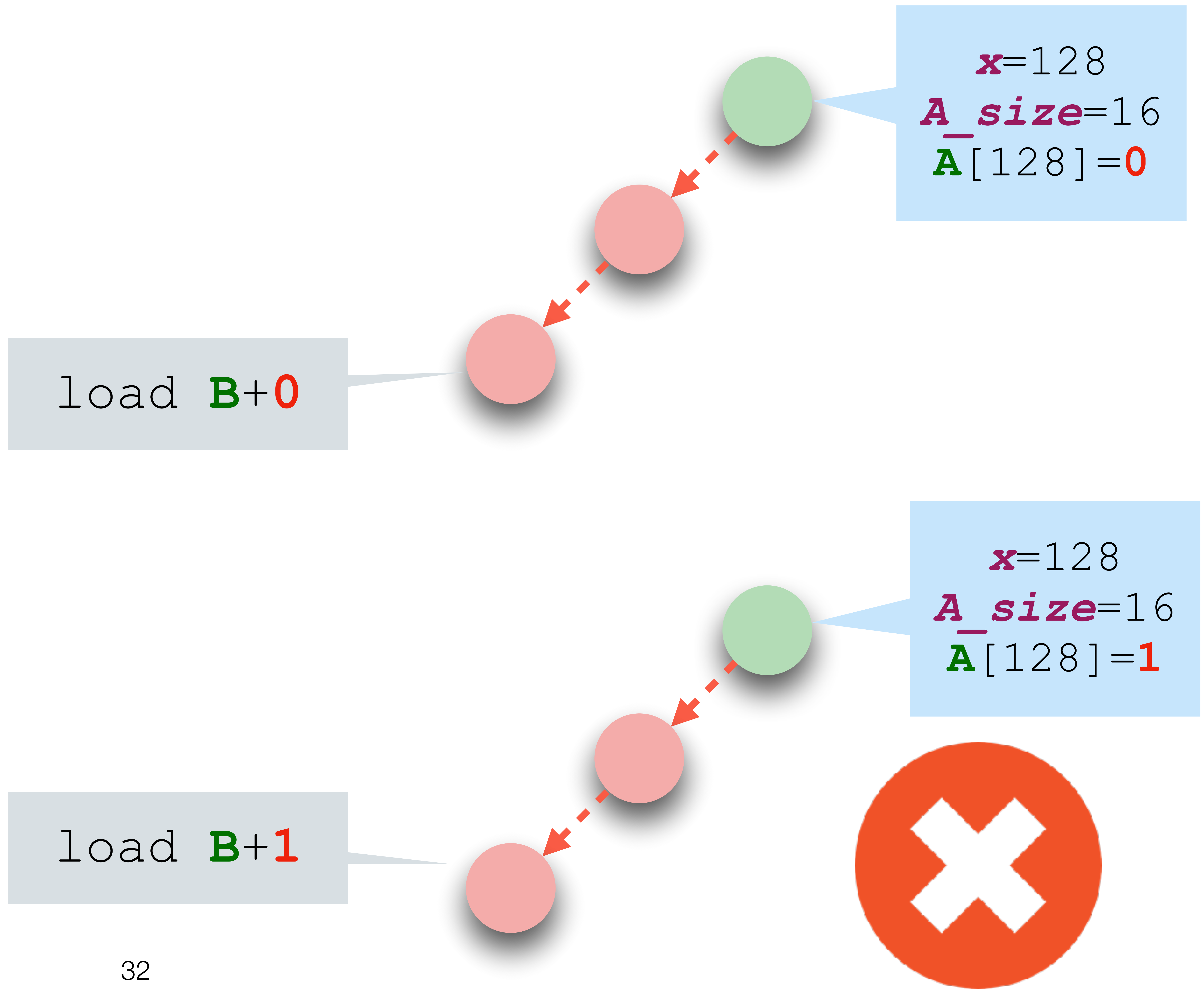

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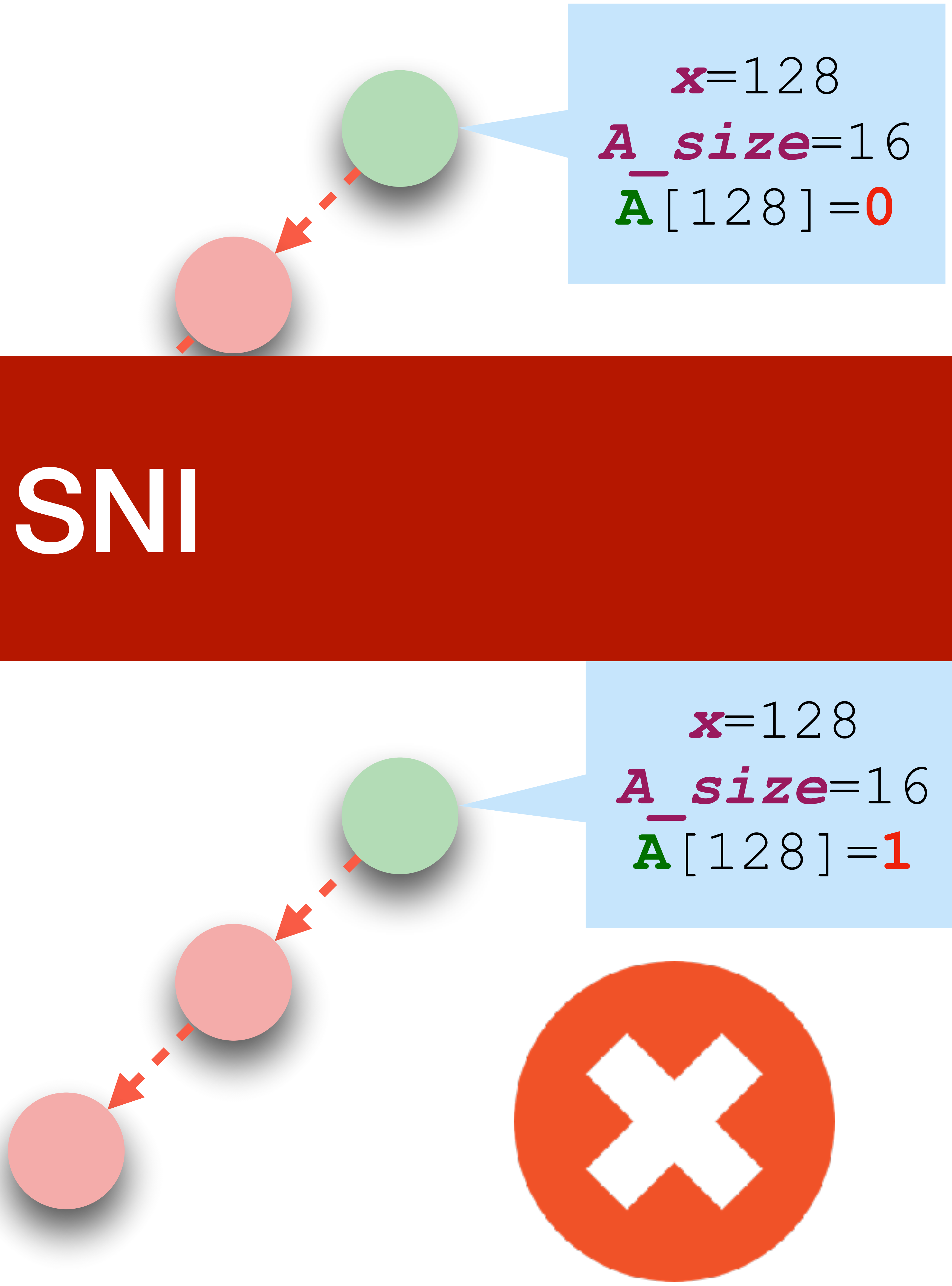


Spectre v1 violates SNI

🟩 Non-speculative

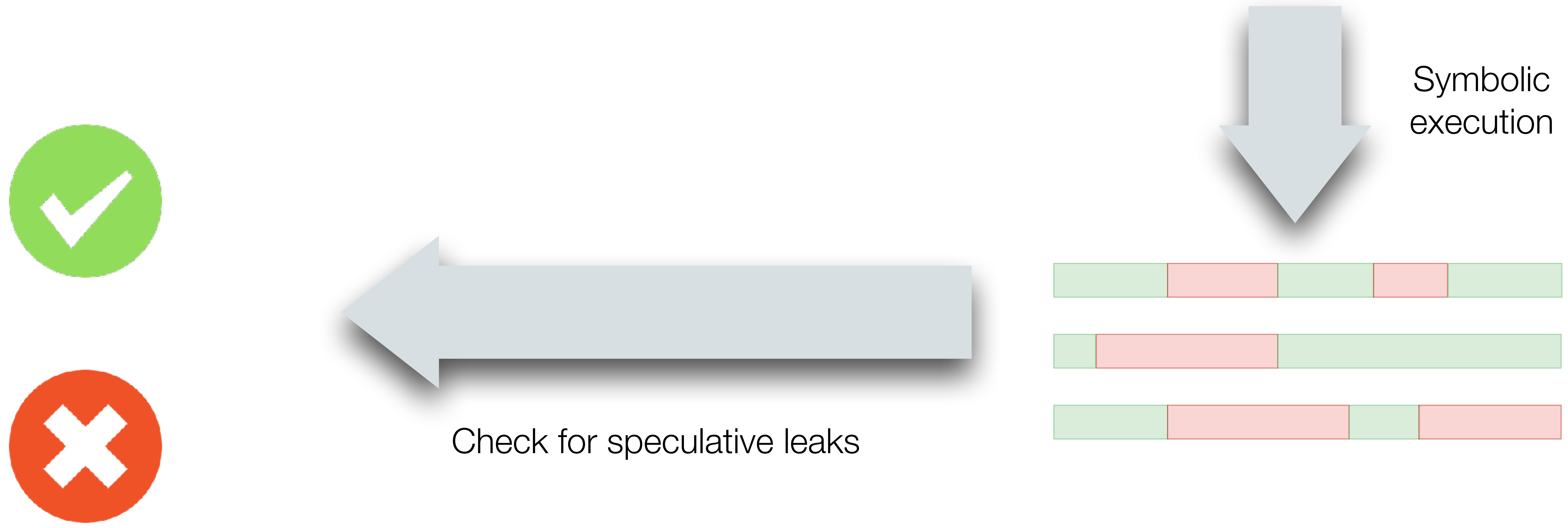
🟥 Speculative

Detecting speculative leaks

```
        mov     rax, A_size
        mov     rcx, x
        cmp     rcx, rax
        jae     END
    L1: mov     rax, A[rcx]
        mov     rax, B[rax]
```

x64 to µASM

```
              rax <- A_size
              rcx <- x
              jmp rcx≥rax, END
        L1:   load rax, A + rcx
              load rax, B + rax
        END:
```



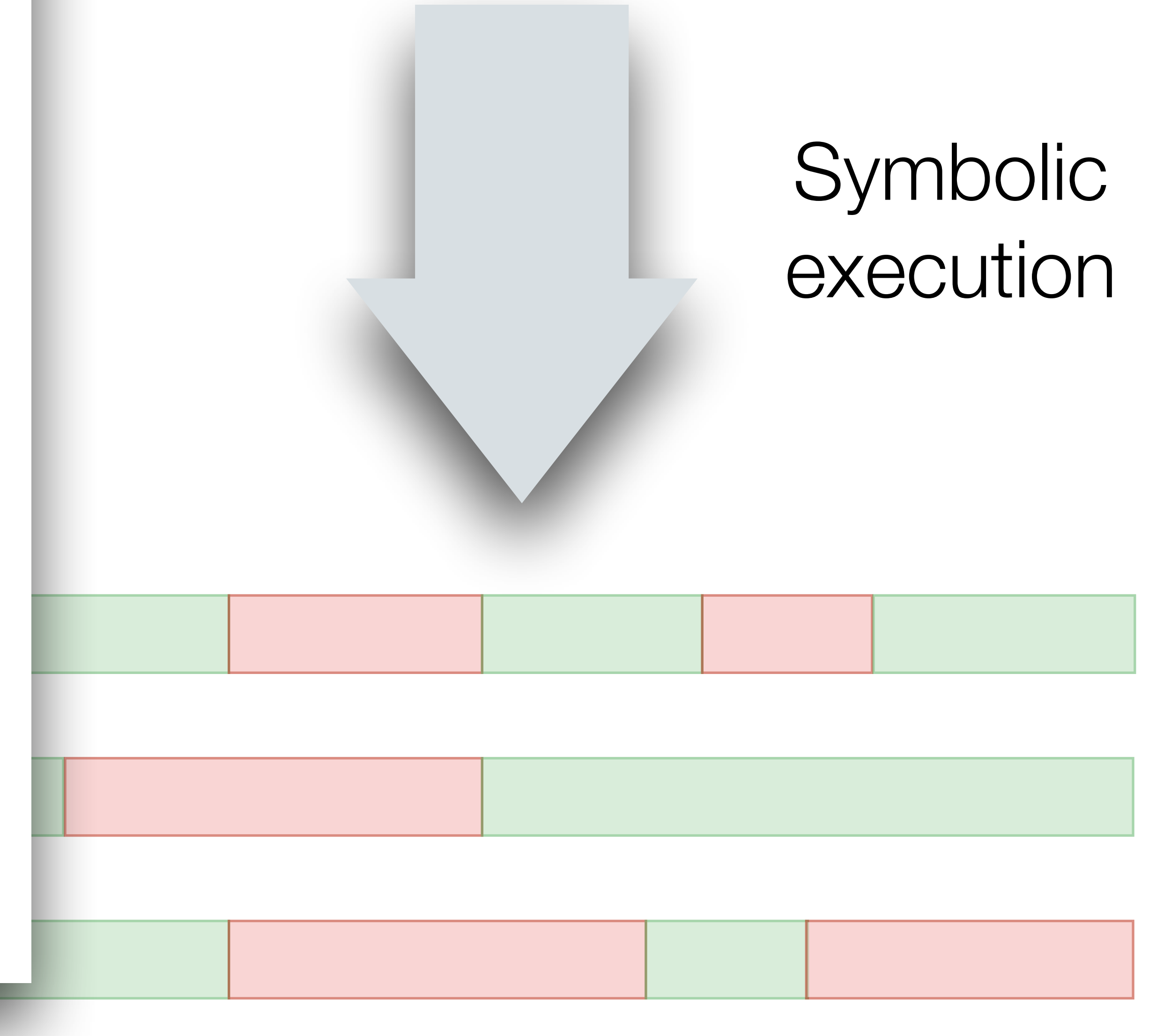
Detecting speculative leaks

```
    mov    rax, A_s
    mov    rcx, x
    cmp    rcx, rax
    jae    END
L1: mov    rax, A[r
    mov    rax, B[r
```

```
rax <- A_size
rcx <- x
jmp rcx≥rax, END
load rax, A + rcx
load rax, B + rax
```

Spectector

https://spectector.github.io



Check for speculative leaks

Case study: compiler mitigations

Patrignani, Guarnieri — Exorcising spectres with secure compilers — CCS 2021
https://arxiv.org/abs/1910.08607

Case study: compiler mitigations

Injection of LFENCEs

LFENCE ***stops*** speculation

Compilers (***ICC***, ***MSVC***) insert LFENCE after ***branch instructions***

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```

ICC enforces ***SNI*** (security proof) + unnecessary LFENCEs

MSVC is **insecure** — leaks checked with Spectector

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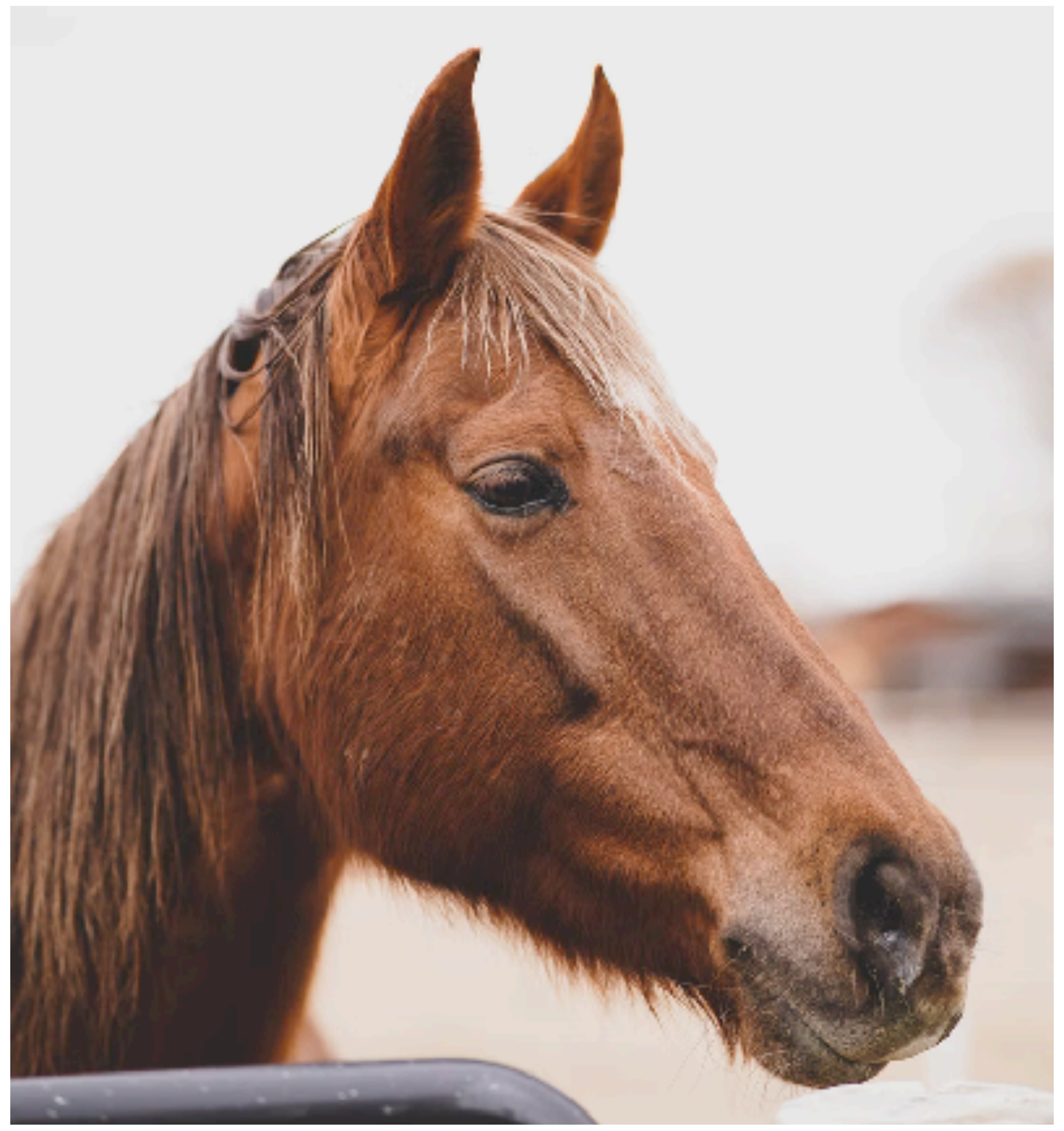
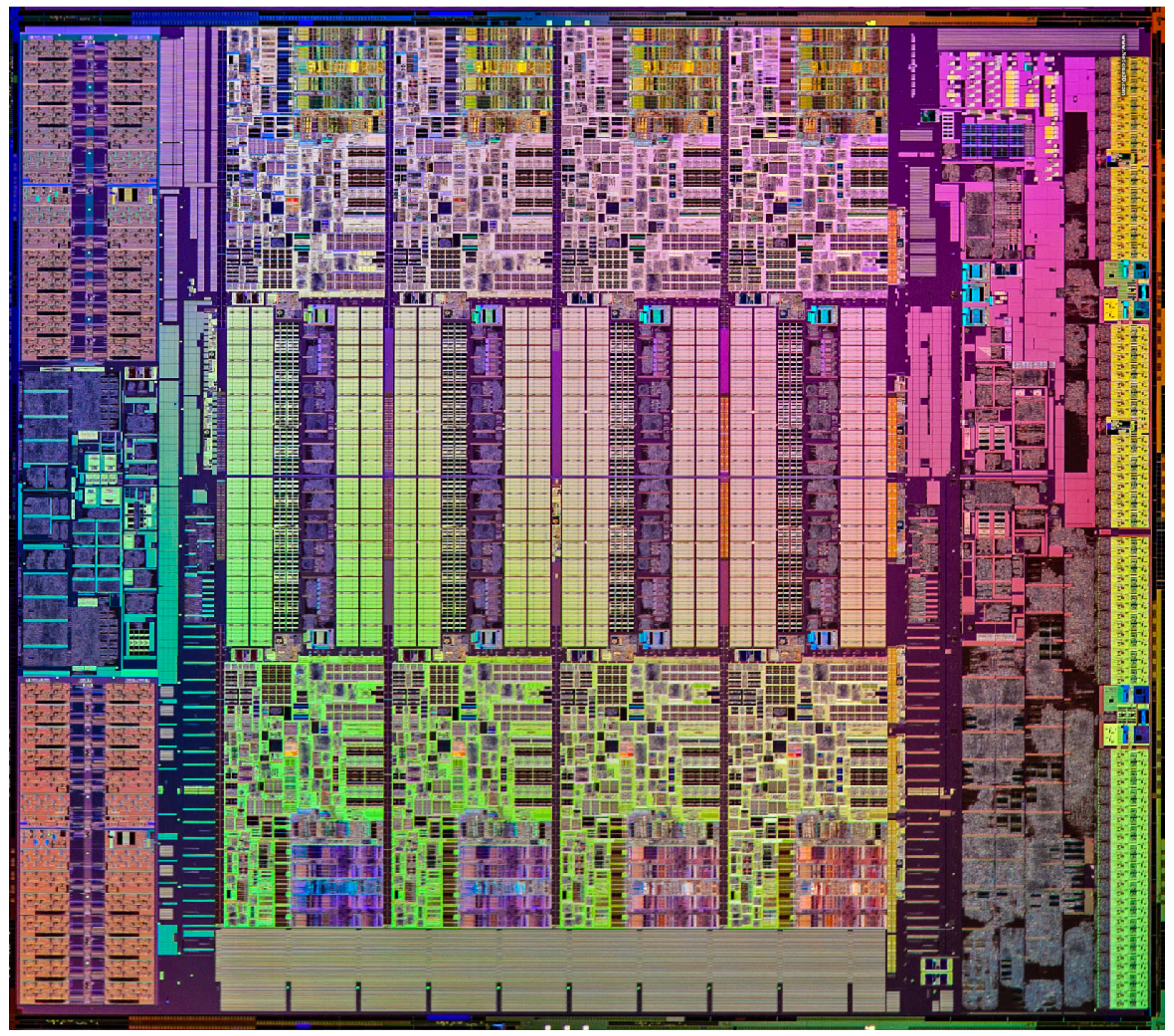
Outline

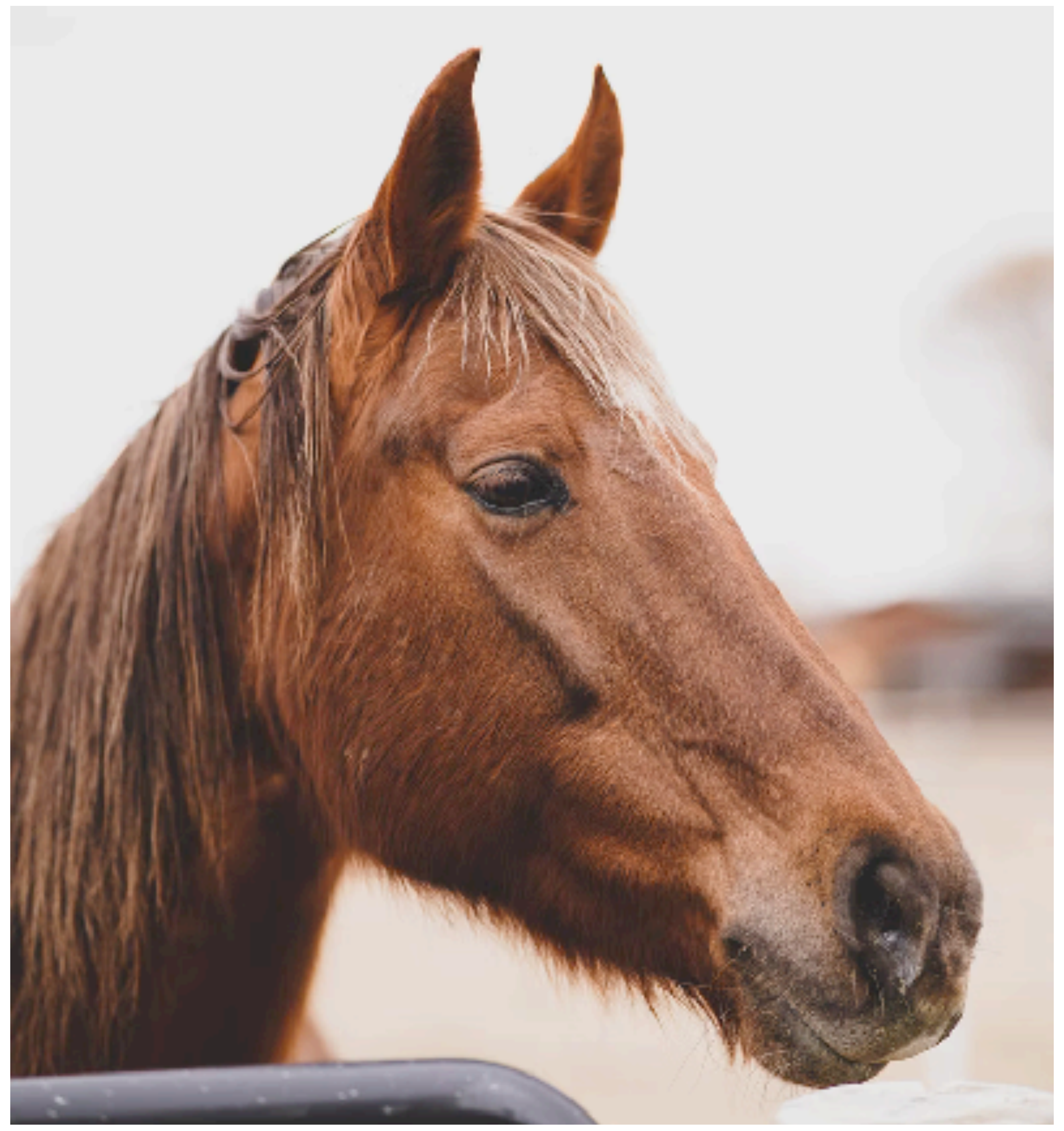
A problem of (missing) abstractions

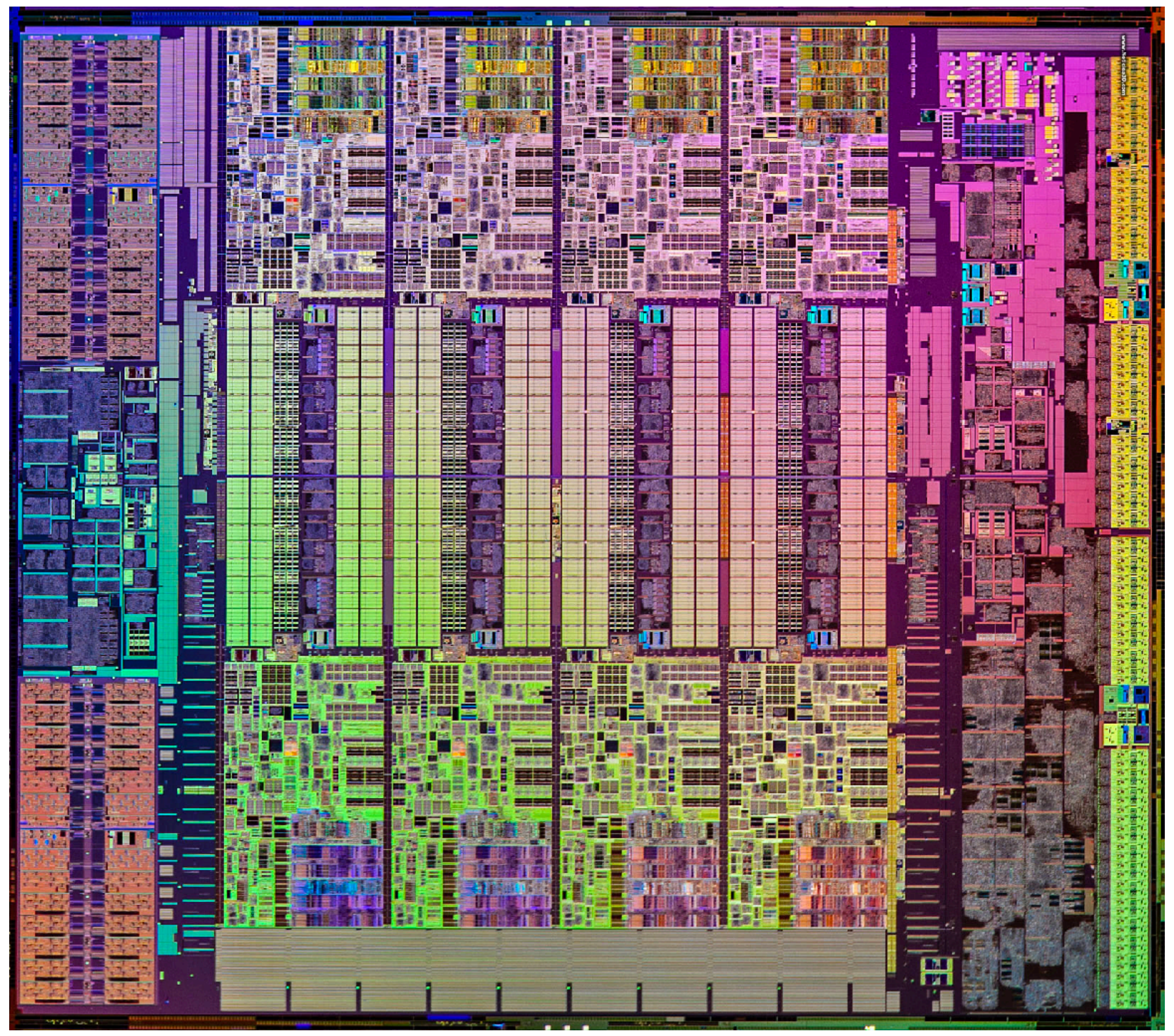


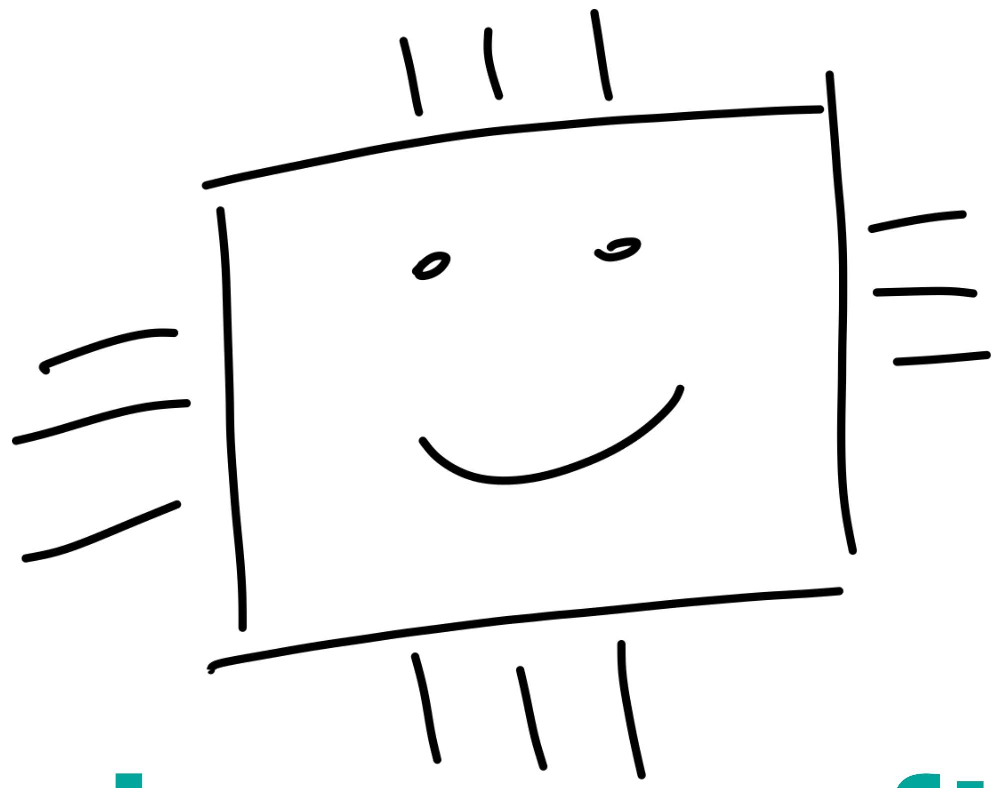


???

A problem of (missing) abstractions







Hardware-software contract

Challenges

We need ***precise*** and ***simple*** **hardware-software contracts** for ***security***

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Challenge 3: Contract-aware analysis and secure compilation techniques to enforce program security

Collaborators

- Boris Köpf @ Microsoft Research
- Jan Reineke @ Saarland University
- José F. Morales @ IMDEA Software
- Pepe Vila @ IMDEA Software
- Andrés Sánchez @ IMDEA Software
- Marco Patrignani @ University of Trento

Supported by Intel Strategic Research Alliance (ISRA) "Information Flow Tracking across the Hardware-Software Boundary"

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