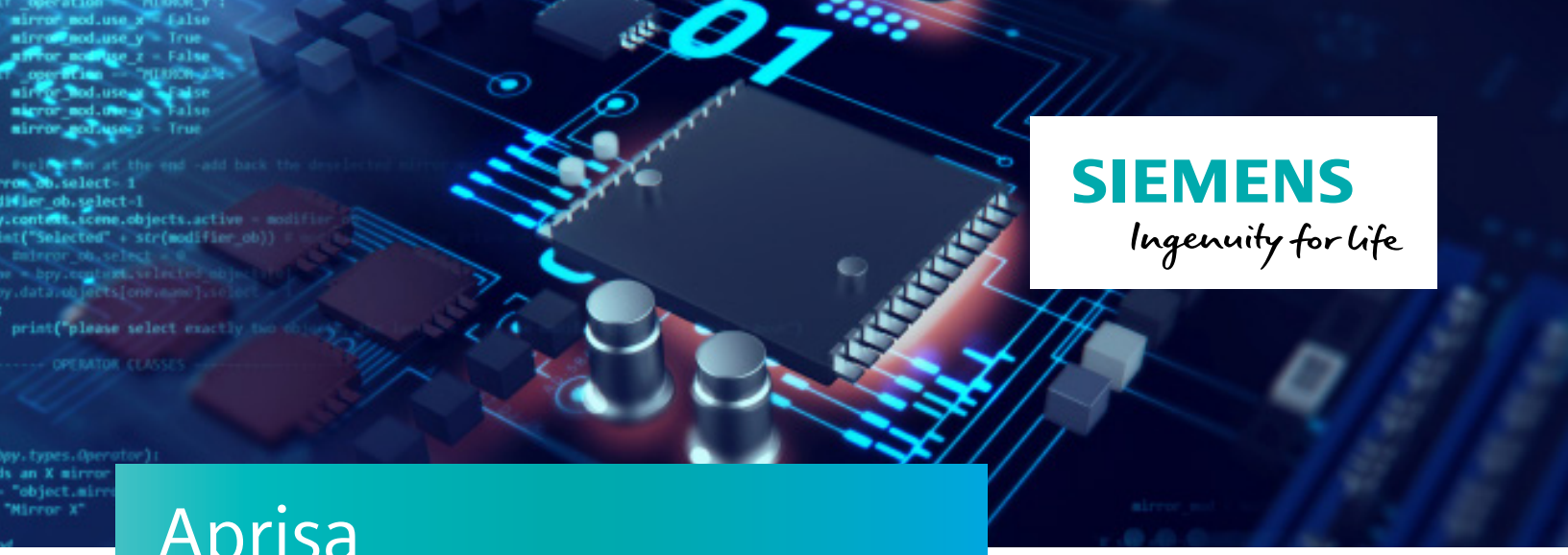


SIEMENS
Ingenuity for life

Aprisa

Place-and-route solution

Benefits

- Reduces time to design closure by more than 2X over the competition
- Delivers 25% better timing, 15% better power consumption, and 10% better die-size than competition
- Is easy to adopt and has the lowest overall cost of ownership
- Worldwide customer-proven with hundreds of successful tape-outs

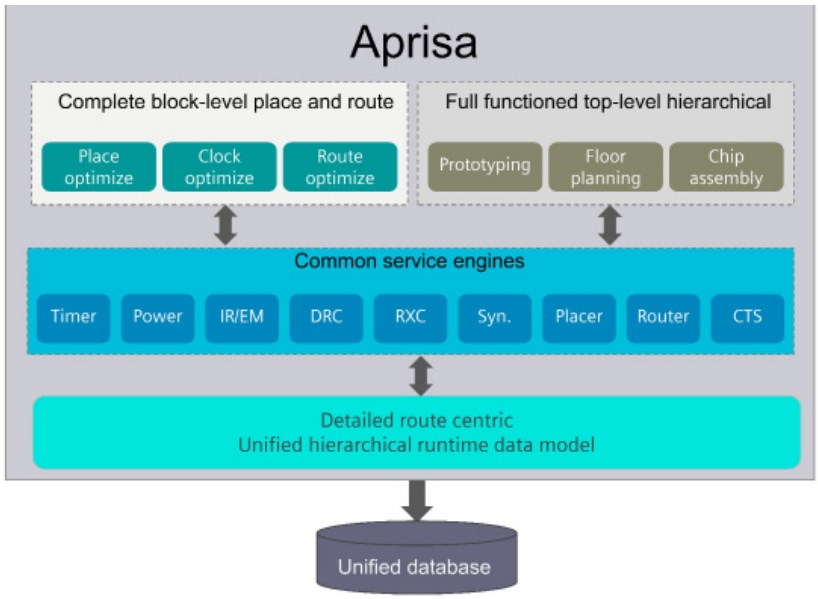
Features

- Uses a unique detailed-route-centric architecture with unified hierarchical runtime data model
- Includes patented technologies for superior timing, power and die size
- Certified by leading foundries and ready for designs at advanced process nodes down to 7 nm
- Is interoperable with popular digital design flows with support of standard input/output formats
- Includes highly signoff-correlated analysis engines.
- Easy GUI and scripting support

The detailed route-centric solution

Aprisa is an automatic digital place-and-route (P&R) system that offers complete functionalities for both top-level hierarchical design and block-level physical implementation for complex digital IC design projects. It includes cutting-edge technologies in proto-typing, floor-planning, chip-assembly, placement, clock tree synthesis, routing, optimization and embedded analysis engines. Aprisa supports standard data inputs and outputs, such as Verilog, SDC, LEF/DEF, Liberty, UPF, and GDSII.

The core of the technology is the detailed-route-centric architecture and hierarchical database, specifically developed to address the design challenges with advanced FinFET technology. Because routability impacts the design from the very beginning, the Aprisa router-based architecture, with its tightly integrated functions, is able to achieve fast design closure. Aprisa eliminates front-to-back iterations and results in optimal quality-of-results (performance, power, reliability, chip-area) with competitive runtime.



Aprisa represents a place-and-route paradigm shift.

Aprisa

Near-signoff timing analysis – Advanced industry standard on-chip-variation (OCV) methods, including LVF.

Color-aware DPT routing – Patented routing technology uses correct-by-construction implementation to guarantees no double-patterning technology violations during DRC signoff.

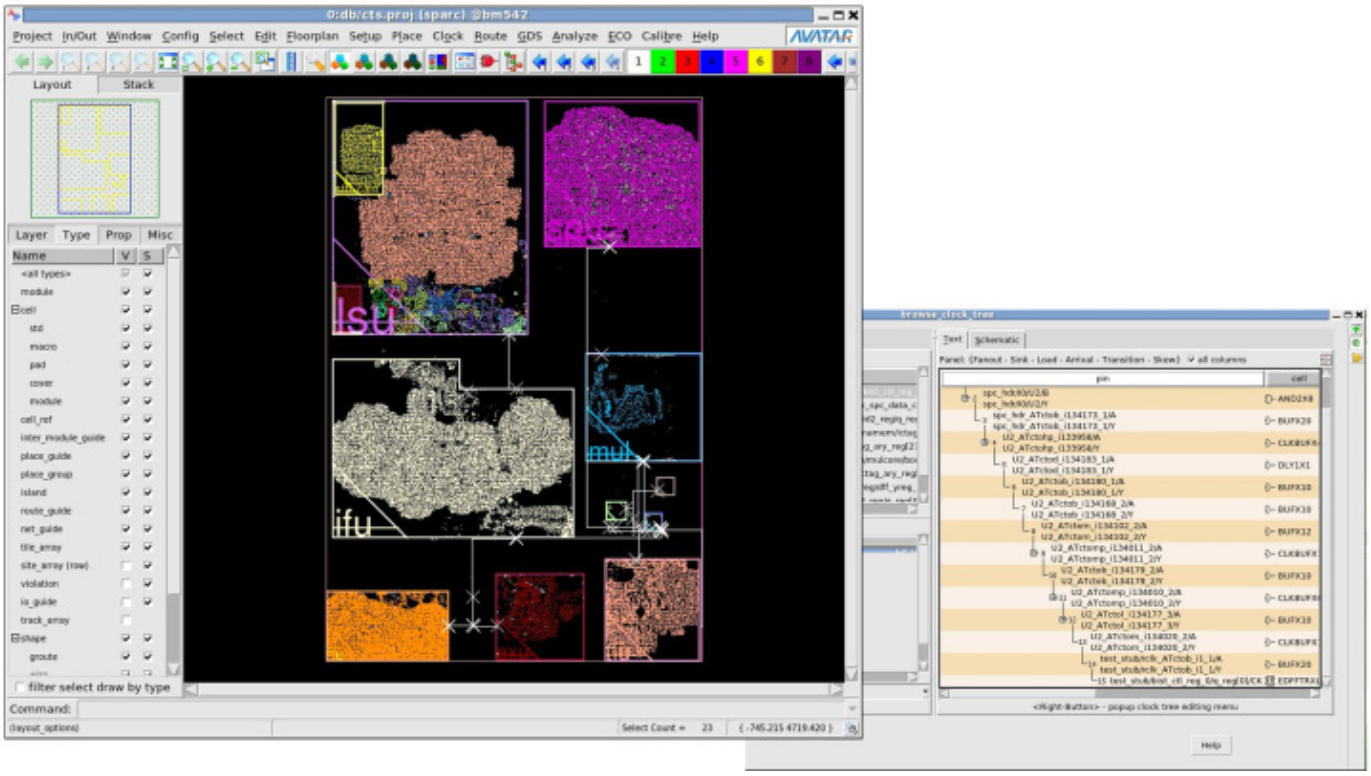
Congestion-aware low-R routing – Precise estimation of congestion and timing during placement optimization to assign timing critical net to higher layers that has lower resistance for better timing.

IR-aware P&R – Automatically detects and avoids potential IR hotspots during placement.

EM-aware routing – Supports all EM rules of advanced process nodes, with integrated EM checking and fixing during routing.

Low power-driven optimization – Native support of both UPF and CPF with leakage and dynamic power driven optimization

Foundry support – Certified by leading semiconductor foundries for designs at advanced process node



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