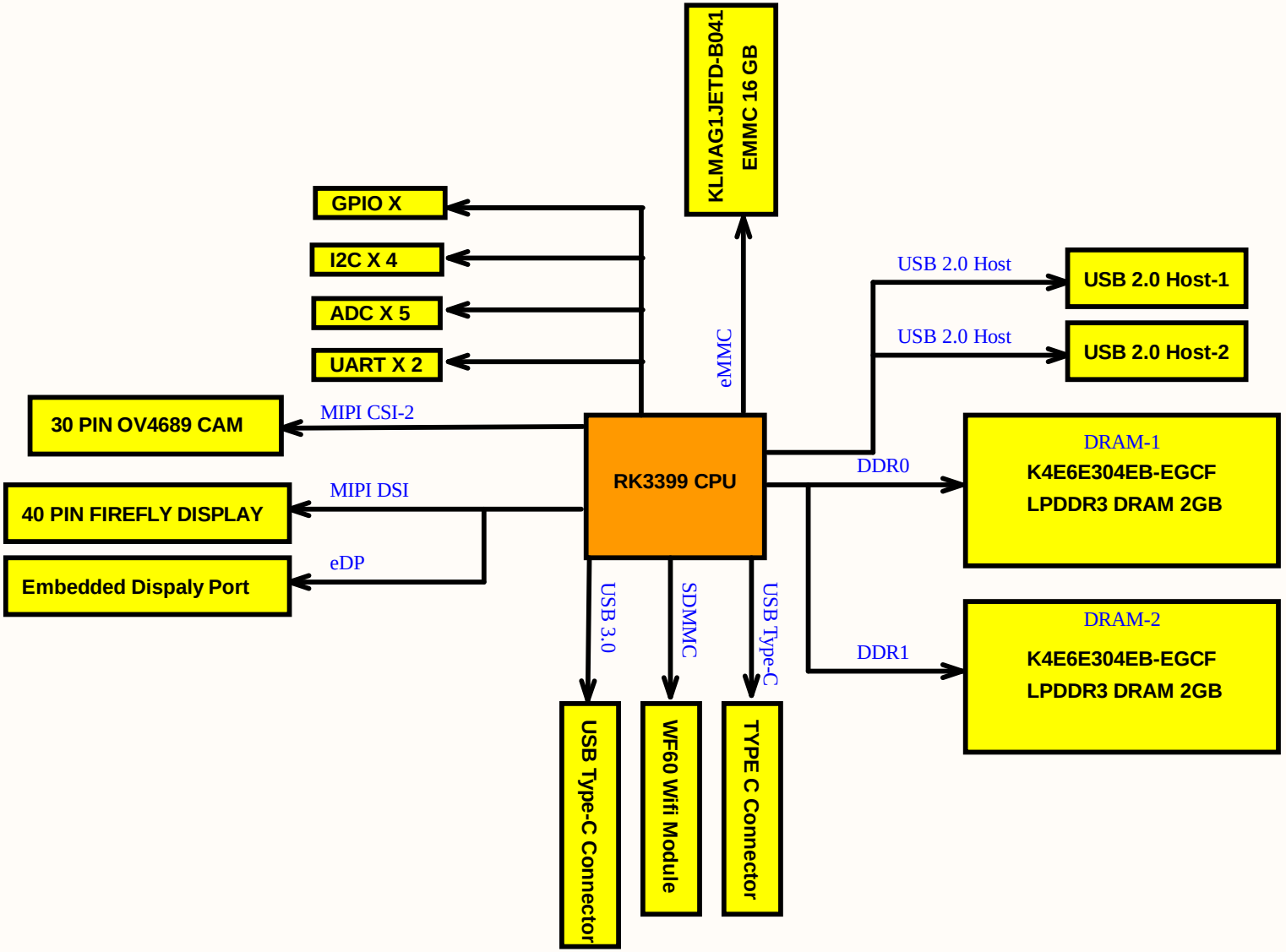
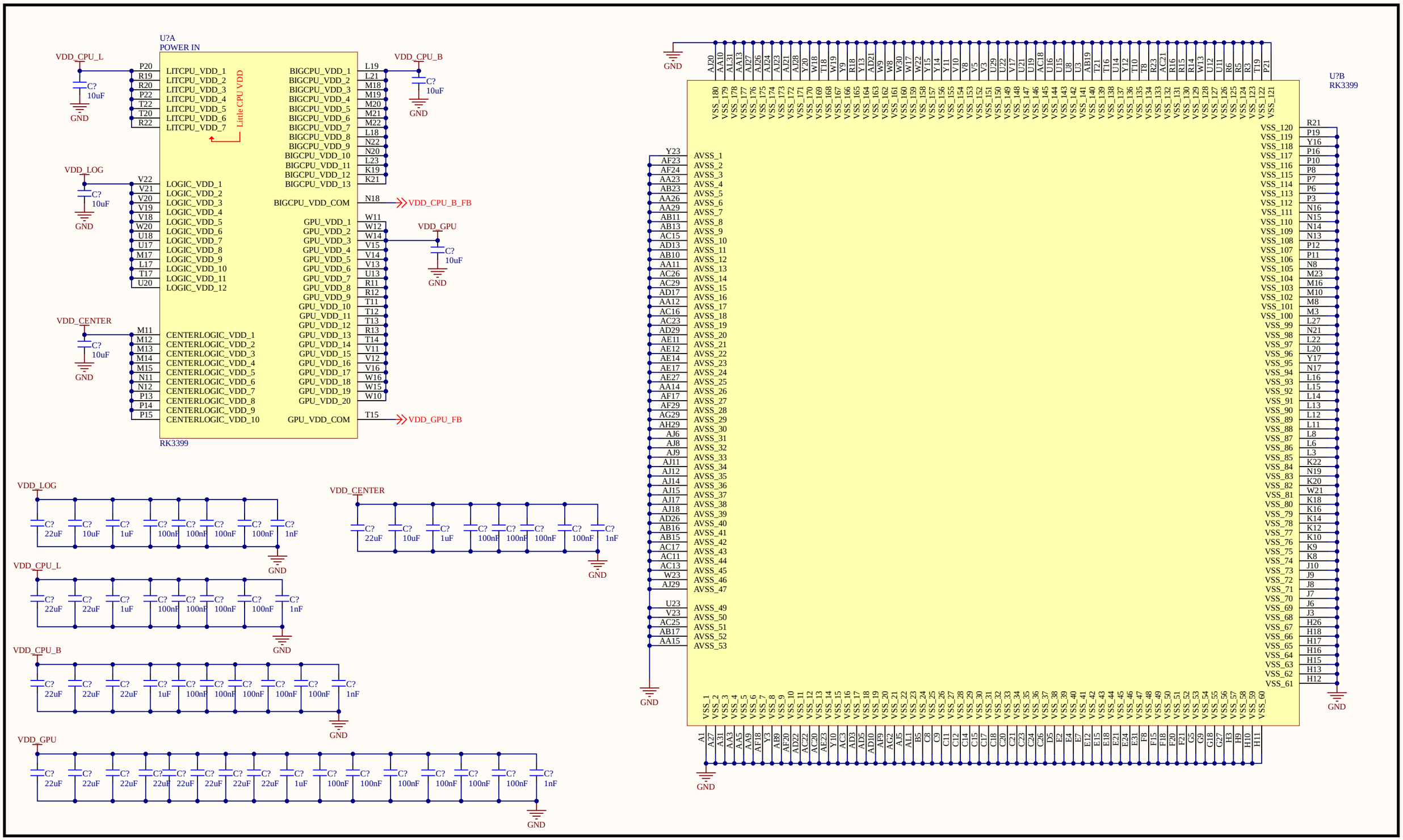


TITLE:	**RK3399 SOM Board Design V1.0**		
DOCUMENT NAME:	**[0]- Block Diagram.SchDoc**		
PROJECT CODE:	**A_V1.0**	Sheet **1** of **12**	
SCALE 1:1	TEMPLATE: A4	AUTHOR: AVIRAL MISHRA	

ESTEEM PCB

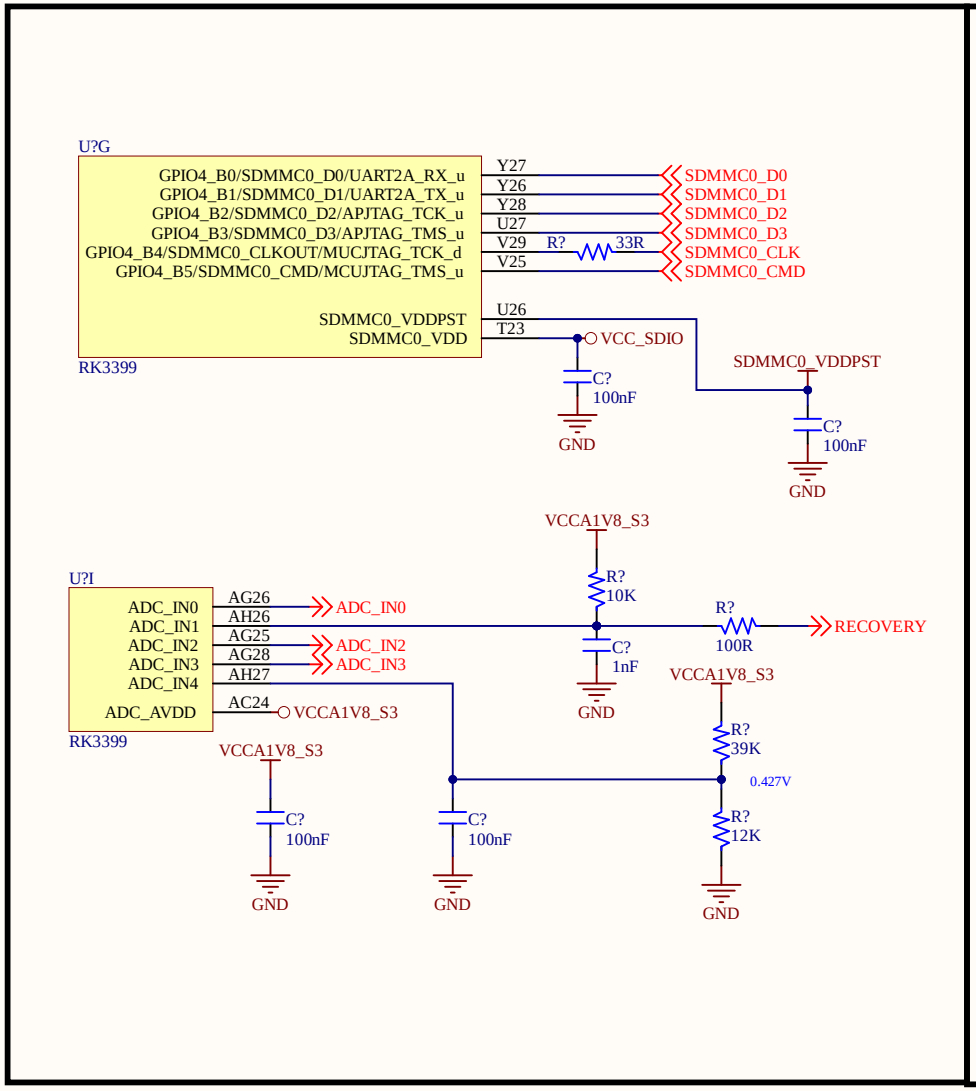
Power Page of CPU

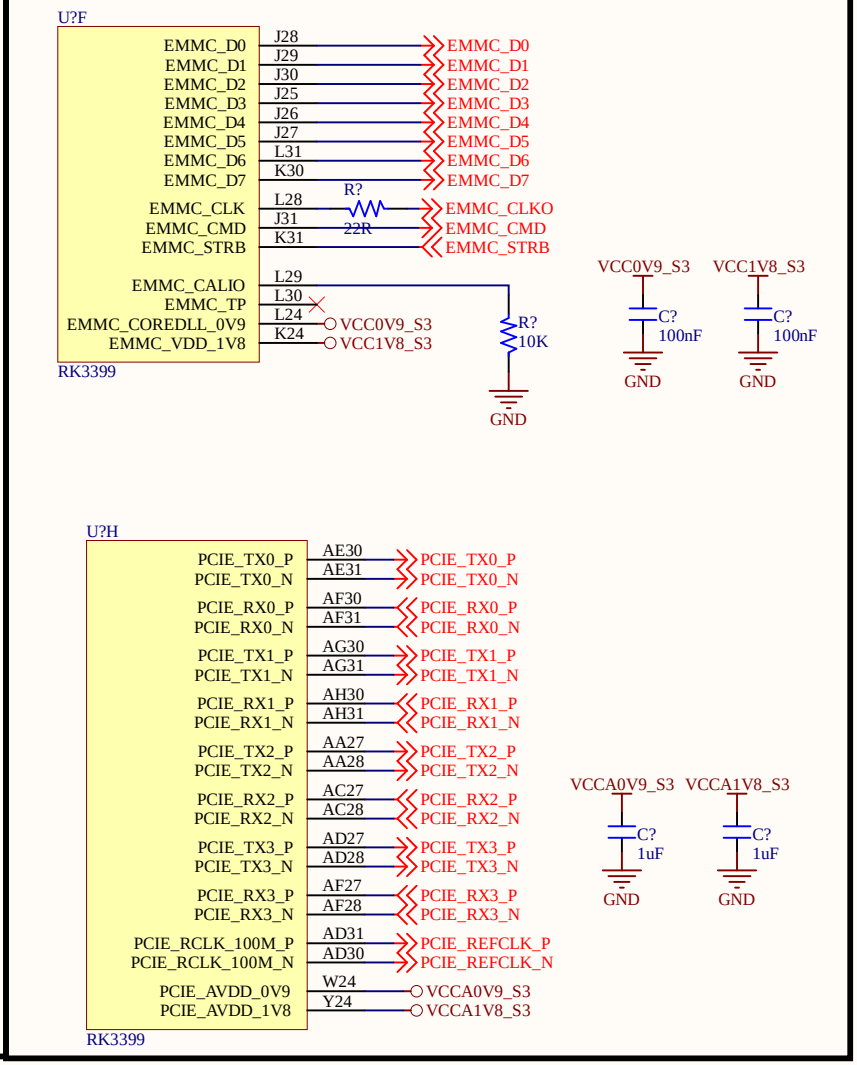


TITLE:	**RK3399 SOM Board Design V1.0**		
DOCUMENT NAME:	**[1]-Power Pins Page of RK3399.SchDoc**		
PROJECT CODE:	**A_V1.0**	Sheet	**2** of **12**
SCALE 1:1	TEMPLATE: A3	AUTHOR: ABC	

ESTEEM PCB

EMMC, SDMMC, PCIE and ADC of CPU

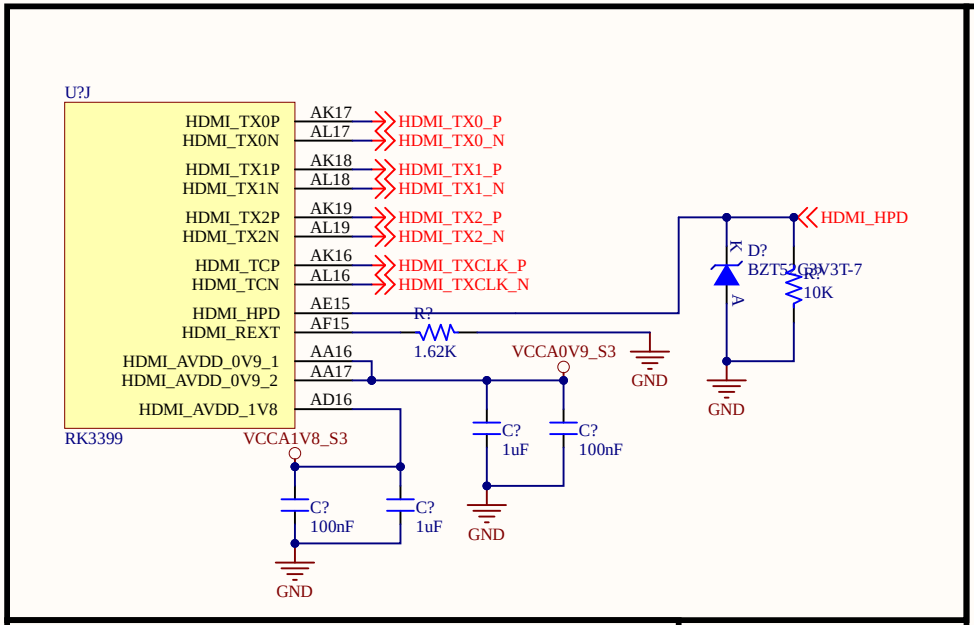


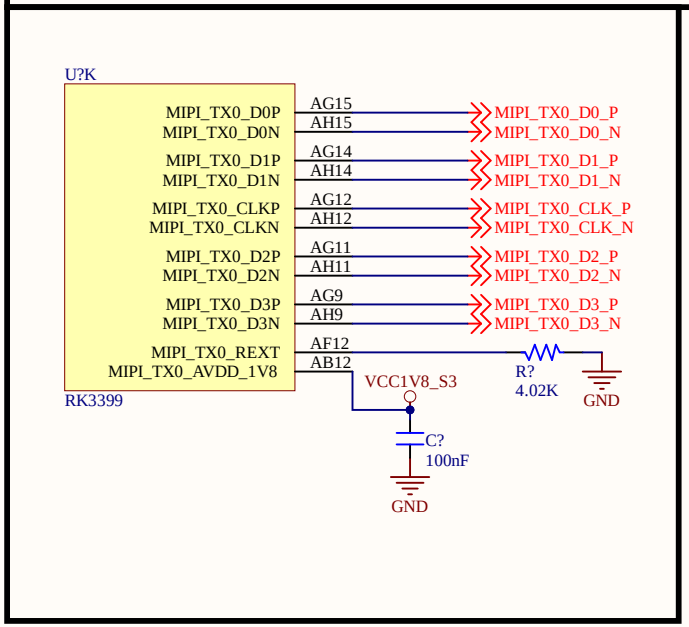


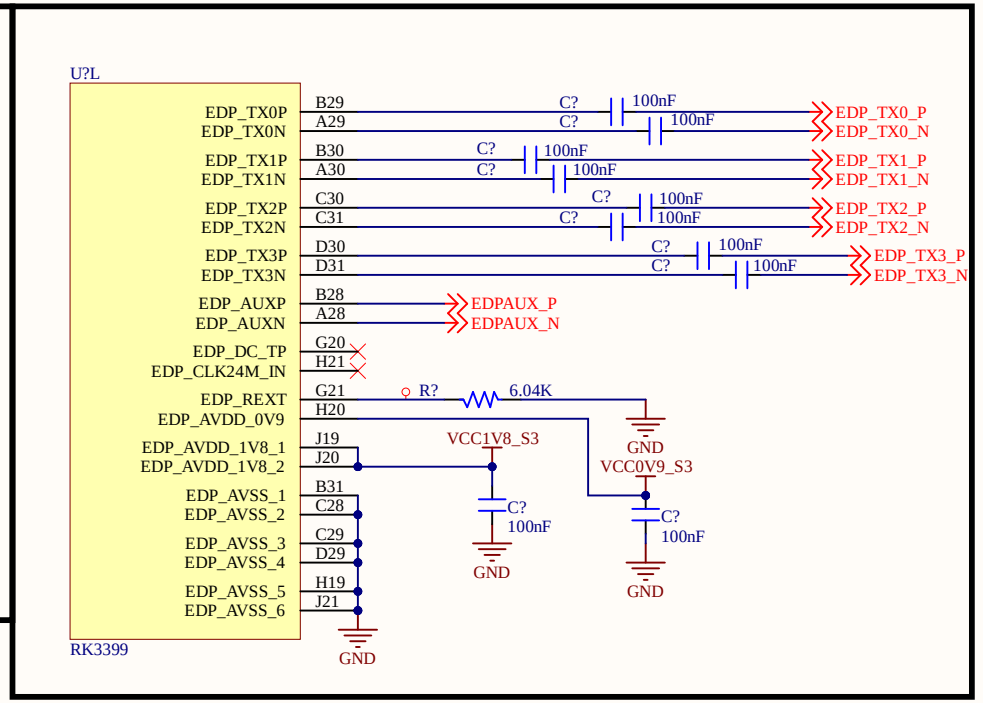
TITLE:	**RK3399 SOM Board Design V1.0**		
DOCUMENT NAME:	**[2]-RK3399_EMMC_ADC_PCIE.SchDoc**		
PROJECT CODE:	**A_V1.0**	Sheet **3** of **12**	
SCALE 1:1	TEMPLATE: A4	AUTHOR: AVIRAL MISHRA	

ESTEEM PCB

Display, HDMI and EDP of CPU



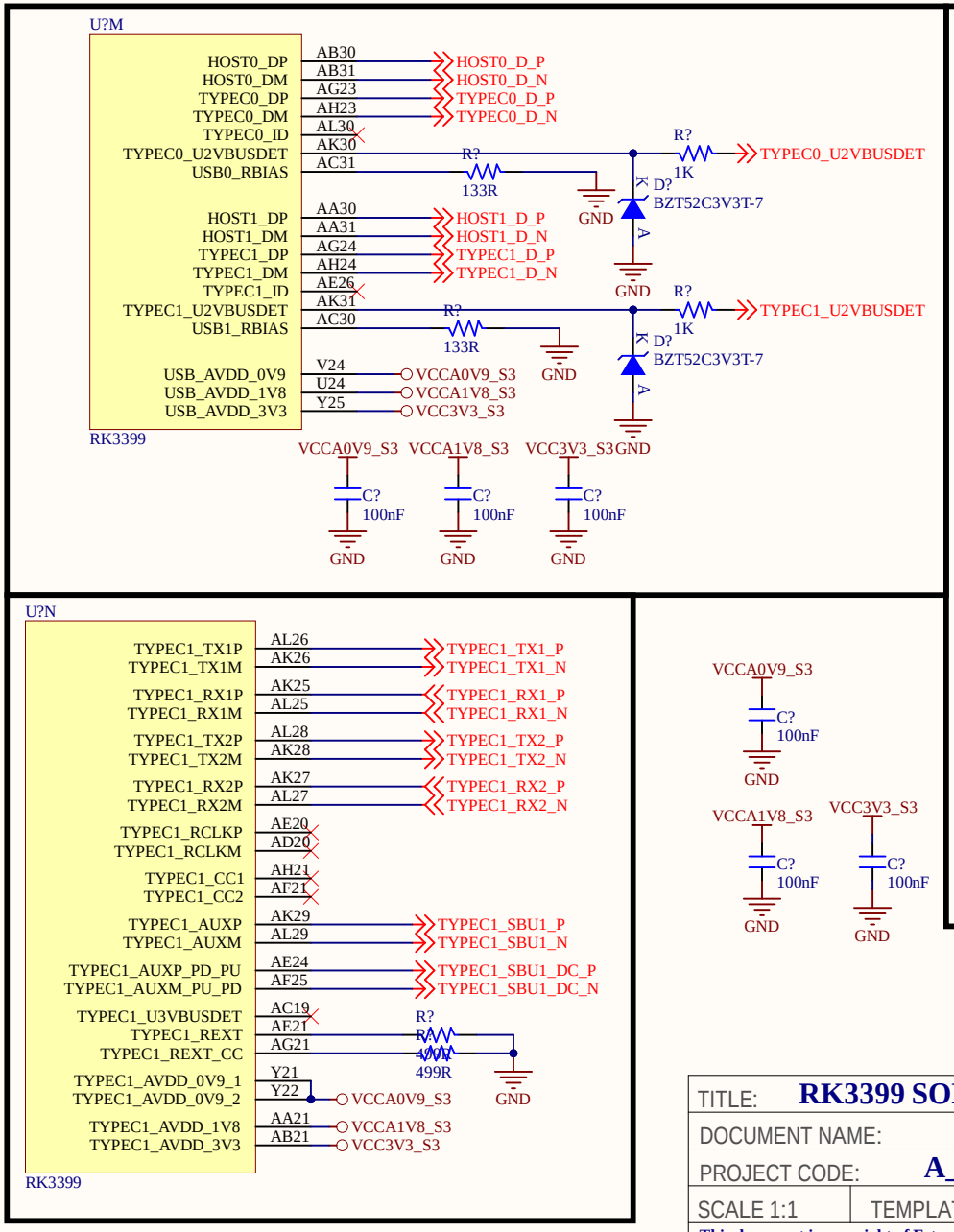


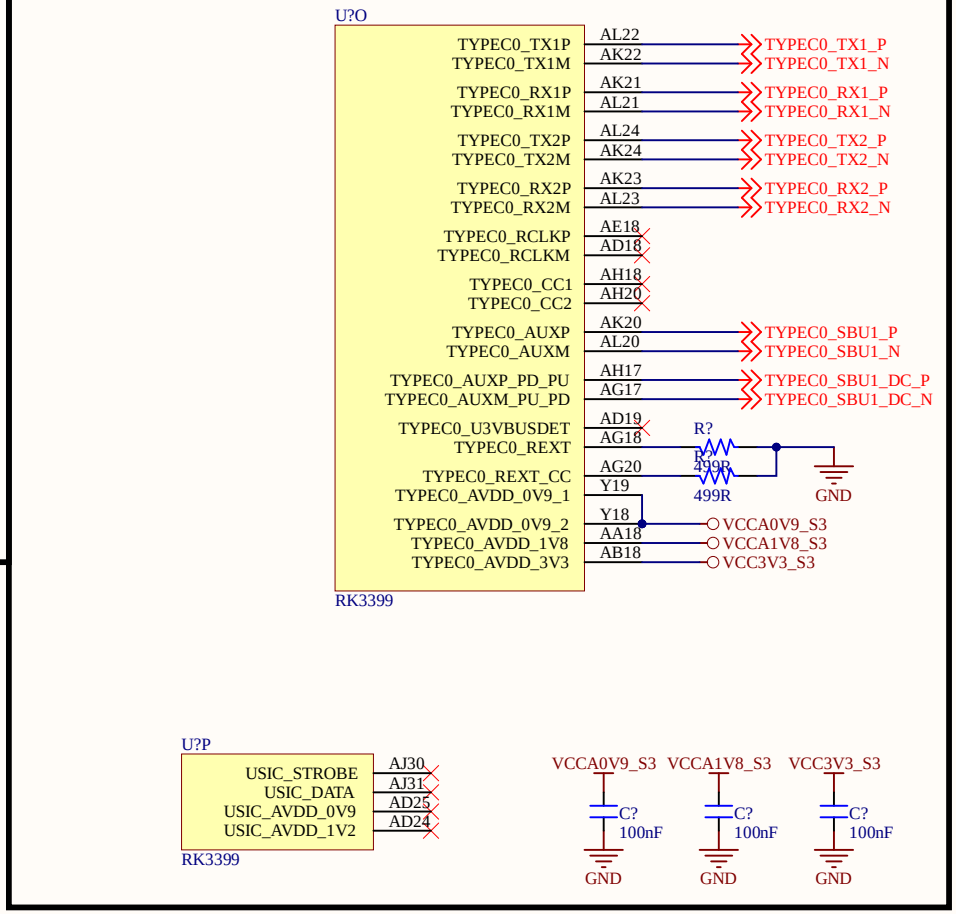


TITLE:	**RK3399 SOM Board Design V1.0**		
DOCUMENT NAME:	**[3]-RK3399 EDP_CSI_HDMI.SchDoc**		
PROJECT CODE:	**A_V1.0**	Sheet **4** of **12**	
SCALE 1:1	TEMPLATE: A4	AUTHOR: AVIRAL MISHRA	

ESTEEM PCB

USBs and USIC of CPU

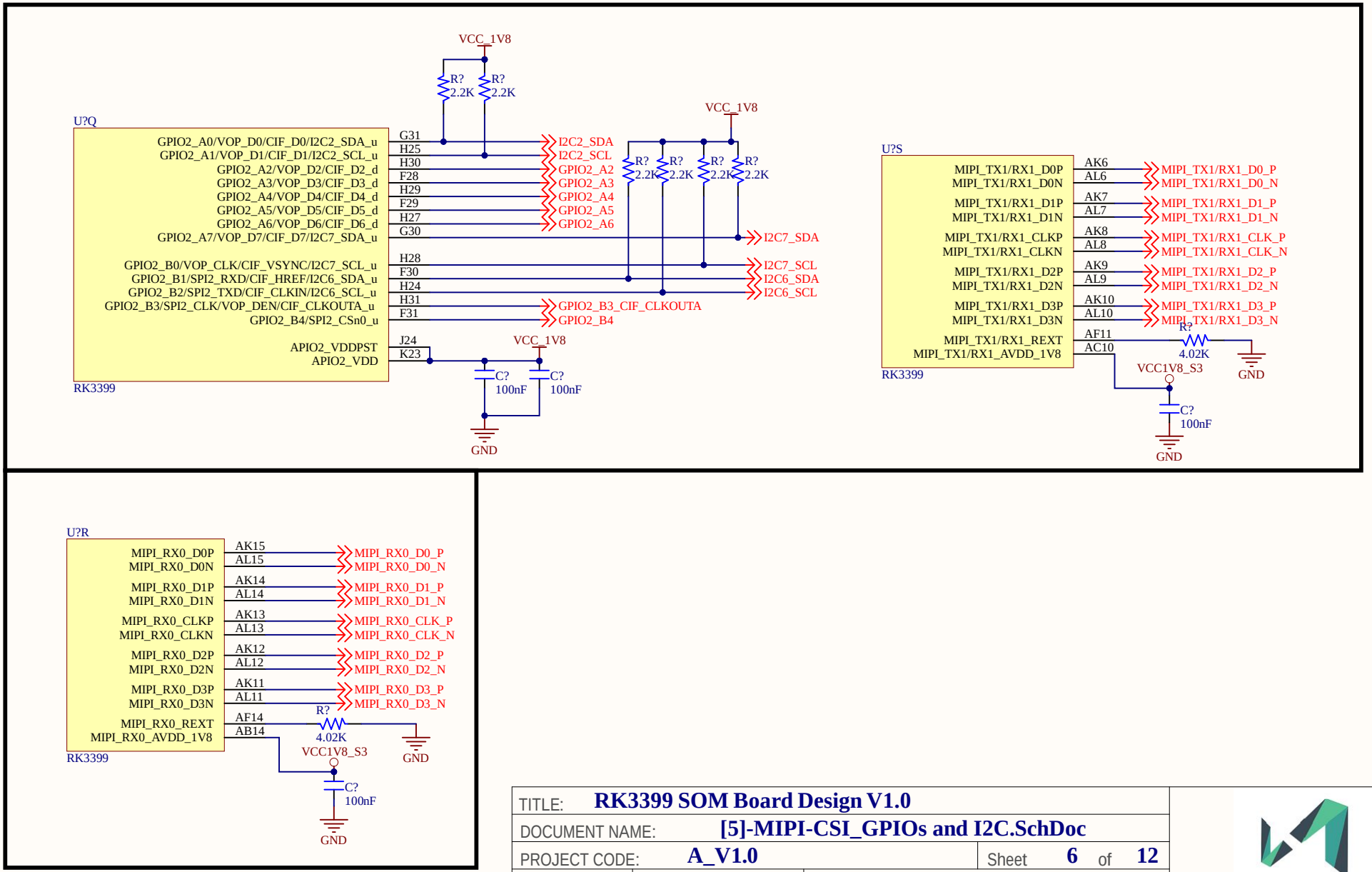




TITLE:	**RK3399 SOM Board Design V1.0**		
DOCUMENT NAME:	**[4]-USB2, TYPEC, USIC.SchDoc**		
PROJECT CODE:	**A_V1.0**	Sheet **5** of **12**	
SCALE 1:1	TEMPLATE: A4	AUTHOR: AVIRAL MISHRA	

ESTEEM PCB

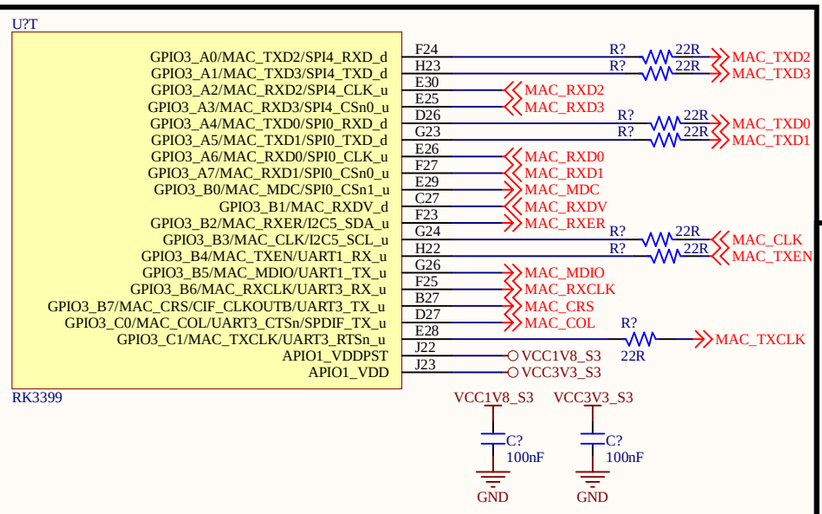
DVP MIPI CSI FOR CPU

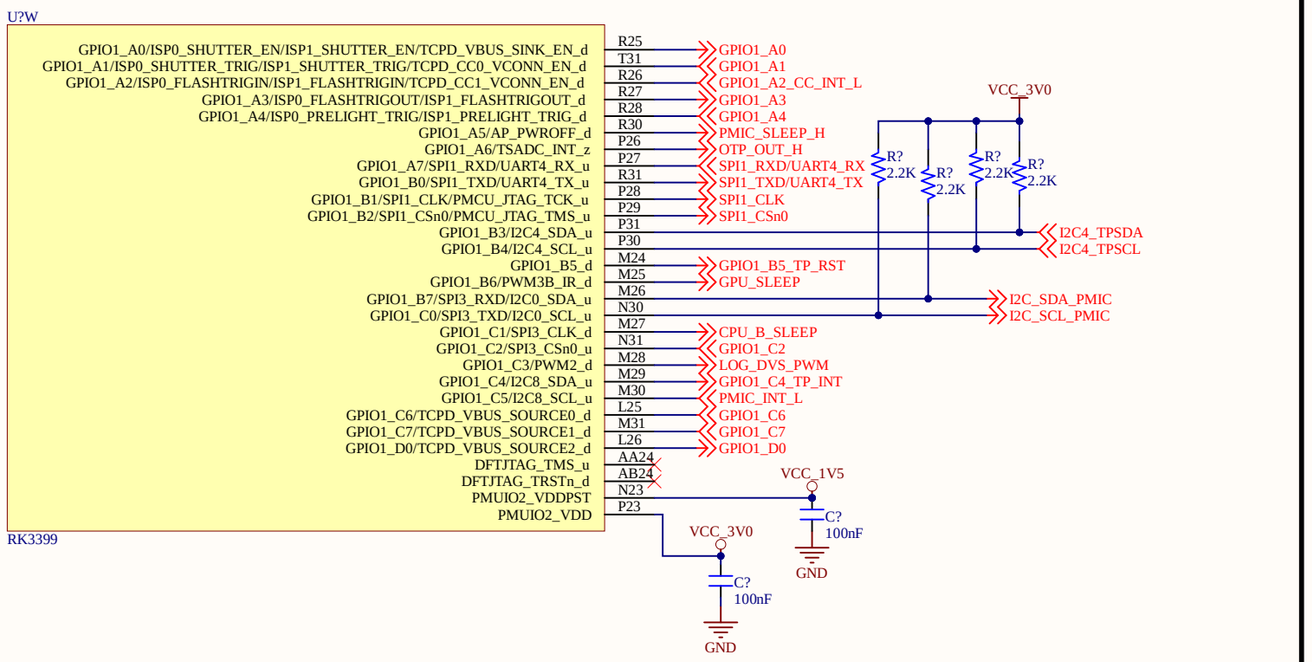


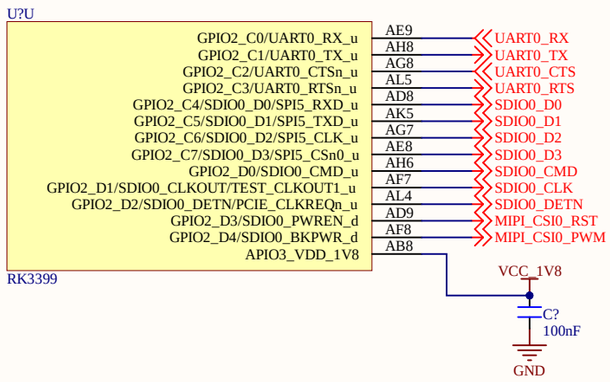
TITLE:	**RK3399 SOM Board Design V1.0**		
DOCUMENT NAME:	**[5]-MIPI-CSI_GPIOs and I2C.SchDoc**		
PROJECT CODE:	**A_V1.0**	Sheet **6** of **12**	
SCALE 1:1	TEMPLATE: A4	AUTHOR: AVIRAL MISHRA	

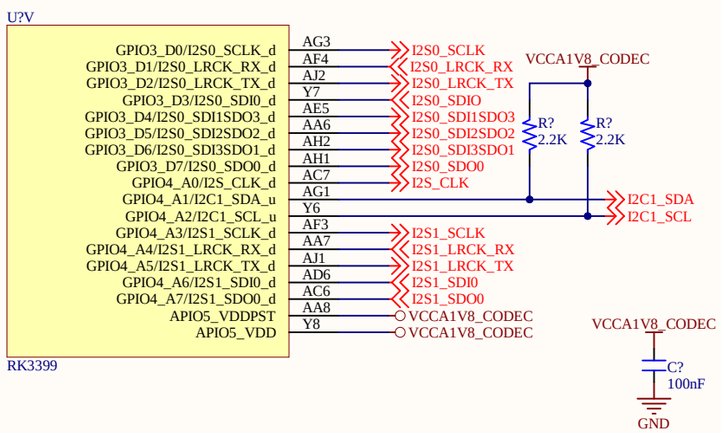
ESTEEM PCB

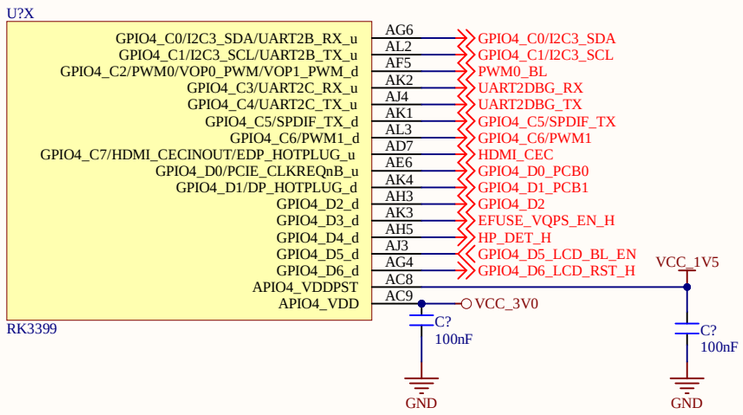
RGMII/SDIO AND SPI Part of CPU

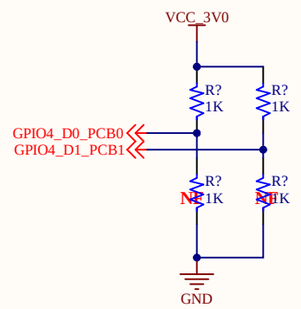








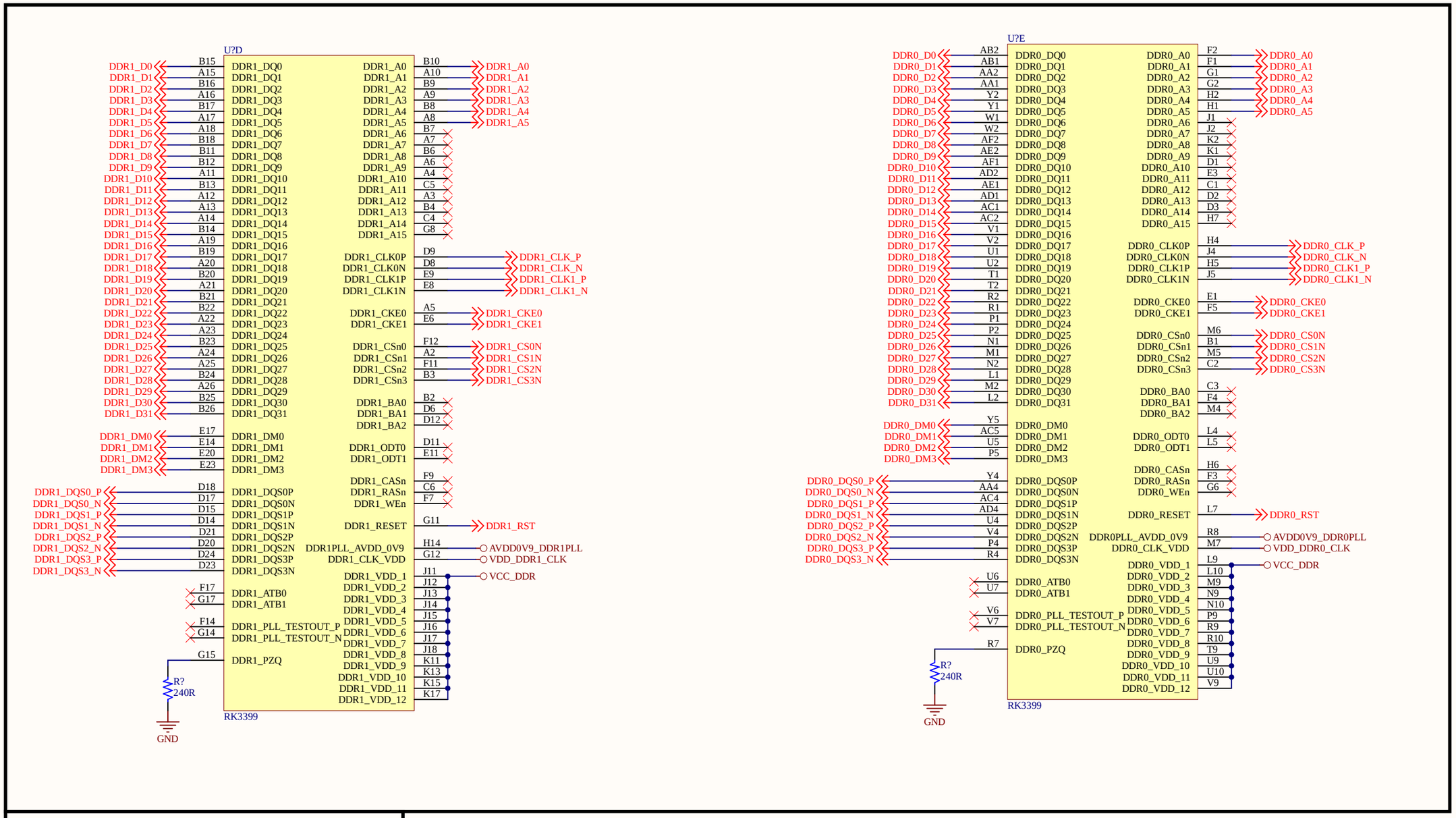


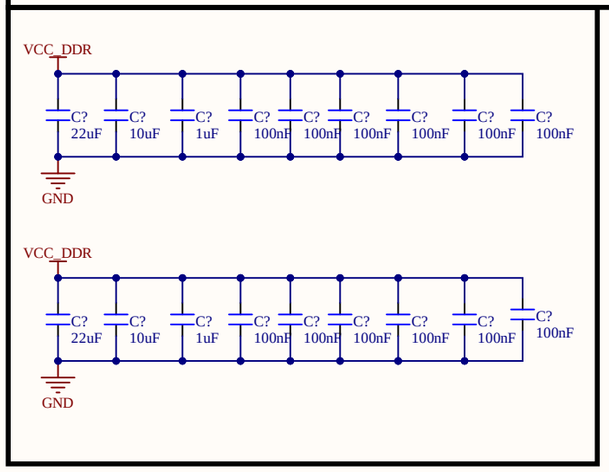


TITLE:	**RK3399 SOM Board Design V1.0**
DOCUMENT NAME:	**[6]-RGMII_SDIO_SPI_GPIOs etc.SchDoc**
PROJECT CODE:	**A_V1.0**
Sheet	**7 of 12**
SCALE 1:1	TEMPLATE: A3 AUTHOR: ABC

ESTEEM PCB

LPDDR3 of CPU

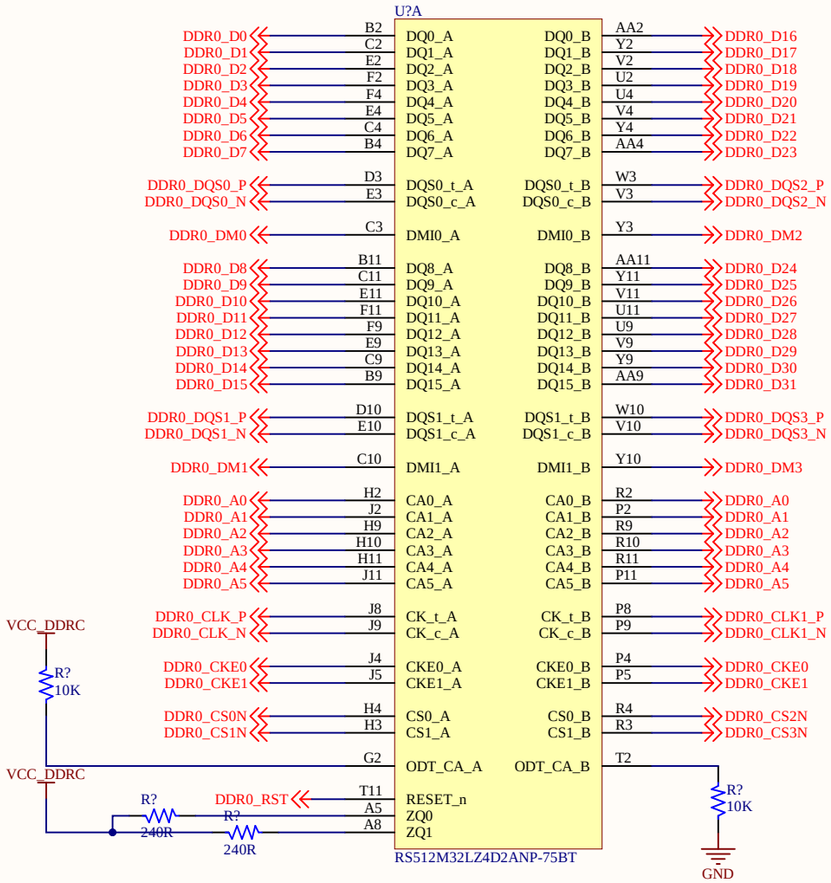




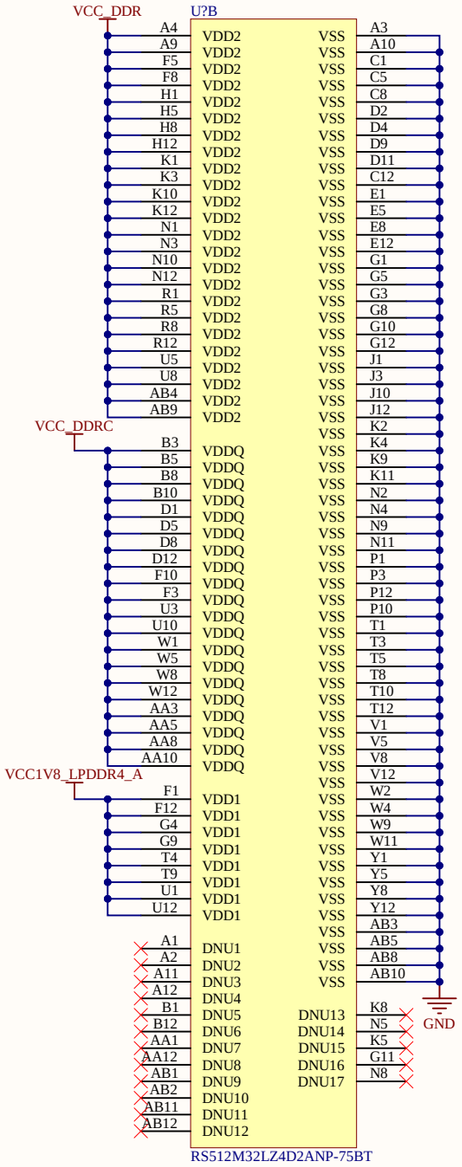
TITLE:	**RK3399 SOM Board Design V1.0**
DOCUMENT NAME:	**[7]-RK3399 SDRAM Page.SchDoc**
PROJECT CODE:	**A_V1.0**
Sheet	**8** of **12**
SCALE 1:1	TEMPLATE: A3
AUTHOR:	ABC

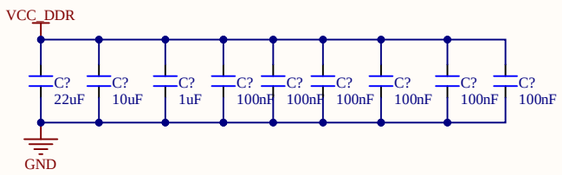
ESTEEM PCB

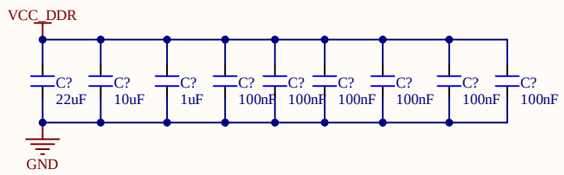
RS512M32LZ4D2ANP-75BT DRAM

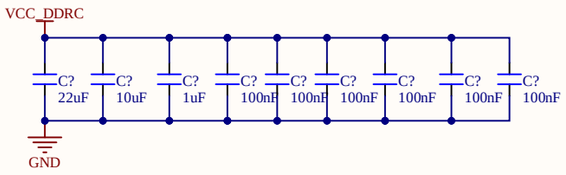


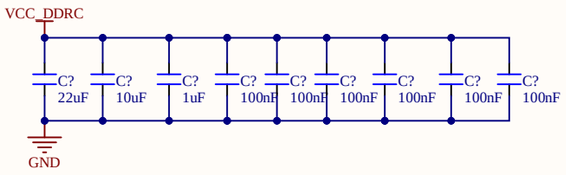
VCC1 -> VCC1V8_LPDDR4 (Supply Pins)
VCC2 -> VCC_DDR (CA Power)
VCCQ-> VCC_DDRC (I/O Buffer Power)

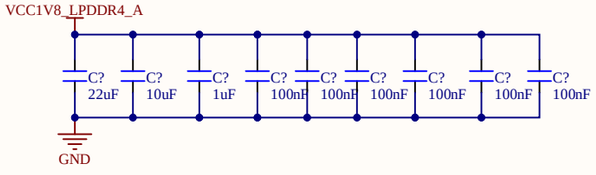








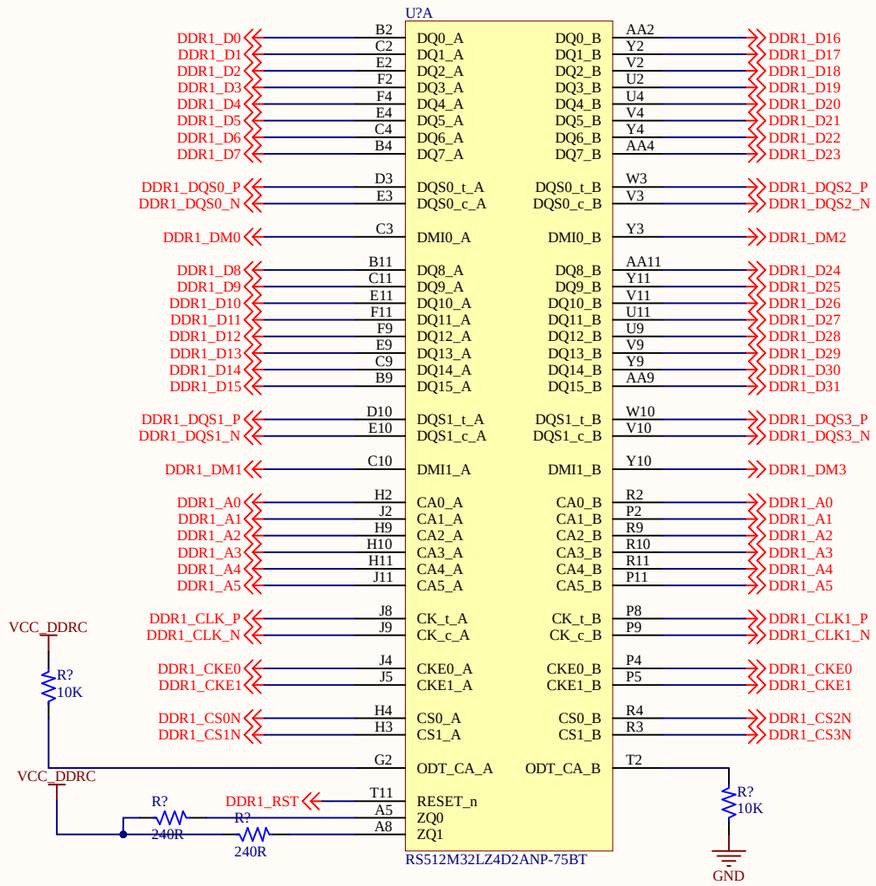




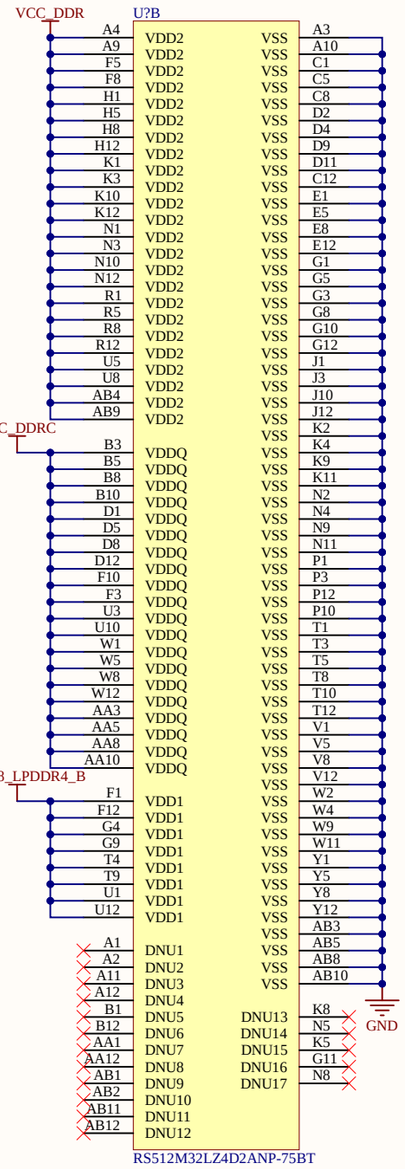
TITLE:	**RK3399 SOM Board Design V1.0**		
DOCUMENT NAME:	**[8]-LPDDR4 SDRAM-1.SchDoc**		
PROJECT CODE:	**A_V1.0**	Sheet	**9** of **12**
SCALE 1:1	TEMPLATE: A3	AUTHOR:	ABC

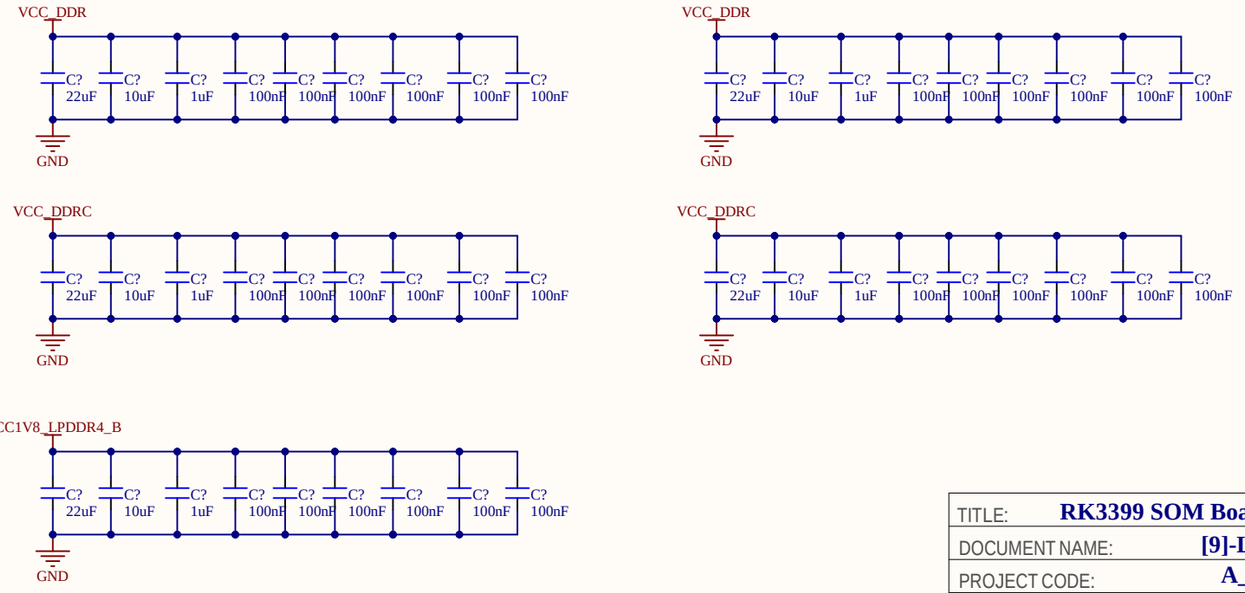
ESTEEM PCB

RS512M32LZ4D2ANP-75BT DRAM



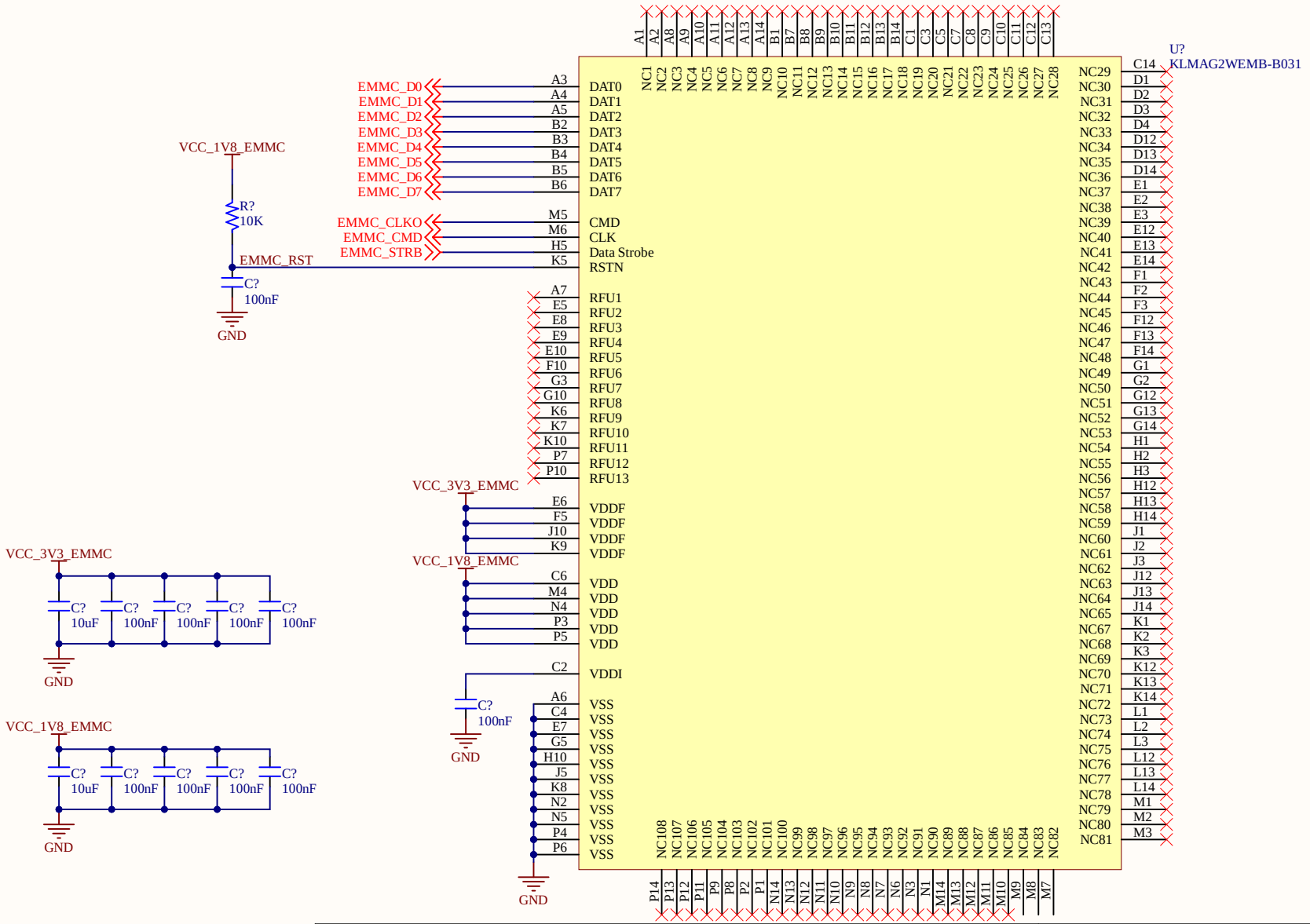
VCC1 -> VCC1V8_LPDDR4 (Supply Pins)
VCC2 -> VCC_DDR (CA Power)
VCCQ-> VCC_DDRC (I/O Buffer Power)





TITLE:	RK3399 SOM Board Design V1.0		
DOCUMENT NAME:	[9]-LPDDR4 SDRAM-2.SchDoc		
PROJECT CODE:	A_V1.0	Sheet	10 of 12
SCALE 1:1	TEMPLATE: A3	AUTHOR:	ABC

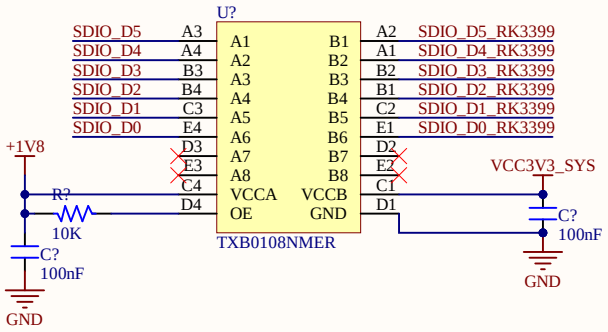
ESTEEM PCB

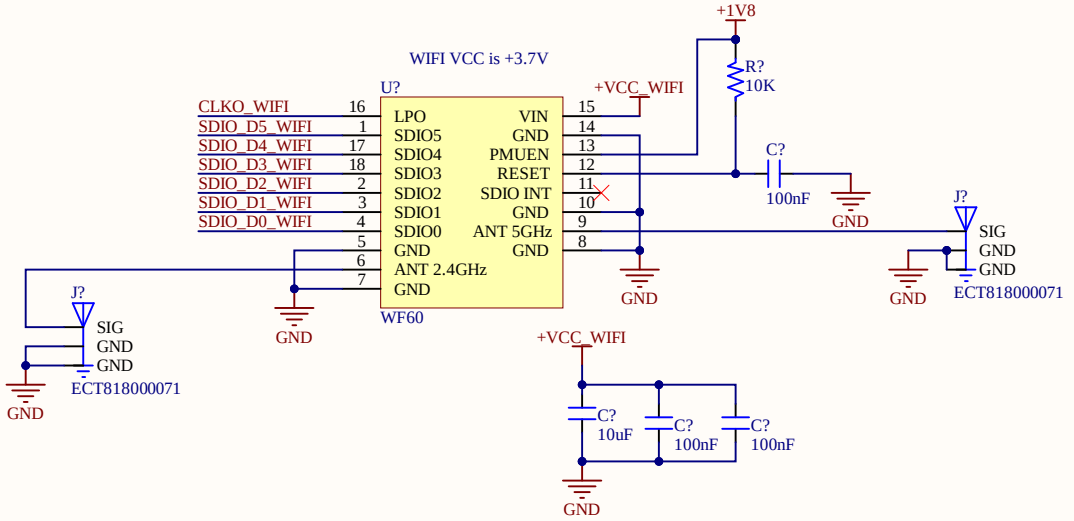


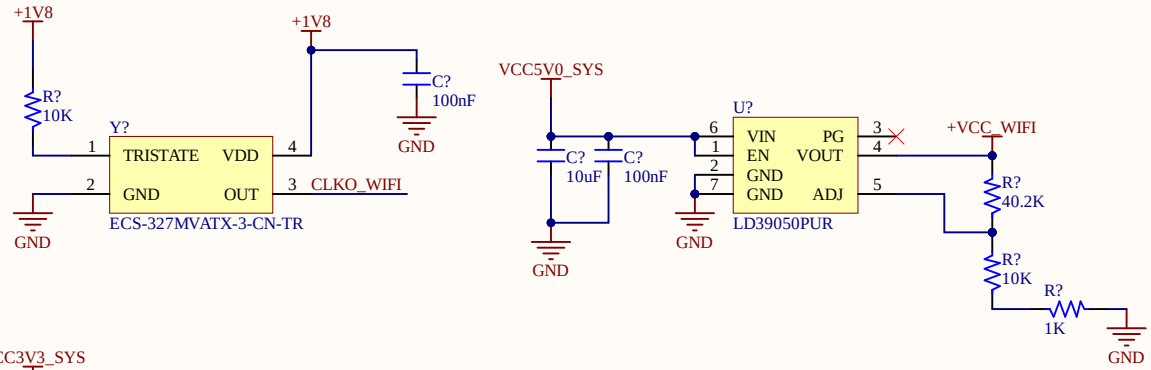
TITLE:	**RK3399 SOM Board Design V1.0**		
DOCUMENT NAME:	**[10]-EMMC Chip.SchDoc**		
PROJECT CODE:	**A_V1.0**	Sheet **11** of **12**	
SCALE 1:1	TEMPLATE: A4	AUTHOR: AVIRAL MISHRA	

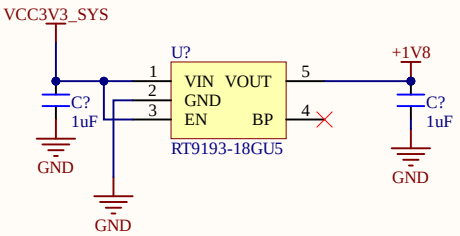
ESTEEM PCB

ERROR!!! Compare with WF60 Datasheet









- The load capacitor including SD card and PCB, the load capacitor of SD card in protocol should be less than 10 pF.

- **3.0V operation: 50 MHz with 40pF**
- **1.8V operation: 208 MHz with 21pF**

Figure 4- 38 SDMMC Loading Capacitor

3. Card capacitance range is defined as follows:

Capacitance	Min	Max	Units	Notes
C_{CARD} (C_{DIE} + C_{PKG})	5	10	pF	---

Table 6-10 : Card Capacitance Range

Figure 4- 39 SD Card Load Capacitor

SDIO/SDMMC layout requirements are shown as Table 4-17:

TITLE:	**RK3399 SOM Board Design V1.0**		
DOCUMENT NAME:	**[11]-WIFI Module WF60.SchDoc**		
PROJECT CODE:	**A_V1.0**	Sheet	**12** of **12**
SCALE 1:1	TEMPLATE: A4	AUTHOR:	AVIRAL MISHRA

ESTEEM PCB