LVDS Owner's Manual

Low-Voltage Differential Signaling

3rd Edition, Spring 2004

National Semiconductor

The Sight & Sound of Information

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The last thing an engineer ever does is read the owner's manual. An engineer expects to be able to use his or her skills and training to figure out how to use a product without ever referring to the instructions. In my experience, either through intuition or trial and error, most of us will eventually figure out the basics. However, while this may be reasonable for assembling a toy or even working on a car, it is an expensive and time consuming way to go about electrical engineering.

National Semiconductor has written this LVDS Owner's Manual to assist you. This design guide compiles the information and concepts that we think you will need to save you valuable time and money and maximize the benefit of using National's Low-Voltage Differential Signaling (LVDS) solutions.

National is the premier analog semiconductor solution supplier and the innovator of LVDS. Our experience with LVDS gives us the insight to be your trusted advisor. This third edition of the LVDS Owner's Manual is an easy-to-read compendium that contains useful information for everyone. There is an introduction to the technology, concepts, and applications for someone just starting to design with LVDS. We offer guidance on how to select the right LVDS device and family for your application whether it is chip-to-chip, mezzanine-to-mezzanine, or box-to-box. Perhaps most helpful is our guidance for proper selection of cables, termination, and backplane design considerations.

We are confident that you will find the LVDS Owner's Manual a useful reference guide and an introduction to the many application support tools that we offer. Please visit our support website at LVDS.national.com for more information or to contact one of our applications engineers.

We are grateful for your business and we look forward to supporting all of your analog semiconductor solution needs.

Sincerely,

National Semiconductor
LVDS Group

Table of contents

Chapter 1 - Introduction to LVDS

1.1 The trend to LVDS 1-1

1.2 Getting speed with low noise and low power 1-1

1.3 LVDS ICs 1-4

1.4 Bus LVDS (BLVDS) 1-4

1.5 LVDS applications 1-5

Chapter 2 - Using LVDS

2.1 Why low swing differential? 2-1

2.2 An economical interface 2-4

2.3 Embedded LVDS I/O in FPGAs and ASICs 2-5

2.4 National's wide range of LVDS solutions 2-9

2.5 Conclusion 2-9

Chapter 3 - High-speed design

3.1 PCB layout tips 3-1

3.2 Lowering Electromagnetic Interface (EMI) 3-6

3.3 AC-coupling 3-14

Chapter 4 - Designing with LVDS

4.1 Introduction 4-1

4.2 Results of good vs. bad design practices 4-2

4.3 Lowering Electromagnetic Interference (EMI) 4-5

4.4 Common-mode noise rejection 4-6

4.5 LVDS configuration 4-8

4.6 Failsafe biasing of LVDS 4-10

4.7 Power-off high impedance bus pins 4-12

LVDS Owner's Manual

Chapter 5 - Backplane design considerations and Bus LVDS

5.1 Configurations 5-1

5.2 Bus LVDS 5-3

5.3 Backplane design considerations 5-5

5.4 Additional information 5-14

Chapter 6 - Cable, connectors, and performance testing

6.1 General comments 6-1

6.2 Cabling suggestions 6-1

6.3 Cable ground and shield connections 6-4

Chapter 7 - Performance testing

7.1 LVDS signal quality 7-1

7.2 BERT 7-7

Chapter 8 - Evaluation kits

8.1 Evaluation/demo boards 8-1

Appendix

A.1 LVDS application notes, white papers A-1

A.2 Glossary A-2

A.3 Detailed explanation of datasheet parameters A-4

A.4 National Semiconductor worldwide sales offices A-7

Chapter 1
Introduction to LVDS

Low-Voltage Differential Signaling (LVDS) is a new technology addressing the needs of today's high performance data transmission applications. The LVDS standard is becoming the most popular differential data transmission standard in the industry. This is driven by two simple features: "Gigabits @ milliwatts!"

LVDS delivers high data rates while consuming significantly less power than competing technologies. In addition, it brings many other benefits, which include:

- Low-voltage power supply compatibility
- Low noise generation
- High noise rejection
- Robust transmission signals
- Ability to be integrated into system level ICs

LVDS technology allows products to address high data rates ranging from 100's of Mbps to greater than 2 Gbps. For all of the above reasons, it has been deployed across many market segments wherever the need for speed and low power exists.

1.1 The trend to LVDS

Consumers are demanding more realistic visual information in the office and in the home. This drives the need to move video, 3D graphics and photo-realistic image data from cameras to PCs and printers through LAN, phone, and satellite systems to home set-top boxes and digital VCRs. Solutions exist today to move this high-speed digital data both very short and very long distances, on printed circuit boards (PCB) and across fiber or satellite networks. Moving this data from board-to-board or box-to-box however, requires an extremely high-performance solution that consumes a minimum of power, generates little noise, (must meet increasingly stringent FCC/CISPR EMI requirements) is relatively immune to noise, and is cost-effective.

National Semiconductor first introduced LVDS as a standard in 1994. National recognized that the demand for bandwidth was increasing at an exponential rate while users also desired low power dissipation. This exceeded the speed capabilities of RS-422 and RS-485 differential transmission standards. While Emitter Coupled Logic (ECL or PECL) was available at the time, it is incompatible with standard logic levels, uses negative power rails, and leads to high chip-power dissipation. These factors limited its wide spread acceptance.

LVDS is differential, using two signal lines to convey information. While sounding like a penalty, this is actually a benefit. The cost is two traces (or conductors) to convey a signal, but the gain is noise tolerance in the form of common-mode rejection.

Signal swing can be dropped to only a few hundred millivolts because the signal-to-noise rejection has been improved. The small swing enables faster data rates since the rise time is now so much shorter.

1.2 Getting speed with low noise and low power

LVDS is a low swing, differential signaling technology, which allows single channel data transmission at hundreds or even thousands of Megabits per second (Mbps). Its low swing and current-mode driver outputs create low noise and provide very low power consumption across a wide range of frequencies.

1.2.1 How LVDS works

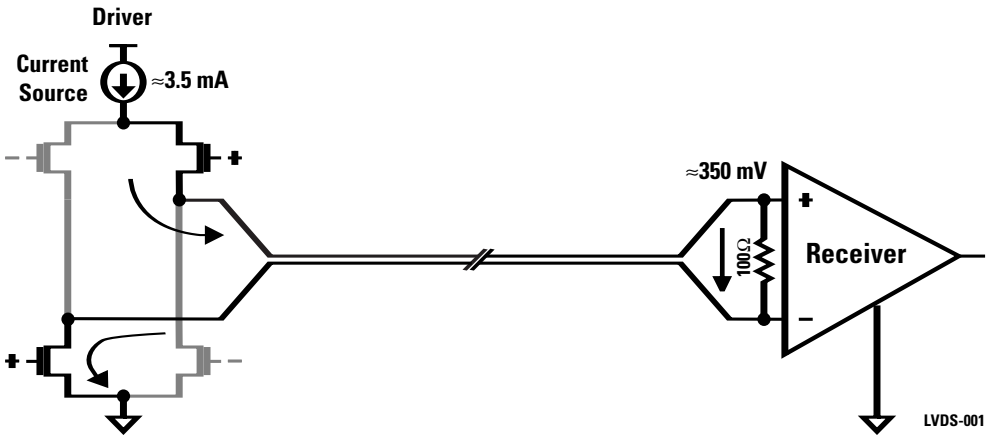


Figure 1.1. Simplified diagram of LVDS Driver and receiver connected via 100Ω differential impedance media

LVDS outputs consist of a current source (nominal 3.5 mA) that drives the differential pair lines. The basic receiver has a high DC input impedance, so the majority of driver current flows across the 100Ω termination resistor generating about 350 mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid "one" or "zero" logic state.

1.2.2 The LVDS Standard

LVDS is currently standardized by the TIA/EIA (Telecommunications Industry Association/Electronic Industries Association) ANSI/TIA/EIA-644-A (LVDS) Standard

The generic (multi-application) LVDS standard, ANSI/TIA/EIA-644-A, began in the TIA Data Transmission Interface committee TR30.2 in 1995. It was revised and published as ANSI/TIA/EIA-644-A in 2001. The ANSI/TIA/EIA standard defines driver output and receiver input characteristics, thus it is an electrical-only standard. It does not include functional specifications, protocols or even complete cable characteristics since these are application dependent. ANSI/TIA/EIA-644-A is intended to be reference by other standards that specify the complete interface (i.e., connectors, protocol). This allows it to be easily adopted into many applications.

ANSI/TIA/EIA-644-A (LVDS) standard

Table 1.1. ANSI/TIA/EIA-644 (LVDS) standards

Parameter	Description	Min.	Max.	Units
V_{OD}	Differential output voltage	247	454	mV
V_{OS}	Offset voltage	1.125	1.375	V
V_{OD}	|Change to V_{OD}|		50	|mV|
V_{OS}	|Change to V_{OS}|		50	|mV|
I_{SA}, I_{SB}	Short circuit current		24	|mA|
tr/tf	Output rise/fall times (200 Mbps)	0.26	1.5	ns
	Output rise/fall times (<200 Mbps)	0.26	30% of tui†	ns
I_{IN}	Input current		20	|µA|
V_{TH}	Receive threshold voltage		+100	mV
V_{IN}	Input voltage range	0	2.4	V

† tui is unit interval (i.e. bit width).
Note: Actual datasheet specifications may be significantly better.

(See Appendix A for a detailed explanation of these parameters.)

The ANSI/TIA/EIA standard recommends a maximum data rate of 655 Mbps (based on a limiting set of assumptions) and it also provides a theoretical maximum of 1.923 Gbps based on a loss-less medium. This allows the referencing standard to specify the maximum data rate required depending upon required signal quality and media length/type.

The standard also covers minimum media specifications, failsafe operation of the receiver under fault conditions, and other configuration issues such as multiple receiver operation.

The ANSI/TIA/EIA-644 standard was approved in November 1995. National held the editor position for this standard. The 644 spec has been revised to include additional information about multiple receiver operation. The revised spec was published in February 2001 with the title TIA-644-A.

There was another LVDS standard from an IEEE project. This standard came out of an effort to develop a standard for purposes such as linking processors in a multiprocessing system or grouping workstations into a cluster. This Scalable Coherent Interface (SCI) program originally specified a differential ECL interface that provided the high data rates required but did not address power concerns or integration.

The low-power SCI-LVDS standard was later defined as a subset of SCI and is specified in the IEEE 1596.3 standard. The SCI-LVDS standard also specifies signaling levels (electrical specifications) similar to the ANSI/TIA/EIA-644-A standard for the high-speed/low-power SCI physical layer interface. The standard also defines the encoding for packet switching used in SCI data transfers. The IEEE 1596.3 standard was approved in March 1996, but expired 5 years later and was not renewed. National chaired this standardization committee.

In the interest of promoting a wider standard, no specific process technology, medium, or power supply voltages are defined by either standard. This means that LVDS can be implemented in CMOS, GaAs or other applicable technologies, migrate from 5V to 3.3V to sub-3V supplies, and transmit over PCB traces or cable, thereby serving a broad range of applications in many industry segments.

1.3 LVDS ICs

A wide variety of LVDS Interface devices is available from a range of suppliers. LVDS is most commonly found in the following types of ICs.

Line drivers/receivers

These devices are typically used to convert single-ended signals, such as LVCMOS into a format more suitable for transmission over a backplane or a cable. They are available in single-channel as well as multi-channel configurations.

SerDes

Serializer/deserializer pairs are used to multiplex a number of low-speed CMOS lines and to transmit them as a single channel running at a higher data rate. SerDes ICs are typically used to reduce the number of connector pins or lines within cables and backplanes. SerDes functions are being embedded into large and complex ICs in order to reduce the number of I/Os on the IC package.

Switches

Switching architectures are favored over bus architectures when data-rates are high. As a consequence, switches tend to operate at high data rates. LVDS is a common choice for the I/Os on these ICs. Switches can be used for clock distribution. LVDS is one of the most suitable signaling standards for clocks of any frequency because of reliable signal integrity.

1.4 Bus LVDS (BLVDS)

Bus LVDS, sometimes called BLVDS, is a new family of bus interface circuits based on LVDS technology, specifically addressing multipoint cable or backplane applications. it differs from standard LVDS in providing increased drive current to handle double terminations that are required in multipoint applications.

Bus LVDS addresses many of the challenges faced in a high-speed bus design.

- Bus LVDS eliminates the need for a special termination pull-up rail
- It eliminates the need for active termination devices
- Utilizes common power supply rails (3.3V or 5V)
- Employs a simple termination scheme
- Minimizes power dissipation in the interface devices
- Generates little noise
- Supports live insertion of cards
- Drives heavily loaded multi-point busses at 100's of Mbps

The Bus LVDS products provide designers with new alternatives for solving high-speed, multi-point bus interface problems. Bus LVDS has a wide application space ranging from telecom infrastructure and datacom applications where card density demands high-performance backplanes to industrial applications where long cable length and noise immunity are useful.

Refer to Chapter 5 for more details on Bus LVDS.

1.5 LVDS applications

The high-speed and low power/noise/cost benefits of LVDS make it a compelling technology, that fits into a broad range of applications. Some examples are listed in Table 1.2.

Table 1.2. Sample applications

PC/computing	Telecom/datacom	Consumer/commercial
Flat-panel displays	Switches	Home/commercial video links
Monitor link	Add/drop multiplexers	Set top boxes
SCI processor interconnect	Hubs	In-flight entertainment
Printer engine links	Routers	Game displays/control
Digital Copiers	Access systems	
System clustering	Broadband concentrators	
Multimedia peripheral links	Base stations	

Chapter 2
Using LVDS

2.1 Why low-swing differential?

The differential data transmission method used in LVDS is less susceptible to common-mode noise than single-ended schemes. Differential transmission uses two wires with opposite current/voltage swings instead of the one wire used in single-ended methods to convey data information. The advantage of the differential approach is that if noise is coupled onto the two wires as common-mode (the noise appears on both lines equally) and is thus rejected by the receivers, which looks at only the difference between the two signals. The differential signals also tend to radiate less noise than single-ended signals due to the canceling of magnetic fields. In addition, the current-mode driver is not prone to ringing and switching spikes, further reducing noise.

Because differential technologies such as LVDS reduce concerns about noise, they can use lower signal voltage swings. This advantage is crucial, because it is impossible to raise data rates and lower power consumption without using low voltage swings. The low swing nature of the driver means data can be switched very quickly. Since the driver is also current-mode, very low – almost flat – power consumption across frequency is obtained. Switching spikes in the driver are very small, so that ICC does not increase exponentially as switching frequency is increased. Also, the power consumed by the load (3.5 mA x 350 mV = 1.2 mW) is very small in magnitude.

2.1.1 A quick comparison between differential signaling technologies

Table 2.1. Comparison of LVDS with RS-422 and PECL

Parameter	RS-422	PECL	LVDS
Differential driver output voltage	±2 to ±5V	±600 to 1000 mV	±250-450 mV
Receiver input threshold	±200 mV	±200 to 300 mV	±100 mV
Data rate	<30 Mbps	>400 Mbps	>400 Mbps

Parameter	RS-422	PECL	LVDS*
Supply current quad driver (no load, static)	60 mA (max)	32 to 65 mA (max)	8.0 mA
Supply current quad receiver (no load, static)	23 mA (max)	40 mA (max)	15 mA (max)
Propagation delay of driver	11 ns (max)	4.5 ns (max)	1.7 ns (max)
Propagation delay of receiver	30 ns (max)	7.0 ns (max)	2.7 ns (max)
Pulse skew (driver or receiver)	N/A	500 ps (max)	400 ps (max)

*LVDS devices noted are DS90LV047A/048A

Table 2.1 compares basic LVDS signaling levels with those of PECL and shows that LVDS has half the voltage swing of PECL. LVDS swings are one-tenth of RS-422 and also traditional TTL/CMOS levels.

Another voltage characteristic of LVDS is that the drivers and receivers do not depend on a specific power supply, such as 5V. Therefore, LVDS has an easy migration path to lower supply voltages such as 3.3V or even 2.5V, while still maintaining the same signaling levels and performance. In contrast, technologies such as ECL or PECL have a greater dependence on the supply voltage, which make it difficult to migrate systems utilizing these technologies to lower supply voltages.

2.1.2 Easy termination

The transmission medium must be terminated to its characteristic differential impedance to complete the current loop and terminate the high-speed (edge rates) signals. That requirement is the same, whether the LVDS transmission medium consists of a cable or of controlled impedance traces on a printed circuit board. If the medium is not properly terminated, signals reflect from the end of the cable or trace and may interfere with succeeding signals. Proper termination also reduces unwanted electromagnetic emissions and provides the optimum signal quality.

To prevent reflections, LVDS requires a terminating resistor that is matched to the actual cable or PCB trace's differential impedance. Commonly, 100Ω media and terminations are employed. This resistor completes the current loop and properly terminates the signal. This resistor is placed across the differential signal lines as close as possible to the receiver input.

Figure 2.1. LVDS termination

Figure 2.1a. Internal termination

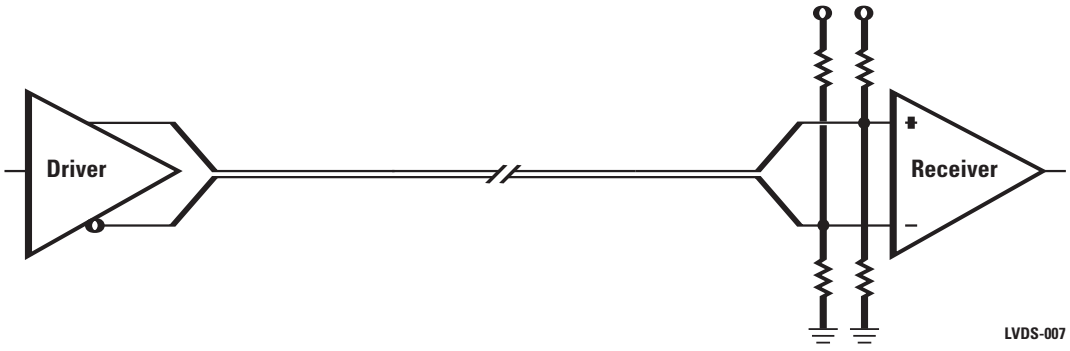


Figure 2.2. PECL termination

The simplicity of the LVDS termination scheme makes it easy to implement in **most** applications. ECL and PECL require a more complex termination than the one-resistor solution for LVDS. PECL connections must meet several requirements at the same time. The receivers must be biased to around 1V below V_{EE}. The transmission lines must be terminated and there must be a resistive path for DC current to flow from the driver. The example in the Figure 2.2 shows an implementation with a Thévenin network.

2.1.3 Maximum switching speed

Maximum switching speed of an LVDS Interface is a complex question, and its answer depends upon several factors. These factors are the performance of the line driver (edge rate) and receiver, the bandwidth of the media, and the required signal quality for the application.

Since the driver outputs are very fast, the limitation on speed is commonly restricted by:

1. How fast TTL data can be delivered to the driver – in the case of simple PHY devices that translate a TTL/CMOS signal to LVDS (i.e. DS90LV047A)
2. Bandwidth performance of the selected media (cable) – type and length dependent

For example, the factor that limits the speed of the DS90LV047A LVDS driver is the rate that TTL data can be delivered.

National's Channel Link devices (SerDes) capitalize on the speed mismatch between TTL and LVDS by serializing the TTL data into a narrower LVDS data stream (more about this later).

2.1.4 Saving power

LVDS technology saves power in several important ways. The power dissipated by the load (the 100Ω termination resistor) is a mere 1.2 mW. In comparison, an RS-422 driver typically delivers 3V across a 100Ω termination. It dissipates 90 mW of power — 75x more than LVDS.

LVDS devices are implemented in CMOS processes, which provide low static power consumption. The circuit design of the drivers and receiver require roughly one-tenth the power supply current of PECL/ECL devices.

Aside from the power dissipated in the load and static I_{DD} current, LVDS also lowers system power through its current-mode driver design. This design greatly reduces the frequency component of I_{DD}. The I_{DD} vs. frequency plot for LVDS is virtually flat between 10 MHz and 100 MHz. The quad device, DS90C031/2 uses less than 50 mA total, for driver and receiver at 100 MHz. Compare this to TTL/CMOS transceivers whose dynamic power consumption increases exponentially with frequency.

2.1.5 LVDS configurations

Figure 2.3. Point-to-point configuration

LVDS drivers and receivers are commonly used in a point-to-point configuration, as shown in Figure 2.3. Dedicated point-to-point links provide the best signal quality due to the clear path they provide. In this configuration, LVDS is capable of transmitting high-speed signals over substantial lengths of cable while using remarkably little power and generating very little noise. However, other topologies/configurations are also possible.

When the system architect is more interested in minimizing the number of interconnects than in raw performance, LVDS is a great technology to consider. LVDS is well suited to bi-directional signaling and bus applications.

The configuration shown in Figure 2.4 allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin), so this configuration should be considered only where noise is low and transmission distance is short (<10m). Chapter 5 contains an overview of Bus LVDS devices, which are designed for double termination loads and provide full LVDS compatible levels.

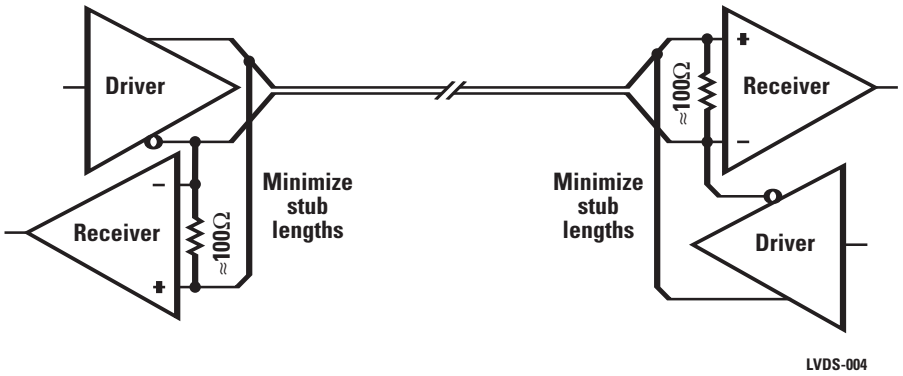


Figure 2.4. Bi-directional half-duplex configuration

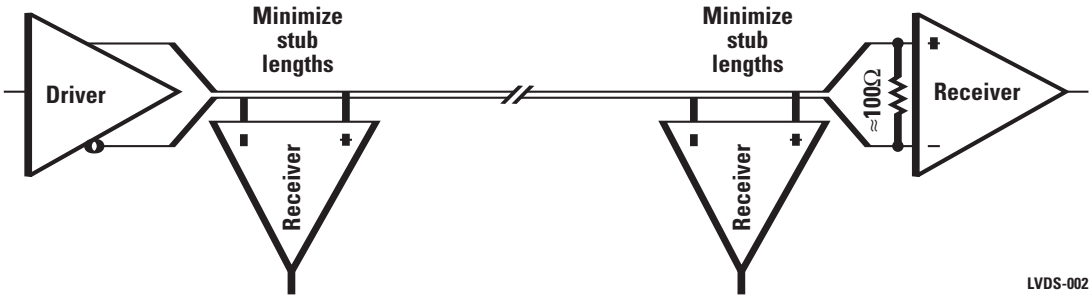


Figure 2.5. Multidrop configuration

A multidrop configuration connects multiple receivers to a driver. These are useful in data distribution applications. They can also be used if the stub lengths are as short as possible (less than 20 mm – application dependent). Section 5.2 also covers multidrop applications.

2.2 An economical interface

LVDS is a cost-effective solution:

1. National's LVDS CMOS implementations provide better price/performance ratios as compared to custom solutions on elaborate processes.
2. High performance can be achieved using common, off-the-shelf CAT3 cable and connectors, and/or FR4 material.
3. LVDS consumes very little power, thereby reducing or eliminating power supplies, fans, and other peripherals.
4. LVDS is a low-noise and noise-tolerant technology, minimizing problems.

5. LVDS transceivers are cost-efficient products that can also be integrated around digital cores providing a higher level of integration.
6. LVDS moves data much faster than TTL, so multiple TTL signals can be serialized or multiplexed into a single LVDS channel, reducing board, connectors, and cabling costs.

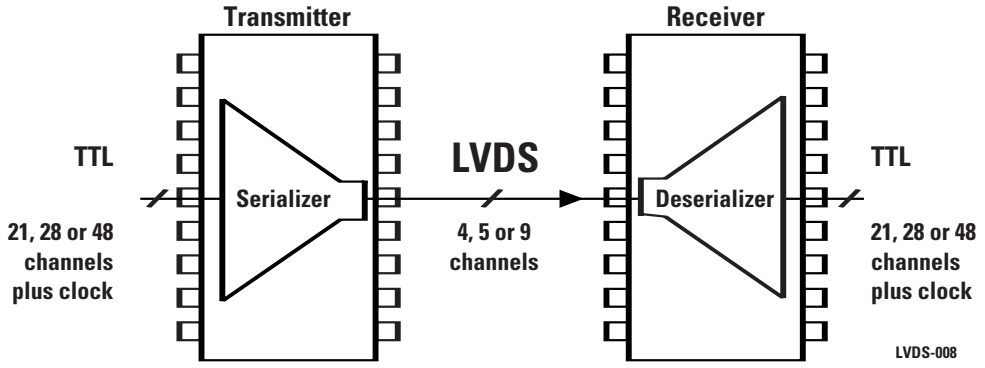


Figure 2.6. National's Channel Link chipsets convert a TTL bus into a compact LVDS data stream and back to TTL

In fact, in some applications, the Printed Circuit Board (PCB), cable, and connector cost savings greatly overshadow any additional silicon costs. Smaller PCBs, cables, and connectors also result in a much more ergonomic, user-friendly system.

2.3 Embedded LVDS I/O in FPGAs and ASICs

The latest Field Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs) are moving into the Bus LVDS application space. These new product offerings have enhanced LVDS drive characteristics designed to be more compatible with a typical multidrop topology. There are advantages and disadvantages to these FPGA platforms over discrete solutions. For example, fewer ICs on a PCB generally lead to simpler designs with fewer interconnects, and integrated solutions are sometimes necessary when board size is a concern.

System designers should weigh these advantages against the compromises they will be making in signal integrity. They should also be aware that discrete solutions are typically more cost effective than integrated FPGA platforms.

Several major design challenges still need to be addressed in order to successfully design a robust backplane interface.

1. Stub length: This is the trace length from the backplane trace, through the backplane connector to the Bus LVDS receiver. Long stubs in multidrop and multipoint buses lead to poor signal integrity.
2. ESD protection: Resistance to electrostatic discharge (ESD) improves the reliability of system boards during insertion and removal events.
3. Capacitive loading: This is the capacitance seen at the I/O of an active device. High capacitance leads to low impedance and low noise margin.

2.3.1 Stub length

Reductions in stub length are one of the best ways to improve the signal integrity of a multidrop or multipoint bus.

As a rule of thumb, stub lengths should be no longer than 2.5 cm or 1 in., (see Section 5.3.3) It is possible to design with longer stub trace lengths, but bus noise from signal reflections limit system performance.

A board designer does not always have a great deal of flexibility with respect to the placement of the FPGA or ASIC on his board. If an LVDS receiver is integrated into a larger IC, its placement depends on a number of factors. These factors tend to conflict with the signal integrity related needs of the receiver being near the backplane connector. The designer's ability to control trace lengths between the connector and the ICs inputs are further diminished when an FPGA contains a large number of high-speed I/Os.

A discrete solution enables the placement of LVDS I/Os for optimum signal integrity. This is one less factor that the board designer needs to worry about as the balances the compromises over the placement of the larger ICs.

2.3.2 ESD protection

Anytime a board or cable is handled or plugged into a system, the opportunity exists for ESD events to occur. Integrated circuits mounted to the external interfaces on the board are most likely to be in the ESD event path. Selecting devices with high ESD tolerances will increase the reliability of the board. It is desirable to isolate and protect sensitive programmable devices from the stresses associated with ESD events with interface devices from National.

Example HBM ESD protection levels

DS90LV047	>10 kV
DS90LV048	>10 kV
DS90CP22	>5.0 kV
DS92LV090	>4.5 kV
DS92LV040	>4.0 kV

Many of the FPGAs and PLDs pass HBM ESD tests in the range of 1000V to 2000V. For these designs requiring more protection, a lower-cost, stand-alone LVDS IC provides this protection on behalf of the high-end ICs.

2.3.3 Capacitive loading

Plug-in cards present capacitive loads on backplane traces. As the loading on the backplane bus traces increases, their impedance drops. The drop in impedance reduces the available noise margin and the reliability of operation in the design.

The three factors on a plug-in card that contribute to the capacitive loading on a bus are the:

- Bulk capacitance load resulting from the connector
- PCB trace
- I/O structure of the device

In a good design the connector contributes 2 pF to 3 pF, the trace contributes 2 pF to 3 pF, and the device contributes 4 pF to 5 pF. The total load in such a design is around 10 pF.

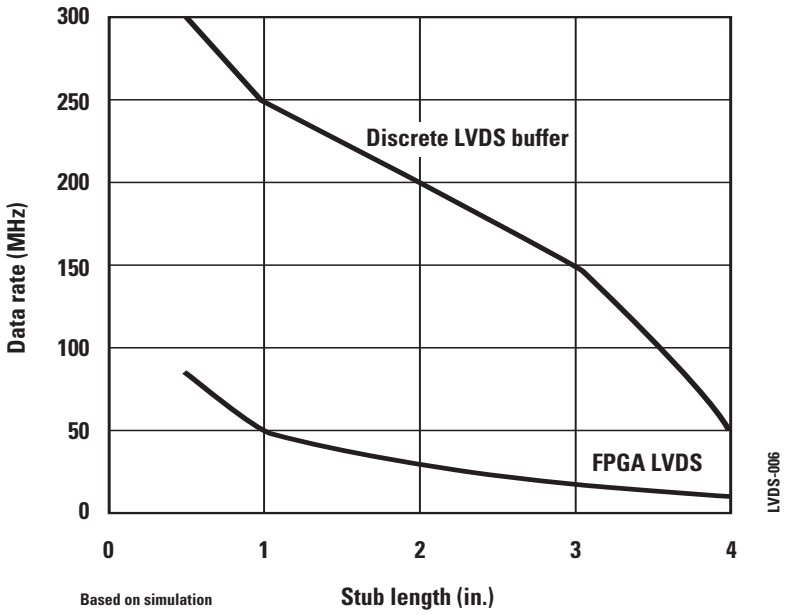


Figure 2.7. Comparison of backplane performance between integrated and discrete solutions

The flexibility of programmable devices comes at the cost of capacitance. National Bus LVDS products have an I/O capacitance of 5 pF. The I/O capacitance of a programmable device is approximately double or 10 pF. This increase in capacitance will lower the loaded bus impedance, thereby reducing the available noise margin and lowering the reliability of operation in the design.

Figure 2.7 is the result of a simulation comparing the performance of a discrete solution with the performance of an FPGA with embedded LVDS I/Os. The data rates that can be supported by the discrete solution are several times higher, which is mostly a result of lower capacitance in the I/Os.

2.3.4 Cable drive capability

Today's system requirements often define high-speed serial intra- and inter-chassis connections. This makes the ability to drive cables an important aspect of I/O performance. Comparing LVDS outputs typical of advanced FPGAs available today with the new generation of LVDS devices shows a substantial difference in capabilities.

Figure 2.8 shows the results of an experiment, comparing the abilities of different circuits to drive cables. Data taken on the FPGA was done with minimal internal logic. The only structures used in this optimized setup for the FPGA were the input stage, internal buffering and the output stage. If more internal logic is switching inside the FPGA, then there is more noise on the LVDS I/O signals. The National device was fully operational with all outputs switching at the input frequency.

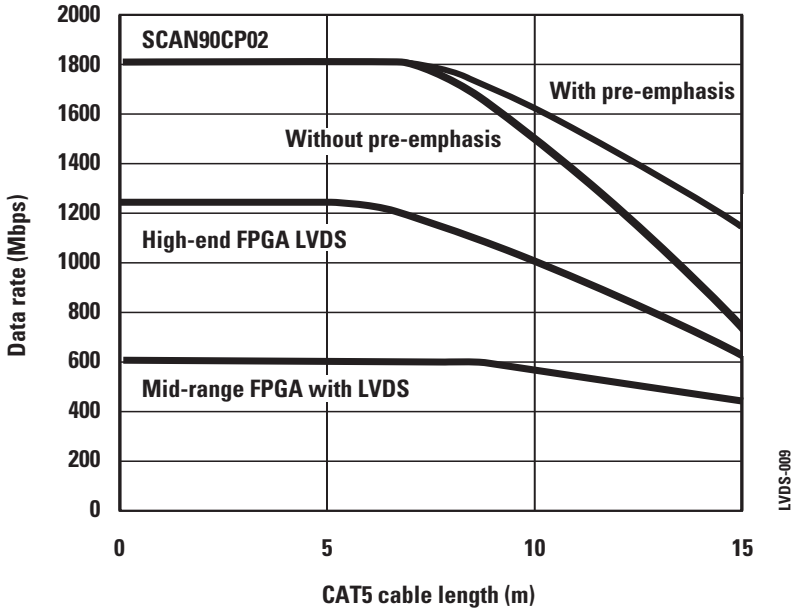


Figure 2.8. Comparison of cable-drive performance between integrated and discrete solutions

The discrete LVDS devices have I/Os that have been optimized for driving cables. Figure 2.8 clearly demonstrates that their performance is superior to the general-purpose I/Os of the FPGA.

2.3.5 Flexibility

FPGAs with high-speed LVDS I/Os tend to be more expensive than similar devices with lower speed I/Os. The designer might realize value from the more expensive FPGA when all or most of the high-speed I/Os are being used. It is often the case, however, that the number of I/Os does not closely match the requirements of the design. When that happens, much of the high-value performance that the designer is paying for goes to waste.

There are many discrete LVDS products on the market, with a wide range of interface configurations and bus widths. It is much more likely that a designer will find a suitable LVDS interface on a discrete component, than he will on an FPGA. A solution more closely suited to a design's minimum requirements will certainly be more cost effective.

2.4 National's wide range of LVDS solutions

National offers LVDS technology in several forms. For example, National's 5V DS90C031/DS90C032 and 3V DS90LV047A/DS90LV048A quad line driver/receiver devices implement LVDS technology in discrete packages for general-purpose use. This family of basic line drivers and receivers also contains single, dual, and quad footprints.

For the specialized task of connecting laptop and notebook computers to their high-resolution LCD screens, National offers the Flat Panel Display Link (FPD-Link) and LVDS Display Interface (LDI) devices. These parts provide a high bandwidth, low power, small size, interface enabling XGA/SXGA/UXGA and beyond displays for notebook and monitor applications.

Another more generalized use of LVDS is in the National channel link family, which can convert 21, 28, or 48 bits of parallel data to 3, 4, or 8 channels of LVDS serial data, plus LVDS clock. These devices provide fast data pipes (up to 6.4 Gbps throughput) and are well suited for high-speed network hubs, router applications, or anywhere a low-cost, high-speed link is needed. Their serializing nature provides a greater price/performance ratio as cables and connector physical size are greatly reduced.

Bus LVDS is an extension of the LVDS line drivers and receivers family. They are specifically designed for multidrop and multipoint applications where the bus is terminated at both ends. They may also be used in heavily loaded backplanes where the effective impedance is lower than 100Ω. In this case, the drivers may see a load in the 30Ω to 50Ω range. Bus LVDS drivers provide about 10 mA of output current so that they provide LVDS swings with heavier termination loads. Transceivers and repeaters are currently available in this product family.

The 18-, 16-, and 10-bit serializer and deserializer families of devices are available that embed and recover clock and data from a single serial stream. These chipsets also provide a high level of integration with on-chip clock recovery circuitry. All deserializers provide a random data lock capability, an industry first. The deserializer can be hot-plugged in to a live data bus and does not require sending special characters for PLL training.

Special functions are also being developed using LVDS technology. This family provides additional functionality over the simple PHY devices. Currently a special low-skew clock transceiver with 6 CMOS outputs is available (DS92CK16) along with a line of crosspoint switches.

2.5 Conclusion

LVDS technology solutions eliminate the trade-offs in speed, power, noise, and cost for high-performance data transmission applications. In doing so, LVDS not only achieves great benefits in existing applications, but opens the door to many new ones.

Chapter 3
High-speed design

3.1 PCB layout tips

As a technology, LVDS is relevant in systems where the data rates range from around 100 MHz to 2 GHz. At these frequencies a PCB can no longer be treated as a simple collection of interconnects. Traces carrying these high-speed signals need to be treated like transmission lines. These transmission lines should be designed with appropriate impedance and they need to be correctly terminated.

The topics covered in this chapter range from impedance calculations and signal integrity to proper power-supply design. They are relevant for any high-speed design, whether it employs ECL, CML, or LVDS.

Generalized design recommendations are provided next.

The fast edge rate of an LVDS driver means that impedance matching is very important – even for short runs. Matching the differential impedance is important. Discontinuities in differential impedance will create reflections, which will degrade the signal and also show up as common-mode noise. Common-mode noise on the line will not benefit from the canceling magnetic field effect of differential lines and will be radiated as EMI.

Controlled differential impedance traces should be used as soon as possible after the signal leaves the IC. Try to keep stubs and uncontrolled impedance runs to <12 mm or 0.5 in. Also, avoid 90° turns since this causes impedance discontinuities; use 45° turns, radius or bevel PCB traces.

Minimize skew between conductors within a differential pair. Having one signal of the pair arrive before the other creates a phase difference between voltages along the signal pairs that appear and radiate as common-mode noise.

Use bypass capacitors at each package and make sure each power or ground trace is wide and short (do not use 50Ω dimensions) with multiple vias to minimize inductance to the power planes.

A detailed list of suggestions for designing with LVDS is shown next. The suggestions are cost-efficient and easy to implement. By using these suggestions as guidelines, your LVDS-based systems should provide maximum performance and be quick and easy to develop.

3.1.1 PCB design

1. Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals. Dedicating planes for V_{CC} and ground are typically required for high-speed design. The solid ground plane is required to establish a controlled (known) impedance for the transmission line interconnects. A narrow spacing between power and ground will also create an excellent high frequency bypass capacitance.
2. Isolate fast edge rate CMOS/TTL signals from LVDS signals, otherwise the noisy single-ended CMOS/TTL signals may couple crosstalk onto the LVDS lines. It is best to put TTL and LVDS signals on a different layer(s), which should be isolated by the power and ground planes.
3. Keep drivers and receivers as close to the (LVDS port side) connectors as possible. This helps to ensure that noise from the board is not picked up onto the differential lines and will not escape the board as EMI, from the cable interconnect. This recommendation also helps to minimize skew between the lines. Skew tends to be proportional to length; therefore, by limiting length, we also limit skew. Please see Chapter 5 for more information on routing high-speed signals through connectors.
4. Bypass each LVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best.

Power supply: A 4.7 µF or 10 µF, 35V tantalum capacitor works well between supply and ground. Choosing a capacitor value which best filters the largest power/ground frequency components (usually 100 MHz to 300 MHz) is best. This can be determined by checking the noise spectrum of V_{CC} across bypass capacitors. The voltage rating of tantalum capacitors is critical and must not be less than 5 x V_{CC}. Some electrolytic capacitors also work well.

V_{CC} pins: One or two multi-layer ceramic (MLC) surface mount capacitors (0.1 µF and 0.01 µF) in parallel should be used between each V_{CC} pin and ground if possible. For best results, the capacitors should be placed as close as possible to the V_{CC} pins to minimize parasitic effects that defeat the frequency response of the capacitance. Wide (>4 bits) and PLL-equipped (e.g., channel link and FPD-link) LVDS devices should have at least two capacitors per power type, while other LVDS devices are usually fine with a 0.1 µF capacitor. The bottom line is to use good bypassing practices.

EMI problems often start with power and ground distribution problems. EMI can be greatly reduced by keeping power and ground planes quiet. As a general rule of thumb, a target of <100 mV of noise on the power lines should be the target for power supply bypassing; however, some devices have more stringent requirements. Consult your device's datasheet for exact requirements.

1. Power and ground should use wide (low impedance) traces — their job is to be a low impedance point. Do not use 50Ω design rules on power and ground traces.
2. Keep ground PCB return paths short and wide. Provide a return path that creates the smallest loop for the image currents to return.
3. Cables should employ a ground return wire connecting the grounds of the two systems. This provides for common-mode currents to return on a short known path and is especially important in box-to-box applications where ground return paths will help limit shifts in ground potential. See Section 6.3.
4. Use two vias to connect to power and ground from bypass capacitor pads to minimize inductance effects. Surface mount capacitors are good as they are compact and can be located close to device pins.

3.1.2 Traces

1. Edge-coupled microstrip, edge-coupled stripline, or broad-side striplines all work well for differential lines.
2. Traces for LVDS signals should be closely coupled and designed for 100Ω differential impedance. See Section 3.1.3.
3. Edge-coupled microstrip lines offer the advantage that a higher differential Z_O is possible (100Ω to 150Ω). Also, it may be possible to route from a connector pad to the device pad without any via. This provides a "cleaner" interconnect. A limitation of microstrip lines is that these can only be routed on the two outside layers of the PCB, thus routing channel density is limited.
4. Stripline may be either edge-coupled or broad-side coupled lines. Since they are embedded in the board stack and typically sandwiched between ground planes, they provide additional shielding. This limits radiation and also limits coupling of noise onto the lines. However, they do require the use of vias to connect to them.

3.1.3 Differential traces

1. Use controlled impedance PCB traces that match the differential impedance of your transmission medium (e.g., cable) and termination resistor. Route the differential pair traces as close together as possible and as soon as they leave the IC. This helps to eliminate reflections and ensures that noise is coupled as common-mode. Signals that are 1 mm apart radiate far less noise than traces 3 mm apart, as magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

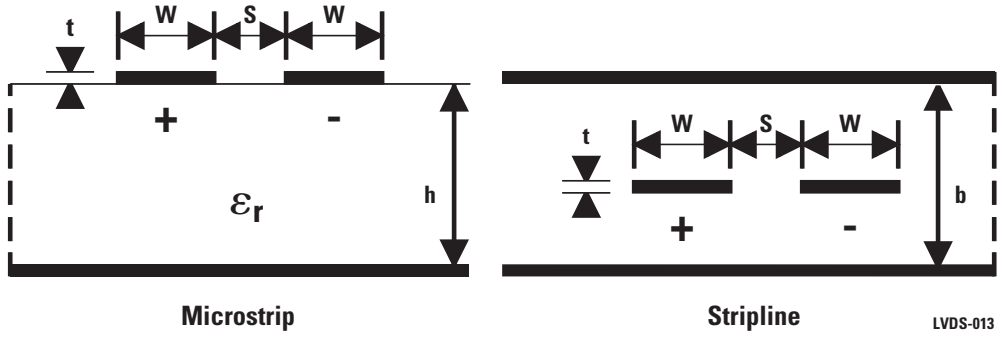


Figure 3.1. Microstrip and stripline differential traces

When designing for a specific differential Z_O (Z_{DIFF}) for edge-coupled lines, it is best to adjust trace width "W" to alter Z_{DIFF}. It is not recommended to adjust "S" which should be the minimum spacing specified by your PCB vendor for line-to-line spacing. You can obtain National's Transmission Line RAPIDESIGNER by visiting our website (search for Rapidesigner) or contact the National support center for your area. (Lit# 633200-001 metric or Lit# 633201-001 English units) and application note AN-905, (Lit# 100905-002) to calculate Z_O and Z_{DIFF}, or use the equations below for edge-coupled differential lines:

Microstrip

$$Z_{DIFF} \approx 2 \times Z_0 \left(1 - 0.48 e^{-0.96 \frac{S}{h}}\right) \Omega$$

Stripline

$$Z_{DIFF} \approx 2 \times Z_0 \left(1 - 0.374 e^{-0.29 \frac{S}{h}}\right) \Omega$$

Microstrip

$$Z_0 = \frac{60}{\sqrt{0.457 \varepsilon_r + 0.67}} \ell n \left(\frac{4h}{0.67\left(0.8W + t\right)}\right) \Omega$$

Stripline

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ell n \left(\frac{4b}{0.67\pi\left(0.8W + t\right)}\right) \Omega$$

Note: For edge-coupled striplines, the term "0.374" may be replaced with "0.748" for lines which are closely coupled (S < 12 mils).

Broadside coupled line structures can also be used. The dimensions for this type of line are shown in Figure 3.2. Broadside coupled striplines can be useful in backplane design as these use only one routing channel and may be easier to route through the connector pin field.

There is no closed-form equation for calculating the impedance of broadside-coupled stripline. Instead, a field solver should be used.

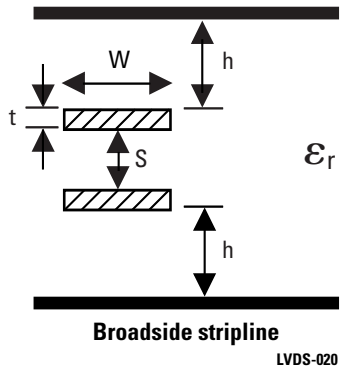


Figure 3.2. Broadside couple stripline

Always use consistent dimensions (e.g., all dimensions in mils, cm or mm) for S, h, W, and t when making calculations.

Cautionary note: The expressions for Z_{DIFF} were derived from empirical data and results may vary. Please refer to AN-905 for accuracy information and ranges supported.

Common values of dielectric constant (εr) for various printed circuit board (PCB) materials are given in Table 3.1. Consult your PCB manufacturer for actual numbers for the specific material that you plan to use. Note that in most LVDS applications, the widely used FR-4 PCB material is acceptable. GETEK is about 1.5x as expensive as FR-4, but can be considered for 1000+ MHz designs. Also note that ε_r will vary within a single board. It is not uncommon for FR-4 PCBs to vary by 10% across one board, affecting skew. This is another good reason to keep differential lines close together.

Table 3.1. Properties of PCB materials

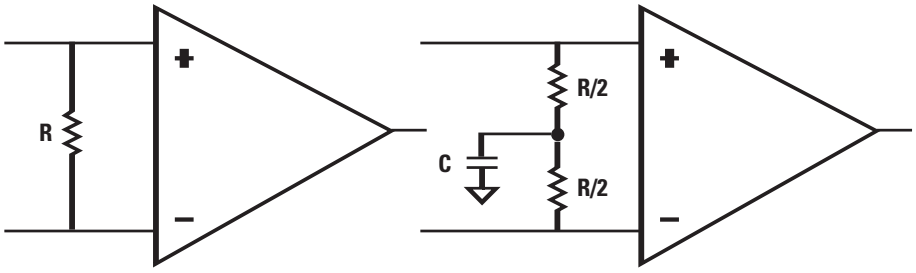
PCB material	Dielectric constant (′r)	Loss tangent
Air	1.0	0
PTFE (Teflon)	2.1 to 2.5	0.0002 to 0.002
BT resin	2.9 to 3.9	0.003 to 0.012
Polyimide	2.8 to 3.5	0.004 to 0.02
Silica (quartz)	3.8 to 4.2	0.0006 to 0.005
Polyimide/glass	3.8 to 4.5	0.003 to 0.01
Epoxy/glass (FR-4)	4.1 to 5.3	0.002 to 0.02
GETEK	3.8 to 3.9	0.010 to 0.015 (1 MHz)
ROGERS4350 core	3.48 ± 0.05	0.004 @ 10G, 23°C
ROGERS4403 prepreg	3.17 ± 0.05	0.005 @ 10G, 23°C

2. Match electrical lengths between traces of a pair to minimize skew. Skew between the signals of a pair will result in a phase difference between the signals. That phase difference will destroy the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, v = c/εr where c (the speed of light) = 0.2997 mm/ps or 0.0118 in./ps). A general rule is to match lengths of the pair to within 100 mils.

3. Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match trace length and to ensure isolation between pairs of differential lines.
4. Minimize the number of vias and other discontinuities on the line.
5. Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels instead.
6. Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable. The key to "imbalances" is to make as few as possible and as small as possible. Differential transmission works best on a balanced interconnect. For the best results, both lines of the pair should be as identical as possible.

3.1.4 Termination

1. Use a termination resistor that best matches the differential impedance of your transmission line. It should be between 90Ω and 130Ω for point-to-point cable applications. Remember that the current-mode outputs need the termination resistor to generate the proper differential voltage. LVDS is not intended to work without a termination resistor.
2. Typically, a single, passive resistor across the pair at the receiver end suffices.
3. Surface mount resistors are best. PCB stubs, component leads, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be <7 mm (12 mm max.).
4. Resistor tolerance of 1% or 2% is recommended. Note that from a reflection point of view, a 10% mismatch in impedance causes a 5% reflection. The closer the match, the better. Match to the nominal differential impedance of the interconnect. For multidrop/multipoint applications, match the differential impedance to the fully loaded case.
5. Center tap capacitance termination may also be used in conjunction with two 50Ω resistors to filter common-mode noise at the expense of extra components if desired. This termination is not commonly used or required.



Where R = Z_{DIFF} (between 100Ω and 120Ω), C ≈ 50 pF

Components should be surface-mount components, placed close to the receiver.

Use 1-2% resistors.

LVDS-015

Figure 3.3. Common differential termination schemes

3.1.5 The "S" Rule

Using the edge-to-edge "S" distance between the traces of a pair, other separations can be defined:

- The distance between two pairs should be >2S.
- The distance between a pair and a TTL/CMOS signal should be >3S at a minimum. Even better, locate the TTL/CMOS signals on a different plane isolated by a ground plane.
- If a guard ground trace or ground fill is used, it should be >2S away.

3.2 Lowering Electromagnetic Interference (EMI)

3.2.1 Electromagnetic radiation of differential signals

Today's increasing data rates and tough electromagnetic compatibility (EMC) standards are making electromagnetic radiation an increasing concern. System designers are usually most concerned with far field electromagnetic radiation, propagated through transverse electromagnetic (TEM) waves, which can escape through shielding and cause a system to fail EMC tests.

Fields around a conductor are proportional to voltage or current, which are small in the case of LVDS. The fields are distorted by and interact with their environment, which is why EMI is so hard to predict. The fields can be distorted to advantage, however, and such is the case with tightly coupled differential lines ("+" and "–" signals in close proximity with one another).

In single-ended lines like CMOS/TTL lines shown in Figure 3.4, almost all the electric field lines are free to radiate away from the conductor. Certain structures can intercept these fields. But some of these fields can travel as TEM waves which may escape the system and cause EMI problems.

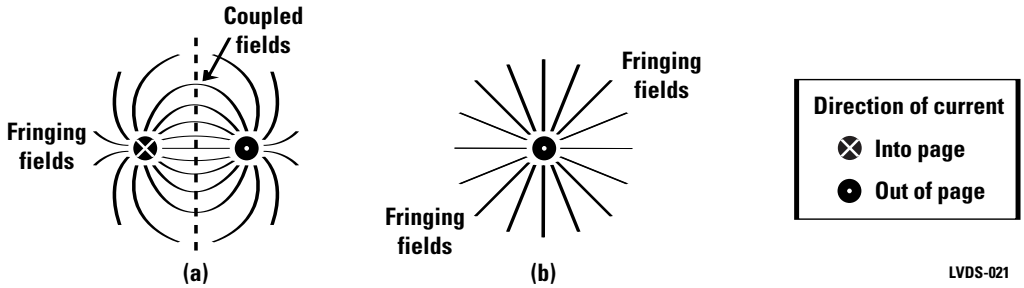


Figure 3.4. Electromagnetic field cancellation in differential signals (a) through coupling vs. a single-ended signal (b)

Balanced differential lines, however, have equal but opposite ("odd" mode) signals. This means that the concentric magnetic field lines tend to cancel and the electric fields (shown in Figure 3.4b) tend to couple. These coupled electric fields are "tied up" and cannot escape to propagate as TEM waves beyond the immediate vicinity of the conductors. Only the stray fringing fields are allowed to escape to the far field. Therefore, for coupled differential signals, much less field energy is available to propagate as TEM waves vs. single-ended lines. The closer the "+" and "–" signals, the tighter or better the coupling.

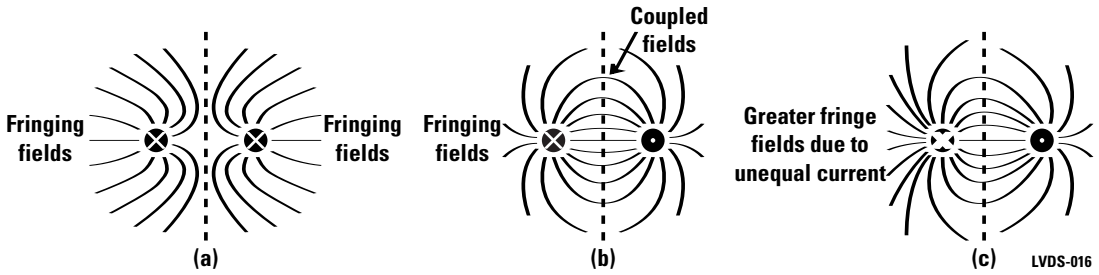


Figure 3.5. Even or common-mode signals (a), ideal equal and opposite odd mode signals (b), and unbalanced signals (c) on differential lines

Clearly, the voltages and currents of the two ("+" and "–") conductors are not always equal and opposite. For LVDS, the DC currents should never flow in the same direction as in Figure 3.5a, but factors can cause an imbalance in currents (c) vs. the ideal case in (b). When this imbalance happens, an excess of field fringing occurs since the field strength of the two conductors is unequal. The extra fringe fields can escape as TEM waves and lead to more EMI.

Similar effects can be seen in microstrip and stripline PCB traces shown in Figure 3.6. The ideal cases for microstrip and stripline are represented by (a) and (b). Here we see that the microstrip ground plane helps couple additional field lines from below, tying up more field lines and reducing EMI. Stripline almost completely shields the conductors and therefore can significantly decrease EMI, but has the penalty of slower propagation velocity (about 40% slower than microstrip), more PCB layers, additional vias, and difficulty in achieving 100Ω Z_O (Z_{DIFF}).

The use of shield traces with microstrip, as in Figure 3.6d, will result in more shielding without significantly impacting propagation velocity. Be careful to add the shield trace (preferably ground) on both sides of the pair (d). Running the shield trace – or any trace – on one side (c) creates an imbalance that can increase EMI. Ground trace shields should have frequent vias to the underlying ground plane at regular (<¼ wavelength) intervals, and should be placed at least 2S from the pair.

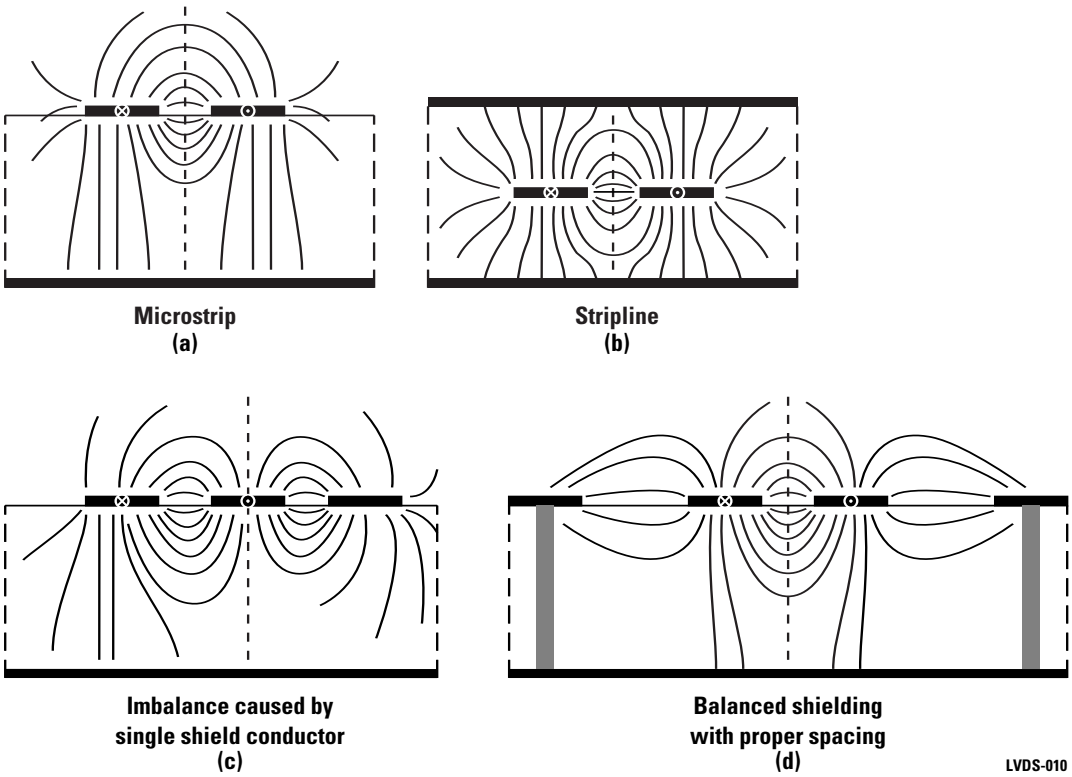


Figure 3.6. Ideal differential signals on microstrip (a) and stripline (b), negative effects of unbalanced shielding (c), and positive effects of balanced shielding (d)

3.2.2 Design practices for low EMI

As discussed in the preceding paragraphs, the two most important factors to consider when designing differential signals for low EMI are 1) close coupling between the conductors of each pair and 2) minimizing the imbalances between the conductors of each pair. Let us discuss close coupling first.

In order for sufficient coupling to occur, the space between the conductors of a pair should be kept to a minimum as shown in Figure 3.7. (Note that matched transmission impedance must also be maintained). Stripline power and ground planes/traces should not be closer than the distance between conductors. This practice will lead to closer coupling between the conductors, as compared with the coupling between each conductor and the power/ground planes. A good rule is to keep S < W, S < h, and x greater or equal to the larger of 2S or 2W. The best practice is to use the closest spacing, "S," allowed by your PCB vendor and then adjust trace widths, "W," to control differential impedance.

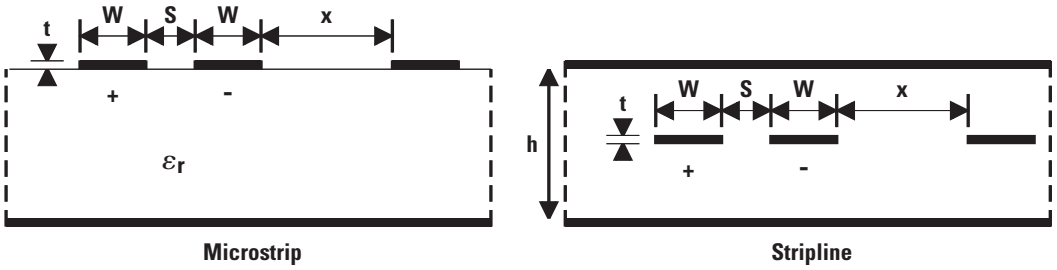


Figure 3.7. Coupling of differential traces

Minimize the distance between the "+" and the "-" signal to create sufficient coupling (canceling) of electromagnetic fields. As previously mentioned, close coupling between conductors of a pair reduces electromagnetic emissions. It also increases the immunity of the circuit to received electromagnetic noise. Noise coupled onto the conductors will do so as common-mode noise, which will then be rejected by the receiver. Since the differential pair is a current loop, minimizing conductor spacing also reduces the antenna loop.

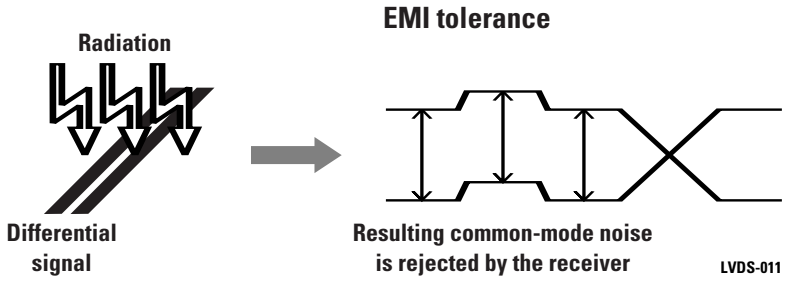


Figure 3.8. Close coupling not only reduces EM emissions, but improves EM immunity too

It is also important to minimize imbalances in order to reduce EMI. Complex interaction between objects of a system generate fields and are they are difficult to predict (especially in the dynamic case), but certain generalizations can be made. The impedance of your signal traces should be well controlled. If the impedances of two trace within a pair are different, it will lead to an imbalance. The voltage and fields of one signal will be different from its partner. This will tend to create more fringing fields and therefore more EMI as we have seen.

There is a basic rule to follow. Any unavoidable discontinuity introduced in proximity to differential lines should be introduced equally, to both members of the pair. Examples of discontinuities include: components, vias, power and ground planes, and PCB traces. Remember that the key word is balance.

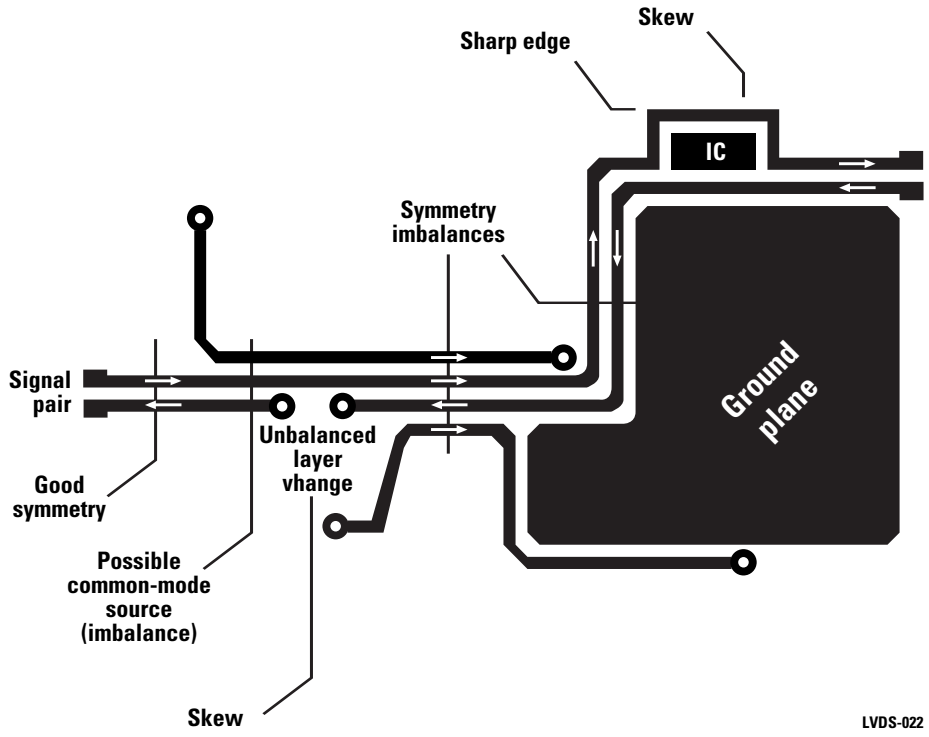


Figure 3.9. This PCB layout contains many sources of differential signal imbalance that will tend to increase electromagnetic radiation

Unfortunately unless you have an elaborate EMI lab, fields resulting from imbalances cannot easily be measured. Waveforms, however, are easy to measure. Fields are proportional to voltage/current amplitude at any given point in time. Any factors affecting the time (i.e., delay, velocity) and/or amplitude (i.e., attenuation) properties of the signals can increase EMI and can be seen on a scope. Figure 3.10 illustrates how waveforms – easily seen on a scope – can help predict far field EMI. First, the beneficial field canceling effects of ideal differential signals (b) vs. single-ended signals (a) are compared.

A real differential signal, however, is non-ideal and contains skew, unbalanced pulse widths and edge rates, common-mode noise, and unbalanced attenuation. These affect the relative amplitudes of the fields at any given moment, reducing the canceling effects of the differential signals, and potentially increasing EMI. Thus, the waveforms of one conductor of a pair should balance or mirror the other to minimize EMI.

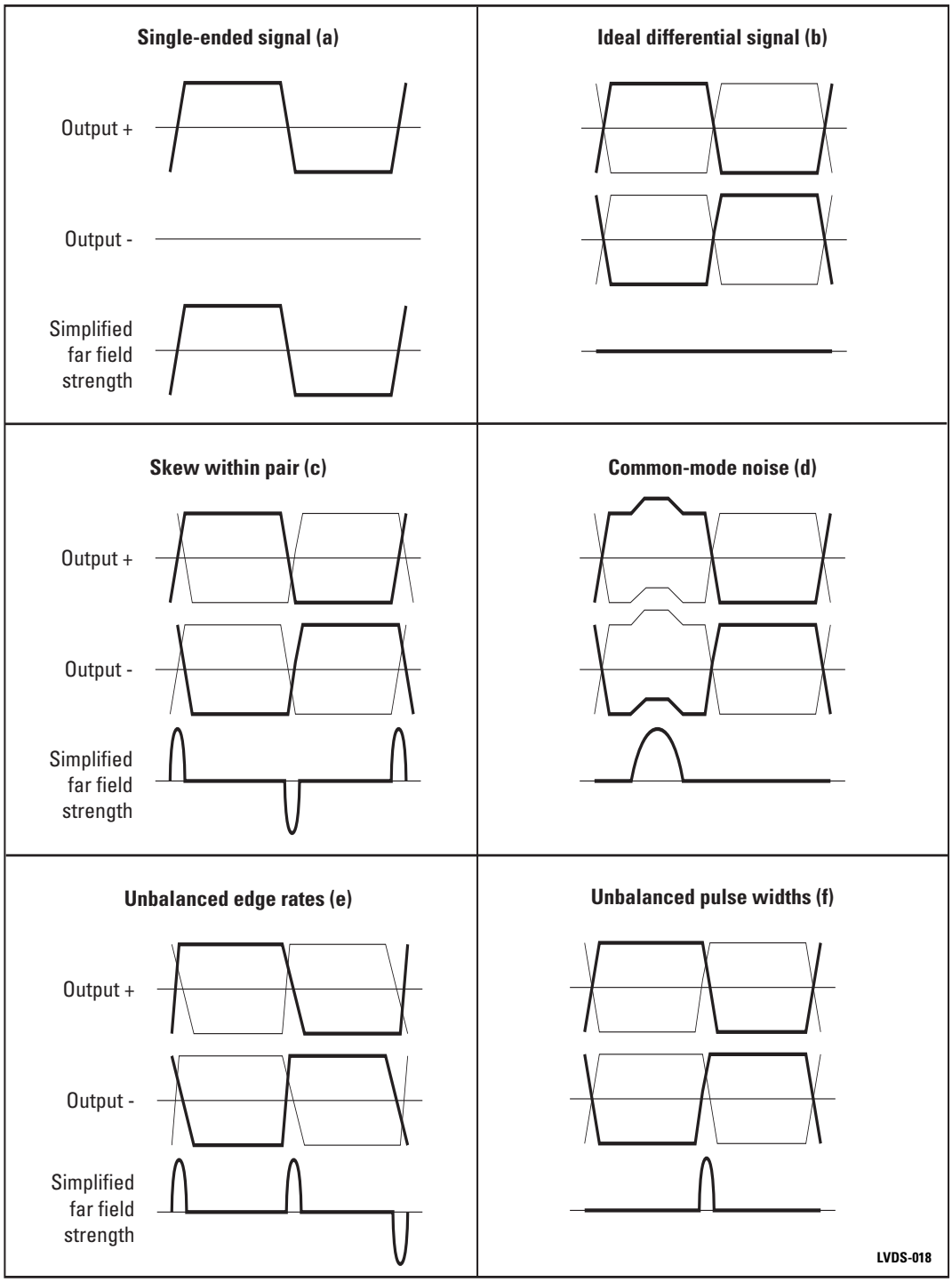


Figure 3.10. Diagram showing simplified far field radiation under various situations

3.2.3 EMI test results

The PCB setup shown below was used to examine the effects on EMI of closely coupled differential signals vs. uncoupled signals. The setup compares two sets of LVDS signals. One set contains pairs whose spacing is less than the trace width (S < W). The other set consists of pairs that are not closely coupled (S >> W). Note that the differential impedance of the widely spaced pair is still 100Ω.

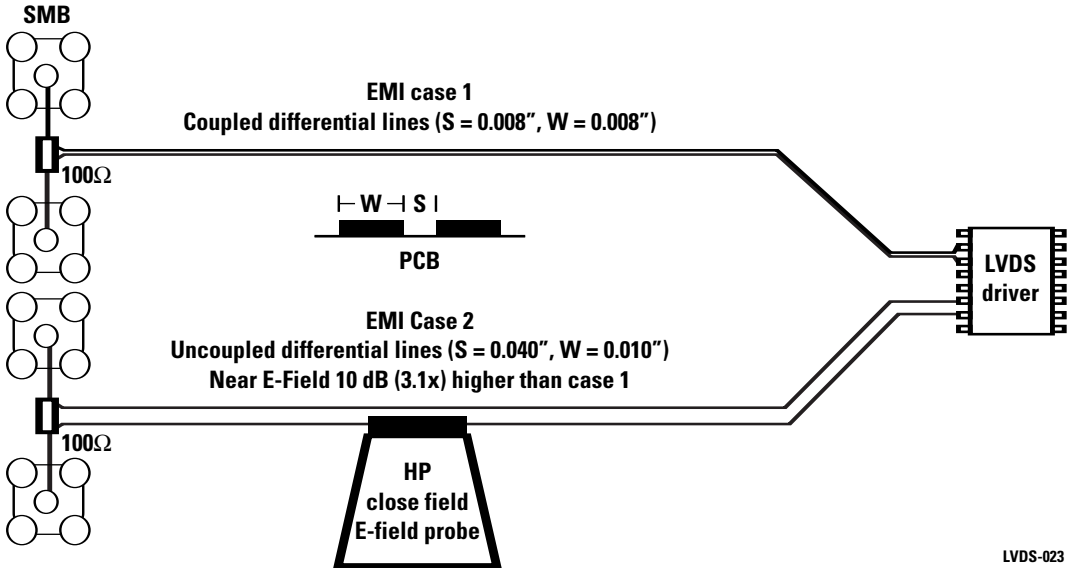


Figure 3.11. EMI test setup

Near (close) field electric field measurements were made for both cases while using a 32.5 MHz 50% duty cycle clock as the source. The plots in Figure 3.12 show the E-field strength results for case 2, the uncoupled case. The first plot shows the E-field strength over 200 MHz to 1 GHz. The second plot looks more closely at the frequencies between 30 MHz and 300 MHz. The electric field noise shows up as "spikes" which occur at harmonics of the input frequency.

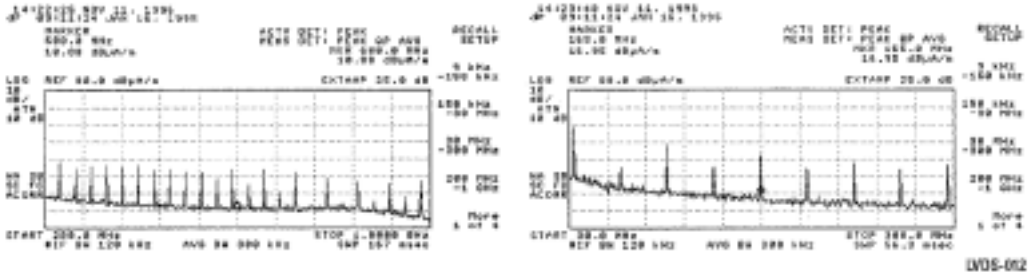


Figure 3.12. Near E-field strength for uncoupled signals
(Case 2): 200 MHz – 1 GHz (Case 2): 30 MHz – 300 MHz

The two plots in Figure 3.13 show the E-field strength for case 1 in which the differential pair is closely coupled. Notice that the harmonics are significantly reduced.

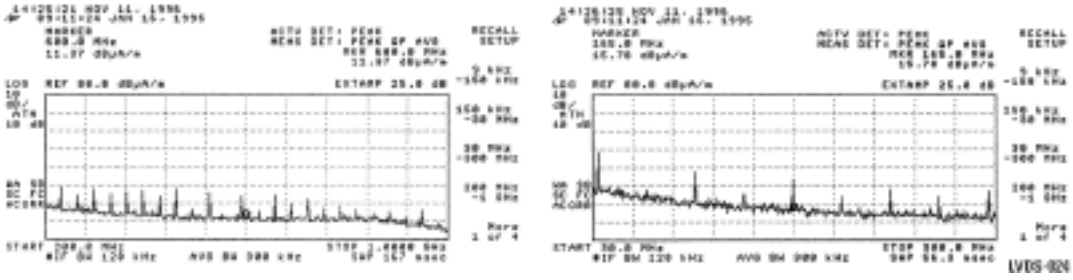


Figure 3.13 Near E-field strength for closely coupled signals
(Case 1): 200 MHz – 1 GHz (Case 1): 30 MHz – 300 MHz

In the far field, the EMI of the closely coupled pair should radiate much less due to the coupling of the electric fields. Even in the near field, however, the closely coupled pair generated much weaker electric fields. The electric field generated by the closely coupled pair was about 10 dB (>3x) lower than the field generated by the uncoupled pair.

This test illustrates two things:

1. Use of differential signals vs. single-ended signals can be used effectively to reduce emissions.
2. The EMI advantages of differential signs will be lost or greatly diminished unless the signals are closely coupled.

This test used uncoupled LVDS signals to represent single-ended signals. Most single-ended signals such as TTL or GTL, have a much greater swing and involve much greater currents, so their EMI is expected to be even greater than what is shown here.

3.2.4 Ground return paths

A conductor that carries current requires an opposite mirror current to return through some part of the system. This return current path will be the path of least resistance. For high-speed signals, the return current path will be the path of least inductance.

Since LVDS is differential, the signal current that flows in one conductor of a pair will flow back through the other conductor, completing the current-loop. This is ideal, because the current return antenna loop area is minimized since the traces of a pair are closely spaced. Real signals, however, will have some common-mode noise current, which must return also. This common-mode current will be capacitively coupled to ground and return to the driver through the path of least inductance. Therefore, a short ground current return path is needed between the driver and receiver in differential systems.

On PCBs, the best current return path is a uniform, unbroken ground plane beneath the LVDS signals. The ground plane will allow the common-mode (even mode) current to return directly under the LVDS signals. This closely coupled path is the path of least inductance and means that the current loop area is minimized.

Similarly, in cables, a ground return wire or wires should be used between driver and receiver. This allows the return path to be in close proximity to the signal pairs reducing the current loop area. (See Chapter 6 on Cables).

3.2.5 Cable shielding

Shielding is an effective way to reduce EMI. Shielding should be connected directly to both driver enclosure and receiver enclosure when possible. Shields are not designed to handle significant ground return currents, so it may be necessary to construct a filter network which isolates the shield from ground at one end (See Chapter 6).

3.2.6 EMC conclusion

To take advantage of the inherent low EMI properties of LVDS, designers should ensure the conductors of each pair are (1) closely coupled and (2), well-balanced. Impedance, both single-ended and differential, should be controlled and matched.

3.3 AC-coupling

Why would you want to AC-couple a signal?

1. To change the DC bias voltage when interfacing logic families with different input thresholds (such as optical systems where LVDS and PECL are used), or
2. To protect drivers from possibly getting shorted when used in a removable interface (such as on cards used in network switches and routers), or
3. To prevent DC currents flowing between systems with different ground potentials

If your application meets one of these requirements and you are using encoded data, use AC-coupling.

AC-coupling works best with encoded data that provides an equal number of ones and zeros (a DC-balanced signal). Just to name a few, 50% duty-cycle clocks, 8b/10b coding, and Manchester-coded data are all examples of DC-balanced signals. DC-balanced data should be used when AC-coupled.

For signals with good DC-balancing, the useful spectral content of the data usually has a low frequency cutoff, and it is possible to pass the information with minimal degradation in content. However, for any signal passed through an AC-coupling circuit, you should expect a small portion of the signal to be filtered out.

When AC-coupling is used, the DC common-mode bias voltage used in LVDS and many other logic families is lost. Although many devices have a wide common-mode operating voltage range, this should be verified in the device's datasheet. For devices limited in common-mode operating range, a simple bias circuit can be used to properly bias the signal.

The most common method of AC-coupling is to use a DC-blocking capacitor. For high-speed designs, the smallest available package should be used. This will help minimize degradation of the signal due to package parasitics.

LVDS-091

Figure 3.14. AC-coupling

To find the appropriate capacitor value to use, you can use the following equation as a rough approximation:

$$C = \frac{\left(7.8 \times N \times Tb\right)}{R}$$

Tb = bit period
R = impedance
N = the maximum number of consecutive identical bits

Every AC-coupled signal will have some droop in amplitude when passed through a capacitor. The equation listed above takes into account a 0.25 dB droop.

The most commonly used capacitor values found in high-speed applications are 0.1 µF and 0.01 µF capacitors. These capacitors are easy to find and have sufficient bandwidth to support most high-speed data rates.

For applications where edge rates are very fast, placing the AC-coupling capacitors closer to the receiver inputs may provide better results since edge rates will be slower.

In general, for logic interconnects within the same PCB, a simple DC-coupled interface is best. If AC-coupling must be used, then make sure that DC-balanced data is used.

Chapter 4
Designing with LVDS

4.1 Introduction

LVDS has low-swing, differential, ~3.5 mA current-mode outputs that can help reduce noise/EMI significantly, but these outputs switch (rise and fall) in less than a nanosecond, which means that almost every interconnect will act as a transmission line. Therefore, knowledge of ultra-high-speed board design and differential signal theory is required. Designing high-speed differential boards is not difficult or expensive. So familiarize yourself with the techniques outlined in Chapter 3 before you begin your design.

4.1.1 High-speed layout

See Chapter 3.

4.1.2 Unused pins

LVDS inputs - Leave unused LVDS receiver inputs open (floating) for LVDS receivers unless directed differently by the specific component's datasheet. Their internal failsafe feature will provide sufficient biasing to put the outputs in a known state. These unused receiver inputs should not be connected to noise sources such as cables or long PCB traces - float them near the pin. LVDS receivers are high-speed, high-gain devices, and only a small amount of noise, if picked up differentially will cause the receiver to respond. This causes false transitions on the output and increases power consumption.

LVDS and TTL outputs - Leave all unused LVDS and TTL outputs open (floating) to conserve power. Do not tie them to ground.

TTL inputs - Tie unused TTL transmitter/driver inputs and control/enable signals to power or ground or in certain cases they may be left open if the datasheet supports this condition. Some devices provide internal pull down (or up) devices to bias the pins. Again, consult the datasheet for information regarding the device's features. This type of information is typically included in the pin description table.

4.1.3 Probing LVDS transmission lines

Always use a high impedance (>100 kΩ), low capacitance (<0.5 pF) probe/scope with a wide bandwidth (>1 GHz). Improper probing will give deceiving results. LVDS is not intended to be loaded with a 50 Ω load to ground. This will distort the differential signal and offset voltages of the driver.

Differential probes are recommended over two standard scope probes due to match and balance concerns. Probe/scope combinations should have enough bandwidth to properly monitor the signal. Tektronix and Agilent (HP) both make probes that are well suited for measuring LVDS signals. (See Chapter 7)

4.1.4 Loading LVDS I/O – preserving balance

Avoid placing any devices which heavily load the low, ~3.5 mA LVDS output drive. If additional ESD protection devices are desired, use components, which do not add a significant load to the LVDS output. Some of the connectors with integrated polymer ESD protection are a good option.

Try not to disturb the differential balance. Treat both members of a pair equally.

4.2 Results of good vs. bad design practices

4.2.1 Impedance mismatches

It is very common for designers to automatically use off-the-shelf cables and connectors and 50Ω autorouting when making new designs. While this may work for some LVDS designs, it can lead to noise problems. Remember that LVDS is differential and does have low-swing, current-mode outputs designed to reduce noise. However, the transition times are quite fast. This means impedance matching (especially differential impedance matching) is very important. Those off-the-shelf connectors and that cheap blue ribbon cable are not meant for high-speed signals (especially differential signals) and do not always have controlled impedance.

Figure 4.1 shows a time-domain reflectometer (TDR) impedance trace of such a system. As one can plainly see, impedances are neither matched nor controlled. This example is not the worst case – it is a typical example reflecting common TTL design practices. The reflections caused by impedance mismatching will generate a lot of noise and EMI.

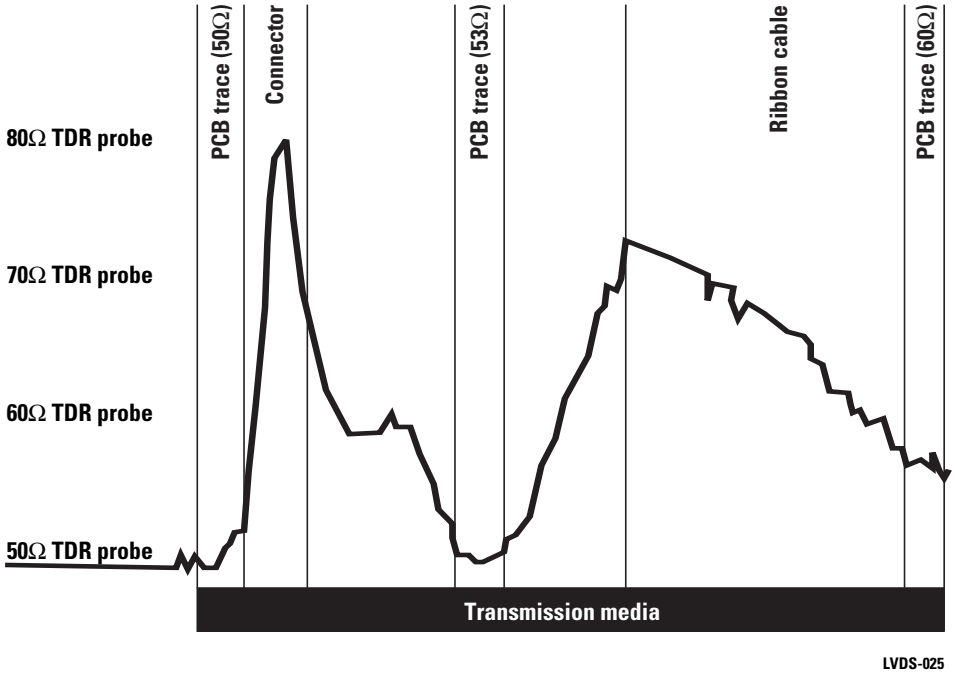


Figure 4.1. TDR plot of transmission media with mismatched impedance

Figure 4.2 is a trace of an improved design that follows most of the high-speed differential design practices discussed in Chapter 3. The TDR differential impedance plot is much flatter and noise is dramatically reduced.

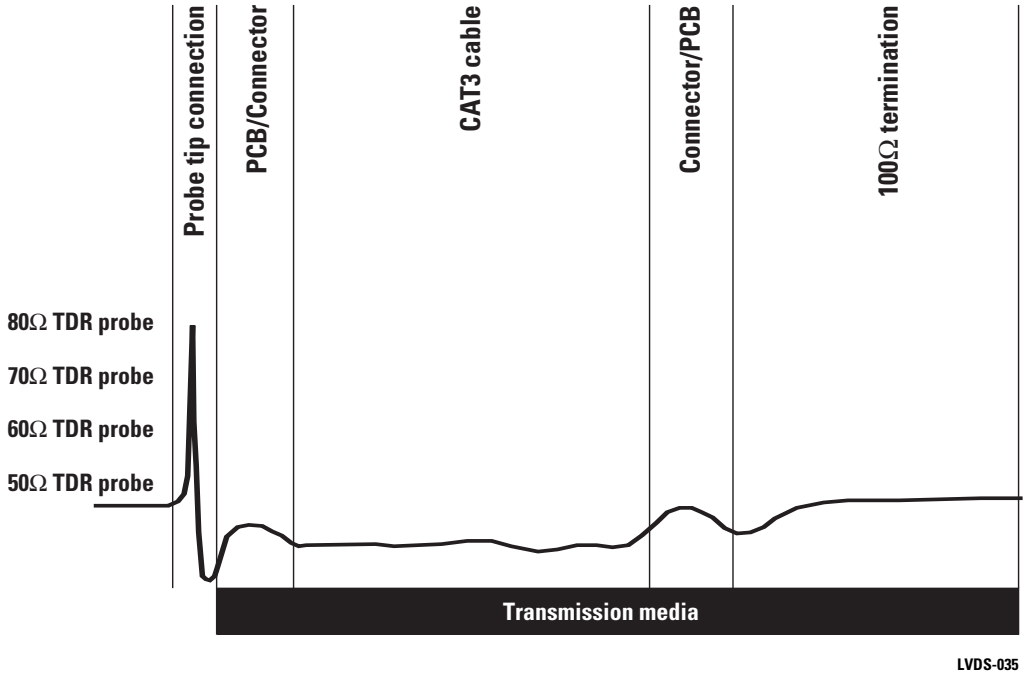


Figure 4.2. Minimize impedance variations for best performance

4.2.2 Crosstalk between TTL and LVDS signals

Figure 4.3 and 4.4 show the effects of TTL coupling onto LVDS lines. Figure 4.3 shows the LVDS waveforms before coupling. The second shows the effects of a 25 MHz, 0V to 3V TTL signal upon the LVDS signals running adjacent for 4 in. The result is an LVDS waveform modulated by the TTL signal. Note that the LVDS pair is not affected exactly equally – the signal which runs closest to the TTL trace is affected more than the other. The receiver will not reject this difference as common-mode noise. While it will not falsely trigger the receiver, it does degrade the signal quality of the LVDS signal and reduce noise margin. The common-mode noise will be rejected by the receiver, but can radiate as EMI.

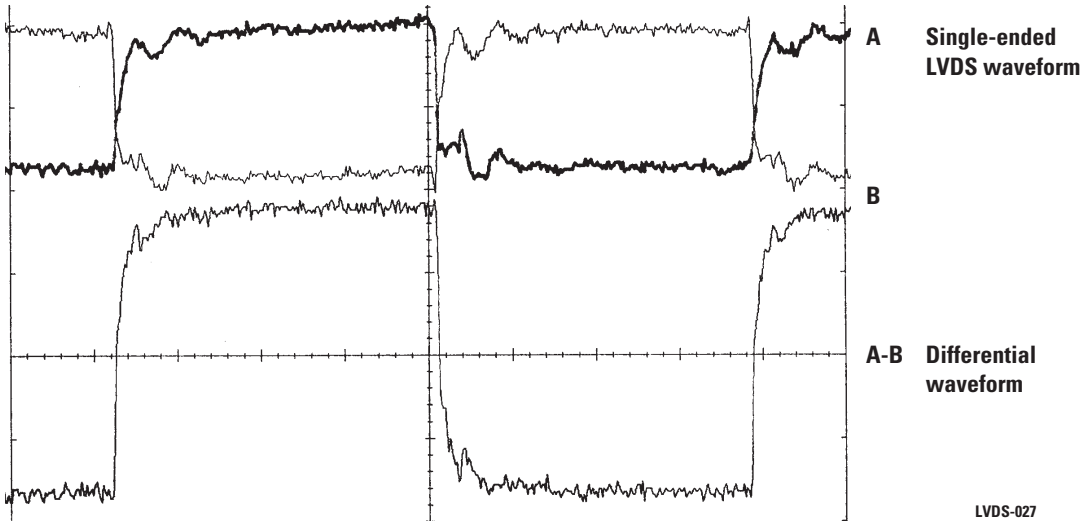


Figure 4.3. LVDS signals before crosstalk

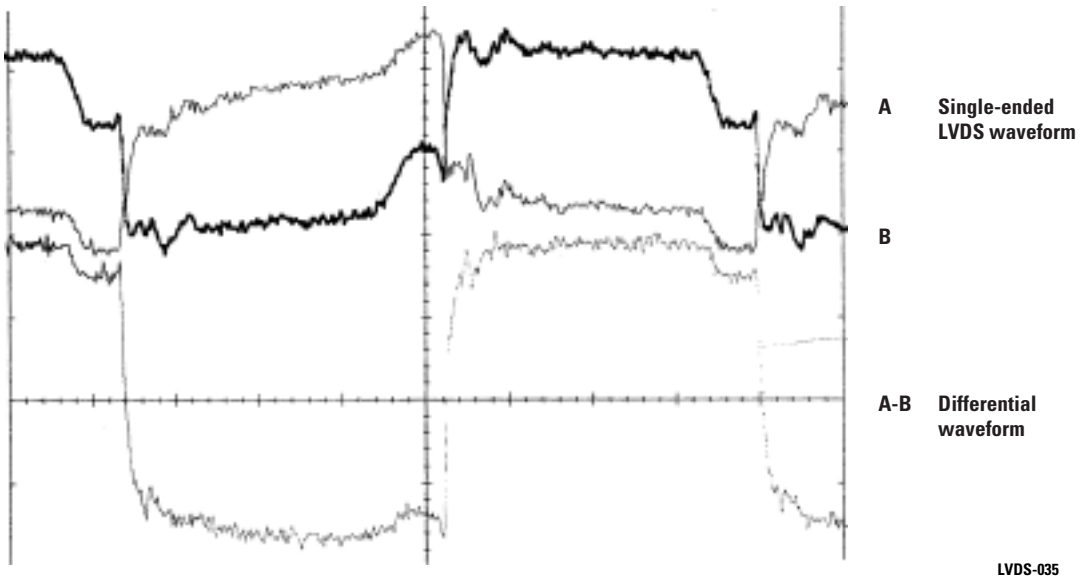


Figure 4.4. LVDS signals affected by TTL crosstalk

4.2.3 Interfacing LVDS backplane drivers with FPGAs

There is a simple but common mistake that many designers make when interfacing their LVDS ICs with their FPGAs (or ASICs). They overdrive the single-ended signal from the FPGA into the LVTTL I/O of the LVDS transmitter.

Many FPGAs are capable of driving signals over short backplanes. For that purpose, the output driver can be set to drive large amplitude signals, perhaps even with pre-emphasis. When that large signal is sent over only 3 to 6 in. of FR4 to the input stage of an LVDS buffer, it will cause problems.

The designer should avoid saturating the inputs of backplane drivers by lowering the signal amplitudes from the FPGA.

4.3 Lowering Electromagnetic Interference (EMI)

4.3.1 LVDS and lower EMI

High-speed data transmission usually means fast edge rates and high EMI. LVDS, however, has many positive attributes that help lower EMI:

1. The low output voltage swing (~350 mV)
2. Relatively slow slew rates, $\frac{\Delta V}{\Delta t} \sim \frac{0.350V}{0.350\,ns} = 1\text{V / ns}$
3. Differential (odd mode operation) so magnetic fields tend to cancel
4. “Soft” output corner transitions
5. Minimum ICC spikes due to low current-mode operation and internal circuit design

To realize these advantages, however, designers must take care to ensure the close proximity of the pair conductors and to avoid creating impedance imbalances within a pair. The following sections describe these EMI-friendly design practices.

4.4 Common-mode noise rejection

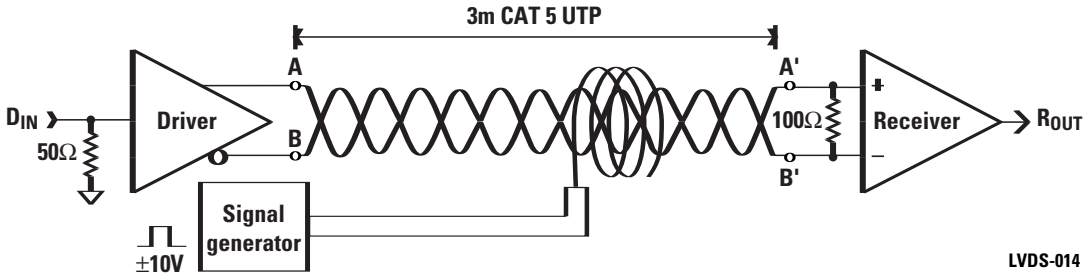


Figure 4.5. Common-mode noise rejection test setup

Test setup:

- Driver: DS90C031 (one channel)
- Receiver: DS90C032 (one channel)
- V_{CC} = 5V
- T_A = 25°C

This test demonstrates the common-mode noise rejection ability of National's LVDS receivers. Some have expressed concern over the noise immunity of LVDS because of its low voltage swing (±350 mV swing with <±100 mV thresholds). Provided that the differential signals run close together through controlled impedance media, most of the noise on LVDS lines will be common-mode. In other words, EMI, crosstalk, and power/ground shifts will appear equally on each pair and this common-mode noise will be rejected by the receiver. The plots below show common-mode noise rejection with V_{CM} noise up to –0.5V to +3.25V peak-to-peak.

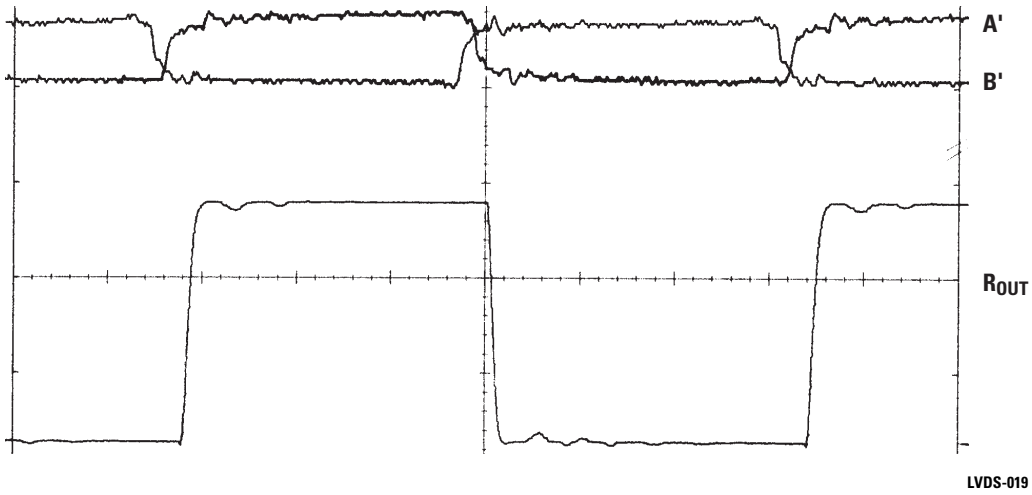


Figure 4.6. Reference waveform showing LVDS signal and receiver output

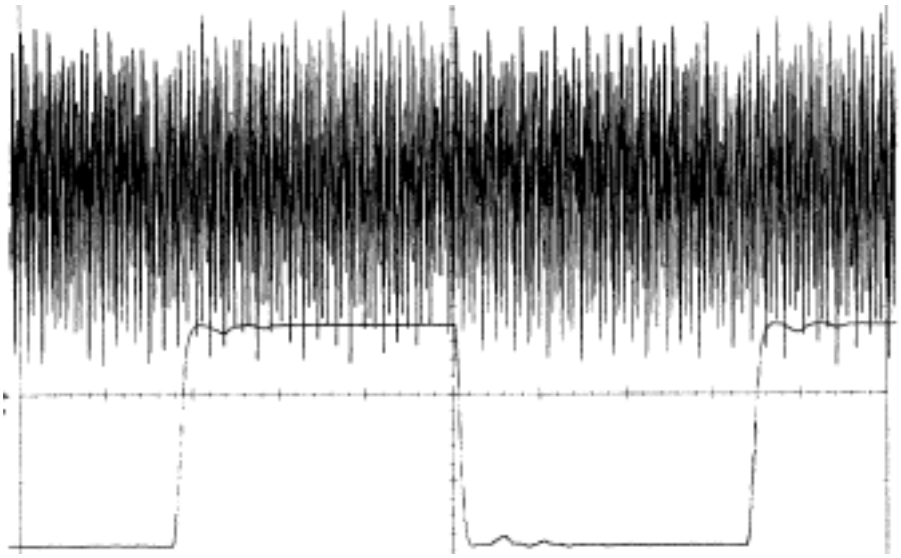


Figure 4.7. Coupled common-mode noise of 0.5V to 1.75V peak-to-peak and resulting clean receiver output

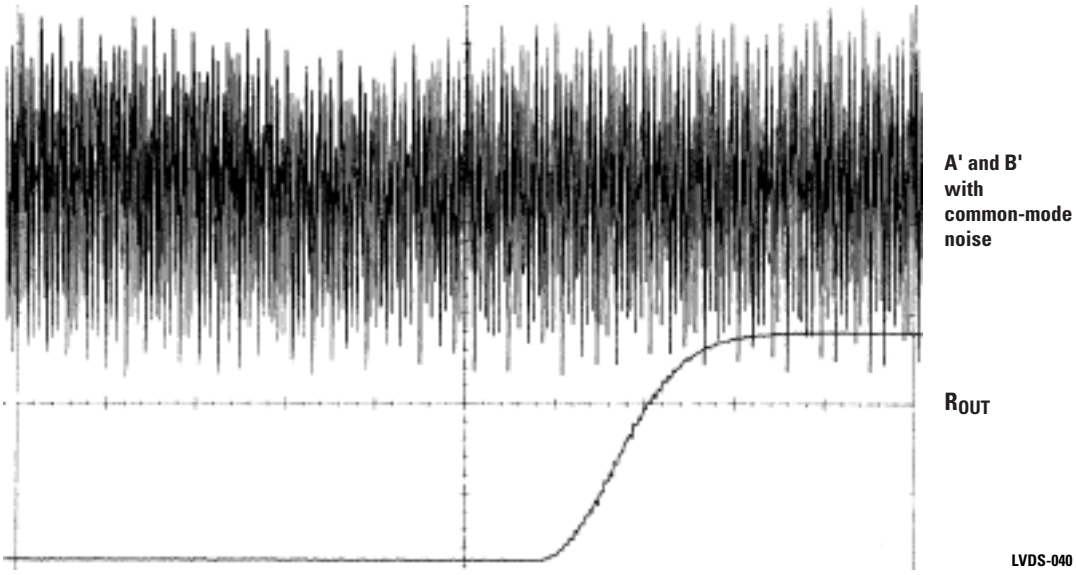


Figure 4.8. Expanded view of coupled common-mode noise waveform and clean receiver output

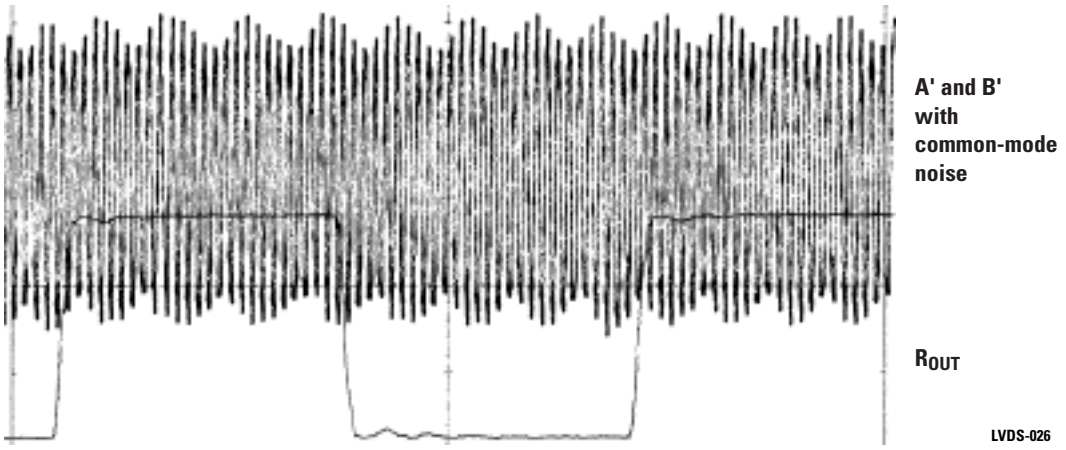


Figure 4.9. Clean receiver output despite –0.5V to +3.25V peak-to-peak common-mode noise

4.5 LVDS configurations

Unlike many other technologies such as ECL and CML which are more limited in configurations, LVDS has many possible configurations.

Figure 4.10. Point-to-point configuration

LVDS drivers and receivers are typically used in a point-to-point arrangement (Figure 4.10), but other topologies are possible. The point-to-point configuration does provide the best signal path and should be used for very high-speed interconnect links. Point-to-point links are commonly used in conjunction with crosspoint switches.

The configuration shown in Figure 4.11 allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin) if using standard LVDS drivers. A better solution would be to employ Bus LVDS drivers, which are designed for double termination loads. The simplest configuration for bi-directional communication is to implement a LVDS or Bus LVDS transceiver. They provide levels compatible with LVDS and do not trade off noise margin. Common-mode range for LVDS and Bus LVDS is ±1V (typical), so cable lengths tend to be in the tens of meters.

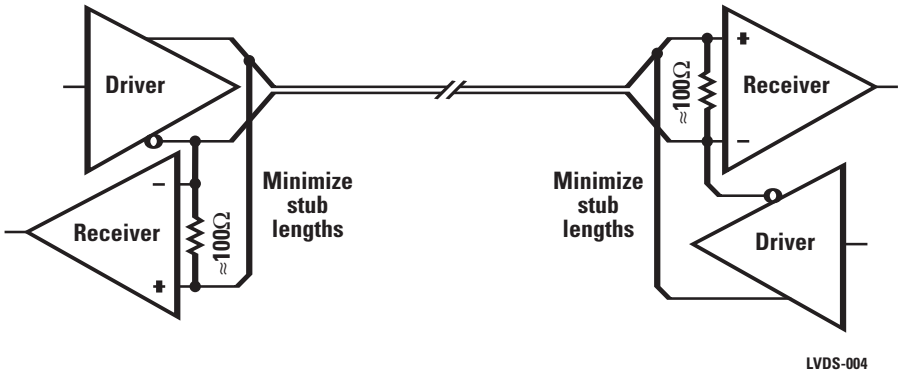


Figure 4.11. Bi-directional half-duplex configuration

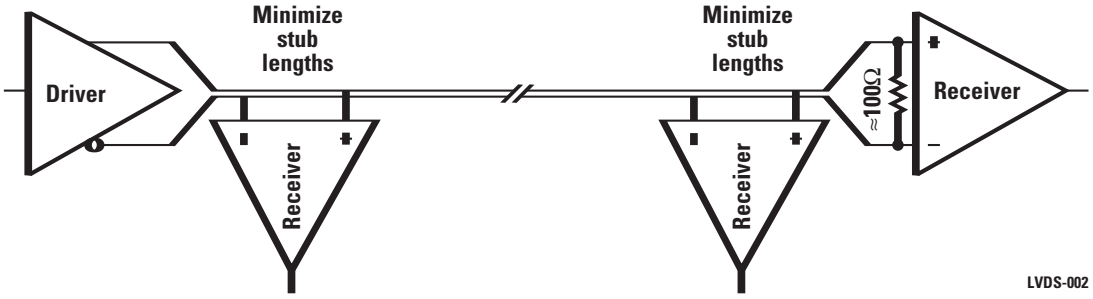


Figure 4.12. Multidrop configuration

LVDS receivers have high impedance inputs, so a multidrop configuration can also be used. A multidrop configuration will be most effective when transmission distance is short and stub lengths are less than ~15 mm (as short as possible). Use receivers with power-off high impedance if the network needs to remain active when one or more nodes are powered down. This application is good when the same set of data needs to be distributed to multiple locations.

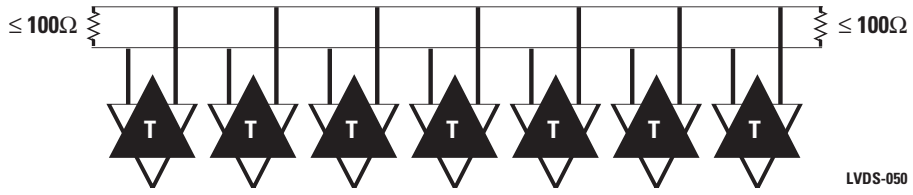


Figure 4.13. Multipoint configuration

A multipoint bus supports multiple drivers, but only one is allowed to be active at any given time.

With Bus LVDS devices, double terminated busses can be used without trading off signal swing and noise-margin. Termination should be located at both ends of the bus. Failsafe biasing should be considered if a known state on the bus is required when all drivers are in TRI-STATE®. When a designer is working with the multidrop bus, he should keep stubs off the mainline as short as possible, and he should pay special attention to device edge-rate specifications. Faster edge-rates will increase transmission line effects caused by long stubs.

4.6 Failsafe biasing of LVDS

4.6.1 Most applications

Most LVDS receivers have internal failsafe circuitry that forces the output to be in a known logic state (HIGH) under certain fault conditions. These conditions include open, shorted, and terminated receiver inputs. Always consult the component's datasheet to determine which type of failsafe protection is supported. Here is a summary of LVDS failsafe conditions:

Open input pins - Unused receiver inputs should be left OPEN. Do not tie unused receiver inputs to ground or other voltages. The internal failsafe bias resistors will pull the "+" input high, and the "–" input low, thus guaranteeing a high, stable output state. This minimizes power dissipation and switching noise.

Terminated input pins - If the cable is removed and the inputs to the receiver have a termination resistor across them, then the output will be stable (HIGH). Noise picked up at the input, if differential in nature, can cause the device to respond. If this is the case see Section 4.6.2.

Terminated input pins - Noisy Environments - See Section 4.6.2 if failsafe must be guaranteed in noisy environments when the cable is disconnected from the driver's end or if the driver is in TRI-STATE.

Shorted inputs - The receiver output will remain in a high state when the inputs are shorted. This is considered a fault condition protection only. It is not specified across the input voltage range of the receiver.

With some devices, such as National's Bus LVDS family of devices, outputs may also be in other states, such as TRI-STATE, when used in the configurations stated above. Please consult the specific device's datasheet for details.

4.6.2 Boosting failsafe in noisy environments

The internal failsafe circuitry is designed to source/sink a very small amount of current, providing failsafe protection for floating receiver inputs, shorted receiver inputs and terminated receiver inputs as described above and in the component's datasheet.

It is not designed to provide failsafe in noisy environments when the cable is disconnected from the driver or receiver's end or if the driver is in TRI-STATE. When this happens, the cable can become a floating antenna, which can pick up noise. If the cable picks up more differential noise than the internal failsafe circuitry can overcome, the receiver may switch or oscillate. If this condition occurs in your application, it is recommended that you choose a balanced and/or shielded cable, which will reduce the amount of differential noise on the cable.

In addition, you may wish to add external failsafe resistors to create a larger noise margin. However, adding more failsafe current will tend to unbalance the symmetrical LVDS output drive (loop) current and degrade signal quality somewhat. Therefore, a compromise should be the ultimate goal.

4.6.3 Choosing external failsafe resistors

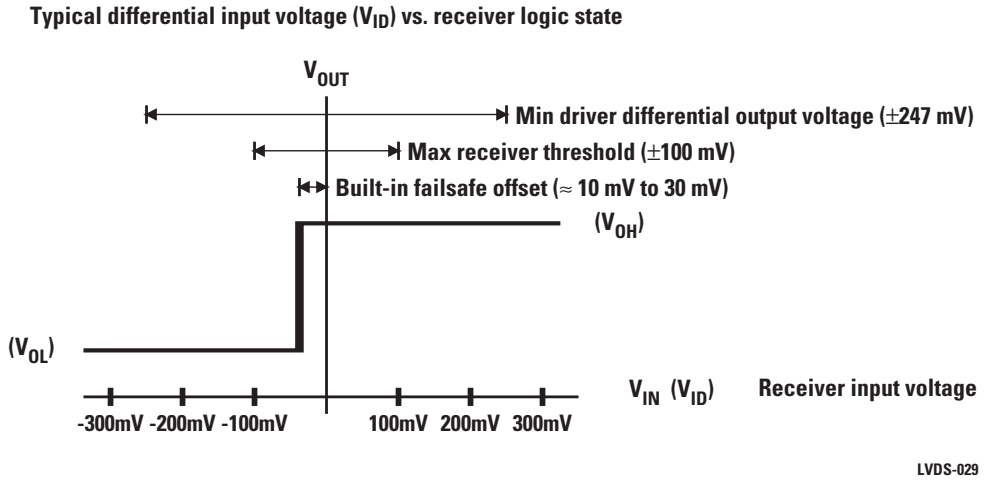


Figure 4.14. External failsafe can be added, but must be small enough not to significantly affect driver current

Figure 4.14 shows that National's present LVDS devices typically have an internal failsafe voltage of about -10 mV to 30 mV. If the driver in your application will not always actively drive the receiver and the cable is expected to pick up more than 10 mV of differential noise, you may need to add additional failsafe resistors.

The resistors are chosen by first measuring/predicting the amount of differential-mode noise you will need to overcome. V_{FSB} is the offset voltage generated across the termination resistor (typically 100Ω). Note that you do not need to provide a bias (V_{FSB}) that is greater than the receiver threshold (100 mV). Typically +15 mV or +20 mV is sufficient. You only need enough to overcome the differential noise, since the internal failsafe circuitry will always guarantee a positive offset. In fact, making V_{FSB} too large will contend with the driver output causing the driven signal to become imbalanced and reduce signal quality.

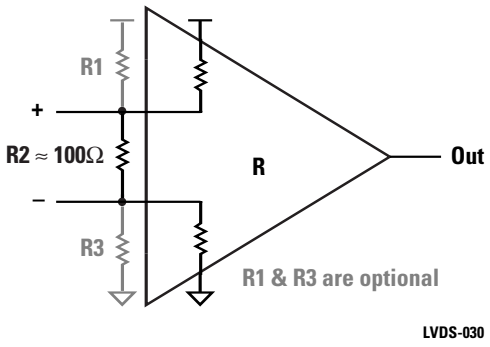


Figure 4.15. Simplified internal failsafe circuitry and optional external "helper" failsafe resistors

For best results, follow these procedures when choosing external failsafe resistors:

1. First ask the question "Do I need external failsafe?" If your LVDS driver is always active, you will not need external failsafe. If the cable is never disconnected from the driver end while the system is active and/or your cable will not pick up much differential-mode noise, you may not need to boost failsafe. If you have a noisy backplane application where the driver does not always drive the receiver, or if the driver card can be unplugged, then you may need additional failsafe biasing.

2. Measure/predict the amount of differential-mode noise at the receiver end of the cable in worst-case conditions. If you measure a great deal of noise, use a balanced cable such as twisted pair cabling. UTP cables tends to mostly pick up common-mode noise and not differential-mode noise. Do not use simple ribbon cables that can pick up differential-mode noise due to fixed positions of the conductors.

   Use a shielded cable whenever possible. Using a balanced and/or shielded cable is the best way to prevent noise problems in noisy environments.

3. Once you have chosen the appropriate cable, measure the amount of differential voltage at the receiver under worst-case conditions. Set this equal to V_{FSB} in the equation below and solve for the external failsafe resistors R1 and R3.

4. You now have an equation relating R1 to R3. Choose R1 and R3 so that: (1) they approximately satisfy the third equation for V_{CM} = 1.2V, and (2) they are large enough that they do not create a bias which will contend with the driver current ($I_{BIAS} << I_{LOOP}$, equation two). In general, R1 and R3 should be greater than 20 kΩ for V_{CC} = 5V and greater than 12 kΩ for V_{CC} = 3.3V. Remember that you want just enough I_{BIAS} to overcome the differential noise, but not enough to significantly affect signal quality.

5. The external failsafe resistors may change your equivalent termination resistance, R_{TEQ}. Fine-tune the value of R2 to match R_{TEQ} to within about 10% of your differential transmission line impedance.

See AN-1194 - Failsafe Biasing of LVDS Interfaces

4.7 Power-off high-impedance bus pins

Power-off high-impedance is a useful feature; most second and third generation LVDS receivers provide this feature. This is typically listed as a feature and also as a condition of the I_{IN} parameter. This feature is useful in applications that employ more than one receiver and they are powered from local power supplies. If the power is turned off to one node, it should not load down the line and prevent communication between other powered-up nodes.

Chapter 5
Backplane design considerations and Bus LVDS

Many high-speed applications require more than just the ability to run point-to-point or from one driver to multiple receivers. Multiple driver(s) and/or receiver(s) on one interconnect is an efficient and common bus application. This requires a double termination of the interconnect to properly terminate the signal at both ends of the bus. Multipoint configurations offer an efficient balance between interconnect density and throughput. LVDS drivers are not intended for double termination loads, thus an enhanced family of devices was invented by National to bring the advantages of LVDS to bus applications.

For multidrop (with the driver located in the middle) and multipoint applications, the bus normally requires termination at both ends of the media. If the bus were terminated with 100Ω at both ends, a driver in the middle would see an equivalent load of 50Ω. Depending upon the load spacing, the effective impedance of the bus may drop further, and for signal quality reasons, the terminations may be as low as 60Ω. Again, a driver would see both resistors in parallel, thus a 30Ω load.

Standard (644) LVDS drivers have only 3.5 mA of loop current. If these were used to drive the doubly terminated bus with a termination load of 30Ω, they would only generate a 105 mV differential voltage on the bus. This small differential voltage is not sufficient when noise margins, reflections, over-drive and signal quality are taken into account. In fact, even doubling the drive is not enough for a heavily loaded backplane application.

Bus LVDS addresses the issue of driving a low impedance interconnect by boosting its driver current to about 10 mA. This means that into a load as low as 30Ω, a 300 mV differential signal is maintained. Thus, LVDS-like signaling with all of its benefits is obtained in doubly terminated bus applications.

5.1 Configurations

Backplanes present special challenges to data transmission systems. This is due to the variety of interconnections (multidrop, multipoint, and switch fabrics) and also the close spacing of the loads. For these very reasons, National invented the Bus LVDS family of interface devices to extend the benefits of LVDS into backplane applications, which commonly require two terminations.

There are a number of ways of implementing high-speed backplanes. Each of these ways of implementing a backplane has advantages and disadvantages.

5.1.1 Multidrop (single termination)

A multidrop bus consists of one transmitter and multiple receivers (broadcast bus). Note that the driver is restricted to be located at one end of the bus and the other end is terminated. This configuration is useful for data distribution applications and may employ standard LVDS or Bus LVDS devices depending upon loading.

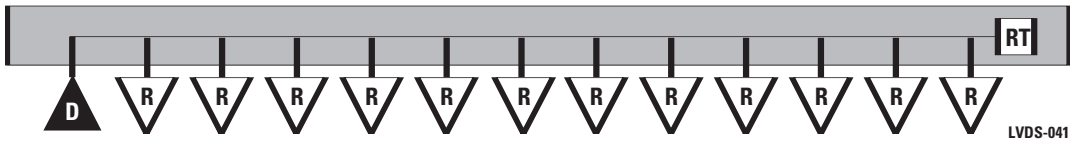


Figure 5.1. Multidrop application with a single termination

This architecture lends itself to serialization of the bus but without the need for a central switch card/chip. Serialization results in less interconnect (fewer connector pins and backplane traces) which in many cases reduces the stack-up of the backplane to fewer layers.

A disadvantage of this configuration is the restricted location of the driver, and (if required) complexity of a back channel (communication path from the loads back to the source).

5.1.2 Multidrop (double termination)

A multidrop bus consists of one transmitter and multiple receivers (broadcast bus). Note that with Bus LVDS, the driver can be placed anywhere in the multidrop bus and the bus is terminated at both ends.

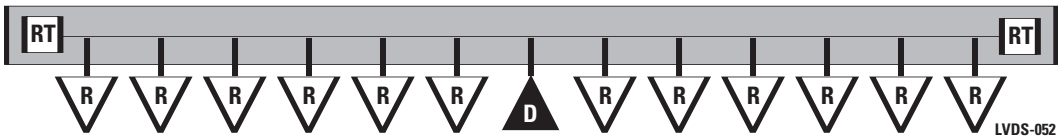


Figure 5.2. Multidrop application with double termination

Again, this architecture lends itself to serialization of the bus but without the need for a central switch card/chip. Serialization results in less interconnect (fewer connector pins and backplane traces). The advantages and disadvantages are the same as those discussed in Section 5.1.1.

5.1.3 Data distribution with point-to-point links

A distribution amplifier can also be used to buffer the signal into multiple copies which then drive independent interconnects to their loads. This offers optimized signal quality, the capability to drive long leads (long stub) to the loads, at the expense of interconnect density.

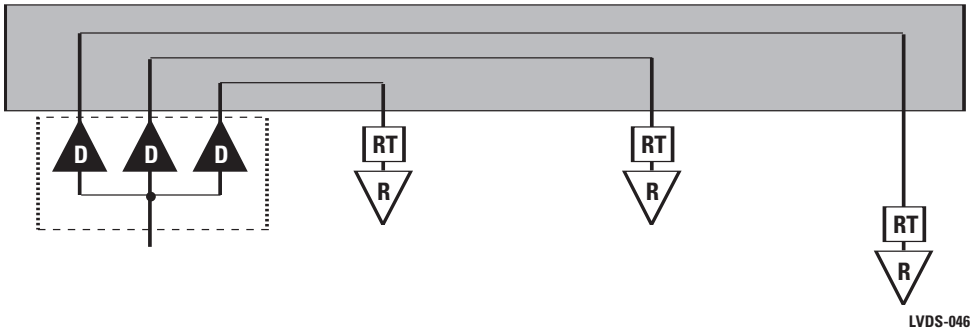


Figure 5.3. Data distribution application

5.1.4 Multipoint

The multipoint bus requires the least amount of interconnect (routing channels and connector pins), while providing bi-directional, half-duplex communication.

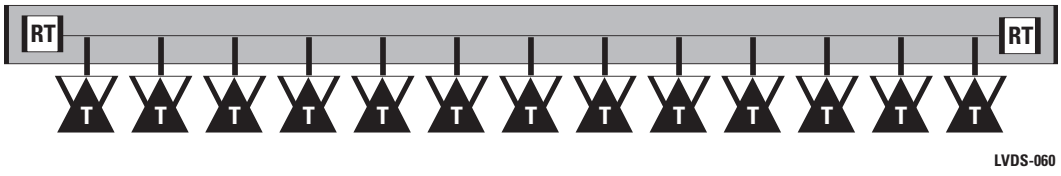


Figure 5.4. Multipoint application

However, on this type of bus, there can only be one transaction at a time. Thus, a priority and arbitration scheme are typically required. These may be protocol or hardware solutions, depending upon the application.

5.1.5 Switch matrix

Switch busses are growing in popularity for systems that require the very highest throughput possible. It is possible to have simultaneous transactions occurring on the switch bus at the same time and it has the cleanest electrical signal path of all the bus options (multidrop and multipoint, due to the no-stub effect).

The disadvantage of this type of scheme is that interconnect density increases with the number of loads, and also the complexity of the central switching card.

The switch application, due to its inherent optimized signal quality, is commonly used for links running hundreds of megabits per second into the gigabit per second range. The top speed tends to be limited by the bandwidth of the interconnect.

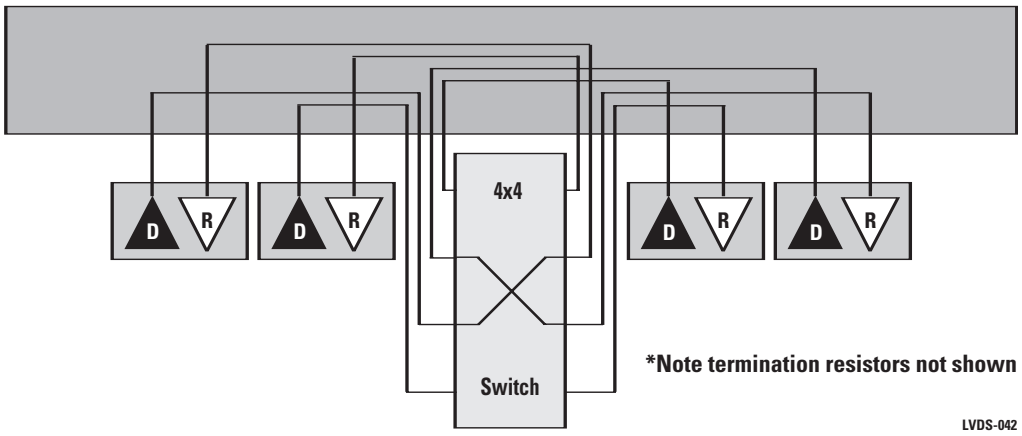


Figure 5.5. Switch application

5.2 Bus LVDS

5.2.1 System benefits of Bus LVDS

There are numerous system benefits to using Bus LVDS over other technologies that have historically been used for bus interconnect. Many of these advantages are discussed next, but can be summed up again with "Gigabits @ milliwatts!".

5.2.2 High-speed capability

Bus LVDS is capable of driving a multidrop or multipoint bus at high-speeds – for example:

- at 155 Mbps across a 20 slot multipoint FR4 backplane
- at 400 Mbps across a 10 slot multidrop FR4 backplane
- at 66 MHz with ultra-low skew clock buffers
- at 800 Mbps for point-to-point links

Previously, this has only really been achievable with the more costly high-speed ECL products. These present a translation challenge between common TTL devices and ECL drivers, and also power supply/termination problems. Other single-ended technologies were limited to sub 100 MHz applications and presented tough termination and power dissipation problems. For a detailed comparison of backplane technologies, please refer to National Application Note 1123 – Sorting out Backplane Driver Alphabet Soup.

5.2.3 Low power

Bus LVDS switches an interconnect with only 10 mA of loop current. This is much less than other high performance bus technologies that use large amounts of current (as much as 80 mA in the case of BTL and 40+ mA for GTL) to switch a bus with an incident wave. Typically, the load power for Bus LVDS is only 2.5 mW. The current-mode drivers tend to offer low power dissipation, even at high data signaling rates. Lastly, with the low swings required, the supply rails may be less than 5V, 3.3V, or even 2.5V. These three reasons make LVDS and Bus LVDS components extremely low power.

5.2.4 Low swing/low noise/low EMI

Bus LVDS uses a low swing differential signal. This small balanced signal transition generates small EMI, and the current-mode driver limits spiking into the supply rails. These reasons make the Bus LVDS driver capable of running at better than 10x the frequency of TTL at lower EMI levels.

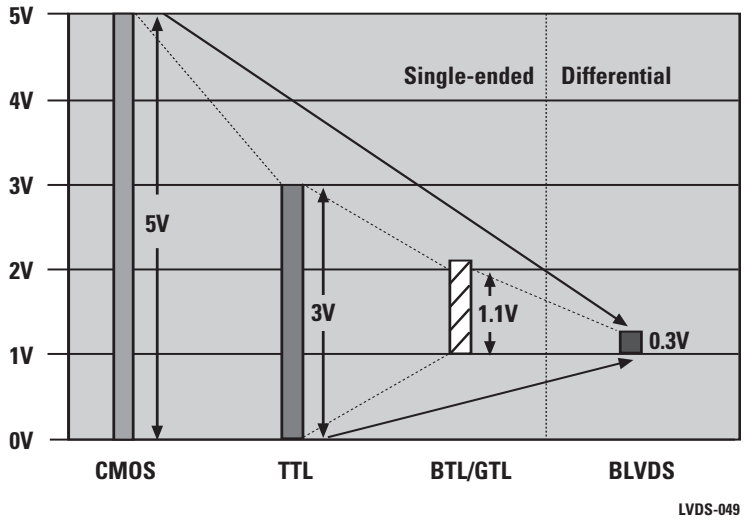


Figure 5.6. Comparison of voltage swings for various backplane technologies

CMOS and TTL technologies use a large swing and often large currents in order to switch a bus. This switching can cause ringing and undershoot which can be a large contributor to system EMI.

BTL addressed this noise issue by reducing its output swing to just 1V. However, it still uses large amounts of current to switch the bus with an incident wave (80 mA typical) and still uses the single-ended approach with limited noise margins and a complex termination scheme.

As we have seen, Bus LVDS uses only 10 mA to switch the bus with an incident wave, is low swing (300 mV typical) and is differential. We saw in Section 3.3 how differential signaling can help substantially reduce system EMI. The small swing also provides the high-speed capability while consuming minimal power.

5.2.5 Low system cost

All of National's Bus LVDS products are implemented in a core CMOS technology, which allows for low manufacturing cost and the ability to integrate more functionality onto one piece of silicon. By putting the coding, clock recovery, and other PHY/LINK layer digital functions into the interface device, ASIC complexity and risk is greatly reduced. Immense system savings can be obtained through the use of the serializer and deserializer chipsets. Connectors, cable size, and cost may be reduced. In most cases, these savings more than compensate for the interface silicon cost!

5.2.6 System benefits

Besides the cost effectiveness of using Bus LVDS, there are also other system savings in using Bus LVDS:

- Low power
  - Its CMOS design helps reduce the cost of system power supplies and cooling, enabling fan-free applications!
- Simple passive terminations
  - A bus can be implemented using only discrete components for termination. Other high-speed bus technologies such at GTL, BTL and ECL require active termination devices and/or oddball supply rails, (+1.5V, +2.1V for example) which add to system cost and power distribution complexity.
- Serialization
  - National's Bus LVDS portfolio consists of bus-able serializers and deserializers which reduce system interconnect and connector size.
- Low noise
  - The low noise characteristic of Bus LVDS help with the limitation of EMI within a system which can help with system cycle times and system cost reductions.

5.3 Backplane design considerations

Prior to the start of any system design, the following methodology should be used.

1. System design starts with a solid power and ground distribution system. When this is left to the last step, it tends to be the source of noise and EMI problems.
2. Next, consider the transmission line configuration and layout. Optimize paths to provide the best signal quality. Locating certain devices close to the connector location and other devices (potential noise sources) far away is one way to do this. Give priority to the layout of the transmission line traces to avoid unnecessary via and imbalances.
3. Complete the remaining digital design.
4. Always review the completed layout.

5.3.1 Loading effects

Figure 5.7 shows a differential bus with one card plugged in. The card adds a load to the bus, which is mainly composed of a bulk capacitance load resulting from the connector (2 pF to 3 pF), the PCB trace (2 pF to 3 pF), and the device (4 pF to 5 pF), for a total load of about 10 pF. Limit the number of vias on the card's stub to minimize capacitance loading. Also keep stub lengths as short as possible. These two tips will help maintain a high "loaded" bus impedance that will increase noise margins.

The flexibility of programmable devices comes at the cost of capacitance. National's Bus LVDS products have an I/O capacitance of 5 pF. The I/O capacitance of a programmable device is approximately double, or 10 pF. This increase in capacitance will lower the loaded bus impedance, thereby reducing the available noise margin and lowering the maximum frequency of operation in the design.

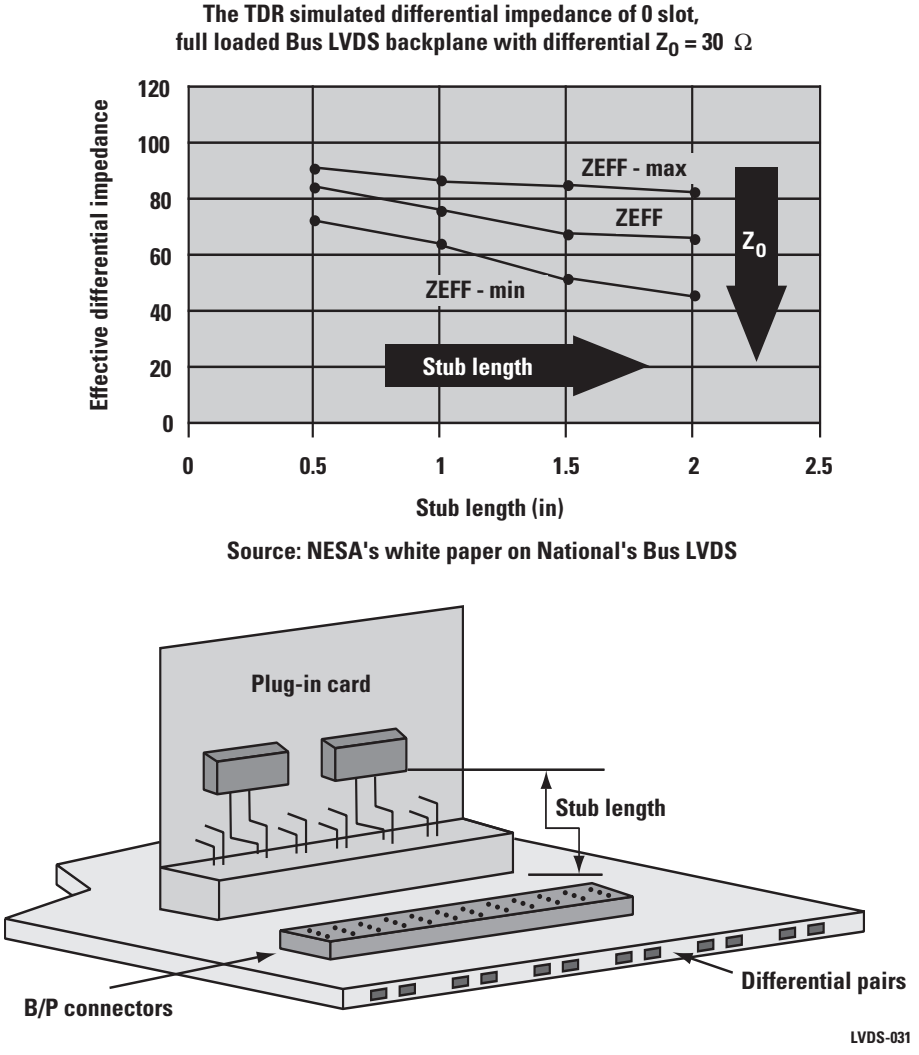


Figure 5.7. Diagram of backplane demonstrating stub length

Bus LVDS is capable of operating in wild card configurations! Depending upon system noise margin goals, full card loading is NOT required. Termination selection is a bit tricky, but should be matched to a fully loaded case (or slightly higher). Signal integrity is good even for half loaded or section loaded busses! Single-ended technologies cannot support this feature due to noise margin violations.

Figure 5.8 provides a TDR simulation of backplane impedance vs. loading.

- Case A shows the raw traces only (no via)
- Case B inserts the backplane connectors
- Case C adds all the cards into the bus, note that the cards do not include the device
- Case D adds the device to the card, thus it is a fully loaded system

Notice that about 50% of the loading is due only to the backplane connectors and their vias. Also notice how the velocity of the signal is slowed by the loading. The final loaded impedance of the bus requires two 56Ω termination resistors placed at each end of the bus.

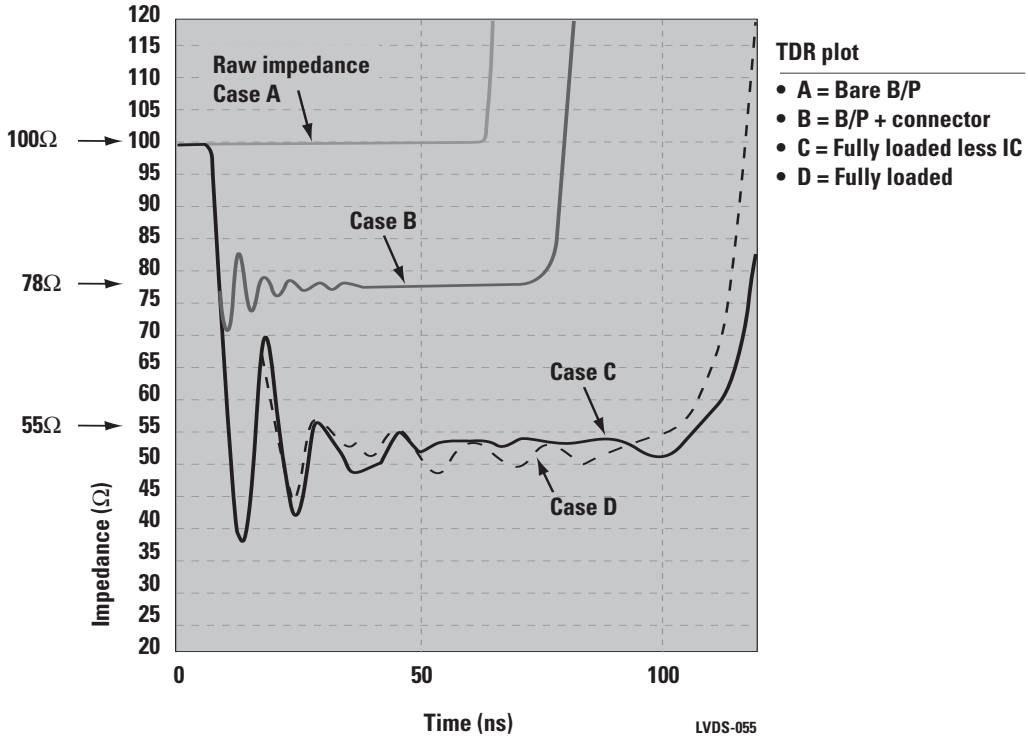


Figure 5.8. TDR plots

5.3.2 Bus termination

Termination is required for two reasons:

1. Current-mode drivers require the resistor to complete the current loop.
2. Bus LVDS edge rates are fast and the interconnect will act as a transmission line; therefore terminations are needed to limit reflections.

Bus LVDS only requires a simple termination of a single surface mount resistor across the line at each end of the bus for multipoint applications. There is no need for a special VT rail or active termination devices, as with single-ended technologies (TTL/BTL/GTL). The resistor should be equal to or slightly greater than the loaded differential impedance of the line. Typically, it is located at both ends of the backplane depending upon the configuration/application. (See also Section 4.6 on Failsafe Biasing).

5.3.3 Stub length

A long stub adds to the capacitive load, lowers the loaded impedance even more and tends to impact signal quality. For this reason, stub interconnect should be a microstrip and the number of vias (0 to 1 is best) should be limited. Figure 5.9 is from the NESA (North East System Associates, Inc.) white paper on Bus LVDS* (available from LVDS.national.com) and illustrates how increasing stub length lowers the loaded impedance. That same paper studies the relationship between maximum stub-length and data-rate. There is a strong correlation between the edge rate of a signal, and the maximum stub length that can be supported. LVDS drivers generate rising and falling edges in the region of 0.2 ns to 0.5 ns. Figure 5.9 is a TDR trace, where the launched signal has an edge rate of 0.3 ns and is therefore a good simulation of a real LVDS signal. The paper concludes that stub lengths should typically be 1 in. to 1.5 in. or less. As frequency increases, edge rates also typically increase.

There is one golden rule for stubs: **The shorter the better!**

**Signal Integrity and Validation of National's Bus LVDS (BLVDS) Technology in Heavily Loaded Backplanes*. Dr. Jinhua Chen et al. North East Systems Associates, Inc.

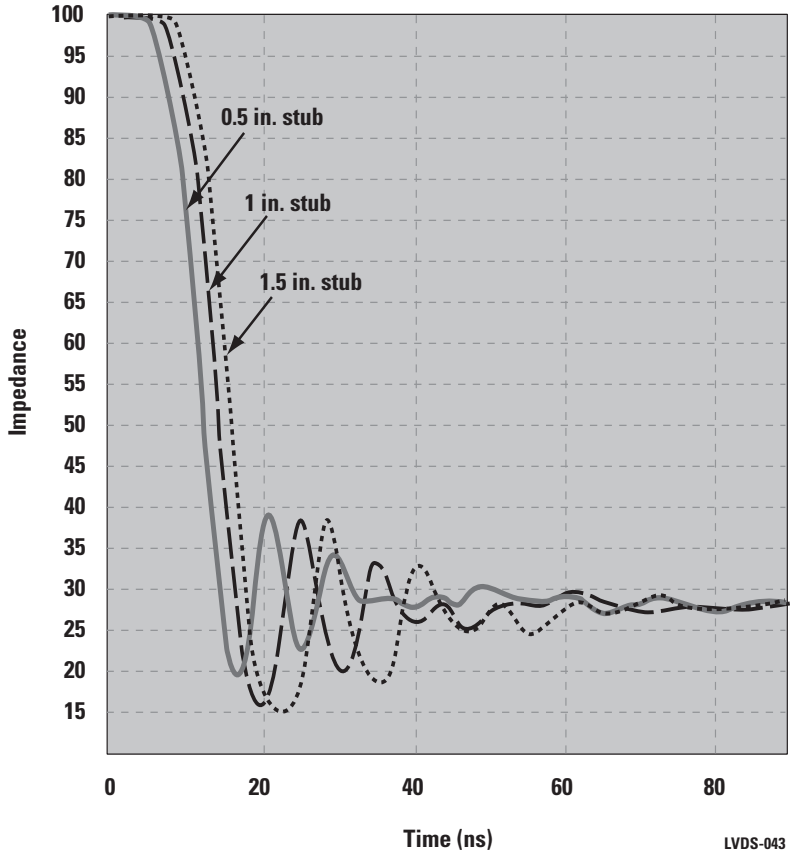


Figure 5.9. TDR plot with 300 ps input signal vs. 0.5 in., 1.0 in., and 1.5 in. stub

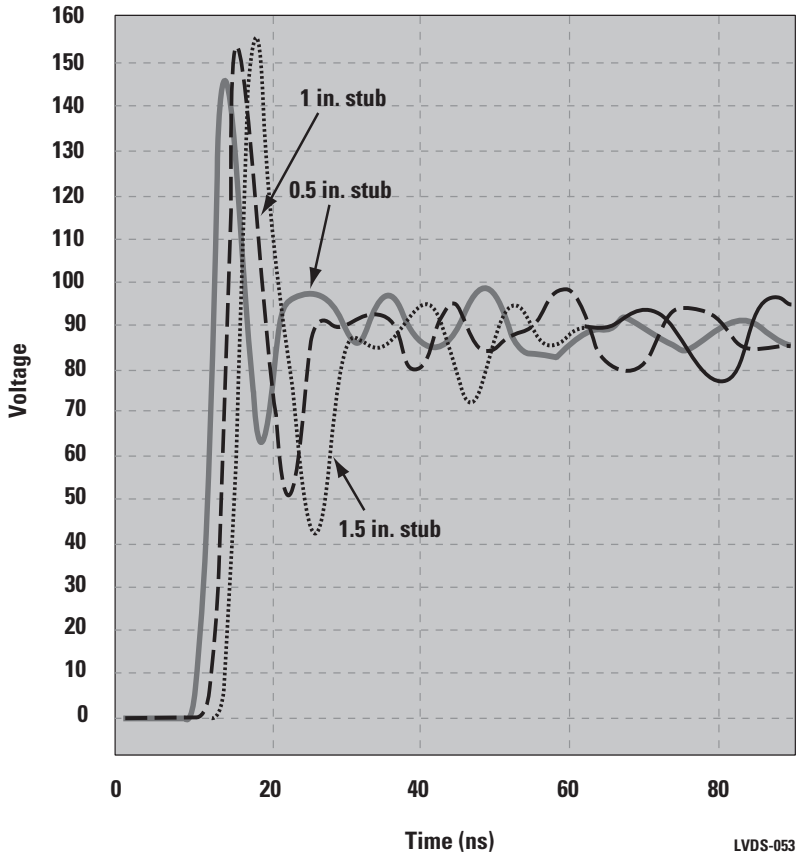


Figure 5.10. 300 ps input signal vs. 0.5", 1.0" and 1.5" stub

5.3.4 Connectors

Connectors are a complex topic and are the subject of many heated debates at standard committee meetings. There are two basic types: standard matrix based connectors (3 rows of 32 pins) and special connectors. The special connectors may be optimized for differential signals or may use elaborate techniques to clamp to the PCB. The elaborate connectors tend to avoid via structures and thus offer the highest bandwidth. However, they are also very application specific and tend to be rather expensive.

More common is the use of standard connectors for a mix of differential, power, ground and single-ended connections (see Figure 5.11). The graphic shows a variety of pinout recommendations for single-ended and differential options.

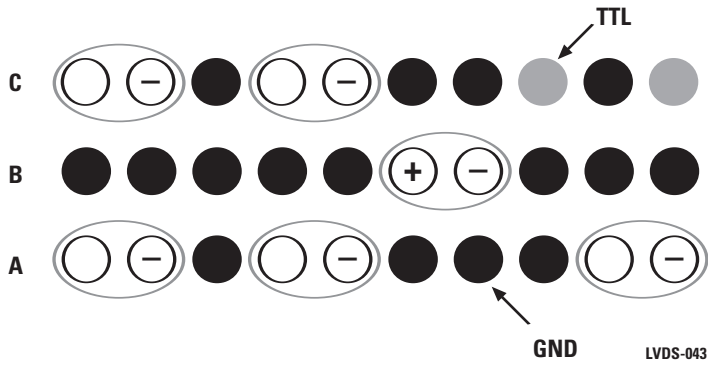


Figure 5.11. Typical connector pinouts

For differential lines in a matrix (single-ended) connector, adjacent pins in a row tend to be better as electrical lengths are the same. In addition, the row with the shorter path provides a better path over a longer row.

Ground signal assignment can be used to isolate large swing (TTL) signals from the small-swing lines (LVDS) as shown in Figure 5.11.

Connector example: Teradyne VHDM high-speed differential connector

This is a differentially optimized high-density connector for applications into the Gigabit per second range. It is offered in both 8-row (which provides 3 differential pairs) and 5-row (which provides 2 differential pairs) configurations. The 8-row connector can coexist with the basic 8-row VHDM single-ended connector and also power/ground contacts. Shielding is provided between wafers providing excellent isolation of signal contacts. The backplane layout is also improved over earlier generations and the new footprint now supports wider traces (10 mils) to be routed through the pin field easing backplane design. The backplane side of the connector accepts either the single-ended or differential versions of VHDM. Skew has been minimized within the pair and pairs are also routed together (see next drawing). This is an example of a high-throughput differential optimized connector that provides excellent signal quality. For details, please visit the Teradyne website at: www.teradyne.com/prods/bps/vhdm/hsd.html.

Check our LVDS website (LVDS.national.com) for the results of this testing. The white paper containing the test details was presented at DesignCon 2001 and titled, “Gigabit Backplane Design, Simulation, and Measurement - the unabridged story.”

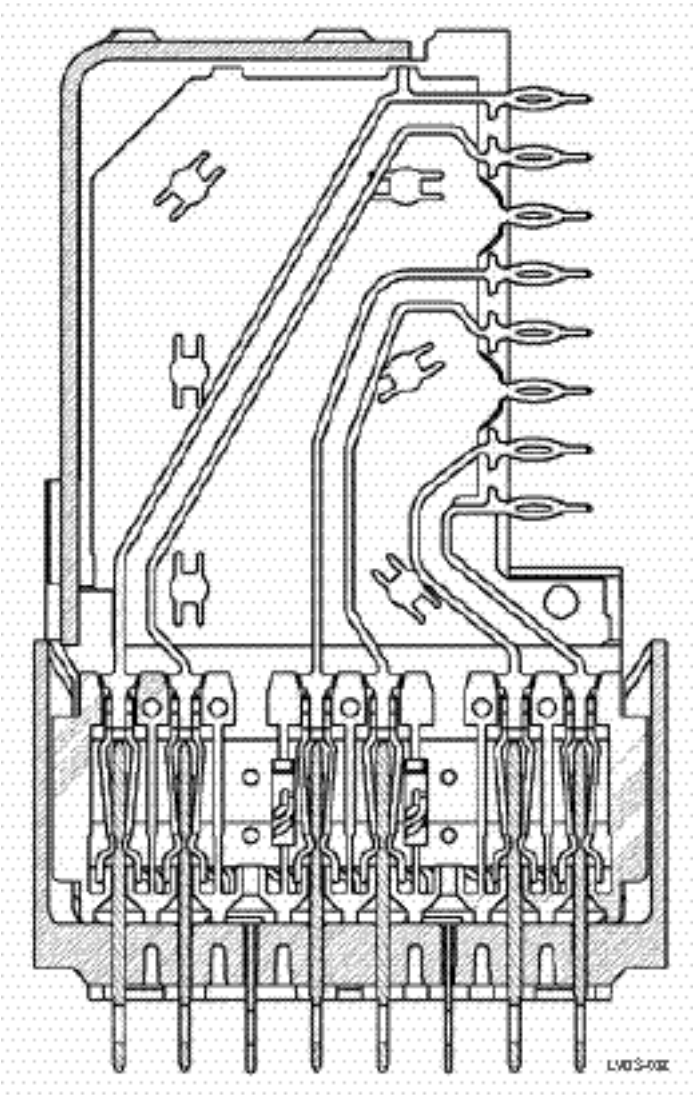


Figure 5.12. Cross section of VHDM HSD (graphic courtesy of Teradyne)

5.3.5 Failsafe biasing

Failsafe biasing may be required if a known state is required on the bus when any of the following conditions occur:

- All drivers are in TRI-STATE – common in multipoint applications
- All drivers are removed or powered-off

If this is the case, additional biasing (beyond the internal failsafe biasing of the receivers) may be provided with a failsafe biasing (power) termination as shown in Figure 5.13.

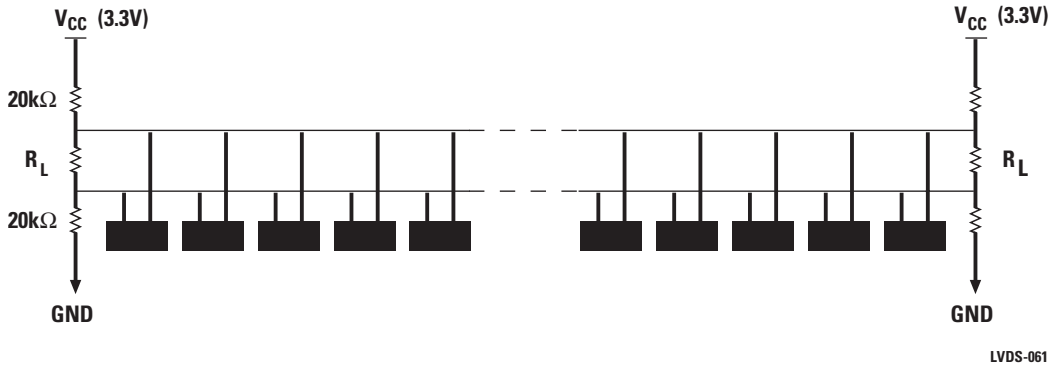


Figure 5.13. Multipoint bus with failsafe bias

In selecting failsafe resistor values note the following:

- The magnitude of the resistors should be one to two orders higher than the termination resistor, to prevent excessive loading to the driver and waveform distortion
- The mid-point of the failsafe bias should be close to the offset voltage of the driver (+1.25V) to prevent a large common-mode shift from occurring between active and TRI-STATE (passive) bus conditions
- The pull-up and pull-down resistors should be used at both ends of the bus for the quickest response
- Note that signal quality is reduced as compared to active driving (on/on)
- See Section 4.6 for equations for selecting failsafe biasing resistors

5.3.6 Hot plugging/live insertion

Live insertion, or hot swapping, is of particular importance to the telecommunications marketplace. In these applications, it is critical that maintenance, upgrading and repair can be performed without shutting down the entire system or causing disruption to the traffic on the backplane. Bus LVDS's wide common-mode range of ±1V plays a key role in supporting this function. Upon insertion of a card into a live backplane, the occurrence of abnormalities on the signals are common on both signals, thus data is not impacted. This allows for safe hot swapping of cards, making the systems robust and reliable.

Lab testing done in National's LVDS interface lab has shown zero-bit errors while plugging in or removing cards from an active bus (BERT). During the test, up to four cards were inserted at once without an error! This is due to the fact that the differential lines equally load the active line on contact and any glitch seen is a common-mode modulation that is ignored by the receivers.

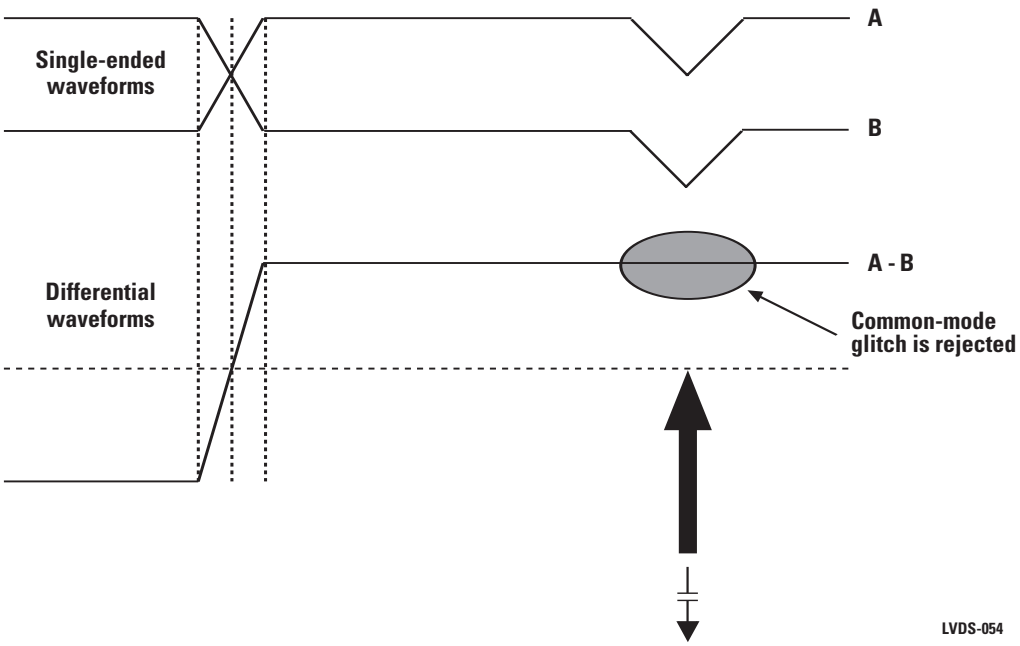


Figure 5.14. Live insertion waveforms

However, standard power sequencing is still recommended to ensure proper biasing of the devices (substrate). For insertion, the following sequence should be guaranteed by hardware design:

1. Ground
2. Power
3. I/O pins

For removal, the reverse order is recommended (3-2-1). This sequence can be supported a number of ways. Staggered power pin connectors may be employed (available from multiple sources and even compatible with many matrix connector styles). Multiple connectors are also commonly used. A DIN connector for the I/O, and "Jack" like connectors for power and ground is one approach. Yet another option uses card edge contact on the rails to establish a GND bias when the card is first inserted into the card rail.

5.4 Additional information

Detailed backplane design information is available from National's website in the form of white papers and application notes. National has also teamed up with NESA and jointly published a number of white papers and conference papers. Recent papers are available from both websites:

- LVDS.national.com
- http://www.nesa.com

Chapter 6
Cable, connectors, and performance testing

6.1 General comments

When choosing cables and connectors for LVDS it is important to remember:

1. Use controlled impedance media. The cables and connectors you use should have a differential impedance of about 100Ω. They should not introduce major impedance discontinuities that cause signal reflections.

2. Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable, multi-conductor) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential-mode) noise, which is rejected by the receiver.

3. For cable distances <0.5m, most cables can be made to work effectively. For distances 0.5m < d < 10m, CAT3 twisted pair cable works well and is readily available and relatively inexpensive. Other types of cables may also be used as required by a specific application. This includes twin-ax cables built from separate pairs and ribbon style constructions, which are then coiled.

6.2 Cabling suggestions

As described above, try to use balanced cables (twisted pair, twin-ax, or flex circuit with closely coupled differential traces). The creators of LVDS intended it to be used over a wide variety of media. The exact media is not specified in the LVDS Standard. The intention was to leave that aspect to the referencing standard that specifies the complete interface. This includes the media, data rate, length, connector, function, and pin assignments. In some applications that are very short (<0.3m), ribbon cable or flex circuit may be acceptable. In box-to-box applications, a twisted pair or twin-ax cable would be a better option due to robustness, shielding and balance. Whatever cable you do choose, following the suggestions below will help you achieve optimal results.

6.2.1 Twisted pair

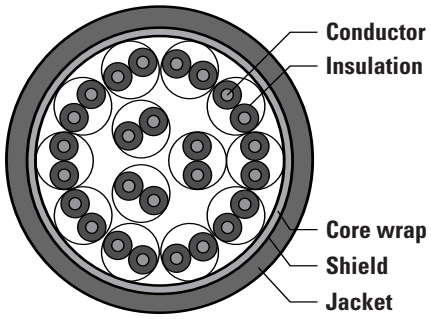


Figure 6.1. Drawing of twisted pair cable – cross-section

Twisted pair cables provide a good, low-cost solution with good balance, are flexible, and capable of medium to long runs depending upon the application skew budget. A variety of shielding options are available. Twisted pair cables are offered unshielded, with an overall shield or with shields around each pair in conjunction with overall shield. Installing connectors on twisted pair cables is difficult.

1. Twisted pair is a good choice for LVDS. CAT3 cable is good for runs up to about 10m, while CAT5 has been used for longer runs.
2. For the lowest skew, group skew-dependent pairs together (in the same ring to minimize skew between pairs).
3. Ground and/or terminate unused conductors (do not float).

6.2.2 Twin-ax cables

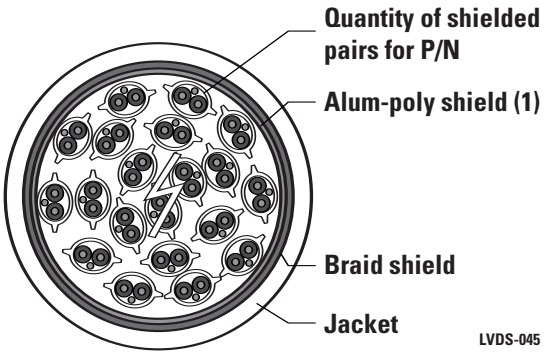


Figure 6.2. Drawing of individually shielded parallel pair twin-ax cable – cross section

Twin-ax cables are flexible, have low skew and shields around each pair for isolation. Since they are not twisted, they tend to have very low skew within a pair and between pairs. These cables are for long runs and have been commonly deployed in Channel Link and FPD-Link applications.

1. Drain wires per pair may be connected together in the connector header to reduce pin count.
2. Ground and/or terminate unused conductors.

6.2.3 Flex circuit

Flex circuit is a good choice for very short runs, but it is difficult to shield. It can be used as an interconnect between boards within a system.

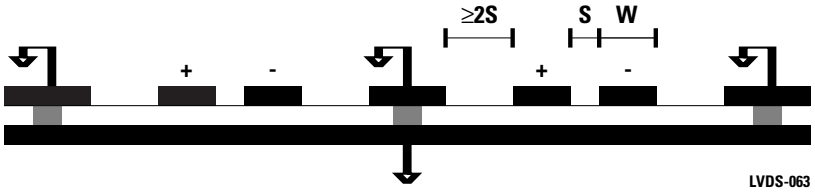
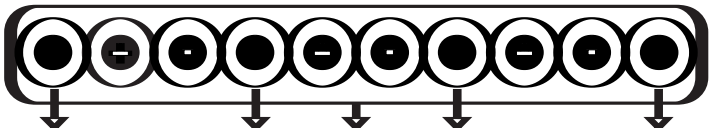


Figure 6.3. Flex circuit – cross-section

1. Closely couple the members of differential pairs (S < W). Do not run signal pairs near the edges of the cable, as these are not balanced.
2. Use a ground plane to establish the impedance.
3. Use ground shield traces between the pairs if there is room. Connect these ground traces to the ground plane through vias at frequent intervals.

6.2.4 Ribbon cable

Ribbon cable is cheap and is easy to use and shield. Ribbon cable is not well suited for high-speed differential signaling (good coupling is difficult to achieve), but it is OK for very short runs.



LVDS-051

Figure 6.4. Flat cable – cross-section

1. If ribbon cable must be used, separate the pairs with ground wires. Do not run signal pairs at the edges of the ribbon cable.
2. Use shielded cable if possible. Shielded flat cable is available.

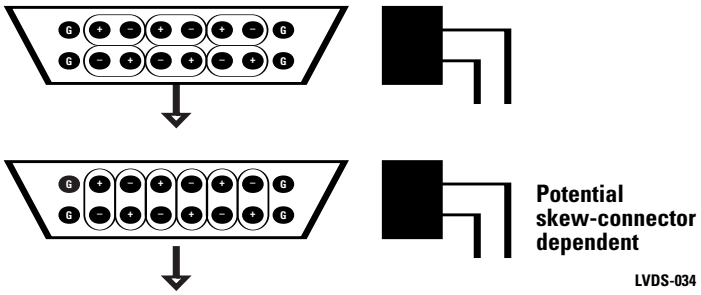
6.2.5 Additional cable information

Additional information on cable construction may be found in National Application Note AN-916. Also, many cable, connector and interconnect system companies provide detailed information on their respective websites about different cable options. A non-inclusive list of a few different options is provided below:

- 3M www.3M.com/interconnects/
- Spectra-strip cable products www.spectra-strip.amphenol.com/default.CFM
- AMP http://connect.amp.com/

6.2.6 Connectors

Connectors are also application dependent and depend upon the cable system being used, the number of pins, the need for shielding and other mechanical footprint concerns. Standard connectors have been used at low to medium data rates, and optimized low skew connectors have been developed for medium- to high-speed applications.



LVDS-034

Figure 6.5. Typical connector pinouts

1. Choose low-skew, impedance-matching connectors if possible.
2. Group members of each pair together. Pins of a pair should be close together (adjacent) not separated from each other. This is done to maintain balance, and to help ensure that external noise, if picked up, will be common-mode and not differential in nature.

3. Some connectors have different length leads for different pins. Group pairs on same length leads. Consult the connector manufacturer for the orientation of pins that yield the lowest skew and crosstalk for your particular connector. Shorter pin lengths tend to be better than long ones, minimize this distance if possible.
4. Place ground pins between pairs where possible and convenient. Especially use ground pins to separate TTL/CMOS signals from LVDS signals.
5. Ground end pins. Do not use end pins for high-speed signals, if possible, as they offer less balance.
6. Ground and/or terminate unused pins.

Many different connector options exist. One such cable-connector system that has been used for LVDS with great results is the 3M "High-speed MDR Digital Data Transmission System." This cable system is featured on the National channel-link (48-bit) and LDI evaluation kits. The connector is offered in a surface mount option that has very small skew between all the pins. Different cable types are also supported.

6.3 Cable ground and shield connections

In many systems, cable shielding is required for EMC compliance. Although LVDS provides benefits of low EMI when used properly, shielding is still usually a good idea especially for box-to-box applications. Together, cable shielding and ground return wires help reduce EMI. The shielding contains the EMI and the ground return wire (the pair shield or drain wire in some cables) and provides a small loop area return path for common-mode currents. Typically one or more pairs are assigned to ground (circuit common). Using one or more pair reduces the DC resistance (DCR) of the path by the parallel connection of the conductors. This provides a known, very low impedance return path for common-mode currents.

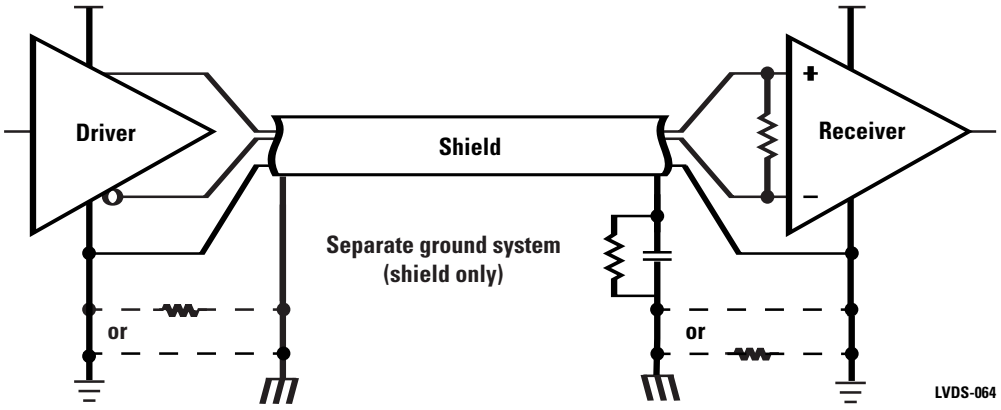


Figure 6.6. Typical grounding scheme

In most applications, the grounding system will be common to both the receiver and the driver. The cable shield is connected at one end with a DC connection to the common ground (frame ground). Avoid "pig-tail" (high-inductance) ground wiring from the cable. The other end of the shield is typically connected with a capacitor or network of a capacitor and a resistor as shown in the Figure 6.6. This prevents DC current flow in the shield. In the case where connectors are involved that penetrate the system's enclosure, the cable shield must have a circumferential contact to the connector's conductive backshell to provide an effective shield and must make good contact.

Note: It is beyond the scope of this book to effectively deal with cabling and grounding systems in detail. Please consult other texts on this subject and be sure to follow applicable safety and legal requirements for cabling, shielding, and grounding.

Chapter 7
Performance testing

7.1 LVDS signal quality

Signal quality may be measured by a variety of means. Common methods are:

- Measuring rise time at the load
- Measuring jitter in an eye pattern
- Bit error rate testing
- Other means

Eye patterns and Bit Error Rate Testing (BERT) are commonly used to determine signal quality. These two methods are described next.

7.1.1 LVDS signal quality: jitter measurements using eye patterns

This report provides an example of a data rate vs. cable length curve for LVDS drivers and receivers in a typical application for a particular twisted pair cable. The questions of: "How far?" and "How fast?" seem simple to answer at first, but after detailed study, the answers become quite complex.

This is not a simple device parameter specification. But rather, a system level question where a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and also the pulse coding that will be used (NRZ for example). Additionally, other system level components should be known too. This includes details about cables, connectors, and the PCB.

Since the purpose is to measure signal quality, it should be done in a test fixture that closely matches the end environment – or even better – in the actual application. Eye pattern measurements are useful in measuring the amount of jitter vs. the unit interval to establish the data rate vs. cable length curves and therefore are a very accurate way to measure the expected signal quality in the end application.

7.1.2 Why eye patterns?

The eye pattern is used to measure the effects of inter-symbol interference on random data being transmitted through a particular medium. The prior data bits effect the transition time of the signal. This is especially true for NRZ data that does not guarantee transitions on the line. For example, in NRZ coding, a transition high after a long series of lows has a slower rise time than the rise time of a periodic (010101) waveform. This is due to the low pass filter effects of the cable.

Figure 7.1 illustrates the superposition of six different data patterns. Overlaid, they form the eye pattern that is the input to the cable. The right hand side of this figure illustrates the same pattern at the end of the cable. Note the rounding of the formerly sharp transitions. The width of the crossing point is now wider and the opening of the eye is also now smaller (see Application Note AN-808 for an extensive discussion on eye patterns).

When line drivers (generators) are supplying symmetrical signals to clock leads, the period of the clock, rather than the unit interval of the clock waveform, should be used to determine the maximum cable lengths (e.g., though the clock rate is twice the data rate, the same maximum cable length limits apply). This is due to the fact that a periodic waveform is not prone to distortion from inter-symbol distortion as is a data line.

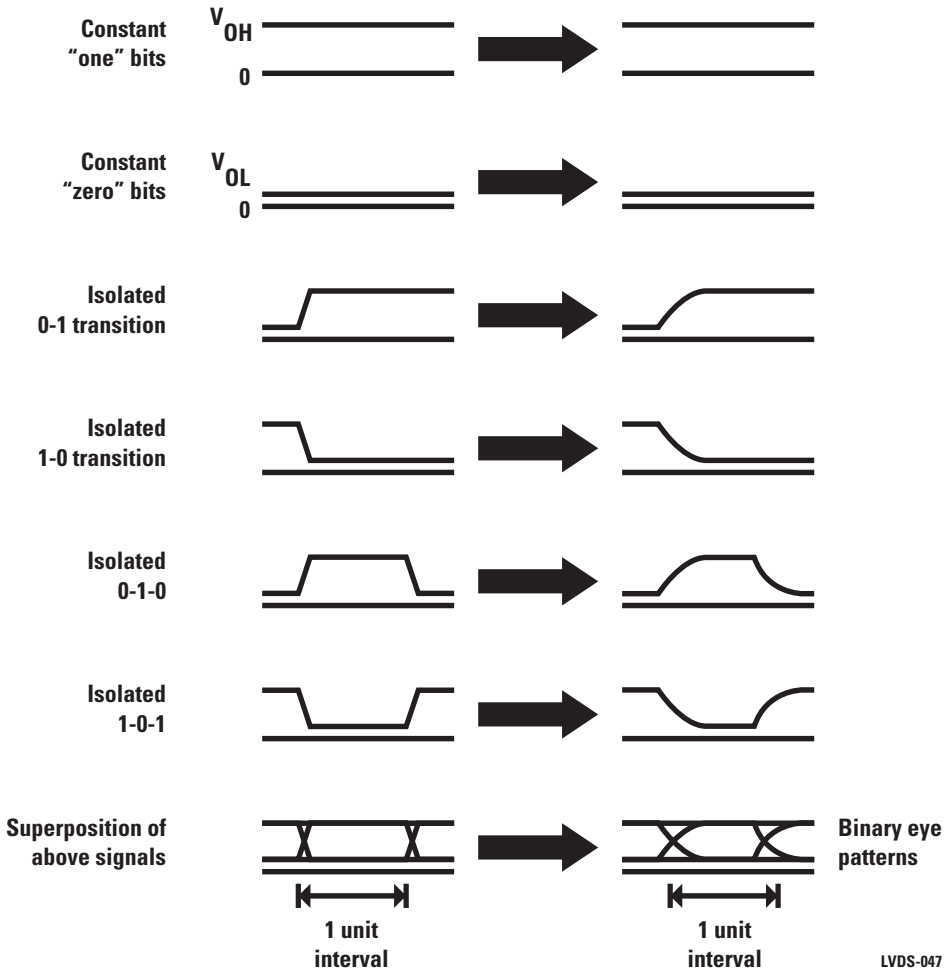


Figure 7.1. Formation of an eye pattern by superposition

Figure 7.2 describes the measurement locations for minimum jitter. Peak-to-peak jitter is the width of the signal crossing the optimal receiver thresholds. For a differential receiver, that would correspond to 0V (differential). However, the receiver is specified to switch between -100 mV and +100 mV. Therefore for a worse case jitter measurement, a box should be drawn between ±100 mV and the jitter measured between the first and last crossing at ±100 mV. If the vertical axis units in Figure 7.2 were 100 mV/div, the worse case jitter is at ±100 mV levels.

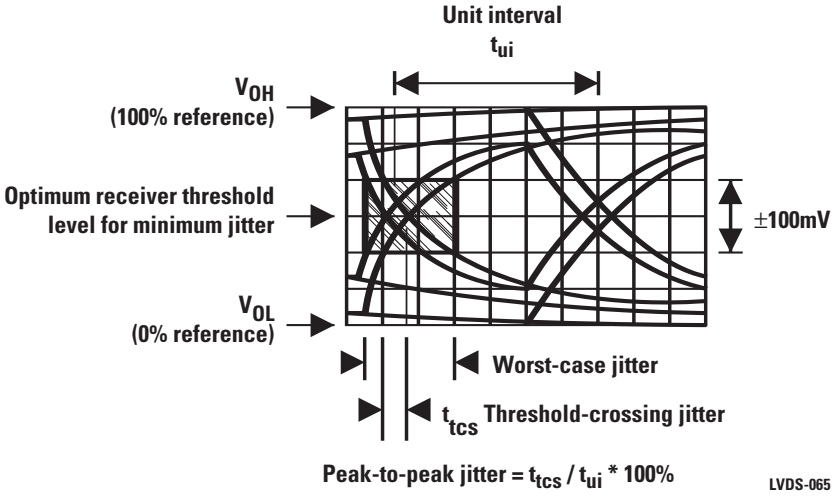


Figure 7.2. NRZ data eye pattern

7.1.3. Eye pattern test circuit

LVDS drivers and receivers are typically used in an uncomplicated point-to-point configuration as shown in Figure 7.3. It details the test circuit that was used to acquire the eye pattern measurements. It includes the following components:

PCB#1 – DS90C031 LVDS quad driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP AMPLIMITE™ .050 series connector.

Cable – The cable used for this testing was Berk-Tek part number 271211. This is a CAT3 105Ω (differential-mode) 28 AWG stranded twisted pair cable (25 pair with overall shield) commonly used on SCSI applications. This cable represents a common data interface cable. For this test report, the following cable lengths were tested: 1, 2, 3, 5, and 10m. Cables longer that 10m were not tested, but may be employed at lower data rates. Berk-Tek no longer manufactures this cable. Similar cable is available through other vendors such as Hitachi Cable Manchester. (Part # 49251)

PCB#2 – DS90C032 LVDS quad receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMPLIMITE .050 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.

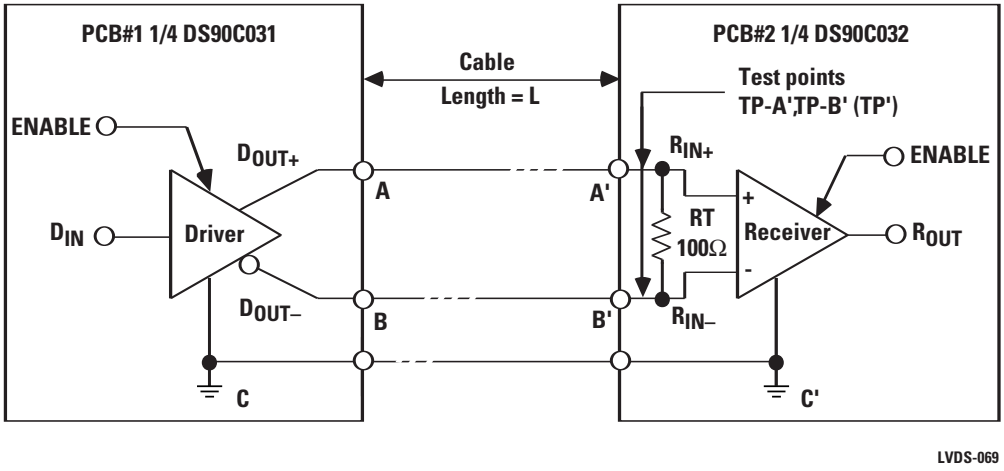


Figure 7.3. LVDS signal quality test circuit

7.1.4 Test procedure

A pseudo random bit sequence (PRBS) generator was connected to the driver input, and the resulting eye pattern (measured differentially at TP') was observed on the oscilloscope. Different cable lengths (L) were tested, and the frequency of the input signal was increased until the measured jitter equaled 20% with respect to the unit interval for the particular cable length. The coding scheme used was NRZ. Jitter was measured twice at two different voltage points. Jitter was first measured at the 0V differential voltage (optimal receiver threshold point) for minimum jitter, and second at the maximum receiver threshold points (±100 mV) to obtain the worst case or maximum jitter at the receiver thresholds. Occasionally jitter is measured at the crossing point alone and although this will result in a much lower jitter point, it ignores the fact that the receivers may not switch at that very point. For this reason, this signal quality test report measured jitter at both points.

7.1.5 Using differential probes

The use of differential probes is usually recommended when testing any differential signal, whether it be LVDS, ECL, or CML. The same effects that a differential receiver in a real system benefits from, apply to oscilloscopes and other forms of test equipment.

Differential probing leads to more accurate measurements and better noise rejection than single ended probing, but the results need to be interpreted with care. The definition and use of the term 'Differential swing' is not consistent across the industry. Many data-sheets and the LVDS specification define it as $(D_{O+}) - (D_{O-})$. This is not the same amplitude that would be measured by a differential probe. The output of such a probe will typically be $2 \times [(D_{O+}) - (D_{O-})]$.

7.1.6 Results and data points

Table 7.1. 20% jitter table @ 0V differential (minimum jitter)

Cable length (m)	Data rate (Mbps)	Unit interval (ns)	Jitter (ns)
1	400	2.500	0.490
2	391	2.555	0.520
3	370	2.703	0.524
5	295	3.390	0.680
10	180	5.550	1.160

As described above, jitter was measured at the 0V differential point. For the case with the 1m cable, 490 ps of jitter at 400 Mbps was measured, and with the 10m cable, 1.160 ns of jitter at 180 Mbps was measured.

Table 7.2. 20% Jitter table @ ±100 mV (maximum Jitter)

Cable length (m)	Data rate (Mbps)	Unit interval (ns)	Jitter (ns)
1	200	5.000	1.000
2	190	5.263	1.053
3	170	5.882	1.176
5	155.5	6.431	1.286
10	100	10.000	2.000

The second case measured jitter between ±100 mV levels. For the 1m cable, 1 ns of jitter was measured at 200 Mbps, and for the 10m cable, 2 ns of jitter occurred at 100 Mbps.

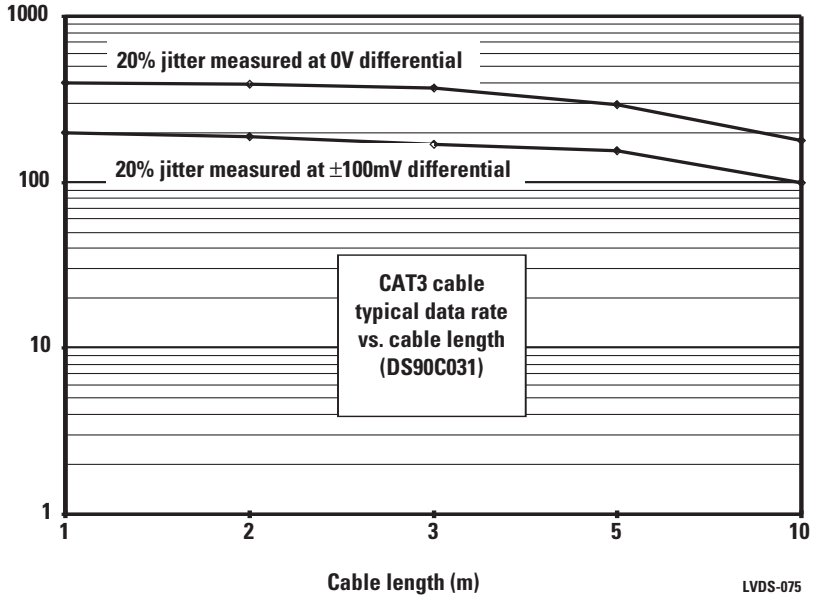


Figure 7.4. Typical data rate vs. cable length for 0m to 10m CAT3 cable

Care should be taken in long cable applications using LVDS. When directly coupled, LVDS provides up to ±1V common-mode rejection. Long cable applications may require larger common-mode support. If this is the case, transformer coupling or alternate technologies (such as RS-485) should be considered.

Figure 7.4 is a graphical representation of the relationship between data rate and cable length for the application under test. Both curves assume a maximum allotment of 20% jitter with respect to the unit interval. Basically, data rates between 200 Mbps to 400 Mbps are possible at shorter lengths, and rates of 100 Mbps to 200 Mbps are possible at 10m. Note that employing a different coding scheme, cable, or wire gauge (AWG) will create a different relationship between maximum data rate vs. cable length. Designers are greatly encouraged to experiment on their own.

7.1.7 Additional data on jitter and eye patterns

For additional information on LVDS "data rate vs. cable length" please consult the list of LVDS application notes on the LVDS website at: LVDS.national.com.

At this time of this printing the following application notes were available:

Application note #	Devices tested
AN-977	DS90C031/032
AN-1088	DS90LV017/027, DS92LV010A

7.1.8 Conclusions – eye pattern testing

Eye patterns provide a useful tool to analyze jitter and the resulting signal quality as it captures the effects of a random data pattern. They provide a method to determine the maximum cable length for a given data rate or vice versa. Different systems, however, can tolerate different levels of jitter. Commonly 5%, 10%, or 20% is acceptable with 20% jitter usually being an upper practical limit. More than 20% jitter tends to close down the eye opening, making error-free recovery of NRZ data more difficult. This report illustrates data rate vs. distance for a common, inexpensive type of cable.

7.2 BERT

Bit error ratio testing is another approach to determine signal quality. This test method is described next.

7.2.1 LVDS cable driving performance using BERT

The questions of: "How far?" and "How fast?" seem simple to answer at first, but after detailed study, their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question, and to be answered correctly a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and the pulse coding that will be used (Non-Return to Zero (NRZ) for example – see Application Note AN-808 for more information about coding). Additionally, other system level components should be known too. This includes details about the cable, connector and information about the printed circuit boards (PCB). Since the purpose is to measure signal quality/performance, it should be done in a test fixture that matches the end environment precisely if possible. The actual application would be best if possible. There are numerous methods to measure signal quality, including eye pattern (jitter) measurements and BER tests.

This report provides the results of a series of BER tests performed on the DS90C031/032 LVDS quad line driver/receiver devices. The results can be generalized to other National LVDS products. Four drivers were used to drive 1m to 5m of standard twisted pair cables at selected data rates. Four receivers were used to recover the data at the load end of the cable.

7.2.2 What is a BERT?

Bit error ratio testing is one way to measure the performance of a communications system. The standard equation for a bit error rate measurement is:

BER = (number of bit errors)/(total number of bits)

Common measurement points are bit error rates of:
$1^3 \times 10^{-12}$ => one or less errors in 1 trillion bits sent
1×10^{-14} => one or less errors in 100 trillion bits sent

Note that BERT is time intensive. The time length of the test is determined by the data rate and also the desired performance benchmark. For example, if the data rate is 50 Mbps, and the benchmark is an error rate of 1×10^{-14} or better, a run time of 2,000,000 seconds is required for a serial channel. 2,000,000 seconds equates to 555.6 hours or 23.15 days!

7.2.3 BERT circuit

LVDS drivers and receivers are typically used in an uncomplicated point-to-point configuration as shown in Figure 7.2. This figure details the test circuit that was used. It includes the following components:

PCB#1 – DS90C031 LVDS quad driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMPLIMITE .050 series connector.

Cable – Cable used for this testing was Berk-Tek part number 271211. This is a CAT3 105Ω (differential-mode) 28 AWG stranded twisted pair cable (25 pair with overall shied) commonly used in SCSI applications. This cable represents a common data interface cable. For this test report, cable lengths of 1m and 5m were tested. Berk-Tek no longer manufactures this cable. Similar cable is available through other vendors such as Hitachi Cable Manchester. (Part # 49251)

PCB#2 – DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMPLIMITE .050 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.

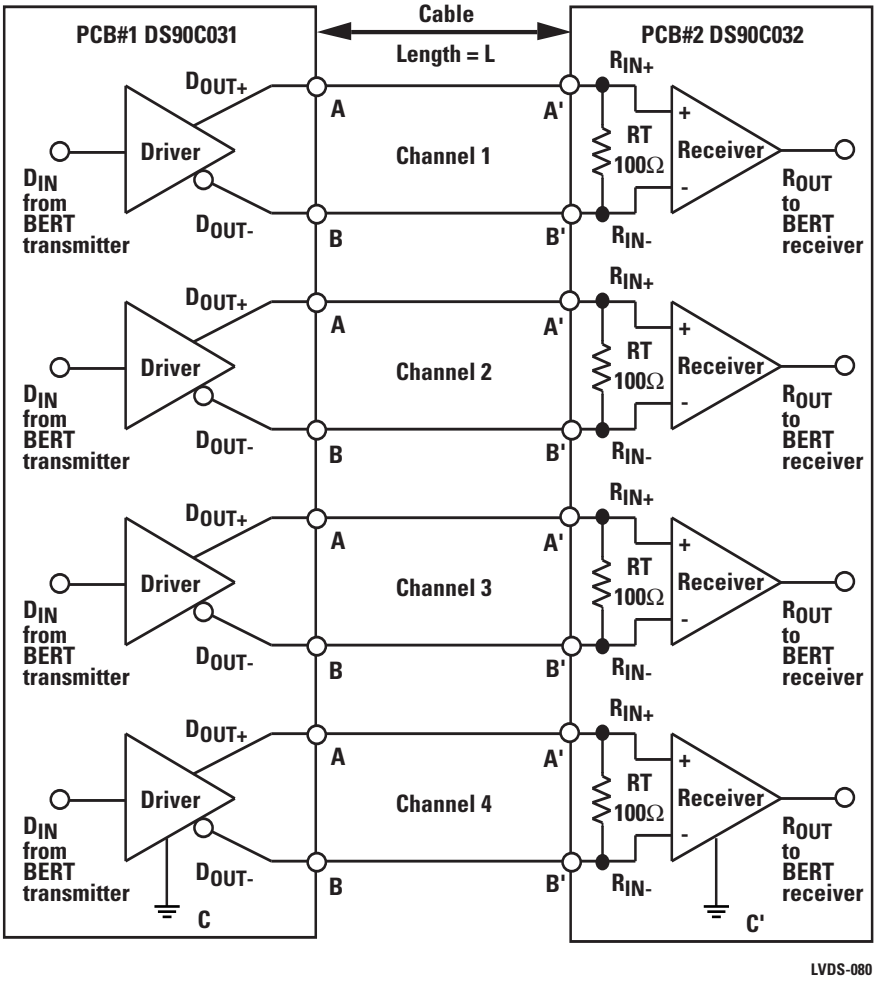


Figure 7.5. LVDS BERT circuit

7.2.4 Test procedure

A parallel high-speed bit error ratio transmitter/receiver set (Tektronix MultiBERT-100) was employed for the tests. The transmitter was connected to the driver inputs, and the receiver outputs were connected to the BERT receiver inputs. Different cable lengths and data rates were tested. The tester was configured to provide a PRBS of 2^{15}- 1 (32,767 bit long sequence). In the first test, the same input signal was applied to all four of the LVDS channels under test. For the other tests, the PRBS was offset by 4 bits, thus providing a random sequence between channels. The coding scheme used was NRZ. Upon system test configuration, the test was allowed to run uninterrupted for a set amount of time. At completion of the time block, the results were recorded which included: elapsed seconds, total bits transmitted and number of bit errors recorded. For the three tests documented next, a power supply voltage of +5.0V was used and the tests were conducted at room temperature.

7.2.5 Tests and results

The goal of the tests was to demonstrate errors ratios of less than 1×10^{-12} are obtainable.

Test 1
Conditions

- Data rate = 50 Mbps
- Cable length = 1m
- PRBS code = 2^{15}- 1 NRZ

For this test, the PRBS code applied to the four driver inputs was identical. This created a "simultaneous output switching" condition on the device.

Results

- Total seconds: 87,085 (1 day)
- Total bits: $1{,}723 \times 10^{13}$
- Errors = 0
- Error ratio = $< 1 \times 10^{-12}$

Test 2
Conditions

- Data rate = 100 Mbps
- Cable length = 1m
- PRBS code = 2^{15}- 1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

Results

- Total seconds: 10,717 (~3 hr)
- Total bits: 4.38×10^{12}
- Errors = 0
- Error ratio = $< 1 \times 10^{-12}$

Test 3
Conditions

- Data rate = 100 Mbps
- Cable length = 5m
- PRBS code = 2^{15}- 1 NRZ

For this test, the PRBS code applied to the four driver inputs was offset by four bits. This creates a random pattern between channels.

Results

- Total seconds: 10,050 (~2.8 hr)
- Total bits: 4×10^{12}
- Errors = 0
- Error ratio = $< 1 \times 10^{-12}$

7.2.6 Conclusions – BERT

All three of the tests ran error free and demonstrate extremely low bit error ratios using LVDS technology. The tests concluded that error ratios of < 1 x 10^{15}- 1 can be obtained at 100 Mbps operation across 5m of twisted pair cable.

BER tests only provide a "go/no go" data point if zero errors are detected. It is recommended to conduct further tests to determine the point of failure (data errors). This will yield important data that indicates the amount of margin in the system. This was done in tests conducted by increasing the cable length from 1m to 5m, and also adjusting the data rate from 50 Mbps to 100 Mbps.

Additionally, bench checks were made while adjusting the power supply voltage from 5.0V to 4.5V and 5.5V, adjusting clock frequency, and applying hot/cold temperatures to the device under test (DUT). No errors were detected during these checks (tests were checks only and were not conducted over time, i.e., 24 hr). BERTs conclude that the PRBS patterns were transmitted error free across the link. This was concluded by applying a pattern to the input and monitoring the receiver output signal.

Chapter 8
Evaluation kits

8.1 Evaluation/demo boards

Evaluation boards are available for a nominal charge that demonstrate the basic operation of selected LVDS devices. The evaluation boards can be ordered through National's distributors. The following table provides product family, PCB description, NSID(s) of devices on the PCB, kit order number, and errata sheet (if applicable). Manuals for evaluation boards are available online at LVDS.national.com.

LVDS family	PCB description	NSIDs on PCB	Order number
LVDS	LVDS Quad line driver/receiver eval board	DS90LV047A, DS90LV048A	LVDS47/48EVK
LVDS	LVDS 800 Mbps crosspoint evaluation board	DS90CP22M-8	LVDSCP22EVK
LVDS	LVDS - LVDS buffer evaluation board	DS90LV001	LVDS001EVK
LVDS	LVDS Quad line driver/receiver eval (unstuffed board)	DS90C031, DS90C032, or DS90LV031A, DS90LV032A	Lit# 550061-001
LVDS/STA	2 x 2 Crosspoint switch evaluation kit	SCAN90CP02	SCAN90CP02EVK
Channel link	Channel link evaluation board 133 MHz, 2.5/3.3V, 48-bit	DS90CR485, DS90CR486	CLINK3V48BT-133
Channel link	Channel link evaluation board 20 to 85 MHz, 3.3V, 28-bit	DS90CR287, DS90CR288A	CLINK3V28BT-85
Channel link	Channel link evaluation board 112 MHz, 3.3V, 48-bit	DS90CR483, DS90CR484	CLINK3V48BT-112
Bus LVDS	Bus LVDS SER/DES evaluation mini-backplane, *errata sheet available*	DS92LV1021, DS92LV1210	BLVDS01 (Limited supply)
Bus LVDS	Bus LVDS SER/DES with random lock RX evaluation mini-backplane, *errata sheet available*	DS92LV1021, DS92LV1212	BLVDS02
Bus LVDS	Bus LVDS SER/DES PRBS generator and checker board (40 MHz)	DS92LV1021, DS92LV1212A	BLVDS03
Bus LVDS	Bus LVDS SER/DES w/ random lock RX evaluation mini-backplane	DS92LV1023, DS92LV1224	BLVDS04
Bus LVDS	Bus LVDS SER/DES PRBS generator and checker board (66 MHz)	DS92LV1023, DS92LV1224	BLVDS05
Bus LVDS	Bus LVDS 16-bit SER/DES evaluation board View the schematic	DS92LV16	BLVDS16EVK
Bus LVDS	Bus LVDS 18-bit SER/DES evaluation board View the schematic View the PCB layout View the BLVDS92LV18EVK BOM	DS92LV18	BLVDS18EVK
Bus LVDS/ UTOPIA	UTOPIA-LVDS bridge evaluation board	DS92UT16	UTOPIA16EVK
Bus LVDS/ STA (JTAG)	SCAN system test access evaluation kit	SCAN921023, SCAN921224,	SCANSTAEVK

Please note that several flat panel display evaluation kits are also available that utilize LVDS technology. These evaluation kits are showcased from the Appinfo/FPD page.

Appendix

A.1 LVDS application notes, white papers

National provides an in depth application site on LVDS. This site provides the design community with the latest information on National's expanding LVDS family. Below is a list of available application notes at the time of publication. To view the application notes, or to find the latest list, please visit the LVDS.national.com

Application notes

AN-905 Transmission Line RAPIDESIGNER Operation and Applications Guide

AN-971 Introduction to LVDS

AN-977 Signal Quality – Eye Patterns

AN-1032 Introduction to FPD-Link

AN-1040 Bit Error Rate Testing

AN-1041 Introduction to Channel Link

AN-1056 STN Panel Application

AN-1059 Timing (RSKM) Information

AN-1060 LVDS - Megabits @ milliwatts (EDN Reprint)

AN-1084 Channel Link Parallel Application of Link Chips

AN-1085 PCB and Interconnect Design Guidelines

AN-1088 Signal Quality

AN-1108 PCB and Interconnect Design Guidelines

AN-1109 Multi-drop Application of Channel Links

AN-1110 Power Dissipation of LVDS Drivers and Receivers

AN-1115 Bus LVDS and DS92LV010A XCVR

AN-1123 Sorting out Backplane Driver Alphabet Soup

AN-1173 High Speed Bus LVDS Clock Distribution Using the DS92CK16 Clock Distribution Device

AN-1194 Failsafe Biasing of LVDS Interfaces

AN-1217 How to Validate Bus LVDS SerDes Signal Integrity Using an Eye Mask

AN-1238 Wide Bus Applications Using Parallel Bus LVDS SerDes Devices

White papers

Gigabit Backplane Design, Simulation and Measurement - the unabridged story
DesignCon 2001

A Baker's Dozen of High-Speed Differential Backplane Design Tips
DesignCon 2000

Bus LVDS Expands Applications for Low Voltage Differential Signaling (LVDS)
DesignCon 2000

Signal integrity and validation of Bus LVDS (BLVDS) technology in heavily loaded backplanes
DesignCon 1999

National Edge articles

The Many Flavors of LVDS

Eye Opening Enhancements Extend the Reach of High-Speed Interfaces

A.2 Glossary

AN	Application Note
ANSI	American National Standards Institute
ASIC	Application Specific Integrated Circuit
B/P	Backplane
BER	Bit Error Rate
BERT	Bit Error Rate Test
BLVDS	Bus LVDS
BTL	Backplane Transceiver Logic
CAT3	CAT3 (Cable classification)
CAT5	CAT5 (Cable classification)
CISPR	International Special Committee on Radio Interference (Comité International Spécial des Perturbations Radioélectriques)
D	Driver
DCR	DC Resistance
DUT	Device Under Test
ECL	Emitter Coupled Logic
EIA	Electronic Industries Association
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EN	Enable
ESD	Electrostatic Discharge
EVK	Evaluation Kit
FCC	Federal Communications Commission
FPD	Flat Panel Display
FPD-LINK	Flat Panel Display Link
Gbps	Gigabits per second
GTL	Gunning Transceiver Logic

Appendix

HBM	Human Body Model
Hi-Z	High Impedance
IC	Integrated Circuit
I/O	Input/Output
IBIS	I/O Buffer Information Specification
IDC	Insulation Displacement Connector
IEEE	Institute of Electrical and Electronics Engineers
kbps	kilobits per second
LAN	Local Area Network
LDI	LVDS Display Interface
LVDS	Low Voltage Differential Signaling
Mbps	Mega bits per second
MDR	Mini Delta Ribbon
MLC	Multi Layer Ceramic
NRZ	Non Return to Zero
PCB	Printed Circuit Board
PECL	Pseudo Emitter Coupled Logic
PHY	Physical layer device
PLL	Phase Lock Loop
PRBS	Pseudo Random Bit Sequence
R	Receiver
RFI	Radio Frequency Interference
RS	Recommended Standard
RT	Termination Resistor
RX	Receiver
SCI	Scalable Coherent Interface
SCSI	Small Computer Systems Interface
SDI	Serial Digital Interface
Ser/Des	Serializer/Deserializer
SUT	System Under Test
T	Transceiver
TDR	Time Domain Reflectometry
TEM	Transverse Electro-Magnetic
TFT	Thin Film Transistor
TI	Totally Irrelevant
TIA	Telecommunications Industry Association
TP	Test Point
TTL	Transistor Transistor Logic
TWP	Twisted Pair
TX	Transmitter
UTP	Unshielded Twisted Pair
VCM	Common-mode Voltage
VCR	Video Cassette Recorder

A.3 Detailed explanation of datasheet parameters

V_{IH} High level input voltage: TTL input specification used for data and control pins

V_{IL} Low level input voltage: TTL input specification used for data and control pins

V_{CL} Input clamp voltage: a specification for the clamp voltage given a current

I_{IN} Input current: the amount of current drawn by each TTL input

V_{OH} High level output voltage: TTL output specification used for data and control pins

V_{OL} Low level output voltage: TTL output specification used for data and control pins

I_{OS} Output short circuit current: amount of current drawn when outputs are shorted to GND

I_{OZ} TRI-STATE output current: amount of current drawn when the outputs are in TRI-STATE; the outputs are either disabled by a control pin or the device is put in powerdown mode

V_{TH} Differential threshold high voltage: any input signal above this threshold will have a logic HIGH on the output

V_{TL} Differential threshold low voltage: any signal below this threshold will have a logic low on the output

V_{OD} Output differential voltage: the amplitude result of (DO+) – (DO-)

ΔV_{OD} Output differential voltage unbalanced: the difference in amplitude between the positive and negative LVDS outputs

V_{OS} Offset voltage: the common-mode voltage of the LVDS output

ΔV_{OS} Offset voltage unbalanced: the difference in common-mode voltage between the positive and negative LVDS outputs

I_{OX} Power-off output current: the amount of current drawn when V_{DD} = 0 and the outputs are either at 0V or another positive voltage

I_{CCD} Serializer total supply current (includes load current): the total amount of current drawn by a serializer

I_{CCR} Receiver total supply current (includes load current): the total amount of jitter drawn by a deserializer

I_{CCT} Transceiver total supply current (includes load current): the amount of current drawn by both a serializer and a deserializer

I_{CCX} Transceiver total supply current when powered down: the total current drawn when a transceiver is put into powerdown mode

I_{CCXD} Serializer total supply current when powered down: the total current drawn by a serializer in powerdown mode

I_{CCXR} Receiver total supply current when powered down: the total current drawn by a receiver in powerdown mode

t_{TCP} Transmit clock period: a TTL clock input specification for the serializer

Appendix

t_{TCIH} Transmit clock high time: specification for the portion of the clock period that must be high

t_{TCIL} Transmit clock low time: specification for the portion of the clock period that must be low

t_{CLKT} TCLK input transition time: rise/fall time requirement for the input clock measured at 10% and 90%

t_{JIT} TCLK input jitter: the maximum amount of jitter that the input clock will tolerate

t_{LLHT} Bus LVDS low-to-high transition time (measured from 20% - 80%): rise time specification for the LVDS signal

t_{LHLT} Bus LVDS high-to-low transition time (measured from 20% - 80%): fall time specification for the LVDS signal

t_{DIS} D_{IN} (0-x) Setup to TCLK: setup time requirement between data and clock for a serializer

t_{DIH} D_{IN} (0-x) Hold from TCLK: hold time requirement between data and clock for a serializer

t_{HZD} D_O ± HIGH to TRI-STATE delay: the amount of time required for a serializer's LVDS outputs to change from HIGH to TRI-STATE

t_{LZD} D_O ± LOW to TRI-STATE delay: the amount of time required for a serializer's LVDS outputs to change from LOW to TRI-STATE

t_{ZHD} D_O ± TRI-STATE to HIGH delay: the amount of time required for a serializer's LVDS outputs to change from TRI-STATE to a HIGH state

t_{ZLD} D_O ± TRI-STATE to LOW delay: the amount of time required for a serializer's LVDS outputs to change from TRI-STATE to a LOW state

t_{SPW} SYNC pulse width: the number of clock cycles the SYNC pin must be asserted HIGH before the device enters SYNC mode and SYNC patterns appear at the LVDS outputs

t_{PLD} Serializer PLL lock time: the number of clock cycles the PLL requires to lock to the input clock before data can appear at the LVDS outputs

t_{SD} Serializer delay: the amount of time required for data to travel through a serializer

t_{RJIT} Random jitter: the amount of Gaussian jitter produced

t_{DJIT} Deterministic jitter: the amount of non-Gaussian jitter produced

t_{RFCP} REFCLK period: period requirement for the REFCLK input pin

t_{RFDC} REFCLK duty cycle: duty cycle requirement for the REFCLK input pin

$t_{RFCP/TCP}$ Ratio of REFCLK to TCLK: indicates the allowable difference between the TCLK and REFCLK periods

t_{RFFT} REFCLK transition time: the rise and fall time requirement for the REFCLK pin

t_{RCP} Recovered Clock (RCLK) period: the period of the clock recovered from the LVDS inputs

t_{RDC} RCLK duty cycle: the duty cycle of the clock recovered from the LVDS inputs

t_{CLH} CMOS/TTL low-to-high transition time: the rise time specification for TTL outputs

t_{CHL}	CMOS/TTL high-to-low transition time: the fall time specification for TTL outputs
t_{ROS}	R_{OUT} (0-x) setup data to RCLK: the amount of setup time provided between the RCLK edge (usually rising) and output data
t_{ROH}	R_{OUT} (0-x) hold data to RCLK: the amount of hold time provided between the RCLK edge (usually rising) and output data
t_{HZR}	HIGH to TRI-STATE delay: the amount of time for a deserializer's TTL outputs to change from HIGH to TRI-STATE
t_{LZR}	LOW to TRI-STATE Delay: the amount of time for a deserializer's TTL outputs to change from LOW to TRI-STATE
t_{ZHR}	TRI-STATE to HIGH delay: the amount of time for a deserializer's TTL outputs to change from TRI-STATE to HIGH
t_{ZLR}	TRI-STATE to LOW delay: the amount of time for a deserializer's TTL outputs to change from TRI-STATE to LOW
t_{DD}	Deserializer delay: the amount of time for data to travel through a deserializer
t_{DSR1}	Deserializer PLL lock time from PWRDWN: the amount of time required for the deserializer's PLL to lock after exiting powerdown mode
t_{DSR2}	Deserializer PLL lock time from SYNCPAT: the amount of time before the deserializer's PLL locks to the incoming SYNC pattern
t_{RNMI-R}	Ideal deserializer noise margin – Right: the amount of margin available for noise as measured from the ideal bit stop position to the right edge of the sampling window
t_{RNMI-L}	Ideal deserializer noise margin – Left: the amount of margin available for noise as measured from the ideal bit start position to the left edge of the sampling window

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Index

A

ANSI/TIA/EIA-644 standard: 1-3

Applications notes: 3-3, 3-4, 4-12, 6-3, 7-1, 7-6, 7-7, A-1

applications: *See LVDS applications*

B

backplane: 1-4, 2-5, 2-6, 2-7, 3-3, 4-5, 4-12, 5-1, 5-2, 5-3, 5-4, 5-5, 5-6, 5-7, 5-8, 5-9, 5-11, 5-13, 5-14, 8-1, A-1, A-2

behavioral model: *See IBIS*

BER testing: 7-7, 7-8, A-1, A-2

bidirectional: *See LVDS configurations*

Bit Error Rate Testing: *See BER testing*

Broadside stripline: 3-3, 3-4

Bus LVDS: 1-4, 2-4, 2-5, 2-7, 2-9, 4-8, 4-9, 4-10, 5-1, 5-2, 5-3, 5-4, 5-5, 5-6, 5-7, 5-8, 5-9, 5-11, 5-13, 8-1, A-1, A-2, A-6

bypassing: 3-1

C

cable shielding: 3-2, 3-6, 3-7, 3-8, 3-14, 5-11, 6-1, 6-3, 6-4

cables: 1-2, 1-3, 1-4, 2-2, 2-3, 2-4, 2-5, 2-6, 2-8, 2-9, 3-1, 3-3, 3-5, 3-14, 4-2, 4-8, 4-10, 4-11, 4-12, 5-5, 6-1, 6-2, 6-3, 6-4, 7-1, 7-4, 7-5, 7-6, 7-7, 7-8, 7-9, 7-10, A-2

CAT3 cable: *See twisted pair cable*

CAT5 cable: *See twisted pair cable*

Channel Link: 2-3, 2-5, 2-9, 3-2, 6-2, 8-1, A-1

CMR: *See common-mode noise rejection*

common-mode noise rejection: 1-1, 2-1, 3-1, 3-2, 3-3, 3-5, 3-7, 3-9, 3-10, 3-14, 3-15, 4-4, 4-6, 4-7, 4-8, 4-12, 5-13, 6-1, 6-3, 6-4, 7-6, A-3, A-5

comparisons to other technologies: 2-1, 2-3, 2-7, 2-8, 5-3, 5-4

connector: 1-4, 2-5, 2-6, 2-9, 3-2, 3-3, 5-1, 5-2, 5-5, 5-6, 5-11, 5-14, 6-1, 6-2, 6-3, 6-4, 7-4, 7-7, A-3

cost: 1-1, 1-5, 2-5, 2-6, 2-7, 2-8, 2-9, 5-5, 5-6, 6-1

Crosspoint: 2-9, 4-8, 8-1

crosstalk: 3-1, 4-4, 4-6, 6-4

D

data rate over cables: 1-1

demo boards: *See evaluation boards*

differential impedance: 1-2, 2-2, 3-1, 3-2, 3-3, 3-5, 3-8, 3-12, 4-2, 4-3, 5-8, 6-1

differential waveform: 4-4, 4-6, 4-7, 5-13, 7-1

drivers and receivers: 1-4, 2-1, 2-3, 2-9, 3-1, 4-8, 7-1, 7-4, 7-7, A-1

E

electromagnetic interference/radiation/compatibility: *See EMI*

EMI: 1-1, 3-1, 3-2, 3-4, 3-6, 3-7, 3-8, 3-9, 3-10, 3-12, 3-13, 3-14, 4-1, 4-2, 4-4, 4-5, 4-6, 5-4, 5-5, 6-1, 6-4, A-2

EMI test: 3-12

evaluation boards: 8-1

F

failsafe: 1-3, 4-1, 4-9, 4-10, 4-11, 4-12, 5-8, 5-12, 5-13, A-1

Flat Panel Display-Link: *See FPD*

flex circuit: 6-1, 6-2

floating pins: *See unused pins*

FPD: 2-9, 3-2, 6-2, 8-1, A-1, A-2

G

ground return path: 3-2, 3-14

H

hot insertion: 5-13

hot swap: *See hot insertion*

I

I/O models: *See IBIS*

IBIS: A-3

IEEE 1596.3: 1-3

IOFF: *See power off high impedance*

J

jitter: 7-1, 7-3, 7-5, 7-6, 7-7, A-5, A-6

L

live insertion: *See power off high impedance*

LVDS standard: *See ANSI/TIA/EIA-644 standard*

M

microstrip: 3-2, 3-3, 3-7, 3-8, 5-8

multipoint: 1-4, 2-5, 2-6, 2-9, 3-5, 4-9, 5-1, 5-2, 5-3, 5-8, 5-12, 5-13

N

noise: 1-1, 1-4, 1-5, 2-1, 2-3, 2-4, 2-5, 2-6, 2-7, 2-8, 2-9, 3-1, 3-2, 3-3, 3-5, 3-9, 3-10, 3-12, 3-14, 4-1, 4-2, 4-3, 4-4, 4-6, 4-7, 4-8, 4-9, 4-10, 4-11, 4-12, 5-1, 5-4, 5-5, 5-6, 5-7, 6-1, 6-3, 7-5, A-6

Index

P

PCB design: 1-1, 1-3, 2-2, 2-5, 2-6, 3-1, 3-2, 3-3, 3-4, 3-5, 3-7, 3-8, 3-9, 3-10, 3-12, 3-15, 4-1, 5-6, 5-10, 7-1, 7-4, 7-7, 8-1, A-1, A-3

PECL: 1-1, 2-1, 2-2, 2-3, 3-14, A-3

power off high impedance: 4-9, 4-12

power supply: 1-1, 1-3, 1-4, 2-1, 2-3, 3-2, 5-3, 7-8, 7-10

printed circuit board: *See PCB design*

probing: *See signal probing*

R

RAPIDESIGNER: 3-3, A-1

receivers: *See drivers and receivers*

ribbon: 4-2

RS-422: 1-1, 2-1, 2-3

S

SCI standard: *See IEEE 1596.3 standard*

shielding: *See cable shielding*

signal probing: 4-1, 7-5

simulation models: *See IBIS*

single-ended waveforms: 1-4, 2-1, 3-1, 3-6, 3-10, 3-13, 3-14, 4-5, 5-3, 5-4, 5-7, 5-8, 5-10, 5-11

stripline: 3-2, 3-3, 3-4, 3-7, 3-8

stub length: 2-4, 2-5, 2-6, 4-9, 5-2, 5-3, 5-6, 5-8, 5-9, 5-10

T

TDR measurements: 4-2, 4-3, 5-7, 5-8, 5-9, A-3

termination: 1-2, 1-4, 2-2, 2-3, 2-4, 2-9, 3-3, 3-5, 4-8, 4-9, 4-10, 4-11, 4-12, 5-1, 5-2, 5-3, 5-4, 5-5, 5-7, 5-8, 5-12, 5-13, A-3

time domain reflectometer: *See IBIS*

traces: 1-1, 1-3, 2-2, 2-6, 3-1, 3-2, 3-3, 3-4, 3-5, 3-6, 3-7, 3-8, 3-9, 3-14, 4-1, 5-1, 5-2, 5-5, 5-7, 5-11, 6-1, 6-2, 7-4, 7-7

TRI-STATE: 4-10, 5-12, 5-13, A-5, A-6

twisted pair cable: 2-4, 4-8, 4-12, 6-1, 6-2, 7-1, 7-4, 7-7, 7-10, A-3

TWP: *See twisted pair cable*

U

Unused pins: 4-1, 6-4

UTP: *See twisted pair cable*

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