# Rockchip

# RK3399

# Datasheet

**Revision 1.6**
**Mar. 2017**

# Revision History

| Date | Revision | Description |
|---|---|---|
| 2017-3-1 | 1.6 | ● Update |
| 2016-12-20 | 1.5 | ● Update "Recommended Operating Conditions" for CPU A72 |
| 2016-12-06 | 1.4 | ● Removed repeated "EMMC_COREDLL_0V9" in section 3.2<br>● Add ball description for "EMMC_COREDLL_0V9" in section 2.6 |
| 2016-10-30 | 1.3 | ● Updated ball description for DDR1 in section 2.6 |
| 2016-9-30 | 1.2 | ● Update the description about video codec |
| 2016-8-15 | 1.1 | ● Updated I2C information about Fast-mode plus feature<br>● Updated video codec about H264/H265/VP9<br>● Updated voltage information for power supply<br>● Updated PCIe specification<br>● Updated "Features" section |
| 2016-5-04 | 1.0 | ● Initial Release |

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# NOTICE

# Chapter 1 Introduction

## 1.1 Overview

RK3399 is a low power, high performance processor for computing, personal mobile internet devices and other smart device applications. Based on Big.Little architecture, it integrates dual-core Cortex-A72 and quad-core Cortex-A53 with separate NEON coprocessor.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3399 supports multi-format video decoders including H.264/H.265/VP9up to4Kx2K@60fps, especially, H.264/H.265 decoders support 10bits coding, and also supports H.264/MVC/VP8 encoders by 1080p@30fps, high-quality JPEG encoder/decoder, and special image preprocessor and postprocessor.

Embedded 3D GPU makes RK3399 completely compatible with OpenGL ES1.1/2.0/3.0/3.1, OpenCL and DirectX 11.1. Special 2D hardware engine with MMU will maximize display performance and provide very smooth operation.

RK3399 has high-performance dual channel external memory interface (DDR3/DDR3L/LPDDR3/LPDDR4) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

## 1.2 Features

**The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.**

### 1.2.1 Microprocessor

- Dual-core ARM Cortex-A72 MPCore processor and Quad-core ARM Cortex-A53MPCore processor, both are high-performance, low-power and cached application processor
- Two CPU clusters.Big cluster with dual-coreCortex-A72 is optimized for high-performance and little cluster with quad-core Cortex-A53 is optimized for low power.
- Full implementation of the ARM architecture v8-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerating media and signal processing
- ARMv8 Cryptography Extensions
- SCU ensures memory coherency between the MPCore for each cluster
- CCI500 ensures the memory coherency between the two clusters
- Each Cortex-A72 integrates48KB L1 instruction cache and 32KB L1 data cache with 4-way set associative. Each Cortex A53 integrates 32KB L1 instruction cache and 32kB L1 data cache separately with 4-way set associative
- 1MB unified L2 Cache for Big cluster, 512KB unified L2 Cache for Little cluster
- Trustzone technology support
- Full Coresight debug solution
  - Debug and trace visibility of whole systems
  - ETM trace support
  - Invasive and non-invasive debug
- Eight separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
  - PD_A72_B0: 1st Cortex-A72 + Neon + FPU + L1 I/D cache of big cluster
  - PD_A72_B1: 2nd Cortex-A72+ Neon + FPU + L1 I/D cache of big cluster
  - PD_SCU_B: SCU + L2 Cache controller, and including PD_A72_B0, PD_A72_B1, debug logic of big cluster
  - PD_A53_L0: 1st Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
  - PD_A53_L1: 2nd Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster

- PD_A53_L2: 3rd Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
- PD_A53_L3: 4th Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
- PD_SCU_L: SCU + L2 Cache controller, and including PD_A53_L0, PD_A53_L1, PD_A53_L2, PD_A53_L3, debug logic of little cluster

- Two isolated voltage domain to support DVFS for big cluster and little cluster separately.

### 1.2.2 Memory Organization

- Internal on-chip memory
  - BootROM
  - Internal SRAM
- External off-chip memory①
  - DDR3/DDR3L/LPDDR3/LPDDR4
  - SPI NOR/NAND Flash
  - eMMC 5.1
  - SD 3.0/MMC 4.51

### 1.2.3 Internal Memory

- Internal BootROM
  - Size : 32KB
  - Support system boot from the following device :
    - SPI interface
    - eMMC interface
    - SD/MMC interface
  - Support system code download by the following interface:
    - USB OTG interface
- Internal SRAM
  - Size : 200KB
  - Support security and non-security access
  - Security or non-security space is software programmable
  - Security space can be 0KB,4KB,8KB,12KB,16KB,… up to 64KB by 4KB step

### 1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/DDR3L/LPDDR3/LPDDR4)
  - Compatible with JEDEC standard DDR3-1866 /DDR3L-1866 /LPDDR3-1866 / LPDDR4 SDRAM
  - Support 2 channels, each channel is 16 or 32bits data width
  - Support up to 2 ranks (chip selects) for each channel; totally 4GB(max) address space. Maximum address space of one rank in a channel is also 4GB, which is software-configurable
  - 32bits/64bits data width is software programmable
  - Programmable timing parameters to support DDR3/DDR3L/LPDDR3/LPDDR4 SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Embedded dynamic drift detection in the PHY to get dynamic drift compensation with the controller
  - Programmable output and ODT impedance with dynamic PVT compensation
  - Low power modes, such as power-down and self-refresh for DDR3/DDR3L/LPDDR3/LPDDR4 SDRAM
  - Support standby mode to auto-gating DDR controller clock for power save
  - Support power down DDR controller and DDR PHY
  - Support hardware-based DDR frequency scaling

- eMMC Interface
  - Fully compliant with JEDEC eMMC 5.1and eMMC 5.0 specification
  - There is only one eMMC interface

- It is backward compliant with eMMC 4.51 and earlier versions specification.
- Supports HS400, HS200, DDR50 and legacy operating modes.
- Provide eMMC boot sequence to receive boot data from external eMMC device
- Configurable (Minimum 1 Block Size) FIFO used to aid data transfer between the CPU and the controller
- Handle the FIFO overrun and underrun condition by stopping interface clock
- Up to 3200Mbits per second data rate using 8 parallel data lines (eMMC HS400)
- Up to 1600Mbits per second data rate using 8 parallel data lines (eMMC HS200)
- Up to 832Mbits per second data rate using 8 parallel data lines (eMMC DDR52 mode)
- Transfers the data in 1 bit, 4 bit and 8 bit modes
- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.51
  - There are 2 MMC interfaces which can be configured as SD/MMC or SDIO
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - Data bus width is 4bits

### 1.2.5 System Component

- Cortex-M0
  - Two Cortex-M0 inside RK3399 to cooperate with Cortex-A72/Cortex-A53
  - Thumb instruction set combines high code density with 32-bit performance
  - Integrated sleep modes for low power consumption
  - Fast code execution permits slower processor clock or increases sleep mode time
  - Deterministic, high-performance interrupt handling for time-critical applications
  - Serial Wire Debug reduces the number of pins required for debugging

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK3399
  - One oscillator with 24MHz clock input and 8 embedded PLLs
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components

- PMU (power management unit)
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - 6 separate voltage domains
  - 30 separate power domains, which can be power up/down by software based on different application scenes

- Timer
  - 14 on-chip 64bits Timers in SoC with interrupt-based operation for non-secure application
  - 12 on-chip 64bits Timers in SoC with interrupt-based operation for secure application
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input

- PWM
  - Four on-chip PWMs with interrupt-based operation

- Programmable pre-scaled operation to bus clock and then further scaled
- Embedded 32-bit timer/counter facility
- Support capture mode
- Support continuous mode or one-shot mode
- Provides reference mode and output various duty-cycle waveform

- Watchdog
  - Three Watchdogs in SoC with 32 bits counter width
  - Counter clock is from APB bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- Mailbox
  - Two Mailboxes in SoC to service multi-core communication
  - Support four mailbox elements per mailbox, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide 32 lock registers for software to use to indicate whether mailbox is occupied

- Bus Architecture
  - 128bit/64-bit/32-bit multi-layer AXI/AHB/APB composite bus architecture
  - CCI500 embedded to support two clusters cache coherency
  - 5 embedded AXI interconnect
    - PERI low performance interconnect with one 128-bits AXI master, seven 64-bits AXI masters, one 32-bits AXI master, two 64-bits AXI slaves, five 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - PERI high performance interconnect with one 128-bits AXI master, one 128-bits AXI slave, four 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - DISPLAY interconnect with two 128-bits AXI masters, two 64-bits AXI masters, one 32-bits AXI master and lots of 32-bits AHB/APB slaves
    - GPU interconnect with one 128-bits AXI master and 32-bits APB slave
    - VIDEO interconnect with two 128-bits AXI masters, two 64-bits AXI masters and four 32-bits AHB slaves
  - Flexible different QoS solution to improve the utility of bus bandwidth

- Interrupt Controller
  - Support 8 PPI interrupt source and 148 SPI interrupt sources input from different components inside RK3399
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed, high-level sensitive for SPI and low-level sensitive for PPI
  - Support Locality-specific Peripheral Interrupts (LPIs). These interrupts are generated by a peripheral writing to a memory-mapped register in the controller
  - Two AXI stream interrupt interfaces separately for each cluster
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache

- Embedded DMA manager thread
- Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
- Signals the occurrence of various DMA events using the interrupt output signals
- Mapping relationship between each channel and different interrupt outputs is software-programmable
- Two embedded DMA controller, BUS_DMAC is for bus system, PERI_DMAC is for peripheral system
- DMAC0 features:
  - 6 channels totally
  - 10 hardware request from peripherals
  - 2 interrupt output
  - Dual APB slave interface for register configuration, designated as secure and non-secure
  - Support Trustzone technology and programmable secure state for each DMA channel
- DMAC1 features:
  - 8 channels totally
  - 20 hardware request from peripherals
  - 2 interrupt output
  - Dual APB slave interface for register configuration, designated as secure and non-secure
  - Support Trustzone technology and programmable secure state for each DMA channel

- Security system
  - Support Trustzone technology for the following components inside RK3399
    - Cortex-A72, support security and non-security mode, switch by software
    - Cortex-A53, support security and non-security mode, switch by software
    - Except Cortex-A72 and Cortex-A53, the other masters in the SoC can also support security and non-security mode by software-programmable
    - Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
    - Internal memory, part of space is addressed only in security mode, detailed size is software-programmable together with TZMA (Trustzone memory adapter)
    - External DDR space can be divided into eight parts; each part can be software-programmable to be addressed in security mode or non-security mode
  - Embedded dual-channel encryption and decryption engine
    - Support AES 128/192/256 bits key mode, ECB/CBC/CTR/XTS chain mode, Slave/FIFO mode
    - Support DES/3DES (ECB and CBC chain mode), 3DES (EDE/EEE key mode), Slave/FIFO mode
    - Support SHA1/SHA256/MD5(with hardware padding) HASH function, FIFO mode only
    - Support 160-bit Pseudo Random Number Generator (PRNG)
    - Support 256-bit True Random Number Generator (TRNG)
    - Support PKA 512/1024/2048 bit Exp Modulator
  - Support security boot
  - Support security debug

### 1.2.6 Video CODEC

- Video Decoder
  - MMU embedded

- Real-time video decoder of MPEG-1, MPEG-2, MPEG-4, H.263, H.264, H.265, VC-1, VP9, VP8, MVC
- H.264/AVC, Base/Main/High/High10 profile @ level 5.1; up to 4Kx2K @ 30fps
- H.265/HEVC, Main/Main10 profile @ level 5.1 High-tier; up to 4Kx2K @ 60fps
- VP9, profile 0, up to 4Kx2K @ 60fps
- MPEG-1, ISO/IEC 11172-2, up to 1080P @ 60fps
- MPEG-2, ISO/IEC 13818-2, SP@ML, MP@HL, up to 1080P @ 60fps
- MPEG-4, ISO/IEC 14496-2, SP@L0-3, ASP@L0-5, up to 1080P @ 60fps
- VC-1, SP@ML, MP@HL, AP@L0-3, up to 1080P @ 60fps
- MVC is supported based on H.264 or H.265, up to 1080P @ 60fps
- 
- Supports frame timeout interrupt, frame finish interrupt and bit stream error interrupt
- Error detection and concealment support for all video formats
- Output data format YUV420 semi-planar, YUV400(monochrome), YUV422 is supported by H.264
- For MPEG-4, GMC (global motion compensation) not supported
- For VC-1, up-scaling and range mapping are supported in image post-processor
- For MPEG-4 SP/H.263, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

- Video Encoder
  - Support video encoder for H.264 UP to HP@level4.1, MVC and VP8
  - MMU Embedded
  - Only support I and P slices, not B slices
  - Support error resilience based on constrained intra prediction and slices
  - Input data format:
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Image size is from 96x96 to 1920x1080(Full HD)
  - Maximum frame rate is up to 1920x1080@30FPS②

### 1.2.7 JPEG CODEC

- JPEG decoder
  - Input JPEG file: YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image: YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI (region of image) decode
  - Maximum data rate④ is up to 76million pixels per second
  - Embedded memory management unit(MMU)

- JPEG encoder
  - Input raw image:
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555

 

- RGB565 and BGR565
- RGB888 and BRG888
- RGB101010 and BRG101010

- Output JPEG file: JFIF file format 1.02 or Non-progressive JPEG
- Encoder image size up to 8192x8192(64million pixels) from 96x32
- Maximum data rate④ up to 90million pixels per second
- Embedded memory management unit(MMU)

### 1.2.8 Image Enhancement

- Image pre-processor
  - Only used together with HD video encoder inside RK3399, not support stand-alone mode
  - Provides RGB to YCbCr 4:2:0 color space conversion, compatible with BT601, BT709 or user defined coefficients
  - Provides YCbCr4:2:2 to YCbCr4:2:0 color space conversion
  - Support cropping operation from 8192x8192 to any supported encoding size
  - Support rotation with 90 or 270 degrees
- Video stabilization
  - Work in combined mode with HD video encoder inside RK3399 and stand-alone mode
  - Adaptive motion compensation filter
  - Support scene detection from video sequence, encodes key frame when scene change noticed
- Image Post-Processor (embedded inside video decoder)
  - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
  - Also work as a stand-alone mode, its input data is from image data stored in external memory
  - Input data format:
    - Any format generated by video decoder in combined mode
    - YCbCr 4:2:0 semi-planar
    - YCbCr 4:2:0 planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
  - Output data format:
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
    - Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888, RGB565, ARGB4444 etc.
  - Input image size:
    - Combined mode: from 48x48 to 8176x8176 (66.8Mpixels)
    - Stand-alone mode: width from 48 to 8176, height from 48 to 8176, and maximum size limited to 16.7Mpixels
    - Step size is 16 pixels
  - Output image size: from 16x16 to 1920x1088 (horizontal step size 8, vertical step size 2)
  - Support image up-scaling:
    - Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
    - Arbitrary non-integer scaling ratio separately for both dimensions
    - Maximum output width is 3x input width
    - Maximum output height is 3x input height

 

- Support image down-scaling:
  - Arbitrary non-integer scaling ratio separately for both dimensions
  - Unlimited down-scaling ratio
- Support YUV to RGB color conversion, compatible with BT.601-5, BT.709 and user definable conversion coefficient
- Support dithering (2x2 ordered spatial dithering) for 4/5/6bit RGB channel precision
- Support programmable alpha channel and alpha blending operation with the following overlay input formats:
  - 8bit alpha +YUV444, big endian channel order with AYUV8888
  - 8bit alpha +24bit RGB, big endian channel order with ARGB8888
- Support de-interlacing with conditional spatial de-interlace filtering, only compatible with YUV420 input format
- Support RGB image contrast/brightness/color saturation adjustment
- Support image cropping & digital zoom only for JPEG or stand-alone mode
- Support picture in picture
- Support image rotation (horizontal flip, vertical flip, rotation 90,180 or 270 degrees)

- Image Enhancement-Processor (IEP)
  - Image format
    - Input data: XRGB/RGB565/YUV420/YUV422
    - Output data: ARGB/RGB565/YUV420/YUV422
    - The format ARGB/XRGB/RGB565/YUV support swap
    - Support YUV semi-planar/planar
    - Support BT601_l/BT601_f/BT709_l/BT709_f color space conversion
    - Support RGB dither up/down conversion
    - Support YUV up/down sampling conversion
    - Max resolution for static image up to 8192x8192
    - Max resolution for dynamic image
      - De-interlace: 1920x1080
      - Sampling noise reduction: 1920x1080
      - Compression noise reduction: 4096x2304
      - Enhancement: 4096x2304
  - Enhancement
    - Gamma adjustment with programmable mapping table
    - Hue/Saturation/Brightness/Contrast enhancement
    - Color enhancement with programmable coefficient
    - Detail enhancement with filter matrix up to 7x7
    - Edge enhancement with filter matrix up to 7x7
    - Programmable difference table for detail enhancement
    - Programmable distance table for detail and edge enhancement
  - Noise reduction
    - Compression noise reduction with filter matrix up to 7x7
    - Programmable difference table for compression noise reduction
    - Programmable distance table for compression noise reduction
    - Spatial sampling noise reduction
    - Temporal sampling noise reduction
    - Optional coefficient for sampling noise reduction
  - De-interlace
    - Input 4 fields, output 2 frames mode
    - Input 4 fields, output 1 frames mode
    - Input 2 fields, output 1 frames mode
    - Programmable motion detection coefficient
    - Programmable high frequency factor
    - Programmable edge interpolation parameter
    - Source width up to 1920
  - Embedded memory management unit(MMU)

 

### 1.2.9 Graphics Engine

- 3D Graphics Engine:
  - ARM Mali-T860MP4 GPU, support OpenGL ES1.1/2.0/3.0, OpenCL1.2, DirectX11.1 etc.
  - Embedded 4 shader cores with shared hierarchical tiler
  - Provide MMU and L2 Cache with 256KB size
  - Image quality using double-precision FP64, and anti-aliasing capabilities
  - 10-bit and 16-bit YUV input and output formats

- 2D Graphics Engine:
  - Source format:
    - ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422(SupportYUV422SP10bit/YUV420SP10bit)
  - Destination formats:
    - ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422(Support YVYU422/420 output)
  - Max resolution: 8192x8192 source, 4096x4096 destination
  - Block transfer and Transparency mode
  - Color fill with gradient fill, and pattern fill
  - Alpha blending modes including global alpha, per pixel alpha (color/alpha channel separately) and fading
  - Arbitrary non-integer scaling ratio, from 1/16 to 16
  - 0, 90, 180, 270-degree rotation, x-mirror, y-mirror & rotation operation
  - ROP2, ROP3, ROP4
  - Support 4k/64k page size MMU

### 1.2.10 Video IN/OUT

- Camera Interface
  - One or two MIPI-CSI input interface
- Image Signal Processer
  - There are two ISP (Image Sensor Processor) built-in
  - Maximum input resolution of one ISP is 14M pixels
  - Main scaler with pixel-accurate up-scaling and down-scaling to any resolution between 4416x3312 and 32x16 pixel in processing mode
  - Self scaler with pixel-accurate up-scaling and down-scaling to any resolution between 1920x1080 and 32x16 pixel in processing mode
  - support of semi planar NV21 color storage format
  - support of independent image cropping on main and self-path
  - ITU-R BT 601/656 compliant video interface supporting YCbCr or RGB Bayer data
  - 12-bit camera interface
  - 12-bit resolution per color component internally
  - YCbCr 4:2:2 processing
  - quantization and Huffman tables
  - Windowing and frame synchronization
  - Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
  - Luminance/chrominance and chrominance blue/red swapping for YUV input signals
  - Continuous resize support
  - Color processing (contrast, saturation, brightness, hue, offset, range)
  - Display-ready RGB output in self-picture path (RGB888, RGB666 and RGB565)
  - Rotation unit in self-picture path (90°, 180°, 270° and h/v flipping) for RGB output
  - Read port provided to read back a picture from system memory
  - Simultaneous picture read back, resizing and storing through self path while main
  - path captures the camera picture
  - Black level compensation

- Four channel Lens shade correction (Vignetting)
- Auto focus measurement
- White balancing and black level measurement
- Auto exposure support by brightness measurement in 5x5 sub windows
- Defect pixel cluster correction unit (DPCC) supports on the fly and table based pixel correction
- De-noising pre filter (DPF)
- Enhanced color interpolation (RGB Bayer demosaicing)
- Chromatic aberration correction
- Combined edge sensitive Sharpening / Blurring filter (Noise filter)
- Color correction matrix (cross talk matrix)
- Global Tone Mapping with wide dynamic range unit (WDR)
- Image Stabilization support and Video Stabilization Measurement
- Flexible Histogram calculation
- Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)
- Solarize effect through gamma correction

- Display Interface
  - Embedded two VOP, output from the following display interface.
    - One or Two MIPI-DSI port
    - One eDP port
    - One DP port
    - One HDMI port
  - Support AFBC function co-operation with GPU
    - decompress FB generated by GPU FBC
    - support 2560x1600 UI
    - support ARGB888, RGB888, RGB565
    - output for one layer among WIN0/1/2/3
    - only support one IFDBC block which can be used for WIN0/1/2/3 by configuration

- Video Output Processor(VOP_BIG)
  - Display interface
    - HDMI interface
      - Support 480p/480i/576p/576i/720p/1080p/1080i/4k
      - Support RGB/YUV420(up to 10bit) format
    - DP interface
      - Support progressive/interlace
      - Support RGB/YUV420/YUV422/YUV444(up to 10bit) format
    - MIPI interface
      - MIPI DCS command mode
      - Dual-MIPI
    - EDP interface
    - Max resolution
      - Max input resolution：4096x2304
      - Max output resolution：4096x2160
    - Scanning timing 8192x4096
    - Support configurable polarity of DCLK/HSYNC/VSYNC/DEN
  - Display process
    - CABC
    - BCSH,10bit
    - Support display data swap
    - Support YUV2RGB transition and RGB2YUV transition
    - Support YUV2YUV
    - GAMMA
    - Support blank display and black display

- Support standby mode
- X-MIRROR, Y-MIRROR for win0/win1/win2/win3/hwc
- scale down for TV over scan

- Layer process
  - Background layer
    - programmable 30-bit color
  - Afbcd
    - format: ARGB8888/RGB888/RGB565
    - Support block split
    - win_sel(win0/win1/win2/win3)
  - Win0/Win1 layer
    - Support data format
      - RGB888, ARGB888, RGB565,
      - YCbCr420SP, YCbCr422SP, CbCr444SP, YUYV420, YUYV422, YVYU420, YVYU422
      - RGB(8bit), YUV(8bit/10bit), YVYU/YUYV(8bit)
    - YUV clip
      - Y-8bit: 16~235; UV-8bit: 16~240
      - Y-10bit: 64~940; UV-10bit: 64~960
    - CSC
      - RGB2YUV, YUV2RGB, RGB2RGB, YUV2YUV
    - Support max input resolution 4096x8192
    - Support max output resolution 4096x2160
    - Support virtual display
    - Support 1/8 to 8 scaling-down and scaling-up engine
      - scale up using Bicubic and bilinear
      - scale down using bilinear and average
      - per-pix alpha + scale
    - Support data swap
      - RGB/BPP: rb_swap
      - YUV: mid_swap, uv_swap
    - transparency color key, prior to alpha blending and fading
    - Support fading/alpha blending
    - Support interlace output
  - Win2/Win3 layer
    - Support data format
      - RGB888, ARGB888, RGB565
      - 8BPP
      - little endian and big endian for BPP
      - BYPASS and LUT mode(32bit LUT，8bit AA+8bit-RGB) for BPP
    - CSC
      - RGB2YUV, RGB2RGB
    - 4 display regions
      - only one region at one scanning line
    - Support data swap
      - RGB/BPP: rb_swap
    - Support transparency color key, prior to alpha blending and fading
    - Support fading/alpha blending
    - Support interlace output
  - Hardware Cursor layer
    - Support data format
      - RGB888, ARGB888, RGB565
      - 8BPP
      - little endian and big endian for BPP
      - BYPASS and LUT mode(32bit LUT，8bit AA+8bit-RGB)for BPP
    - CSC
      - RGB2YUV

- Support four hwc size: 32x32,64x64,96x96,128x128
- Support 2 color modes: normal and reversed color
- Support fading/alpha blending
- Support displaying out of panel, right or bottom
- Support interlace output

- Support p2i
- Overlay
  - support RGB and YUV domain overlay
  - Support 6 layers, background/win0/win1/win2/win3/hwc
  - Win0/Win1/Win2/Win3 overlay position exchangeable
  - Alpha blending
    - Support multi alpha blending modes
    - Support pre-multiplied alpha
    - Support global alpha and per_pix alpha
    - Support 256 level alpha
    - Layer0/layer1/layer2/layer3/hwc support alpha

- Write back
  - Support format
    - RGB565(8bit), RGB888P(8bit)
    - YUV420(8bit)
  - Support scale
    - horizontal scale down using bilinear, 0.25~1.0
    - vertical throw odd/even line
- Embedded memory management unit(MMU)

- Video Output Processor(VOP_LIT)
  - Display interface
    - HDMI interface
      - Support 480p/480i/576p/576i/720p/1080p/1080i
      - Support RGB format
    - DP interface
      - Support progressive/interlace
      - Support RGB/YUV420/YUV422/YUV444format
    - MIPI interface
      - MIPI DCS command mode
      - Dual-MIPI
    - EDP interface
    - Max resolution
      - Max input resolution：4096x2304
      - Max output resolution：2560x1600
    - Scanning timing 8192x4096
    - Support configurable polarity of DCLK/HSYNC/VSYNC/DEN
  - Display process
    - CABC
    - BCSH,10bit
    - Support display data swap
    - Support YUV2RGB transition and RGB2YUV transition
    - Support YUV2YUV
    - GAMMA
    - Support blank display and black display
    - Support standby mode
    - X-MIRROR, Y-MIRROR for win0/win2/hwc
    - scale down for TV overscan
  - Layer process
    - Background layer
      - programmable30 bit color
    - Win0 layer

 

- Support data format
  - RGB888, ARGB888, RGB565,
  - YCbCr420SP, YCbCr422SP, CbCr444SP, YUYV420, YUYV422, YVYU420, YVYU422
  - RGB(8bit), YUV(8bit), YVYU/YUYV(8bit)
- YUV clip
  - Y-8bit: 16~235; UV-8bit: 16~240
- CSC
  - RGB2YUV, YUV2RGB, RGB2RGB, YUV2YUV
- Support max input resolution 4096x8192
- Support max output resolution 2560x1600
- Support virtual display
- Support 1/8 to 8 scaling-down and scaling-up engine
  - scale up using Bicubic and bilinear
  - scale down using bilinear and average
  - per-pix alpha + scale
- Support data swap
  - RGB/BPP: rb_swap
  - YUV: mid_swap, uv_swap
- transparency color key, prior to alpha blending and fading
- Support fading/alpha blending
- Support interlace output

◆ Win2 layer
- Support data format
  - RGB888, ARGB888, RGB565
  - 8BPP
  - little endian and big endian for BPP
  - BYPASS and LUT mode(32bit LUT，8bit AA+8bit-RGB) for BPP
- CSC
  - RGB2YUV, RGB2RGB
- 4 display regions
  - only one region at one scanning line
- Support data swap
  - RGB/BPP: rb_swap
- Support transparency color key, prior to alpha blending and fading
- Support fading/alpha blending
- Support interlace output

◆ Hardware Cursor layer
- Support data format
  - RGB888, ARGB888, RGB565
  - 8BPP
  - little endian and big endian for BPP
  - BYPASS and LUT mode(32bit LUT，8bit AA+8bit-RGB)for BPP
- CSC
  - RGB2YUV
- Support four hwc size: 32x32,64x64,96x96,128x128
- Support 2 color modes: normal and reversed color
- Support fading/alpha blending
- Support displaying out of panel, right or bottom
- Support interlace output

◆ Support p2i

◆ Overlay
- support RGB and YUV domain overlay
- Support 4 layers, background/win0/win2/hwc
- Win0/Win2 overlay position exchangeable
- Alpha blending
  - Support multi alpha blending modes

- ✧ Support pre-multiplied alpha
- ✧ Support global alpha and per_pix alpha
- ✧ Support 256 level alpha
- ✧ Layer0/layer2/hwc support alpha

◆ Embedded memory management unit(MMU)

### 1.2.11 HDMI

- Single Physical Layer PHY with support for HDMI 1.4 and 2.0 operation
- For HDMI operation, support for the following:
  - HPD input analog comparator
  - 13.5–600MHz input reference clock
  - Up to 10-bit Deep Color modes
  - Up to 18Gbps aggregate bandwidth
  - Up to 1080p at 120Hz and 4kx2k at 60Hz HDTV display resolutions and up to QXGA graphic display resolutions
  - 3-D video formats
- Link controller flexible interface with 30-, 60- or 120-bit SDR data access
- Support HDCP 1.4/2.2

### 1.2.12 MIPI PHY

- Embedded 3 MIPI PHY, MIPI0 only for DSI, MIPI1 for DSI or CSI, MIPI2 only for CSI
- Lane operation ranging from 80 Mbps to 1.5 Gbps in forward direction
- Each port has 4 data lane, providing up to 6.0 Gbps data rate
- Support 1080p@60fps output with single channel
- Support 2560x1600@60fps output with MIPI0 and MIPI1 dual channel

### 1.2.13 eDP PHY

- Compliant with eDP™ Specification, version 1.3
- Support RGB 6/8/10bitvideo format
- Up to 4 physical lanes of 2.7/1.62 Gbps/lane
- Support VESA DMT and CVT timing standards
- Fully support EIA/CEA-861Dvideo timing and Info Frame structure
- Hot plug and unplug detection and link status monitor
- Supports Panel Self Refresh(PSR)

### 1.2.14 DisplayPort

- Compliant with DisplayPort Specification, version 1.2
- Compliant with HDCP2.2 (and back compatible with HDCP1.3)
- There is only one DisplayPort controller built-in RK3399 which is shared by 2 Type-C interface
- 25-600Mhz pixel clock
- Supports 8/10 bpp RGB, YCbCr422, YCbCr420formats
- Supports up to 4kx2k at 60Hz resolution
- Variety of audio formats–PCM and compressed, over I2S or SPDIF interfaces
- 1Mbps AUX channel

### 1.2.15 TYPE-C Interface

- Embedded 2 Type-C PHY
- Compliant with USB Type-C Specification, revision 1.1
- Compliant with USB Power Delivery Specification, revision 2.0
- Attach/detach detection and signaling as DFP, UFP and DRP
- Plug orientation/cable twist detection
- Enable/disable VBUS as DFP and DRP (when operating as DFP)
- VBUS detection as UFP and DRP (when operating as UFP)
- USB Power Delivery communication across the CC wire

- Support USB3.0 Type-C and DisplayPort 1.2 Alt Mode on USB Type-C. Two PMA TX-only lanes and two PMA half-duplex TX/RX lanes (can be configured as TX-only or RX-only)
- Up to 5Gbps data rate for USB3.0
- Up to 5.4Gbps(HBR2) data rate for DP1.2, can support 1/2/4 lane mode
- Support DisplayPort AUX channel

### 1.2.16 Audio Interface

- I2S/PCM
  - Three I2S/PCM in SoC
  - I2S0/I2S2 support up to 8 channels TX and 8 channels RX. I2S1 supports up to 2 channels TX and 2 channels RX
  - I2S2 is connected to HDMI and DisplayPort internally. I2S0 and I2S1 are exposed for peripherals.
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - I2S and PCM mode cannot be used at the same time

- SPDIF
  - Support two 16-bit audio data store together in one 32-bit wide location
  - Support biphase format stereo audio data output
  - Support 16 to 31-bit audio data left or right justified in 32-bit wide sample data buffer
  - Support 16, 20, 24 bits audio data transfer in linear PCM mode
  - Support non-linear PCM transfer

### 1.2.17 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus width
  - There are 2 total MMC interfaces which may be configured as SD/MMC or SDIO

- GMAC 10/100/1000M Ethernet Controller
  - There is one Giga Ethernet interface
  - Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - Supports both full-duplex and half-duplex operation
  - Preamble and start-of-frame data (SFD) insertion in Transmit, and deletion in Receive paths
  - Automatic CRC and pad generation controllable on a per-frame basis
  - Options for Automatic Pad/CRC Stripping on receive frames
  - Programmable InterFrameGap (40-96 bit times in steps of 8)
  - Supports a variety of flexible address filtering modes
  - Separate 32-bit status returned for transmission and reception packets
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Support detection of LAN wake-up frames and AMD Magic Packet frames
  - Support checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame
  - Support checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams
  - Comprehensive status reporting for normal operation and transfers with errors
  - Automatic generation of PAUSE frame control or backpressure signal to the GMAC core based on Receive FIFO-fill (threshold configurable) level
  - Handles automatic retransmission of Collision frames for transmission

- Discards frames on late collision, excessive collisions, excessive deferral and underrun conditions

- SPI Controller
  - 6 on-chip SPI controllers are inside
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
  - Embedded two 32x16bits FIFO for TX and RX operation respectively

- UART Controller
  - 5 on-chip UART controllers inside RK3399
  - DMA-based or interrupt-based operation
  - Embedded two 64Bytes FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start,stop and parity
  - Support different input clock for UART operation to get up to 4Mbps or other special baud rate
  - Support non-integer clock divides for baud clock generation
  - Support auto flow control mode for UART0 and UART3

- I2C controller
  - 9 on-chip I2C controllers
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Serial 8bits oriented and bidirectional data transfers can be made
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode or up to 1 Mbit/s in Fast-mode Plus.

- GPIO
  - 5 groups of GPIO (GPIO0~GPIO4), totally have 122 GPIOs
  - All of GPIOs can be used to generate interrupt to CPU
  - GPIO0 and GPIO1 can be used to wakeup system from low-power mode
  - The pull direction (pull-up or pull-down) for all of GPIOs are software-programmable
  - All of GPIOs are always in input direction in default after power-on-reset
  - The drive strength for all of GPIOs is software-programmable

- USB OTG3.0
  - Embedded 2 USB OTG3.0 interfaces
  - Compatible Specification
    - Universal Serial Bus 3.0 Specification, Revision 1.0
    - Universal Serial Bus Specification, Revision 2.0
    - eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  - Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer
  - Simultaneous IN and OUT transfer for USB3.0, up to 8Gbps bandwidth
  - Descriptor Caching and Data Pre-fetching
  - USB3.0 Device Features
    - Up to 7 IN endpoints, including control endpoint 0
    - Up to 6 OUT endpoints, including control endpoint 0
    - Up to 13 endpoint transfer resources, each one for each endpoint
    - Flexible endpoint configuration for multiple applications/USB set-configuration modes
    - Hardware handles ERDY and burst
    - Stream-based bulk endpoints with controller automatically initiating data movement

    - Isochronous endpoints with isochronous data in data buffers
    - Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support
  - USB 3.0 xHCI Host Features
    - Support up to 64 devices
    - Support 1 interrupter
    - Support 1 USB2.0 port and 1 Super-Speed port
    - Concurrent USB3.0/USB2.0 traffic, up to 8.48Gbps bandwidth
    - Support standard or open-source xHCI and class driver
    - Support xHCI Debug Capability
  - USB 3.0 Dual-Role Device (DRD) Features
    - Static Device operation
    - Static Host operation
    - USB3.0/USB2.0 OTG A device and B device basing on ID
    - UFP/DFP and Data Role Swap Defined in USB TypeC Specification
    - Not support USB3.0/USB2.0 OTG session request protocol(SRP), host negotiation protocol(HNP) and Role Swap Protocol(RSP)

- USB 2.0 Host
  - Embedded 2 USB 2.0 Host interfaces
  - Compatible with USB 2.0Host specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- PCIe
  - One PCIe port in RK3399
  - Compatible with PCI Express Base Specification Revision 2.1
  - Dual operation mode: Root Complex(RC)and End Point(EP)
  - Maximum link width is 4, single bi-directional Link interface
  - Support 2.5GT/s serial data transmission rate per lane per direction
  - Support DMA within the module, 2 channels, 2 RAM partitions, 2K bytes depth
  - Support Resizable BAR Capability
  - Support Single Physical PCI Functions in Endpoint Mode
  - Support Legacy Interrupt and MSI and MSI-X interrupt
  - Support Outbound and Inbound Address Translation
  - Support 8 Virtual Functions attached to Physical Function
  - Support PCI Express Active State Power Management (ASPM) state L0s and L1
  - Support L1 Power Management Substate
  - Support PCI Function power states D0, D1 and D3, and the corresponding link power states L0, L1 and L2

### 1.2.18 Others

- Temperature Sensor(TS-ADC)
  - Embedded 2 channel TS-ADC in RK3399
  - TS-ADC clock must be less than 800KHZ
  - 10-bits TS-ADC up to 50KS/s sampling rate
  - -40~125C temperature range and 5℃ temperature resolution

- SAR-ADC (Successive Approximation Register)
  - 6-channel single-ended 10-bit SAR analog-to-digital converter
  - SAR-ADC clock must be less than 13MHZ
  - Conversion speed range is up to 1MS/s sampling rate

- eFuse
  - Two 1024bits(32x32) high-density electrical Fuse are integrated in RK3399

- Support standby mode and power down mode
- Embedded power-switch
- Embedded four redundancy bits

- Package Type
  - FCBGA828(body: 21mmx21mm; ball size: 0.35mm; ball pitch: 0.65mm)

*Notes :*① *DDR3/DDR3L/LPDDR3/LPDDR4could not be used simultaneously*
②*Actual maximum frame rate will depend on the clock frequency and system bus performance*
③*Actual maximum data rate will depend on the clock frequency and JPEG compression rate*

## 1.3 Block Diagram

The following diagram shows the basic block diagram.

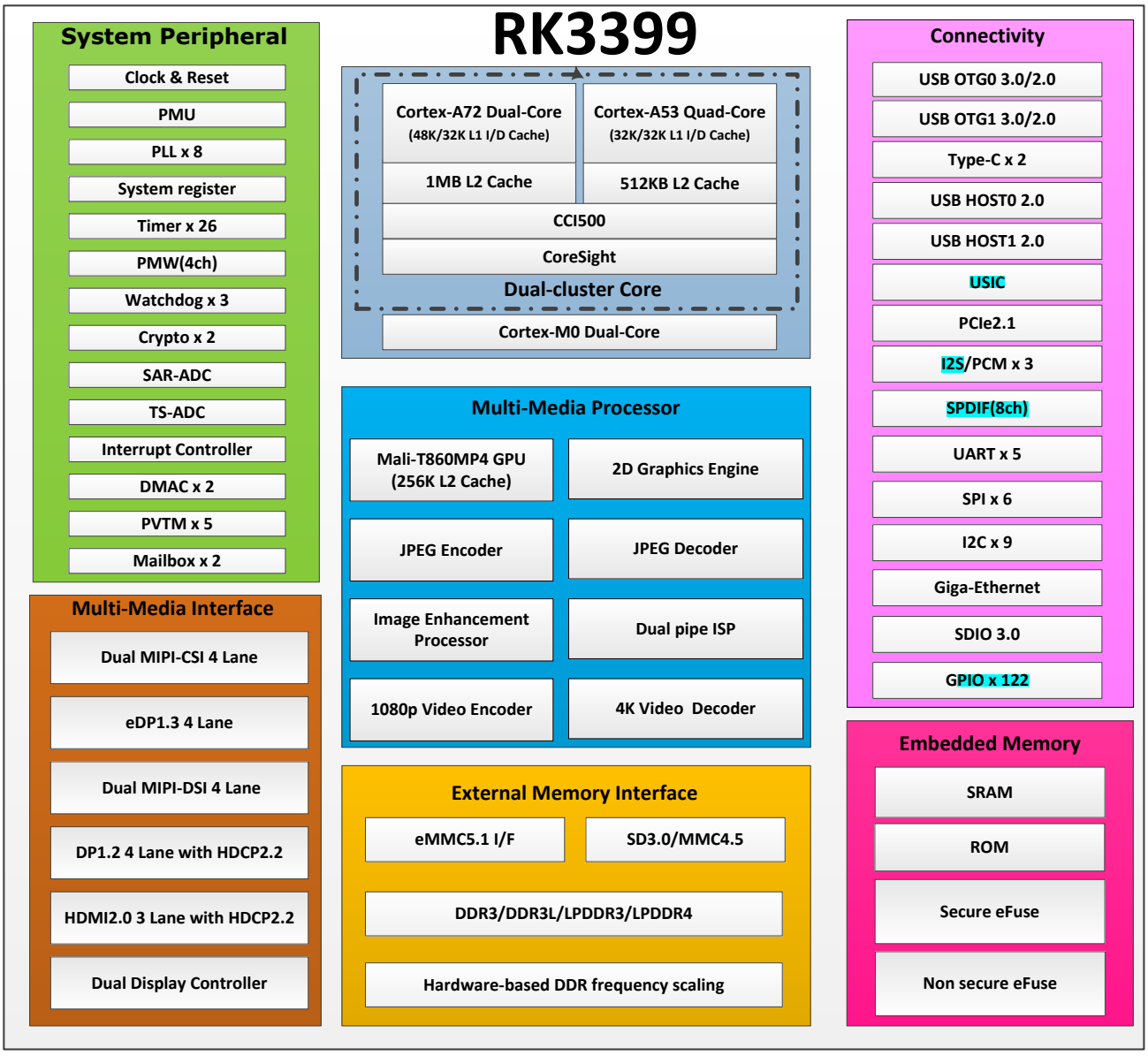


Fig. 1-1 Block Diagram

# Chapter 2 Package information

## 2.1 Ordering information

| Orderable Device | RoHS status | Package | Package Qty | Device special feature |
|---|---|---|---|---|
| RK3399 | Pb-Free | FCBGA828 | 600 | Cortex A72 + Cortex A53 |

## 2.2 Top Marking

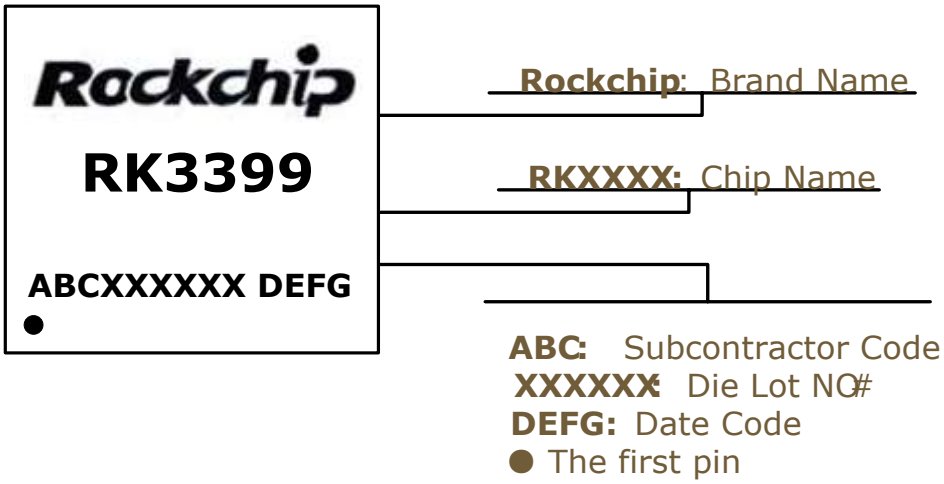


Fig. 2-1 Top Marking

## 2.3 Dimension

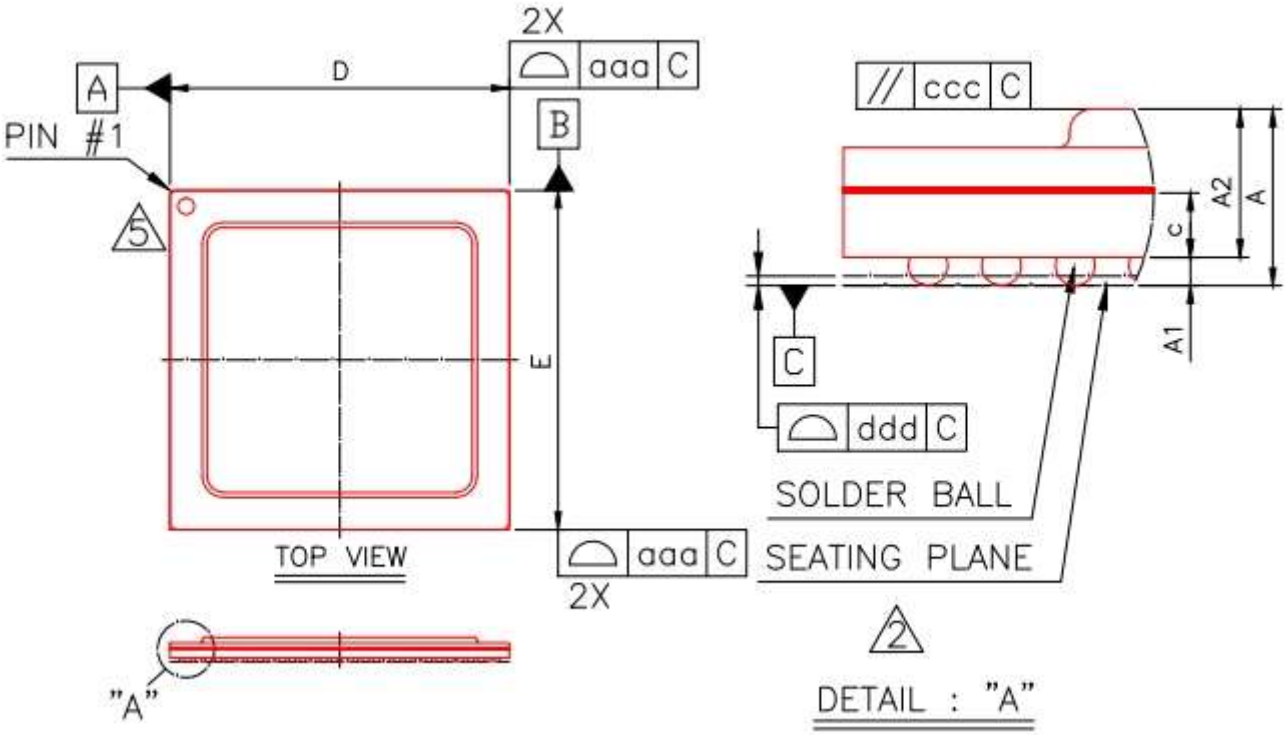


Fig. 2-2 Package Top and SideView

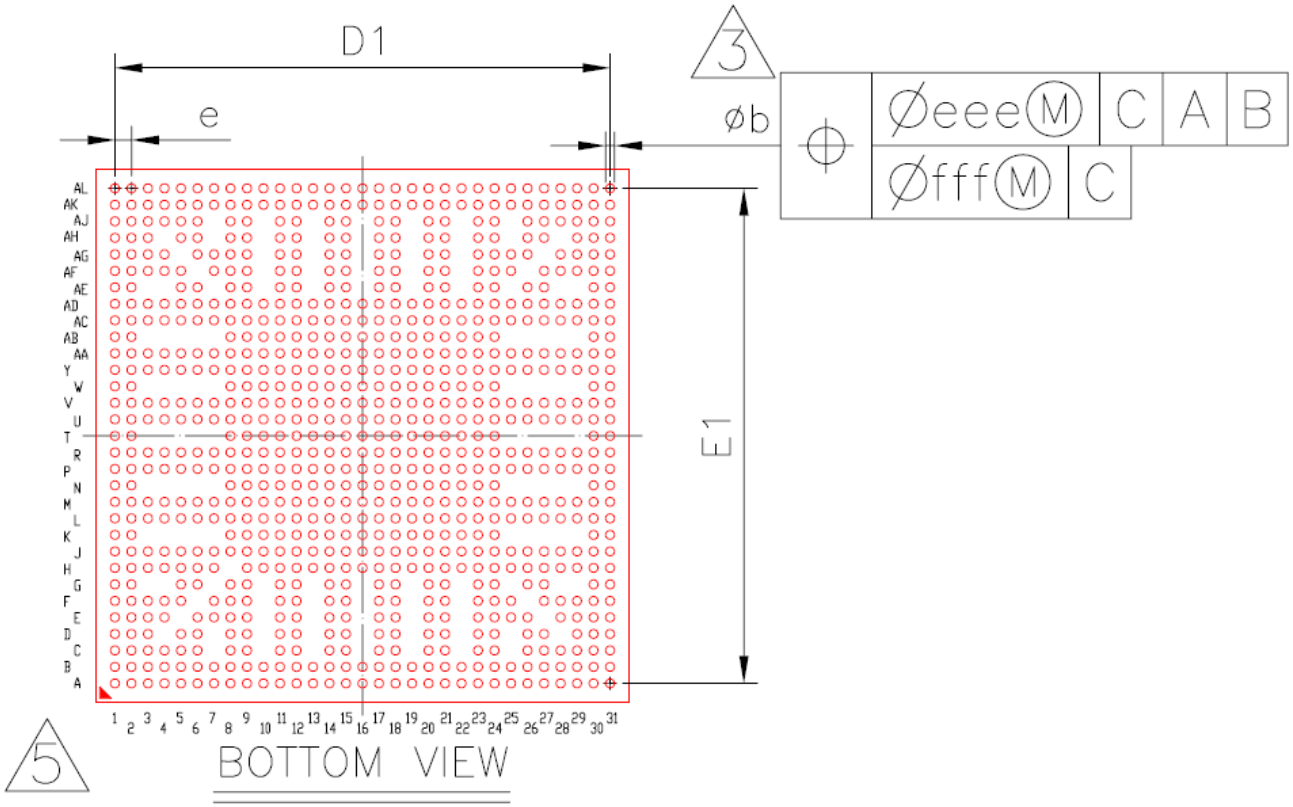


Fig. 2-3 Package Bottom View

| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | MIN | NORMAL | MAX | MIN | NORMAL | MAX |
| A | 1.41 | 1.51 | 1.61 | 0.056 | 0.059 | 0.063 |
| A1 | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| A2 | 1.11 | 1.26 | 1.41 | 0.044 | 0.050 | 0.056 |
| C | 0.47 | 0.57 | 0.67 | 0.019 | 0.022 | 0.026 |
| D | 20.90 | 21.00 | 21.15 | 0.823 | 0.827 | 0.833 |
| E | 20.90 | 21.00 | 21.15 | 0.823 | 0.827 | 0.833 |
| D1 | --- | 19.50 | --- | --- | 0.768 | --- |
| E1 | --- | 19.50 | --- | --- | 0.768 | --- |
| e | --- | 0.65 | --- | --- | 0.026 | --- |
| b | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| aaa | 0.20 | | | 0.008 | | |
| ccc | 0.25 | | | 0.010 | | |
| ddd | 0.20 | | | 0.008 | | |
| eee | 0.25 | | | 0.010 | | |
| fff | 0.10 | | | 0.004 | | |

Fig. 2-4 Package Dimension

*Notes :*

*1) Controlling dimension: millimeter*
*2) Primary datum C and seating plane are defined by the spherical crowns of the solder balls.*
*3) Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.*
*4) Special characteristics C class: A, ddd*
*5) The pattern of pin 1 fiducial is for reference only.*
6) *The tilt of heat sink should be within 10mil(0.254mm) (vertical position)*

## 2.4 Ball Map

Fig. 2-5 Ball Mapping Diagram

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| A | VSS_1 | DDR1_CSN1 | DDR1_A12 | DDR1_A10 | DDR1_CKE0 | DDR1_A9 | DDR1_A7 | DDR1_A5 |
| B | DDR0_CSN1 | DDR1_BA0 | DDR1_CSN3 | DDR1_A13 | VSS_24 | DDR1_A8 | DDR1_A6 | DDR1_A4 |
| C | DDR0_A12 | DDR0_CSN3 | DDR0_BA0 | DDR1_A14 | DDR1_A11 | DDR1_RASN | NP | VSS_25 |
| D | DDR0_A10 | DDR0_A13 | DDR0_A14 | NP | VSS_38 | DDR1_BA1 | NP | DDR1_CLK0N |
| E | DDR0_CKE0 | VSS_39 | DDR0_A11 | VSS_40 | NP | DDR1_CKE1 | VSS_41 | DDR1_CLK1N |
| F | DDR0_A1 | DDR0_A0 | DDR0_RASN | DDR0_BA1 | DDR0_CKE1 | NP | DDR1_WEN | VSS_48 |
| G | DDR0_A2 | DDR0_A3 | NP | NP | VSS_53 | DDR0_WEN | NP | DDR1_A15 |

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| H | DDR0_A5 | DDR0_A4 | VSS_57 | DDR0_CLK0P | DDR0_CLK1P | DDR0_CASN | DDR0_A15 | NP |
| J | DDR0_A6 | DDR0_A7 | VSS_68 | DDR0_CLK0N | DDR0_CLK1N | VSS_69 | VSS_70 | VSS_71 |
| K | DDR0_A9 | DDR0_A8 | NP | NP | NP | NP | NP | VSS_74 |
| L | DDR0_DQ29 | DDR0_DQ31 | VSS_85 | DDR0_ODT0 | DDR0_ODT1 | VSS_86 | DDR0_RESETN | VSS_87 |
| M | DDR0_DQ27 | DDR0_DQ30 | VSS_100 | DDR0_BA2 | DDR0_CSN2 | DDR0_CSN0 | DDR0_CLK_VDD | VSS_101 |
| N | DDR0_DQ26 | DDR0_DQ28 | NP | NP | NP | NP | NP | VSS_105 |
| P | DDR0_DQ24 | DDR0_DQ25 | VSS_112 | DDR0_DQS3P | DDR0_DM3 | VSS_113 | VSS_114 | VSS_115 |
| R | DDR0_DQ23 | DDR0_DQ22 | VSS_123 | DDR0_DQS3N | VSS_124 | VSS_125 | DDR0_PZQ | DDR0PLL_AVDD_0V9 |

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| T | DDR0_DQ20 | DDR0_DQ21 | NP | NP | NP | NP | NP | VSS_134 |
| U | DDR0_DQ18 | DDR0_DQ19 | VSS_141 | DDR0_DQS2P | DDR0_DM2 | DDR0_ATB0 | DDR0_ATB1 | VSS_142 |
| V | DDR0_DQ16 | DDR0_DQ17 | VSS_151 | DDR0_DQS2N | VSS_152 | DDR0_PLL_TESTOUT_P | DDR0_PLL_TESTOUT_N | VSS_153 |
| W | DDR0_DQ6 | DDR0_DQ7 | NP | NP | NP | NP | NP | VSS_161 |
| Y | DDR0_DQ5 | DDR0_DQ4 | VSS_8 | DDR0_DQS0P | DDR0_DM0 | GPIO4_A2/I2C1_SCL | GPIO3_D3/I2S0_SDI0 | APIO5_VDD |
| AA | DDR0_DQ3 | DDR0_DQ2 | VSS_4 | DDR0_DQS0N | VSS_5 | GPIO3_D5/I2S0_SDI2SDO2 | GPIO4_A4/I2S1_LRCK_RX | APIO5_VDDPST |
| AB | DDR0_DQ1 | DDR0_DQ0 | NP | NP | NP | NP | NP | APIO3_VDD_1V8 |
| AC | DDR0_DQ14 | DDR0_DQ15 | VSS_16 | DDR0_DQS1P | DDR0_DM1 | GPIO4_A7/I2S1_SDO0 | GPIO4_A0/I2S_CLK | APIO4_VDDPST |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| AD | DDR0_DQ13 | DDR0_DQ11 | VSS_17 | DDR0_DQS1N | VSS_18 | GPIO4_A6/I2S1_SDI0 | GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG | GPIO2_C4/SDIO0_D0/SPI5_RXD |
| AE | DDR0_DQ12 | DDR0_DQ9 | NP | NP | GPIO3_D4/I2S0_SDI1SDO3 | GPIO4_D0/PCIE_CLKREQNB | NP | GPIO2_C7/SDIO0_D3/SPI5_CSN0 |
| AF | DDR0_DQ10 | DDR0_DQ8 | GPIO4_A3/I2S1_SCLK | GPIO3_D1/I2S0_LRCK_RX | GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM | NP | GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1 | GPIO2_D4/SDIO0_BKPWR |
| AG | GPIO4_A1/I2C1_SDA | VSS_21 | GPIO3_D0/I2S0_SCLK | GPIO4_D6 | NP | GPIO4_C0/I2C3_SDA/UART2B_RX | GPIO2_C6/SDIO0_D2/SPI5_CLK | GPIO2_C2/UART0_CTSN |
| AH | GPIO3_D7/I2S0_SDO0 | GPIO3_D6/I2S0_SDI3SDO1 | GPIO4_D2 | NP | GPIO4_D4 | GPIO2_D0/SDIO0_CMD | NP | GPIO2_C1/UART0_TX |
| AJ | GPIO4_A5/I2S1_LRCK_TX | GPIO3_D2/I2S0_LRCK_TX | GPIO4_D5 | GPIO4_C4/UART2C_TX | VSS_22 | AVSS_31 | NP | AVSS_32 |
| AK | GPIO4_C5/SPDIF_TX | GPIO4_C3/UART2C_RX | GPIO4_D3 | GPIO4_D1/DP_HOTPLUG | GPIO2_C5/SDIO0_D1/SPI5_TXD | MIPI_TX1/RX1_D0P | MIPI_TX1/RX1_D1P | MIPI_TX1/RX1_CLKP |
| AL | VSS_23 | GPIO4_C1/I2C3_SCL/UART2B_TX | GPIO4_C6/PWM1 | GPIO2_D2/SDIO0_DETN/PCIE_CLKREQN | GPIO2_C3/UART0_RTSN | MIPI_TX1/RX1_D0N | MIPI_TX1/RX1_D1N | MIPI_TX1/RX1_CLKN |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |

| | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|
| A | DDR1_A3 | DDR1_A1 | DDR1_DQ10 | DDR1_DQ12 | DDR1_DQ13 | DDR1_DQ14 | DDR1_DQ1 | DDR1_DQ3 |
| B | DDR1_A2 | DDR1_A0 | DDR1_DQ8 | DDR1_DQ9 | DDR1_DQ11 | DDR1_DQ15 | DDR1_DQ0 | DDR1_DQ2 |
| C | VSS_26 | NP | VSS_27 | VSS_28 | NP | VSS_29 | VSS_30 | NP |
| D | DDR1_CLK0P | NP | DDR1_ODT0 | DDR1_BA2 | NP | DDR1_DQS1N | DDR1_DQS1P | NP |
| E | DDR1_CLK1P | NP | DDR1_ODT1 | VSS_42 | NP | DDR1_DM1 | VSS_43 | NP |
| F | DDR1_CASN | NP | DDR1_CSN2 | DDR1_CSN0 | NP | DDR1_PLL_TESTOUT_P | VSS_49 | NP |
| G | VSS_54 | NP | DDR1_RESETN | DDR1_CLK_VDD | NP | DDR1_PLL_TESTOUT_N | DDR1_PZQ | NP |

| 0 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|
| H | VSS_58 | VSS_59 | VSS_60 | VSS_61 | VSS_62 | DDR1PLL_AVDD_0V9 | VSS_63 | VSS_64 |
| J | VSS_72 | VSS_73 | DDR1_VDD_1 | DDR1_VDD_2 | DDR1_VDD_3 | DDR1_VDD_4 | DDR1_VDD_5 | DDR1_VDD_6 |
| K | VSS_75 | VSS_76 | DDR1_VDD_9 | VSS_77 | DDR1_VDD_10 | VSS_78 | DDR1_VDD_11 | VSS_79 |
| L | DDR0_VDD_1 | DDR0_VDD_2 | VSS_88 | VSS_89 | VSS_90 | VSS_91 | VSS_92 | VSS_93 |
| M | DDR0_VDD_3 | VSS_102 | CENTERLOGIC_VDD_1 | CENTERLOGIC_VDD_2 | CENTERLOGIC_VDD_3 | CENTERLOGIC_VDD_4 | CENTERLOGIC_VDD_5 | VSS_103 |
| N | DDR0_VDD_4 | DDR0_VDD_5 | CENTERLOGIC_VDD_6 | CENTERLOGIC_VDD_7 | VSS_108 | VSS_109 | VSS_110 | VSS_111 |
| P | DDR0_VDD_6 | VSS_116 | VSS_106 | VSS_107 | CENTERLOGIC_VDD_8 | CENTERLOGIC_VDD_9 | CENTERLOGIC_VDD_10 | VSS_117 |
| R | DDR0_VDD_7 | DDR0_VDD_8 | GPU_VDD_8 | GPU_VDD_9 | GPU_VDD_13 | VSS_129 | VSS_130 | VSS_131 |

| 0 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|
| T | DDR0_VDD_9 | VSS_135 | GPU_VDD_10 | GPU_VDD_11 | GPU_VDD_12 | GPU_VDD_14 | GPU_VDD_COM | VSS_138 |
| U | DDR0_VDD_10 | DDR0_VDD_11 | VSS_126 | VSS_127 | GPU_VDD_7 | VSS_137 | VSS_143 | VSS_144 |
| V | DDR0_VDD_12 | VSS_154 | GPU_VDD_15 | GPU_VDD_16 | GPU_VDD_6 | GPU_VDD_5 | GPU_VDD_4 | GPU_VDD_17 |
| W | VSS_162 | GPU_VDD_20 | GPU_VDD_1 | GPU_VDD_2 | VSS_128 | GPU_VDD_3 | GPU_VDD_19 | GPU_VDD_18 |
| Y | VSS_166 | VSS_15 | VSS_155 | VSS_136 | VSS_164 | VSS_156 | VSS_157 | VSS_118 |
| AA | VSS_6 | VSS_179 | AVSS_13 | AVSS_17 | VSS_177 | AVSS_26 | AVSS_53 | HDMI_AVDD_0V9_1 |
| AB | VSS_9 | AVSS_12 | AVSS_8 | MIPI_TX0_AVDD_1V8 | AVSS_9 | MIPI_RX0_AVDD_1V8 | AVSS_42 | AVSS_41 |
| AC | APIO4_VDD | MIPI_TX1/RX1_AVDD_1V8 | AVSS_44 | NC_7 | AVSS_45 | NC_4 | AVSS_10 | AVSS_18 |

| AD | GPIO2_D3/SDIO0_PWREN | VSS_19 | NC_2 | NC_3 | AVSS_11 | NC_5 | NC_6 | HDMI_AVDD_1V8 |
|---|---|---|---|---|---|---|---|---|
| AE | GPIO2_C0/UART0_RX | NP | AVSS_21 | AVSS_22 | NP | AVSS_23 | HDMI_HPD | NP |
| AF | VSS_20 | NP | MIPI_TX1/RX1_REXT | MIPI_TX0_REXT | NP | MIPI_RX0_REXT | HDMI_REXT | NP |
| AG | MIPI_TX0_D3P | NP | MIPI_TX0_D2P | MIPI_TX0_CLKP | NP | MIPI_TX0_D1P | MIPI_TX0_D0P | NP |
| AH | MIPI_TX0_D3N | NP | MIPI_TX0_D2N | MIPI_TX0_CLKN | NP | MIPI_TX0_D1N | MIPI_TX0_D0N | NP |
| AJ | AVSS_33 | NP | AVSS_34 | AVSS_35 | NP | AVSS_36 | AVSS_37 | NP |
| AK | MIPI_TX1/RX1_D2P | MIPI_TX1/RX1_D3P | MIPI_RX0_D3P | MIPI_RX0_D2P | MIPI_RX0_CLKP | MIPI_RX0_D1P | MIPI_RX0_D0P | HDMI_TCP |
| AL | MIPI_TX1/RX1_D2N | MIPI_TX1/RX1_D3N | MIPI_RX0_D3N | MIPI_RX0_D2N | MIPI_RX0_CLKN | MIPI_RX0_D1N | MIPI_RX0_D0N | HDMI_TCN |
| | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |

| 0 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|
| A | DDR1_DQ5 | DDR1_DQ6 | DDR1_DQ16 | DDR1_DQ18 | DDR1_DQ20 | DDR1_DQ23 | DDR1_DQ24 | DDR1_DQ26 |
| B | DDR1_DQ4 | DDR1_DQ7 | DDR1_DQ17 | DDR1_DQ19 | DDR1_DQ21 | DDR1_DQ22 | DDR1_DQ25 | DDR1_DQ28 |
| C | VSS_31 | VSS_32 | NP | VSS_33 | VSS_34 | NP | VSS_35 | VSS_36 |
| D | DDR1_DQS0N | DDR1_DQS0P | NP | DDR1_DQS2N | DDR1_DQS2P | NP | DDR1_DQS3N | DDR1_DQS3P |
| E | DDR1_DM0 | VSS_44 | NP | DDR1_DM2 | VSS_45 | NP | DDR1_DM3 | VSS_46 |
| F | DDR1_ATB0 | VSS_50 | NP | VSS_51 | VSS_52 | NP | GPIO3_B2/MAC_RXER/I2C5_SDA | GPIO3_A0/MAC_TXD2/SPI4_RXD |
| G | DDR1_ATB1 | VSS_55 | NP | EDP_DC_TP | EDP_REXT | NP | GPIO3_A5/MAC_TXD1/SPI0_TXD | GPIO3_B3/MAC_CLK/I2C5_SCL |

| 828 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|
| H | VSS_65 | VSS_66 | EDP_AVSS_5 | EDP_AVDD_0V9 | EDP_CLK24M_IN | GPIO3_B4/MAC_TXEN/UART1_RX | GPIO3_A1/MAC_TXD3/SPI4_TXD | GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL |
| J | DDR1_VDD_7 | DDR1_VDD_8 | EDP_AVDD_1V8_1 | EDP_AVDD_1V8_2 | EDP_AVSS_6 | APIO1_VDDPST | APIO1_VDD | APIO2_VDDPST |
| K | DDR1_VDD_12 | VSS_80 | BIGCPU_VDD_12 | VSS_82 | BIGCPU_VDD_13 | VSS_84 | APIO2_VDD | EMMC_VDD_1V8 |
| L | LOGIC_VDD_10 | BIGCPU_VDD_8 | BIGCPU_VDD_1 | VSS_96 | BIGCPU_VDD_2 | VSS_97 | BIGCPU_VDD_11 | EMMC_COREDLL_0V9 |
| M | LOGIC_VDD_9 | BIGCPU_VDD_3 | BIGCPU_VDD_4 | BIGCPU_VDD_5 | BIGCPU_VDD_6 | BIGCPU_VDD_7 | VSS_104 | GPIO1_B5 |
| N | VSS_94 | BIGCPU_VDD_COM | VSS_83 | BIGCPU_VDD_10 | VSS_98 | BIGCPU_VDD_9 | PMUIO2_VDDPST | GPIO0_A2/WIFI_26MHZ |
| P | PLL_AVSS | PLL_AVDD_1V8 | VSS_119 | LITCPU_VDD_1 | VSS_121 | LITCPU_VDD_4 | PMUIO2_VDD | GPIO0_B5/TCPD_VBUS_FDIS/TCPD_VBUS_SOURCE3 |
| R | PLL_AVDD_0V9 | VSS_165 | LITCPU_VDD_2 | LITCPU_VDD_3 | VSS_120 | LITCPU_VDD_7 | VSS_133 | PMUIO1_VDD_1V8 |

| 0 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|
| T | LOGIC_VDD_11 | VSS_168 | VSS_122 | LITCPU_VDD_6 | VSS_139 | LITCPU_VDD_5 | SDMMC0_VDD | PMU_VDD_0V9 |
| U | LOGIC_VDD_8 | LOGIC_VDD_7 | VSS_146 | LOGIC_VDD_12 | VSS_147 | VSS_149 | AVSS_49 | USB_AVDD_1V8 |
| V | VSS_148 | LOGIC_VDD_5 | LOGIC_VDD_4 | LOGIC_VDD_3 | LOGIC_VDD_2 | LOGIC_VDD_1 | AVSS_50 | USB_AVDD_0V9 |
| W | VSS_159 | VSS_169 | VSS_167 | LOGIC_VDD_6 | VSS_81 | VSS_158 | AVSS_46 | PCIE_AVDD_0V9 |
| Y | VSS_95 | TYPEC0_AVDD_0V9_2 | TYPEC0_AVDD_0V9_1 | VSS_170 | TYPEC1_AVDD_0V9_1 | TYPEC1_AVDD_0V9_2 | AVSS_1 | PCIE_AVDD_1V8 |
| AA | HDMI_AVDD_0V9_2 | TYPEC0_AVDD_1V8 | NC_8 | NC_9 | TYPEC1_AVDD_1V8 | NC_11 | AVSS_4 | DFTJTAG_TMS |
| AB | AVSS_52 | TYPEC0_AVDD_3V3 | VSS_140 | NC_10 | TYPEC1_AVDD_3V3 | NC_1 | AVSS_5 | DFTJTAG_TRSTN |
| AC | AVSS_43 | VSS_145 | TYPEC1_U3VBUSDET | VSS_13 | VSS_132 | VSS_12 | AVSS_19 | ADC_AVDD |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| AD | AVSS_16 | TYPEC0_RCLKM | TYPEC0_U3VBUSDET | TYPEC1_RCLKM | VSS_163 | VSS_11 | EFUSE | USIC_AVDD_1V2 |
| AE | AVSS_24 | TYPEC0_RCLKP | NP | TYPEC1_RCLKP | TYPEC1_REXT | NP | VSS_14 | TYPEC1_AUXP_PD_PU |
| AF | AVSS_27 | VSS_7 | NP | VSS_10 | TYPEC1_CC2 | NP | AVSS_2 | AVSS_3 |
| AG | TYPEC0_AUXM_PU_PD | TYPEC0_REXT | NP | TYPEC0_REXT_CC | TYPEC1_REXT_CC | NP | TYPEC0_DP | TYPEC1_DP |
| AH | TYPEC0_AUXP_PD_PU | TYPEC0_CC1 | NP | TYPEC0_CC2 | TYPEC1_CC1 | NP | TYPEC0_DN | TYPEC1_DN |
| AJ | AVSS_38 | AVSS_39 | NP | VSS_180 | VSS_172 | NP | VSS_173 | VSS_174 |
| AK | HDMI_TX0P | HDMI_TX1P | HDMI_TX2P | TYPEC0_AUXP | TYPEC0_RX1P | TYPEC0_TX1M | TYPEC0_RX2P | TYPEC0_TX2M |
| AL | HDMI_TX0N | HDMI_TX1N | HDMI_TX2N | TYPEC0_AUXM | TYPEC0_RX1M | TYPEC0_TX1P | TYPEC0_RX2M | TYPEC0_TX2P |
| | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |

| 25 | 26 | 27 | 28 | 29 | 30 | 31 | 0 |
|---|---|---|---|---|---|---|---|
| DDR1_DQ27 | DDR1_DQ29 | VSS_2 | EDP_AUXN | EDP_TX0N | EDP_TX1N | VSS_3 | A |
| DDR1_DQ30 | DDR1_DQ31 | GPIO3_B7/MAC_CRS/UART3_TX/CIF_CLKOUTB | EDP_AUXP | EDP_TX0P | EDP_TX1P | EDP_AVSS_1 | B |
| NP | VSS_37 | GPIO3_B1/MAC_RXDV | EDP_AVSS_2 | EDP_AVSS_3 | EDP_TX2P | EDP_TX2N | C |
| NP | GPIO3_A4/MAC_TXD0/SPI0_RXD | GPIO3_C0/MAC_COL/UART3_CTSN/SPDIF_TX | NP | EDP_AVSS_4 | EDP_TX3P | EDP_TX3N | D |
| GPIO3_A3/MAC_RXD3/SPI4_CSN0 | GPIO3_A6/MAC_RXD0/SPI0_CLK | NP | GPIO3_C1/MAC_TXCLK/UART3_RTSN | GPIO3_B0/MAC_MDC/SPI0_CSN1 | GPIO3_A2/MAC_RXD2/SPI4_CLK | VSS_47 | E |
| GPIO3_B6/MAC_RXCLK/UART3_RX | NP | GPIO3_A7/MAC_RXD1/SPI0_CSN0 | GPIO2_A3/VOP_D3/CIF_D3 | GPIO2_A5/VOP_D5/CIF_D5 | GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA | GPIO2_B4/SPI2_CSN0 | F |
| NP | GPIO3_B5/MAC_MDIO/UART1_TX | VSS_56 | NP | NP | GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA | GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA | G |

| 25 | 26 | 27 | 28 | 29 | 30 | 31 | 0 |
|---|---|---|---|---|---|---|---|
| GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL | VSS_67 | GPIO2_A6/VOP_D6/CIF_D6 | GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL | GPIO2_A4/VOP_D4/CIF_D4 | GPIO2_A2/VOP_D2/CIF_D2 | GPIO2_B3/SPI2_CLK/VOP_DEN/CIF_CLKOUTA | H |
| EMMC_D3 | EMMC_D4 | EMMC_D5 | EMMC_D0 | EMMC_D1 | EMMC_D2 | EMMC_CMD | J |
| NP | NP | NP | NP | NP | EMMC_D7 | EMMC_STRB | K |
| GPIO1_C6/TCPD_VBUS_SOURCE0 | GPIO1_D0/TCPD_VBUS_SOURCE2 | VSS_99 | EMMC_CLK | EMMC_CALIO | EMMC_TP | EMMC_D6 | L |
| GPIO1_B6/PWM3B_IR | GPIO1_B7/SPI3_RXD/I2C0_SDA | GPIO1_C1/SPI3_CLK | GPIO1_C3/PWM2 | GPIO1_C4/I2C8_SDA | GPIO1_C5/I2C8_SCL | GPIO1_C7/TCPD_VBUS_SOURCE1 | M |
| NP | NP | NP | NP | NP | GPIO1_C0/SPI3_TXD/I2C0_SCL | GPIO1_C2/SPI3_CSN0 | N |
| GPIO0_A6/PWM3A_IR | GPIO1_A6/TSADC_INT | GPIO1_A7/SPI1_RXD/UART4_RX | GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK | GPIO1_B2/SPI1_CSN0/PMCU_JTAG_TMS | GPIO1_B4/I2C4_SCL | GPIO1_B3/I2C4_SDA | P |
| GPIO1_A0/ISP0_SHUTTER_EN/ISP1_SHUTTER_EN/TCPD_VBUS_SINK_EN | GPIO1_A2/ISP0_FLASHTRIGIN/ISP1_FLASHTRIGIN/TCPD_CC1_VCONN_EN | GPIO1_A3/ISP0_FLASHTRIGOUT/ISP1_FLASHTRIGOUT | GPIO1_A4/ISP0_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG | GPIO0_A1/DDRIO_PWROFF/TCPD_CCDB_EN | GPIO1_A5/AP_PWROFF | GPIO1_B0/SPI1_TXD/UART4_TX | R |

| 25 | 26 | 27 | 28 | 29 | 30 | 31 | 0 |
|---|---|---|---|---|---|---|---|
| NP | NP | NP | NP | NP | NPOR | GPIO1_A1/ISP0_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_CC0_VCONN_EN | T |
| PMU_VDD_1V8 | SDMMC0_VDDPST | GPIO4_B3/SDMMC0_D3/APJTAG_TMS | GPIO0_B0/SDMMC0_WRPT/TEST_CLKOUT2 | VSS_150 | GPIO0_B3 | GPIO0_A0/TEST_CLKOUT0/CLK32K_IN | U |
| GPIO4_B5/SDMMC0_CMD/MCUJTAG_TMS | GPIO0_B4/TCPD_VBUS_BDIS | GPIO0_A5/EMMC_PWRON | GPIO0_A7/SDMMC0_DET | GPIO4_B4/SDMMC0_CLKOUT/MUCJTAG_TCK | GPIO0_B1/PMUIO2_VOLSEL | GPIO0_A3/SDIO0_WRPT | V |
| NP | NP | NP | NP | NP | VSS_160 | GPIO0_B2 | W |
| USB_AVDD_3V3 | GPIO4_B1/SDMMC0_D1/UART2A_TX | GPIO4_B0/SDMMC0_D0/UART2A_RX | GPIO4_B2/SDMMC0_D2/APJTAG_TCK | AVSS_48 | XOUT_OSC | XIN_OSC | Y |
| GPIO0_A4/SDIO0_INTN | AVSS_6 | PCIE_TX2_P | PCIE_TX2_N | AVSS_7 | USB1_DP | USB1_DN | AA |
| NP | NP | NP | NP | NP | USB0_DP | USB0_DN | AB |
| AVSS_51 | AVSS_14 | PCIE_RX2_P | PCIE_RX2_N | AVSS_15 | USB1_RBIAS | USB0_RBIAS | AC |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| USIC_AVDD_0V9 | AVSS_40 | PCIE_TX3_P | PCIE_TX3_N | AVSS_20 | PCIE_RCLK_100M_N | PCIE_RCLK_100M_P | AD |
| NP | TYPEC1_ID | AVSS_25 | NP | NP | PCIE_TX0_P | PCIE_TX0_N | AE |
| TYPEC1_AUXM_PU_PD | NP | PCIE_RX3_P | PCIE_RX3_N | AVSS_28 | PCIE_RX0_P | PCIE_RX0_N | AF |
| ADC_IN2 | ADC_IN0 | NP | ADC_IN3 | AVSS_29 | PCIE_TX1_P | PCIE_TX1_N | AG |
| NP | ADC_IN1 | ADC_IN4 | NP | AVSS_30 | PCIE_RX1_P | PCIE_RX1_N | AH |
| NP | VSS_175 | VSS_176 | VSS_171 | AVSS_47 | USIC_STROBE | USIC_DATA | AJ |
| TYPEC1_RX1P | TYPEC1_TX1M | TYPEC1_RX2P | TYPEC1_TX2M | TYPEC1_AUXP | TYPEC0_U2VBUSDET | TYPEC1_U2VBUSDET | AK |
| TYPEC1_RX1M | TYPEC1_TX1P | TYPEC1_RX2M | TYPEC1_TX2P | TYPEC1_AUXM | TYPEC0_ID | VSS_178 | AL |
| 25 | 26 | 27 | 28 | 29 | 30 | 31 | |

## 2.5 Ball Pin Number Order

Table 2-1 Ball Pin Number Order Information

| PIN# | PIN name | PIN# | PIN name |
|---|---|---|---|
| A1 | VSS_1 | E23 | DDR1_DM3 |
| A2 | DDR1_CSN1 | E24 | VSS_46 |
| A3 | DDR1_A12 | E25 | GPIO3_A3/MAC_RXD3/SPI4_CSN0 |
| A4 | DDR1_A10 | E26 | GPIO3_A6/MAC_RXD0/SPI0_CLK |
| A5 | DDR1_CKE0 | E28 | GPIO3_C1/MAC_TXCLK/UART3_RTSN |
| A6 | DDR1_A9 | E29 | GPIO3_B0/MAC_MDC/SPI0_CSN1 |
| A7 | DDR1_A7 | E30 | GPIO3_A2/MAC_RXD2/SPI4_CLK |
| A8 | DDR1_A5 | E31 | VSS_47 |
| A9 | DDR1_A3 | F1 | DDR0_A1 |
| A10 | DDR1_A1 | F2 | DDR0_A0 |
| A11 | DDR1_DQ10 | F3 | DDR0_RASN |
| A12 | DDR1_DQ12 | F4 | DDR0_BA1 |
| A13 | DDR1_DQ13 | F5 | DDR0_CKE1 |
| A14 | DDR1_DQ14 | F7 | DDR1_WEN |
| A15 | DDR1_DQ1 | F8 | VSS_48 |
| A16 | DDR1_DQ3 | F9 | DDR1_CASN |
| A17 | DDR1_DQ5 | F11 | DDR1_CSN2 |
| A18 | DDR1_DQ6 | F12 | DDR1_CSN0 |
| A19 | DDR1_DQ16 | F14 | DDR1_PLL_TESTOUT_P |
| A20 | DDR1_DQ18 | F15 | VSS_49 |
| A21 | DDR1_DQ20 | F17 | DDR1_ATB0 |
| A22 | DDR1_DQ23 | F18 | VSS_50 |
| A23 | DDR1_DQ24 | F20 | VSS_51 |
| A24 | DDR1_DQ26 | F21 | VSS_52 |
| A25 | DDR1_DQ27 | F23 | GPIO3_B2/MAC_RXER/I2C5_SDA |
| A26 | DDR1_DQ29 | F24 | GPIO3_A0/MAC_TXD2/SPI4_RXD |
| A27 | VSS_2 | F25 | GPIO3_B6/MAC_RXCLK/UART3_RX |
| A28 | EDP_AUXN | F27 | GPIO3_A7/MAC_RXD1/SPI0_CSN0 |
| A29 | EDP_TX0N | F28 | GPIO2_A3/VOP_D3/CIF_D3 |
| A30 | EDP_TX1N | F29 | GPIO2_A5/VOP_D5/CIF_D5 |
| A31 | VSS_3 | F30 | GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA |
| AA1 | DDR0_DQ3 | F31 | GPIO2_B4/SPI2_CSN0 |
| AA2 | DDR0_DQ2 | G1 | DDR0_A2 |
| AA3 | VSS_4 | G2 | DDR0_A3 |
| AA4 | DDR0_DQS0N | G5 | VSS_53 |
| AA5 | VSS_5 | G6 | DDR0_WEN |
| AA6 | GPIO3_D5/I2S0_SDI2SDO2 | G8 | DDR1_A15 |
| AA7 | GPIO4_A4/I2S1_LRCK_RX | G9 | VSS_54 |
| AA8 | APIO5_VDDPST | G11 | DDR1_RESETN |
| AA9 | VSS_6 | G12 | DDR1_CLK_VDD |
| AA10 | VSS_179 | G14 | DDR1_PLL_TESTOUT_N |
| AA11 | AVSS_13 | G15 | DDR1_PZQ |

| PIN# | PIN name | PIN# | PIN name |
|---|---|---|---|
| AA12 | AVSS_17 | G17 | DDR1_ATB1 |
| AA13 | VSS_177 | G18 | VSS_55 |
| AA14 | AVSS_26 | G20 | EDP_DC_TP |
| AA15 | AVSS_53 | G21 | EDP_REXT |
| AA16 | HDMI_AVDD_0V9_1 | G23 | GPIO3_A5/MAC_TXD1/SPI0_TXD |
| AA17 | HDMI_AVDD_0V9_2 | G24 | GPIO3_B3/MAC_CLK/I2C5_SCL |
| AA18 | TYPEC0_AVDD_1V8 | G26 | GPIO3_B5/MAC_MDIO/UART1_TX |
| AA19 | NC_8 | G27 | VSS_56 |
| AA20 | NC_9 | G30 | GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA |
| AA21 | TYPEC1_AVDD_1V8 | G31 | GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA |
| AA22 | NC_11 | H1 | DDR0_A5 |
| AA23 | AVSS_4 | H2 | DDR0_A4 |
| AA24 | DFTJTAG_TMS | H3 | VSS_57 |
| AA25 | GPIO0_A4/SDIO0_INTN | H4 | DDR0_CLK0P |
| AA26 | AVSS_6 | H5 | DDR0_CLK1P |
| AA27 | PCIE_TX2_P | H6 | DDR0_CASN |
| AA28 | PCIE_TX2_N | H7 | DDR0_A15 |
| AA29 | AVSS_7 | H9 | VSS_58 |
| AA30 | USB1_DP | H10 | VSS_59 |
| AA31 | USB1_DN | H11 | VSS_60 |
| AB1 | DDR0_DQ1 | H12 | VSS_61 |
| AB2 | DDR0_DQ0 | H13 | VSS_62 |
| AB8 | APIO3_VDD_1V8 | H14 | DDR1PLL_AVDD_0V9 |
| AB9 | VSS_9 | H15 | VSS_63 |
| AB10 | AVSS_12 | H16 | VSS_64 |
| AB11 | AVSS_8 | H17 | VSS_65 |
| AB12 | MIPI_TX0_AVDD_1V8 | H18 | VSS_66 |
| AB13 | AVSS_9 | H19 | EDP_AVSS_5 |
| AB14 | MIPI_RX0_AVDD_1V8 | H20 | EDP_AVDD_0V9 |
| AB15 | AVSS_42 | H21 | EDP_CLK24M_IN |
| AB16 | AVSS_41 | H22 | GPIO3_B4/MAC_TXEN/UART1_RX |
| AB17 | AVSS_52 | H23 | GPIO3_A1/MAC_TXD3/SPI4_TXD |
| AB18 | TYPEC0_AVDD_3V3 | H24 | GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL |
| AB19 | VSS_140 | H25 | GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL |
| AB20 | NC_10 | H26 | VSS_67 |
| AB21 | TYPEC1_AVDD_3V3 | H27 | GPIO2_A6/VOP_D6/CIF_D6 |
| AB22 | NC_1 | H28 | GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL |
| AB23 | AVSS_5 | H29 | GPIO2_A4/VOP_D4/CIF_D4 |
| AB24 | DFTJTAG_TRSTN | H30 | GPIO2_A2/VOP_D2/CIF_D2 |
| AB30 | USB0_DP | H31 | GPIO2_B3/SPI2_CLK/VOP_DEN/CIF_CLKOUTA |
| AB31 | USB0_DN | J1 | DDR0_A6 |
| AC1 | DDR0_DQ14 | J2 | DDR0_A7 |
| AC2 | DDR0_DQ15 | J3 | VSS_68 |

| PIN# | PIN name | PIN# | PIN name |
|---|---|---|---|
| AC3 | VSS_16 | J4 | DDR0_CLK0N |
| AC4 | DDR0_DQS1P | J5 | DDR0_CLK1N |
| AC5 | DDR0_DM1 | J6 | VSS_69 |
| AC6 | GPIO4_A7/I2S1_SDO0 | J7 | VSS_70 |
| AC7 | GPIO4_A0/I2S_CLK | J8 | VSS_71 |
| AC8 | APIO4_VDDPST | J9 | VSS_72 |
| AC9 | APIO4_VDD | J10 | VSS_73 |
| AC10 | MIPI_TX1/RX1_AVDD_1V8 | J11 | DDR1_VDD_1 |
| AC11 | AVSS_44 | J12 | DDR1_VDD_2 |
| AC12 | NC_7 | J13 | DDR1_VDD_3 |
| AC13 | AVSS_45 | J14 | DDR1_VDD_4 |
| AC14 | NC_4 | J15 | DDR1_VDD_5 |
| AC15 | AVSS_10 | J16 | DDR1_VDD_6 |
| AC16 | AVSS_18 | J17 | DDR1_VDD_7 |
| AC17 | AVSS_43 | J18 | DDR1_VDD_8 |
| AC18 | VSS_145 | J19 | EDP_AVDD_1V8_1 |
| AC19 | TYPEC1_U3VBUSDET | J20 | EDP_AVDD_1V8_2 |
| AC20 | VSS_13 | J21 | EDP_AVSS_6 |
| AC21 | VSS_132 | J22 | APIO1_VDDPST |
| AC22 | VSS_12 | J23 | APIO1_VDD |
| AC23 | AVSS_19 | J24 | APIO2_VDDPST |
| AC24 | ADC_AVDD | J25 | EMMC_D3 |
| AC25 | AVSS_51 | J26 | EMMC_D4 |
| AC26 | AVSS_14 | J27 | EMMC_D5 |
| AC27 | PCIE_RX2_P | J28 | EMMC_D0 |
| AC28 | PCIE_RX2_N | J29 | EMMC_D1 |
| AC29 | AVSS_15 | J30 | EMMC_D2 |
| AC30 | USB1_RBIAS | J31 | EMMC_CMD |
| AC31 | USB0_RBIAS | K1 | DDR0_A9 |
| AD1 | DDR0_DQ13 | K2 | DDR0_A8 |
| AD2 | DDR0_DQ11 | K8 | VSS_74 |
| AD3 | VSS_17 | K9 | VSS_75 |
| AD4 | DDR0_DQS1N | K10 | VSS_76 |
| AD5 | VSS_18 | K11 | DDR1_VDD_9 |
| AD6 | GPIO4_A6/I2S1_SDI0 | K12 | VSS_77 |
| AD7 | GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG | K13 | DDR1_VDD_10 |
| AD8 | GPIO2_C4/SDIO0_D0/SPI5_RXD | K14 | VSS_78 |
| AD9 | GPIO2_D3/SDIO0_PWREN | K15 | DDR1_VDD_11 |
| AD10 | VSS_19 | K16 | VSS_79 |
| AD11 | NC_2 | K17 | DDR1_VDD_12 |
| AD12 | NC_3 | K18 | VSS_80 |
| AD13 | AVSS_11 | K19 | BIGCPU_VDD_12 |
| AD14 | NC_5 | K20 | VSS_82 |

| PIN# | PIN name | PIN# | PIN name |
|---|---|---|---|
| AD15 | NC_6 | K21 | BIGCPU_VDD_13 |
| AD16 | HDMI_AVDD_1V8 | K22 | VSS_84 |
| AD17 | AVSS_16 | K23 | APIO2_VDD |
| AD18 | TYPEC0_RCLKM | K24 | EMMC_VDD_1V8 |
| AD19 | TYPEC0_U3VBUSDET | K30 | EMMC_D7 |
| AD20 | TYPEC1_RCLKM | K31 | EMMC_STRB |
| AD21 | VSS_163 | L1 | DDR0_DQ29 |
| AD22 | VSS_11 | L2 | DDR0_DQ31 |
| AD23 | EFUSE | L3 | VSS_85 |
| AD24 | USIC_AVDD_1V2 | L4 | DDR0_ODT0 |
| AD25 | USIC_AVDD_0V9 | L5 | DDR0_ODT1 |
| AD26 | AVSS_40 | L6 | VSS_86 |
| AD27 | PCIE_TX3_P | L7 | DDR0_RESETN |
| AD28 | PCIE_TX3_N | L8 | VSS_87 |
| AD29 | AVSS_20 | L9 | DDR0_VDD_1 |
| AD30 | PCIE_RCLK_100M_N | L10 | DDR0_VDD_2 |
| AD31 | PCIE_RCLK_100M_P | L11 | VSS_88 |
| AE1 | DDR0_DQ12 | L12 | VSS_89 |
| AE2 | DDR0_DQ9 | L13 | VSS_90 |
| AE5 | GPIO3_D4/I2S0_SDI1SDO3 | L14 | VSS_91 |
| AE6 | GPIO4_D0/PCIE_CLKREQNB | L15 | VSS_92 |
| AE8 | GPIO2_C7/SDIO0_D3/SPI5_CSN0 | L16 | VSS_93 |
| AE9 | GPIO2_C0/UART0_RX | L17 | LOGIC_VDD_10 |
| AE11 | AVSS_21 | L18 | BIGCPU_VDD_8 |
| AE12 | AVSS_22 | L19 | BIGCPU_VDD_1 |
| AE14 | AVSS_23 | L20 | VSS_96 |
| AE15 | HDMI_HPD | L21 | BIGCPU_VDD_2 |
| AE17 | AVSS_24 | L22 | VSS_97 |
| AE18 | TYPEC0_RCLKP | L23 | BIGCPU_VDD_11 |
| AE20 | TYPEC1_RCLKP | L24 | EMMC_COREDLL_0V9 |
| AE21 | TYPEC1_REXT | L25 | GPIO1_C6/TCPD_VBUS_SOURCE0 |
| AE23 | VSS_14 | L26 | GPIO1_D0/TCPD_VBUS_SOURCE2 |
| AE24 | TYPEC1_AUXP_PD_PU | L27 | VSS_99 |
| AE26 | TYPEC1_ID | L28 | EMMC_CLK |
| AE27 | AVSS_25 | L29 | EMMC_CALIO |
| AE30 | PCIE_TX0_P | L30 | EMMC_TP |
| AE31 | PCIE_TX0_N | L31 | EMMC_D6 |
| AF1 | DDR0_DQ10 | M1 | DDR0_DQ27 |
| AF2 | DDR0_DQ8 | M2 | DDR0_DQ30 |
| AF3 | GPIO4_A3/I2S1_SCLK | M3 | VSS_100 |
| AF4 | GPIO3_D1/I2S0_LRCK_RX | M4 | DDR0_BA2 |
| AF5 | GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM | M5 | DDR0_CSN2 |

| PIN# | PIN name | PIN# | PIN name |
|---|---|---|---|
| AF7 | GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1 | M6 | DDR0_CSN0 |
| AF8 | GPIO2_D4/SDIO0_BKPWR | M7 | DDR0_CLK_VDD |
| AF9 | VSS_20 | M8 | VSS_101 |
| AF11 | MIPI_TX1/RX1_REXT | M9 | DDR0_VDD_3 |
| AF12 | MIPI_TX0_REXT | M10 | VSS_102 |
| AF14 | MIPI_RX0_REXT | M11 | CENTERLOGIC_VDD_1 |
| AF15 | HDMI_REXT | M12 | CENTERLOGIC_VDD_2 |
| AF17 | AVSS_27 | M13 | CENTERLOGIC_VDD_3 |
| AF18 | VSS_7 | M14 | CENTERLOGIC_VDD_4 |
| AF20 | VSS_10 | M15 | CENTERLOGIC_VDD_5 |
| AF21 | TYPEC1_CC2 | M16 | VSS_103 |
| AF23 | AVSS_2 | M17 | LOGIC_VDD_9 |
| AF24 | AVSS_3 | M18 | BIGCPU_VDD_3 |
| AF25 | TYPEC1_AUXM_PU_PD | M19 | BIGCPU_VDD_4 |
| AF27 | PCIE_RX3_P | M20 | BIGCPU_VDD_5 |
| AF28 | PCIE_RX3_N | M21 | BIGCPU_VDD_6 |
| AF29 | AVSS_28 | M22 | BIGCPU_VDD_7 |
| AF30 | PCIE_RX0_P | M23 | VSS_104 |
| AF31 | PCIE_RX0_N | M24 | GPIO1_B5 |
| AG1 | GPIO4_A1/I2C1_SDA | M25 | GPIO1_B6/PWM3B_IR |
| AG2 | VSS_21 | M26 | GPIO1_B7/SPI3_RXD/I2C0_SDA |
| AG3 | GPIO3_D0/I2S0_SCLK | M27 | GPIO1_C1/SPI3_CLK |
| AG4 | GPIO4_D6 | M28 | GPIO1_C3/PWM2 |
| AG6 | GPIO4_C0/I2C3_SDA/UART2B_RX | M29 | GPIO1_C4/I2C8_SDA |
| AG7 | GPIO2_C6/SDIO0_D2/SPI5_CLK | M30 | GPIO1_C5/I2C8_SCL |
| AG8 | GPIO2_C2/UART0_CTSN | M31 | GPIO1_C7/TCPD_VBUS_SOURCE1 |
| AG9 | MIPI_TX0_D3P | N1 | DDR0_DQ26 |
| AG11 | MIPI_TX0_D2P | N2 | DDR0_DQ28 |
| AG12 | MIPI_TX0_CLKP | N8 | VSS_105 |
| AG14 | MIPI_TX0_D1P | N9 | DDR0_VDD_4 |
| AG15 | MIPI_TX0_D0P | N10 | DDR0_VDD_5 |
| AG17 | TYPEC0_AUXM_PU_PD | N11 | CENTERLOGIC_VDD_6 |
| AG18 | TYPEC0_REXT | N12 | CENTERLOGIC_VDD_7 |
| AG20 | TYPEC0_REXT_CC | N13 | VSS_108 |
| AG21 | TYPEC1_REXT_CC | N14 | VSS_109 |
| AG23 | TYPEC0_DP | N15 | VSS_110 |
| AG24 | TYPEC1_DP | N16 | VSS_111 |
| AG25 | ADC_IN2 | N17 | VSS_94 |
| AG26 | ADC_IN0 | N18 | BIGCPU_VDD_COM |
| AG28 | ADC_IN3 | N19 | VSS_83 |
| AG29 | AVSS_29 | N20 | BIGCPU_VDD_10 |
| AG30 | PCIE_TX1_P | N21 | VSS_98 |
| AG31 | PCIE_TX1_N | N22 | BIGCPU_VDD_9 |

| PIN# | PIN name | PIN# | PIN name |
|---|---|---|---|
| AH1 | GPIO3_D7/I2S0_SDO0 | N23 | PMUIO2_VDDPST |
| AH2 | GPIO3_D6/I2S0_SDI3SDO1 | N24 | GPIO0_A2/WIFI_26MHZ |
| AH3 | GPIO4_D2 | N30 | GPIO1_C0/SPI3_TXD/I2C0_SCL |
| AH5 | GPIO4_D4 | N31 | GPIO1_C2/SPI3_CSN0 |
| AH6 | GPIO2_D0/SDIO0_CMD | P1 | DDR0_DQ24 |
| AH8 | GPIO2_C1/UART0_TX | P2 | DDR0_DQ25 |
| AH9 | MIPI_TX0_D3N | P3 | VSS_112 |
| AH11 | MIPI_TX0_D2N | P4 | DDR0_DQS3P |
| AH12 | MIPI_TX0_CLKN | P5 | DDR0_DM3 |
| AH14 | MIPI_TX0_D1N | P6 | VSS_113 |
| AH15 | MIPI_TX0_D0N | P7 | VSS_114 |
| AH17 | TYPEC0_AUXP_PD_PU | P8 | VSS_115 |
| AH18 | TYPEC0_CC1 | P9 | DDR0_VDD_6 |
| AH20 | TYPEC0_CC2 | P10 | VSS_116 |
| AH21 | TYPEC1_CC1 | P11 | VSS_106 |
| AH23 | TYPEC0_DN | P12 | VSS_107 |
| AH24 | TYPEC1_DN | P13 | CENTERLOGIC_VDD_8 |
| AH26 | ADC_IN1 | P14 | CENTERLOGIC_VDD_9 |
| AH27 | ADC_IN4 | P15 | CENTERLOGIC_VDD_10 |
| AH29 | AVSS_30 | P16 | VSS_117 |
| AH30 | PCIE_RX1_P | P17 | PLL_AVSS |
| AH31 | PCIE_RX1_N | P18 | PLL_AVDD_1V8 |
| AJ1 | GPIO4_A5/I2S1_LRCK_TX | P19 | VSS_119 |
| AJ2 | GPIO3_D2/I2S0_LRCK_TX | P20 | LITCPU_VDD_1 |
| AJ3 | GPIO4_D5 | P21 | VSS_121 |
| AJ4 | GPIO4_C4/UART2C_TX | P22 | LITCPU_VDD_4 |
| AJ5 | VSS_22 | P23 | PMUIO2_VDD |
| AJ6 | AVSS_31 | P24 | GPIO0_B5/TCPD_VBUS_FDIS/TCPD_VBUS_SOURCE3 |
| AJ8 | AVSS_32 | P25 | GPIO0_A6/PWM3A_IR |
| AJ9 | AVSS_33 | P26 | GPIO1_A6/TSADC_INT |
| AJ11 | AVSS_34 | P27 | GPIO1_A7/SPI1_RXD/UART4_RX |
| AJ12 | AVSS_35 | P28 | GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK |
| AJ14 | AVSS_36 | P29 | GPIO1_B2/SPI1_CSN0/PMCU_JTAG_TMS |
| AJ15 | AVSS_37 | P30 | GPIO1_B4/I2C4_SCL |
| AJ17 | AVSS_38 | P31 | GPIO1_B3/I2C4_SDA |
| AJ18 | AVSS_39 | R1 | DDR0_DQ23 |
| AJ20 | VSS_180 | R2 | DDR0_DQ22 |
| AJ21 | VSS_172 | R3 | VSS_123 |
| AJ23 | VSS_173 | R4 | DDR0_DQS3N |
| AJ24 | VSS_174 | R5 | VSS_124 |
| AJ26 | VSS_175 | R6 | VSS_125 |
| AJ27 | VSS_176 | R7 | DDR0_PZQ |
| AJ28 | VSS_171 | R8 | DDR0PLL_AVDD_0V9 |

| PIN# | PIN name | PIN# | PIN name |
|---|---|---|---|
| AJ29 | AVSS_47 | R9 | DDR0_VDD_7 |
| AJ30 | USIC_STROBE | R10 | DDR0_VDD_8 |
| AJ31 | USIC_DATA | R11 | GPU_VDD_8 |
| AK1 | GPIO4_C5/SPDIF_TX | R12 | GPU_VDD_9 |
| AK2 | GPIO4_C3/UART2C_RX | R13 | GPU_VDD_13 |
| AK3 | GPIO4_D3 | R14 | VSS_129 |
| AK4 | GPIO4_D1/DP_HOTPLUG | R15 | VSS_130 |
| AK5 | GPIO2_C5/SDIO0_D1/SPI5_TXD | R16 | VSS_131 |
| AK6 | MIPI_TX1/RX1_D0P | R17 | PLL_AVDD_0V9 |
| AK7 | MIPI_TX1/RX1_D1P | R18 | VSS_165 |
| AK8 | MIPI_TX1/RX1_CLKP | R19 | LITCPU_VDD_2 |
| AK9 | MIPI_TX1/RX1_D2P | R20 | LITCPU_VDD_3 |
| AK10 | MIPI_TX1/RX1_D3P | R21 | VSS_120 |
| AK11 | MIPI_RX0_D3P | R22 | LITCPU_VDD_7 |
| AK12 | MIPI_RX0_D2P | R23 | VSS_133 |
| AK13 | MIPI_RX0_CLKP | R24 | PMUIO1_VDD_1V8 |
| AK14 | MIPI_RX0_D1P | R25 | GPIO1_A0/ISP0_SHUTTER_EN/ISP1_SHUTTER_EN/TCPD_VBUS_SINK_EN |
| AK15 | MIPI_RX0_D0P | R26 | GPIO1_A2/ISP0_FLASHTRIGIN/ISP1_FLASHTRIGIN/TCPD_CC1_VCONN_EN |
| AK16 | HDMI_TCP | R27 | GPIO1_A3/ISP0_FLASHTRIGOUT/ISP1_FLASHTRIGOUT |
| AK17 | HDMI_TX0P | R28 | GPIO1_A4/ISP0_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG |
| AK18 | HDMI_TX1P | R29 | GPIO0_A1/DDRIO_PWROFF/TCPD_CCDB_EN |
| AK19 | HDMI_TX2P | R30 | GPIO1_A5/AP_PWROFF |
| AK20 | TYPEC0_AUXP | R31 | GPIO1_B0/SPI1_TXD/UART4_TX |
| AK21 | TYPEC0_RX1P | T1 | DDR0_DQ20 |
| AK22 | TYPEC0_TX1M | T2 | DDR0_DQ21 |
| AK23 | TYPEC0_RX2P | T8 | VSS_134 |
| AK24 | TYPEC0_TX2M | T9 | DDR0_VDD_9 |
| AK25 | TYPEC1_RX1P | T10 | VSS_135 |
| AK26 | TYPEC1_TX1M | T11 | GPU_VDD_10 |
| AK27 | TYPEC1_RX2P | T12 | GPU_VDD_11 |
| AK28 | TYPEC1_TX2M | T13 | GPU_VDD_12 |
| AK29 | TYPEC1_AUXP | T14 | GPU_VDD_14 |
| AK30 | TYPEC0_U2VBUSDET | T15 | GPU_VDD_COM |
| AK31 | TYPEC1_U2VBUSDET | T16 | VSS_138 |
| AL1 | VSS_23 | T17 | LOGIC_VDD_11 |
| AL2 | GPIO4_C1/I2C3_SCL/UART2B_TX | T18 | VSS_168 |
| AL3 | GPIO4_C6/PWM1 | T19 | VSS_122 |
| AL4 | GPIO2_D2/SDIO0_DETN/PCIE_CLKREQN | T20 | LITCPU_VDD_6 |
| AL5 | GPIO2_C3/UART0_RTSN | T21 | VSS_139 |
| AL6 | MIPI_TX1/RX1_D0N | T22 | LITCPU_VDD_5 |

| PIN# | PIN name | PIN# | PIN name |
|---|---|---|---|
| AL7 | MIPI_TX1/RX1_D1N | T23 | SDMMC0_VDD |
| AL8 | MIPI_TX1/RX1_CLKN | T24 | PMU_VDD_0V9 |
| AL9 | MIPI_TX1/RX1_D2N | T30 | NPOR |
| AL10 | MIPI_TX1/RX1_D3N | T31 | GPIO1_A1/ISP0_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/TCPD_CC0_VCONN_EN |
| AL11 | MIPI_RX0_D3N | U1 | DDR0_DQ18 |
| AL12 | MIPI_RX0_D2N | U2 | DDR0_DQ19 |
| AL13 | MIPI_RX0_CLKN | U3 | VSS_141 |
| AL14 | MIPI_RX0_D1N | U4 | DDR0_DQS2P |
| AL15 | MIPI_RX0_D0N | U5 | DDR0_DM2 |
| AL16 | HDMI_TCN | U6 | DDR0_ATB0 |
| AL17 | HDMI_TX0N | U7 | DDR0_ATB1 |
| AL18 | HDMI_TX1N | U8 | VSS_142 |
| AL19 | HDMI_TX2N | U9 | DDR0_VDD_10 |
| AL20 | TYPEC0_AUXM | U10 | DDR0_VDD_11 |
| AL21 | TYPEC0_RX1M | U11 | VSS_126 |
| AL22 | TYPEC0_TX1P | U12 | VSS_127 |
| AL23 | TYPEC0_RX2M | U13 | GPU_VDD_7 |
| AL24 | TYPEC0_TX2P | U14 | VSS_137 |
| AL25 | TYPEC1_RX1M | U15 | VSS_143 |
| AL26 | TYPEC1_TX1P | U16 | VSS_144 |
| AL27 | TYPEC1_RX2M | U17 | LOGIC_VDD_8 |
| AL28 | TYPEC1_TX2P | U18 | LOGIC_VDD_7 |
| AL29 | TYPEC1_AUXM | U19 | VSS_146 |
| AL30 | TYPEC0_ID | U20 | LOGIC_VDD_12 |
| AL31 | VSS_178 | U21 | VSS_147 |
| B1 | DDR0_CSN1 | U22 | VSS_149 |
| B2 | DDR1_BA0 | U23 | AVSS_49 |
| B3 | DDR1_CSN3 | U24 | USB_AVDD_1V8 |
| B4 | DDR1_A13 | U25 | PMU_VDD_1V8 |
| B5 | VSS_24 | U26 | SDMMC0_VDDPST |
| B6 | DDR1_A8 | U27 | GPIO4_B3/SDMMC0_D3/APJTAG_TMS |
| B7 | DDR1_A6 | U28 | GPIO0_B0/SDMMC0_WRPT/TEST_CLKOUT2 |
| B8 | DDR1_A4 | U29 | VSS_150 |
| B9 | DDR1_A2 | U30 | GPIO0_B3 |
| B10 | DDR1_A0 | U31 | GPIO0_A0/TEST_CLKOUT0/CLK32K_IN |
| B11 | DDR1_DQ8 | V1 | DDR0_DQ16 |
| B12 | DDR1_DQ9 | V2 | DDR0_DQ17 |
| B13 | DDR1_DQ11 | V3 | VSS_151 |
| B14 | DDR1_DQ15 | V4 | DDR0_DQS2N |
| B15 | DDR1_DQ0 | V5 | VSS_152 |
| B16 | DDR1_DQ2 | V6 | DDR0_PLL_TESTOUT_P |
| B17 | DDR1_DQ4 | V7 | DDR0_PLL_TESTOUT_N |
| B18 | DDR1_DQ7 | V8 | VSS_153 |

| PIN# | PIN name | PIN# | PIN name |
|---|---|---|---|
| B19 | DDR1_DQ17 | V9 | DDR0_VDD_12 |
| B20 | DDR1_DQ19 | V10 | VSS_154 |
| B21 | DDR1_DQ21 | V11 | GPU_VDD_15 |
| B22 | DDR1_DQ22 | V12 | GPU_VDD_16 |
| B23 | DDR1_DQ25 | V13 | GPU_VDD_6 |
| B24 | DDR1_DQ28 | V14 | GPU_VDD_5 |
| B25 | DDR1_DQ30 | V15 | GPU_VDD_4 |
| B26 | DDR1_DQ31 | V16 | GPU_VDD_17 |
| B27 | GPIO3_B7/MAC_CRS/UART3_TX/CIF_CLKOUTB | V17 | VSS_148 |
| B28 | EDP_AUXP | V18 | LOGIC_VDD_5 |
| B29 | EDP_TX0P | V19 | LOGIC_VDD_4 |
| B30 | EDP_TX1P | V20 | LOGIC_VDD_3 |
| B31 | EDP_AVSS_1 | V21 | LOGIC_VDD_2 |
| C1 | DDR0_A12 | V22 | LOGIC_VDD_1 |
| C2 | DDR0_CSN3 | V23 | AVSS_50 |
| C3 | DDR0_BA0 | V24 | USB_AVDD_0V9 |
| C4 | DDR1_A14 | V25 | GPIO4_B5/SDMMC0_CMD/MCUJTAG_TMS |
| C5 | DDR1_A11 | V26 | GPIO0_B4/TCPD_VBUS_BDIS |
| C6 | DDR1_RASN | V27 | GPIO0_A5/EMMC_PWRON |
| C8 | VSS_25 | V28 | GPIO0_A7/SDMMC0_DET |
| C9 | VSS_26 | V29 | GPIO4_B4/SDMMC0_CLKOUT/MUCJTAG_TCK |
| C11 | VSS_27 | V30 | GPIO0_B1/PMUIO2_VOLSEL |
| C12 | VSS_28 | V31 | GPIO0_A3/SDIO0_WRPT |
| C14 | VSS_29 | W1 | DDR0_DQ6 |
| C15 | VSS_30 | W2 | DDR0_DQ7 |
| C17 | VSS_31 | W8 | VSS_161 |
| C18 | VSS_32 | W9 | VSS_162 |
| C20 | VSS_33 | W10 | GPU_VDD_20 |
| C21 | VSS_34 | W11 | GPU_VDD_1 |
| C23 | VSS_35 | W12 | GPU_VDD_2 |
| C24 | VSS_36 | W13 | VSS_128 |
| C26 | VSS_37 | W14 | GPU_VDD_3 |
| C27 | GPIO3_B1/MAC_RXDV | W15 | GPU_VDD_19 |
| C28 | EDP_AVSS_2 | W16 | GPU_VDD_18 |
| C29 | EDP_AVSS_3 | W17 | VSS_159 |
| C30 | EDP_TX2P | W18 | VSS_169 |
| C31 | EDP_TX2N | W19 | VSS_167 |
| D1 | DDR0_A10 | W20 | LOGIC_VDD_6 |
| D2 | DDR0_A13 | W21 | VSS_81 |
| D3 | DDR0_A14 | W22 | VSS_158 |
| D5 | VSS_38 | W23 | AVSS_46 |
| D6 | DDR1_BA1 | W24 | PCIE_AVDD_0V9 |
| D8 | DDR1_CLK0N | W30 | VSS_160 |

| PIN# | PIN name | PIN# | PIN name |
|---|---|---|---|
| D9 | DDR1_CLK0P | W31 | GPIO0_B2 |
| D11 | DDR1_ODT0 | Y1 | DDR0_DQ5 |
| D12 | DDR1_BA2 | Y2 | DDR0_DQ4 |
| D14 | DDR1_DQS1N | Y3 | VSS_8 |
| D15 | DDR1_DQS1P | Y4 | DDR0_DQS0P |
| D17 | DDR1_DQS0N | Y5 | DDR0_DM0 |
| D18 | DDR1_DQS0P | Y6 | GPIO4_A2/I2C1_SCL |
| D20 | DDR1_DQS2N | Y7 | GPIO3_D3/I2S0_SDI0 |
| D21 | DDR1_DQS2P | Y8 | APIO5_VDD |
| D23 | DDR1_DQS3N | Y9 | VSS_166 |
| D24 | DDR1_DQS3P | Y10 | VSS_15 |
| D26 | GPIO3_A4/MAC_TXD0/SPI0_RXD | Y11 | VSS_155 |
| D27 | GPIO3_C0/MAC_COL/UART3_CTSN/ SPDIF_TX | Y12 | VSS_136 |
| D29 | EDP_AVSS_4 | Y13 | VSS_164 |
| D30 | EDP_TX3P | Y14 | VSS_156 |
| D31 | EDP_TX3N | Y15 | VSS_157 |
| E1 | DDR0_CKE0 | Y16 | VSS_118 |
| E2 | VSS_39 | Y17 | VSS_95 |
| E3 | DDR0_A11 | Y18 | TYPEC0_AVDD_0V9_2 |
| E4 | VSS_40 | Y19 | TYPEC0_AVDD_0V9_1 |
| E6 | DDR1_CKE1 | Y20 | VSS_170 |
| E7 | VSS_41 | Y21 | TYPEC1_AVDD_0V9_1 |
| E8 | DDR1_CLK1N | Y22 | TYPEC1_AVDD_0V9_2 |
| E9 | DDR1_CLK1P | Y23 | AVSS_1 |
| E11 | DDR1_ODT1 | Y24 | PCIE_AVDD_1V8 |
| E12 | VSS_42 | Y25 | USB_AVDD_3V3 |
| E14 | DDR1_DM1 | Y26 | GPIO4_B1/SDMMC0_D1/UART2A_TX |
| E15 | VSS_43 | Y27 | GPIO4_B0/SDMMC0_D0/UART2A_RX |
| E17 | DDR1_DM0 | Y28 | GPIO4_B2/SDMMC0_D2/APJTAG_TCK |
| E18 | VSS_44 | Y29 | AVSS_48 |
| E20 | DDR1_DM2 | Y30 | XOUT_OSC |
| E21 | VSS_45 | Y31 | XIN_OSC |

## 2.6 Power/ground IO descriptions

Table 2-2 Power/Ground IO information

| Group | Ball # | Descriptions |
|---|---|---|
| VSS | A1,A27,A31,AA3,AA5,AA9,AA10,AA13,AB9,AB19,AC3,AC18,AC20,AC21,AC22,AD3,AD5,AD10,AD21,AD22,AE23,AF9,AF18,AF20,AG2,AJ5,AJ20,AJ21,AJ23,AJ24,AJ26,AJ27,AJ28,AL1,AL31,B5,C8,C9,C11,C12,C14,C15,C17,C18,C20,C21,C23,C24,C26,D5,E2,E4,E7,E12,E15,E18,E21,E24,E31,F8,F15,F18,F20,F21,G5,G9,G18,G27,H3,H9,H10,H11,H12,H13,H15,H16,H17,H18,H26,J3,J6,J7,J | Internal Logic Ground and Digital IO Ground |

| Group | Ball # | Descriptions |
|---|---|---|
| | 8,J9,J10,K8,K9,K10,K12,K14,K16,K18,K20,K22,L3,L6,L8,L11,L12,L13,L14,L15,L16,L20,L22,L27,M3,M8,M10,M16,M23,N8,N13,N14,N15,N16,N17,N19,N21,P3,P6,P7,P8,P10,P11,P12,P16,P19,P21,R3,R5,R6,R14,R15,R16,R18,R21,R23,T8,T10,T16,T18,T19,T21,U3,U8,U11,U12,U14,U15,U16,U19,U21,U22,U29,V3,V5,V8,V10,V17,W8,W9,W13,W17,W18,W19,W21,W22,W30,Y3,Y9,Y10,Y11,Y12,Y13,Y14,Y15,Y16,Y17,Y20 | |
| BIGCPU_VDD | K19,K21,L18,L19,L21,L23,M18,M19,M20,M21,M22,N18,N20,N22 | Internal BIG CPU A72 Power |
| LITCPU_VDD | P20,P22,R19,R20,R22,T20,T22 | Internal LITTLE CPU A53 Power |
| GPU_VDD | R11,R12,R13,T11,T12,T13,T14,T15,U13,V11,V12,V13,V14,V15,V16,W10,W11,W12,W14,W15,W16 | Internal GPU power |
| LOGIC_VDD | L17,M17,T17,U17,U18,U20,V18,V19,V20,V21,V22,W20 | Internal Logic Power |
| CENTERLOGIC_VDD | M11,M12,M13,M14,M15,N11,N12,P13,P14,P15 | Internal center logic power |
| DDR0_VDD | L9,L10,M9,N9,N10,P9,R9,R10,T9,U9,U10,V9 | DDR0 Digital IO Power |
| DDR0_CLK_VDD | M7 | DDR0Clock IO Power |
| DDR0PLL_AVDD_0V9 | R8 | DDR0 PHY PLL power |
| DDR1_VDD | J11,J12,J13,J14,J15,J16,J17,J18,K11,K13,K15,K17 | DDR1 Digital IO Power |
| DDR1_CLK_VDD | G12 | DDR1 Clock IO Power |
| DDR1PLL_AVDD_0V9 | H14 | DDR1 PHY PLL power |
| PMU_VDD_0V9 | T24 | Internal PMU Domain Power |
| PMU_VDD_1V8 | U25 | |
| PMUIO1_VDD | R24 | PMUIO1 Domain IO Power |
| PMUIO2_VDD | P23 N23 | PMUIO2 Domain IO Power |
| APIO1_VDD | J23 | GPIO group 1 Digital Power |
| APIO1_VDDPST | K23 | GPIO group 1Bias |
| APIO2_VDD | L23 J22 | GPIO group 2 Digital Power |
| APIO2_VDDPST | J24 | GPIO group 2 Bias |
| APIO3_VDD | AB8 | GPIO group 3 Digital Power |
| APIO4_VDD | AC9 | GPIO group 4 Digital Power |
| APIO4_VDDPST | AC8 | GPIO group 4Bias |
| APIO5_VDD | Y8 | GPIO group 5 Digital Power |
| APIO5_VDDPST | AA8 | GPIO group 5Bias |
| SDMMC0_VDD | T23, U26 | SDMMC Digital IO Power |
| AVSS | AA11,AA12,AA14,AA15,AA23,AA26,AA29,AB10,AB11,AB13,AB15,AB16,AB17,AB23,AC11,AC13,AC15,AC16,AC17,AC23,AC25,AC26,AC29,AD13,AD17,AD26,AD29,AE11,AE12,AE14,AE17,AE27,AF17,AF23,AF24,AF29,AG29,AH29,AJ6,AJ8,AJ9,AJ11,AJ12,AJ14,AJ15,AJ17,AJ18,AJ29,B31,C28,C29,D29,H19,J21,U23,V23,W23,Y23,Y29 | Analog Ground |
| PLL_AVDD_0V9 | R17 | PLL 0.9V Analog Power |
| PLL_AVDD_1V8 | P18 | PLL 1.8V Analog Power |

| Group | Ball # | Descriptions |
|---|---|---|
| PLL_AVSS | P17 | PLL Analog Ground |
| ADC_AVDD | AC24 | SAR-ADC/TSADC Power |
| EMMC_VDD_1V8 | K24 | eMMC digital power |
| EMMC_COREDLL_0V9 | L24 | eMMC core digital power |
| USB_AVDD_0V9 | V24 | USB 2.0 Digital Power |
| USB_AVDD_1V8 | U24 | USB 2.0 Analog Power |
| USB_AVDD_3V3 | Y25 | USB 2.0 Analog Power |
| TYPEC0_AVDD_0V9 | Y18,Y19 | Type-C Digital Power |
| TYPEC0_AVDD_1V8 | AA18 | Type-C Analog Power |
| TYPEC0_AVDD_3V3 | AB18 | Type-C Analog Power |
| TYPEC1_AVDD_0V9 | Y21,Y22 | Type-C Digital Power |
| TYPEC1_AVDD_1V8 | AA21 | Type-C Analog Power |
| TYPEC1_AVDD_3V3 | AB21 | Type-C Analog Power |
| EFUSE | AD23 | eFuse IO Digital Power |
| USIC_AVDD_1V2 | AD24 | USIC 1.2V Power Supply |
| USIC_AVDD_0V9 | AD25 | USIC 0.9V Power Supply |
| EDP_AVDD_0V9 | H20 | eDP0.9V Power Supply |
| EDP_AVDD_1V8 | J19,J20 | eDP 1.8V Power Supply |
| EDP_AVSS | B31,C28,C29,D29,H19,J21 | eDP analog ground |
| HDMI_AVDD_0V9 | AA16,AA17 | HDMI 0.9V Power Supply |
| HDMI_AVDD_1V8 | AD16 | HDMI 1.8V Power Supply |
| MIPI_AVDD_1V8 | AB14 AB12 AC10 | MIPI 1.8V Power Supply |
| PCIE_AVDD_0V9 | W24 | PCIE 0.9V analog power |
| PCIE_AVDD_1V8 | Y24 | PCIE 1.8V analog power |

## 2.7 Function IO description

Table 2-3 Function IO description

| Pin Name | Func 1 | Func 2 | Func 3 | Func 4 | Type | Def | PD/PU | Default | INT |
|---|---|---|---|---|---|---|---|---|---|
| GPIO0_A0/TESTCLKOUT0/CLK32K_IN | gpio0_a[0] | testclkout0 | clk32k_in | | I/O | I | up | 5mA | √ |
| GPIO0_A1/DDRIO_PWROFF/TCPD_CCDB_EN | gpio0_a[1] | ddrio_pwroff | tcpd_ccdb_en | | I/O | I | up | 5mA | √ |
| GPIO0_A2/WIFI_26MHZ | gpio0_a[2] | wifi_26m | | | I/O | I | down | 5mA | √ |
| GPIO0_A3/SDIO0_WRPT | gpio0_a[3] | sdio0_wrpt | | | I/O | I | down | 5mA | √ |
| GPIO0_A4/SDIO0_INTN | gpio0_a[4] | sdio0_intn | | | I/O | I | down | 5mA | √ |
| GPIO0_A5/EMMC_PWRON | gpio0_a[5] | emmc_pwren | | | I/O | I | up | 5mA | √ |
| GPIO0_A6/PWMA3_IR | gpio0_a[6] | pwma3_ir | | | I/O | I | down | 5mA | √ |
| GPIO0_A7/SDMMC0_DET | gpio0_a[7] | sdmmc0_dectn | | | I/O | I | up | 5mA | √ |
| GPIO0_B0/SDMMC0_WRPRT/TEST_CLKOUT2 | gpio0_b[0] | sdmmc0_wrprt | test_clkout2 | | I/O | I | up | 5mA | √ |
| GPIO0_B1/PMUIO2_1833_VOLSEL | gpio0_b[1] | pmuio2_1833_volsel | | | I/O | I | down | 5mA | √ |
| GPIO0_B2 | gpio0_b[2] | | | | I/O | I | down | 5mA | √ |
| GPIO0_B3 | gpio0_b[3] | | | | I/O | I | down | 5mA | √ |
| GPIO0_B4/TCPD_VBUS_BDIS | gpio0_b[4] | tcpd_vbus_bdis | | | I/O | I | down | 5mA | √ |
| GPIO0_B5/TCPD_VBUS_FDIS/TCPD_VBUS_SOURCE3 | gpio0_b[5] | tcpd_vbus_fdis | tcpd_vbus_source3 | | I/O | I | down | 5mA | √ |
| GPIO1_A0/ISP_SHUTTER_EN/TCPD_VBUS_SINK_EN | gpio1_a[0] | isp0_shutter_en | isp1_shutter_en | tcpd_vbus_sink_en | I/O | I | down | 3mA | √ |
| GPIO1_A1/ISP_SHUTTER_TRIG/TCPD_CC0_VCONN_EN | gpio1_a[1] | isp0_shutter_trig | isp1_shutter_trig | tcpd_cc0_vconn_en | I/O | I | down | 3mA | √ |
| GPIO1_A2/ISP_FLASHTRIGIN/TCPD_CC1_VCONN_EN | gpio1_a[2] | isp0_flashtrigin | isp1_flashtrigin | tcpd_cc1_vconn_en | I/O | I | down | 3mA | √ |
| GPIO1_A3/ISP_FLASHTRIGOUT | gpio1_a[3] | isp0_flashtrigout | isp1_flashtrigout | | I/O | I | down | 3mA | √ |
| GPIO1_A4/ISP_PRELIGHT_TRIG | gpio1_a[4] | isp0_prelight_trig | isp1_prelight_trig | | I/O | I | down | 3mA | √ |
| GPIO1_A5/AP_PWROFF | gpio1_a[5] | ap_pwroff | | | I/O | I | down | 3mA | √ |
| GPIO1_A6/TSADC_INT | gpio1_a[6] | tsadc_int | | | I/O | I | high-z | 3mA | √ |
| GPIO1_A7/PMCU_UART4DBG_RX/SPI1_RXD | gpio1_a[7] | pmcu_uart4dbg_rx | spi1_rxd | | I/O | I | up | 6mA | √ |
| GPIO1_B0/PMCU_UART4DBG_TX/SPI1_TXD | gpio1_b[0] | pmcu_uart4dbg_tx | spi1_txd | | I/O | I | up | 6mA | √ |

| Pin Name | Func 1 | Func 2 | Func 3 | Func 4 | Type | Def | PD/PU | Default | INT |
|---|---|---|---|---|---|---|---|---|---|
| GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK | gpio1_b[1] | pmcu_jtag_tck | spi1_clk | | I/O | I | up | 6mA | √ |
| GPIO1_B2/SPI1_CSN0/PMCU_JTAG_TMS | gpio1_b[2] | pmcu_jtag_tms | spi1_csn0 | | I/O | I | up | 6mA | √ |
| GPIO1_B3/I2C4_SDA | gpio1_b[3] | i2c4_sda | | | I/O | I | up | 3mA | √ |
| GPIO1_B4/I2C4_SCL | gpio1_b[4] | i2c4_scl | | | I/O | I | up | 3mA | √ |
| GPIO1_B5 | gpio1_b[5] | | | | I/O | I | down | 3mA | √ |
| GPIO1_B6/PWMB3_IR | gpio1_b[6] | pwmb3_ir | | | I/O | I | down | 3mA | √ |
| GPIO1_B7/SPI3_RXD/I2C0_SDA | gpio1_b[7] | spi3_rxd | i2c0_sda | | I/O | I | up | 3mA | √ |
| GPIO1_C0/SPI3_TXD/I2C0_SCL | gpio1_c[0] | spi3_txd | i2c0_scl | | I/O | I | up | 3mA | √ |
| GPIO1_C1/SPI3_CLK | gpio1_c[1] | spi3_clk | | | I/O | I | down | 3mA | √ |
| GPIO1_C2/SPI3_CSN0 | gpio1_c[2] | spi3_csn0 | | | I/O | I | up | 3mA | √ |
| GPIO1_C3/PWM2 | gpio1_c[3] | pwm2 | | | I/O | I | down | 3mA | √ |
| GPIO1_C4/I2C8_SDA | gpio1_c[4] | i2c8_sda | | | I/O | I | up | 3mA | √ |
| GPIO1_C5/I2C8_SCL | gpio1_c[5] | i2c8_scl | | | I/O | I | up | 3mA | √ |
| GPIO1_C6/DFTJTAG_TDI/TCPD_VBUS_SOURCE0 | gpio1_c[6] | dftjtag_tdi | tcpd_vbus_source0 | | I/O | I | down | 6mA | √ |
| GPIO1_C7/DFTJTAG_TDO/TCPD_VBUS_SOURCE1 | gpio1_c[7] | dftjtag_tdo | tcpd_vbus_source1 | | I/O | I | down | 6mA | √ |
| GPIO1_D0/DFTJTAG_CLK/TCPD_VBUS_SOURCE2 | gpio1_d[0] | dftjtag_clk | tcpd_vbus_source2 | | I/O | I | down | 6mA | √ |
| GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA | gpio2_a[0] | vop_data[0] | io_cif_data0 | i2c2_sda | I/O | I | up | 3mA | √ |
| GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL | gpio2_a[1] | vop_data[1] | io_cif_data1 | i2c2_scl | I/O | I | up | 3mA | √ |
| GPIO2_A2/VOP_D2/CIF_D2 | gpio2_a[2] | vop_data[2] | io_cif_data2 | | I/O | I | down | 3mA | √ |
| GPIO2_A3/VOP_D3/CIF_D3 | gpio2_a[3] | vop_data[3] | io_cif_data3 | | I/O | I | down | 3mA | √ |
| GPIO2_A4/VOP_D4/CIF_D4 | gpio2_a[4] | vop_data[4] | io_cif_data4 | | I/O | I | down | 3mA | √ |
| GPIO2_A5/VOP_D5/CIF_D5 | gpio2_a[5] | vop_data[5] | io_cif_data5 | | I/O | I | down | 3mA | √ |
| GPIO2_A6/VOP_D6/CIF_D6 | gpio2_a[6] | vop_data[6] | io_cif_data6 | | I/O | I | down | 3mA | √ |
| GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA | gpio2_a[7] | vop_data[7] | io_cif_data7 | i2c7_sda | I/O | I | up | 3mA | √ |
| GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL | gpio2_b[0] | vop_clk | io_cif_vsync | i2c7_scl | I/O | I | up | 3mA | √ |
| GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA | gpio2_b[1] | spi2_rxd | io_cif_href | i2c6_sda | I/O | I | up | 3mA | √ |

| Pin Name | Func 1 | Func 2 | Func 3 | Func 4 | Type | Def | PD/PU | Default | INT |
|---|---|---|---|---|---|---|---|---|---|
| GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL | gpio2_b[2] | spi2_txd | io_cif_clkin | i2c6_scl | I/O | I | up | 3mA | √ |
| GPIO2_B3/SPI2_CLK/VOP_DEN/CIF_CLKOUT | gpio2_b[3] | spi2_clk | io_cif_clkout | vop_den | I/O | I | up | 3mA | √ |
| GPIO2_B4/SPI2_CSN0 | gpio2_b[4] | spi2_csn0 | | | I/O | I | up | 3mA | √ |
| GPIO2_C0/UART0_RX | gpio2_c[0] | uart0_rx | | | I/O | I | up | 5mA | √ |
| GPIO2_C1/UART0_TX | gpio2_c[1] | uart0_tx | | | I/O | I | up | 5mA | √ |
| GPIO2_C2/UART0_CTSN | gpio2_c[2] | uart0_ctsn | | | I/O | I | up | 5mA | √ |
| GPIO2_C3/UART0_RTSN | gpio2_c[3] | uart0_rtsn | | | I/O | I | up | 5mA | √ |
| GPIO2_C4/SDIO0_D0/SPI5_RXD | gpio2_c[4] | sdio0_data0 | spi5_rxd | | I/O | I | up | 5mA | √ |
| GPIO2_C5/SDIO0_D1/SPI5_TXD | gpio2_c[5] | sdio0_data1 | spi5_txd | | I/O | I | up | 5mA | √ |
| GPIO2_C6/SDIO0_D2/SPI5_CLK | gpio2_c[6] | sdio0_data2 | spi5_clk | | I/O | I | up | 5mA | √ |
| GPIO2_C7/SDIO0_D3/SPI5_CSN0 | gpio2_c[7] | sdio0_data3 | spi5_csn0 | | I/O | I | up | 5mA | √ |
| GPIO2_D0/SDIO0_CMD | gpio2_d[0] | sdio0_cmd | | | I/O | I | up | 5mA | √ |
| GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1 | gpio2_d[1] | sdio0_clkout | test_clkout1 | | I/O | I | up | 5mA | √ |
| GPIO2_D2/SDIO0_DETN/PCIE_CLKREQN | gpio2_d[2] | sdio0_detect_n | pcie_clkreqn | | I/O | I | up | 5mA | √ |
| GPIO2_D3/SDIO0_PWREN | gpio2_d[3] | sdio0_pwren | | | I/O | I | down | 5mA | √ |
| GPIO2_D4/SDIO0_BKPWR | gpio2_d[4] | sdio0_bkpwr | | | I/O | I | down | 5mA | √ |
| GPIO3_A0/MAC_TXD2/SPI4_RXD | gpio3_a[0] | mac_txd2 | spi4_rxd | trace_data12 | I/O | I | down | 4mA | √ |
| GPIO3_A1/MAC_TXD3/SPI4_TXD | gpio3_a[1] | mac_txd3 | spi4_txd | trace_data13 | I/O | I | down | 4mA | √ |
| GPIO3_A2/MAC_RXD2/SPI4_CLK | gpio3_a[2] | mac_rxd2 | spi4_clk | trace_data14 | I/O | I | up | 4mA | √ |
| GPIO3_A3/MAC_RXD3/SPI4_CSN0 | gpio3_a[3] | mac_rxd3 | spi4_csn0 | trace_data15 | I/O | I | up | 4mA | √ |
| GPIO3_A4/MAC_TXD0/SPI0_RXD | gpio3_a[4] | mac_txd0 | spi0_rxd | | I/O | I | down | 4mA | √ |
| GPIO3_A5/MAC_TXD1/SPI0_TXD | gpio3_a[5] | mac_txd1 | spi0_txd | | I/O | I | down | 4mA | √ |
| GPIO3_A6/MAC_RXD0/SPI0_CLK | gpio3_a[6] | mac_rxd0 | spi0_clk | | I/O | I | up | 4mA | √ |
| GPIO3_A7/MAC_RXD1/SPI0_CSN0 | gpio3_a[7] | mac_rxd1 | spi0_csn0 | | I/O | I | up | 4mA | √ |
| GPIO3_B0/MAC_MDC/SPI0_CSN1 | gpio3_b[0] | mac_mdc | spi0_csn1 | | I/O | I | up | 4mA | √ |
| GPIO3_B1/MAC_RXDV | gpio3_b[1] | mac_rxdv | | | I/O | I | down | 4mA | √ |

| Pin Name | Func 1 | Func 2 | Func 3 | Func 4 | Type | Def | PD/PU | Default | INT |
|---|---|---|---|---|---|---|---|---|---|
| GPIO3_B2/MAC_RXER/I2C5_SDA | gpio3_b[2] | mac_rxer | i2c5_sda | | I/O | I | up | 4mA | √ |
| GPIO3_B3/MAC_CLK/I2C5_SCL | gpio3_b[3] | mac_clk | i2c5_scl | | I/O | I | up | 4mA | √ |
| GPIO3_B4/MAC_TXEN/UART1_RX | gpio3_b[4] | mac_txen | uart1_rx | | I/O | I | up | 4mA | √ |
| GPIO3_B5/MAC_MDIO/UART1_TX | gpio3_b[5] | mac_mdio | uart1_tx | | I/O | I | up | 4mA | √ |
| GPIO3_B6/MAC_RXCLK/UART3_RX | gpio3_b[6] | mac_rxclk | uart3_rx | | I/O | I | up | 4mA | √ |
| GPIO3_B7/MAC_CRS/UART3_TX/CIF_CLKOUTB | gpio3_b[7] | mac_crs | uart3_tx | cif_clkoutb | I/O | I | up | 4mA | √ |
| GPIO3_C0/MAC_COL/UART3_CTSN/SPDIF_TX | gpio3_c[0] | mac_col | uart3_ctsn | spdif_tx | I/O | I | up | 4mA | √ |
| GPIO3_C1/MAC_TXCLK/UART3_RTSN | gpio3_c[1] | mac_txclk | uart3_rtsn | | I/O | I | up | 4mA | √ |
| GPIO3_D0/I2S0_SCLK | gpio3_d[0] | i2s0_sclk | trace_data0 | | I/O | I | down | 3mA | √ |
| GPIO3_D1/I2S0_LRCK_RX | gpio3_d[1] | i2s0_lrck_rx | trace_data1 | | I/O | I | down | 3mA | √ |
| GPIO3_D2/I2S0_LRCK_TX | gpio3_d[2] | i2s0_lrck_tx | trace_data2 | | I/O | I | down | 3mA | √ |
| GPIO3_D3/I2S0_SDI0 | gpio3_d[3] | i2s0_sdi0 | trace_data3 | | I/O | I | down | 3mA | √ |
| GPIO3_D4/I2S0_SDI1SDO3 | gpio3_d[4] | i2s0_sdi1sdo3 | trace_data4 | | I/O | I | down | 3mA | √ |
| GPIO3_D5/I2S0_SDI2SDO2 | gpio3_d[5] | i2s0_sdi2sdo2 | trace_data5 | | I/O | I | down | 3mA | √ |
| GPIO3_D6/I2S0_SDI3SDO1 | gpio3_d[6] | i2s0_sdi3sdo1 | trace_data6 | | I/O | I | down | 3mA | √ |
| GPIO3_D7/I2S0_SDO0 | gpio3_d[7] | i2s0_sdo0 | trace_data7 | | I/O | I | down | 3mA | √ |
| GPIO4_A0/I2S_CLK | gpio4_a[0] | i2s_clk | trace_ctl | | I/O | I | down | 3mA | √ |
| GPIO4_A1/I2C1_SDA | gpio4_a[1] | i2c1_sda | trace_clk | | I/O | I | up | 3mA | √ |
| GPIO4_A2/I2C1_SCL | gpio4_a[2] | i2c1_scl | trace_data8 | | I/O | I | up | 3mA | √ |
| GPIO4_A3/I2S1_SCLK | gpio4_a[3] | i2s1_sclk | trace_data9 | | I/O | I | down | 3mA | √ |
| GPIO4_A4/I2S1_LRCK_RX | gpio4_a[4] | i2s1_lrck_rx | trace_data10 | | I/O | I | down | 3mA | √ |
| GPIO4_A5/I2S1_LRCK_TX | gpio4_a[5] | i2s1_lrck_tx | trace_data11 | | I/O | I | down | 3mA | √ |
| GPIO4_A6/I2S1_SDI0 | gpio4_a[6] | i2s1_sdi0 | | | I/O | I | down | 3mA | √ |
| GPIO4_A7/I2S1_SDO0 | gpio4_a[7] | i2s1_sdo0 | | | I/O | I | down | 3mA | √ |
| GPIO4_B0/SDMMC0_D0/UART2DBG_RX | gpio4_b[0] | sdmmc0_data0 | uart2dbg_rx | | I/O | I | up | 6mA | √ |
| GPIO4_B1/SDMMC0_D1/UART2DBG_TX | gpio4_b[1] | sdmmc0_data1 | uart2dbg_tx | hdcpjtag_trstn | I/O | I | up | 6mA | √ |

| Pin Name | Func 1 | Func 2 | Func 3 | Func 4 | Type | Def | PD/PU | Default | INT |
|---|---|---|---|---|---|---|---|---|---|
| GPIO4_B2/SDMMC0_D2/APJTAG_TCK | gpio4_b[2] | sdmmc0_data2 | ap_jtag_tck | hdcpjtag_tdi | I/O | I | up | 6mA | √ |
| GPIO4_B3/SDMMC0_D3/APJTAG_TMS | gpio4_b[3] | sdmmc0_data3 | ap_jtag_tms | hdcpjtag_tdo | I/O | I | up | 6mA | √ |
| GPIO4_B4/SDMMC0_CLKOUT/MUCJTAG_TCK | gpio4_b[4] | sdmmc0_clkout | mcujtag_tck | hdcpjtag_tck | I/O | I | down | 6mA | √ |
| GPIO4_B5/SDMMC0_CMD/MCUJTAG_TMS | gpio4_b[5] | sdmmc0_cmd | mcujtag_tms | hdcpjtag_tms | I/O | I | up | 6mA | √ |
| GPIO4_C0/I2C3_SDA_HDMI/UART2DBG_RX | gpio4_c[0] | i2c3_sda_hdmi | uart2dbg_rx | | I/O | I | up | 3mA | √ |
| GPIO4_C1/I2C3_SCL_HDMI/UART2DBG_TX | gpio4_c[1] | i2c3_scl_hdmi | uart2dbg_tx | | I/O | I | up | 3mA | √ |
| GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM | gpio4_c[2] | pwm0 | vop0_pwm | vop1_pwm | I/O | I | down | 3mA | √ |
| GPIO4_C3/UART2DBG_RX/UARTHDCP_RX | gpio4_c[3] | uart2dbg_rx | uarthdcp_rx | | I/O | I | up | 3mA | √ |
| GPIO4_C4/UART2DBG_TX/UARTHDCP_TX | gpio4_c[4] | uart2dbg_tx | uarthdcp_tx | | I/O | I | up | 3mA | √ |
| GPIO4_C5/SPDIF_TX | gpio4_c[5] | spdif_tx | | | I/O | I | down | 3mA | √ |
| GPIO4_C6/PWM1 | gpio4_c[6] | pwm1 | | | I/O | I | down | 3mA | √ |
| GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG | gpio4_c[7] | hdmi_cecinout | edp_hotplug | | I/O | I | up | 3mA | √ |
| GPIO4_D0/PCIE_CLKREQN | gpio4_d[0] | pcie_clkreqn | | | I/O | I | up | 3mA | √ |
| GPIO4_D1/DP_HOTPLUG | gpio4_d[1] | dp_hotplug | | | I/O | I | down | 3mA | √ |
| GPIO4_D2 | gpio4_d[2] | | | | I/O | I | down | 3mA | √ |
| GPIO4_D3 | gpio4_d[3] | | | | I/O | I | down | 3mA | √ |
| GPIO4_D4 | gpio4_d[4] | | | | I/O | I | down | 3mA | √ |
| GPIO4_D5 | gpio4_d[5] | | | | I/O | I | down | 3mA | √ |
| GPIO4_D6 | gpio4_d[6] | | | | I/O | I | down | 3mA | √ |

*Notes :*

*①:Pad types : I = input , O = output , I/O = input/output (bidirectional) ,*
*AP = Analog Power , AG = Analog Ground*
*DP = Digital Power , DG = Digital Ground*
*A = Analog*

*②: Output Drive strength is configurable, it's the suggested value in this table. Unit is mA , only Digital IO have drive value*

*③:Reset state: I = input without any pull resistor O = output*

*④:It is die location. For examples, "Left side" means that all the related IOs are always in left side of die*

*⑤:Power supply means that all the related IOs are in this IO power domain. If multiple powers are included, they are connected together in one IO power ring*

*⑥:The pull up/pull down is configurable.*

# 2.8 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on diffierent interface.

## 2.8.1 eMMC

Table 2-4 eMMC pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| eMMC | EMMC_PWREN | I/O | eMMC card power control |
| | EMMC_STRB | I/O | eMMC strobe signal |
| | EMMC_CLK | O | eMMC clock |
| | EMMC_CALIO | I/O | CALIO connects to 10k +/- 1% resistor |
| | EMMC_TP | O | Analog DLL charge pump test point |
| | EMMC_DATA*i* | I/O | DATA*i* (*i*=0~7), 8bits data lines |
| | EMMC_CMD | I/O | eMMC CMD line |

## 2.8.2 PCIe

Table 2-5 PCIe pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| PCIe | PCIE_RCLK_100M_N<br>PCIE_RCLK_100M_P | O | 100MHz differential reference clock out for PCIe peripheral |
| | PCIE_TX[*i*]_N<br>PCIE_TX[*i*]_P<br>(i=0~3) | O | PCIe differential data output signals |
| | PCIE_RX[*i*]_N<br>PCIE_RX[*i*]_P<br>(i=0~3) | I | PCIe differential data input signals |
| | PCIE_CLKREQN | I | PCIe clock request from PCIe peripheral |

## 2.8.3 USB

Table 2-6 USB2 pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| USB 2.0<br>(*i*=0,1) | USB[*i*]_DN | I/O | USB 2.0 data DN |
| | USB[*i*]_DP | I/O | USB 2.0 data DP |
| | USB[*i*]_RBIAS | I | Connect 135ohm resister to ground |

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| USB 3.0<br>And<br>Type-C<br>(*i*=0,1) | TYPEC[*i*]_DN | I/O | USB 2.0 data DN |
| | TYPEC[*i*]_DP | I/O | USB 2.0 data DP |
| | USB[*i*]_RBIAS | I | Connect 135ohm resister to ground (Shared with USB 2.0 host) |
| | TYPEC[*i*]_ID | I | USB 2.0 OTG ID detection |
| | TYPEC[*i*]_VBUSDET | I | VBUS BUMP into the PHY for VBUS monitor |
| | TYPEC[*i*]_CC2 | I/O | Configuration Channel2 pin used for connectiondetect interface configuration and VCONN. |

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| | TYPEC[*i*]_CC1 | I/O | Configuration Channel1 pin used for connectiondetect interface configuration and VCONN. |
| | TYPEC[*i*]_TX1P<br>TYPEC[*i*]_TX1M | O | Lane 0 transmitter serial data - USB Tx or DP Tx. TX+/TX1- USB Type-C receptacle pins (A2/A3) |
| | TYPEC[*i*]_TX2P<br>TYPEC[*i*]_TX2M | O | Lane 3 transmitter serial data - USB Tx or DP Tx. TX2+/TX2- USB Type-C receptacle pins (B2/B3) |
| | TYPEC[*i*]_RX1P<br>TYPEC[*i*]_RX1M | I/O | Lane 1 transmitter/receiver serial data - USB Rx or DP Tx. RX1+/RX1- USB Type-C receptacle pins (B11/B10) |
| | TYPEC[*i*]_RX2P<br>TYPEC[*i*]_RX2M | I/O | Lane 2 transmitter/receiver serial data - USB Rx or DP Tx. RX2+/RX2- USB Type-C receptacle pins (A11/A10) |
| | TYPEC[*i*]_RCLKM<br>TYPEC[*i*]_RCLKP | O | External reference clock. Supports nominal frequencies of19.2, 20, 24, 27, 54 and 108 MHz. The following external referenceclock sources are supported:<br>• AC coupled differential low swing clock (HCSL levels)<br>• DC single ended clock on ref_p pin. In this mode ref_mshouldbe tied to ground. This mode is for test purposes only.<br>A reference clock must be provided either on these external pinsor the refclock internal SoC-side pin. |
| | TYPEC[*i*]_REXT | I | External calibration resistor |
| | TYPEC[*i*]_REXT_CC | I | Bump to conect external precision resistors for internalcalibration circuits. |
| | TYPEC[*i*]_AUXM/PU_PD<br>TYPEC[*i*]_AUXP/PD_PU | I/O | AUX pull-up/pull-down polarity reversal pins. For normal connectororientation, there is a weak pull-down on aux_p wires and aweak pull-up on aux_m wire. These pins are used to reverse thisfor the flipped connector case. |
| | TYPEC[*i*]_AUXM<br>TYPEC[*i*]_AUXP | I/O | AUX differential Tx/Rx serial data |

### 2.8.4 eDP

Table 2-7 eDP pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| eDP | EDP_TX*i*P(*i*=0~3) | O | eDP data lane positive output |
| | EDP_TX*i*N(*i*=0~3) | O | eDP data lane negative output |
| | EDP_DC_TP | O | eDP PHY DC test point |
| | EDP_AUXP | I/O | eDP CH-AUX positive differential output |
| | EDP_AUXN | I/O | eDP CH-AUX negative differential output |
| | EDP_REXT | I | Let it floating |
| | EDP_CLK24M_IN | I | 24MHz input reference clock |
| | EDP_HOTPLUG | I | eDP external hot plug signal |

### 2.8.5 HDMI

Table 2-8 HDMI pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| HDMI | HDMI_TX*i*N(*i*=0~2) | O | HDMI negative TMDS differential line driver data output |

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| | HDMI_X*i*P(*i*=0~2) | O | HDMI positive TMDS differential line driver data output |
| | HDMI_TCN | O | HDMI negative TMDS differential line driver clock output |
| | HDMI_TCP | O | HDMI positive TMDS differential line driver clock output |
| | HDMI_REXT | I/O | HDMI reference resistor connection |
| | HDMI_HPD | I/O | HDMI hot plug detect signal |
| | I2C3_SDA_HDMI | I/O | I2C data line for HDMI |
| | I2C3_SCL_HDMI | I/O | I2C clock line for HDMI |
| | HDMI_CECINOUT | I/O | HDMI CEC signal |

### 2.8.6 MIPI

Table 2-9 MIPI pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| MIPI_DSI | MIPI_TX0_D*i*N(*i*=0~3) | I/O | MIPI DSI negative differential data line transceiver output |
| | MIPI_TX0_D*i*P(*i*=0~3) | I/O | MIPI DSI positive differential data line transceiver output |
| | MIPI_TX0_CLKP | I/O | MIPI DSI positive differential clock line transceiver output |
| | MIPI_TX0_CLKN | I/O | MIPI DSI negative differential clock line transceiver output |
| | MIPI_TX0_REXT | I/O | MIPI DSI external resistor connection. Recommend to use a 4.02 KΩ E96 resistor. |

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| MIPI_CSI | MIPI_RX0_D*i*N(*i*=0~3) | I/O | MIPI CSI negative differential data line transceiver output |
| | MIPI_RX0_D*i*P(*i*=0~3) | I/O | MIPI CSI positive differential data line transceiver output |
| | MIPI_RX0_CLKP | I/O | MIPI CSI positive differential clock line transceiver output |
| | MIPI_RX0_CLKN | I/O | MIPI CSI negative differential clock line transceiver output |
| | MIPI_RX0_REXT | I/O | MIPI CSI external resistor connection. Recommend to use a 4.02 KΩ E96 resistor. |

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| MIPI_CSI/DSI | MIPI_TX1/RX1_D*i*N(*i*=0~3) | I/O | MIPI CSI negative differential data line transceiver output |
| | MIPI_ TX1/RX1_D*i*P(*i*=0~3) | I/O | MIPI CSI positive differential data line transceiver output |
| | MIPI_ TX1/RX1_CLKP | I/O | MIPI CSI positive differential clock line transceiver output |
| | MIPI_ TX1/RX1_CLKN | I/O | MIPI CSI negative differential clock line transceiver output |
| | MIPI_ TX1/RX1_REXT | I/O | MIPI CSI external resistor connection. Recommend to use a 4.02 KΩ E96 resistor. |

### 2.8.7 ISP

Table 2-10 ISP pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| ISP | ISP_SHUTTER_EN*i*(*i*=0~1) | O | Hold signal for shutter open |
| | ISP_FLASHTRIGOUT*i*(*i*=0~1) | O | Hold signal for flash light |
| | ISP_PRELIGHT_TRIG*i*(*i*=0~1) | O | Hold signal for prelight |
| | ISP_SHUTTER_TRIG*i*(*i*=0~1) | I | External shutter trigger pulse |
| | ISP_FLASHTRIGIN*i*(*i*=0~1) | I | External flash trigger pulse |

### 2.8.8 EFUSE

Table 2-11 EFUSE pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| eFuse | EFUSE | N/A | eFuse program and sense power |

### 2.8.9 SAR-ADC

Table 2-12 SAR-ADC pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| SAR-ADC | ADC_IN[*i*](*i*=0~5) | N/A | SAR-ADC input signal for 3 channel |

### 2.8.10 TSADC

Table 2-13 TSADC pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| TSADC | TSADC_INT | O | TSADC interrupt signal for over temperature |

### 2.8.11 GMAC

Table 2-14 GMAC pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| GMAC | MAC_CLK | I/O | RMII REC_CLK output or GMAC external clock input |
| | MAC_TXCLK | O | RGMII TX clock output |
| | MAC_RXCLK | I | RGMII RX clock input |
| | MAC_MDC | O | GMAC management interface clock |
| | MAC_MDIO | I/O | GMAC management interface data |
| | MAC_TXD*i*(*i*=0~3) | O | GMAC TX data |
| | MAC_RXD*i*(*i*=0~3) | I | GMAC RX data |
| | MAC_TXEN | O | GMAC TX data enable |
| | MAC_RXDV | I | GMAC RX data valid signal |
| | MAC_RXER | I | GMAC RX error signal |
| | MAC_COL | I | PHY Collision signal |
| | MAC_CRS | I | PHY CRS signal |

### 2.8.12 UART

Table 2-15 UART pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| UART[*i*] *i*=0,3 | UART[*i*]_RX | I | UARTsearial data input |
| | UART[*i*]_TX | O | UARTsearial data output |
| | UART[*i*]_CTSN | I | UART clear to send |
| | UART[*i*]_RTSN | O | UART request to send |

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| UART[*i*] *i*=1,2,4 | UART[*i*]_RX | I | UARTsearial data input |
| | UART[*i*]_TX | O | UARTsearial data output |

*Note: UART2 is to be debug port by default.*

### 2.8.13 I2C

Table 2-16 I2C pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| I2C[*i*] *i*=0~8 | I2C[*i*]_SDA | I | I2C data line |
| | I2C[*i*]_SCL | O | I2C serial clock line |

### 2.8.14 PWM

Table 2-17 PWM pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| PWM | PWM0 | I/O | Pulse Width Modulation output |
| | PWM1 | I/O | Pulse Width Modulation output |
| | PWM2 | I/O | Pulse Width Modulation output |
| | PWM3_IR | I/O | Pulse Width Modulation output, special design for IR receiver |
| | VOP0_PWM | I/O | CABC PWM from VOP0 |
| | VOP1_PWM | I/O | CABC PWM from VOP1 |

### 2.8.15 CIF

Table 2-18 CIF pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| Camera IF | CIF_CLKIN | I | Camera interface input pixel clock |
| | CIF_CLKOUT | O | Camera interface output work clock |
| | CIF_CLKOUTB | O | Camera interface output work clock |
| | CIF_VSYNC | I | Camera interface vertical sync signal |
| | CIF_HREF | I | Camera interface horizontial sync signal |
| | CIF_D[*i*](*i*=0~7) | I | Camera interface input pixel data |

### 2.8.16 SPI

Table 2-19 SPI pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| SPI0 | SPI0_CLK | I/O | SPI serial clock |
| | SPI0_CSN0 | I/O | SPIfirstchip select signal,low active |
| | SPI0_CNS1 | I/O | SPIsecondchip select signal,low active |
| | SPI0_TXD | O | SPI serial data output |
| | SPI0_RXD | I | SPI serial data input |

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| SPI[*i*] *i*=1~5 | SPI[*i*]_CLK | I/O | SPI serial clock |
| | SPI[*i*]_CSN0 | I/O | SPIfirstchip select signal,low active |
| | SPI[*i*]_TXD | O | SPI serial data output |
| | SPI[*i*]_RXD | I | SPI serial data input |

### 2.8.17 SPDIF

Table 2-20 SPDIF pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| S/PDIF | SPDIF_TX | O | S/PDIFbiphase data ouput |

### 2.8.18 I2S

Table 2-21 I2S pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| I2S | I2S_CLK | O | I2S/PCM clock source, shared by I2S0 and I2S1 |

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| I2S0/PCM0 8 channels | I2S0_SCLK | I/O | I2S/PCM serial clock |
| | I2S0_LRCK_RX | I/O | I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | I2S0_LRCK_TX | I/O | I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | I2S0_SDI0 | I | I2S/PCM serial data input[0] |
| | I2S0_SDI1SDO3 | I | I2S/PCM serial data input[1] or output [3] |
| | I2S0_SDI2SDO2 | I | I2S/PCM serial data input [2] or output [2] |
| | I2S0_SDI3SDO1 | I | I2S/PCM serial data input [3] or output [1] |
| | I2S0_SDO0 | I | I2S/PCM serial data output [0] |

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| I2S1/PCM1 2 channels | I2S1_SCLK | I/O | I2S/PCM serial clock |
| | I2S1_LRCK_RX | I/O | I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | I2S1_LRCK_TX | I/O | I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | I2S1_SDI0 | I | I2S/PCM serial data input [0] |
| | I2S1_SDO0 | I | I2S/PCM serial data output [0] |

### 2.8.19 DDR Controller

Table 2-22 DDRC pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| DDR[*i*] Controller *(i=0,1)* | DDR[*i*]_ATB[*j*] (*j*=0,1) | O | Analog test bus signals |
| | DDR[*i*]_CLK[*j*]N DDR[*i*]_CLK[*j*]P (*j*=0~1) | O | Differential clock signal to the memory device |
| | DDR[*i*]_CKE[*j*] (*j*=0,1) | O | Active-high clock enable signal to the memory device for two chip select. |
| | DDR[*i*]_CSN[*j*] (*j*=0~3) | O | Active-low chip select signal to the memory device. There are two chip select. |
| | DDR[*i*]_RASN | O | Active-low row address strobe to the memory device. |
| | DDR[*i*]_CASN | O | Active-low column address strobe to the memory device. |
| | DDR[*i*]_WEN | O | Active-low write enable strobe to the memory device. |
| | DDR[*i*]_BA[2:0] | O | Bank address signal to the memory device. |
| | DDR[*i*]_A[15:0] | O | Address signal to the memory device. |
| | DDR[*i*]_DQ[31:0] | I/O | Bidirectional data line to the memory device. |

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| | DDR[*i*]_DQS[*j*]N[*j*=0~3] | I/O | Differential data strobes to/from the memories. For writes, thepad drives these signals. For reads, the memory drives thesesignals. |
| | DDR[*i*]_DQS[*j*]P[*j*=0~3] | I/O | |
| | DDR[*i*]_DM[3:0] | O | Active-low data mask signal to the memory device. |
| | DDR[*i*]_ODT[*j*](*j*=0,1) | O | On-Die Termination output signal for two chip select. |
| | DDR[*i*]_RESETN | O | DDR reset signal to the memory device |
| | DDR0_PLL_TESTOUT_P<br>DDR0_PLL_TESTOUT_N | O | DDR PLL test point |
| | DDR[*i*]_PZQ | I/O | ZQ calibration pad which connects 240ohm±1% resistor |

## 2.8.20 SDIO

Table 2-23 SDIO pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| SDIO Host Controller | SDIO0_CLKOUT | O | SDIO card clock. |
| | SDIO0_CMD | I/O | SDIO card command output and reponse input. |
| | SDIO0_D[0:3] | I/O | SDIOcard data input and output. |
| | SDIO0_DETN | I | SDIOcard detect signal, a 0 represents presence of card. |
| | SDIO0_WRPT | I | SDIOcard write protect signal, a 1 represents write is protected. |
| | SDIO0_PWREN | O | SDIOcard power-enable control signal |
| | SDIO0_INTN | O | SDIOcard interrupt indication |
| | SDIO0_BKPWR | O | the back-end power supply for embedded device |

## 2.8.21 SDMMC

Table 2-24 SDMMC pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| SD/MMC Host Controller | SDMMC0_CLKOUT | O | SDMMC card clock |
| | SDMMC0_CMD | I/O | SDMMCcard command output and reponse input |
| | SDMMC0_D[0:3] | I/O | SDMMCcard data input and output |
| | SDMMC0_WRPRT | I | SDMMC card protect |
| | SDMMC0_DET | I | SDMMCcard detect signal, a 0 represents presence of card |
| | SDMMC0_VDDPST | O | Pin out to external capacitor |

## 2.8.22 JTAG

Table 2-25 JTAG pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| AP JTAG | APJTAG_TCK | I | APJTAG interface clock input/SWD interface clock input |
| | APJTAG_TMS | I/O | APJTAG interface TMS input/SWD interface data out |

Note: AP means CPU core in RK3399 including Cortex A72 and Cortex A53.

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| MCU | MCUJTAG_TCK | I | MCUJTAG interface clock input/SWD interface clock input |

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| JTAG | MCUJTAG_TMS | I/O | MCUJTAG interface TMS input/SWD interface data out |

Note: MCU means built-in micro-controller in RK3399 core domain.

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| PMCU JTAG | PMCU_JTAG_TCK | I | PMU MCU JTAG interface clock input/SWD interface clock input |
| | PMCU_JTAG_TMS | I/O | PMU MCU JTAG interface TMS input/SWD interface data out |

Note: PMCU means built-in micro-controller in RK3399 PMU domain.

### 2.8.23 MISC

Table 2-26 MISC pin description

| Interface | Pin Name | Dir. | Description |
|---|---|---|---|
| Misc | XIN_OSC | I | Clock input of 24MHz crystal |
| | XOUT_OSC | O | Clock output of 24MHz crystal |
| | CLK32K | I | Clock input of 32.768KHz |
| | NPOR | I | Chip hardware reset |
| | AP_PWROFF | O | System power off control port (PMIC_SLEEP) |
| | WIFI_26MHZ | O | 26MHz clock out for WIFI chip |

# Chapter 3 Electrical Specification

## 3.1 Absolute Maximum Ratings

Table 3-1 Absolute maximum ratings

| Paramerters | Related Power Group | Max | Unit |
|---|---|---|---|
| DC supply voltage for Internal digital logic | BIGCPU_VDD,<br>LITCPU_VDD,<br>LOGIC_VDD,<br>CENTERLOGIC_VDD | 1.3 | V |
| DC supply voltage for DDR IO | DDR_VDD | 1.65 | V |
| Storage Temperature | Tstg | 125 | ℃ |
| Max Conjunction Temperature | Tj | 125 | ℃ |

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

## 3.2 Recommended Operating Conditions

The below table describes the recommended operating condition for every clock domain.

Table 3-2 Recommended operating conditions

| Parameters | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Supply voltage for Cortex A72 CPU | BIGCPU_VDD | 0.80 | 0.90 | 1.25 | V |
| Supply voltage for Cortex A53 CPU | LITCPU_VDD | 0.80 | 0.90 | 1.20 | V |
| Supply voltage for GPU | GPU_VDD | 0.80 | 0.90 | 1.20 | V |
| Internal digital logic Power | CENTERLOGIC_VDD<br>LOGIC_VDD | 0.8 | 0.9 | 1.0 | V |
| PMU digital logic power (0.9V) | PMU_VDD_0V9 | 0.81 | 0.9 | 0.99 | V |
| PMU digital logic power (1.8V) | PMU_VDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| EMMC power | EMMC_VDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| Supply voltage for digital GPIO@1.8V mode | PMUIO1_VDD_1V8<br>PMUIO2_VDDPST<br>PMUIO2_VDD<br>APIO2_VDDPST<br>APIO2_VDD<br>APIO3_VDD_1V8<br>APIO4_VDDPST<br>APIO4_VDD<br>APIO5_VDDPST<br>APIO5_VDD<br>SDMMC0_VDD | 1.62<br>1.71<br>1.71<br>1.71<br>1.71<br>1.62<br>1.71<br>1.71<br>1.71<br>1.71<br>1.71 | 1.8<br>1.8<br>1.8<br>1.8<br>1.8<br>1.8<br>1.8<br>1.8<br>1.8<br>1.8<br>1.8 | 1.98<br>1.89<br>1.89<br>1.89<br>1.89<br>1.98<br>1.89<br>1.89<br>1.89<br>1.89<br>1.89 | V |
| Supply voltage for digital GPIO@3.0V mode | PMUIO2_VDDPST<br>PMUIO2_VDD<br>APIO2_VDDPST<br>APIO2_VDD<br>APIO4_VDDPST | 1.425<br>2.85<br>1.425<br>2.85<br>1.425 | 1.5<br>3.0<br>1.5<br>3.0<br>1.5 | 1.575<br>3.15<br>1.575<br>3.15<br>1.575 | V |

| Parameters | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | APIO4_VDD | 2.85 | 3.0 | 3.15 | |
| | APIO5_VDDPST | 1.425 | 1.5 | 1.575 | |
| | APIO5_VDD | 2.85 | 3.0 | 3.15 | |
| | SDMMC0_VDD | 2.85 | 3.0 | 3.15 | |
| Supply voltage for digital GPIO@3.3V mode | APIO1_VDDPST | 1.71 | 1.8 | 1.89 | V |
| | APIO1_VDD | 3.135 | 3.3 | 3.465 | |
| Supply voltage for DDR0 / DDR1 | DDRPLL_AVDD_0V9 | 0.81 | 0.9 | 0.99 | V |
| | DDR_VDD@DDR3 | 1.425 | 1.5 | 1.575 | |
| | DDR_VDD@DDR3L | 1.28 | 1.35 | 1.42 | |
| | DDR_VDD@LPDDR3 | 1.14 | 1.2 | 1.3 | |
| | DDR_VDD@LPDDR4 | 1.06 | 1.1 | 1.17 | |
| | DDR_CLK_VDD@DDR3 | 1.425 | 1.5 | 1.575 | |
| | DDR_CLK_VDD@DDR3L | 1.28 | 1.35 | 1.42 | |
| | DDR_CLK_VDD@LPDDR3 | 1.14 | 1.2 | 1.3 | |
| | DDR_CLK_VDD@LPDDR4 | 1.06 | 1.1 | 1.17 | |
| Supply voltage for SAR-ADC | ADC_AVDD | 1.62 | 1.8 | 1.98 | V |
| Supply voltage for EFUSE | EFUSE | 1.62 | 1.8 | 1.98 | V |
| Supply voltage for PLL | PLL_AVDD_0V9 | 0.81 | 0.9 | 0.99 | V |
| | PLL_AVDD_1V8 | 1.62 | 1.8 | 1.98 | |
| Supply voltage for EDP | EDP_AVDD_0V9 | 0.81 | 0.9 | 0.99 | V |
| | EDP_AVDD_1V8 | 1.62 | 1.8 | 1.98 | |
| Supply voltage for EMMC | EMMC_COREDLL_0V9 | 0.81 | 0.9 | 0.99 | V |
| | EMMC_VDD_1V8 | 1.62 | 1.8 | 1.98 | |
| Supply voltage for HDMI | HDMI_AVDD_0V9 | 0.81 | 0.9 | 0.99 | V |
| | HDMI_AVDD_1V8 | 1.62 | 1.8 | 1.98 | |
| Supply voltage for MIPI | MIPI_TX0_AVDD_1V8<br>MIPI_TX1/RX1_AVDD_1V8<br>MIPI_RX0_AVDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| Supply voltage for PCIE | PCIE_AVDD_0V9 | 0.81 | 0.9 | 0.99 | V |
| | PCIE_AVDD_1V8 | 1.62 | 1.8 | 1.98 | |
| Supply voltage for TYPEC | TYPEC0_AVDD_0V9 | 0.81 | 0.9 | 0.99 | V |
| | TYPEC0_AVDD_1V8 | 1.62 | 1.8 | 1.98 | |
| | TYPEC0_AVDD_3V3 | 2.97 | 3.3 | 3.63 | |
| | TYPEC1_AVDD_0V9 | 0.81 | 0.9 | 0.99 | |
| | TYPEC1_AVDD_1V8 | 1.62 | 1.8 | 1.98 | |
| | TYPEC1_AVDD_3V3 | 2.97 | 3.3 | 3.63 | |
| Supply voltage for USIC | USIC_AVDD_0V9 | 0.81 | 0.9 | 0.99 | V |
| | USIC_AVDD_1V2 | 1.08 | 1.2 | 1.32 | |
| Supply voltage for USB | USB_AVDD_0V9 | 0.81 | 0.9 | 0.99 | V |
| | USB_AVDD_1V8 | 1.62 | 1.8 | 1.98 | |
| | USB_AVDD_3V3 | 2.97 | 3.3 | 3.63 | |
| PLL input clock frequency | | N/A | 24 | N/A | MHz |
| Max CPU frequency of A72 | | | | 1.8 | GHz |
| Max CPU frequency of A53 | | | | 1.4 | GHz |
| Max GPU frequency | | | | 800 | MHz |

| Parameters | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Ambient Operating Temperature [1)] | Ta | 0 | 25 | 80 | ℃ |

*Notes:*

1) Symbol name is same as the pin name in the IO descriptions

2) with the reference software setup, the reference software will limit the chipset temperature about 80℃

## 3.3 DC Characteristics

Table 3-3 DC Characteristics

| Parameters | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Digital GPIO @3.3V | Input Low Voltage | Vil | -0.3 | N/A | 0.8 | V |
| | Input High Voltage | Vih | 2.0 | N/A | 3.465 | V |
| | Output Low Voltage | Vol | N/A | N/A | 0.4 | V |
| | Output High Voltage | Voh | 2.4 | N/A | N/A | V |
| | Threshold Point | Vtr+ | 1 | 1.16 | 1.34 | V |
| | | Vtr- | 1.02 | 1.19 | 1.39 | V |
| | Pull up resistor | RPU | 26 | 46 | 71 | kΩ |
| | Pull down resistor | RPD | 27 | 48 | 102 | kΩ |
| Digital GPIO @1.8V | Input Low Voltage | Vil | -0.3 | N/A | 0.63 | V |
| | Input High Voltage | Vih | 1.17 | N/A | 1.98 | V |
| | Output Low Voltage | Vol | N/A | N/A | 0.45 | V |
| | Output High Voltage | Voh | 1.35 | N/A | N/A | V |
| | Threshold Point | Vtr+ | 0.82 | 0.9 | 1.0 | V |
| | | Vtr- | 0.84 | 0.91 | 1.0 | V |
| | Pull up resistor | RPU | 33 | 58 | 88 | kΩ |
| | Pull down resistor | RPD | 34 | 60 | 93 | kΩ |
| Digital GPIO @3.0V | Input Low Voltage | Vil | -0.3 | N/A | 0.71 | V |
| | Input High Voltage | Vih | 1.875 | N/A | 3.15 | V |
| | Output Low Voltage | Vol | N/A | N/A | 0.375 | V |
| | Output High Voltage | Voh | 2.25 | N/A | N/A | V |
| | Threshold Point | Vtr+ | 0.8 | 0.93 | 1.1 | V |
| | | Vtr- | 0.82 | 0.95 | 1.13 | V |
| | Pullup Resistor | RPU | 33 | 59 | 89 | kΩ |
| | Pulldown Resistor | RPD | 34 | 61 | 95 | kΩ |
| DDR IO | I/O supply voltage VIOS | DDR3 | 1.425 | 1.5 | 1.575 | V |
| | | DDR3L | 1.28 | 1.35 | 1.42 | V |
| | | LPDDR3 | 1.14 | 1.2 | 1.3 | V |
| | | LPDDR4 | 1.06 | 1.1 | 1.17 | V |
| | I/O output voltage VIOT | DDR3 | 0.49 | 0.50 | 0.51 | VIOS |
| | | DDR3L | 0.49 | 0.50 | 0.51 | VIOS |
| | | LPDDR3 | | 1 | | VIOS |
| | | LPDDR4 | | 0 | | |
| MIPI_DSI IO | HS TX static Common-mode voltage | VCMTX | 150 | 200 | 250 | mV |
| | VCMTX mismatch when output is Differential-1 or Differential-0 | \|ΔVCMTX(1,0)\| | N/A | N/A | 5 | mV |

| Parameters | | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | HS transmit differential voltage | \|VOD\| | 140 | 200 | 270 | mV |
| | VOD mismatch when output is Differential-1 or Differential-0 | \|ΔVOD\| | N/A | N/A | 14 | mV |
| | HS output high voltage | VOHHS | N/A | N/A | 360 | mV |
| | Single ended output impedance | ZOS | 40 | 50 | 62.5 | Ω |
| | Single ended output impedance mismatch | ΔZOS | N/A | N/A | 10 | % |
| HDMI | Single-ended standby voltage | Voff | avddtmds±10 | | | mV |
| | Single-ended output swing voltage RT=50Ω | Vswing | 400 | N/A | 600 | mV |
| | | Vswing_data | 400 | N/A | 600 | mV |
| | | Vswing_clock | 200 | N/A | 600 | mV |
| | Single-ended output high voltage | Vh | avddtmds±10 | | | mV |
| | | | avddtmds-200 | N/A | avddtmds+10 | mV |
| | | Vh_data | avddtmds-400 | N/A | avddtmds+10 | mV |
| | | Vh_clock | avddtmds-400 | N/A | avddtmds+10 | mV |
| | Single-ended output low voltage | Vl | avddtmds-600 | N/A | avddtmds-400 | mV |
| | | | avddtmds-700 | N/A | avddtmds-400 | mV |
| | | Vl_data | avddtmds-1000 | N/A | avddtmds-400 | mV |
| | | Vl_clock | avddtmds-1000 | N/A | avddtmds-200 | mV |
| | Differential source termination load | Rterm | 50 | N/A | 200 | Ω |

# 3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

| Parameters | | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Digital GPIO @3.3V | Input leakage current | Ii | Vin = 3.3V or 0V | N/A | N/A | 10 | uA |
| | Tri-state output leakage current | Ioz | Vout = 3.3V or 0V | N/A | N/A | 10 | uA |
| | High level output current | Oih | 25℃ | 6 | N/A | 63.8 | mA |
| | Low level output current | Oil | 25℃ | 4 | N/A | 38.5 | mA |
| Digital GPIO @1.8V | Input leakage current | Ii | Vin = 1.8V or 0V | N/A | N/A | 10 | uA |
| | Tri-state output leakage current | Ioz | Vout = 1.8V or 0V | N/A | N/A | 10 | uA |
| | High level output current | Oih | 25℃ | 3.7 | N/A | 24.6 | mA |
| | Low level output current | Oil | 25℃ | 4.8 | N/A | 26.1 | mA |
| | Input leakage current | Ii | Vin = 3.0V or 0V | N/A | N/A | 10 | uA |

| Parameters | | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Digital GPIO @3.0V | Tri-state output leakage current | Ioz | Vout = 3.0V or 0V | N/A | N/A | 10 | uA |
| | Pull up resistor | RPU | | | | | |
| | Pull down resistor | RPD | | | | | |
| | High level output current | Oih | 25℃ | 5.0 | N/A | 27.9 | mA |
| | Low level output current | Oil | 25℃ | 3.1 | N/A | 20.1 | mA |

# 3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for PLL

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Output frequency range | Fout | | 1 | N/A | 3200 | MHz |
| Lock time | Tlt | | N/A | 250 | 500 | Input clock cycles |
| Power consumption (normal mode) | N/A | FVCO=1GHz | N/A | 3 | N/A | mW |
| Period jitter (random) | N/A | VCO=3200MHz | N/A | NA | 0.11 | Ps(RMS) |
| Junction temperature | N/A | | N/A | 25 | 125 | ℃ |

# 3.6 Electrical Characteristics for SAR-ADC

Table 3-6 Electrical Characteristics for SAR-ADC

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| ADC resolution | | | N/A | 10 | N/A | bits |
| Clock frequency | fCLK | | N/A | N/A | 13 | MHz |
| Clock period | tCLK | | 75 | N/A | N/A | ns |
| Conversion time | Fs | | 13 | N/A | N/A | tCLK |
| Differential Non Linearity | DNL | | N/A | ±1 | N/A | LSB |
| Integral Nn Linearity | INL | | N/A | ±2 | N/A | LSB |
| Analog Supply Current | IAVDD | | N/A | 450 | N/A | uA |
| Digital Supply Current | IVDD | | N/A | 50 | N/A | uA |
| Power Down Current from AVDD | | | NA | 1 | NA | uA |
| Power Down Current from DVDD | | | N/A | 1 | N/A | uA |
| Setup up time | ts | | N/A | 0.5 | N/A | tCLK |

# 3.7 Electrical Characteristics for TSADC

Table 3-7 Electrical Characteristics for TSADC

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| ADC resolution | | | N/A | 10 | N/A | bits |
| TSADC Accuracy | Fs | | N/A | N/A | 5 | ℃ |
| Active power | | | N/A | 0.17 | N/A | mW |
| Clock Frequency | Fclk | | N/A | NA | 800 | KHz |

| | | | | | | |
|---|---|---|---|---|---|---|
| Power Down Current from DVDD | | | N/A | 1 | N/A | uA |

# 3.8 Electrical Characteristics for Type-C PHY

Table 3-8 Electrical Characteristics for Type-C PHY

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Transmitter | | | | | | |
| High input level | VIH | | NA | 1.0 | NA | V |

# 3.9 Electrical Characteristics for USB2.0 PHY

Table 3-9 Electrical Characteristics for USB2.0 PHY

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Transmitter | | | | | | |
| High input level | VIH | | NA | 1.0 | NA | V |
| Low input level | VIL | | NA | 0 | NA | V |
| Output resistance | ROUT | Classic mode (Vout = 0 or 3.3V) | 40.5 | 45 | 49.5 | ohms |
| | | HS mode (Vout = 0 to 800mV) | 40.5 | 45 | 49.5 | ohms |
| Output Capacitance | COUT | seen from D+ or D- | | | 3 | pF |
| Output Common Mode Voltage | VM | Classic (LS/FS) mode | 1.45 | 1.65 | 1.85 | V |
| | | HS mode | 0.175 | 0.2 | 0.225 | V |
| Differential output signal high | VOH | Classic (LS/FS); Io=0mA | 2.97 | 3.3 | 3.63 | V |
| | | Classic (LS/FS); Io=6mA | 2.2 | 0.3 | NA | V |
| | | HS mode; Io=0mA | 360 | 400 | 440 | mV |
| Differential output signal low | VOL | Classic (LS/FS); Io=0mA | -0.33 | 0 | 0.33 | V |
| | | Classic (LS/FS); Io=6mA | NA | 0.3 | 0.8 | V |
| | | HS mode; Io=0mA | -40 | 0 | 40 | mV |
| Receiver | | | | | | |
| Receiver sensitivity | RSENS | Classic mode | | +-250 | | mV |
| | | HS mode | | +-25 | | mV |
| Receiver common mode | RCM | Classic mode | 0.8 | 1.65 | 2.5 | V |
| | | HS mode (differential and squelch comparator) | 0.1 | 0.2 | 0.3 | V |
| | | HS mode (disconnect comparator) | 0.5 | 0.6 | 0.7 | V |

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input capacitance (seen at D+ or D-) | | | NA | NA | 3 | pF |
| Squelch threshold | | | 100 | 112 | 150 | mV |
| Disconnect threshold | | | 570 | 590 | 625 | mV |
| High output level | VOH | | NA | 3.3 | NA | V |
| Low output level | VOL | | NA | 0 | NA | V |

## 3.10 Electrical Characteristics for DDR IO

Table 3-10 Electrical Characteristics for DDR IO

| Parameters | | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| DDR IO @DDR3 mode | Input leakage current | | @ 1.5V | -2 | N/A | 2 | uA |
| DDR IO @DDR3L mode | Input leakage current | | @ 1.35V | -2 | N/A | 2 | uA |
| DDR IO @LPDDR3 mode | Input leakage current | | @ 1.2V | -2 | N/A | 2 | uA |
| DDR IO @LPDDR4 mode | Input leakage current | | @ 1.1V | -2 | N/A | 2 | uA |

## 3.11 Electrical Characteristics for eFuse

Table 3-11 Electrical Characteristics for eFuse

| | Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Active mode | VDD current in Read mode | Iread_vdd | nomal read | N/A | 9 | N/A | mA |
| | VDD current in PGM mode | Ipgm_vdd | STROBE high | N/A | 17 | N/A | mA |
| | VQPS current in PGM mode | Ipgm_vqps | STROBE high | N/A | 0.2 | N/A | uA |
| standby mode | VDD current in standby mode | Istandby_vdd | Standby | N/A | 10 | N/A | uA |

## 3.12 Electrical Characteristics for HDMI

Table 3-12 Electrical Characteristics for HDMI

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Differential output signal rise time | tR | 20~80% RL=50Ω | 75 | N/A | 0.4UI | ps |
| | tR_DATA | 20~80% RL=50Ω | 42.5 | N/A | N/A | ps |
| | tR_CLOCK | 20~80% RL=50Ω | 75 | N/A | N/A | ps |
| Differential output signal fall time | tF | 20~80% RL=50Ω | 75 | N/A | N/A | ps |
| | tF_DATA | 20~80% RL=50Ω | 42.5 | N/A | N/A | ps |
| | tF_CLOCK | 20~80% | 75 | N/A | N/A | ps |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | RL=50Ω | | | | |

## 3.13 Electrical Characteristics for MIPI PHY

Table 3-13 Electrical Characteristics for MIPI PHY

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| HS Transmitter AC specifications (MIPI mode) | | | | | | |
| Common-mode variations above 450 MHz | ΔVCMTX(HF) | | N/A | N/A | 15 | mVRMS |
| Common-mode variations between 50MHz – 450MHz | ΔVCMTX(LF) | | N/A | N/A | 25 | mVPEAK |
| 20%-80% rise time and fall time | TR and TF | | 100 | N/A | N/A | ps |
| HS Receiver AC specifications (MIPI mode) | | | | | | |
| Common-mode interference beyond 450 MHz | ΔVCMRX(HF) | | N/A | N/A | 200 | mV |
| Common-mode interference | ΔVCMRX(LF) | | -50 | NA | 50 | mV |
| Common-mode termination | CCM | | N/A | N/A | 60 | pF |
| LP receiver AC specifications(MIPI mode) | | | | | | |
| Input pulse rejection | eSPIKE | | N/A | N/A | 300 | V.ps |
| Minimum pulse width response | TMIN-RX | | 20 | N/A | N/A | ns |
| Peak interference amplitude | VINT | | N/A | N/A | 400 | mV |
| Interference frequency | fINT | | 450 | N/A | N/A | MHz |
| LP Transmitter AC Specifications(MIPI mode) | | | | | | |
| 15%-85% rise time and fall time | TRLP/TFLP | | N/A | N/A | 25 | ns |
| 30%-85% rise time and fall time | TREOT | | N/A | N/A | 35 | ns |
| Slew rate | δV/δtSR | | N/A | N/A | 150 | mV/ns |
| Load capacitance | CLOAD | | 0 | N/A | 70 | pF |

## 3.14 Electrical Characteristics for eMMC PHY

Table 3-14 Electrical Characteristics for eMMC PHY

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input leakage current | | | N/A | 12 | N/A | pA |
| Tri-state output leakage current | | | N/A | 10 | N/A | pA |

## 3.15 Electrical Characteristics for PCIe PHY

Table 3-15 Electrical Characteristics for PCIe PHY

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Transmitter | | | | | | |
| Unit Interval | UI | 2.5GT/s | 399.88 | N/A | 400.12 | ps |
| Differential p-pTx voltage swing | $V_{TX-DIFF-PP}$ | 2.5GT/s | 0.8 | N/A | 1.2 | V |
| Low power differential p-p Tx voltage swing | $V_{TX-DIFF-PP-LOW}$ | 2.5GT/s | 0.4 | N/A | 1.2 | V |

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Tx de-emphasis level ratio | $V_{TX-DE-RATIO-3.5dB}$ | 2.5GT/s | 3.0 | N/A | 4.0 | dB |
| Transmitter Eye including all jitter sources | $T_{TX-EYE}$ | 2.5GT/s | 0.75 | N/A | N/A | UI |
| Maximum time between the jitter median and max deviation from the median | $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | 2.5GT/s | N/A | N/A | 0.125 | UI |
| Transmitter rise and fall time | $T_{TX-RISE-FALL}$ | 2.5GT/s | 0.125 | N/A | N/A | UI |
| Tx package plus Si differential return loss | $RL_{TX-DIFF}$ | 2.5GT/s | 10 | N/A | N/A | dB |
| Tx package plus Si common mode return loss | $RL_{TX-CM}$ | 2.5GT/s | 6 | N/A | N/A | dB |
| Tx AC common mode voltage | $V_{TX-CM-AC-P}$ | 2.5GT/s | 20 | N/A | N/A | mV |
| Transmitter short-circuit current limit | $I_{TX-SHORT}$ | 2.5GT/s | N/A | N/A | 90 | mA |
| Transmitter DC common-mode voltage | $V_{TX-DC-CM}$ | 2.5GT/s | 0 | N/A | 3.6 | V |
| Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle. | $V_{TX-CM-DC-ACTIVEIDLE-DELTA}$ | 2.5GT/s | 0 | N/A | 100 | mV |
| Electrical Idle Differential Peak Output Voltage | $V_{TX-IDLE-DIFF-AC-p}$ | 2.5GT/s | 0 | N/A | 20 | mV |
| The amount of voltage change allowed during Receiver Detection | $V_{TX-RCV-DETECT}$ | 2.5GT/s | N/A | N/A | 600 | mV |
| Minimum time spent in Electrical Idle | $T_{TX-IDLE-MIN}$ | 2.5GT/s | 20 | N/A | N/A | ns |
| Maximum time to transition to a valid Electrical Idle after sending an EIOS | $T_{TX-IDLE-SET-TOIDLE}$ | 2.5GT/s | N/A | N/A | 8 | ns |
| Maximum time to transition to valid diff signaling after leaving Electrical Idle | $T_{TX-IDLE-TO-DIFFDATA}$ | 2.5GT/s | N/A | N/A | 8 | ns |
| Crosslink random timeout | $T_{CROSSLINK}$ | 2.5GT/s | N/A | N/A | 1.0 | ms |
| AC Coupling Capacitor | $C_{TX}$ | 2.5GT/s | 75 | N/A | 200 | nF |
| Receiver | | | | | | |
| Unit Interval | UI | 2.5GT/s | 399.88 | N/A | 400.12 | ps |
| Differential Rx peak-peak voltage for common Refclk Rx architecture | $V_{RX-DIFF-PP-CC}$ | 2.5GT/s | 0.175 | N/A | 1.2 | V |
| Differential Rx peak-peak voltage for data clocked Rx architecture | $V_{RX-DIFF-PP-DC}$ | 2.5GT/s | 0.175 | N/A | 1.2 | V |
| Receiver eye time opening | $T_{RX-EYE}$ | 2.5GT/s | 0.40 | N/A | N/A | UI |
| Max time delta between median | $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ | 2.5GT/s | 0.3 | N/A | N/A | UI |

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| and deviation from median | | | | | | |
| Rx AC common mode voltage | $V_{RX-CM-AC-P}$ | 2.5GT/s | N/A | N/A | 150 | mVP |
| Rx package plus Si differential return loss | $RL_{RX-DIFF}$ | 2.5GT/s | 10 | N/A | N/A | dB |
| Common mode Rx return loss | $RL_{RX-CM}$ | 2.5GT/s | 6 | N/A | N/A | dB |
| DC differential impedance | $Z_{RX-DIFF-DC}$ | 2.5GT/s | 80 | N/A | 120 | Ω |
| Receiver DC single ended impedance | $Z_{RX-DC}$ | 2.5GT/s | 40 | N/A | 60 | Ω |
| Electrical Idle Detect Threshold | $V_{RX-IDLE-DET-DIFF-p-p}$ | 2.5GT/s | 65 | N/A | 175 | mV |
| Unexpected Electrical Idle Enter Detect Threshold Integration Time | $T_{RX-IDLE-DET-DIFFENTERTIME}$ | 2.5GT/s | N/A | N/A | 10 | ms |
| Lane to Lane skew | $L_{RX-SKEW}$ | 2.5GT/s | N/A | N/A | 20 | ns |

# Chapter 4 Thermal Management

## 4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

## 4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package. The resulting simulation data for reference only, please prevail in kindtest.

Table 4-1 Thermal Resistance Characteristics

| Package (TFBGA) | Power(W) | $\theta_{JA}(℃/W)$ | $\theta_{JB}(℃/W)$ | $\theta_{JC}(℃/W)$ |
|---|---|---|---|---|
| RK3399 | 6.05 | 12.39 | 7.7 | 0.38 |

*Note: The testing JEDEC PCB is based on 6 layers, 114.3x101.6 mm, 1.6 mm Thickness, ambient temperature is 25℃.*